# TITLE : HV070WS1-101

# Preliminary Product Specification

**HYDIS Technologies**

# REVISION HISTORY

| REV. | ECN NO. | DESCRIPTION OF CHANGES | DATE | PREPARED |
|---|---|---|---|---|
| P0 | | ▪ Initial Release | 11. 05.02 | J.I.MOON |
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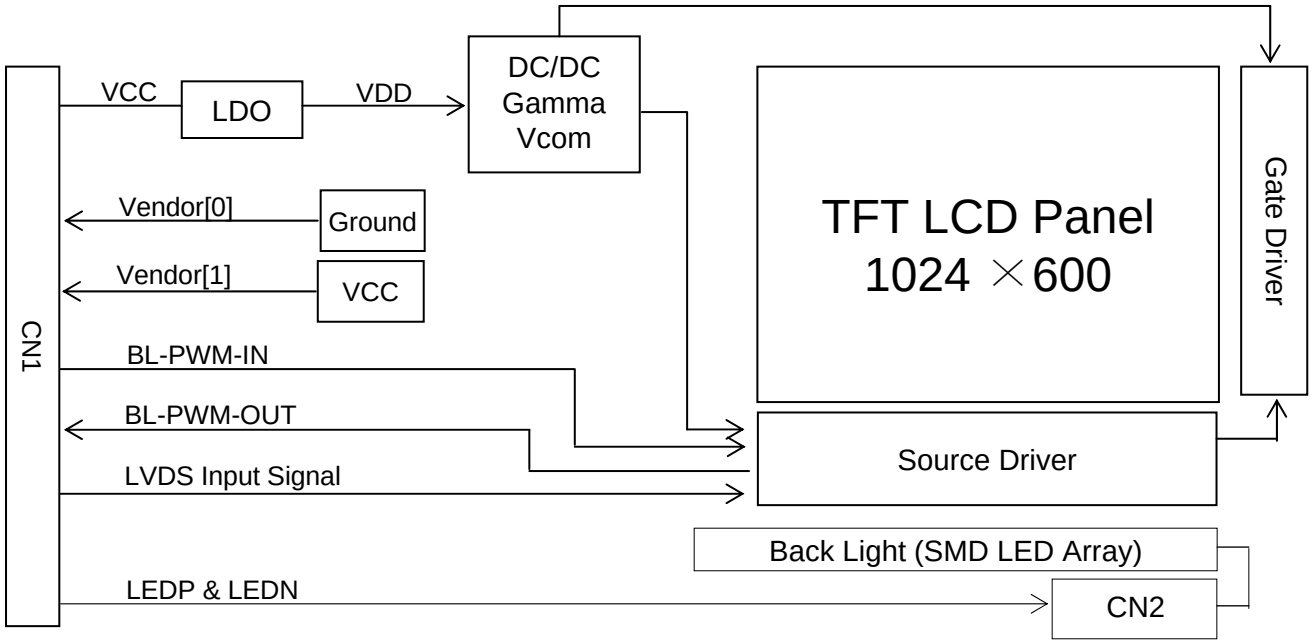
# Contents

# 1.0 GENERAL DESCRIPTION

## 1.1 Introduction

HV070WS1-101 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 7.01 inch diagonally measured active area with WSVGA resolutions (1024 horizontal by 600 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is a low reflection and higher color type.




## 1.2 Features

- FAB site : HYDIS Korea
- Thin and Light Weight
- 3.3 V Logic Power & 16 V Back-light power Supply
- 1 Channel LVDS Interface
- SMD LED (20EA) Array (Bottom Side/Horizontal Direction)
- 16.7M Colors (With Dither & HFRC)
- Need SPI control (CSB, SCL, SDA) for module driving
- Green Product (RoHS) & Halogen free

### 1.3 Application

- E-book, etc

### 1.4 General Specifications

< Table 1. General Specifications >

| Parameter | Specification | Unit | Remark |
|---|---|---|---|
| Active area | 153.6(H) ×90.0(V) | mm | |
| Number of pixels | 1024(H) ×600(V) | pixels | |
| Pixel pitch | 0.15(H) ×0.15(V) | mm | |
| Pixel arrangement | RGB Vertical Stripe | | |
| Display colors | 16.7M | colors | Note 1 |
| Display mode | Normally Black | | |
| Outline dimension | 163.6±0.3(H)×102.9±0.3(V)× 2.47±0.2(D) | mm | Note 2 |
| Weight | 95 (Max.) | g | |
| Back-light | Bottom edge side, 20-LEDs type | | |

Note 1 : Support 16.7M with dither and HFRC

Note 2 : Without component
Horizontal outline dimension is some different to customer request which is
162.8±0.3(H)×102.9±0.3(V)× 2.47±0.2(D)
But outline dimension is confirm value between Hydis and Customer

## 2.0 ABSOLUTE MAXIMUM RATINGS

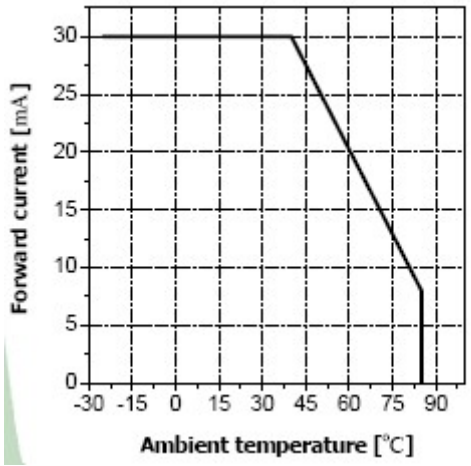
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

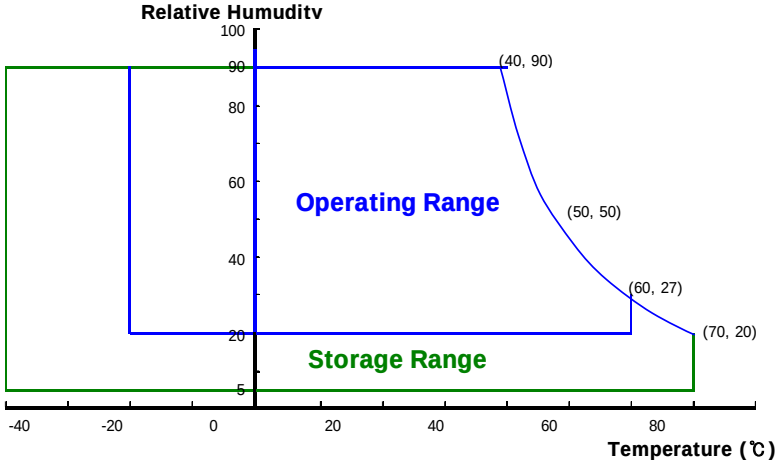
< Table 2. Absolute Maximum Ratings > Ta=25+/-2°C

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Logic Power Supply Voltage | $V_{CC}$ | -0.3 | $V_{CC}$+0.3 | V | |
| Back-light Power Supply Voltage | $V_L$ | -0.3 | 40 | V | |
| Back-light LED Current | $I_L$ | - | 30 | mA | Note 1 |
| Back-light LED Reverse Voltage | $V_R$ | - | 5 | V | |
| Operating Temperature | $T_{OP}$ | -20 | +60 | ℃ | Note 1, Note 2 |
| Storage Temperature | $T_{SP}$ | -40 | +70 | ℃ | |

Note 1. Ambient temperature vs allowable forward current are shown in the figure below.

Note 2. Temperature and relative humidity range are shown in the figure below.
90% RH Max. ( 40℃ ≥ Ta)
Maximum wet - bulb temperature at 39℃ or less. ( > 40℃) No condensation.



# 3.0 ELECTRICAL SPECIFICATIONS

## 3.1 Electrical Specifications

< Table 3. Electrical Specifications >

| Parameter | | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Logic Power Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | Note 1 |
| Logic Power Supply Current | $I_{CC}$ | - | TBD | 290 | mA | |
| Logic Power Consumption | $P_C$ | | TBD | 0.96 | W | |
| Back-light Power Supply Voltage | $V_L$ | - | 16 | 17 | V | Note 2 |
| Back-light Power Supply Current | $I_L$ | - | 20 | 25 | mA | |
| Back-light Power Consumption | $P_{BL}$ | - | - | 1.36 | W | Note 2, 4 |
| Back-light PWM Frequency | $F_{PWM}$ | - | TBD | - | KHz | CABC Off mode |
| Back-light PWM Frequency | $F_{PWM}$ | - | TBD | - | KHz | CABC On mode |
| High Level PWM Signal Voltage | $V_{PWMH}$ | - | TBD | - | V | |
| Low Level PWM Signal Voltage | $V_{PWML}$ | - | TBD | - | V | |
| High Level Differential Input Signal ($V_{CM}$ = 1.2V) | $V_{TH}$ | - | - | 0.1 | V | LVDS input |
| Low Level Differential Input Signal | $V_{TL}$ | - 0.1 | - | - | V | |
| Input voltage range (singled-end) | $V_{IN}$ | 0 | - | 2.4 | V | |
| Differential input voltage | $\lvert V_{ID} \rvert$ | 0.1 | - | 0.6 | V | |
| Differential input common mode voltage | $V_{CM}$ | ( $\lvert V_{ID} \rvert$ /2) | | 2.4- ( $\lvert V_{ID} \rvert$ /2) | V | |
| Input Current | $V_{IN}$ | -10 | - | -10 | μA | |
| Panel unit life time | | 50,000 | - | - | Hrs | Without BL,PCB |
| Total Power Consumption | $P_{total}$ | - | - | 2.32 | W | Note 1,2,4 |

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The logic current draw and power consumption specified is for 3.3V at 25℃.
a) Typ : Window XP pattern, b) Max : White pattern

2. The supply voltage is measured and specified at the interface connector of LCM.
The Backlight current draw and power consumption specified is 16V at 25℃.
The voltage and current value means value for chain.

3. PWM frequency and voltage level is fixed by customer.

4. Backlight power consumption is calculated value for reference ($V_L$ × $I_L$ × 4 chains).
About maximum power of backlight is 16V × 25mA × 4 chains = 1.36W

### 3.2 PWM Duty Ratio vs Brightness

**TBD**

# 4.0 OPTICAL SPECIFICATIONS

## 4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of Θ and Φ equal to 0°. We refer to $\Theta_{Ø=0}$ (=Θ3 ) as the 3 o'clock direction (the "right"), $\Theta_{Ø=90}$ (= Θ12 ) as the 12 o'clock direction ("upward"), $\Theta_{Ø=180}$ (= Θ9 ) as the 9 o'clock direction ("left") and $\Theta_{Ø=270}$(= Θ6 ) as the 6 o'clock direction ("bottom"). While scanning Θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. $V_{CC}$ shall be 3.3+/- 0.3V at 25°C.

## 4.2 Optical Specifications

<Table 4. Optical Specifications>

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle range | Horizontal | $\Theta_3$ | CR > 10 | 75 | 85 | | Deg. | Note 1 |
| | | $\Theta_9$ | | 75 | 85 | | Deg. | |
| | Vertical | $\Theta_{12}$ | | 75 | 85 | | Deg. | |
| | | $\Theta_6$ | | 75 | 85 | | Deg. | |
| Luminance Contrast ratio | | CR | Θ = 0° | 640 | 800 | - | | Note 2 |
| Luminance of White | 1 Points | $Y_w$ | Θ = 0° | | 30 (CTF) | | $cd/m^2$ | Note 4 |
| | | | | 340 | 400 (CTF) | - | $cd/m^2$ | |
| White Luminance uniformity | 9 Points | Δ Y9 | | 72 | 80 | - | % | Note 5 |
| White Chromaticity | | $W_x$ | Θ = 0° | 0.280 | 0.301 | 0.340 | | Note 3 |
| | | $W_y$ | | 0.310 | 0.330 | 0.370 | | |
| Reproduction of color | Red | $R_x$ | Θ = 0° | 0.563 | 0.593 | 0.623 | | |
| | | $R_y$ | | 0.323 | 0.353 | 0.383 | | |
| | Green | $G_x$ | | 0.283 | 0.313 | 0.343 | | |
| | | $G_y$ | | 0.559 | 0.589 | 0.619 | | |
| | Blue | $B_x$ | | 0.121 | 0.151 | 0.181 | | |
| | | $B_y$ | | 0.099 | 0.129 | 0.159 | | |
| Response Time | | Total ($T_r + T_d$) | Ta= 25° C Θ = 0° | - | 50 | - | ms | Note 6 |
| Cross Talk | | CT | Θ = 0° | - | - | 2.0 | % | Note 7 |

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure1).

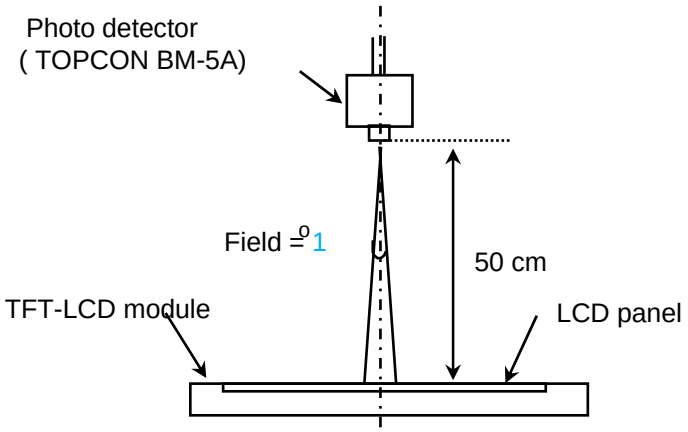
2. Contrast measurements shall be made at viewing angle of Θ = 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (see Figure1). Luminance Contrast Ratio (CR) is defined mathematically as CR = Luminance when displaying a white raster / Luminance when displaying a black raster.

3. Reference only / Standard Front Surface Treatment Measured with green cover glass. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

4. The luminance value of 400 cd/m2 means the brightness of PWM is 100%. The luminance value of 30 cd/m2 means the brightness of lower PWM. CTF means that measure brightness at only center point at Figure 2.

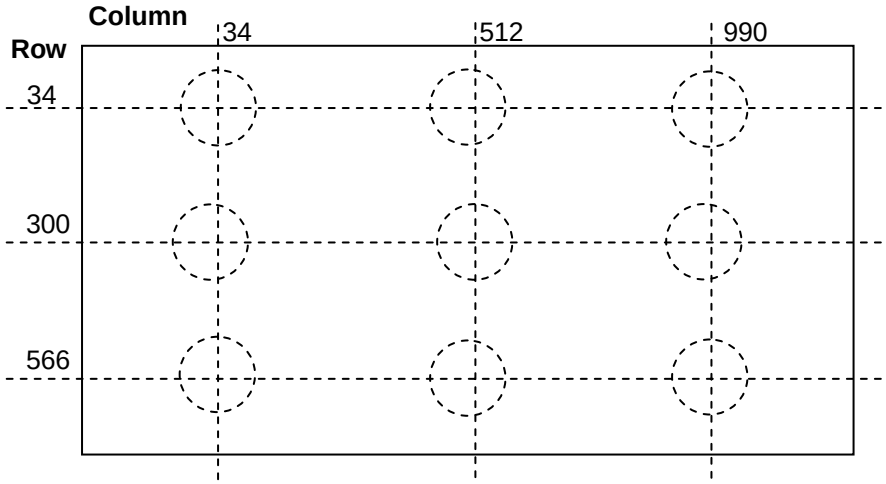
### 4.3 Optical Measurements

**Figure 1. Measurement Set Up**




Optical characteristics measurement setup

**Figure 2. Uniformity Measurement Locations (9 points)**




Note 5.
The White luminance uniformity on LCD surface is then expressed as :
ΔY = ( Minimum Luminance of 9 points / Maximum Luminance of 9 points ) * 100
Refer Figure 2 about measurement points

* LED Condition = (Duty Ratio 100%, LED current 20mA)

**Figure 3. Response Time Testing**

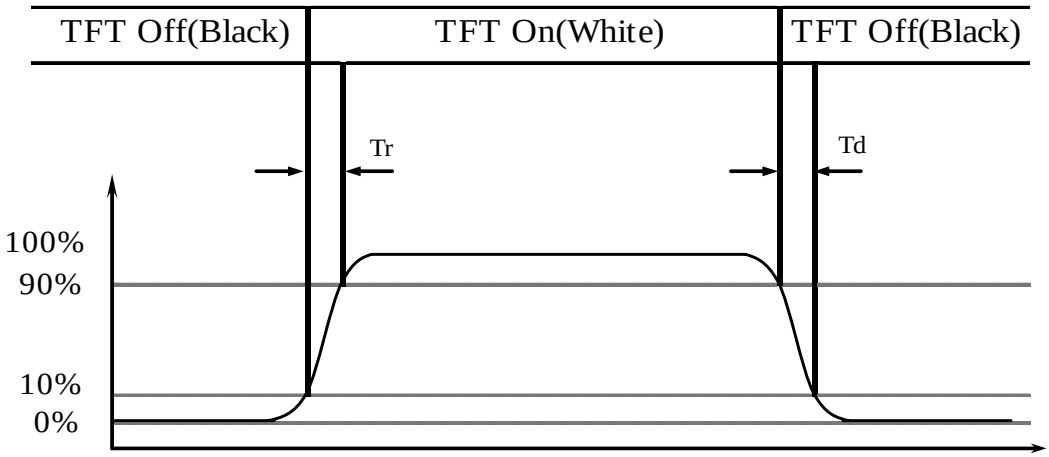
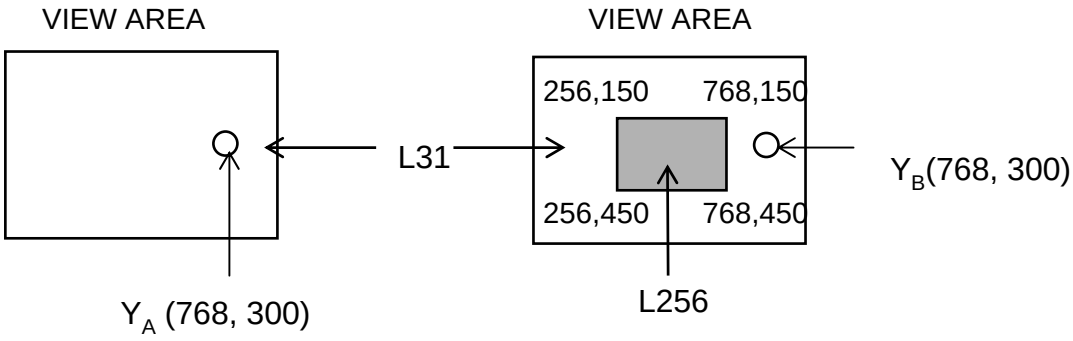


**Figure 4. Cross Modulation Test Description**




$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Where:

$Y_A$ = Initial luminance of measured area (cd/m$^2$)

$Y_B$ = Subsequent luminance of measured area (cd/m$^2$)

The location measured will be exactly the same in both patterns

Note 6.

The electro-optical response time measurements shall be made as Figure 3 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Note 7.

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to Figure 4).

# 5.0 INTERFACE CONNECTIONS

## 5.1 Electrical Interface Connection

### CN1 Interface Connector (AA01B-P030VA1, Manufactured by JAE)

<Table 5, Electrical Interface Connection >

| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
|---|---|---|---|---|---|
| 1 | VCC | +3.3V Power Supply | 16 | D1-IN-N | LDVS differential data input |
| 2 | GND | Ground | 17 | Vendor[1] | Vendor distinguish pin 2 |
| 3 | VCC | +3.3V Power Supply | 18 | D1-IN-P | LDVS differential data input |
| 4 | CLK-IN-N | LVDS Clock input (Negative) | 19 | CSB | Serial Communication Chip Select |
| 5 | VCC | +3.3V Power Supply | 20 | GND | Ground |
| 6 | CLK-IN-P | LVDS Clock input (Positive) | 21 | SCL | Serial Communication Clock Input |
| 7 | GND | Ground | 22 | D2-IN-N | LDVS differential data input |
| 8 | GND | Ground | 23 | SDA | Serial Communication Data Input |
| 9 | LEDP | Power supply for LED [Anode] | 24 | D2-IN-P | LDVS differential data input |
| 10 | D0-IN-N | LDVS differential data input | 25 | GND | Ground |
| 11 | LEDN | Power supply for LED [Cathode] | 26 | GND | Ground |
| 12 | D0-IN-P | LDVS differential data input | 27 | BL-PWM-IN | Brightness Control Signal |
| 13 | GND | Ground | 28 | D3-IN-N | LDVS differential data input |
| 14 | GND | Ground | 29 | BL-PWM-OUT | Backlight Dimmer Signal |
| 15 | Vendor[0] | Vendor distinguish pin 1 | 30 | D3-IN-P | LDVS differential data input |

## 5.2 LVDS Interface

**LVDS Transmitter :** THC63LVDM83A

<Table 6, LVDS Interface >

| Input signal | Transmitter | | Interface | | AA01B-P030VA1 | Remark |
|---|---|---|---|---|---|---|
| | Pin No | Pin No | System (Tx) | TFT-LCD (Rx) | Pin No. | |
| R0 | 51 | 48<br>47 | OUT0-<br>OUT0+ | D0-IN-N<br>D0-IN-P | 10<br>12 | |
| R1 | 52 | | | | | |
| R2 | 54 | | | | | |
| R3 | 55 | | | | | |
| R4 | 56 | | | | | |
| R5 | 3 | | | | | |
| G0 | 4 | | | | | |
| G1 | 6 | 46<br>45 | OUT1-<br>OUT1+ | D1-IN-N<br>D1-IN-P | 16<br>18 | |
| G2 | 7 | | | | | |
| G3 | 11 | | | | | |
| G4 | 12 | | | | | |
| G5 | 14 | | | | | |
| B0 | 15 | | | | | |
| B1 | 19 | | | | | |
| B2 | 20 | 42<br>41 | OUT2-<br>OUT2+ | D2-IN-N<br>D2-IN-P | 22<br>24 | |
| B3 | 22 | | | | | |
| B4 | 23 | | | | | |
| B5 | 24 | | | | | |
| HSYNC | 27 | | | | | |
| VSYNC | 28 | | | | | |
| DE | 30 | | | | | |
| R6 | 50 | 38<br>37 | OUT3-<br>OUT3+ | D3-IN-N<br>D3-IN-P | 28<br>30 | |
| R7 | 2 | | | | | |
| G6 | 8 | | | | | |
| G7 | 10 | | | | | |
| B6 | 16 | | | | | |
| B7 | 18 | | | | | |
| Reserved | 25 | | | | | |
| MCLK | 31 | 40 | CLKOUT- | CLK-IN-N | 4 | |
| | | 39 | CLKOUT+ | CLK-IN-P | 6 | |

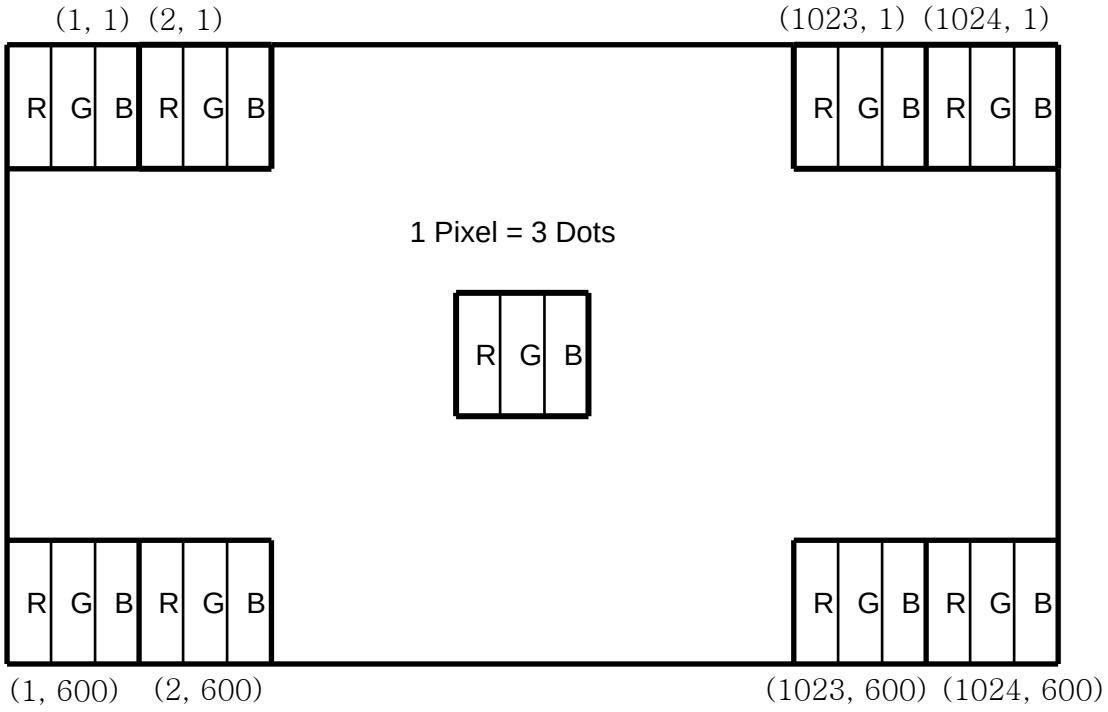
### 5.3 Back-light Interface

CN2 LED FPC Connector ( solder type **)**

<Table 7, LED FPC connection >

| Pin No. | Symbol | Function | Remark |
|---|---|---|---|
| 1 | Anode1 | LED Anode Power Supply | Typ. 16V |
| 2 | | | |
| 3 | Cathode1 | LED Cathode Power Supply | |
| 4 | | LED Cathode Power Supply | |

### 5.4 Data Input Format



# 6.0. SIGNAL TIMING SPECIFICATIONS

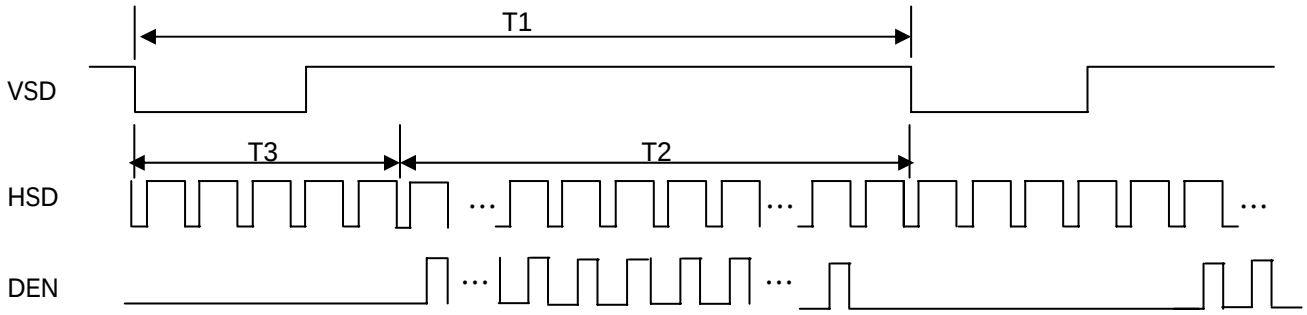
## 6.1 Timing specification at HV Mode (LVDS Transmitter Input)

<Table 8, Signal Timing >

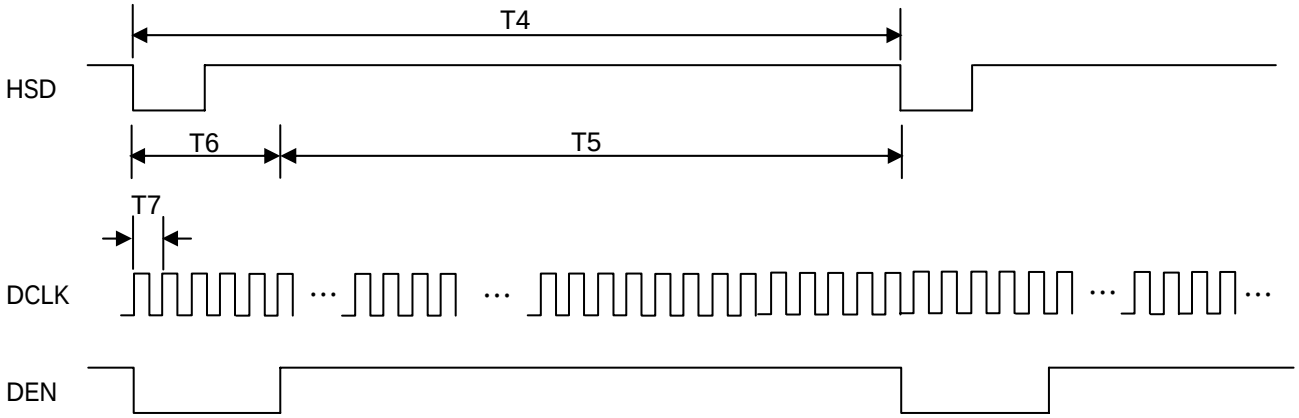
| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Frame Rate | - | 40 | 60 | 73 | Hz |
| Frame Period | T1 | 624 | 635 | 750 | Lines |
| Vertical Display Time | T2 | - | 600 | - | Lines |
| Vertical Blanking Time | T3 | - | 35 | - | Lines |
| 1 Line Scanning Time | T4 | 1200 | 1344 | 1400 | Clocks |
| Horizontal Display Time | T5 | - | 1024 | - | Clocks |
| Horizontal Blanking Time | T6 | - | 320 | - | Clocks |
| Clock Rate | 1/T7 | 40.8 | 51.2 | 63 | MHz |

# 7.0 SIGNAL TIMING WAVEFORMS

## 7.1 Vertical Input Timing Waveforms of Interface Signal




## 7.2 Horizontal Input Timing Waveforms of Interface Signal

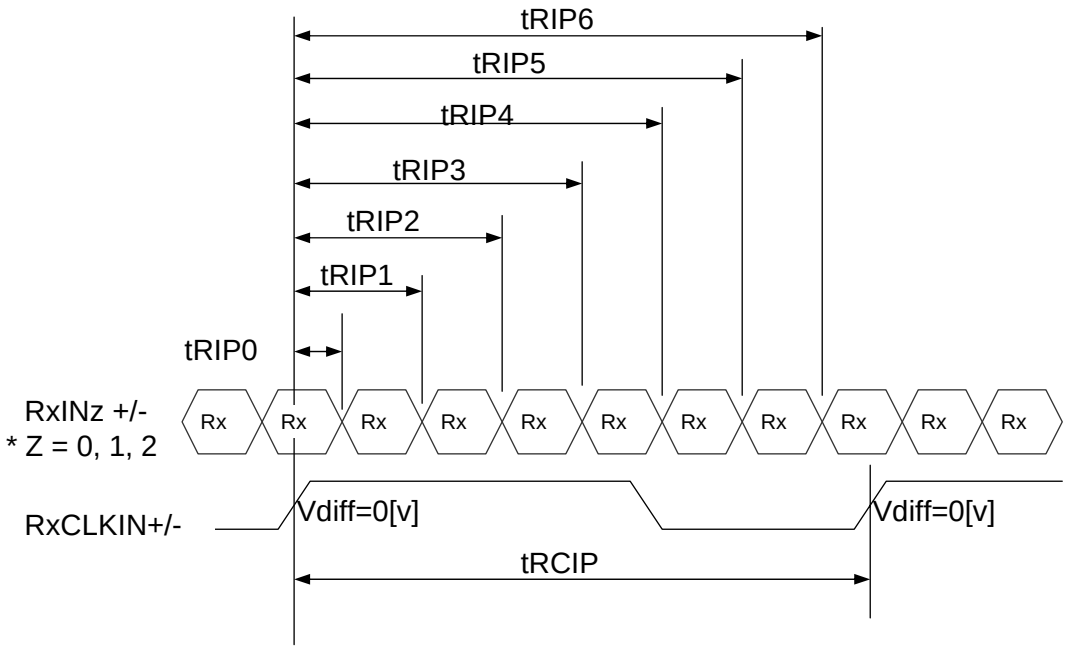


### 7.3 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter

< Table 9, LVDS Rx Interface Timing Specification>

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| CLKIN Period | tRCIP | - | 19.53 | - | nsec | |
| Input Data 0 | tRIP0 | -0.4 | 0.0 | +0.4 | nsec | |
| Input Data 1 | tRIP1 | tRICP/7-0.4 | tRICP/7 | tRICP/7+0.4 | nsec | |
| Input Data 2 | tRIP2 | 2 ×tRICP/7-0.4 | 2 ×tRICP/7 | 2 ×tRICP/7+0.4 | nsec | |
| Input Data 3 | tRIP3 | 3 ×tRICP/7-0.4 | 3 ×tRICP/7 | 3 ×tRICP/7+0.4 | nsec | |
| Input Data 4 | tRIP4 | 4 ×tRICP/7-0.4 | 4 ×tRICP/7 | 4 ×tRICP/7+0.4 | nsec | |
| Input Data 5 | tRIP5 | 5 ×tRICP/7-0.4 | 5 ×tRICP/7 | 5 ×tRICP/7+0.4 | nsec | |
| Input Data 6 | tRIP6 | 6 ×tRICP/7-0.4 | 6 ×tRICP/7 | 6 ×tRICP/7+0.4 | nsec | |



## 8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

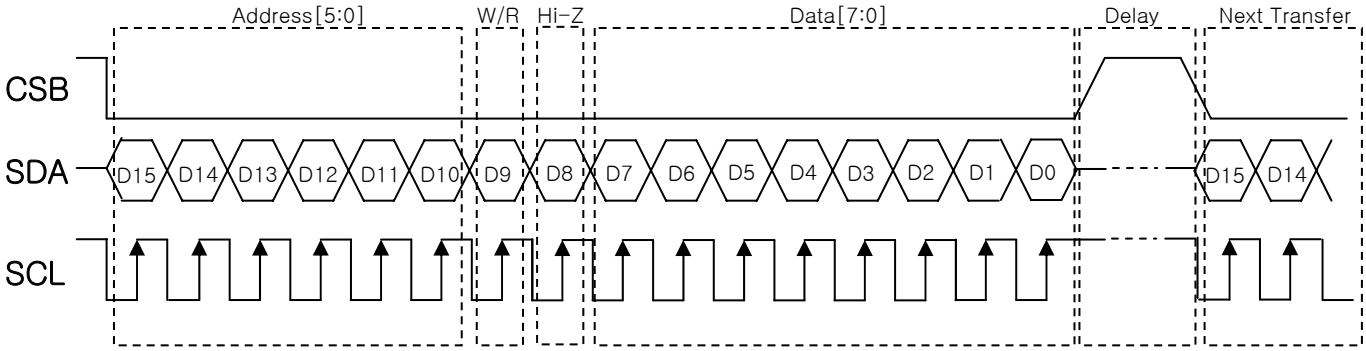
A total of 16.7M colors are displayed with dither & HFRC using 64 gray from 8bit input.

| Colors & Gray Scale | | Data signal | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red data | | | | | | | | Green data | | | | | | | | Blue data | | | | | | | |
| | | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | G0 | G1 | G2 | G3 | G4 | G5 | G6 | G7 | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Light Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Purple | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale of Red | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ▽ | ↓ | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale of Green | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | ▽ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ↓ | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale of Blue | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | ▽ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ↓ | | | | | | | |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale of White & Black | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | △ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | Brighter | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | ▽ | ↓ | | | | | | | | ↓ | | | | | | | | ↓ | | | | | | | |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 9.0 3-WIRE SERIAL PORT INTERFACE (SPI INTERFACE)

This module use 3-wire serial port interface as function configuration and parameter setting

## 9.1 3-Wire command format




| Bit | Description |
|---|---|
| D15-D10 | Register Address [5:0] |
| D9 | W/R control bit. “0” for Write; “1” for Read |
| D9 | Hi-z bit during read mode. Any data within this bits will be ignored during write Mode |
| D7-D0 | Data for the W/R operation to the address indicated by Address phase |

## 9.2 3-Wire Write format

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D1 |
| Register Address [5:0] | | | | | | 0 | X | Data (Issued by external controller) | | | | | | | |

## 9.3 3-Wire Read format

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D1 |
| Register Address [5:0] | | | | | | 1 | Hi-Z | Data (Issued by 3-wire engine) | | | | | | | |

## 9.4 3-wire control register

9.4.1 R00 : System Control Register

| Designation | Address | Description |
|---|---|---|
| MODE | R0[0] | DE/SYNC mode select.<br>MODE = “0”, HSD/VSD mode.<br>MODE = “1”, DE mode. (Default) |
| DCKPOL | R0[1] | DCLK polarity control bit<br>DCLKPOL = “0” : Data sampling at DCLK falling edge. (Default)<br>DCLKPOL = “1” : Data sampling at DCLK rising edge. |
| GRB | R0[2] | Global reset bit.<br>GRB=“0”, The controller is in reset state.<br>GRB=“1”, Normal operation. (Default) |
| STBYB | R0[3] | Standby mode selection bit.<br>STBYB = “0”, Timing control, driver and DC-DC converter, are off, and all outputs are High-Z.<br>STBYB = “1”, Normal operation. (Default) |
| UPDN | R0[4] | Gate Up or Down scan control.<br>UPDN = “0”, STV2 output vertical start pulse and UD pin output Logical “0” to Gate driver. (Default)<br>UPDN = “1”, STV1 output vertical start pulse and UD pin output Logical “1” to Gate driver. (Default) |
| SHLR | R0[5] | Right/Left sequence control of source driver.<br>SHLR = “0”, Shift left : Last data = S1<-S2<-S3…<-S960 = First Data<br>SHLR = “1”, Shift left : Last data = S1->S2->S3…->S960 = Last Data (Default) |
| - | R0[6] | Reserved |
| PWR_EN | R0[7] | POWER enable.<br>PWR_EN = H, enable PWM, Charge pump and VCOM buffer. |

9.4.2 R01 : System Control Register

| Designation | Address | Description |
|---|---|---|
| | R1[0] | Reserved |
| RES[1:0] | R1[2:1] | Display resolution selection.<br>RES[1:0] = “01”, for 1024(RGB)*768 display resolution. (dual or cascade)<br>RES[1:0] = “00”, for 1024(RGB)*600 display resolution. (dual or cascade) (Default)<br>RES[1:0] = “10”, for 800(RGB)*600 display resolution. (dual or cascade)<br>RES[1:0] = “11”, for 800(RGB)*480 display resolution. (dual or cascade) (601~936 channel disable) |
| BIST | R1[3] | Normal Operation / BIST pattern select.<br>BIST = H : BIST (DCLK input is not needed)<br>BIST = L : Normal Operation (Default) |
| DITHER | R1[4] | Dithering function enable control.<br>DITHER = “1”, Enable internal dithering function.<br>DITHER = “0”, Disable internal dithering function. (Default) |
| HFRC | R1[5] | H-FRC selection<br>HFRC = H : H-FRC enable<br>HFRC = L : H-FRC disable (Default)<br>If DITHER = H and HFRC = L : enable only FRC/dithering function<br>If DITHER = L, disable dithering function<br>(H-FRC and FRC both disable) |
| CABC_EN[1:0] | R1[7:6] | CABC H/W enable pin. Normally pull low.<br>When CABC_EN = “00”, CABC OFF. (Default mode)<br>When CABC_EN = “01”, User interface Image.<br>When CABC_EN = “10”, Still Picture.<br>When CABC_EN = “11”, Moving Image. |

9.4.3 R02 : System Control Register

| Designation | Address | Description |
|---|---|---|
| | R2[5:0] | Reserved |
| NBW | R2[6] | Normally black or normally white setting.<br>NBW = H : Normally black<br>NBW = L : Normally white (Default) |
| BIST | R2[7] | Reserved |

9.4.4 R03 : Gate on sequence controller register

| Designation | Address | Description |
|---|---|---|
| SEL[1:0] | R3[1:0] | Gate on sequence select<br>SEL[0] / SEL[1] / Pin control function<br>1 / 1 / Z+2<br>1 / 0 / 2<br>0 / 1 / 1<br>0 / 0 / Z (Default) |
| Frame | R3[2] | Frame inverse or not select.<br>FRAME = “1”, Uniform<br>FRAME = “0”, Frame inverse (Default) |
| - | R3[7:3] | Reserved |

9.4.5 R0E : test mode (1)

| Designation | Address | Description |
|---|---|---|
| TEST_mode(1) | R0E[7:0] | Enter test mode (1)<br>TEST_mode = 8’h5F, enter<br>TEST_mode = other exit (Default) |

9.4.6 R0F : test mode (2)

| Designation | Address | Description |
|---|---|---|
| TEST_mode(2) | R0F[7:0] | Enter test mode (2)<br>TEST_mode = 8’hA4, enter<br>TEST_mode = other exit (Default) |

9.4.7 R0D : charging time control (3)

| Designation | Address | Description |
|---|---|---|
| OE_WIDTH | R0D[7:0] | Inversion type select. Enter Test mode (1) and (2) first.<br>Then R0D setting will be active<br>TEST_mode = 8'h00, increase charge time |

9.4.8 R02 : charge sharing control

| Designation | Address | Description |
|---|---|---|
| EQC_ADJ | R02[7:0] | Inversion type select. Enter Test mode (1) and (2) first.<br>Then R10 setting will be active<br>EQC_ADJ = 8'h43, adjust charge sharing time |

9.4.9 R0A : BIAS current control (5)

| Designation | Address | Description |
|---|---|---|
| BIAS_TRIG | R0A[7:0] | Inversion type select. Enter Test mode (1) and (2) first.<br>Then R10 setting will be active<br>BIAS_TRIG = 8'h28, trigger bias reduction |

9.4.10 R10 : inversion architecture

| Designation | Address | Description |
|---|---|---|
| INV | R10F[7:0] | Inversion type select. Enter Test mode (1) and (2) first.<br>Then R10 setting will be active<br>2line / 1dot = 8'h41<br>1line / 1dot = 8'h01 (Default) |

9.4.11 R38 : PWM_DIV setting

<table>
<tr><th>Designation</th><th>Address</th><th>Description</th></tr>
<tr><td>PWM_DIV[3:0]</td><td>R38[7:0]</td><td>
PWM Dimmer frequency step setting
<table>
<tr><th>R38[7:0]</th><th>PWM_DIV[3:0]</th><th>Register function</th></tr>
<tr><td>0x0C</td><td>000</td><td>Don’t use.</td></tr>
<tr><td>0x1C</td><td>001</td><td>1</td></tr>
<tr><td>0x2C</td><td>010</td><td>2</td></tr>
<tr><td>0x3C</td><td>011</td><td>3</td></tr>
<tr><td>0x4C</td><td>100</td><td>4</td></tr>
<tr><td>0x5C</td><td>101</td><td>5</td></tr>
<tr><td>0x6C</td><td>110</td><td>6</td></tr>
<tr><td>0x7C</td><td>111</td><td>7 (Default)</td></tr>
</table>
<table>
<tr><th>PWM Reference Frequency (FOSC)</th><th>Real PWM Frequency of DIMO</th></tr>
<tr><td>51.2MHz (Typical)</td><td>PWM Frequency = $\frac{\text{FOSC}}{256 \times 128 \times \text{PWM\_DIV[2:0]}}$</td></tr>
</table>
In order in maintain the dimming frequency for brightness control at different display resolution (typical 1024 x 600) at normal mode. We will change default value of PWM_DIV to follow as table
<table>
<tr><th>Display Resolution</th><th>Default value of PWM_DIV</th></tr>
<tr><td>RES[1:0] = “00”</td><td>111</td></tr>
<tr><td>RES[1:0] = “01”</td><td>111</td></tr>
<tr><td>RES[1:0] = “10”</td><td>110</td></tr>
<tr><td>RES[1:0] = “11”</td><td>100</td></tr>
</table>
</td></tr>
</table>

Note : The R6 and R38 register will be available when the R0E and R0F register already had issued.

## 9.5 Recommend Register Setting (CABC Off mode)

Register write sequence : R00 (Reset)→ R00 (Into Standby mode) → R01 (Enable Normally Black) → R02 (Enable FRC / Dither, CABC off Mode) → R0E (Enter Test mode (1)) → R0F (Enter Test mode (2))→ R0D (SDRRS on) → R00 (Release standby mode)

If you don't use register write sequence, it may cause faulty operation.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| R01 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| R02 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R0E | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| R0F | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0D | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

## 9.6 Recommend Register Setting (CABC on mode (Moving Picture)

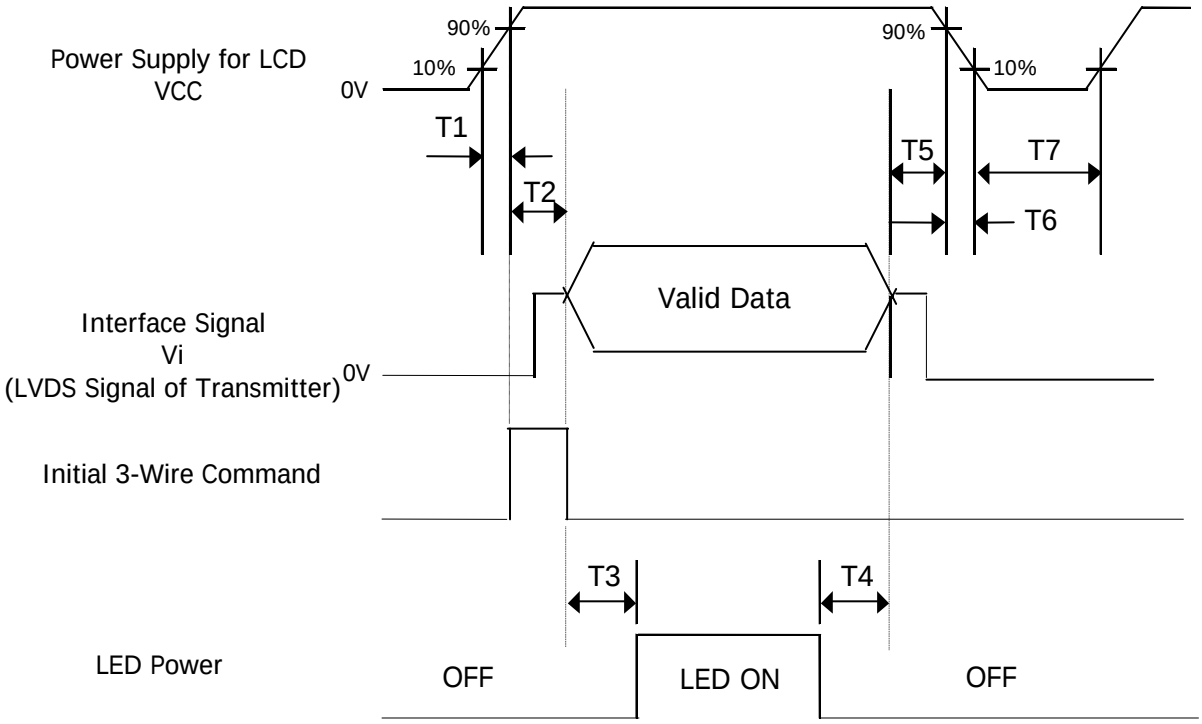
Register write sequence : R00 (Reset)→ R00 (Into Standby mode) → R01 (Enable Normally Black) → R02 (Enable FRC / Dither, CABC off Mode) → R0E (Enter Test mode (1)) → R0F (Enter Test mode (2)) → R0D (SDRRS on)→ R38 (PWM Frequency = 1.5KHz) → R00 (Release standby mode)

If you don't use register write sequence, it may cause faulty operation.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| R01 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| R02 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R0E | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| R0F | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0D | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R38 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| R00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

## 10.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below




| Parameter | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| T1 | 0.5 | | 10 | ms | |
| T2 | 0 | | 16 | ms | |
| T3 | 200 | | | ms | |
| T4 | 200 | | | ms | |
| T5 | 0 | | | ms | |
| T6 | 3 | | | ms | |
| T7 | 400 | | | ms | |

Notes : 1. When the power supply VDD is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

# 11.0 MECHANICAL CHARACTERISTICS

## 11.1 Dimensional Requirements

Figure 5 & 6 (located in 12.0) shows mechanical outlines for the model

<Table9, Mechanical Characters >

| Parameter | Specification | Unit |
|---|---|---|
| Active Area | 153.60(H) X 90.00(V) | mm |
| Number of pixels | 1024(H) X 600(V) (1 pixel = R + G + B dots) | |
| Pixel pitch | 0.15(H) X 0.15(V) | |
| Pixel arrangement | RGB Vertical stripe | |
| Display colors | 16.7M | |
| Display mode | Normally Black | |
| Outline dimension | 163.6±0.3(H)×102.9±0.3(V)× 2.47±0.2(D) | mm |
| Weight | 95 (Max.) | g |
| Back-light | Edge side 20-LEDs type ( 5 X 4 Array) | |

## 11.2 LR and Polarizer Hardness.

The surface of the LCD has an Low reflection coating and a coating to reduce scratching.

## 11.3 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 150lux. The manufacture shall furnish limit samples of the panel showing the light leakage acceptable.

## 12.0 MECHANICAL DRAWING

**Figure 5. TFT-LCD Module Outline Dimension (Front View)**

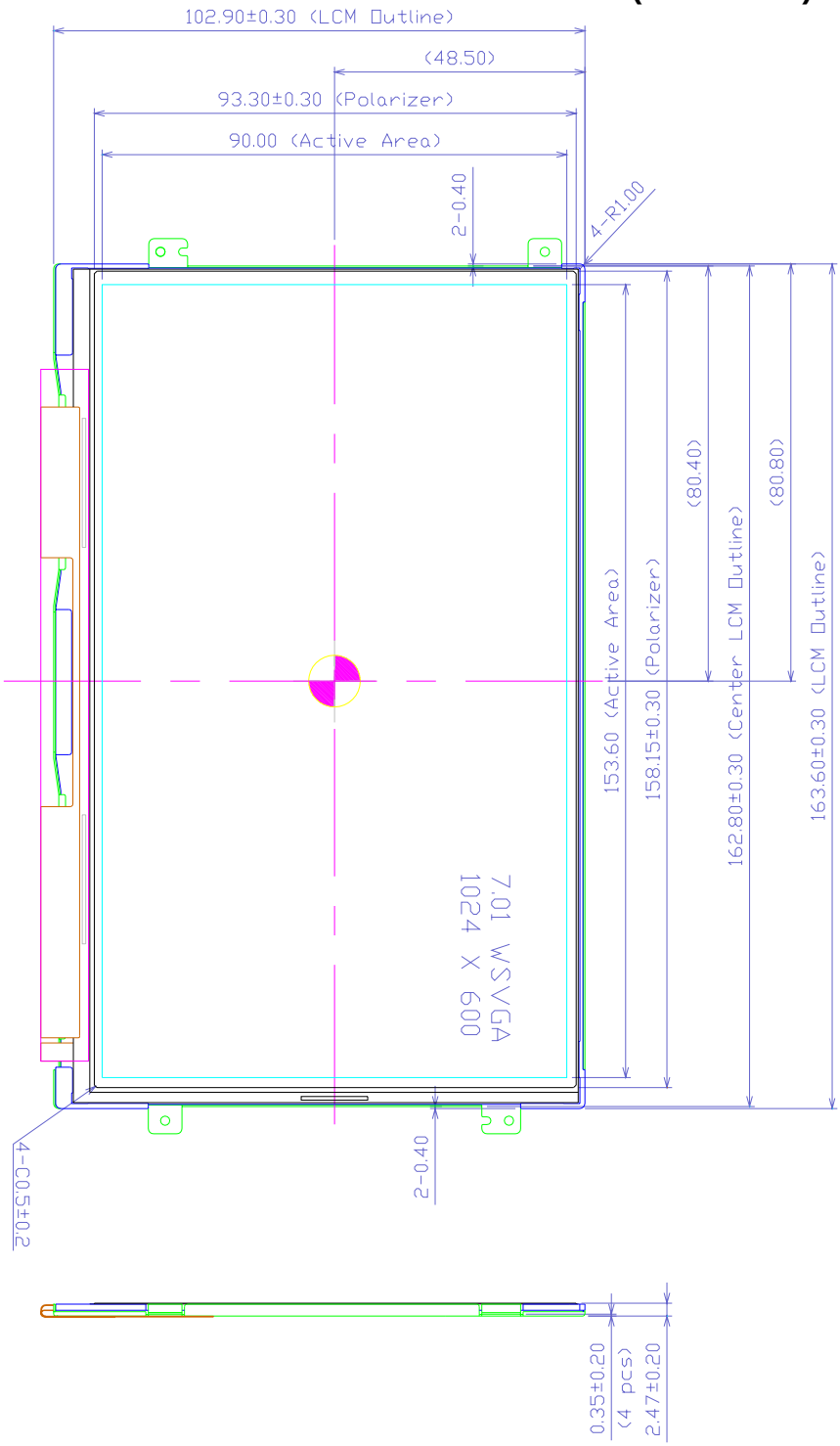
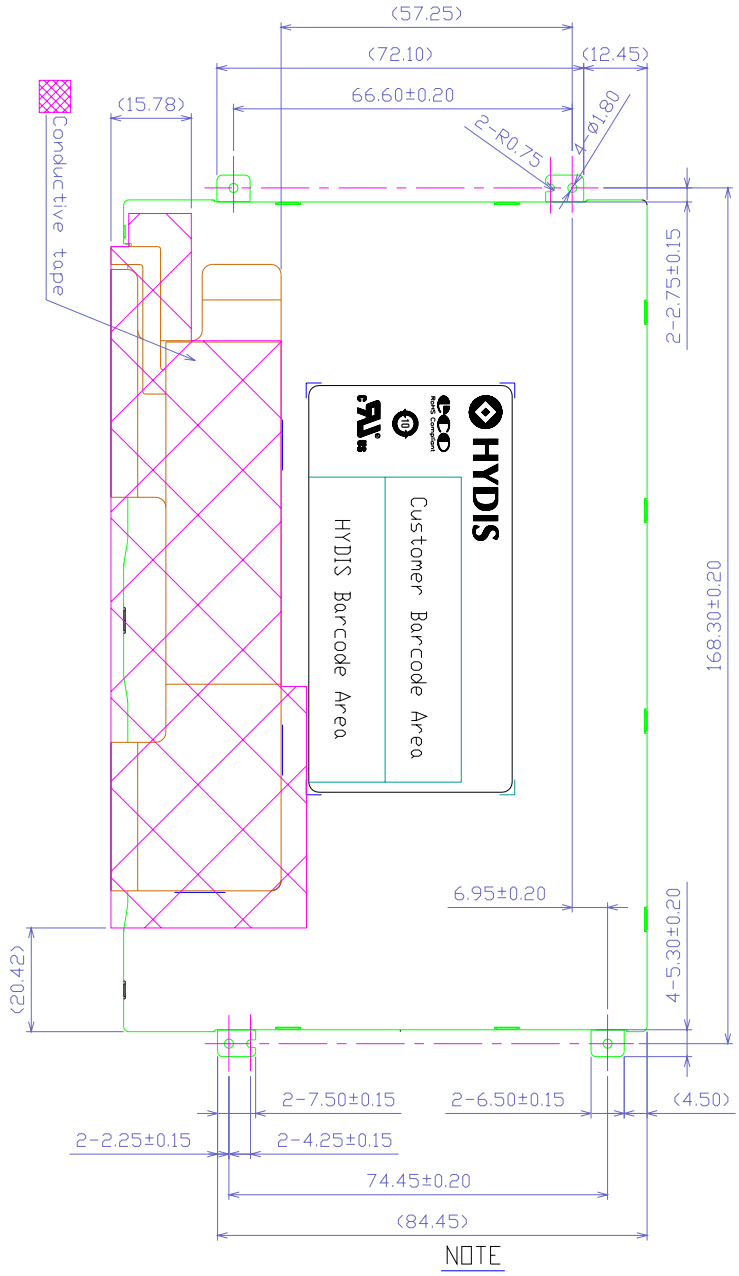


**Figure 6. TFT-LCD Module Outline Dimensions (Rear view)**




NOTE

1.CN1: JAE AA01B P030VA1
2.BL FPC SOLDERING HIGHT : 0.5 Max. (Form PCB)
3.LCM BENDING ALLOWANCE SPEC. : 0.3
4.LCM BURR SPEC : INNER SIDE 0.03 Max.
5.OTHER SPECIFICATION : REFERS TO SPEC SHEET

## 13.0 RELIABLITY TEST

The Reliability test items and its conditions are shown in below.

<Table10, Reliability Test>

| No | Test Item | | Conditions |
|---|---|---|---|
| 1 | High temperature operation test | | Ta = 60 °C, 240 hrs |
| 2 | Low temperature operation test | | Ta = -20 °C, 24 hrs |
| 3 | High temperature storage test | | Ta = 70 °C, 240 hrs |
| 3 | Low temperature storage test | | Ta = -40 °C, 240 hrs |
| 5 | High temperature & high humidity operation test | | Ta = 60 ℃, 90%RH, 240hrs |
| 6 | Thermal shock | | Ta = -40 °C ↔ 70 °C<br>(30min residence, 30sec rise/fall time), 100 cycle |
| 7 | Altitude operating | | 631hPa (12500ft) |
| 8 | Altitude storage | | 165hPa (42000ft) |
| 9 | Mechanical shock | | 80G, sine wave, 11ms 3times at each direction,<br>6 directions |
| 10 | Mechanical vibration | Sine sweep | 1.5G, sine wave, 10Hz → 500Hz → 10Hz, 0.37 oct / min,<br>3 axis, 1hour / axis |
| 11 | | Random | 3 Grams, random vibration, 3 axis, 15 min / axis |
| 12 | Electro-static discharge test (non-operating) | | Contact (Case/front surface) : 150pF, 150ohm, +/- 8kV<br>Air (Case/front surface) : 150pF, 150ohm, +/- 15kV<br>FPC Input : 100pF, 100ohm, +/- 200V |

## 14.0 HANDLING & CAUTIONS

### 14.1 Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

### 14.2 Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass (epoxy) material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

**14.3 Cautions for the operation**

- When the module is operating, do not lose MCLK, DE signals. If any one of these signals were lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

**14.4 Cautions for the atmosphere**

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

**14.5 Cautions for the module characteristics**

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

**14.6 Cautions for the digitizer assembly**

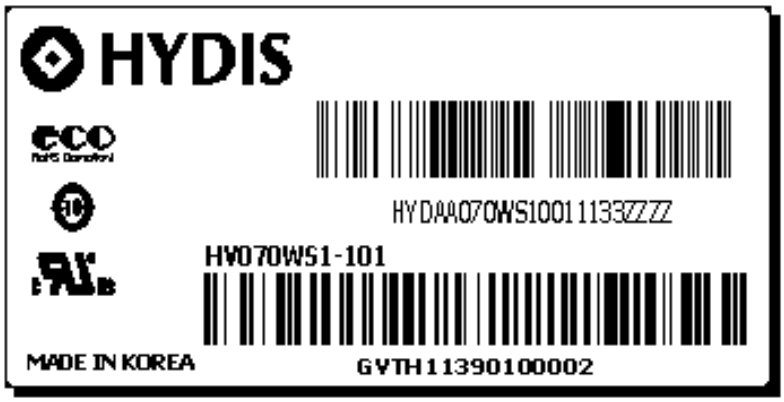
- When assembling FPC connector, do not flip connector past 90° due to possible damage to connector.
- When positioning digitizer underneath driver IC, do not lift driver IC past 90° due to possible damage to drive IC pattern.
- Please be warned that during assembly of digitizer, the opening or closing of FPC will result in possible electrostatic discharge damage to the LED

**14.7 Other cautions**

- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

# 15.0 LABELS

## 15.1 Product Label




**Customer Barcode**

| V | V | V | P | P | P | P | P | P | P | P | P | P | Y | Y | W | W | Z | Z | Z | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

01~03 : Vendor code
04~14 : QPN
15~16 : Manufactured year
17~18 : Manufactured week
19~22 : Serial number (32 digit/alphabet)

**HYDIS Barcode**

| 1 | | 2 | 3 | 4 | | 5 | 6 | | | | 7 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

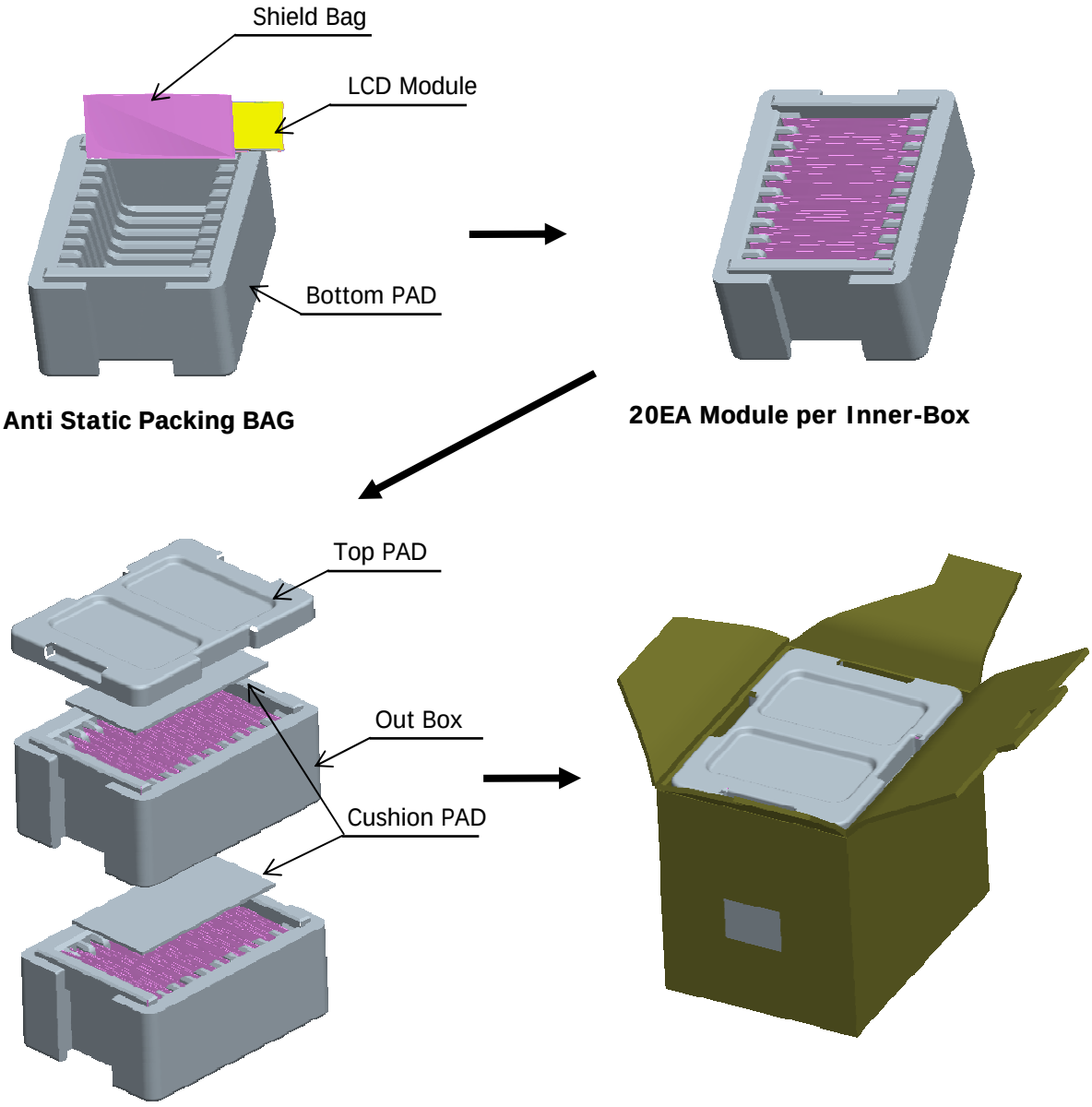
No 1. Control Number
No 2. Rank / Grade
No 3. Line Classification
(HYDIS : H)
No 4. Year (5 : 2005, 6 : 2006, …)
No 5. Month (1, 2, 3,…, 9, X, Y, Z)
No 6. FG Code
No 7. Serial Number

**15.2 Packing Label**

TBD

# 16.0 PACKING INFORMATION

## 16.1 Packing order




Notes : 1. Box Dimension: 350mm(W) X 265mm(D) X 320mm(H)
2. Package Quantity in one Box : 40pcs