Advance Information

24-Channel Matrix TFEL Panel Display Column Driver

Ordering Information

Device	Package Options	
	44-Lead Ceramic J-Bend	Die
HV08	HV08DJ	HV08X

Features

- ☐ TTL-compatible imputs
- ☐ Up to 70V modulation voltage
- ☐ Capability of 16 levels of gray shading
- ☐ 6MHz data shift rate
- ☐ 24 Outputs per device (can be cascaded)
- ☐ Minimum 40mA high-voltage output source/sink capability
- ☐ Pin-programmable shift direction
- ☐ D/A conversion can be performed in as little as 3μS
- ☐ Diodes in output structure allow usage in energy recovery systems (non-gray shaded)
- ☐ Integrated high-voltage CMOS technology
- ☐ Available in 44-lead ceramic J-bend package or in die form

General Description

The HV08 is a 24-channel column driver IC designed for general purpose electroluminescent display use. Each channel of the HV08 consists of a 4-bit wide shift register, a 4-bit counter, and a high voltage sample and hold circuit to perform a D/A conversion to one of 16 arbitrary voltage levels. The output of each channel is buffered by a source-follower structure which allows both sourcing and sinking of output current.

DIR is a shift direction select pin which has been provided to allow the user to reverse shift direction between channels and to interchange the function of the shift register data input and output pins. When the DIR input is high, data is shifted in a clockwise direction. Data is accepted at pins I/01 through I/04 and output at O/I1 through O/I4. When the DIR input is low, data is shifted in a counterclockwise direction. Data is accepted at pins O/I1 through O/I4 and output at pins I/01 through I/04.

D/A conversion is accomplished by means of a high-voltage sample and hold circuit which is controlled by a 4-bit counter. For each channel, data is serially shifted through the (4-bit wide) shift register by the rising edge of SCLK. With the MODE signal high, the data in the shift register is transferred to a polynomial counter by the rising edge of CCLK. The mode signal is then brought low and the counter is down-counted to zero; again, the rising edge of CCLK. During the period that the counter is not zero, a sample switch is held closed which allows a storage capacitor to be charged to voltage at the V_R (ramp voltage) input to the device. The high voltage output also follows V_R during this period. When the counter reaches zero, the sample switch is opened. The output then holds at the value of V_R that was present when zero count occurred. A diode provides for the discharge of the storage capacitor once V_R is less than the voltage on the capacitor.

Electrical Characteristics

Low-Voltage DC Characteristics

Symbol	Parameter	Min	Typ[2]	Max	Units	Conditions
V_{DD}	Low-voltage supply	4.5	5.0	5.5	V	
I_{DD}	V_{DD} supply current (active)		6.0	10.0	mA	f_{SCLK} = 6MHz[1] f_{CCLK} = 6MHz F_{DATA} = 3MHz
I_{DDS}	V_{DD} supply current (standby)			1.0	mA	All V_{IN} = 0V
V_{IH}	High-level input voltage	2.4		V_{DD}	V	
V_{IL}	Low-level input voltage	0		0.8	V	
I_{IH}	High-level input current		1.0	50	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level input current		-1.0	-50	µA	V_{IL} = 0V
C_{IN}	Input capacitance (data, mode, SCLK, CCLK)			10	pF	V_{IN} = 0V, f = 1MHz
T_A	Operating free-air temperature	-55		125	C	
V_{OH}	High-level output voltage	2.8			V	I_{OH} = -4mA, V_{DD} = min
V_{OL}	Low-level output voltage			0.4	V	I_{OL} = 4mA, V_{DD} = min
I_{OH}	High-level output current			-4.0	mA	
I_{OL}	Low-level output current			4.0	mA	

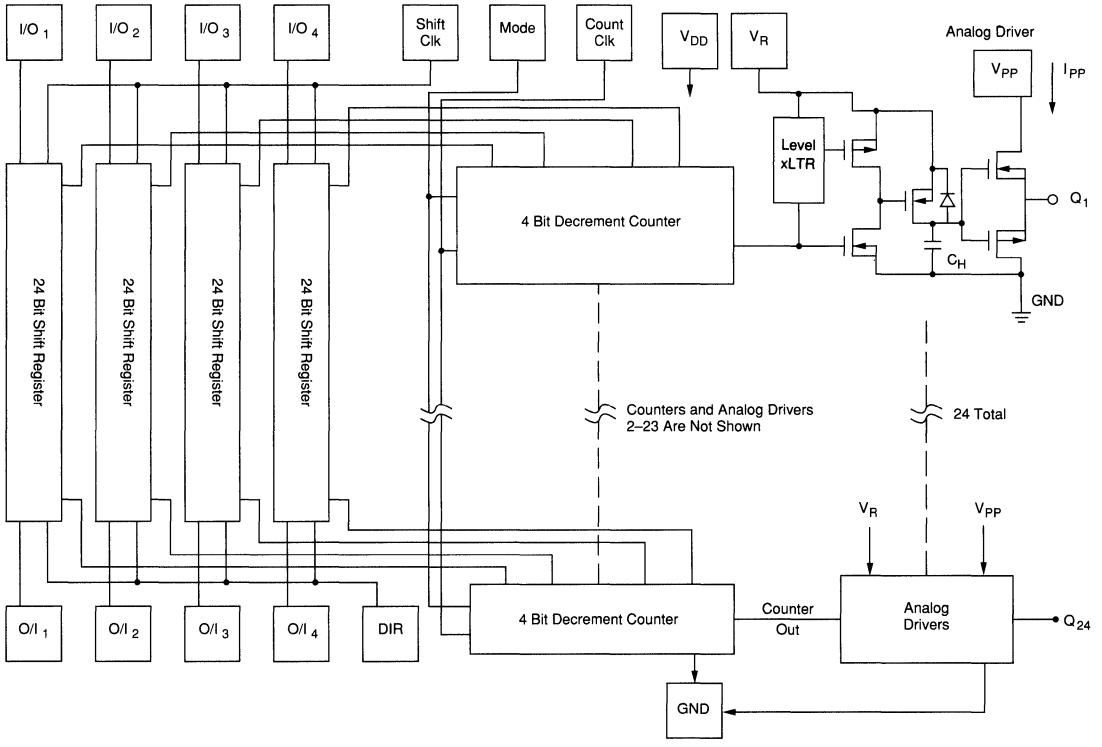
Notes: 1. SCLK, CCLK are continuous.
2. All typical values are at V_{DD} = 5.0V.

High-Voltage DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High-voltage supply	-0.3		70	V	
I_{PP}	V_{PP} supply current			100	µA	V_{PP} = 70V, outputs high or low, no load
V_R	Ramp voltage	0		V_{PP}	V	
I_{AOH} max	Maximum high-voltage analog output source current[1]	-40			mA	V_{PP} = 70V
I_{AOH}	High-voltage analog output source current[1]	-10			mA	V_{PP} = 70V V_R = 30V V_{AO} = 28V
I_{AOL} max	Maximum high-voltage analog output sink current[2]	40			mA	V_{PP} = 70V
I_{AOL}	High-voltage analog output sink current[2]	10			mA	V_{PP} = 70V V_R = 30V V_{AO} = 32V

Notes: 1. Either by N-CH transistor or P-CH output diode.
2. Either by P-CH transistor or N-CH output diode.

Functional Block Diagram



Function Table

Function	Control Inputs				Shift Registers	Counters	Outputs	
	Shift Clock	Counter Clock	Mode	V_R			Serial	Parallel
Load Shift Register	↑	X	L	X	Normal Shift Op.	X	Delayed Data-In	X
Load Counter	No ↑	↑	H	X	No Change	Load Data from S/R to Counter	No Change	Low
Counting	X	↑	L	Initiates Ramp	X	Translates Data to Time	X	D/A Conversion
Voltage Conversion	X	Pulsing	L	Volt Ramping Up	X	Counting	X	Follows Ramp

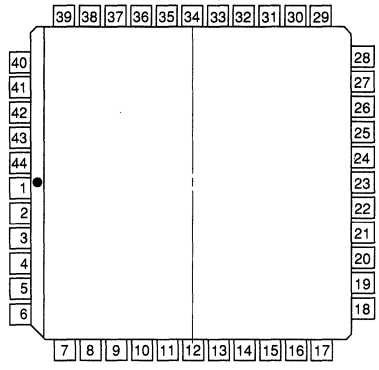
L = Low level, H = High level, X = Irrelevant, ↑ = Low to Hi Transition

Pin Configuration

44-Pin J-Lead

Pin	Function	Pin	Function
1	GND	23	HVout 13
2	DIR	24	HVout 12
3	V_{DD}	25	HVout 11
4	Mode	26	HVout 10
5	O/I_1	27	HVout 9
6	O/I_2	28	HVout 8
7	O/I_3	29	HVout 7
8	O/I_4	30	HVout 6
9	V_R	31	HVout 5
10	V_{PP}	32	HVout 4
11	GND	33	HVout 3
12	HVout 24	34	HVout 2
13	HVout 23	35	HVout 1
14	HVout 22	36	GND
15	HVout 21	37	V_{PP}
16	HVout 20	38	V_R
17	HVout 19	39	I/O_4
18	HVout 18	40	I/O_3
19	HVout 17	41	I/O_2
20	HVout 16	42	I/O_1
21	HVout 15	43	SC
22	HVout 14	44	CC

Package Outline



top view

44-pin J-lead Package

Gray Shade Decoding Scheme

Brightest Shade No.	I/O_1	I/O_2	I/O_3	I/O_4	
16	1	0	0	1	Brightest
15	1	1	0	1	
14	1	1	1	1	
13	1	1	1	0	
12	0	1	1	1	
11	1	0	1	0	
10	0	1	0	1	
9	1	0	1	1	
8	1	1	0	0	
7	0	1	1	0	
6	0	0	1	1	
5	1	0	0	0	
4	0	1	0	0	
3	0	0	1	0	
2	0	0	0	1	
1	0	0	0	0	Dimmest