

Dual 4-Channel High Voltage Switch with Decode

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Order Number / Package		
			20-pin ceramic side-brazed DIP	20-pin Plastic DIP	Die in wafer pack
+70V	-70V	110V P-P	HV1314C	HV1314P	HV1314X
+80V	-80V	130V P-P	HV1316C	HV1316P	HV1316X

Features

- HVCOS[®] Technology
- Up to 130V peak to peak switching capability
- Output On-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45 dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip decode, latch and chip select logic circuitry

Absolute Maximum Ratings*

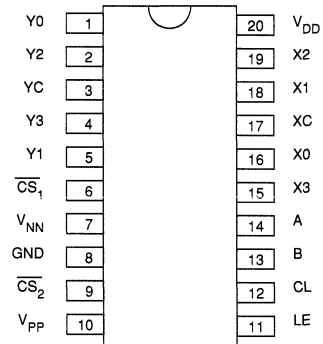
V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) configured as dual 4 channel switches with decode, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the decoded data. Using HVCOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view
20-pin DIP

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R _{SW}		50		40	50		60	ohms	I _{SW} = 5mA
Switch (ON) Resistance	R _{SW}		35		25	35		45	ohms	I _{SW} = 200mA
Switch (ON) Resistance	R _{SW}		55		45	55		65	ohms	V _{PP} = +50V V _{NN} = -50V I _{SW} = 5mA
Switch (ON) Resistance	R _{SW}		40		25	40		50	ohms	V _{PP} = +50V V _{NN} = -50V I _{SW} = 200mA
Switch (ON) Resistance Matching x and y (0-3)	R _{SW}		20			20		20	%	I _{SW} = 5mA V _{PP} = +50V, V _{NN} = -50V
Switch Off Leakage	I _{SWL}		50		0.5	50		150	μA	V _{OUT} = V _{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C _{SW}		100		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C _{IN}				3.5				pF	
Pos. HV Supply Current	I _{PPQ}		200		50	200		200	μA	ALL SWS OFF
Neg. HV Supply Current	I _{NNQ}		-200		-50	-200		-200	μA	
Pos. HV Supply Current	I _{PP}				1.6	3.2			mA	1 SW ON
Neg. HV Supply Current	I _{NN}				-1.6	-3.2			mA	I _{SW} = 5mA
Pos. HV Supply Current	I _{PP}				1.2	2.4			mA	V _{PP} = +50V
Neg. HV Supply Current	I _{NN}				-1.2	-2.4			mA	V _{NN} = -50V 1 SW ON, I _{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I _{DD}				0.001	0.5			mA	

AC Characteristics (VDD = 12V, TC = 25°C)

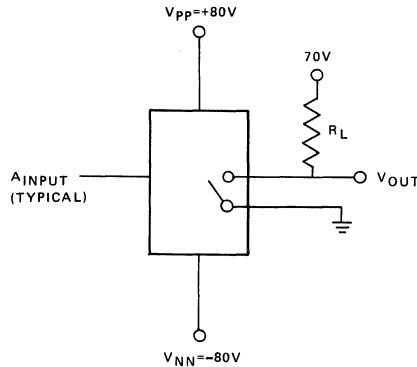
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After LE Rises	t _{HD}				5				ns	
Set Up Time Before LE Rises	t _{SD}				260				ns	
Time Width of LE	t _{WLE}				300				ns	
Time Width of CL	t _{WCL}				100				ns	
Turn On Time	t _{ON}		5		2.5	5		5	μs	
Turn Off Time	t _{OFF}		10		5.0	10		10	μs	
Off Isolation	KO				35	45			dB	f = 5MHz

Recommended Operating Conditions

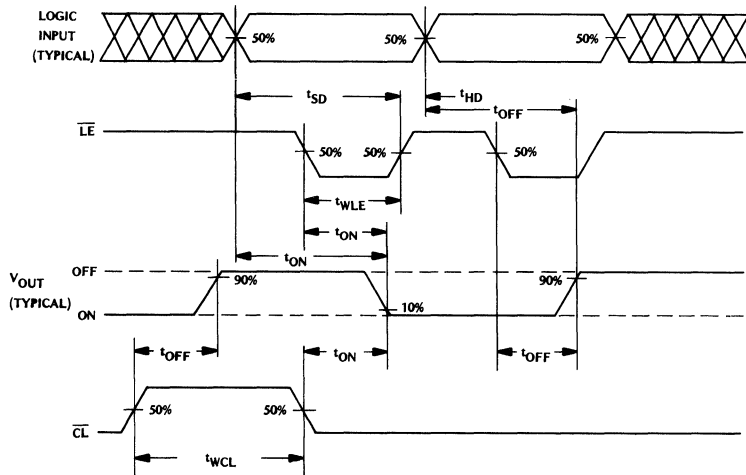
Symbol	Parameter	Device		Value
		HV1314	HV1316	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	$V_{DD} - 2V$ to V_{DD}
V_{IL}	Low level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	$V_{NN} + 15V$ to $V_{PP} - 15V$
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
 Power up sequence: GND VNN VDD VPP
 Power down sequence: VPP VDD VNN GND

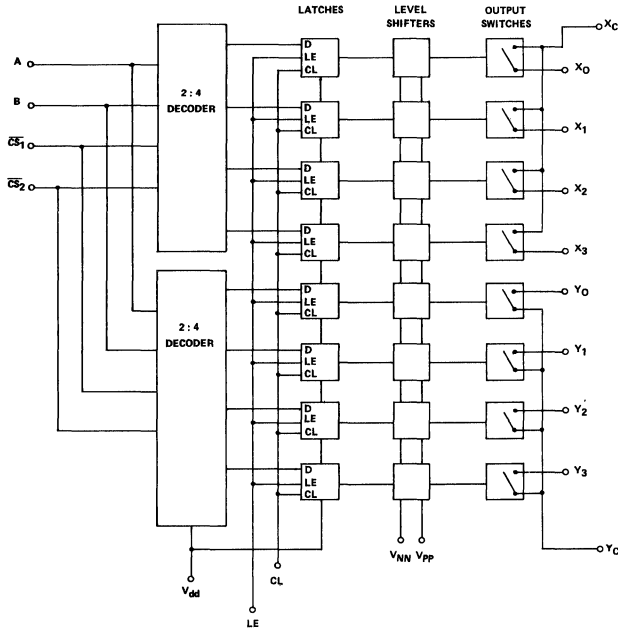
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



Truth Table

B	A	\overline{CS}_1	\overline{CS}_2	LE	CL	X0	X1	X2	X3	Y0	Y1	Y2	Y3
L	L	L	L	L	L	ON				ON			
L	H	L	L	L	L		ON				ON		
H	L	L	L	L	L			ON				ON	
H	H	L	L	L	L				ON				ON
X	X	H	X	L	L	ALL OFF							
X	X	X	H	L	L	ALL OFF							
X	X	X	X	X	H	ALL OFF							
X	X	X	X	H	L	HOLDS PREVIOUS STATE							

Notes:

1. Address data at A and B cause one switch in each group of four to be selected for connection to the common busses XC or YC.
2. The clear input CL overrides all other inputs.
3. Since the latch follows the decoder, only the CL input matters when LE is H.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the decoded selection address information flows through the latch.

Typical Performance Curves

