8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options				
			24-pin ceramic side-brazed DIP	Die in waffle pack	36-pin leaded ceramic chip carrier	24-pin plastic DIP	28-lead plastic chip carrier
+70V	-70V	110V P-P	HV1614C	HV1614X	HV1614CS	HV1614P	HV1614PJ
+80V	-80V	130V P-P	HV1616C	HV1616X	HV1616CS	HV1616P	HV1616PJ

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch and chip select logic circuitry
- ☐ Surface mount package available

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} +0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching	R_{SW}		15			15		15	%	I_{SW} = 5mA V_{PP} = +50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Current	I_{DD}				0.001	5			mA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	1.5		1.6	1.8		1.5		mA	V_{OUT} = 0.7V

AC Characteristics

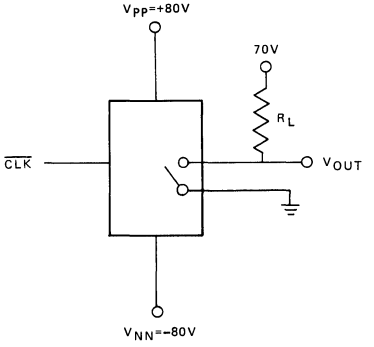
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	
Off Isolation	KO			35	45				dB	f = 5MHz
Max Clock Freq	t_{CLK}					3			MHz	f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			35					ns	

Recommended Operating Conditions

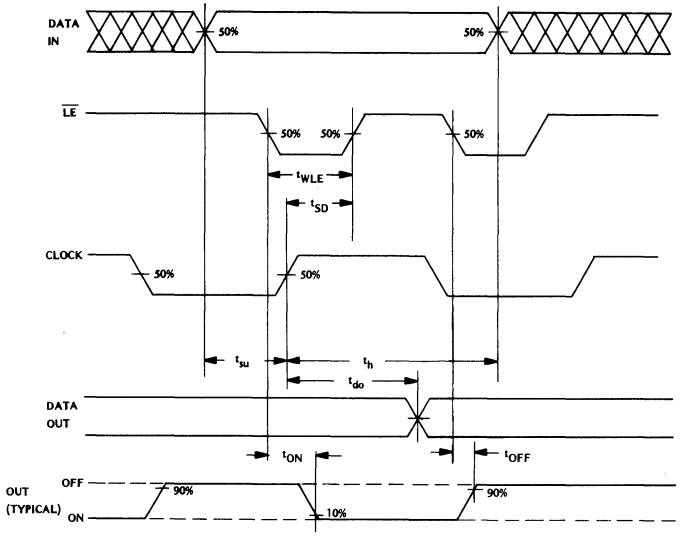
Symbol	Parameter	Device		Value
		HV1614	HV1616	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

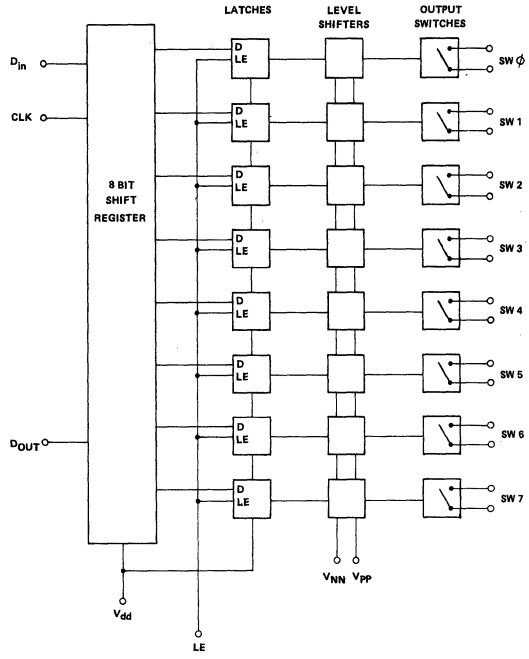
T_{ON}/T_{OFF} Measurement Circuit



Logic Timing Waveforms



Logic Diagram



Truth Table

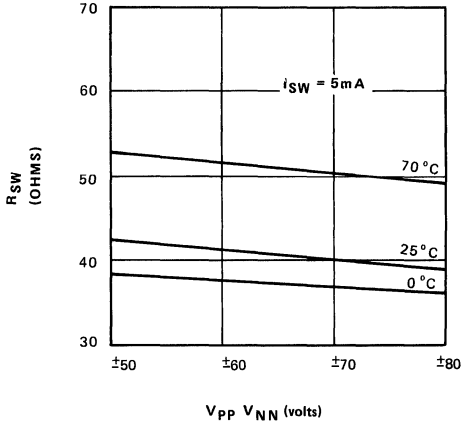
D0	D1	D2	D3	D4	D5	D6	D7	LE	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

Notes:

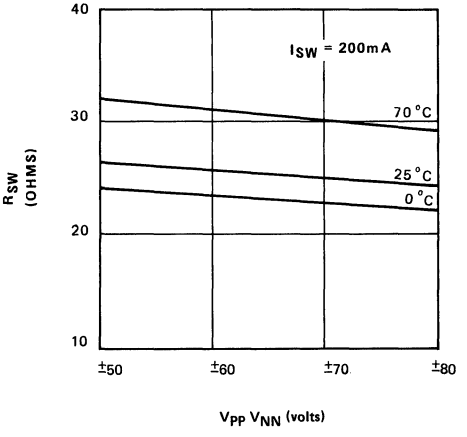
1. The eight switches operate independently
2. Serial data is clocked in on the L→H transition of CK.
3. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if LE is H.

Typical Performance Curves

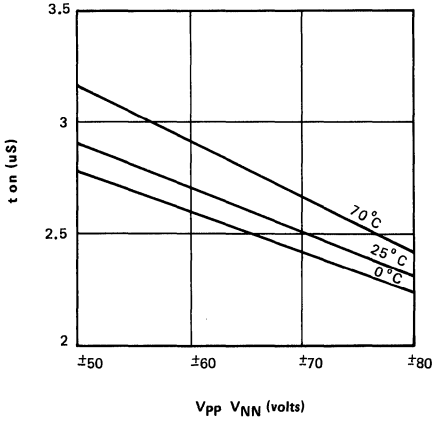
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



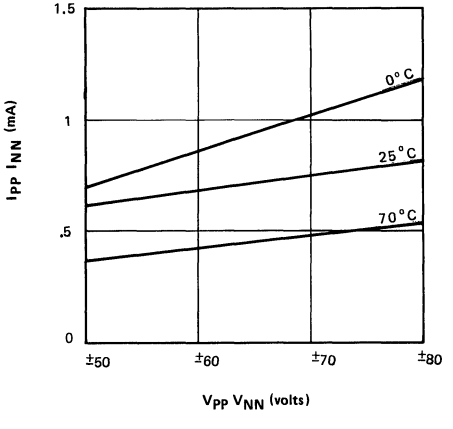
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



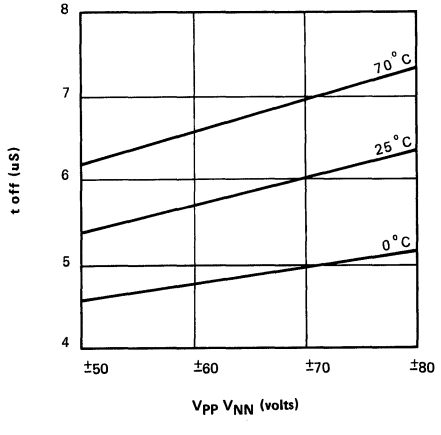
TYPICAL
t on (uS) vs. V_{PP} V_{NN}



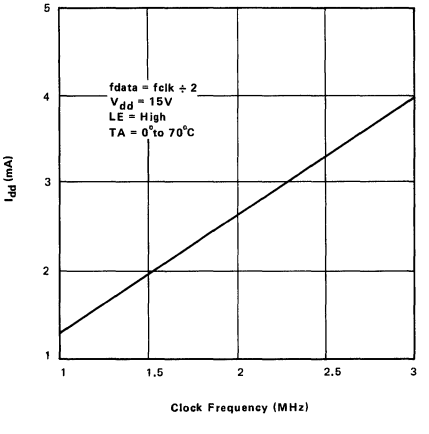
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



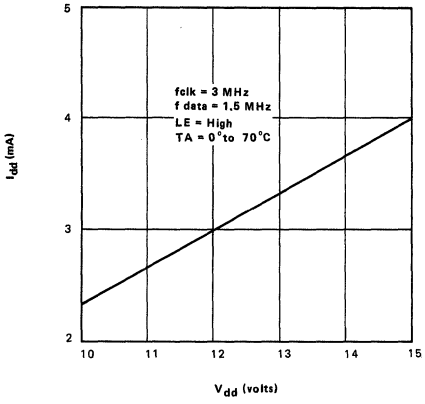
TYPICAL
t_{off} vs. V_{PP} V_{NN}



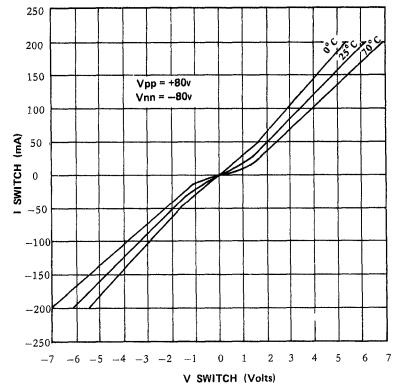
TYPICAL
Idd vs. Frequency



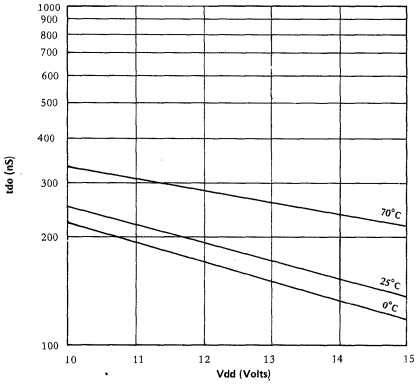
TYPICAL
Idd vs. Vdd



TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
tdo vs Vdd



Pin Configurations

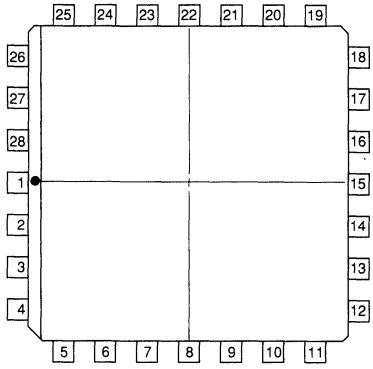
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	LE
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

24-Pin DIP

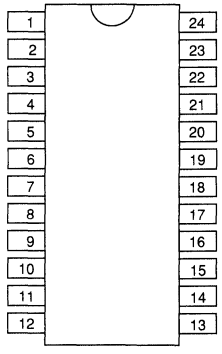
Pin	Function	Pin	Function
1	SW3	13	D_{IN}
2	SW3	14	CK
3	SW2	15	LE
4	SW2	16	D_{OUT}
5	SW1	17	SW7
6	SW1	18	SW7
7	SW0	19	SW6
8	SW0	20	SW6
9	V_{PP}	21	SW5
10	V_{NN}	22	SW5
11	GND	23	SW4
12	V_{DD}	24	SW4

Package Outlines



top view

28-pin J-lead Package



top view

24-pin DIP