Preliminary

8-Channel High Voltage Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options				
			28-Pin Ceramic Side-Brazed DIP	Die in Waffle Pack	36-Pin Leaded Ceramic Chip Carrier	28-Lead Plastic Quad "J" Bend	28-Pin Plastic DIP
+70V	-70V	110V P-P	HV1814C	HV1814X	HV1814CS	HV1814PJ	HV1814P
+80V	-80V	130V P-P	HV1816C	HV1816X	HV1816CS	HV1816PJ	HV1816P

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak output switching
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10 MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch with clear function and chip select logic circuitry

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals: e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} Positive high voltage supply	-0.5V to +90V
V_{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V_{DD} + 0.3V
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{SW}		50		40	50		60	ohms	I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		35		25	35		45	ohms	I_{SW} = 200mA
Switch (ON) Resistance	R_{SW}		55		45	55		65	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 5mA
Switch (ON) Resistance	R_{SW}		40		25	40		50	ohms	V_{PP} = +50V V_{NN} = -50V I_{SW} = 200mA
Switch (ON) Resistance Matching (0-7)	R_{SW}		15			15		15	%	I_{SW} = 5mA V_{PP} = 50V, V_{NN} = -50V
Switch Off Leakage	I_{SWL}		50		0.5	50		150	µA	V_{OUT} = V_{PP} -10V thru 10K with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	RL = 100K
DC Offset Switch On			500		100	500		500	mV	RL = 100K
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current Neg. HV Supply Current	I_{PPQ} I_{NNQ}		200 -200		50 -50	200 -200		200 -200	µA µA	ALL SWS OFF
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.8 -0.8	1.6 -1.6			mA mA	1 SW ON I_{SW} = 5mA
Pos. HV Supply Current Neg. HV Supply Current	I_{PP} I_{NN}				0.6 -0.6	1.2 -1.2			mA mA	V_{PP} = +50V V_{NN} = -50V 1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	
Logic Supply Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Current	I_{DD}				0.001	0.5			mA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	1.5		1.6	1.8		1.5		mA	V_{OUT} = 0.7V

AC Characteristics

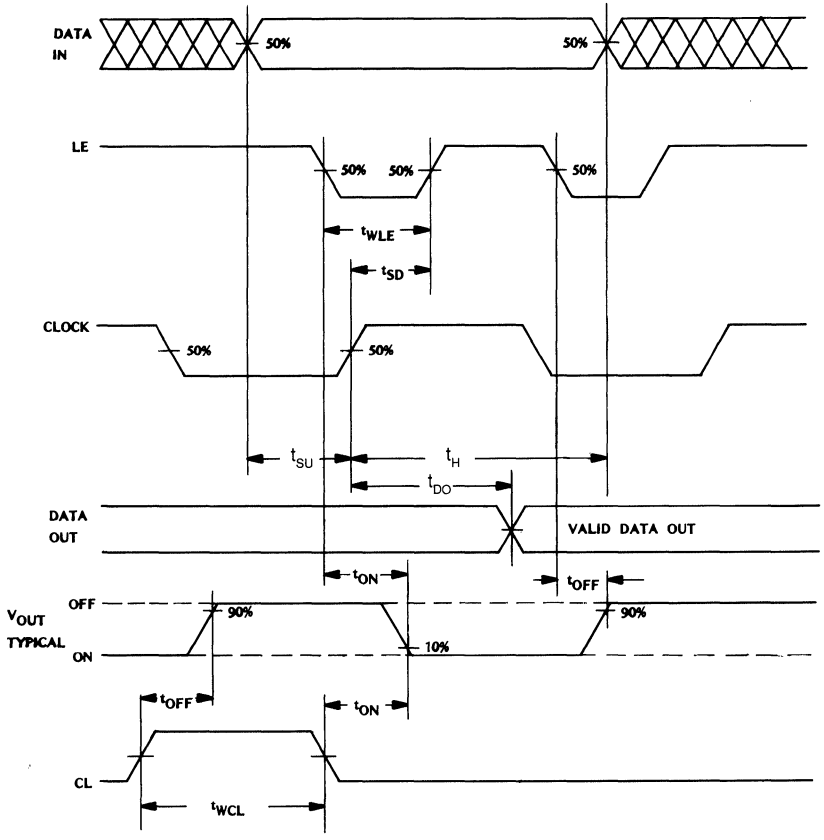
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Max Clock Freq	f_{CLK}					3			MHz	f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data to Clock	t_h			35					ns	
Set Up Time Before LE Rises	t_{SD}			260					ns	
Time Width of LE	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5		2.5	5		5	µs	
Turn Off Time	t_{OFF}		10		5	10		10	µs	
Time Width of CL	t_{WCL}			100					ns	
Off Isolation	KO			35	45				dB	f = 5MHz

Recommended Operating Conditions

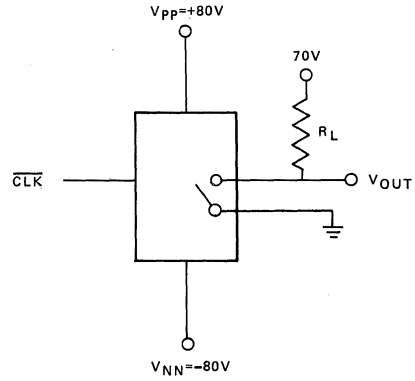
Symbol	Parameter	Device		Value
		HV1814	HV1816	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5 V
V_{PP}	Positive high voltage supply	X		+50.0V to +70.0V
			X	+50.0V to +80.0V
V_{NN}	Negative high voltage supply	X		-50.0V to -70.0V
			X	-50.0V to -80.0V
V_{IH}	High-level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free-air temperature	X	X	0°C to 70°C

Note: For non-ground referenced systems the following must be used:
Power up sequence: GND VNN VDD VPP
Power down sequence: VPP VDD VNN GND

Logic Timing Waveform



T_{ON}/T_{OFF} Measurement Circuit



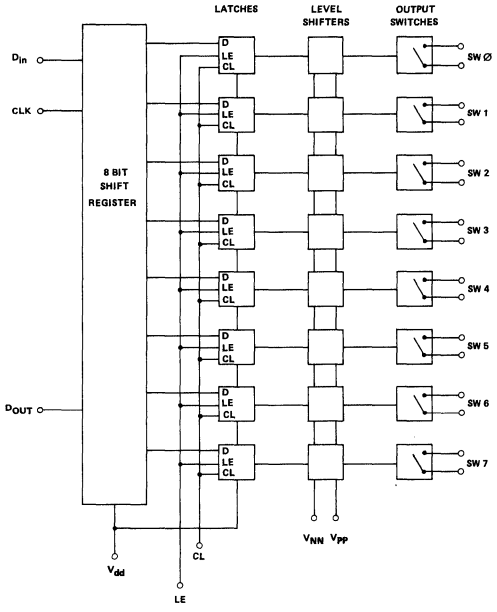
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

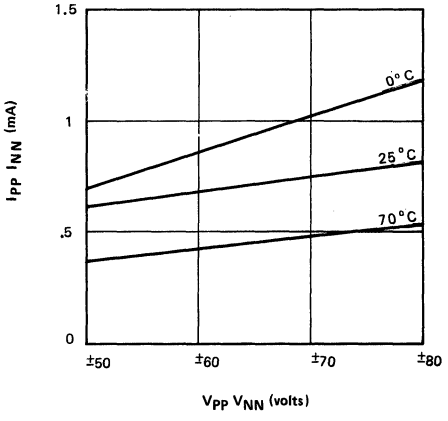
1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition of CK.
3. The clear input overrides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of LE. When LE is low, the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if LE is H.

Logic Diagram

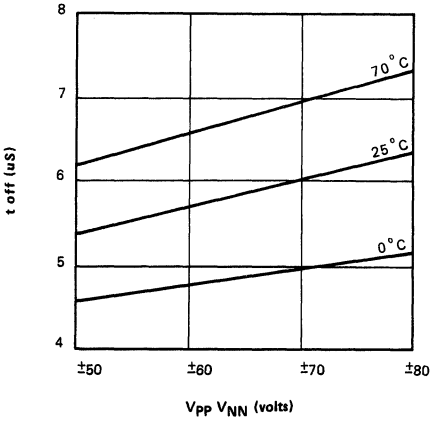


Typical Performance Curves

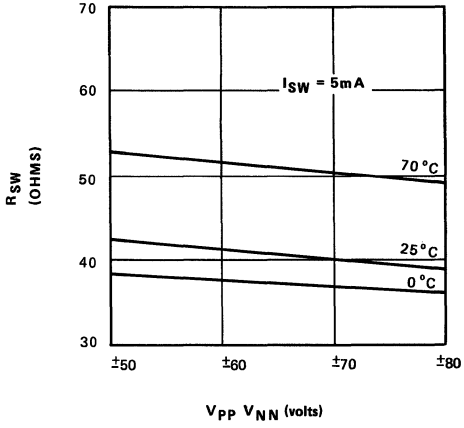
TYPICAL
I_{PP} I_{NN} vs. V_{PP} V_{NN} (ONE SWITCH ON)



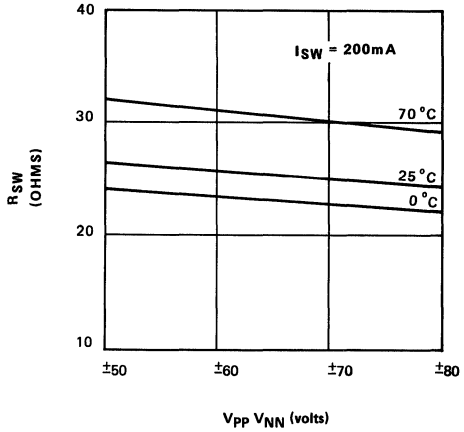
TYPICAL
t_{off} vs. V_{PP} V_{NN}



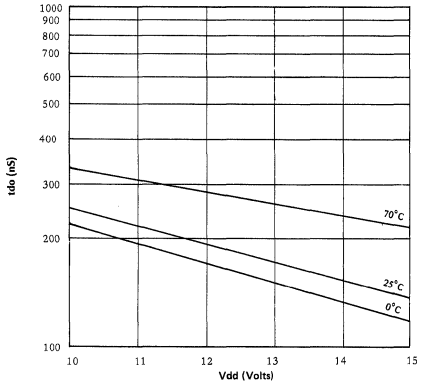
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



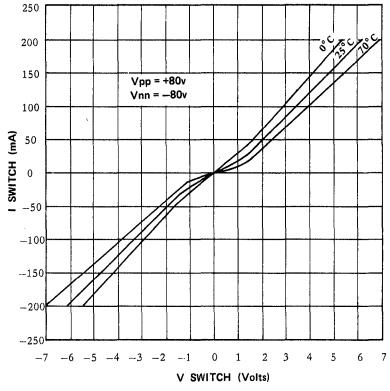
TYPICAL
R_{SW} vs. V_{PP} V_{NN}



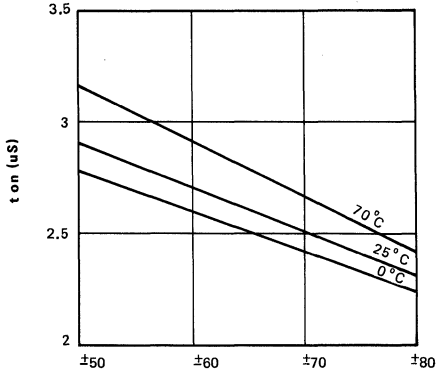
TYPICAL
tdo vs Vdd



TYPICAL
SWITCH CURRENT vs VOLTAGE



TYPICAL
t on (uS) vs. V_{PP} V_{NN}



Pin Configurations

36-Pin Leaded Chip Carrier

Pin	Function	Pin	Function
1	SW3	19	N/C
2	SW3	20	D_{IN}
3	N/C	21	CK
4	SW2	22	LE
5	SW2	23	CL
6	N/C	24	D_{OUT}
7	SW1	25	SW7
8	SW1	26	SW7
9	N/C	27	N/C
10	SW0	28	SW6
11	SW0	29	SW6
12	N/C	30	N/C
13	N/C	31	SW5
14	V_{PP}	32	SW5
15	V_{NN}	33	N/C
16	GND	34	SW4
17	V_{PP}	35	SW4
18	N/C	36	N/C

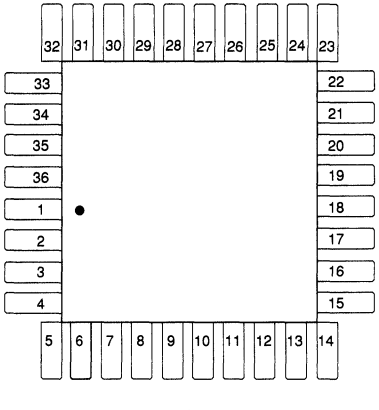
28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

28-Pin J-Lead

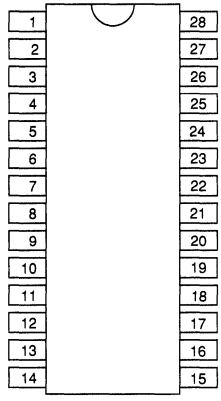
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

Package Outlines



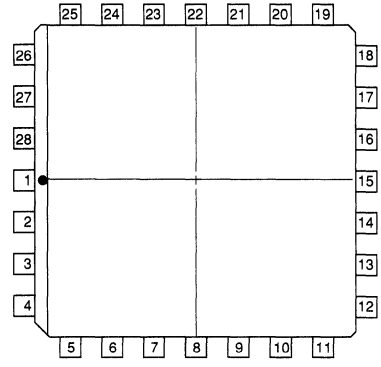
top view

36-pin Leaded Chip Carrier



top view

28-pin DIP



top view

28-pin J-lead Package