

8-Channel High Voltage Analog Switch

Ordering Information

V _{PP}	V _{NN}	V _{SIG}	Package Options		
			28-pin Plastic DIP	28-lead Plastic Chip Carrier	Die
+80V	-80V	130V _{P-P}	HV1816P	HV1816PJ	HV1816X

Features

- HVCMOS[®] technology
- Up to 130V peak to peak output switching
- Output On-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45dB typical output off isolation at 5MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip shift register, latch and clear logic circuitry

General Description

Not recommended for new designs. Please use HV202 instead.

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V _{DD} Logic power supply voltage	-0.5V to +18V
V _{PP} - V _{NN} supply voltage	174V
V _{PP} Positive high voltage supply	-0.5V to +90V
V _{NN} Negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5V to V _{DD} +0.3V
Analog signal range	V _{NN} to V _{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	1.2W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics

(over operating conditions, $V_{PP} = +80V$, $V_{NN} = -80V$ and $V_{DD} = 15V$ unless otherwise noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	$I_{SW} = 5mA$, $V_{SIG} = 0V$
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	$I_{SW} = 200mA$, $V_{SIG} = 0V$
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	$V_{PP} = +50V$, $V_{NN} = -50V$ $I_{SW} = 5mA$, $V_{SIG} = 0V$
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	$V_{PP} = +50V$, $V_{NN} = -50V$ $I_{SW} = 200mA$, $V_{SIG} = 0V$
Switch (ON) Resistance Matching	ΔR_{ONS}		15			15		15	%	$V_{PP} = +50V$, $V_{NN} = -50V$ $I_{SW} = 5mA$, $V_{SIG} = 0V$
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	μA	$V_{SIG} = V_{PP} - 10V$ thru $10K\Omega$ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	$R_L = 100K\Omega$
DC Offset Switch On			500		100	500		500	mV	$R_L = 100K\Omega$
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V $f = 1MHz$
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	μA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	μA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, $I_{SW} = 5mA$
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	$V_{SIG} = 0V$
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	$V_{PP} = +50V$, $V_{NN} = -50V$,
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, $I_{SW} = 5mA$
Switch Output Peak Current					1.5				A	$V_{SIG} \leq 0.1\%$ Duty Cycle, $f = 10KHz$
Logic Supply Average Current	I_{DD}				4	6			mA	$f_{CLK} = 3MHz$
Logic Supply Quiescent Current	I_{DDQ}				10	500			μA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	$V_{OUT} = V_{DD} - 0.7V$
Data Out Sink Current	I_{SINK}	0.7		0.8	0.9		0.7		mA	$V_{OUT} = 0.7V$

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before \overline{LE} Rises	t_{SD}			260					ns	
Time Width of \overline{LE}	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5.0		2.5	5.0	5.0		μs	$R_L = 10K\Omega$
Turn Off Time	t_{OFF}		10		5.0	10	10		μs	$R_L = 10K\Omega$
Time Width of CL	t_{WCL}			150					ns	
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Max Clock Freq	f_{CLK}					3.0			MHz	50% Duty Cycle $f_{DATA} = f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			35					ns	
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

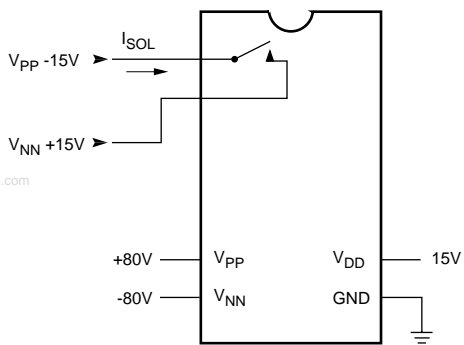
Operating Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	+50V to +80V
V_{NN}	Negative high voltage supply	-50V to -80V
V_{IH}	High level input voltage	$V_{DD} - 2V$ to V_{DD}
V_{IL}	Low-level input voltage	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	$V_{NN} + 15V$ to $V_{PP} - 15V$
T_A	Operating free air-temperature	0° to 70°C

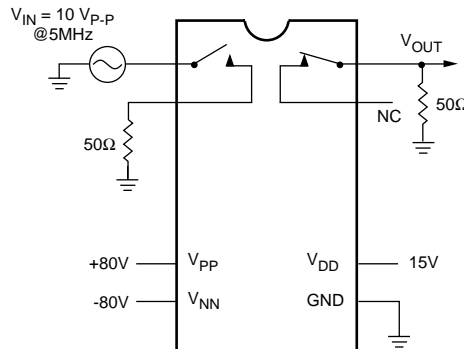
Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

Test Circuits

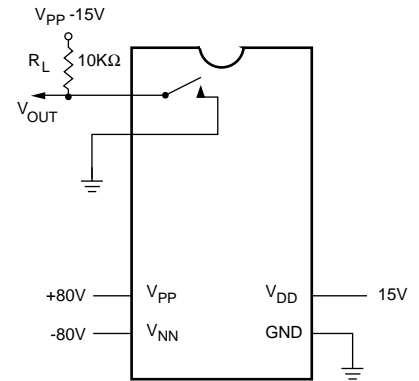


Switch OFF Leakage

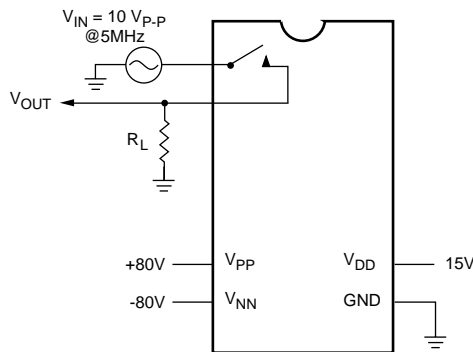


$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk

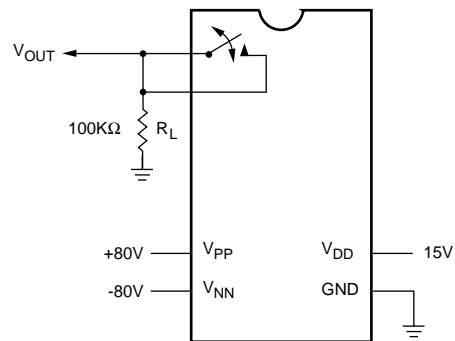


T_{ON}/T_{OFF}



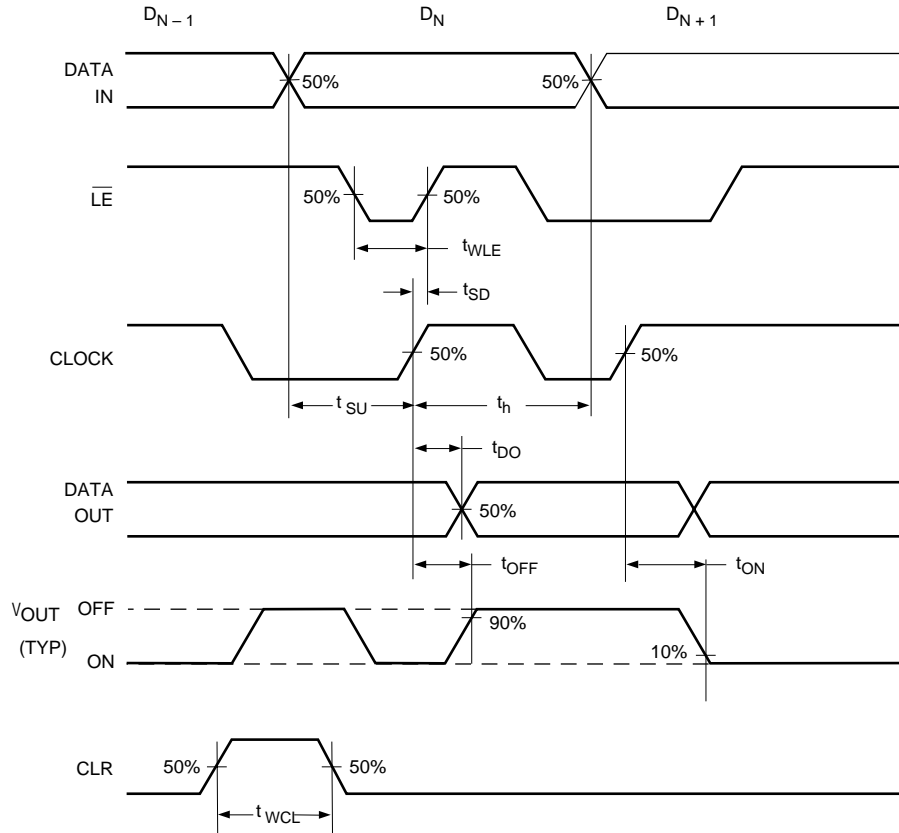
$$K_O = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation



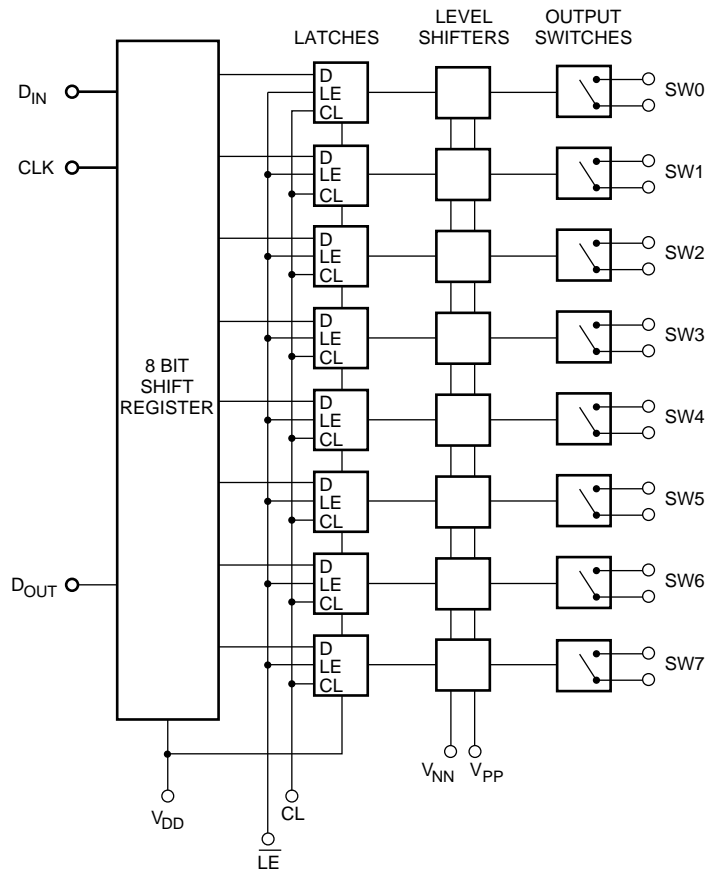
DC Offset ON/OFF

Logic Timing Waveforms



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Logic Diagram



Truth Table

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	\overline{LE}	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

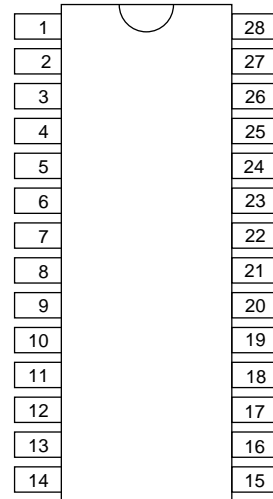
1. The eight switches operate independently.
2. Serial data is clocked in on the L → H transition CLK.
3. The clear input over rides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if \overline{LE} is H.

Pin Configurations

Package Outlines

28-Pin DIP

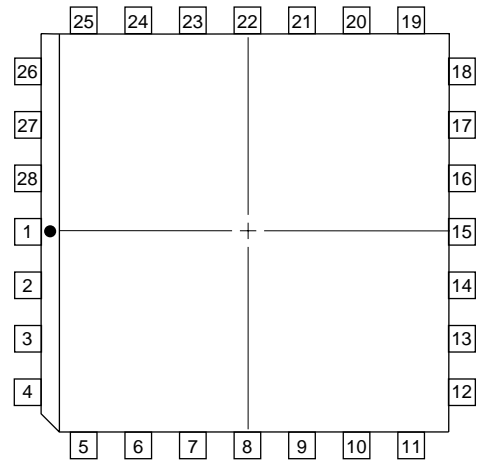
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D _{IN}
3	SW2	17	CLK
4	SW2	18	\overline{LE}
5	SW1	19	CL
6	SW1	20	D _{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V _{PP}	23	SW6
10	V _{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V _{DD}	27	SW4
14	N/C	28	SW4



top view
28-pin DIP

28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D _{IN}
3	SW2	17	CLK
4	SW2	18	\overline{LE}
5	SW1	19	CL
6	SW1	20	D _{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V _{PP}	23	SW6
10	V _{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V _{DD}	27	SW4
14	N/C	28	SW4



top view
28-pin J-Lead Package

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