TITLE: Product Specification of HV208QX1-100

Rev. A

BOE TFT-LCD SBU

BEIJING BOE OPTOELECTRONICS TECHNOLOGY
BOE HYDIS TECHNOLOGY

REVISION HISTORY

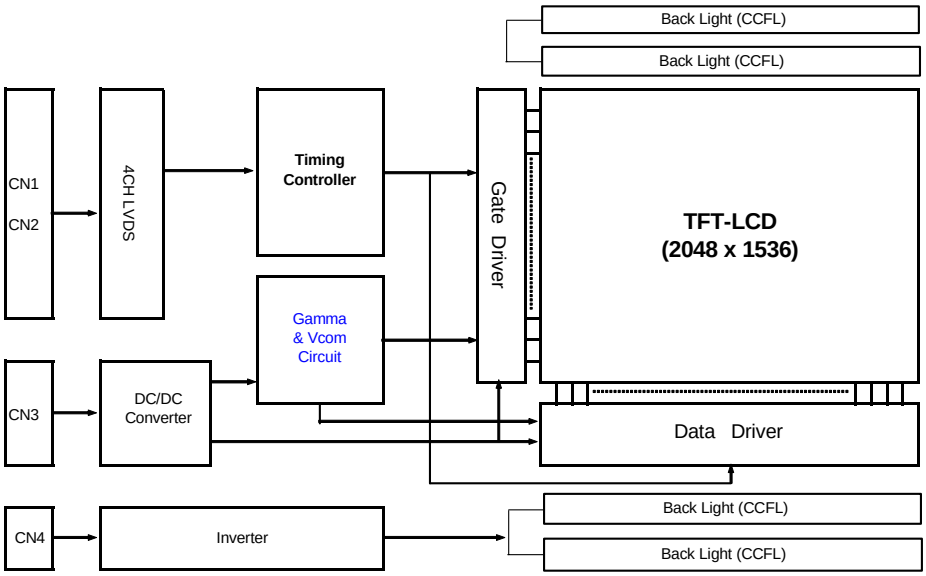
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
0		Initial Release	05.04.04	J.K Han
A	E0505-F019	Optical Specification Contents changed - VDim : 0.8V to 0.0V - Note2 Comment changed	05.07.08	J.K Han

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

This specification applies to the 20.8”(3M) Black & White Monochrome TFT LCD module “HV208QX1”. This module shows a wide viewing angle using unique True Black AFFS (Advanced Fringe Field Switching) Technology with Dual Domain. Basically, This module is controlled by amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has an 20.8 inch diagonally measured active area with QXGA resolutions (2048 horizontal by 1536 vertical pixel array). Supported gray scale is 8-bit per one sub-pixel. Input signal is 4CH LVDS (Low Voltage Differential Signaling) Interface compatible.



1.2 Features

- True Black AFFS(Advanced Fringe Field Switching) Technology with Dual Domain
- High luminance, High contrast ratio and Wide viewing angle
- Gray scale is 8-bit per one sub-pixel
- High speed response
- DE (Data Enable) only mode supports
- 4Ch LVDS Interface with dual pixel / clock
- Direct Type Back-Light (12 CCFL lamps)
- RoHS Adapted

1.3 Applications

- Medical Display

1.4 General Specifications

The following Items are general specifications of the model HV208QX1-100. (Listed in Table1)

<Table1 General Specifications>

Parameter	Specification	Unit	Remark
Active area	423.9(H) × 318.0(V)	mm	
Number of pixels	2048 × 3(H) × 1536(V)	Pixels	
Pixel pitch	0.207(H) × 0.207(V)	mm	
Display mode	Normally Black		
Dimensional outline	457.0(H) × 350.0(V) × 45.0(D)	mm	
Weight	2500 Typ.	gram	Note 1
Back-light	Direct Type (12 CCFL)		Note 2
Surface treatment	Haze 13, Anti-glare & hard-coating (3H)		

Note: 1. Weight Max. 2700g

* Weight 2,500 includes the weight of Shield Cover contrary to 2,300Typ. Of IDT 20.8”

2. CCFL (Cold Cathode Fluorescent Lamp)

2.0 ABSOLUTE MAXIMUM RATINGS

The following Table show maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table2.

<Table2 Absolute Maximum Ratings>

Parameter	Symbol	Min	Max	Unit	Remark
Logic & LCD Input Voltage	V_{DD}	-0.3	13.2	V	Ta = 25℃
Backlight Voltage	V_{INV}	-0.3	13.2	V	
Brightness Control	V_{DIM}	-0.3	5.3	V	
Backlight ON/OFF	B_{BLON}	-1.0	5.3	V	
Operating Temperature (Humidity)	T_{OP} RH	0 8	+50 80	℃ %RH	 ≤ 40 ℃
Storage Temperature (Humidity)	T_{ST} RH	-20 5	+60 95	℃ %RH	 ≤ 40 ℃

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics (Listed in Table3)

<Table3 Electrical specifications> (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Input Voltage	V_{DD}	11.4	12.0	12.6	V	
Inverter Power Input Voltage	V_{INV}	11.4	12.0	12.6	V	
Power Input Current	I_{DD}	-	500	750	mA	Note 1
"H" level Differential input	V_{IL}	100	-	-	mV	Note 2
"L" level Differential input	V_{IH}	-	-	-100	mV	
Back-light lamp Voltage	V_{BL}	-	700	-	Vrms	
Back-light lamp Current	I_{BL}	-	5.5	-	mArms	Per CCFL Note 3
Back-light Lamp Operating Frequency	F_L	-	60	-	KHz	
Lamp Start Voltage	V_S	-	1200	1550 (0°C)	Vrms	Note 4
		-	900	1100 (25°C)	Vrms	
Lamp Life	Hr	40,000	50,000	-	Hours	
Power Consumption	P_{DD}	-	6	-	W	
	P_{INV}	-	46.2	-	W	
	P_{total}	-	52.2	-	W	

Notes:

1. Test Pattern of power supply current
   - Typ: Vertical 8 Gray Bar
   - Max: White (@L255)

2. LVDS Receiver common mode voltage, V_{CM} = 1.2V
3. The lamp frequency should be selected as different as possible from the horizontal synchronous frequency and its harmonics to avoid interference which may cause line flow on the display.
   Back-light lamp Current measure condition : V_{INV}=12V, V_{DIM} : 0V
4. The voltage shown above should be applied to the lamps for more than 1 second to startup. Otherwise the lamps may not to be turned on.

4.0 OPTICAL SPECIFICATIONS

The optical characteristics are measured after 30 minutes warm-up period under 25℃ condition. Equipment for measurement is TOPCON-BM5. This Table shows optical specifications of the Model HV208QX1-100. (Listed in Table4)

<Table4 Optical Specifications>

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10 Horizontal & Vertical	80	89	-	Deg	Note 1
		Θ_9		80	89	-	Deg	
	Vertical	Θ_{12}		80	89	-	Deg	
		Θ_6		80	89	-	Deg	
White Luminance	TYP(V_{DIM}=0.0V)	L_{WTYP}	Θ = 0° Center	690	800	-	cd/m^2	Note 2
	Min(V_{DIM}=3.0V)	L_{WMIM}			100	200	cd/m^2	Note 9
Black Luminance		L_B			1.1	-		Note 2
Contrast Ratio		CR		-	700	-	-	Note 3
White Uniformity	Adjacent	A_WU	Θ = 0° 9Points	80	-	-	%	Note 4
	Total	T_WU		80	-	-		
Black Uniformity	Adjacent	A_BU		70	-	-	%	Note 5
	Total	T_BU		70	-	-		
White Balance	White x	Wx	Θ = 0° (Center)	0.264	0.294	0.324	-	Note 6
	White y	Wy		0.265	0.295	0.325		
Response time	Rising	Tr	Θ = 0° 10% to 90%	-	15	-	msec	Note 7
	Falling	Td		-	20	-		
Cross talk		CT	Θ = 0°	-	2.0	-	%	Note 8

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angle is determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface. (See Figure 1 shown in Appendix).

2. Each White/Black Luminance (L_W/L_B) is defined as the luminance of L255/L0 Gray level at the center 1 point on LCD surface. (See Figure 1 shown in Appendix).

3. Contrast Ratio measurements shall be made at viewing angle of Θ = 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

4. White Uniformity on LCD surface is defined as follows : Where,
   L_{MAX}: The brightest luminance at the measuring points of whole area of white state.
   L_{MIN}: The darkest luminance at the measuring points of whole area of white state.
   L_{Bright}: Bright luminance among the measuring points of adjacent area of white state.
   L_{Dark}: Dark luminance among the measuring points of adjacent area of white state.

4.1 Adjacent White Uniformity (A_WU) is defined as the Minimum value of the Adjacent Luminance Uniformity Ratio. Measuring points are 9 points. (See Figure2 of Appendix)

$$\text{Adjacent Luminance Uniformity Ratio} = \frac{L_{Dark}}{L_{Bright}} \times 100\%$$

4.2 Total White Uniformity (T_WU) is defined as the Value of the Total Luminance Uniformity Ratio. Measuring points are 9 points. (See Figure2 of Appendix)

$$\text{Total Luminance Uniformity Ratio} = \frac{L_{Min}}{L_{Max}} \times 100\%$$

5. Black Uniformity on LCD surface is defined as follows : Where,
   L_{MAX}: The brightest luminance at the measuring points of whole area of black state.
   L_{MIN}: The darkest luminance at the measuring points of whole area of black state.
   L_{Bright}: Bright luminance among the measuring points of adjacent area of black state.
   L_{Dark}: Dark luminance among the measuring points of adjacent area of black state.

5.1 Adjacent Black Uniformity (A_BU) is defined as the Minimum value of the Adjacent Luminance Uniformity Ratio. Measuring points are 9 points. (See Figure2 of Appendix)

$$\text{Adjacent Luminance Uniformity Ratio} = \frac{L_{Dark}}{L_{Bright}} \times 100\%$$

5.2 Total Black Uniformity (T_BU) is defined as the Value of the Total Luminance Uniformity Ratio. Measuring points are 9 points. (See Figure2 of Appendix)

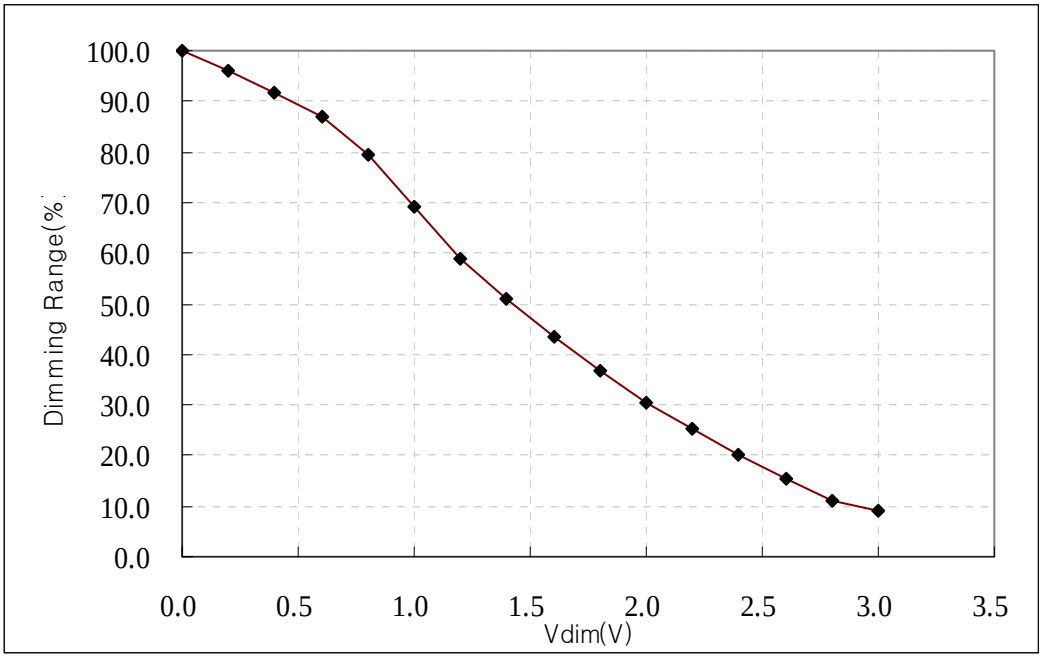
$$\text{Total Luminance Uniformity Ratio} = \frac{L_{Min}}{L_{Max}} \times 100\%$$

6. The White balance chromaticity coordinate shall be calculated from the spectral data measured with white state. Measurements shall be made at the center of the panel.

7. The electro-optical response time measurements shall be made as Figure 3 shown in Appendix by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

8. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See Figure 4 shown in Appendix).

9. This following chart is V_{DIM} vs Dimming Range for you reference



5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection(Digital Signal Connector)

The module-side connector : FI-TWE31PB-VF or Equivalent

The user-side connector : FI-W31S or FI-WE31M or Equivalent

<Table5 Pin Assignment for Receiver Interface Connection>

CN1(Master, Left Side) Pin Assignment			CN2 Pin Assignment		
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	No connection	1	VBLON	Backlight On/Off Signal
2	NC	No connection	2	VDIM_IN	Note1)
3	NC	No connection	3	VDIM_OUT	Note2)
4	NC	No connection	4	NC	No connection
5	NC	No connection	5	NC	No connection
6	GND	Ground	6	GND	Ground
7	SDATA	I2C Data for Brightness	7	NC	No connection
8	SCLK	I2C Clock(3.3V typ)	8	NC	No connection
9	GND	Ground	9	GND	Ground
10	GND	Ground	10	GND	Ground
11	LLVDO3+	Positive LVDS signal(Odd)	11	RLVDO3+	Positive LVDS signal(Odd)
12	LLVDO3-	Negative LVDS signal(Odd)	12	RLVDO3-	Negative LVDS signal(Odd)
13	LLVCLKO+	Positive LVDS clock(Odd)	13	RLVCLKO+	Positive LVDS clock(Odd)
14	LLVCLKO-	Negative LVDS clock(Odd)	14	RLVCLKO-	Negative LVDS clock(Odd)
15	LLVDO2+	Positive LVDS signal(Odd)	15	RLVDO2+	Positive LVDS signal(Odd)
16	LLVDO2-	Negative LVDS signal(Odd)	16	RLVDO2-	Negative LVDS signal(Odd)
17	LLVDO1+	Positive LVDS signal(Odd)	17	RLVDO1+	Positive LVDS signal(Odd)
18	LLVDO1-	Negative LVDS signal(Odd)	18	RLVDO1-	Negative LVDS signal(Odd)
19	LLVDO0+	Positive LVDS signal(Odd)	19	RLVDO0+	Positive LVDS signal(Odd)
20	LLVDO0-	Negative LVDS signal(Odd)	20	RLVDO0-	Negative LVDS signal(Odd)
21	LLVDE3+	Positive LVDS signal(Odd)	21	RLVDE3+	Positive LVDS signal(Odd)
22	LLVDE3-	Negative LVDS signal(Odd)	22	RLVDE3-	Negative LVDS signal(Odd)
23	LLVCLKE+	Positive LVDS clock(Even)	23	RLVCLKE+	Positive LVDS clock(Even)
24	LLVCLKE-	Negative LVDS clock(Even)	24	RLVCLKE-	Negative LVDS clock(Even)
25	LLVDE2+	Positive LVDS signal(Even)	25	RLVDE2+	Positive LVDS signal(Even)
26	LLVDE2-	Negative LVDS signal(Even)	26	RLVDE2-	Negative LVDS signal(Even)
27	LLVDE1+	Positive LVDS signal(Even)	27	RLVDE1+	Positive LVDS signal(Even)
28	LLVDE1-	Negative LVDS signal(Even)	28	RLVDE1-	Negative LVDS signal(Even)
29	LLVDE0+	Positive LVDS signal(Even)	29	RLVDE0+	Positive LVDS signal(Even)
30	LLVDE0-	Negative LVDS signal(Even)	30	RLVDE0-	Negative LVDS signal(Even)
31	GND	Ground	31	GND	Ground

Note1) Brightness Dimming Control Voltage (0 ~ 3.0V, 0V : Max Brightness)
Note2) Brightness Dimming Control Voltage(Generated by I2C data)
Note3) LVDS signal & clock should be wired by twist – pairs or side by side FPC patterns, respectively

5.2 CN3 in Assignment (Analog Power Connector)

The module-side connector : IL-Z-8PL-SMTYE(JAE) or Equivalent

The user-side connector : IL-Z-8S-S125C3 or Equivalent

<Table6 Pin Assignment for Power Interface Connection>

Pin No.	Symbol	Description
1 ~ 4	GND	Ground
5 ~ 8	VIN	+12[V] Power supply for LCD Module Power

5.3 CN4 in Assignment (Inverter Connector)

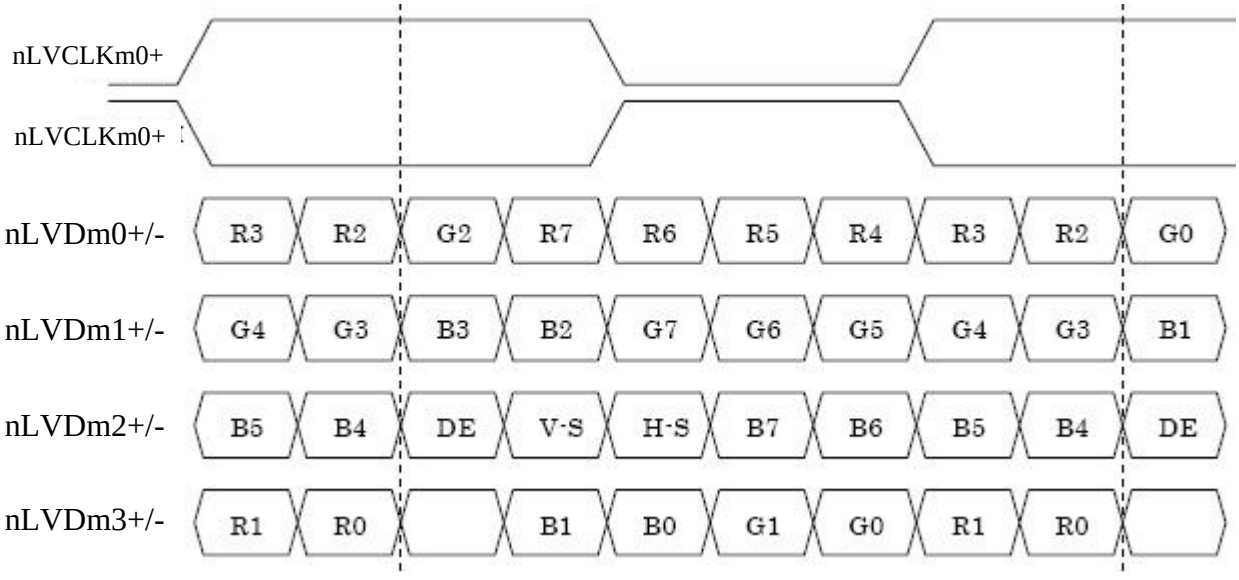
The module-side connector : S12B-PH-SM3-TB(JST) or Equivalent

The user-side connector : PHR-12 or Equivalent

<Table7 Pin Assignment for Inverter Interface Connection>

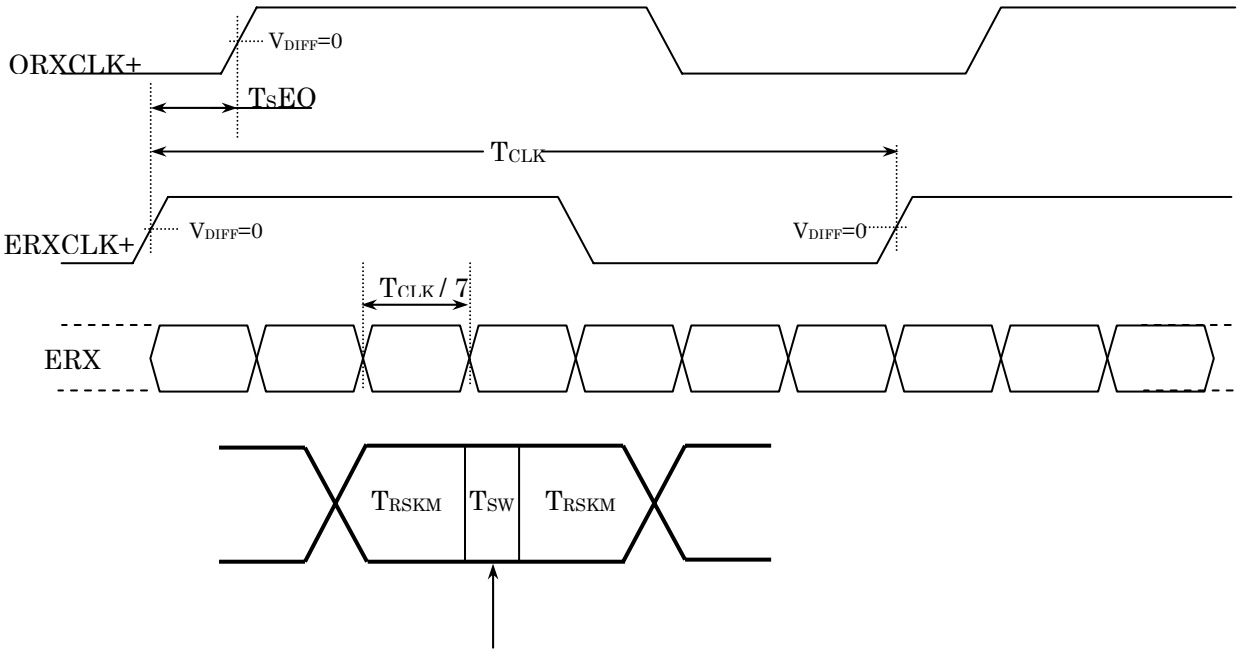
Pin No.	Symbol	Description
1 ~ 5	VBL	+12[V] Power supply for Inverter
6 ~ 10	GND	Ground
11, 12	NC	No Connection

5.4 LVDS Data Mapping((n : L or R, m : D or CLK)

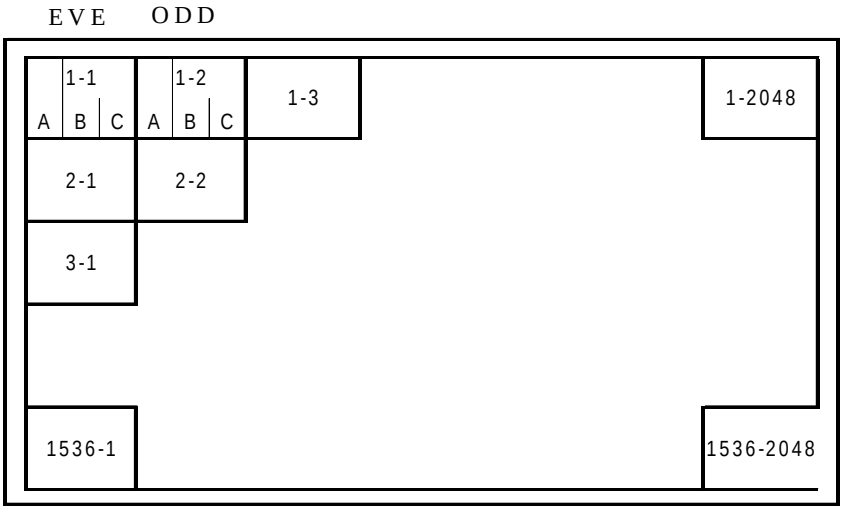


5.5 LVDS Macro AC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{SW}	Sampling Window				820	ps
T_{RSKM}	Receiver Skew Margin	F_{CLK} = 75MHz	540			ps
T_SEO	Skew - Even to Odd port		-3/7		3/7	T_{CLK}



5.6 Data Input Format



6.0 SIGNAL TIMING SPECIFICATIONS

The specification of the signal timing parameter is listed in Table 7.

The HV208QX1-100 is operated by DE only mode.

Therefore Horizontal sync & Vertical Sync. are not used in HV208QX1-100.

<Table 7 Signal Timing Specifications>

ITEM		Symbol	Min.	Typ.	Max.	Unit
Input Clock Frequency		Fc	60	65	66	MHz
		Tc	15.15	15.38	16.66	ns
Horizontal	Scan Rate	Fh	92.86	96.72	96.72	KHz
		Th	10.34	10.34	10.77	us
	Horizontal Active	Tha	-	1024	-	pixel
	Hsync Front Porch	Thfp	-	12	-	Tc
	Hsync Active Width	Thaw	-	68	-	Tc
	Hsync Back Porch	Thbp	-	80	-	Tc
	Horizontal Total	Tht	-	1344	-	pixel
Vertical	Scan Rate (Frame Rate)	Fv	-	60	-	Hz
		Tv	-	16.6	-	ms
	Vertical Active	Tva	-	1536	-	Lines
	Vsync Front Porch	Tvfp	-	6	-	Lines
	Vsync Active Width	Tvsw	-	12	-	Lines
	Vsync Back Porch	Tvbp	-	58	-	Lines
	Vertical Total	Tvt	1547	1612	1628	Lines

7.0 I2C SPECIFICATIONS

Following describes the I2C specifications equipped in the LCD module. Since the DAC (DALLAS DS1803) is used for Brightness and Contrast, Please refer to its own specifications in detail. 2 signals (SCLK and SDATA) in the LCD module interface are used for the DAC.

The address for DAC is '0101101'b. Its port-0 is for Contrast and its port-1 is for Brightness. Reserved addresses are from '0010000'b to '0011111'b and from '0110000'b to '0111111'b.

7.1 I2C Feature Summary

- Standard mode (100KHz max) support
- 3.3V interface
- Slave mode operation only

7.2 Electrical Specification

2 signals (SCLK and SDATA) are equipped at the LCD module interface. SCLK is the clock input as SCL and SDATA is the data input/output as SDA. These signals should be driven by Open-Drain or Open-Collector without any pull-up resister. Both signals are pulled up by 5.1K ohm resisters to 3.3V typ respectively in the LCD module.

Electrical Specification of C/A

	Symbol	Min	Max	Unit
Input Low voltage (*1)	Vil	-0.5	0.5	V
Input High voltage (*2)	Vih	2.3	3.6	V
Input Hysteresis voltage	Vhys	0.4	-	V
Input leakage current @ Vil-Min or Vih-Max (*3)	Ii	-30	30	uA
Output Low voltage	Vol	-	0.5	V
Output High impedance leakage current (*3)	Ioh	-30	30	uA
Input capacitance	Ci	-	35	pF

NOTE :

*1 : Vil (typ) = 0.9V

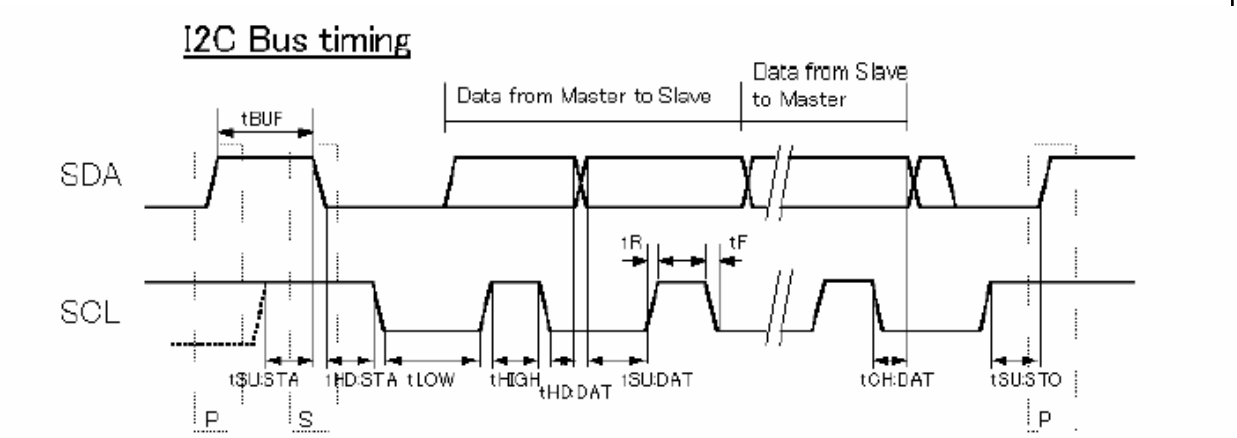
*2 : Vih (typ) = 1.8V

*3 : without pull up resister (5.1K ohm)

7.3 Timing Specification

In the following figure and table, Slave is the control ASICs in the LCD module and Master is the controller to drive the LCD module.
"S" is the START condition and "P" is the STOP condition.

< I2C Bus timing >



Timing Specification of C/A

	Symbol	Min	Max	Unit
Frequency of SCL	fSCL	0	100	KHz
Bus Free Time from STOP to START	tBUF	4.7	-	us
Setup time of START	tSU:STA	4.7	-	us
Hold time of START	tHD:STA	4	-	us
Low time of SCL	tLOW	4.7	-	us
High time of SCL	tHIGH	4	-	us
Data hold time for Slave	tHD:DAT	0	-	us
Data setup time for Slave	tSU:DAT	250	-	ns
Data change from SCL falling edge (to Master)	tCH:DAT	300	900	ns
Rise time Vil-Max --> Vih-Min	tR	-	1000	ns
Fall time Vil-Max <-- Vih-Min	tF	-	300	ns
Setup time of STOP	tSU:STO	4	-	us
Spike suppression	tSP	-	50	ns

8.0 INPUT SIGNALS, GRAY SCALE DISPLAY AT EACH SUB-PIXEL

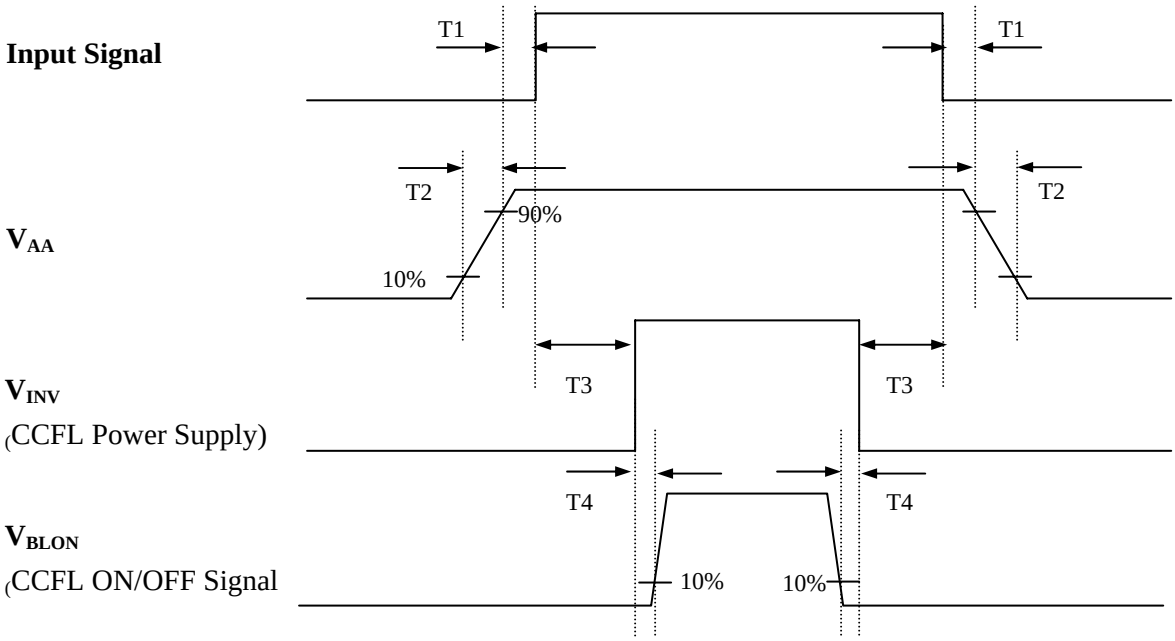
Each pixel is displayed in 256 gray scales from 8bit data signal inputs. Table 8 shows the 8bit input signals for gray scale display at each sub-pixel.

<Table 8 8bit Input signals, Gray scale display at each sub-pixel >

		Data Signal																											
	ODD	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	EVEN	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
Gray Scale of A Sub Pixel	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽ Brighter	↓								↓								↓							
	▽	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of B Sub Pixel	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	▽ Brighter	↓								↓								↓							
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of C Sub Pixel	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	▽ Brighter	↓								↓								↓							
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	▽ Brighter	↓								↓								↓							
	▽	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	White	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as shown in below



- T1 ≥ 30 (ms)
- T2 ≤ 30 (ms)
- T3 ≥ 250 (ms)
- T4 ≥ 5 (ms)

Note: Do not keep the interface signal high-impedance when power is on.

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 5 & 6, shown in Appendix, shows mechanical outlines for the model HV208QX1-100 . Other parameters are shown in Table 10.

<Table10 Dimensional Parameters>

Parameter	Specification	Unit	Remark
Active area	423.9 (H) X 318.0 (V)	mm	
Number of pixels	2048 (H) X 1536 (V)	pixels	
Pixel pitch	0.207 (H) X 0.207 (V)	mm	
Pixel arrangement	Gray Vertical stripe		
Display colors	16,777,216	colors	
Display mode	Normally Black		
Outline dimension	457.0 (H) X 350.0 (V) X 45(D)	mm	1)
Weight	2500 Typ.	gram	2)
Back-light	Direct 12-CCFL type		

1) General tolerance : H & V = ±0.5mm / D = ±0.5mm
2) 2700 Max.

10.2 Mounting

See FIGURE 5 & 6, shown in Appendix

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a hard coating to reduce scratch.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50 cm from the screen with an overhead light level of 300lux.

11.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table11 Reliability test>

No.	Test Items	Conditions
1	High temperature storage test	Ta = 60 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240 hrs
3	High temperature & high humidity	Ta = 50 °C, 80 %RH, 240 hrs
4	High temperature operation test	Ta = 50 °C, 240 hrs
5	Low temperature operation test	Ta = 0 °C, 240 hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle
7	Vibration test (non-operating)	Frequency : 10 - 200 - 10 Hz, 0.29Oct./min Gravity/AMP : 1.5G Period : X,Y,Z 30min
8	Shock test (non-operating)	Gravity : 50G Pulse width : 11 ms, half sine wave Direction : ±X, ±Y, ±Z Two Times for each direction
9	Electrostatic discharge test	Contact : 150 pF, 330Ω, ±8KV 9 Points Air : 150 pF, 330Ω, ±15KV 9 Points

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back-light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose MCLK, DE signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to user the original shipping packages.

13.0 APPENDIX

Figure 1) Measurement Set Up

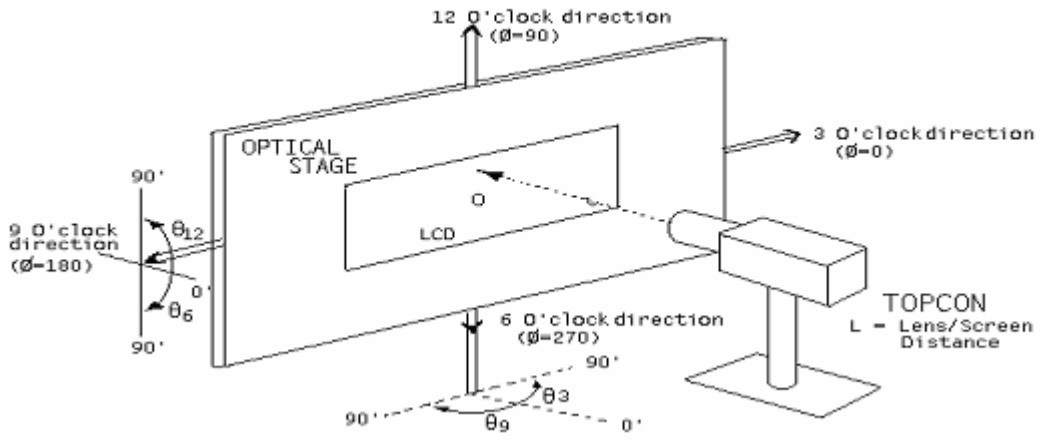


Figure 2) White and Black Uniformity Measurement Points (9 Points)

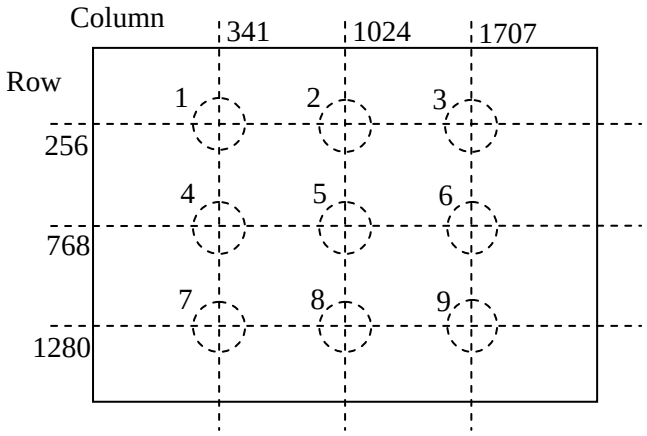


Figure 3) Response Time Testing

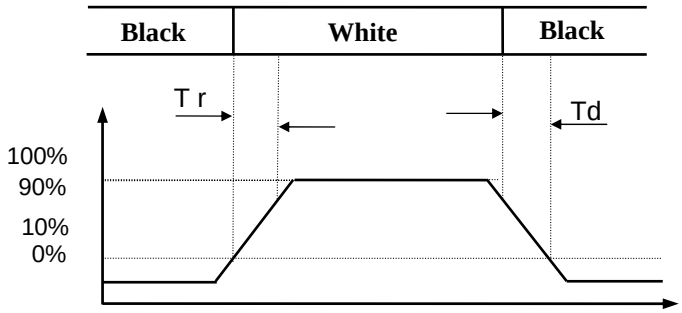
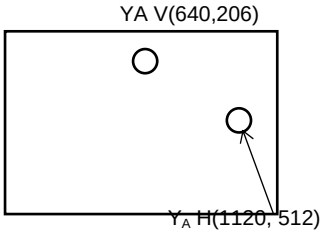
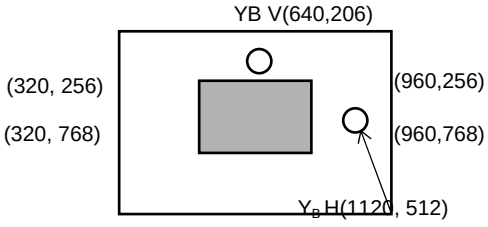


Figure 4) Cross Modulation Test Description

VIEW AREA



VIEW AREA



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns

Figure 5) TFT-LCD Module Outline dimensions (Front view)

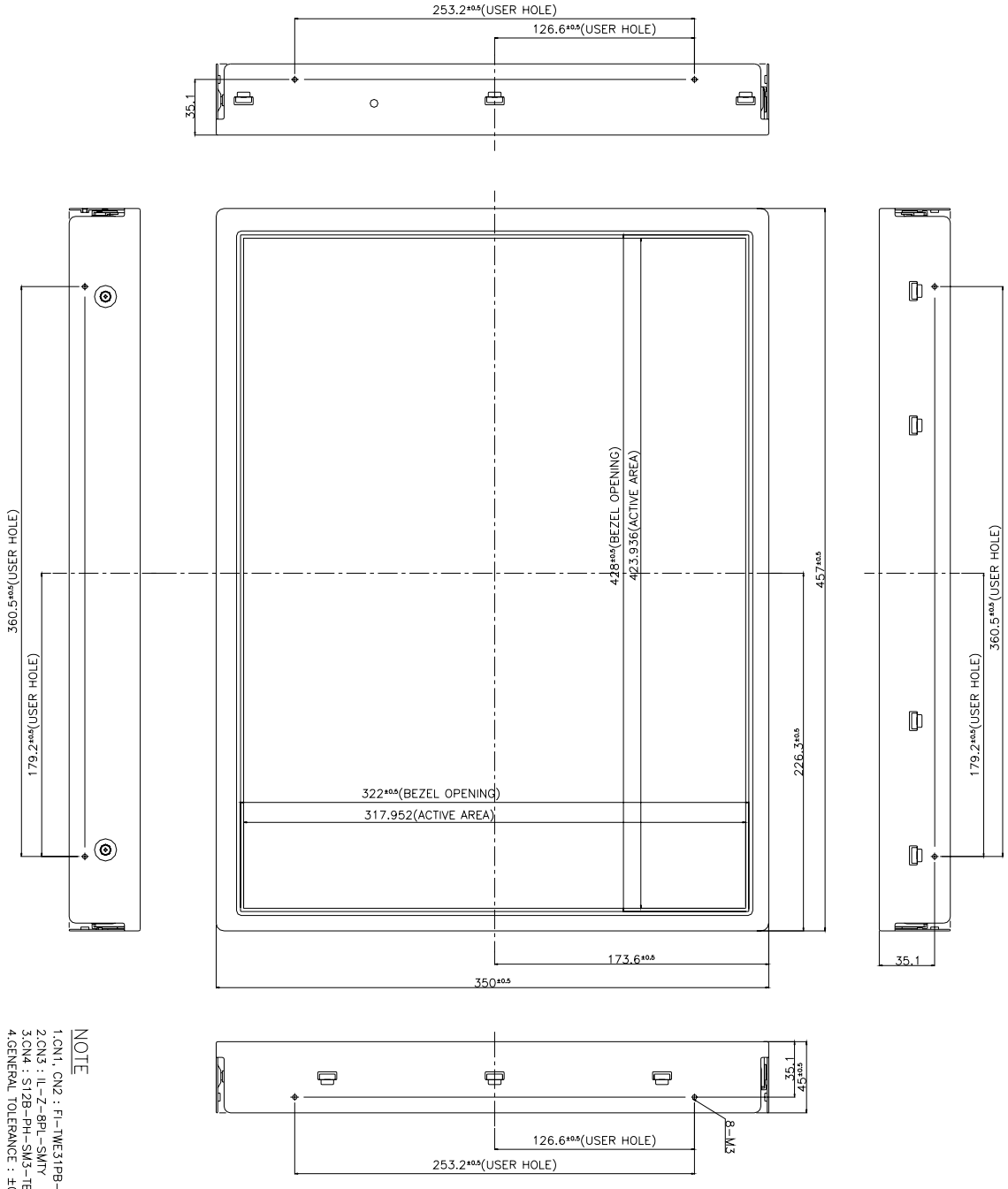


Figure 6) TFT-LCD Module Outline Dimensions (Back view)