Low Charge Injection 8-Channel High Voltage Analog Switches

Features

- HVCMOS® technology for high performance
- Very low quiescent power dissipation – 10µA
- Output on-resistance typically 22 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- -60dB typical output off isolation at 5MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- On-chip shift register, latch and clear logic circuitry
- Flexible high voltage supplies

Applications

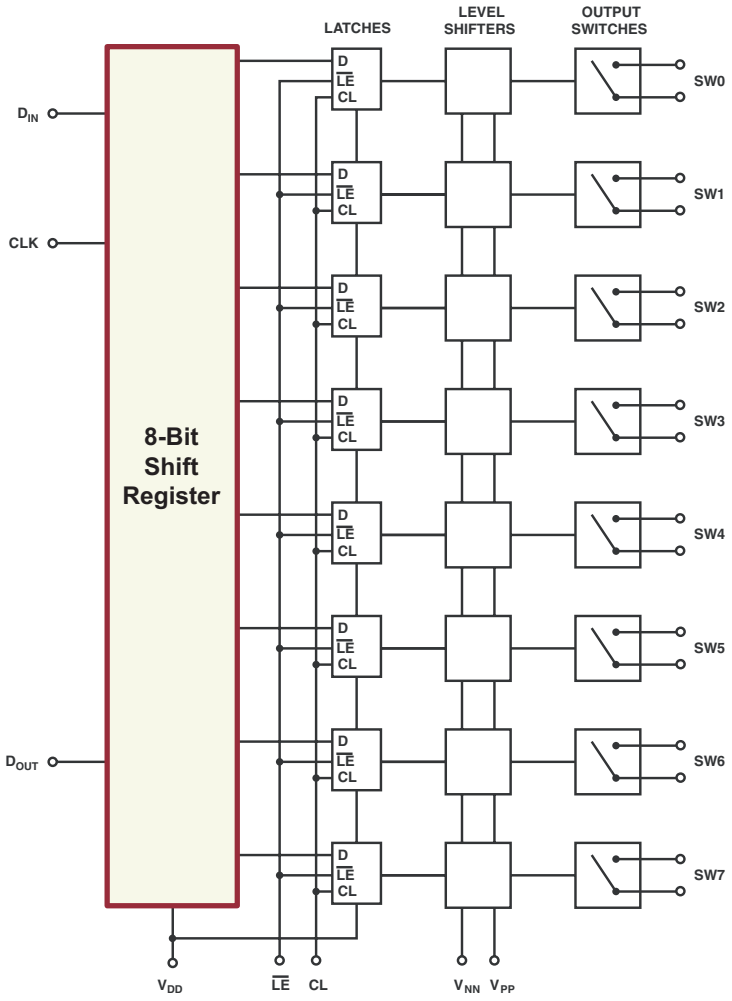
- Medical ultrasound imaging
- Piezoelectric transducer drivers

General Description

These devices are low charge injection 8-channel high-voltage analog switch integrated circuits (ICs) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, these switches combine high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

These ICs are suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/–150V, or +100V/–100V.B

Block Diagram



Ordering Information

Device	Package Options		
	28-Lead PLCC	48-Lead LQFP/TQFP (1.4mm)	25-Ball fpBGA
HV220	-	-	HV220GA
			HV220GA-G
HV20220	HV20220PJ	HV20220FG	-
	HV20220PJ-G	HV20220FG-G	
HV20320	HV20320PJ	-	-
	HV20320PJ-G		

-G indicates the part is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} supply voltage	220V
V_{PP} positive high voltage supply	-0.5V to V_{NN} +200V
V_{NN} negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation: 28-Lead PLCC 48-Lead LQFP/ TQFP(1.4mm) 25-Ball fpBGA	 1.2W 1.0W 1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Operating Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage [1,3]	4.5V to 13.2V
V_{PP}	positive high voltage supply [1,3]	40V to V_{NN} +200V
V_{NN}	negative high voltage supply [1,3]	-40V to -160V
V_{IH}	High level input voltage	V_{DD} -1.5V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V [2]
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbtrary except GND must be powered -up first and powered down last.*
2. *V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.*

Product Marking

Top Marking

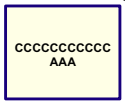
Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

HV20220 FG

Top Marking

Bottom Marking



YY = Year Sealed
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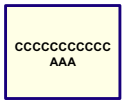
**May be part of top marking*

HV20220 PJ

Top Marking

Bottom Marking



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_____ = "Green" Packaging
**May be part of top marking*

HV20320 PJ

Top Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

HV20220 GA

DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5mA	V_{PP} = +40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5mA	V_{PP} = +100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25	-	30		I_{SIG} = 5mA	V_{PP} = +160V, V_{NN} = -40V
		-	22	-	16	25	-	27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = - 100V	
R_{ONL}	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V_{SIG} = V_{PP} -10V, I_{SIG} = 1.0A	
I_{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V, V_{NN} +10V	
V_{OS}	DC offset switch off	-	300	-	100	300	-	300	mV	R_L = 100Ω	
	DC offset switch on	-	500	-	100	500	-	500	mV	R_L = 100kΩ	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches off	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches on, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches on, I_{SW} = 5.0mA	
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycly < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V, V_{NN} = -40V	
I_{NN}	Supply curent	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V, V_{NN} = -160V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V, V_{NN} = -40V	
I_{DD}	Logic supply average current	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Logic supply Quiescent current	-	10	-	-	10	-	10	µA	---	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} -0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

(Over recommended operating conditions: V_{DD} = 5.0V, unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	150		150			150		ns	---
t_{WLE}	Time width of $\overline{LE}$	150		150			150		ns	---
t_{DO}	Clock delay time to data out		150			150		150	ns	---
t_{WCL}	Time width of CL	150		150			150		ns	---
t_{SU}	Set up time data to clock	15		15	8.0		20		ns	---
t_H	Hold time data from clock	35		35			35		ns	---
f_{CLK}	Clock frequency		5.0			5.0		5.0	MHz	50% Duty cycle, $f_{DATA} = f_{CLK}/2$
t_R, t_F	Clock rise and fall times		50			50		50	ns	---
t_{ON}	Turn on time		5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10kΩ
t_{OFF}	Turn off time		5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10kΩ
dv/dt	Maximun V_{SIG} slew rate		20			20		20	V/ns	V_{PP} = +160V, V_{NN} = -40V
			20			20		20		V_{PP} = +100V, V_{NN} = -100V
			20			20		20		V_{PP} = +40V, V_{NN} = -160V
K_O	Off isolation	-30		-30	-33		-30		dB	f = 5.0MHz, 1kΩ/15pF load
		-58		-58			-58			f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60		-60	-70		-60		dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current		300			300		300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
QC	Charge injection	-	-	-	820	-	-	-	pC	V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V
		-	-	-	600	-	-	-		V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V
		-	-	-	350	-	-	-		V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V

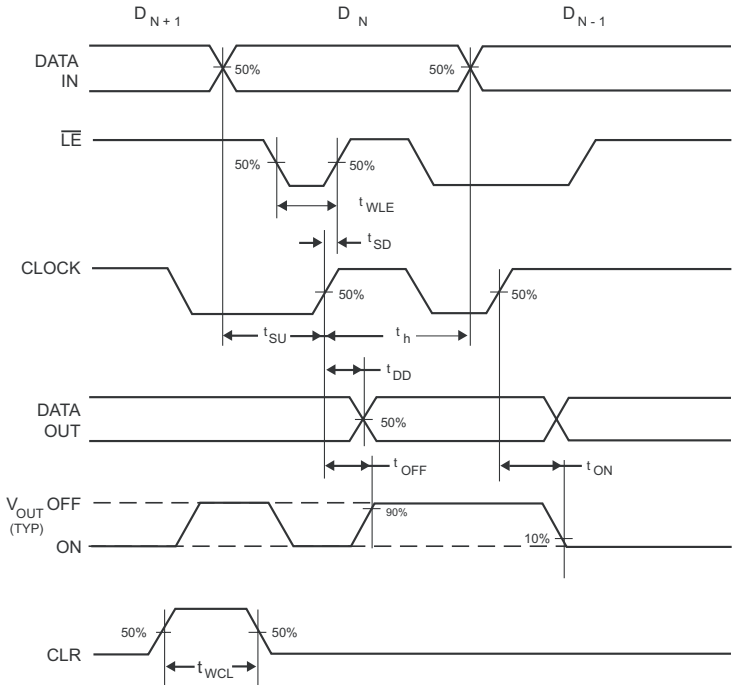
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	All Switches Off							

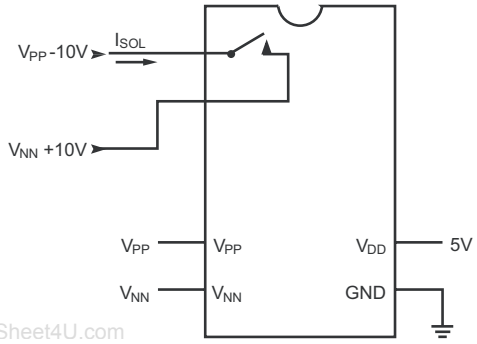
Notes:

1. *The eight switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flow through the latch.*
4. *D_{OUT} is high when data in the shift register 7 is high.*
5. *Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The CLR clear input overrides all other inputs.*

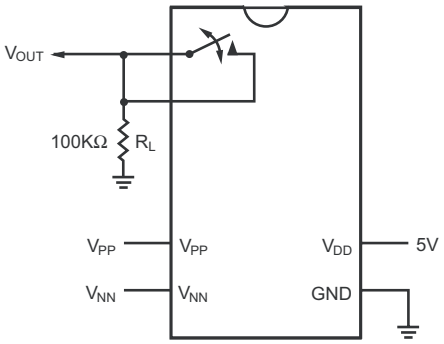
Logic Timing Waveforms



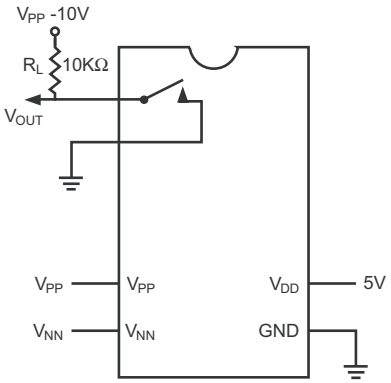
Test Circuits



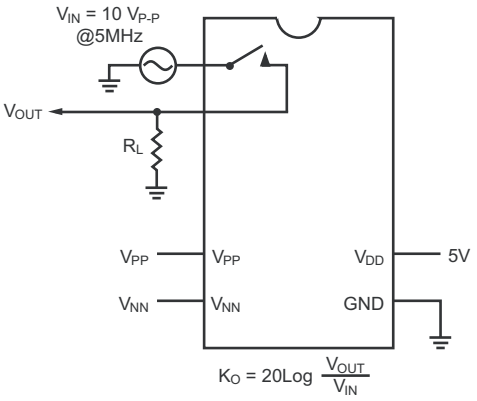
Switch OFF Leakage



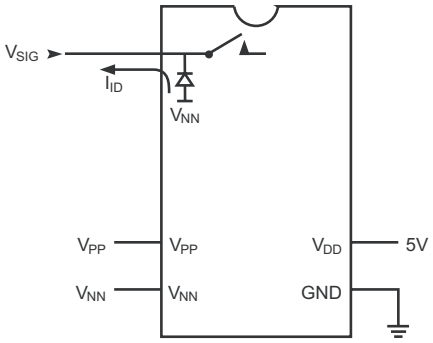
DC Offset ON/OFF



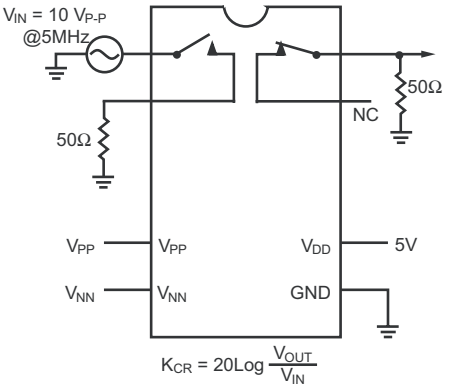
T_{ON}/T_{OFF} Test Circuit



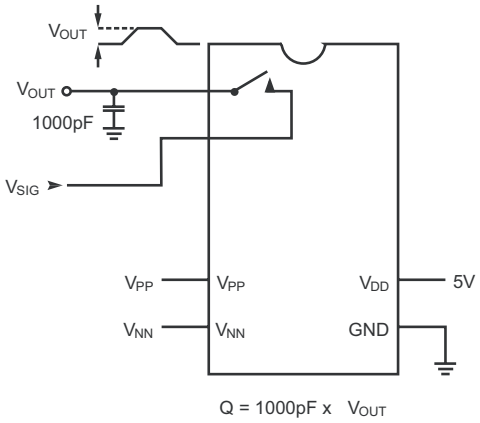
OFF Isolation



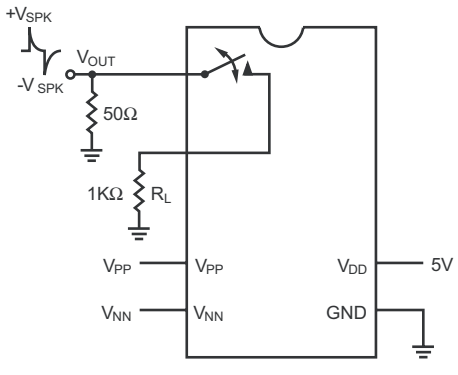
Isolation Diode Current



Crosstalk



Charge Injection

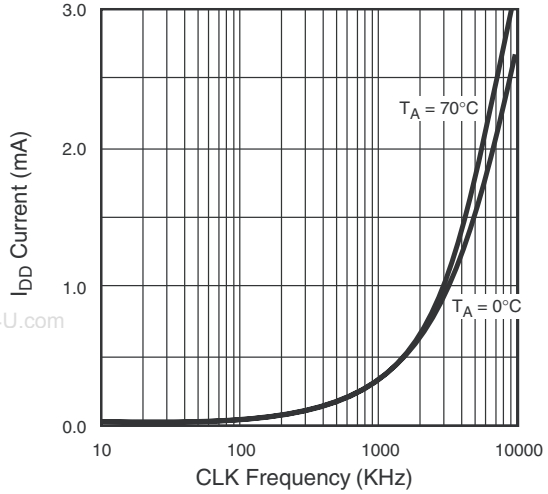


Output Voltage Spike

Typical Performance Curves

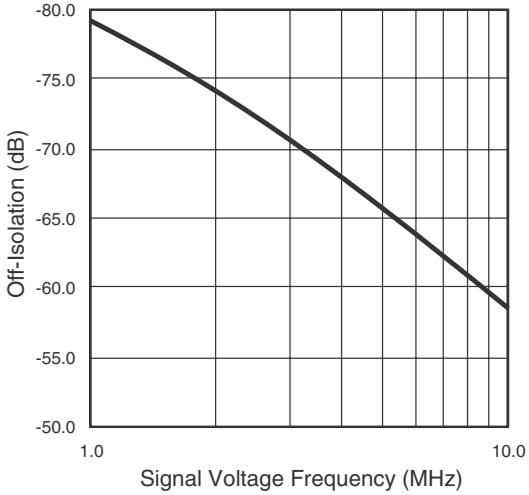
I_{DD} vs Clock Frequency

V_{DD} = 5.0V, V_{PP}/V_{NN} = ±100V, T_A = 0°C to 70°C



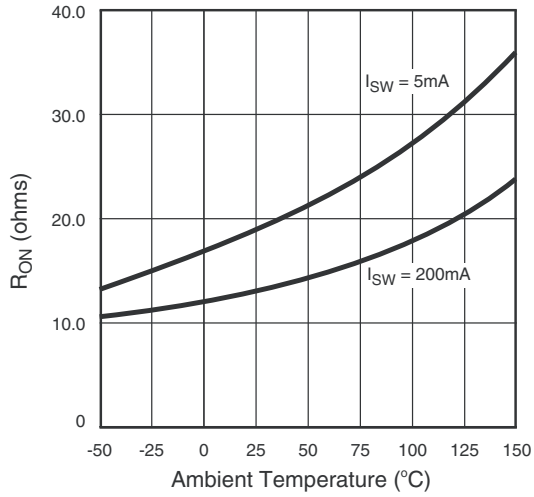
Off-Isolation vs. Signal Voltage Frequency

V_{DD} = 5.0V, V_{PP}/V_{NN} = ±100V



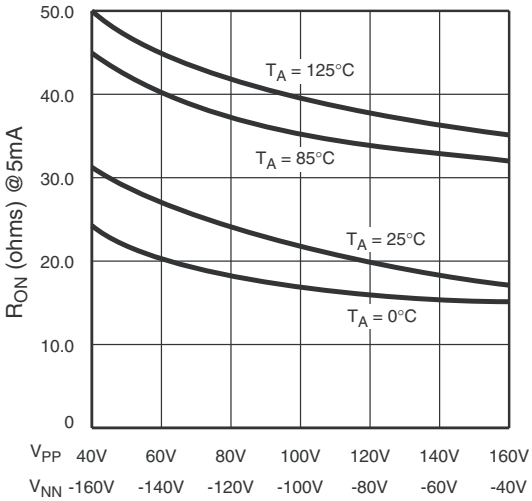
R_{ON} vs. Ambient Temperature T_A

V_{DD} = 5.0V, V_{PP}/V_{NN} = ±100V



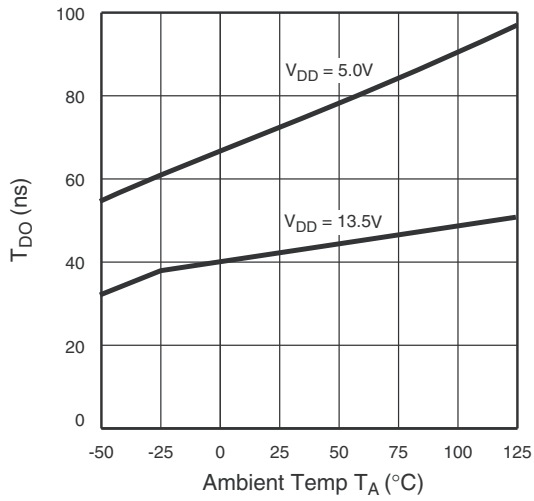
R_{ON} vs. V_{PP}/V_{NN}

V_{DD} = 5.0V



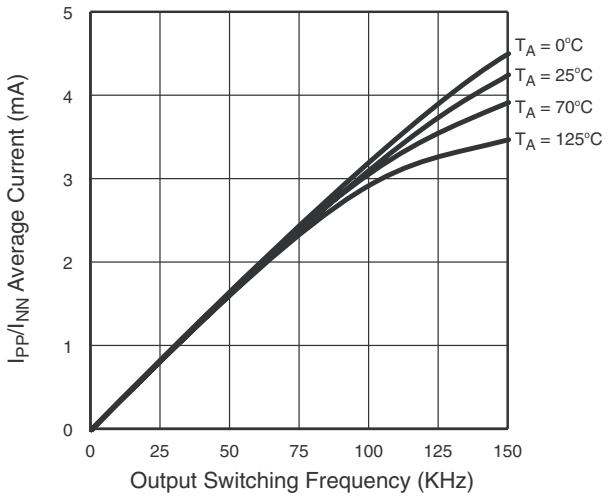
T_{DO} vs. Ambient Temperature T_A

V_{PP}/V_{NN} = ±100V



I_{PP}/I_{NN} vs. Output Switching Frequency

V_{DD} = 5.0V, V_{PP}/V_{NN} = ±100V



Pin Description (HV220GA)

Ball Location	Function
A3	SW1
B2	SW2
B3	SW1
B4	SW0
B5	SW0
B6	V_{NN}
C1	SW3
C2	SW3
C3	SW2
C4	V_{PP}
C5	GND
C6	D_{IN}
C7	V_{DD}
D1	SW4
D2	SW4
D3	SW5
D4	SW7
D5	$\overline{LE}$
D6	CLK
E2	SW5
E3	SW6
E4	SW7
E5	D_{OUT}
E6	CLR
F3	SW6

Pin Description (48-Lead FG)

Pin	Function	Pin	Function
1	SW5	25	V_{NN}
2	N/C	26	N/C
3	SW4	27	N/C
4	N/C	28	GND
5	SW4	29	V_{DD}
6	N/C	30	N/C
7	N/C	31	N/C
8	SW3	32	N/C
9	N/C	33	D_{IN}
10	SW3	34	CLK
11	N/C	35	$\overline{LE}$
12	SW2	36	CLR
13	N/C	37	D_{OUT}
14	SW2	38	N/C
15	N/C	39	SW7
16	SW1	40	N/C
17	N/C	41	SW7
18	SW1	42	N/C
19	N/C	43	SW6
20	SW0	44	N/C
21	N/C	45	SW6
22	SW0	46	N/C
23	N/C	47	SW5
24	V_{PP}	48	N/C

Pin Description (HV20220PJ)

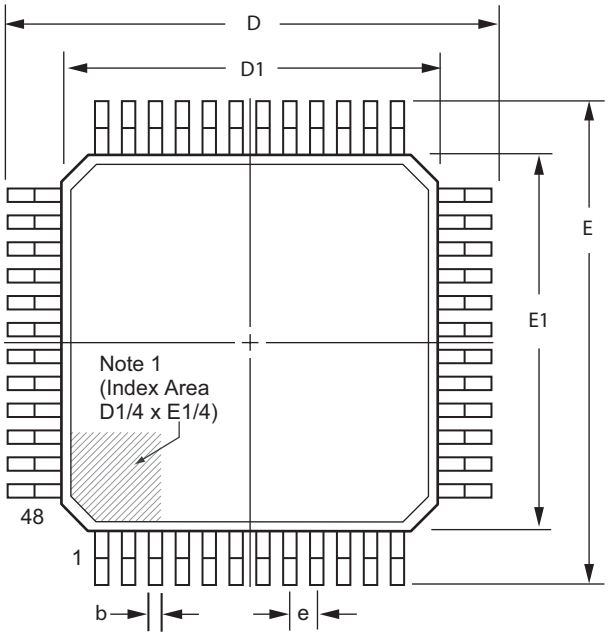
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	V_{PP}	24	SW6
11	N/C	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

Pin Description (HV20320PJ)

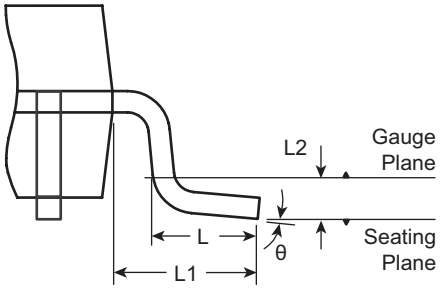
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

48-Lead LQFP Package Outline (FG)

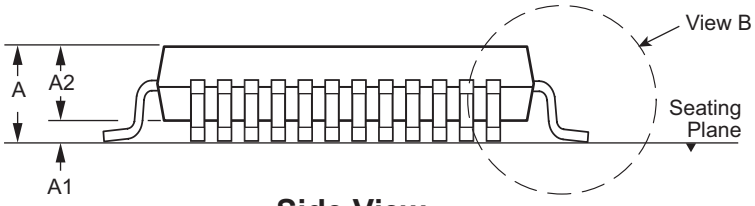
7x7mm body, 1.4mm height (min), 0.50mm pitch



Top View



View B



Side View

Note 1:

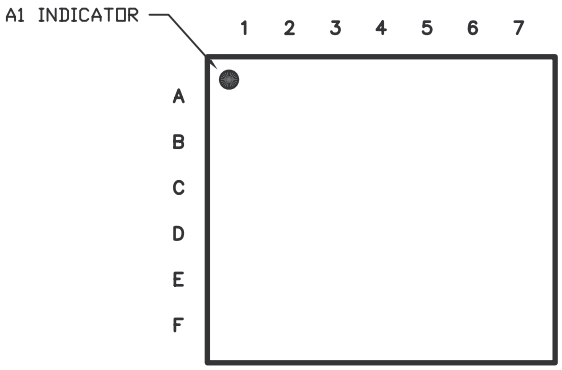
A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40	0.05	1.35	0.17	8.80	6.80	8.80	6.80	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20	7.20	9.20	7.20		0.75			7°

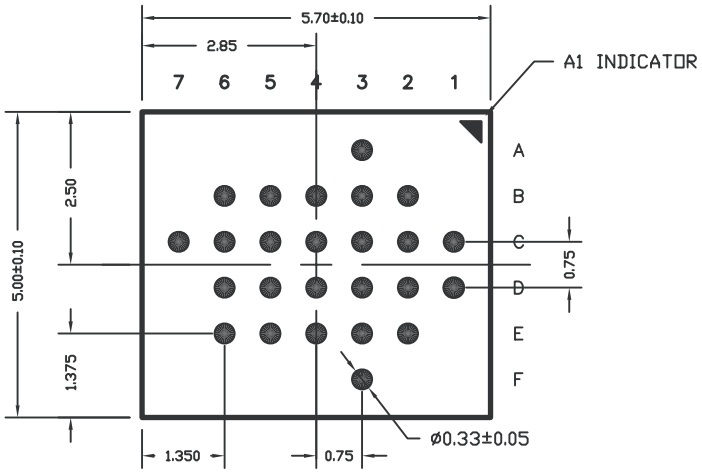
JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

Drawings not to scale.

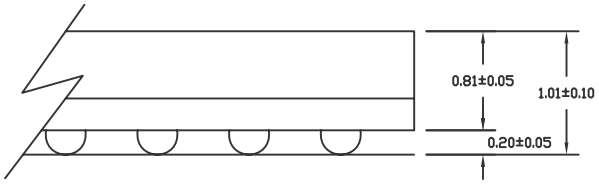
HV220GA 25-Ball fpBGA (GA)



Top View



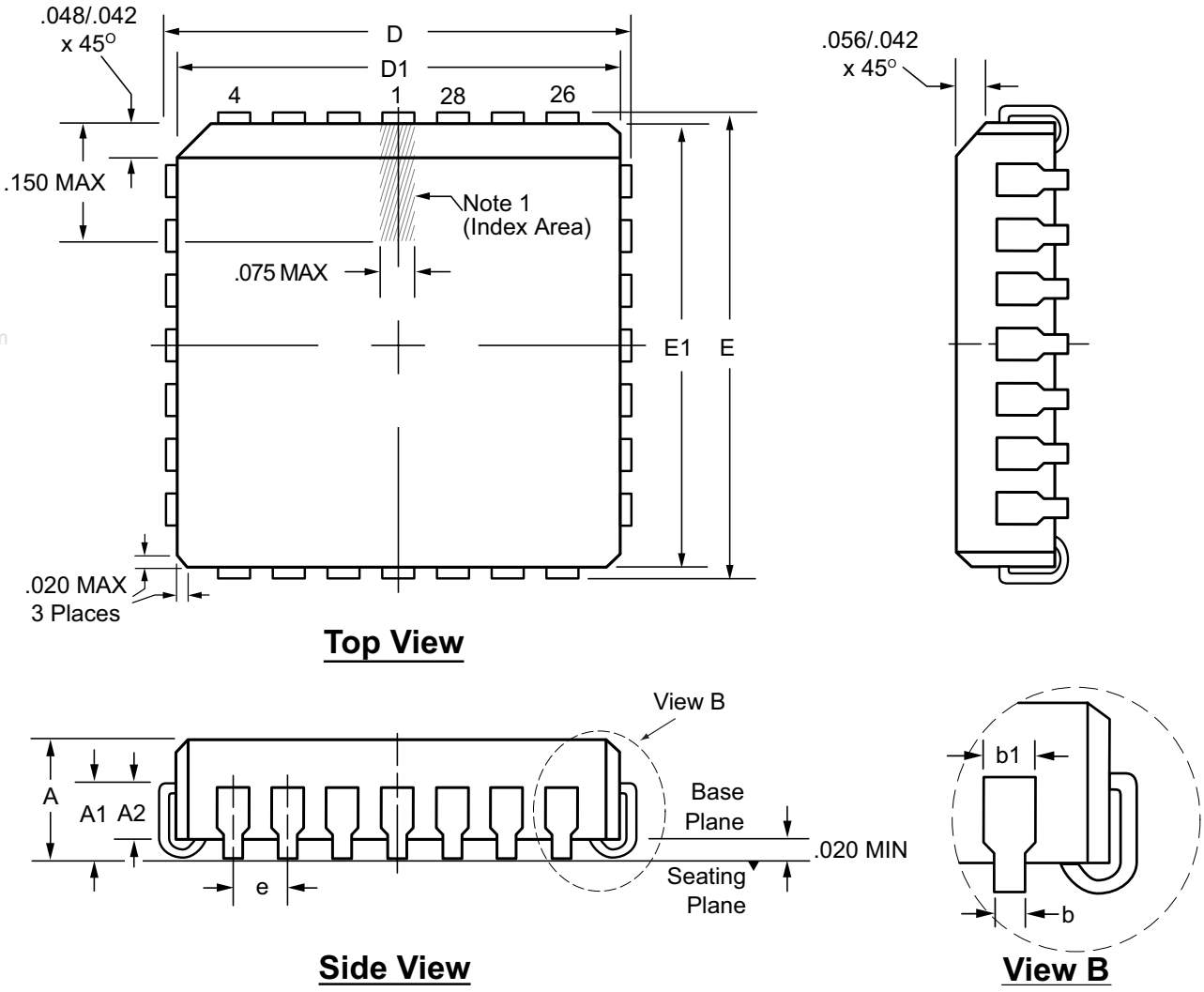
Bottom View



Enlarged Side View

Note:
All dimensions are in millimeters

28-Lead PLCC Package Outline (PJ)



Note 1:
A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com