

Low Charge Injection, 24-Channel, High Voltage Analog Switch with Bleed Resistors

Features

- ▶ 24 Channels of high voltage analog switch
- ▶ Integrated bleed resistors on the outputs
- ▶ 3.3 or 5.0V CMOS input logic level
- ▶ 3:1 MUX-deMUX with 8 states
- ▶ 20MHz data shift clock frequency
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation, 10µA
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

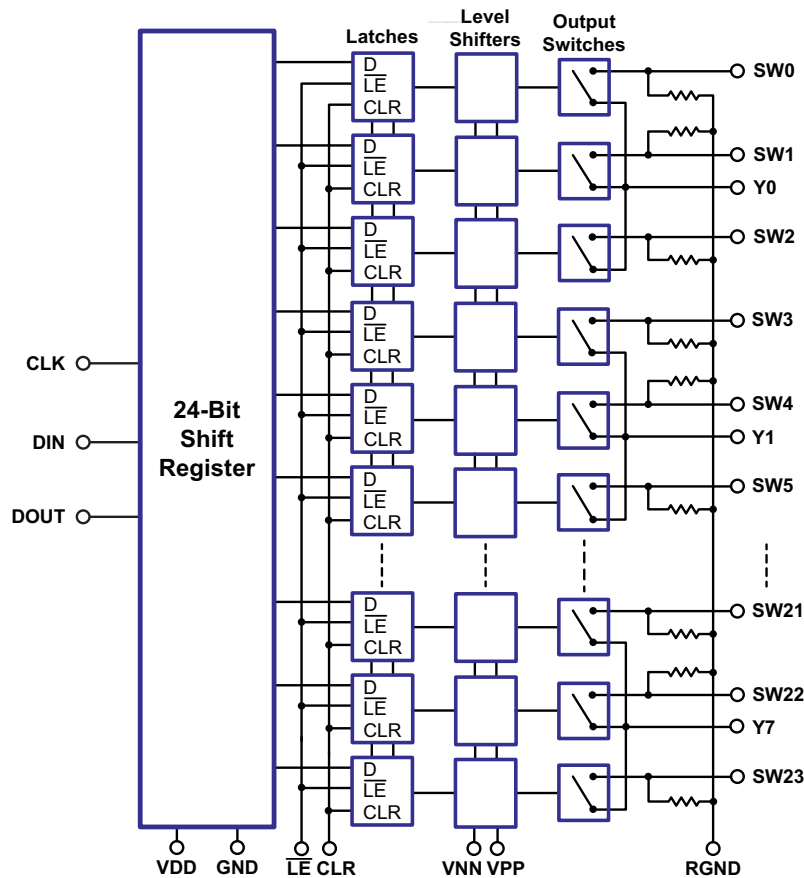
General Description

The Supertex HV2761 is a low charge injection, 24-channel, high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data is shifted into a 24-bit shift register that can then be retained in a 24-bit latch. To reduce any possible clock feed through noise, the latch enable (LE) should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram



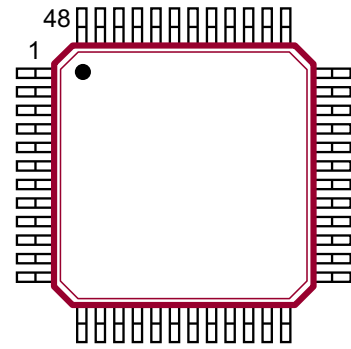
Ordering Information

| Part Number | Package | Packing |
|-----------------|--------------|-----------|
| HV2761FG-G | 48-Lead LQFP | 250/Tray |
| HV2761FG-G M931 | 48-Lead LQFP | 1000/Reel |

-G indicates package is RoHS compliant ("Green")



Pin Configuration



48-Lead LQFP
(top view)

Absolute Maximum Ratings

| Parameter | Value |
|---|------------------------------------|
| V _{DD} logic supply | -0.5V to +6.5V |
| V _{PP} - V _{NN} differential supply | 220V |
| V _{PP} positive supply | -0.5V to V _{NN} + 200V |
| V _{NN} negative supply | +0.5V to - 200V |
| Logic input voltage | -0.5V to V _{DD} + 0.3V |
| Analog signal range | V _{NN} to V _{PP} |
| Peak analog signal current/channel | 3.0A |
| Storage temperature | -65°C to 150°C |
| Power dissipation | 1.0W |

Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed

L = Lot Number

C = Country of Origin*

A = Assembler ID*

— = "Green" Packaging

*May be part of top marking

Bottom Marking



Package may or may not include the following marks: Si or

48-Lead LQFP

Typical Thermal Resistance

| Package | θ_{ja} |
|--------------|---------------|
| 48-Lead LQFP | 52°C/W |

Recommended Operating Conditions

| Sym | Parameter | Value |
|------------------|------------------------------------|---|
| V _{DD} | Logic power supply voltage | 3.0V to 5.5V |
| V _{PP} | Positive high voltage supply | +40V to V _{NN} + 200V |
| V _{NN} | Negative high voltage supply | -40V to - 160V |
| V _{IH} | High level input voltage | 0.9V _{DD} to V _{DD} |
| V _{IL} | Low level input voltage | 0V to 0.1V _{DD} |
| V _{SIG} | Analog signal voltage peak-to-peak | V _{NN} +10V to V _{PP} - 10V |
| T _A | Operating free air temperature | 0°C to 70°C |

Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be V_{NN} ≤ V_{SIG} ≤ V_{PP} or floating during power up/down transition.
3. Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions | |
|-------------------|--|------|-----|-------|------|-----|-------|-----|------|---|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | | |
| R _{ONS} | Small signal switch ON-resistance | - | - | - | 26 | - | - | - | Ω | I _{SIG} = 5.0mA | V _{PP} = +40V, V _{NN} = -160V |
| | | - | - | - | 22 | - | - | - | | I _{SIG} = 200mA | |
| | | - | - | - | 22 | - | - | - | | I _{SIG} = 5.0mA | V _{PP} = +100V, V _{NN} = -100V |
| | | - | - | - | 18 | - | - | - | | I _{SIG} = 200mA | |
| | | - | - | - | 20 | - | - | - | | I _{SIG} = 5.0mA | V _{PP} = +160V, V _{NN} = -40V |
| | | - | - | - | 16 | - | - | - | | I _{SIG} = 200mA | |
| ΔR _{ONS} | Small signal switch ON-resistance matching | - | 20 | - | 5.0 | 20 | - | 20 | % | I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V | |
| R _{ONL} | Large signal switch ON-resistance | - | - | - | 30 | - | - | - | Ω | V _{SIG} = V _{PP} - 10V, I _{SIG} = 1.0A | |
| R _{INT} | Output switch shunt resistance | - | - | 20 | 35 | 50 | - | - | KΩ | Output switch to R _{GND} I _{RINT} = 0.5mA | |
| I _{SOL} | Switch OFF-leakage per switch | - | 5.0 | - | 1.0 | 10 | - | 15 | μA | V _{SIG} = V _{PP} - 10V, V _{NN} +10V | |
| V _{OS} | DC offset switch OFF | - | 300 | - | 100 | 300 | - | 300 | mV | No load | |
| | DC offset switch ON | - | 500 | - | 100 | 500 | - | 500 | | | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches OFF | |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | | | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches ON, I _{SW} = 5.0mA | |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | | | |
| I _{SW} | Switch output peak current | - | - | - | 2.0 | 1.3 | - | - | A | V _{SIG} duty cycle < 0.1% | |
| f _{SW} | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% | |
| I _{PP} | Average V _{PP} supply current | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | V _{PP} = +40V, V _{NN} = -160V | All output switches are turning ON and OFF at 50kHz with no load |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +100V, V _{NN} = -100V | |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +160V, V _{NN} = -40V | |
| I _{NN} | Average V _{NN} supply current | - | 4.0 | - | - | 4.5 | - | 5.0 | mA | V _{PP} = +40V, V _{NN} = -160V | All output switches are turning ON and OFF at 50kHz with no load |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +100V, V _{NN} = -100V | |
| | | - | 4.0 | - | - | 4.5 | - | 5.0 | | V _{PP} = +160V, V _{NN} = -40V | |
| I _{DD} | Average V _{DD} supply current | - | 8.0 | - | - | 8.0 | - | 8.0 | mA | f _{CLK} = 5.0MHz, V _{DD} = 5.0V | |
| I _{DDQ} | Quiescent V _{DD} supply current | - | 10 | - | - | 10 | - | 10 | μA | All logic inputs are static | |
| I _{SOR} | Data out source current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | | mA | V _{OUT} = V _{DD} - 0.7V | |
| I _{SINK} | Data out sink current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | | mA | V _{OUT} = 0.7V | |
| C _{IN} | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- | |

* See Test Circuits on page 5

AC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

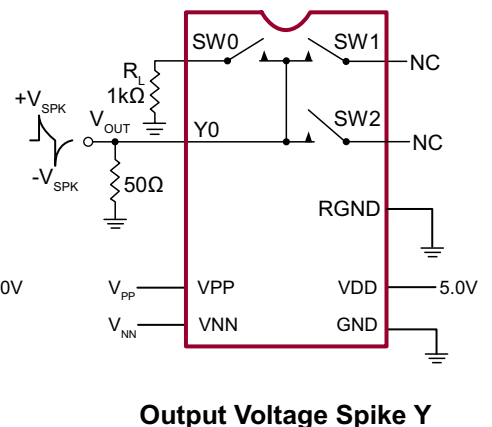
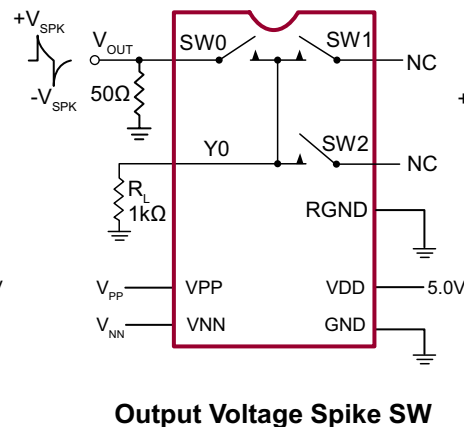
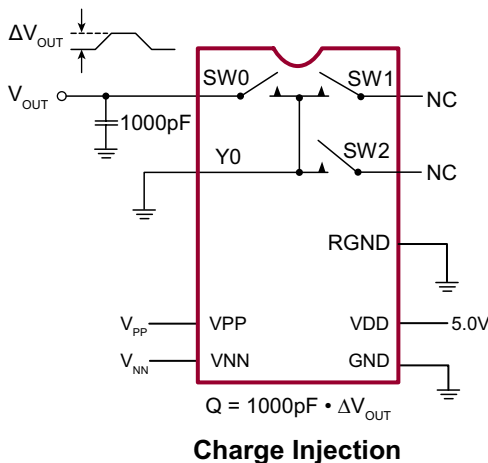
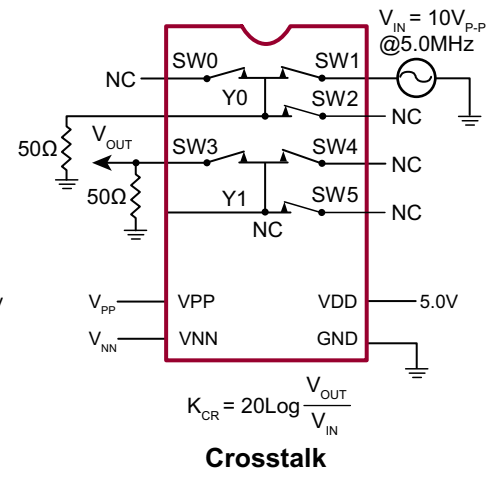
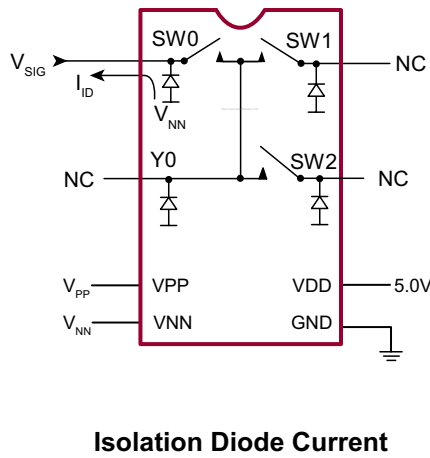
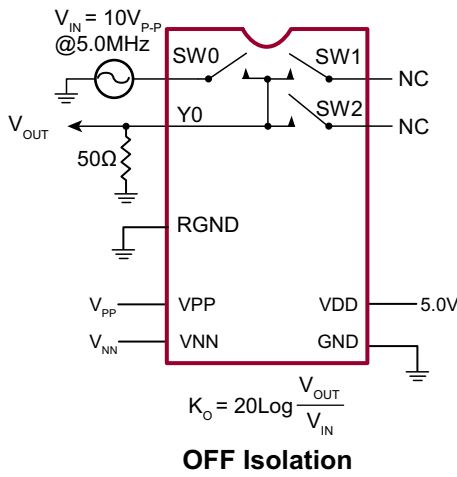
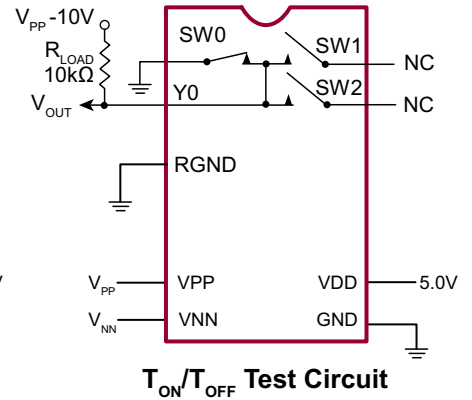
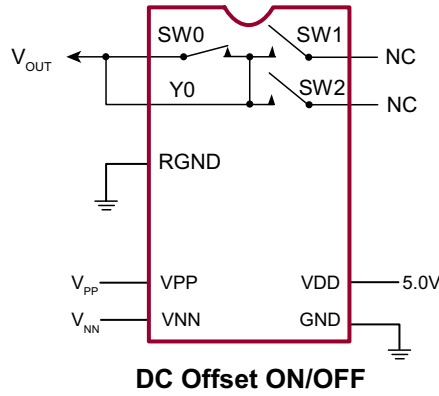
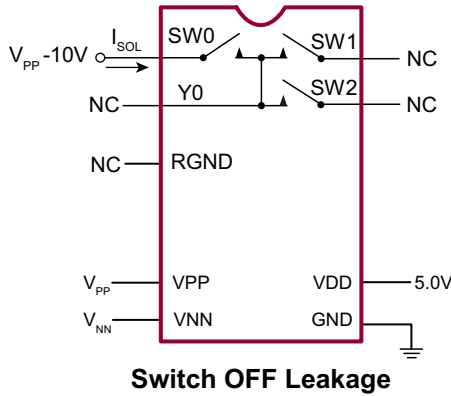
| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions |
|---------------|--|-----|-----|-------|-----|-----|-------|-----|---------|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t_{SD} | Set up time before \overline{LE} rises | 25 | - | 25 | - | - | 25 | - | ns | --- |
| t_{WLE} | Time width of \overline{LE} | 56 | - | - | 56 | - | 56 | - | ns | $V_{DD} = 3.0V$ |
| | | 12 | - | - | 12 | - | 12 | - | | $V_{DD} = 5.0V$ |
| t_{DO} | Clock delay time to data out | 25 | 100 | 25 | 78 | 100 | 25 | 100 | ns | $V_{DD} = 3.0V$ |
| | | 15 | 40 | 15 | 30 | 40 | 15 | 40 | | $V_{DD} = 5.0V$ |
| t_{WCLR} | Time width of CLR | 55 | - | 55 | - | - | 55 | - | ns | --- |
| t_{SU} | Set up time data to clock | 21 | - | 21 | - | - | 21 | - | ns | $V_{DD} = 3.0V$ |
| | | 7.0 | - | 7.0 | - | - | 7.0 | - | | $V_{DD} = 5.0V$ |
| t_H | Hold time data from clock | 5.0 | - | 5.0 | - | - | 5.0 | - | ns | $V_{DD} = 3.0V$ |
| | | 7.0 | - | 7.0 | - | - | 7.0 | - | | $V_{DD} = 5.0V$ |
| f_{CLK} | Clock frequency | - | 8 | - | - | 8 | - | 8 | MHz | $V_{DD} = 3.0V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{DD} = 5.0V$ |
| t_R, t_F | Clock rise and fall times | - | 50 | - | - | 50 | - | 50 | ns | --- |
| t_{ON} | Turn ON time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V,$ $R_{LOAD} = 10k\Omega$ |
| t_{OFF} | Turn OFF time | - | 5.0 | - | - | 5.0 | - | 5.0 | | |
| dv/dt | Maximum V_{SIG} slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +160V, V_{NN} = -40V$ |
| K_O | OFF isolation | -30 | - | -30 | -33 | - | -30 | - | dB | f = 5.0MHz, 1.0k Ω /15pF load |
| | | -58 | - | -58 | -60 | - | -58 | - | | f = 5.0MHz, 50 Ω load |
| K_{CR} | Switch crosstalk | -60 | - | -60 | -70 | - | -60 | - | dB | f = 5.0MHz, 50 Ω load |
| I_{ID} | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300ns pulse width, 2.0% duty cycle |
| $C_{SG(OFF)}$ | OFF capacitance SW to GND | - | 14 | - | 9.0 | 14 | - | 14 | pF | $V_{SIG} = 0V, f = 1.0MHz$ all SW OFF |
| | OFF capacitance Y to GND | - | 35 | - | 27 | 35 | - | 35 | | |
| $C_{SG(ON)}$ | ON capacitance SW to GND | - | 39 | - | 30 | 39 | - | 39 | pF | $V_{SIG} = 0V, f = 1.0MHz$ one SW ON, two SW OFF |
| | ON capacitance Y to GND | - | 39 | - | 30 | 39 | - | 39 | | |
| $+V_{SPK}$ | Output voltage spike (per switch) | - | - | - | - | 150 | - | - | mV | $V_{PP} = +40V, V_{NN} = -160V$ $R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ $R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ $R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |

* See Test Circuits on page 5

AC Electrical Characteristics (cont.) (Over recommended operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions |
|-----|-------------------------------|-----|-----|-------|-----|-----|-------|-----|------|----------------------------------|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| QC | Charge injection (per switch) | - | - | - | 820 | - | - | - | pC | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | - | - | 600 | - | - | - | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | - | - | 350 | - | - | - | | $V_{PP} = +160V, V_{NN} = -40V$ |

Test Circuits



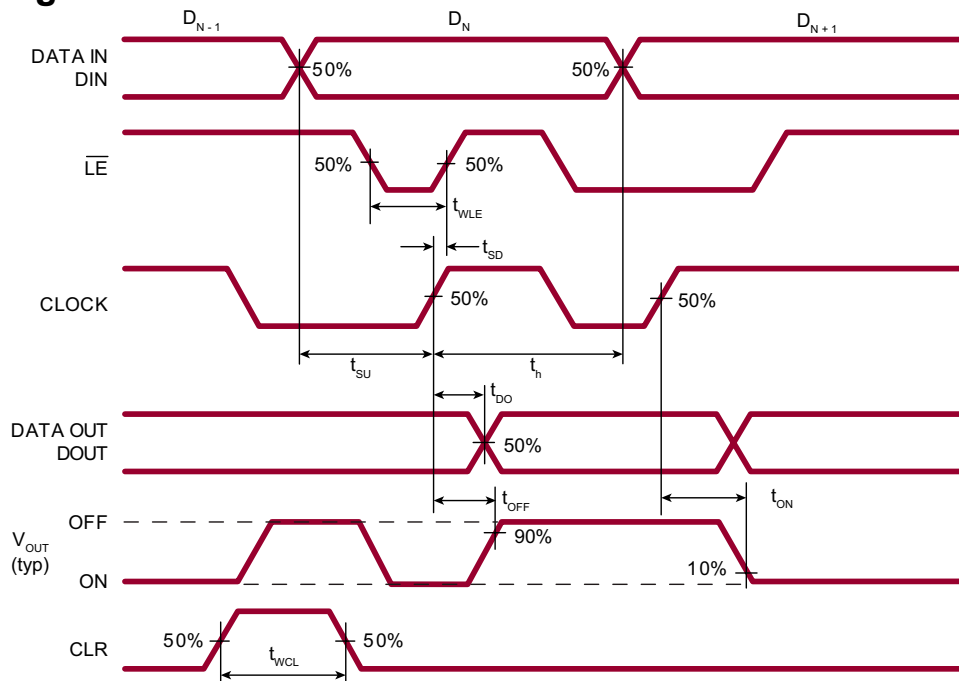
Truth Table

| D0 | D1 | ... | D15 | D16 | ... | D23 | \overline{LE} | CLR | SW0 | SW1 | ... | SW15 | SW16 | ... | SW23 |
|----|----|-----|-----|-----|-----|-----|-----------------|-----|---------------------|-----|-----|------|------|-----|------|
| L | - | | - | - | | - | L | L | OFF | - | | - | - | | - |
| H | - | | - | - | | - | L | L | ON | - | | - | - | | - |
| - | L | | - | - | | - | L | L | - | OFF | | - | - | | - |
| - | H | | - | - | | - | L | L | - | ON | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | L | - | | - | L | L | - | - | | OFF | - | | - |
| - | - | | H | - | | - | L | L | - | - | | ON | - | | - |
| - | - | ... | - | L | ... | - | L | L | - | - | | - | OFF | ... | - |
| - | - | | - | H | | - | L | L | - | - | | - | ON | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | - | L | L | - | - | | - | - | | - |
| - | - | | - | - | | L | L | L | - | - | | - | - | | OFF |
| - | - | | - | - | | H | L | L | - | - | | - | - | | ON |
| X | X | X | X | X | X | X | H | L | HOLD PREVIOUS STATE | | | | | | |
| X | X | X | X | X | X | X | X | H | ALL SWITCHES OFF | | | | | | |

Notes:

1. The 24 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 24 switches go to a state retaining their latched condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift registers data flow through the latch.
4. DOUT is high when data in the register 23 is high.
5. Shift registers clocking has no effect on the switch states if \overline{LE} is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms



Pin Function

| Pin | Function |
|-----|-----------------|
| 1 | VPP |
| 2 | NC |
| 3 | GND |
| 4 | CLR |
| 5 | \overline{LE} |
| 6 | CLK |
| 7 | VDD |
| 8 | GND |
| 9 | DIN |
| 10 | DOUT |
| 11 | NC |
| 12 | VNN |

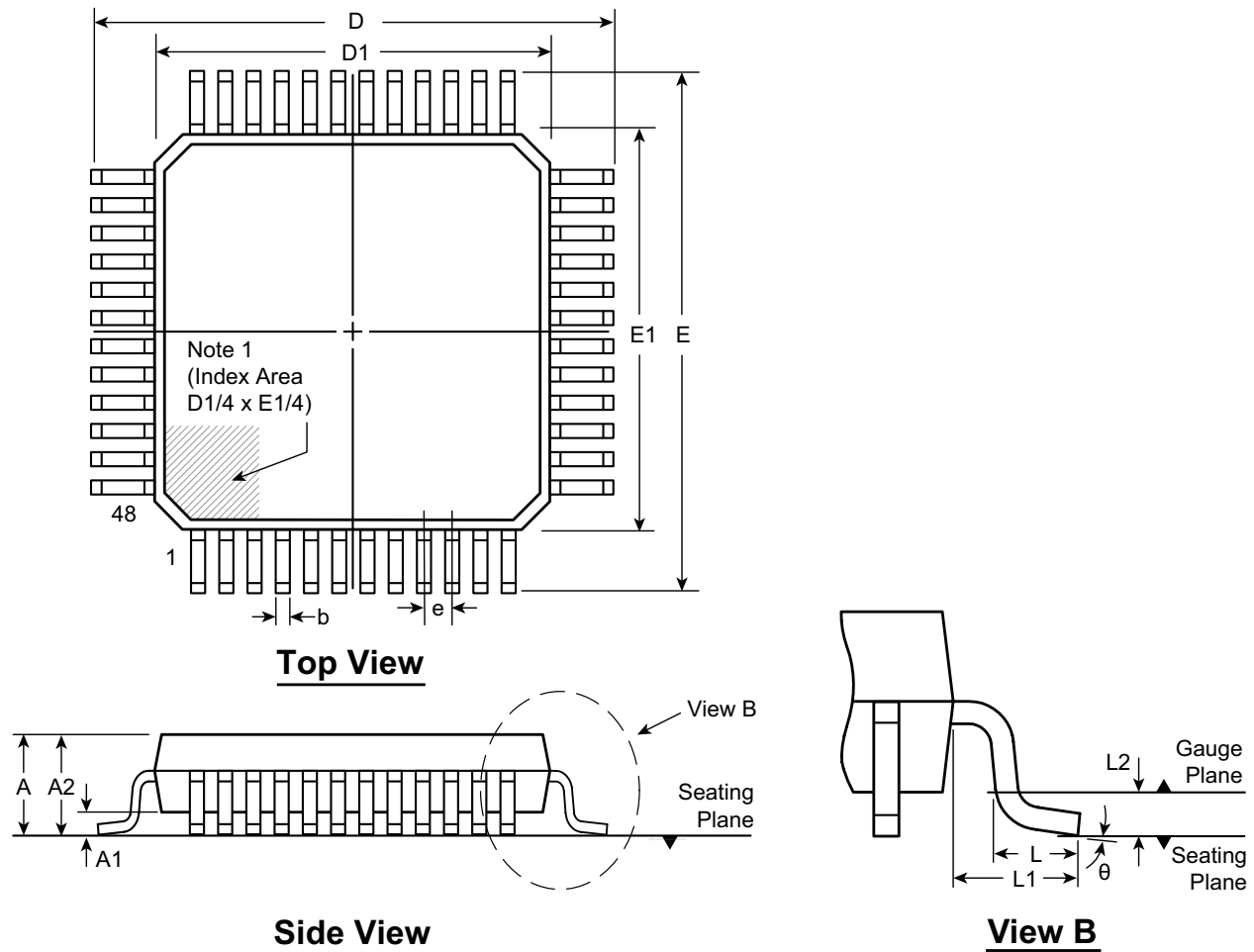
| Pin | Function |
|-----|----------|
| 13 | SW0 |
| 14 | Y0 |
| 15 | SW1 |
| 16 | SW2 |
| 17 | SW3 |
| 18 | Y1 |
| 19 | SW4 |
| 20 | SW5 |
| 21 | SW6 |
| 22 | Y2 |
| 23 | SW7 |
| 24 | SW8 |

| Pin | Function |
|-----|----------|
| 25 | VPP |
| 26 | RGND |
| 27 | SW9 |
| 28 | Y3 |
| 29 | SW10 |
| 30 | SW11 |
| 31 | SW12 |
| 32 | SW13 |
| 33 | Y4 |
| 34 | SW14 |
| 35 | RGND |
| 36 | VNN |

| Pin | Function |
|-----|----------|
| 37 | SW15 |
| 38 | SW16 |
| 39 | Y5 |
| 40 | SW17 |
| 41 | SW18 |
| 42 | SW19 |
| 43 | Y6 |
| 44 | SW20 |
| 45 | SW21 |
| 46 | SW22 |
| 47 | Y7 |
| 48 | SW23 |

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|----------|------|----------|----------|----|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 0.45 | 1.00 REF | 0.25 BSC | 0° |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | 0.60 | | 3.5° | |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | 0.75 | | 7° | |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
 * This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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