

## Low Harmonic Distortion, 32-Channel SPST, High-Voltage Analog Switch

### Features

- 32-Channel SPST (Single-Pole, Single-Throw) High-Voltage Analog Switch
- 3.3V or 5.0V CMOS Input Logic Level
- 20 MHz Data Shift Clock Frequency
- High-Voltage CMOS (HVC MOS) Technology for High Performance
- Very Low Quiescent Power Dissipation (10  $\mu$ A)
- Low Parasitic Capacitance
- DC to 50 MHz Analog Signal Frequency
- -60 dB Typical OFF-Isolation at 5.0 MHz
- CMOS Logic Circuitry for Low Power
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltages
- Integrated Bleed Resistors on the Outputs (HV2902 only)

### Applications

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Heads
- Optical MEMS Modules

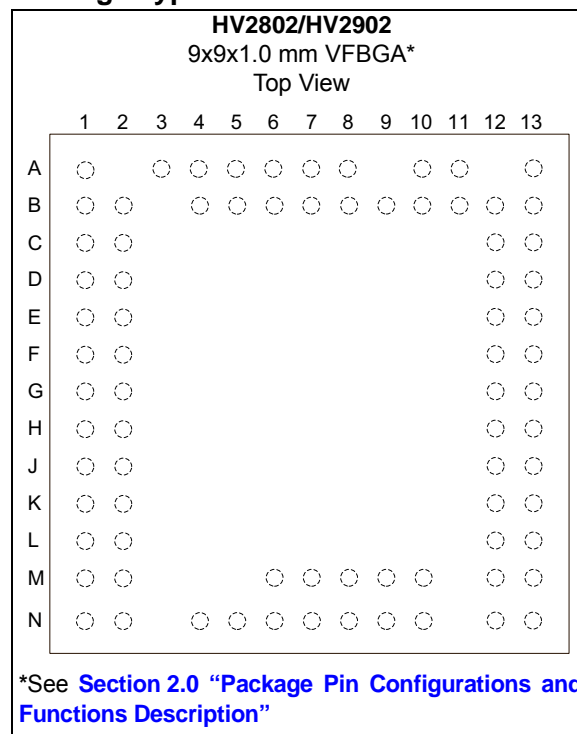
### General Description

The HV2802 and HV2902 are low-charge injection, 32-channel, high-voltage analog switches intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers. The HV2902 has integrated bleed resistors which eliminate voltage build-up on capacitive loads such as piezoelectric transducers.

Input data are shifted into a 32-bit shift register that can then be retained in a 32-bit latch. To reduce any possible clock feedthrough noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using the HVC MOS technology, this device combines high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

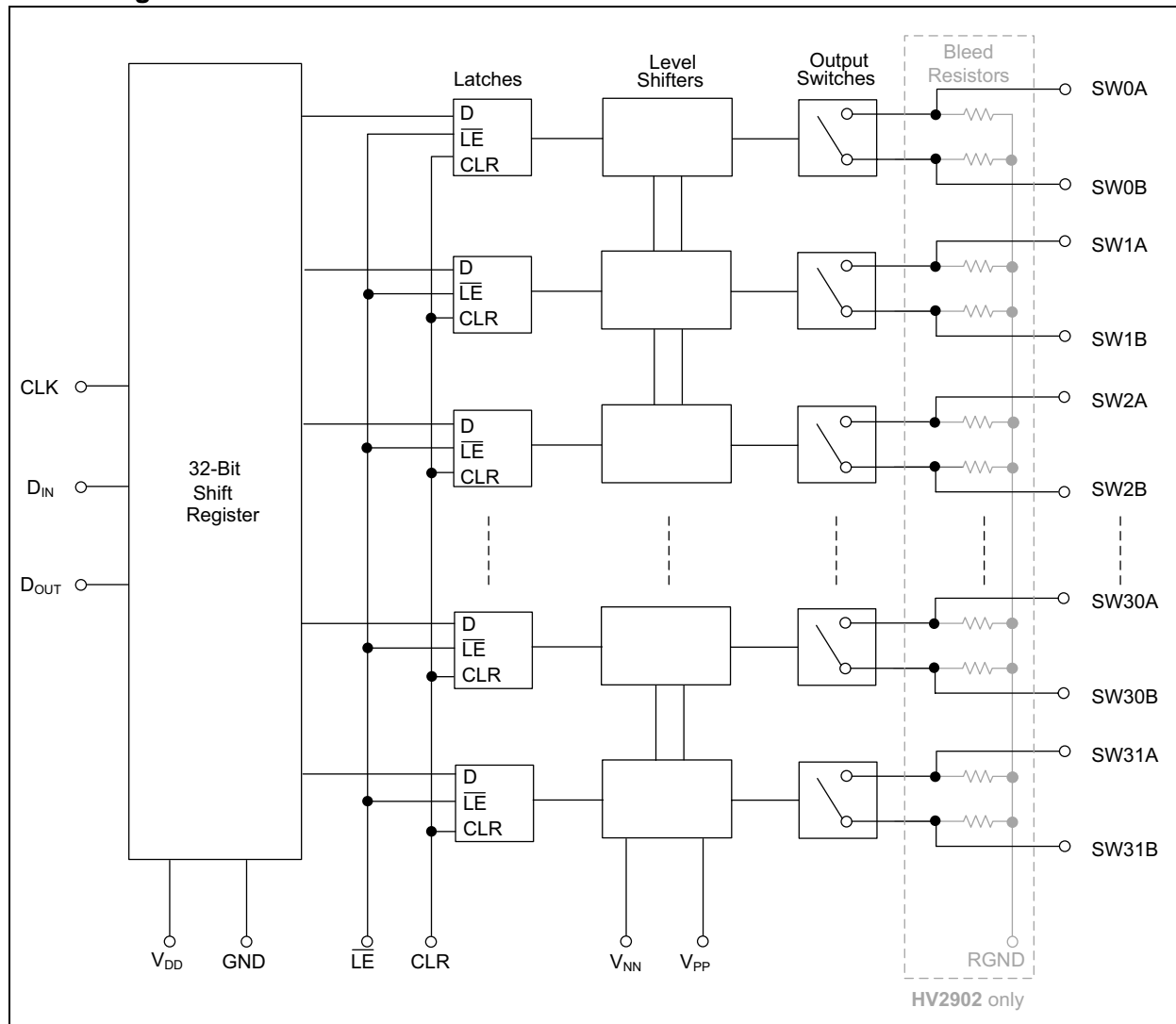
The device is suitable for various combinations of high-voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V and +160V/-40V.

### Package Type



# HV2802/HV2902

## Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

|   |                         |
|---|-------------------------|
| $V_{DD}$ Logic Supply Voltage .....           | -0.5V to +6.5V          |
| $V_{PP}$ - $V_{NN}$ Differential Supply ..... | 220V                    |
| $V_{PP}$ Positive Supply .....                | -0.5V to $V_{NN}$ +200V |
| $V_{NN}$ Negative Supply .....                | +0.5V to -200V          |
| Logic Input Voltage.....                      | -0.5V to $V_{DD}$ +0.3V |
| Analog Signal Range .....                     | $V_{NN}$ to $V_{PP}$    |
| Peak Analog Signal Current/Channel .....      | 3.0A                    |
| Power Dissipation .....                       | 1.5W                    |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Note 1 — 3)

| Parameter                          | Symbol    | Value                          |
|------------------------------------|-----------|--------------------------------|
| Logic Power Supply Voltage         | $V_{DD}$  | +3.0V to +5.5V                 |
| Positive Voltage Supply            | $V_{PP}$  | +40V to $V_{NN}$ +200V         |
| Negative Voltage Supply            | $V_{NN}$  | -40V to -160V                  |
| High-Level Input Voltage           | $V_{IH}$  | $0.9V_{DD}$ to $V_{DD}$        |
| Low-Level Input Voltage            | $V_{IL}$  | 0V to $0.1V_{DD}$              |
| Analog Signal Voltage Peak-to-Peak | $V_{SIG}$ | $V_{NN}$ +10V to $V_{PP}$ -10V |

- Note 1:** Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- 2:**  $V_{SIG}$  must be  $V_{NN} \leq V_{SIG} \leq V_{PP}$  or floating during power up/down transition.
- 3:** Rise and fall times of power supplies  $V_{DD}$ ,  $V_{PP}$ , and  $V_{NN}$  should not be less than 1.0 ms.

# HV2802/HV2902

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified,  $V_{DD} = 5.0V$ ,  $V_{PP} = +100V$ ,  $V_{NN} = -100V$ , Specification at 0°C and 70°C based on characterization and not 100% tested.

| Parameters                                    | Symbol           | 0°C  |      | +25°C |      |      | +70°C |      | Units      | Conditions   |
|---|------------------|------|------|-------|------|------|-------|------|------------|--|
|   |                  | Min. | Max. | Min.  | Typ. | Max. | Min.  | Max. |            |  |
| Small Signal Switch ON-Resistance             | $R_{ONS}$        | —    | 30   | —     | 26   | 38   | —     | 48   | $\Omega$   | $I_{SIG} = 5.0 \text{ mA}$ ,<br>$V_{PP} = +40V$ , $V_{NN} = -160V$               |
|   |                  | —    | 25   | —     | 22   | 27   | —     | 32   |            | $I_{SIG} = 200 \text{ mA}$ ,<br>$V_{PP} = +40V$ , $V_{NN} = -160V$               |
|   |                  | —    | 25   | —     | 22   | 27   | —     | 30   |            | $I_{SIG} = 5.0 \text{ mA}$ ,<br>$V_{PP} = +100V$ , $V_{NN} = -100V$              |
|   |                  | —    | 18   | —     | 18   | 24   | —     | 27   |            | $I_{SIG} = 200 \text{ mA}$ ,<br>$V_{PP} = +100V$ , $V_{NN} = -100V$              |
|   |                  | —    | 23   | —     | 20   | 25   | —     | 30   |            | $I_{SIG} = 5.0 \text{ mA}$ ,<br>$V_{PP} = +160V$ , $V_{NN} = -40V$               |
|   |                  | —    | 22   | —     | 16   | 25   | —     | 27   |            | $I_{SIG} = 200 \text{ mA}$ ,<br>$V_{PP} = +160V$ , $V_{NN} = -40V$               |
| Small Signal Switch ON-Resistance Matching    | $\Delta R_{ONS}$ | —    | 20   | —     | 5    | 20   | —     | 20   | %          | $I_{SIG} = 5.0 \text{ mA}$ ,<br>$V_{PP} = +100V$ , $V_{NN} = -100V$              |
| Large Signal Switch ON-Resistance<br>(Note 1) | $R_{ONL}$        | —    | —    | —     | 15   | —    | —     | —    | $\Omega$   | $V_{SIG} = V_{PP} - 10V$ , $I_{SIG} = 1A$  |
| Value of Output Bleed Resistor                | $R_{INT}$        | —    | —    | 20    | 35   | 50   | —     | —    | k $\Omega$ | Output switch to RGND<br>$I_{RINT} = 0.5 \text{ mA}$                             |
| Switch off Leakage per Switch                 | $I_{SOL}$        | —    | 5    | —     | 1    | 10   | —     | 15   | $\mu A$    | $V_{SIG} = V_{PP} - 10V$ , $V_{NN} + 10V$  |
| Switch DC Offset                              | $V_{OS}$         | —    | 300  | —     | 100  | 300  | —     | 300  | mV         | Switch OFF,<br>$R_{LOAD} = 100 \text{ k}\Omega$ for HV2802<br>No load for HV2902 |
|   |                  | —    | 500  | —     | 100  | 500  | —     | 500  |            | Switch ON<br>$R_{LOAD} = 100 \text{ k}\Omega$ for HV2802<br>No load for HV2902   |
| Quiescent $V_{PP}$ Supply Current             | $I_{PPQ}$        | —    | —    | —     | 10   | 50   | —     | —    | $\mu A$    | All switches off   |
| Quiescent $V_{NN}$ Supply Current             | $I_{NNQ}$        | —    | —    | —     | 10   | 50   | —     | —    |            |  |
| Quiescent $V_{PP}$ Supply Current             | $I_{PPQ}$        | —    | —    | —     | 10   | 50   | —     | —    | $\mu A$    | All switches on,<br>$I_{SW} = 5.0 \text{ mA}$                                    |
| Quiescent $V_{NN}$ Supply Current             | $I_{NNQ}$        | —    | —    | —     | 10   | 50   | —     | —    |            |  |
| Switch Output Peak Current (Note 1)           | $I_{SW}$         | —    | —    | 2     | 3    | —    | —     | —    | A          | $V_{SIG}$ duty cycle < 0.1%  |
| Output Switching Frequency (Note 1)           | $f_{SW}$         | —    | —    | —     | —    | 50   | —     | —    | kHz        | Duty cycle = 50%   |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

**2:** Design guidance only.

## DC ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise specified,  $V_{DD} = 5.0V$ ,  $V_{PP} = +100V$ ,  $V_{NN} = -100V$ , Specification at 0°C and 70°C based on characterization and not 100% tested.

| Parameters                        | Symbol     | 0°C  |      | +25°C |      |      | +70°C |      | Units   | Conditions   |
|-----------------------------------|------------|------|------|-------|------|------|-------|------|---------|--|
|                                   |            | Min. | Max. | Min.  | Typ. | Max. | Min.  | Max. |         |  |
| Average $V_{PP}$ Supply Current   | $I_{PP}$   | —    | 14   | —     | —    | 14   | —     | 14   | mA      | $V_{PP} = +40V$ , $V_{NN} = -160V$<br>All output switches are turning on and off at 50 kHz with no load  |
|                                   |            | —    | 14   | —     | —    | 14   | —     | 14   |         | $V_{PP} = +100V$ , $V_{NN} = -100V$<br>All output switches are turning on and off at 50 kHz with no load |
|                                   |            | —    | 14   | —     | —    | 14   | —     | 14   |         | $V_{PP} = +160V$ , $V_{NN} = -40V$<br>All output switches are turning on and off at 50 kHz with no load  |
| Average $V_{NN}$ Supply Current   | $I_{NN}$   | —    | 14   | —     | —    | 14   | —     | 14   | mA      | $V_{PP} = +40V$ , $V_{NN} = -160V$<br>All output switches are turning on and off at 50 kHz with no load  |
|                                   |            | —    | 14   | —     | —    | 14   | —     | 14   |         | $V_{PP} = +100V$ , $V_{NN} = -100V$<br>All output switches are turning on and off at 50 kHz with no load |
|                                   |            | —    | 14   | —     | —    | 14   | —     | 14   |         | $V_{PP} = +160V$ , $V_{NN} = -40V$<br>All output switches are turning on and off at 50 kHz with no load  |
| Average $V_{DD}$ Supply Current   | $I_{DD}$   | —    | 8    | —     | —    | 8    | —     | 8    | mA      | $f_{CLK} = 5.0\text{ MHz}$ , $V_{DD} = 5.0V$   |
| Quiescent $V_{DD}$ Supply Current | $I_{DDQ}$  | —    | 10   | —     | —    | 10   | —     | 10   | $\mu A$ | All logic inputs are static  |
| Data Out Source Current           | $I_{SOR}$  | 0.45 | —    | 0.45  | 0.70 | —    | 0.40  | —    | mA      | $V_{OUT} = V_{DD} - 0.7V$  |
| Data Out Sink Current             | $I_{SINK}$ | 0.45 | —    | 0.45  | 0.70 | —    | 0.40  | —    | mA      | $V_{OUT} = 0.7V$   |
| Logic Input Capacitance (Note 2)  | $C_{IN}$   | —    | 10   | —     | —    | 10   | —     | 10   | pF      |  |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

**Note 2:** Design guidance only.

# HV2802/HV2902

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified,  $V_{DD} = 5.0V$ ,  $V_{PP} = +100V$ ,  $V_{NN} = -100V$ , Specification at  $0^{\circ}C$  and  $70^{\circ}C$  based on characterization and not 100% tested.

| Parameters  | Symbol        | 0°C  |      | +25°C |      |      | +70°C |      | Units   | Conditions  |
|---|---------------|------|------|-------|------|------|-------|------|---------|---|
|   |               | Min. | Max. | Min.  | Typ. | Max. | Min.  | Max. |         |   |
| Set Up Time Before $\overline{LE}$ Rises (Note 1) | $t_{SD}$      | 25   | —    | 25    | —    | —    | 25    | —    | ns      |   |
| Time Width of $\overline{LE}$ (Note 1)            | $t_{WLE}$     | 56   | —    | 56    | —    | —    | 56    | —    | ns      | $V_{DD} = 3.0V$   |
|   |               | 12   | —    | 12    | —    | —    | 12    | —    |         | $V_{DD} = 5.0V$   |
| Clock Delay Time to Data Out (Note 1)             | $t_{DO}$      | 8    | 40   | 8     | 19   | 40   | 8     | 40   | ns      | $V_{DD} = 3.0V$   |
|   |               | 8    | 30   | 8     | 15   | 30   | 8     | 30   |         | $V_{DD} = 5.0V$   |
| Time Width of CLR (Note 1)                        | $t_{WCLR}$    | 55   | —    | 55    | —    | —    | 55    | —    | ns      |   |
| Set Up Time Data to Clock (Note 1)                | $t_{SU}$      | 21   | —    | 21    | —    | —    | 21    | —    | ns      | $V_{DD} = 3.0V$   |
|   |               | 7    | —    | 7     | —    | —    | 7     | —    |         | $V_{DD} = 5.0V$   |
| Hold Time Data from Clock (Note 1)                | $t_H$         | 5    | —    | 5     | —    | —    | 5     | —    | ns      | $V_{DD} = 3.0V$   |
|   |               | 7    | —    | 7     | —    | —    | 7     | —    |         | $V_{DD} = 5.0V$   |
| Clock Frequency                                   | $f_{CLK}$     | —    | 8    | —     | —    | 8    | —     | 8    | MHz     | $V_{DD} = 3.0V$   |
|   |               | —    | 20   | —     | —    | 20   | —     | 20   |         | $V_{DD} = 5.0V$   |
| Clock Rise and Fall Times                         | $t_R, t_F$    | —    | 50   | —     | —    | 50   | —     | 50   | ns      |   |
| Turn ON Time                                      | $t_{ON}$      | —    | 5    | —     | —    | 5    | —     | 5    | $\mu s$ | $V_{SIG} = V_{PP} - 10V$ ,<br>$R_{LOAD} = 10 k\Omega$     |
| Turn OFF Time                                     | $t_{OFF}$     | —    | 5    | —     | —    | 5    | —     | 5    |         |   |
| Maximum $V_{SIG}$ Slew Rate (Note 1)              | $dv/dt$       | —    | —    | —     | —    | 20   | —     | —    | V/ns    | $V_{PP} = +40V, V_{NN} = -160V$                           |
|   |               | —    | —    | —     | —    | 20   | —     | —    |         | $V_{PP} = +100V, V_{NN} = -100V$                          |
|   |               | —    | —    | —     | —    | 20   | —     | —    |         | $V_{PP} = +160V, V_{NN} = -40V$                           |
| OFF Isolation (Note 1)                            | $K_O$         | —    | —    | —     | -33  | -30  | —     | —    | dB      | $f = 5.0 MHz$ ,<br>$1.0 k\Omega \parallel 15 pF$ load     |
|   |               | —    | —    | —     | -60  | -58  | —     | —    |         | $f = 5.0 MHz$ ,<br>$50\Omega$ load                        |
| Switch Crosstalk (Note 1)                         | $K_{CR}$      | —    | —    | —     | -70  | -60  | —     | —    | dB      | $f = 5.0 MHz$ ,<br>$50\Omega$ load                        |
| Output Switch Isolation Diode Current (Note 1)    | $I_{ID}$      | —    | —    | —     | —    | 300  | —     | —    | mA      | 300 ns pulse width,<br>2.0% duty cycle                    |
| Off Capacitance SW to GND (Note 1)                | $C_{SG(OFF)}$ | —    | —    | —     | 10   | 15   | —     | —    | pF      | 0V, $f = 1.0 MHz$   |
| On Capacitance SW to GND (Note 1)                 | $C_{SG(ON)}$  | —    | —    | —     | 13   | 18   | —     | —    |         |   |
| Output Voltage Spike SWA, SWB (Note 1)            | + $V_{SPK}$   | —    | —    | —     | —    | +150 | —     | —    | mV      | $V_{PP} = +40V, V_{NN} = -160V$<br>$R_{LOAD} = 50\Omega$  |
|   | - $V_{SPK}$   | —    | —    | -150  | —    | —    | —     | —    |         |   |
|   | + $V_{SPK}$   | —    | —    | —     | —    | +150 | —     | —    |         | $V_{PP} = +100V, V_{NN} = -100V$<br>$R_{LOAD} = 50\Omega$ |
|   | - $V_{SPK}$   | —    | —    | -150  | —    | —    | —     | —    |         |   |
|   | + $V_{SPK}$   | —    | —    | —     | —    | +150 | —     | —    |         |   |
| - $V_{SPK}$                                       | —             | —    | -150 | —     | —    | —    | —     |      |         |   |
| Charge Injection (per switch) (Note 1)            | QC            | —    | —    | —     | 820  | —    | —     | —    | pC      | $V_{PP} = +40V, V_{NN} = -160V$                           |
|   |               | —    | —    | —     | 600  | —    | —     | —    |         | $V_{PP} = +100V, V_{NN} = -100V$                          |
|   |               | —    | —    | —     | 350  | —    | —     | —    |         | $V_{PP} = +160V, V_{NN} = -40V$                           |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## TEMPERATURE SPECIFICATIONS

| Parameters                        | Sym.          | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------|---------------|------|------|------|-------|------------|
| <b>Temperature Ranges</b>         |               |      |      |      |       |            |
| Operating Temperature             | $T_A$         | 0    | —    | +70  | °C    |            |
| Storage Temperature               | $T_A$         | -65  | —    | +150 | °C    |            |
| <b>Package Thermal Resistance</b> |               |      |      |      |       |            |
| Thermal Resistance, 78-Ball VFBGA | $\theta_{JA}$ | —    | 32.2 | —    | °C/W  |            |

# HV2802/HV2902

## 1.1 Logic Timing and Truth Table

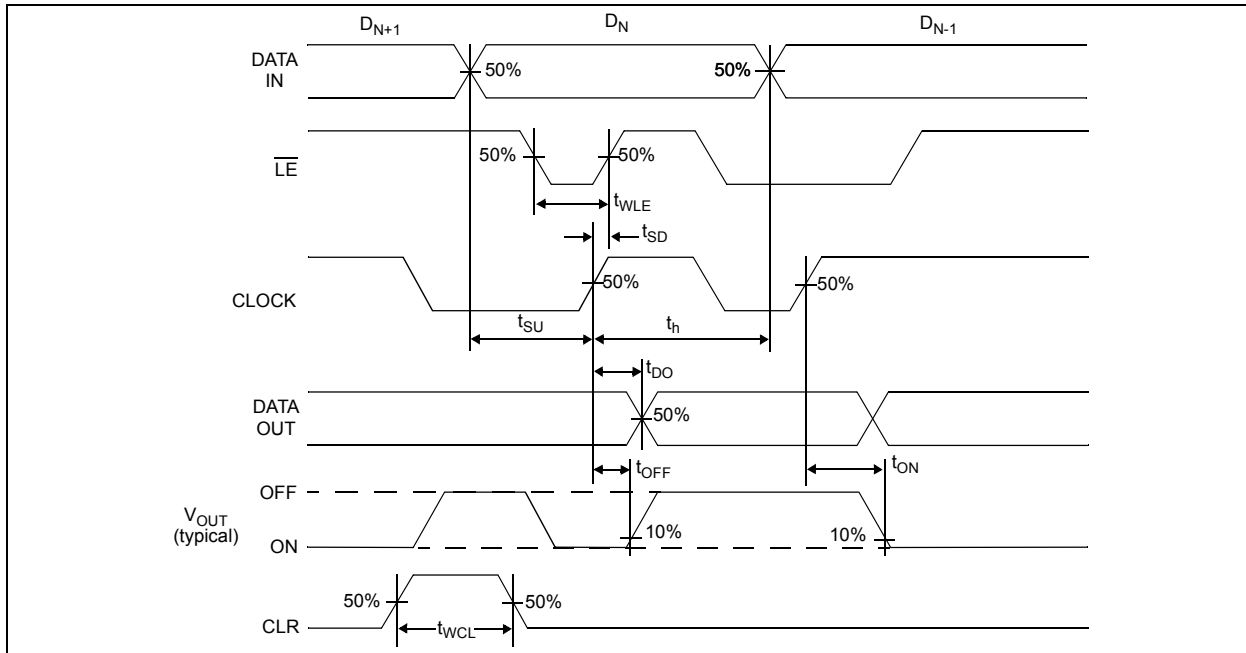


FIGURE 1-1: Logic Timing Waveforms.

TABLE 1-1: TRUTH TABLE (Notes 1 — 6)

| D0 | D1 | ... | D15 | D16 | ... | D31 | $\overline{LE}$ | CLR | SW0                 | SW1 | ... | SW15 | SW16 | ... | SW31 |
|----|----|-----|-----|-----|-----|-----|-----------------|-----|---------------------|-----|-----|------|------|-----|------|
| L  | —  |     | —   | —   |     | —   | L               | L   | OFF                 | —   |     | —    | —    |     | —    |
| H  | —  |     | —   | —   |     | —   | L               | L   | ON                  | —   |     | —    | —    |     | —    |
| —  | L  |     | —   | —   |     | —   | L               | L   | —                   | OFF |     | —    | —    |     | —    |
| —  | H  |     | —   | —   |     | —   | L               | L   | —                   | ON  |     | —    | —    |     | —    |
| —  | —  |     | —   | —   |     | —   | L               | L   | —                   | —   |     | —    | —    |     | —    |
| —  | —  |     | L   | —   |     | —   | L               | L   | —                   | —   |     | OFF  | —    |     | —    |
| —  | —  | ... | H   | —   | ... | —   | L               | L   | —                   | —   | ... | ON   | —    | ... | —    |
| —  | —  |     | —   | L   |     | —   | L               | L   | —                   | —   |     | —    | OFF  |     | —    |
| —  | —  |     | —   | H   |     | —   | L               | L   | —                   | —   |     | —    | ON   |     | —    |
| —  | —  |     | —   | —   |     | —   | L               | L   | —                   | —   |     | —    | —    |     | —    |
| —  | —  |     | —   | —   |     | —   | L               | L   | —                   | —   |     | —    | —    |     | —    |
| —  | —  |     | —   | —   |     | —   | L               | L   | —                   | —   |     | —    | —    |     | —    |
| —  | —  |     | —   | —   |     | L   | L               | L   | —                   | —   |     | —    | —    |     | OFF  |
| —  | —  |     | —   | —   |     | H   | L               | L   | —                   | —   |     | —    | —    |     | ON   |
| X  | X  | X   | X   | X   | X   | X   | H               | L   | HOLD PREVIOUS STATE |     |     |      |      |     |      |
| X  | X  | X   | X   | X   | X   | X   | X               | H   | ALL SWITCHES OFF    |     |     |      |      |     |      |

**Legend:** X = Do not care; L = Low; H = High.

- Note 1:** The 32 switches operate independently.
- 2:** Serial data is clocked in on the L to H transition of the CLK.
- 3:** All 32 switches go to a state retaining their latched condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low, the shift register's data flow through the latch.
- 4:**  $D_{OUT}$  is high when data in register 31 is high.
- 5:** Shift register's clocking has no effect on the switch states if  $\overline{LE}$  is high.
- 6:** The CLR clear input overrides all other inputs.



## 2.0 PACKAGE PIN CONFIGURATIONS AND FUNCTIONS DESCRIPTION

This section details the pin designation for the 78-Ball VFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

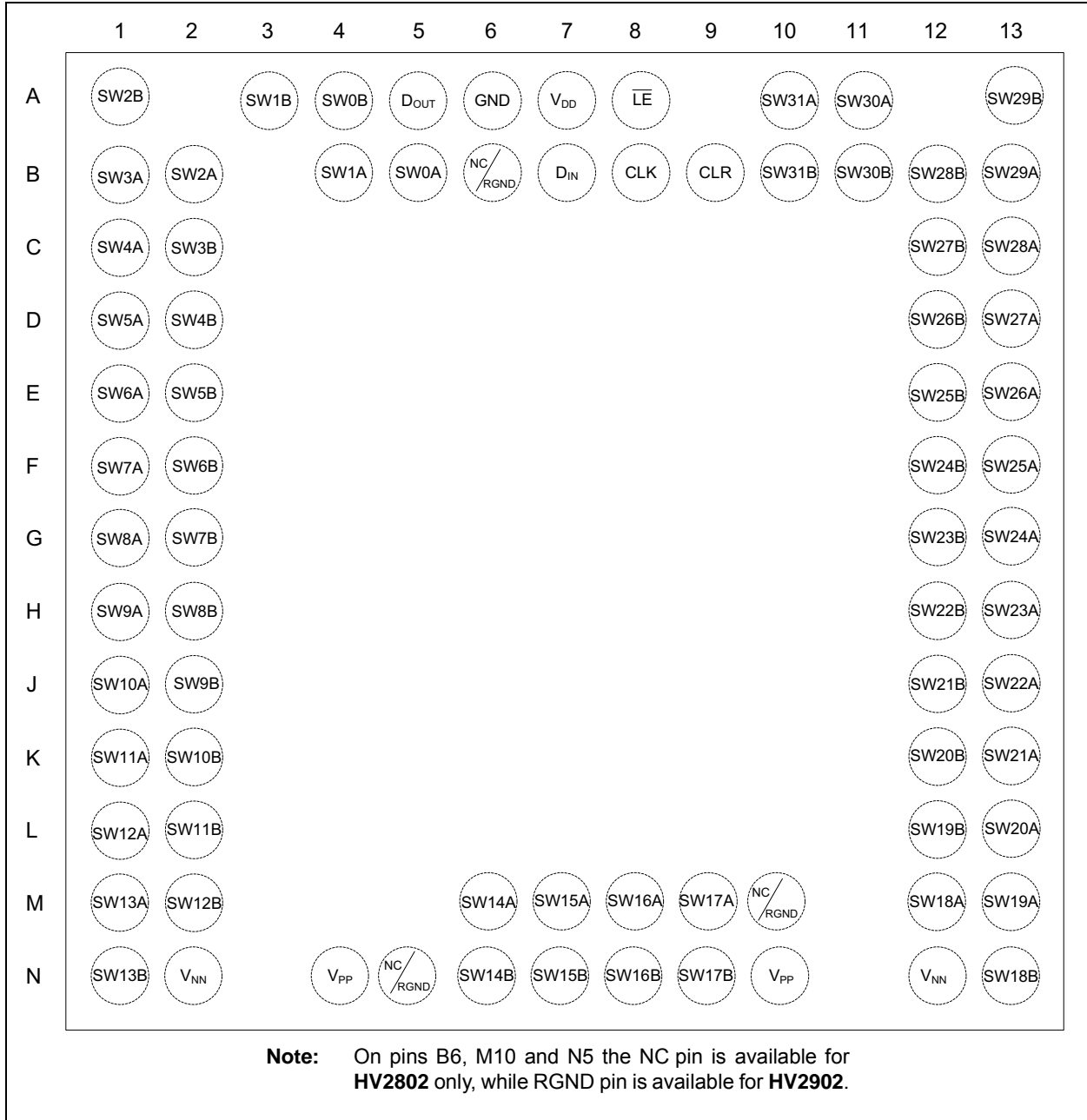


FIGURE 2-1: 78-Ball VFBGA Package - Top View.

# HV2802/HV2902

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Symbol           |                  | Description                            |
|------------|------------------|------------------|--|
|            | 9x9x1.0 VFBGA    |                  |  |
|            | HV2802           | HV2902           |  |
| A1         | SW2B             | SW2B             | Analog switch 2 terminal B             |
| A3         | SW1B             | SW1B             | Analog switch 1 terminal B             |
| A4         | SW0B             | SW0B             | Analog switch 0 terminal B             |
| A5         | D <sub>OUT</sub> | D <sub>OUT</sub> | Data out logic output                  |
| A6         | GND              | GND              | Ground                                 |
| A7         | V <sub>DD</sub>  | V <sub>DD</sub>  | Logic supply voltage                   |
| A8         | LE               | LE               | Latch enable logic input, low active   |
| A10        | SW31A            | SW31A            | Analog switch 31 terminal A            |
| A11        | SW30A            | SW30A            | Analog switch 30 terminal A            |
| A13        | SW29B            | SW29B            | Analog switch 29 terminal B            |
| B1         | SW3A             | SW3A             | Analog switch 3 terminal A             |
| B2         | SW2A             | SW2A             | Analog switch 2 terminal A             |
| B4         | SW1A             | SW1A             | Analog switch 1 terminal A             |
| B5         | SW0A             | SW0A             | Analog switch 0 terminal A             |
| B6         | NC               | RGND             | No connect / Ground for bleed resistor |
| B7         | D <sub>IN</sub>  | D <sub>IN</sub>  | Data in logic input                    |
| B8         | CLK              | CLK              | Clock logic input for shift register   |
| B9         | CLR              | CLR              | Latch clear logic input                |
| B10        | SW31B            | SW31B            | Analog switch 31 terminal B            |
| B11        | SW30B            | SW30B            | Analog switch 30 terminal B            |
| B12        | SW28B            | SW28B            | Analog switch 28 terminal B            |
| B13        | SW29A            | SW29A            | Analog switch 29 terminal A            |
| C1         | SW4A             | SW4A             | Analog switch 4 terminal A             |
| C2         | SW3B             | SW3B             | Analog switch 3 terminal B             |
| C12        | SW27B            | SW27B            | Analog switch 27 terminal B            |
| C13        | SW28A            | SW28A            | Analog switch 28 terminal A            |
| D1         | SW5A             | SW5A             | Analog switch 5 terminal A             |
| D2         | SW4B             | SW4B             | Analog switch 4 terminal B             |
| D12        | SW26B            | SW26B            | Analog switch 26 terminal B            |
| D13        | SW27A            | SW27A            | Analog switch 27 terminal A            |
| E1         | SW6A             | SW6A             | Analog switch 6 terminal A             |
| E2         | SW5B             | SW5B             | Analog switch 5 terminal B             |
| E12        | SW25B            | SW25B            | Analog switch 25 terminal B            |
| E13        | SW26A            | SW26A            | Analog switch 26 terminal A            |
| F1         | SW7A             | SW7A             | Analog switch 7 terminal A             |
| F2         | SW6B             | SW6B             | Analog switch 6 terminal B             |
| F12        | SW24B            | SW24B            | Analog switch 24 terminal B            |
| F13        | SW25A            | SW25A            | Analog switch 25 terminal A            |
| G1         | SW8A             | SW8A             | Analog switch 8 terminal A             |
| G2         | SW7B             | SW7B             | Analog switch 7 terminal B             |
| G12        | SW23B            | SW23B            | Analog switch 23 terminal B            |
| G13        | SW24A            | SW24A            | Analog switch 24 terminal A            |

**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

| Pin Number | Symbol          |                 | Description                          |
|------------|-----------------|-----------------|--------------------------------------|
|            | 9x9x1.0 VFBGA   |                 |                                      |
|            | HV2802          | HV2902          |                                      |
| H1         | SW9A            | SW9A            | Analog switch 9 terminal A           |
| H2         | SW8B            | SW8B            | Analog switch 8 terminal B           |
| H12        | SW22B           | SW22B           | Analog switch 22 terminal B          |
| H13        | SW23A           | SW23A           | Analog switch 23 terminal A          |
| J1         | SW10A           | SW10A           | Analog switch 10 terminal A          |
| J2         | SW9B            | SW9B            | Analog switch 9 terminal B           |
| J12        | SW21B           | SW21B           | Analog switch 21 terminal B          |
| J13        | SW22A           | SW22A           | Analog switch 22 terminal A          |
| K1         | SW11A           | SW11A           | Analog switch 11 terminal A          |
| K2         | SW10B           | SW10B           | Analog switch 10 terminal B          |
| K12        | SW20B           | SW20B           | Analog switch 20 terminal B          |
| K13        | SW21A           | SW21A           | Analog switch 21 terminal A          |
| L1         | SW12A           | SW12A           | Analog switch 12 terminal A          |
| L2         | SW11B           | SW11B           | Analog switch 11 terminal B          |
| L12        | SW19B           | SW19B           | Analog switch 19 terminal B          |
| L13        | SW20A           | SW20A           | Analog switch 20 terminal A          |
| M1         | SW13A           | SW13A           | Analog switch 13 terminal A          |
| M2         | SW12B           | SW12B           | Analog switch 12 terminal B          |
| M6         | SW14A           | SW14A           | Analog switch 14 terminal A          |
| M7         | SW15A           | SW15A           | Analog switch 15 terminal A          |
| M8         | SW16A           | SW16A           | Analog switch 16 terminal A          |
| M9         | SW17A           | SW17A           | Analog switch 17 terminal A          |
| M10        | NC              | RGND            | No connect/Ground for bleed resistor |
| M12        | SW18A           | SW18A           | Analog switch 18 terminal A          |
| M13        | SW19A           | SW19A           | Analog switch 19 terminal A          |
| N1         | SW13B           | SW13B           | Analog switch 13 terminal B          |
| N2         | V <sub>NN</sub> | V <sub>NN</sub> | Negative supply voltage              |
| N4         | V <sub>PP</sub> | V <sub>PP</sub> | Positive supply voltage              |
| N5         | NC              | RGND            | No connect/Ground for bleed resistor |
| N6         | SW14B           | SW14B           | Analog switch 14 terminal B          |
| N7         | SW15B           | SW15B           | Analog switch 15 terminal B          |
| N8         | SW16B           | SW16B           | Analog switch 16 terminal B          |
| N9         | SW17B           | SW17B           | Analog switch 17 terminal B          |
| N10        | V <sub>PP</sub> | V <sub>PP</sub> | Positive supply voltage              |
| N12        | V <sub>NN</sub> | V <sub>NN</sub> | Negative supply voltage              |
| N13        | SW18B           | SW18B           | Analog switch 18 terminal B          |

# HV2802/HV2902

## 3.0 TEST CIRCUIT EXAMPLES

This section details test circuit examples for a few electrical characteristics. The RGND pins are found only on the HV2902 device. The Switch DC Offset of HV2802 needs 100 kΩ external load.

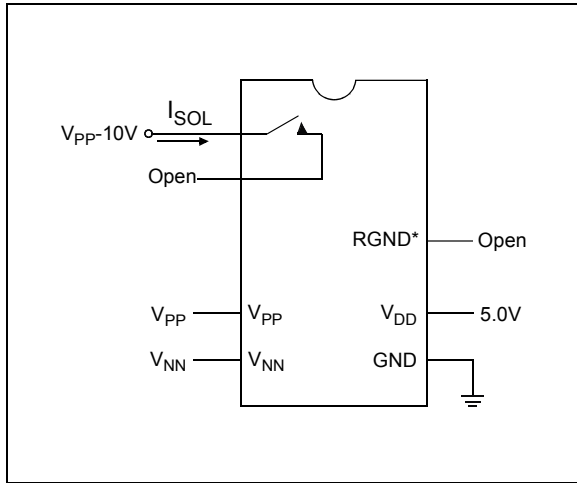


FIGURE 3-1: Switch Off Leakage per Switch.

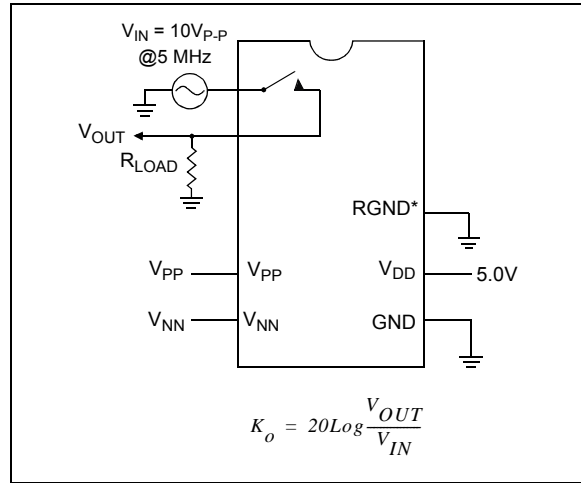


FIGURE 3-4: Off Isolation.

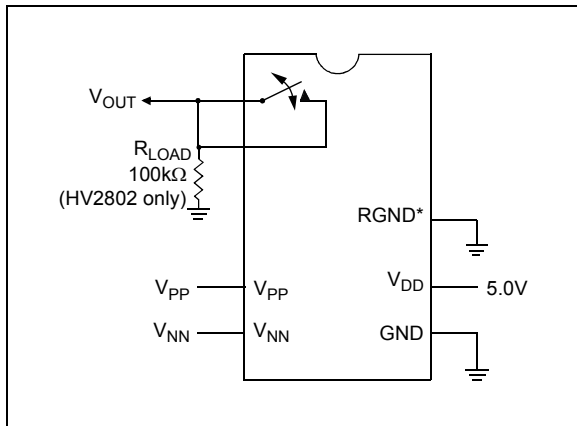


FIGURE 3-2: Switch DC Offset.

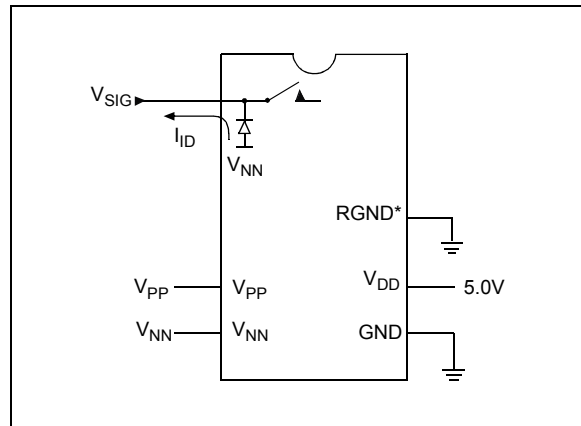


FIGURE 3-5: Output Switch Isolation Diode Current.

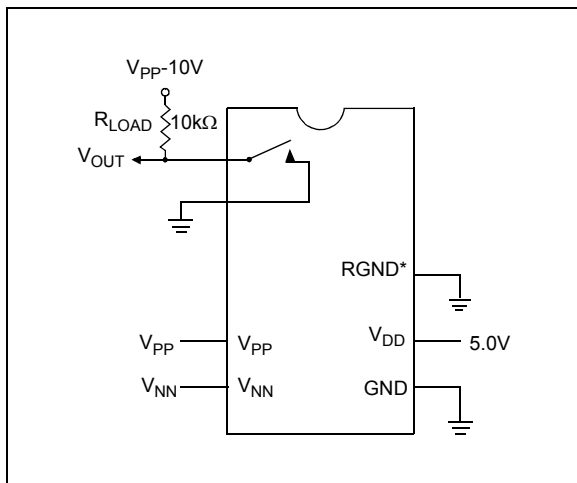


FIGURE 3-3:  $T_{ON}/T_{OFF}$  Test Circuit.

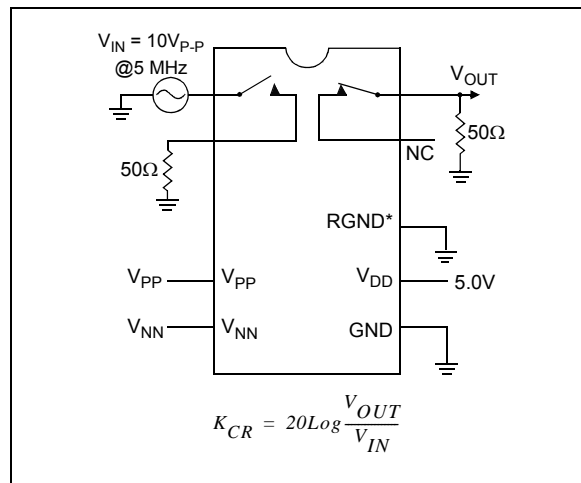


FIGURE 3-6: Switch Crosstalk.

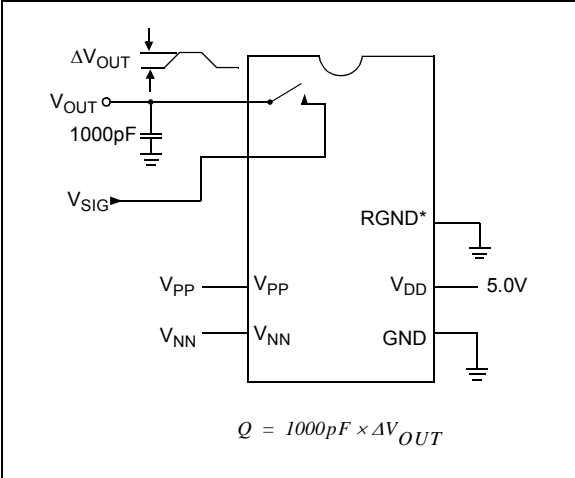


FIGURE 3-7: Charge Injection.

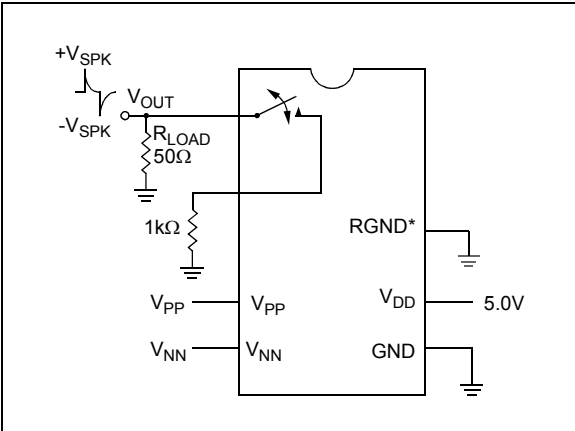


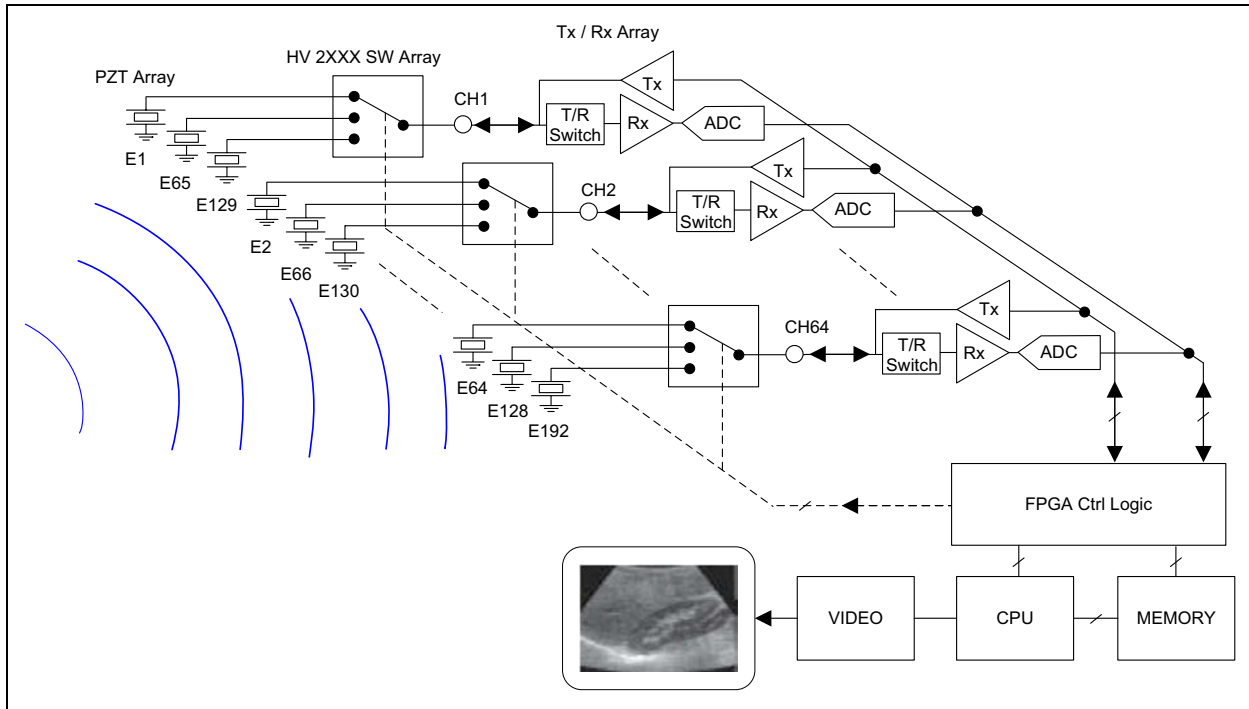
FIGURE 3-8: Output Voltage Spike.

# HV2802/HV2902

## 4.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitters (Tx) arrays in a medical ultrasound system.

Figure 4-1 shows a typical medical ultrasound image system comprising 64-channels of transmit pulsers, 64-channels of receivers (LNA and ADC) and 64-channels of T/R switches connecting to 192 elements of an ultrasound transducer probe via a high-voltage analog switch array.



**FIGURE 4-1:** Typical Medical Ultrasound Imaging System.

The HV2802/HV2902 devices are comprised of two main circuitries:

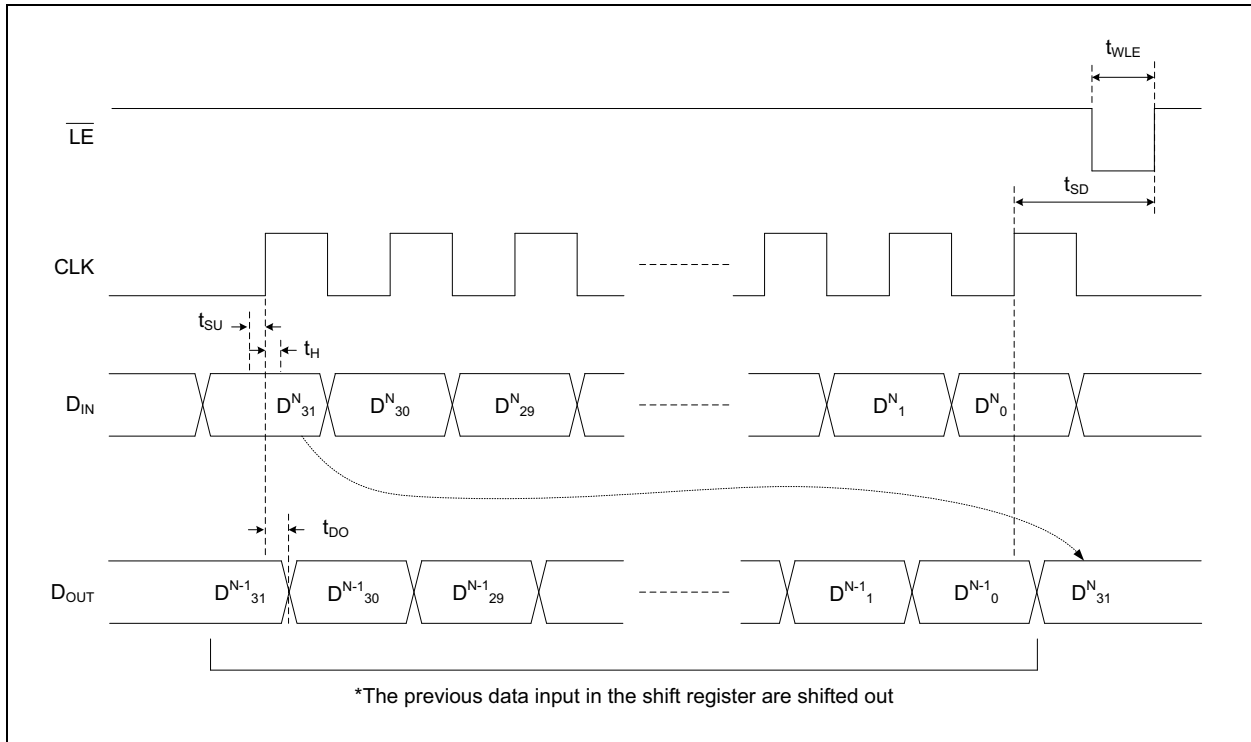
- A low-power CMOS digital serial interface powered by  $V_{DD}$  to control the high-voltage analog switches
- High-voltage bilateral analog switch.

High-voltage supplies  $V_{PP}$  and  $V_{NN}$  are needed by the high-voltage level translation circuitry to control the states of the output high-voltage analog switches. In addition, each high-voltage analog switch can be independently controlled because each switch is controlled via a corresponding latch. A 32-bit shift register and 32 latches allow the user to serially load data into the registers, and after completion, to load the data onto the latches that control the states of the high-voltage analog switches.

The HV2802/HV2902 have a digital serial interface consisting of logic signals, Data In ( $D_{IN}$ ), Clock (CLK), Data Out ( $D_{OUT}$ ), Latch Enable ( $\overline{LE}$ ) and Clear (CLR). The digital circuits are supplied by  $V_{DD}$  and either a 3.3V or a 5V logic can be used. With a  $V_{DD} = 5V$  supply, the serial clock frequency can operate up to 20 MHz.

The data is shifted into the shift registers on the rising edge (low-to-high transition) of the clock. The switch configuration bit of SW31 is shifted in first and the switch configuration bit of SW0 is shifted in last. To avoid clock feedthrough, the latch enable input ( $\overline{LE}$ ) should remain high while the 32-bit data-in signal is shifted into the 32-bit register. After the valid 32-bit data complete shifting into the shift registers, the high-to-low transition of the  $\overline{LE}$  signal transfers the contents of the shift register into the latches. Finally, setting the  $\overline{LE}$  high again allows all the latches to keep the current state, while new data can now be shifted into the shift registers without upsetting the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feedthrough noise. See Figure 4-2 for details.



**FIGURE 4-2:** Latch Enable Timing Waveforms.

When the CLR input is set high, all 32 latches are cleared of the data. Consequently, all the high-voltage switches are set to off state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Hence, after the CLR input is set low, the shift register would still retain the previous data.

The serial input interface of the HV2802/HV2902 allows multiple devices to daisy-chain together. In this configuration,  $D_{OUT}$  of a HV2802/HV2902 device is connected to the  $D_{IN}$  of the subsequent device, and so forth. The last  $D_{OUT}$  of the daisy-chained HV2802/HV2902 can either be floating or fed back to an FPGA to check the previously stored shift register data. To control all the high-voltage analog switch states in daisy-chained N devices, N times 32 clocks and N times 32 bits of data are shifted into shift registers, while  $\overline{LE}$  remains high and CLR remains low. After all N times 32 bits of data finish shifting in, the high-to-low transition of the  $\overline{LE}$  transfers the data from all N times 32-bit shift registers to N times 32 latches simultaneously. Consequently, all N times 32 high-voltage analog switches change states simultaneously.

It is recommended that 0.1  $\mu$ F ceramic decoupling capacitors, with the appropriate voltage ratings, be connected between GND and the other supplies ( $V_{DD}$ ,  $V_{PP}$  and  $V_{NN}$ ). These decoupling capacitors should be placed as close as possible to the device.

The HV2802/HV2902 devices do not have a specific power up/down sequence. During the power up/down period, all the analog switch inputs should be within the  $V_{PP}$  and  $V_{NN}$  range or floating. The rise time and fall time of the power supplies,  $V_{DD}$ ,  $V_{PP}$  and  $V_{NN}$ , should be greater than 1 ms. Violating the rise time or fall time requirement on the power supplies may cause malfunction such as latch-up or even permanent damage of the device.

The HV2902 device has 35 k $\Omega$  integrated bleed resistors connected from all the analog switch terminals A and B to RGND. These bleed resistors eliminate voltage build-up on capacitive loads such as piezoelectric transducers. The HV2802 device does not have integrated bleed resistors.

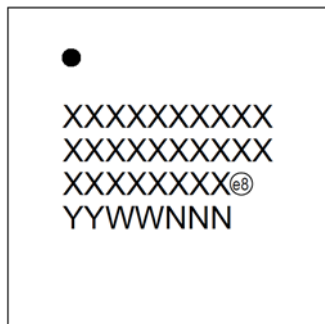
# HV2802/HV2902

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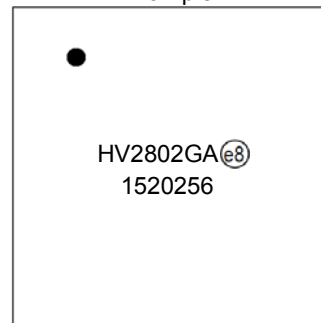
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

78-Ball VFBGA (9x9x1.0)



Example



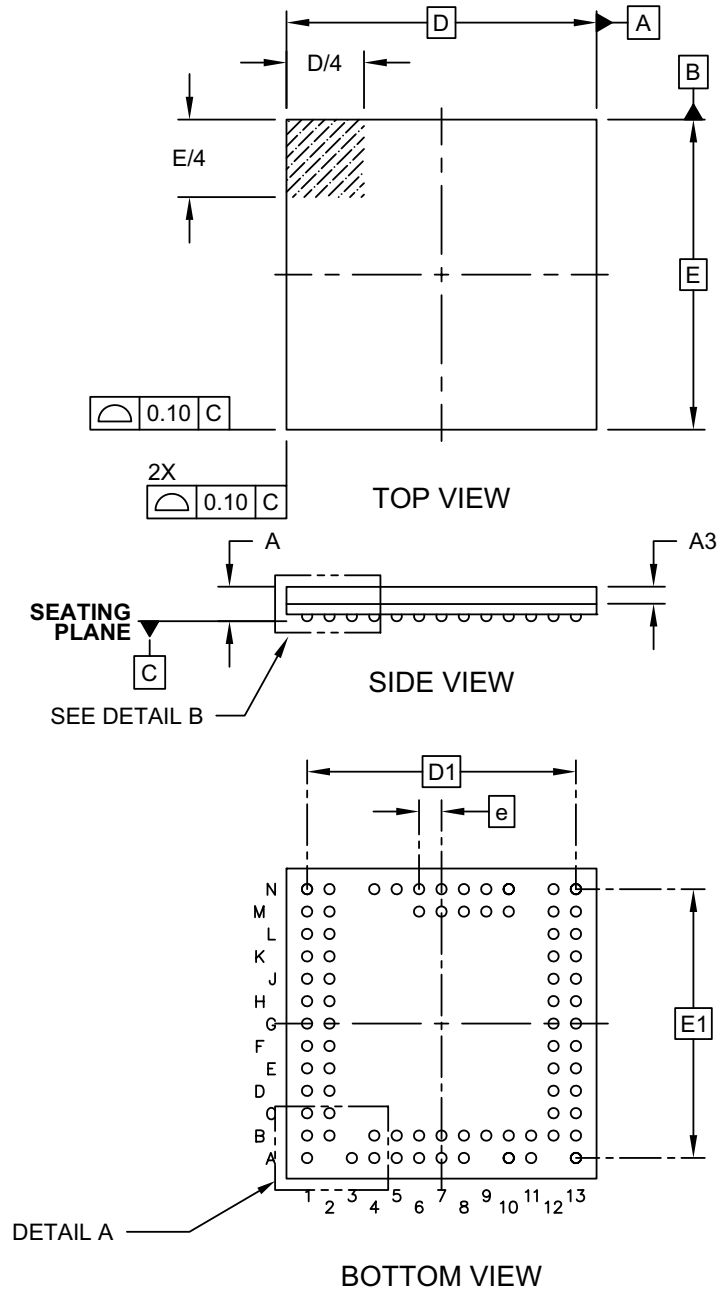
|                |        |  |
|----------------|--------|--|
| <b>Legend:</b> | XX...X | Customer-specific information  |
|                | Y      | Year code (last digit of calendar year)  |
|                | YY     | Year code (last 2 digits of calendar year)   |
|                | WW     | Week code (week of January 1 is week '01')   |
|                | NNN    | Alphanumeric traceability code   |
|                | (e8)   | Pb-free JEDEC designator for Matte Tin (Sn)  |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (e8) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



## 78-Ball Very Thin Fine Pitch Ball Grid Array (5G) - 9x9x1.0 mm Body [VFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



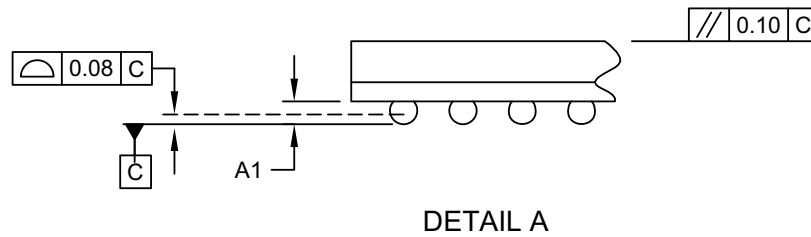
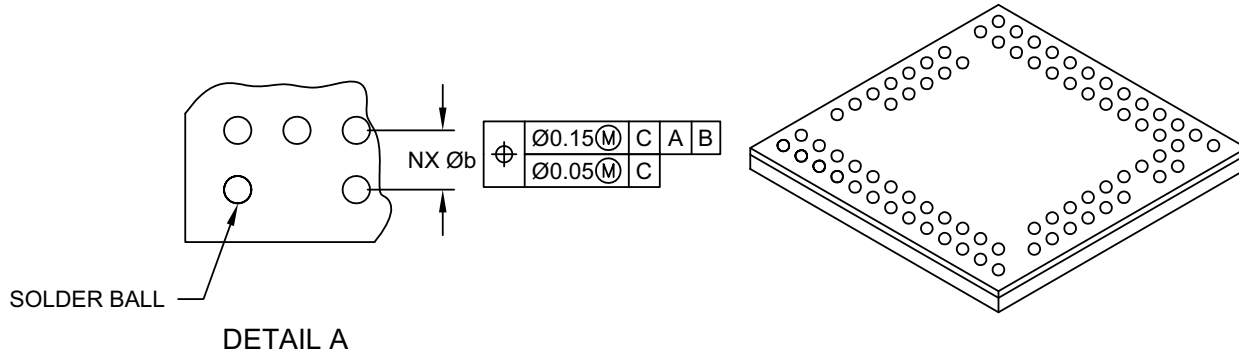
Microchip Technology Drawing C04-371A Sheet 1 of 2

# HV2802/HV2902

## 78-Ball Very Thin Fine Pitch Ball Grid Array (5G) - 9x9x1.0 mm Body [VFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at

<http://www.microchip.com/packaging>



| Dimension Limits     | Units | MILLIMETERS |      |      |
|----------------------|-------|-------------|------|------|
|                      |       | MIN         | NOM  | MAX  |
| Number of Pins       | N     | 78          |      |      |
| Pitch                | e     | 0.65 BSC    |      |      |
| Overall Height       | A     | -           | -    | 1.00 |
| Standoff             | A1    | 0.15        | 0.20 | 0.25 |
| Molded Cap Thickness | A3    | 0.45        | 0.50 | 0.55 |
| Overall Width        | E     | 9.00 BSC    |      |      |
| Overall Ball Pitch   | E1    | 7.80 BSC    |      |      |
| Overall Length       | D     | 9.00 BSC    |      |      |
| Overall Ball Pitch   | D1    | 7.80 BSC    |      |      |
| Ball Diameter        | Øb    | 0.25        | 0.30 | 0.35 |

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M

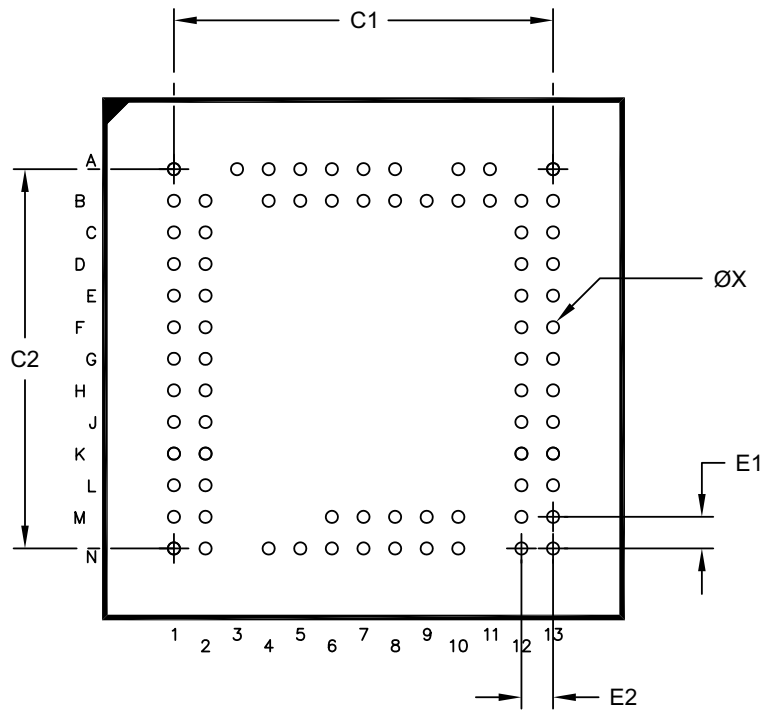
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-371A Sheet 2 of 2

## 78-Ball Very Thin Fine Pitch Ball Grid Array (5G) - 9x9x1.0 mm Body [VFPGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

|                            | Units | MILLIMETERS |      |     |
|----------------------------|-------|-------------|------|-----|
|                            |       | MIN         | NOM  | MAX |
| Contact Pitch              | E1    | 0.65 BSC    |      |     |
| Contact Pitch              | E2    | 0.65 BSC    |      |     |
| Contact Pad Spacing        | C1    |             | 780  |     |
| Contact Pad Spacing        | C2    |             | 7.80 |     |
| Contact Pad Diameter (X78) | X     |             | 0.25 |     |

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2371A

# HV2802/HV2902

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (October 2015)

- Original release of this document.

# HV2802/HV2902

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>XX-X</u>  |
|-----------------|--|
| Device          | Package  |
| Device          | HV2802: 32-Channel SPST, High-Voltage Analog Switch<br>HV2902: 32-Channel SPST, High-Voltage Analog Switch<br>with Bleed Resistors |
| Package         | GA-G = Very Thin Fine Pitch Ball Grid Array (5G) -<br>9x9x1.0 mm (VFBGA), 78-Ball  |

**Examples:**  
a) HV2802GA-G: 78-Ball VFBGA package  
b) HV2902GA-G: 78-Ball VFBGA package

# HV2802/HV2902

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NOTES:



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**Note the following details of the code protection feature on Microchip devices:**

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