HV2809

32-Channel Low Harmonic Distortion High-Voltage Analog Switch Relay Replacement IC

Features

- 32-channel High-voltage Analog Switch
- 2:1 Multiplexer/Demultiplexer
- Enable Control for All-OFF State
- 3.3V or 5V CMOS Input Logic Level
- Extremely Low –10 µA Quiescent Power Dissipation
- Low Parasitic Capacitance
- DC to 50 MHz Analog Signal Frequency
- –60 dB Typical Off-isolation at 5 MHz
- CMOS Logic Circuitry for Low Power
- Excellent Noise Immunity
- Flexible Operating Supply Voltages

Applications

- Electromechanical Relay Replacement in Medical Ultrasound Probes

General Description

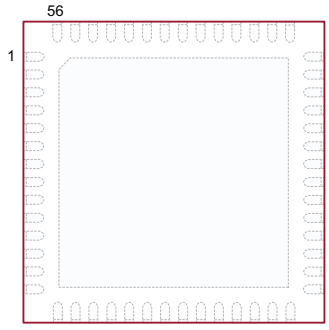
The HV2809 is a 32-channel, low harmonic distortion, high-voltage analog switch integrated circuit designed for medical ultrasound imaging systems as a probe selection relay replacement. It serves as a 16 PDT (16-pole double-throw) high-voltage analog switch array. The enable function allows the parts to be configured as either a 2:1 or 4:1 multiplexer/demultiplexer. The HV2809 is a very fast transducer multiplexer that consumes minimal power and emits no audible noise.

This device combines high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals. The HV2809 is suitable for various combinations of high-voltage supplies, such as VPP/VNN: +40V/–160V, +100V/–100V, and +160V/–40V.

Moreover, the HV2809 comes in an 8 mm x 8 mm x 1 mm 56-lead VQFN package. Compared to an electromechanical relay, it does not only save considerable PCB area but also PCB-assembled height.

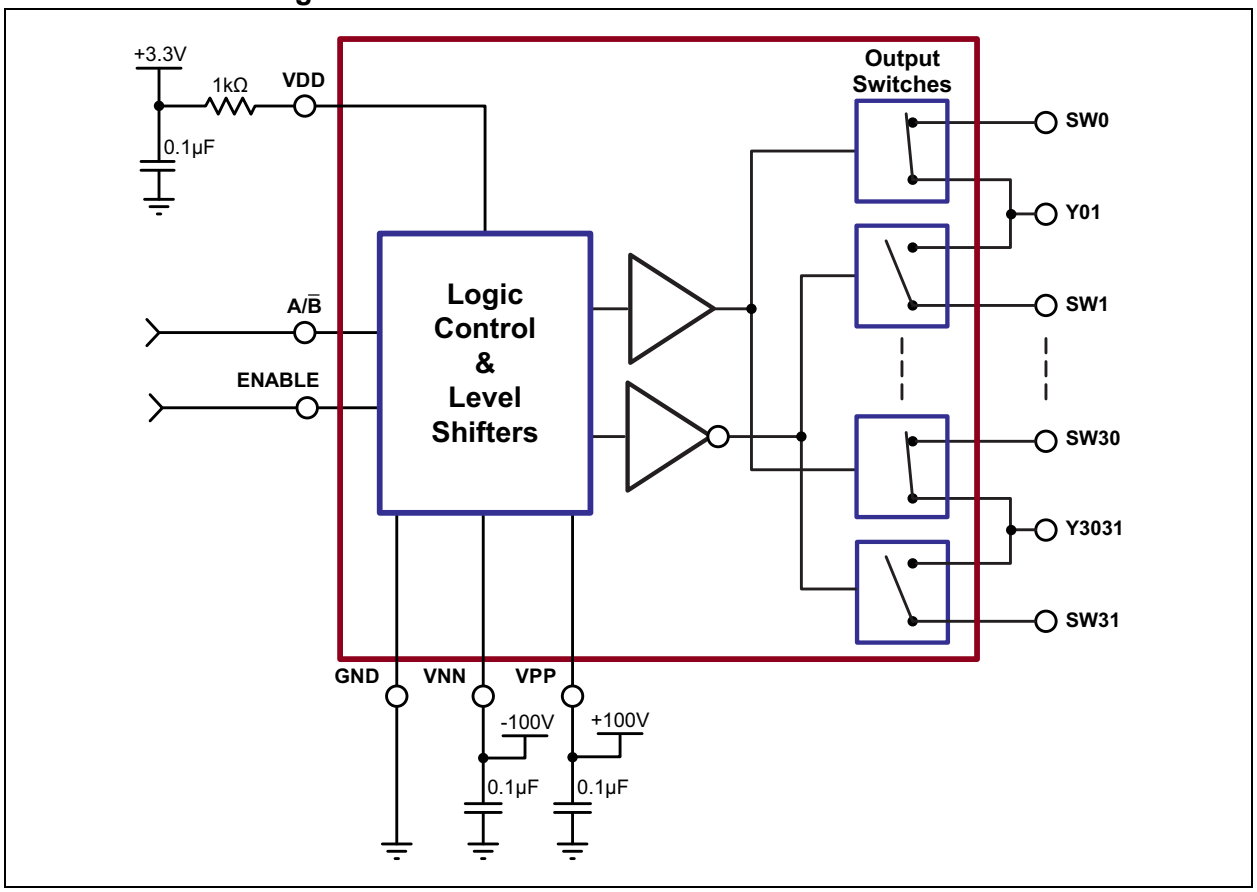
Package Type

56-lead VQFN
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Logic Power Supply Voltage, V_{DD} ..... –0.5V to +6.5V
Differential Supply Voltage, V_{PP}–V_{NN} 220V
High-voltage Positive Supply, V_{PP} ..... –0.5V to V_{NN} +200V
High-voltage Negative Supply, V_{NN} ..... +0.5V to –200V
Logic Input Voltage ..... –0.5V to V_{DD} +0.3V
Analog Signal Range ..... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel 3A
Storage Temperature, T_S ..... –65°C to 150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Power Supply Voltage	V_{DD}	3	—	5.5	V	**Note 1**, **Note 3**
High-voltage Positive Supply	V_{PP}	40	—	V_{NN} +200	V	**Note 1**, **Note 3**
High-voltage Negative Supply	V_{NN}	–40	—	–160	V	**Note 1**, **Note 3**
High-level Input Voltage	V_{IH}	0.9 V_{DD}	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0V	—	0.1 V_{DD}	V	
Analog Signal Voltage Peak to Peak	V_{SIG}	V_{NN} +10V	—	V_{PP}–10V	V	**Note 2**
Operating Ambient Temperature	T_A	0	—	70	°C	

Note 1: Power-up or power-down sequence is arbitrary except GND must be powered up first and powered down last.

2: V_{SIG} must be $V_{NN} \leq V_{SIG} \leq {}_{VPP}$ or floating during power-up or power-down transition.

3: Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1 millisecond.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions. See **Section 3.0 "Test Circuits"**.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch On-resistance	R_{ONS}	—	30	—	26	38	—	48	Ω	I_{SIG} = 5 mA	V_{PP} = +40V, V_{NN} = –160V
		—	25	—	22	27	—	32		I_{SIG} = 200 mA	
		—	25	—	22	27	—	30		I_{SIG} = 5 mA	V_{PP} = +100V, V_{NN} = –100V
		—	18	—	18	24	—	27		I_{SIG} = 200 mA	
		—	23	—	20	25	—	30		I_{SIG} = 5 mA	V_{PP} = +160V, V_{NN} = –40V
		—	22	—	16	25	—	27		I_{SIG} = 200 mA	
Small Signal Switch On-resistance Matching	ΔR_{ONS}	—	20	—	5	20	—	20	%	I_{SIG} = 5 mA, V_{PP} = +100V, V_{NN} = –100V	
Large Signal Switch On-resistance	R_{ONL}	—	—	—	15	—	—	—	Ω	V_{SIG} = V_{PP}–10V, I_{SIG} = 1A	
Switch-off Leakage per Switch	I_{SOL}	—	5	—	1	10	—	15	µA	V_{SIG} = V_{PP} – 10V, V_{NN}+10V	
DC Offset Switch-off	V_{OS}	—	300	—	100	300	—	300	mV	R_L = 100 kΩ	
DC Offset Switch-on		—	500	—	100	500	—	500			
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches off	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches off	
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches on, I_{SW} = 5 mA	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches on, I_{SW} = 5 mA	
Switch Output Peak Current	I_{SW}	—	3	—	3	2	—	2	A	V_{SIG} duty cycle < 0.1%	
Output Switching Frequency	f_{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V_{PP} Supply Current	I_{PP}	—	13	—	—	14	—	16	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	8	—	—	10	—	11		V_{PP} = +100V, V_{NN} = –100V	
		—	8	—	—	10	—	11		V_{PP} = +160V, V_{NN} = –40V	
Average V_{NN} Supply Current	I_{NN}	—	13	—	—	14	—	16	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	8	—	—	10	—	11		V_{PP} = +100V, V_{NN} = –100V	
		—	8	—	—	10	—	11		V_{PP} = +160V, V_{NN} = –40V	
Logic Supply Average Current	I_{DD}	—	0.1	—	—	0.1	—	0.1	mA	V_{DD} = 5V at 50 KHz CW	
Logic Supply Quiescent Current	I_{DDQ}	—	10	—	—	10	—	10	µA	All logic inputs are static.	
Logic Input Capacitance	C_{IN}	—	10	—	—	10	—	10	pF		

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions. See **Section 3.0 "Test Circuits"**.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Turn-on Time	t_{ON}	—	30	—	15	30	—	30	µs	$V_{SIG} = V_{PP} –10V$, $V_{PP} = +100V$, $R_{LOAD} = 10k\Omega$, $V_{NN} = –100V$
Turn-off Time	t_{OFF}	—	30	—	15	30	—	30		
Maximum V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	$V_{PP} = +40V$, $V_{NN} = –160V$
		—	20	—	—	20	—	20		$V_{PP} = +100V$, $V_{NN} = –100V$
		—	20	—	—	20	—	20		$V_{PP} = +160V$, $V_{NN} = –40V$
Off Isolation	K_O	–30	—	–30	–33	—	–30	—	dB	f = 5 MHz,1 kΩ//15 pF load
		–58	—	–58	—	—	–58	—		f = 5 MHz, 50Ω load
Switch Crosstalk	K_{CR}	–60	—	–60	–70	—	–60	—	dB	f = 5 MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	14	—	9	14	—	14	pF	V_{SIG} = 0V, f = 1 MHz, both SW off
Off Capacitance Y to GND		—	28	—	18	28	—	28		
On Capacitance SW to GND	$C_{SG(ON)}$	—	33	—	23	33	—	33	pF	V_{SIG} = 0V, f = 1 MHz, one SW on, one SW off
On Capacitance Y to GND		—	33	—	23	33	—	33		
Output Voltage Spike SW	$+V_{SPK}$	—	250	—	—	250	—	250	mV	$V_{PP} = +40V$, $V_{NN} = –160V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
	$+V_{SPK}$	—	250	—	—	250	—	250		$V_{PP} = +100V$, $V_{NN} = –100V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
	$+V_{SPK}$	—	250	—	—	250	—	250		$V_{PP} = +160V$, $V_{NN} = –40V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
Output Voltage Spike Y	$+V_{SPK}$	—	250	—	—	250	—	250	mV	$V_{PP} = +40V$, $V_{NN} = –160V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
	$+V_{SPK}$	—	250	—	—	250	—	250		$V_{PP} = +100V$, $V_{NN} = –100V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
	$+V_{SPK}$	—	250	—	—	250	—	250		$V_{PP} = +160V$, $V_{NN} = –40V$, $R_{LOAD} = 50\Omega$
	$–V_{SPK}$	—	250	—	—	250	—	250		
Charge Injection	QC	—	—	—	1020	—	—	—	pC	$V_{PP} = +40V$, $V_{NN} = –160V$
		—	—	—	700	—	—	—		$V_{PP} = +100V$, $V_{NN} = –100V$
		—	—	—	370	—	—	—		$V_{PP} = +160V$, $V_{NN} = –40V$

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Junction Temperature	T_J	0	—	125	°C	
Operating Ambient Temperature	T_A	0	—	70	°C	
Storage Temperature	T_S	–65	—	150	°C	
PACKAGE THERMAL RESISTANCE						
56-lead VQFN	θ_{JA}	—	21	—	°C/W	

TRUTH FUNCTION TABLE

Logic Inputs		Switch Status
ENABLE	**A/$\overline{B}$**	
H	H	SW0, 2, 4...30 ON, SW1, 3, 5...31 OFF
H	L	SW0, 2, 4...30 OFF, SW1, 3, 5...31 ON
L	X	All switches OFF

2.0 PIN DESCRIPTION

The details on the pins of HV2809 are listed in Table 2-1. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Y2829	Y terminal of analog switch 28 and 29
2	SW29	SW terminal of analog switch 29
3	SW30	SW terminal of analog switch 30
4	Y3031	Y terminal of analog switch 30 and 31
5	SW31	SW terminal of analog switch 31
6	ENABLE	SW enable logic control input
7	VDD	Logic supply voltage
8	A/$\overline{B}$	SW logic control input
9	GND	Ground
10	SW0	SW terminal of analog switch 0
11	Y01	Y terminal of analog switch 0 and 1
12	SW1	SW terminal of analog switch 1
13	SW2	SW terminal of analog switch 2
14	Y23	Y terminal of analog switch 2 and 3
15	SW3	SW terminal of analog switch 3
16	SW4	SW terminal of analog switch 4
17	Y45	Y terminal of analog switch 4 and 5
18	SW5	SW terminal of analog switch 5
19	SW6	SW terminal of analog switch 6
20	Y67	Y terminal of analog switch 6 and 7
21	SW7	SW terminal of analog switch 7
22	SW8	SW terminal of analog switch 8
23	Y89	Y terminal of analog switch 8 and 9
24	SW9	SW terminal of analog switch 9
25	SW10	SW terminal of analog switch 10
26	Y1011	Y terminal of analog switch 10 and 11
27	SW11	SW terminal of analog switch 11
28	SW12	SW terminal of analog switch 12
29	Y1213	Y terminal of analog switch 12 and 13
30	SW13	SW terminal of analog switch 13
31	VNN	High-voltage negative supply
32	SW14	SW terminal of analog switch 14
33	Y1415	Y terminal of analog switch 14 and 15
34	SW15	SW terminal of analog switch 15
35	VPP	High-voltage positive supply
36	VPP	High-voltage positive supply
37	SW16	SW terminal of analog switch 16
38	Y1617	Y terminal of analog switch 16 and 17
39	SW17	SW terminal of analog switch 17
40	VNN	High-voltage negative supply

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
41	SW18	SW terminal of analog switch 18
42	Y1819	Y terminal of analog switch 18 and 19
43	SW19	SW terminal of analog switch 19
44	SW20	SW terminal of analog switch 20
45	Y2021	Y terminal of analog switch 20 and 21
46	SW21	SW terminal of analog switch 21
47	SW22	SW terminal of analog switch 22
48	Y2223	Y terminal of analog switch 22 and 23
49	SW23	SW terminal of analog switch 23
50	SW24	SW terminal of analog switch 24
51	Y2425	Y terminal of analog switch 24 and 25
52	SW25	SW terminal of analog switch 25
53	SW26	SW terminal of analog switch 26
54	Y2627	Y terminal of analog switch 26 and 27
55	SW27	SW terminal of analog switch 27
56	SW28	SW terminal of analog switch 28
VSUB (Thermal Pad)		The central thermal pad on the bottom of package must be connected to VNN externally.

3.0 TEST CIRCUITS

Refer to Figure 3-1 to Figure 3-9 for the test circuits of HV2809.

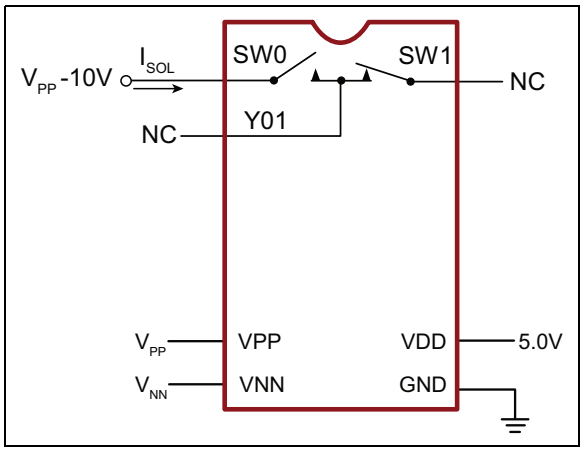


FIGURE 3-1: *Switch-off Leakage.*

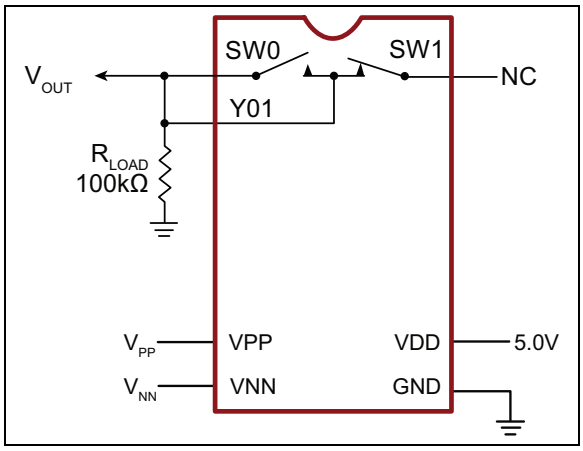


FIGURE 3-2: *DC Offset On/Off.*

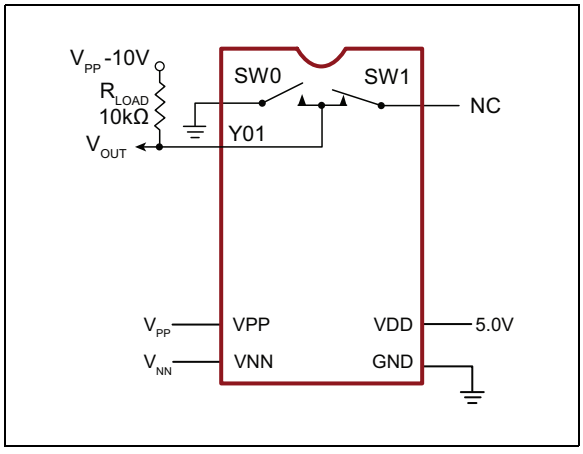


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

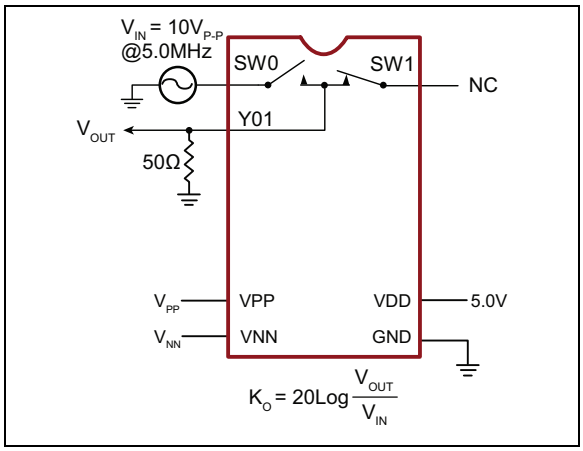


FIGURE 3-4: *Off Isolation.*

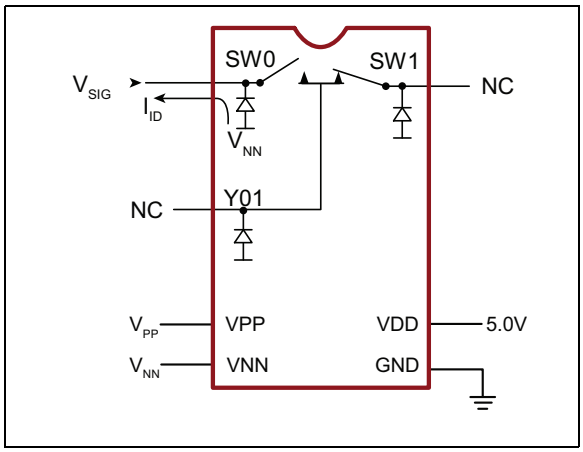


FIGURE 3-5: *Isolation Diode Current.*

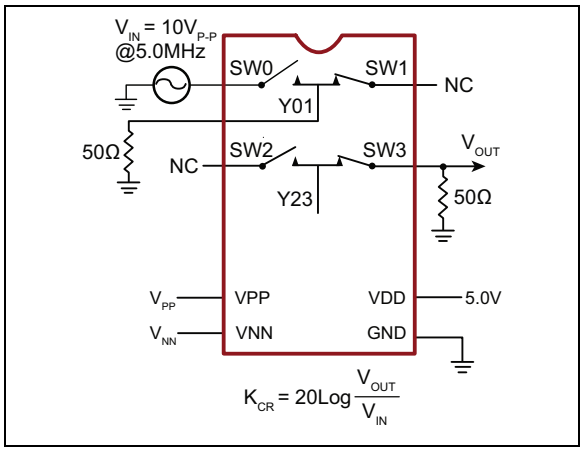


FIGURE 3-6: *Crosstalk.*

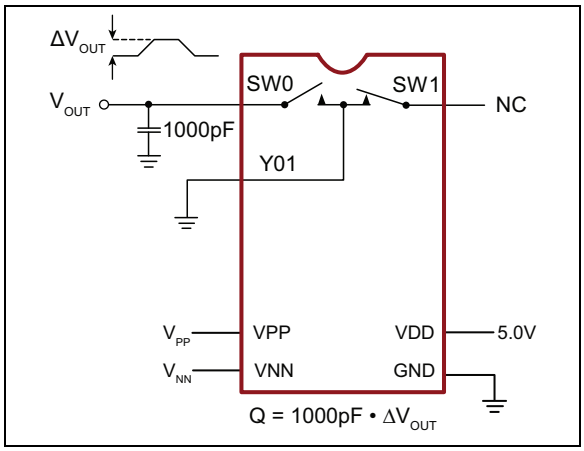


FIGURE 3-7: *Charge Injection.*

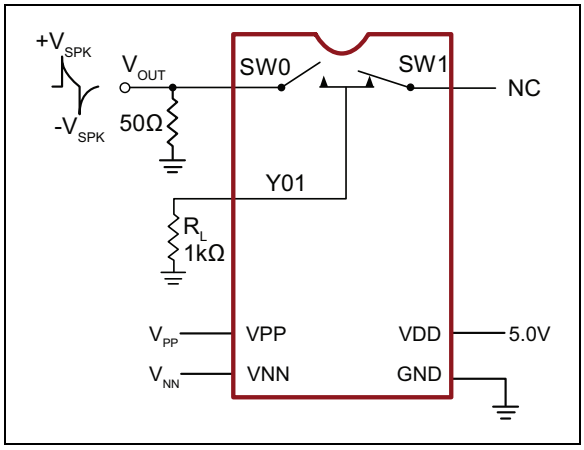


FIGURE 3-8: *Output Voltage Spike SW.*

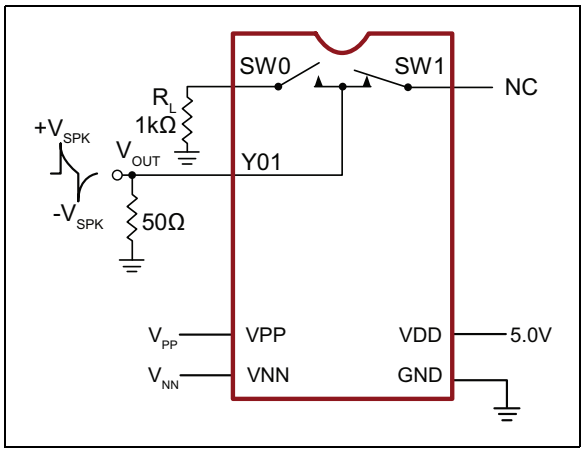


FIGURE 3-9: *Output Voltage Spike Y.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

56-lead VQFN

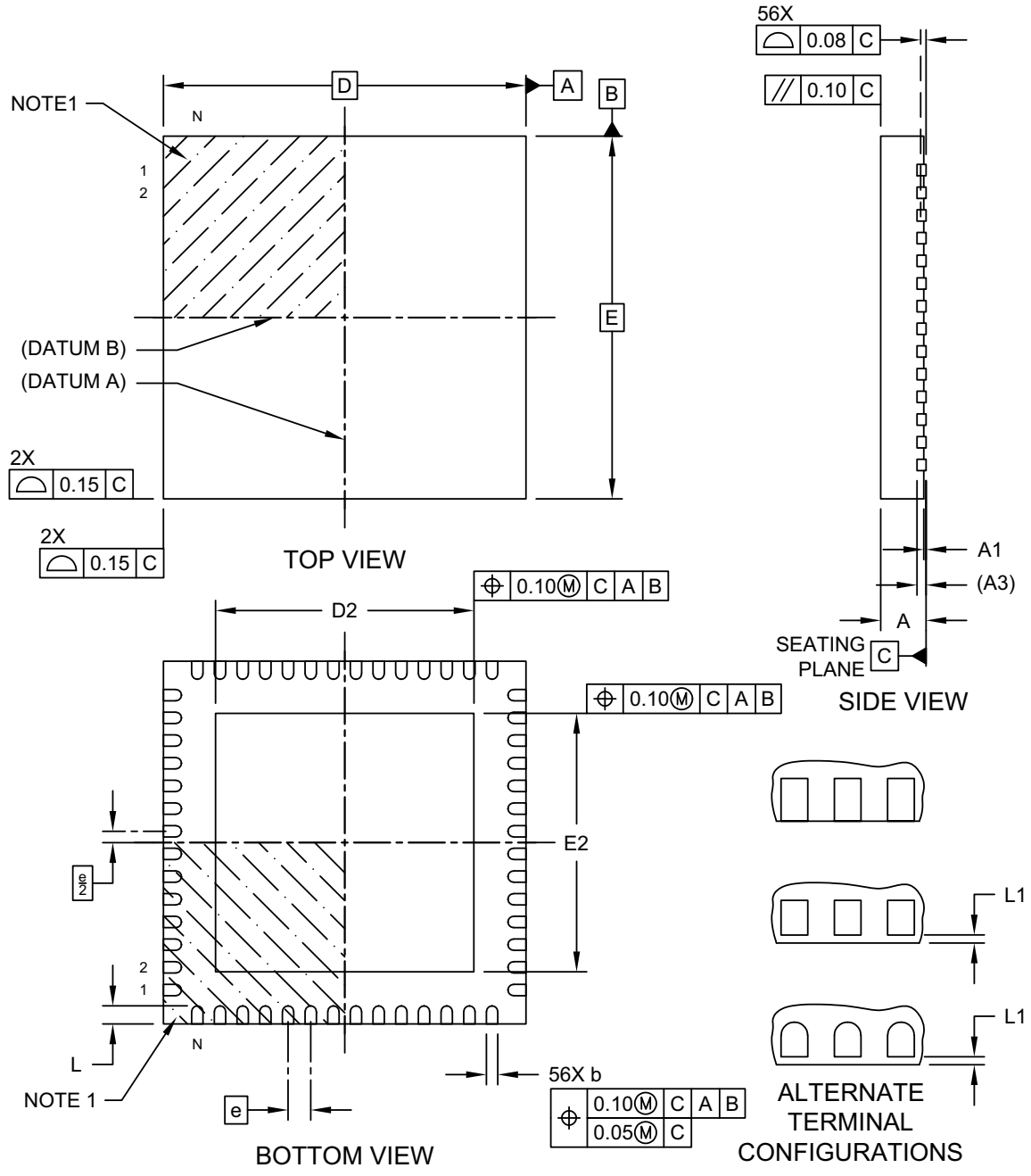
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN]
Supertex Legacy Package K6

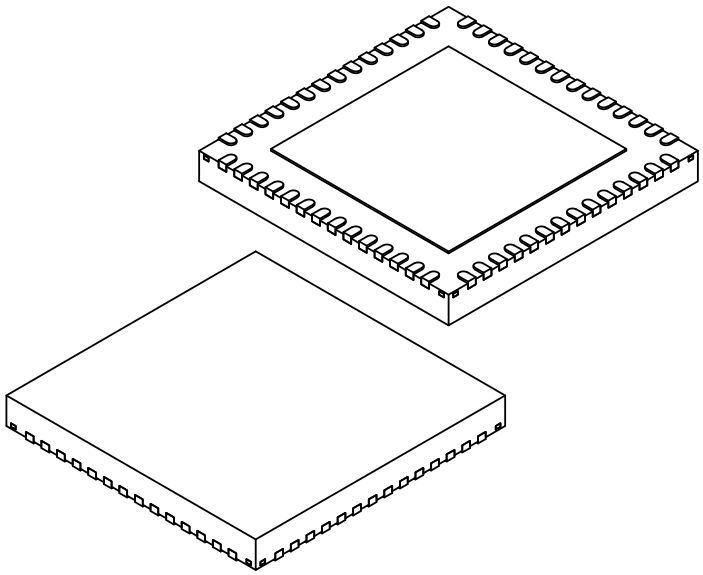
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-299-5XF Rev A Sheet 1 of 2

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN] Supertex Legacy Package K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		56	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	5.60	5.70	5.80
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	5.60	5.70	5.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Pullback (Optional)	L1	-	-	0.15

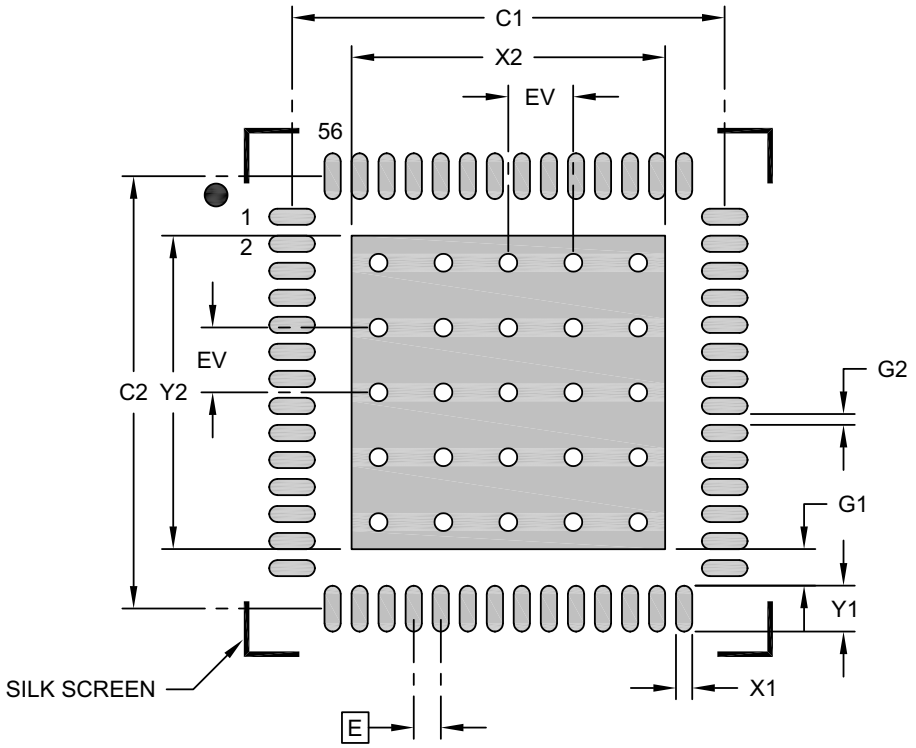
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-299-5XF Rev A Sheet 2 of 2

56-Lead Very Thin Quad Flat, No Lead Package (5XF) - 8x8x1.0 mm Body [VQFN] Supertex Legacy Package K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			5.80
Center Pad Length	Y2			5.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.68		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2299-5FX Rev A

APPENDIX A: REVISION HISTORY

Revision A (June 2023)

- Converted Supertex Doc# DSFP-HV2809 to Microchip DS20005727A
- Changed the quantity of the 56-lead QFN K6 M937 media type from 2000/Reel to 3000/Reel to align packaging specifications with the actual BQM
- Removed reference to “HVCMOS technology” from the document
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV2809	=	32-Channel Low Harmonic Distortion High-Voltage Analog Switch Relay Replacement IC
Package:	K6	=	56-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	250/Tray for a K6 Package
	M937	=	3000/Reel for a K6 Package

Examples:

a) HV2809K6-G: 32-Channel Low Harmonic Distortion High-Voltage Analog Switch Relay Replacement IC, 56-lead VQFN Package, 250/Tray

b) HV2809K6-G-M937: 32-Channel Low Harmonic Distortion High-Voltage Analog Switch Relay Replacement IC, 56-lead VQFN Package, 3000/Reel

Note the following details of the code protection feature on Microchip products:

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