Preliminary

32-Channel Serial To Parallel Converter With P-Channel Open Drain Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV41	HV4122DJ	HV4122PJ	HV4122X
HV42	HV4222DJ	HV4222PJ	HV4222X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages to -225V
- ☐ Source current minimum 80mA
- ☐ Shift register speed 8MHz
- ☐ Strobe and enable inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available
- ☐ Can be used with the HV51 and HV52 to provide 200V push-pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	+0.5V to -15.5V
Off state output voltage[1]	+0.5V to -250V
Logic input levels[1]	+0.5V to V_{DD} - 0.5V
Ground current[2]	1.5A
Continuous total power dissipation[3]	1200mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV41 and HV42 are low voltage serial to high voltage parallel converters wtih P-Channel open drain outputs.These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the logic high to low transition of the clock. The HV41 shifts in the counterclockwise direction when viewed from the top of the package and the HV42 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

For applications requiring active pull down as well as pull up, the HV41 and HV42 can be paired with the HV52 and HV51 devices, respectively. The footprint of the HV41 output pins matches the HV52 output pin footprint when the parts are mounted on opposite sides of a PC Board. Similarly the HV42 output footprint matches the HV51. The logic control and power pin locations do not match.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (voltages referenced to V_{SS})

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 4 MHz F_{DATA} = 2 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-50	µA	ALL V_{IN} = 0V
$I_{O(OFF)}$	Off state output current			-50	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	V_{IH} = -12V
I_{IL}	Low-level logic input current			+1	µA	V_{IL} = 0V
V_{OH}	High-level output data out			V_{DD} + 1.0V	V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{out}	-30.0		V	I_{HVout} = -80mA
		Data out	-1.0		V	I_{Dout} = -100µA
V_{OC}	HV_{out} clamp voltage			+1.5	V	I_{OL} = +80mA

AC Characteristics (@ V_{DD} = -12V, V_{SS} = 0V)

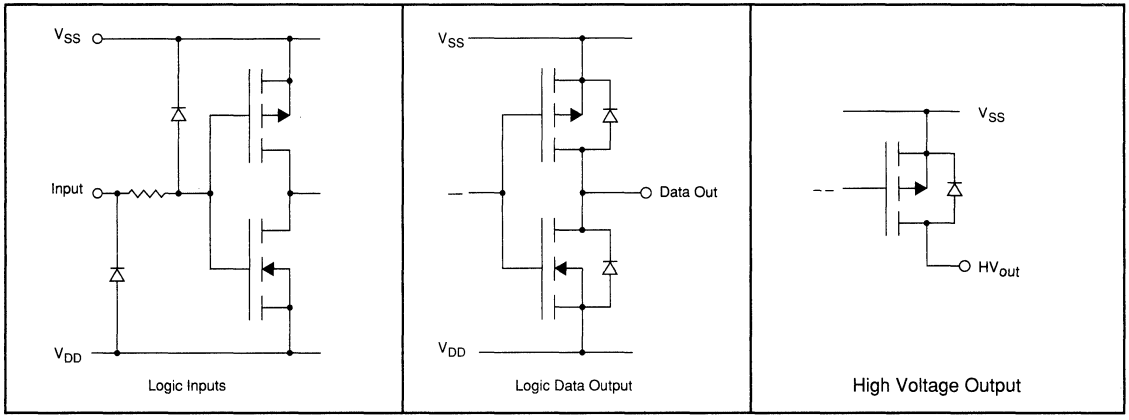
Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low	125		ns	
t_{SU}	Data set-up time before clock rises	50		ns	
t_H	Data hold time after clock rises	20		ns	
t_{ON}	Turn ON time, HV_{out} from enable		400	ns	R_L = 10K to -225V
t_{DHL}	Delay time clock to data high to low		100	ns	
t_{DLH}	Delay time clock to data low to high		100	ns	

Recommended Operating Conditions

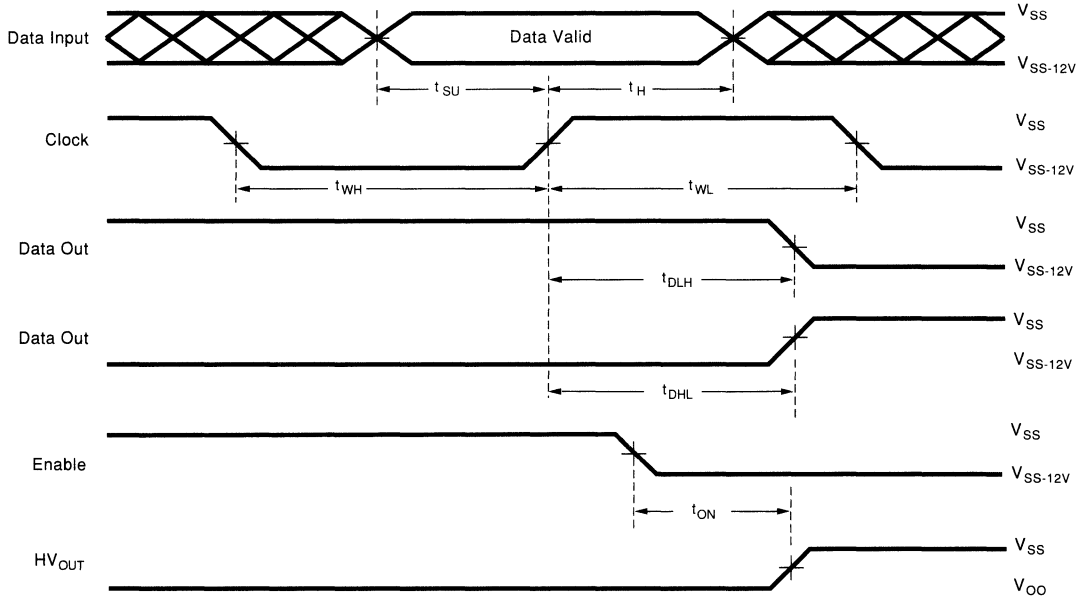
Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Logic supply voltage		-10.8	-12	-13.2	V
V_{OO}	Output off voltage		+0.3		-225	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V		V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0		-2.0	V
f_{CLK}	Clock frequency				4	MHz
T_A	Operating free-air temperature	Commercial	-40		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

Note 1: All voltages are referenced to V_{SS}.

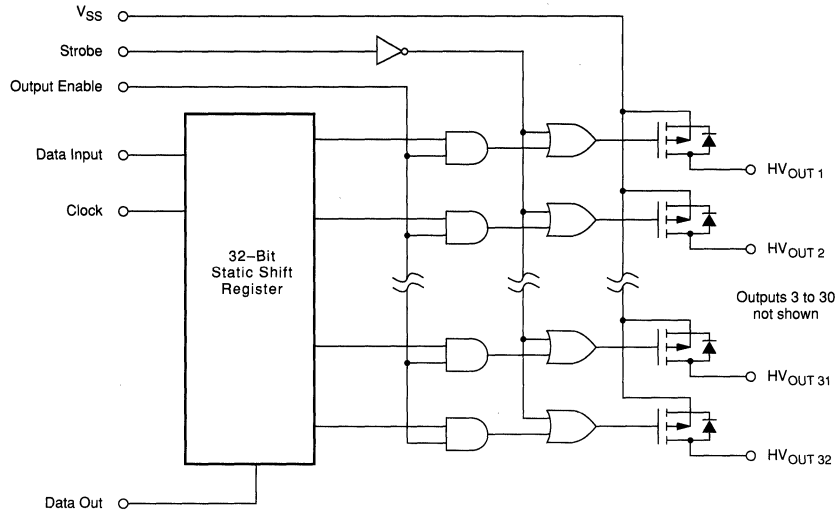
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs		
	DI	CLK	OE	STR	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *
All on	X	X	X	L	* *...*	All On	*
All off	X	X	L	H	* *...*	All Off	*
Load S/R	H or L	↓	L	H	H or L *...*	On or Off *...*	
Output enable	X	H or L	H	H	* *...*	On or Off *...*	*

Notes:

X = Not relevant to the output state.

* = Dependent on previous stage's state before the last CLK : High to low transition.

A logic high bit in the shift register will turn on the corresponding output when the strobe and output enable inputs are both high.

↓ = High to low transition, -12V to V_{SS}

H = High level = -12V

L = Low level = 0V

Pin Configurations

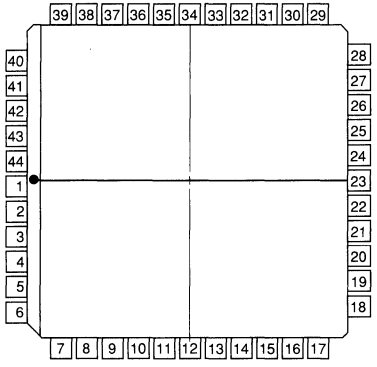
HV41
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Output Enable
2	HVout 18	24	Clock
3	HVout 19	25	V_{SS}
4	HVout 20	26	V_{DD}
5	HVout 21	27	Strobe
6	HVout 22	28	Data In
7	HVout 23	29	HVout 1
8	HVout 24	30	HVout 2
9	HVout 25	31	HVout 3
10	HVout 26	32	HVout 4
11	HVout 27	33	HVout 5
12	HVout 28	34	HVout 6
13	HVout 29	35	HVout 7
14	HVout 30	36	HVout 8
15	HVout 31	37	HVout 9
16	HVout 32	38	HVout 10
17	N/C	39	HVout 11
18	Data Out	40	HVout 12
19	N/C	41	HVout 13
20	N/C	42	HVout 14
21	N/C	43	HVout 15
22	N/C	44	HVout 16

HV42
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Output Enable
2	HVout 15	24	Clock
3	HVout 14	25	V_{SS}
4	HVout 13	26	V_{DD}
5	HVout 12	27	Strobe
6	HVout 11	28	Data In
7	HVout 10	29	HVout 32
8	HVout 9	30	HVout 31
9	HVout 8	31	HVout 30
10	HVout 7	32	HVout 29
11	HVout 6	33	HVout 28
12	HVout 5	34	HVout 27
13	HVout 4	35	HVout 26
14	HVout 3	36	HVout 25
15	HVout 2	37	HVout 24
16	HVout 1	38	HVout 23
17	N/C	39	HVout 22
18	Data Out	40	HVout 21
19	N/C	41	HVout 20
20	N/C	42	HVout 19
21	N/C	43	HVout 18
22	N/C	44	HVout 17

Package Outline



top view

44-pin J-lead Package