Preliminary

32-Channel Serial To Parallel Converter with P-Channel Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{OO} Max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in Waffle Pack
HV45	-300	HV4530DJ	HV4530PJ	HV4530X
	-220	HV4522DJ	HV4522PJ	HV4522X
HV46	-300	HV4630DJ	HV4630PJ	HV4630X
	-220	HV4622DJ	HV4622PJ	HV4622X

Features

- ☐ Processed with HVCMOS Technology
- ☐ Output voltages to -300V
- ☐ Source current minimum 60 mA
- ☐ Shift register speed 8 MHz
- ☐ Polarity and blanking inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available
- ☐ Can be used with the HV55 and HV56 to provide 300V push pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		+0.5V to -16V
Off state output voltage	HV4530/HV4630	+0.5V to -315V
	HV4522/ HV4622	+0.5V to -220V
Logic input levels[1]		+0.5V to V_{DD} - 0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]		1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV45 and HV46 are low-voltage serial to high-voltage parallel converters with P-Channel open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV45 shifts in the counterclockwise direction when viewed from the top of the package and the HV46 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV45 and HV46 can be paired with the HV55 and HV56 devices, respectively. The footprint of the HV45 output pins matches the HV55 output pin footprint when the parts are mounted on opposite sides of a PC Board.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 4 MHz F_{DATA} = 2 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-50	µA	$V_{IN} = V_{SS}$ or V_{DD}
$I_{O(OFF)}$	Off state output current			-50	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			+1	µA	$V_{IL} = V_{SS}$
V_{OH}	High-level output data out		V_{DD} + 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{out}		-30.0	V	I_{HVout} = -60mA
		Data out		-1.0	V	I_{Dout} = -100µA
V_{OC}	HV_{out} clamp voltage			+1.5	V	I_{OL} = +60mA

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low		125	ns	
t_{SU}	Data set-up time before clock rises		50	ns	
t_H	Data hold time after clock rises		20	ns	
t_{ON}	Turn ON time, HV_{out} from enable		400	ns	R_L = 10K to V_{OO} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

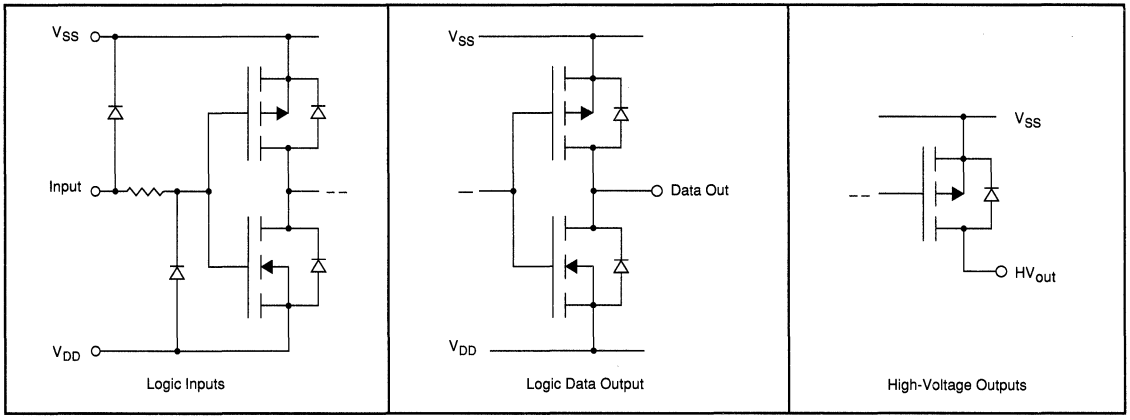
Recommended Operating Conditions

(Note 1)

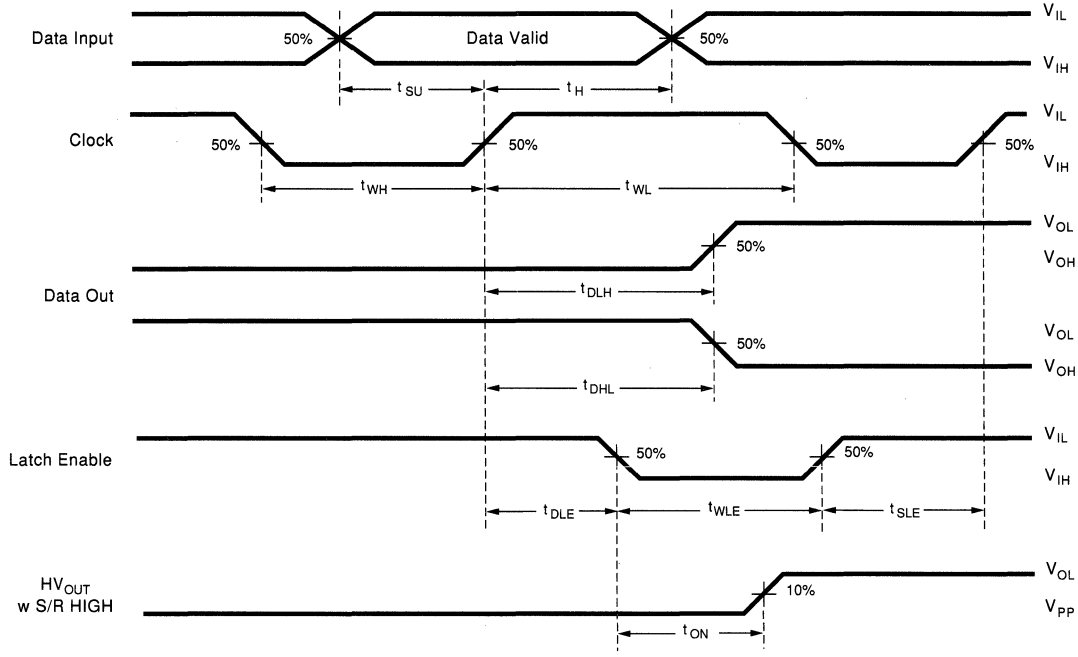
Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		-10.8	-13.2	V
V_{OO}	Output off voltage	HV4530 and HV4630	+0.3	-300	V
		HV4522 and HV4622	+0.3	-200	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V	V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0	-2.0	V
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Commercial	-40	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

Note 1: All voltages are referenced to V_{SS}.

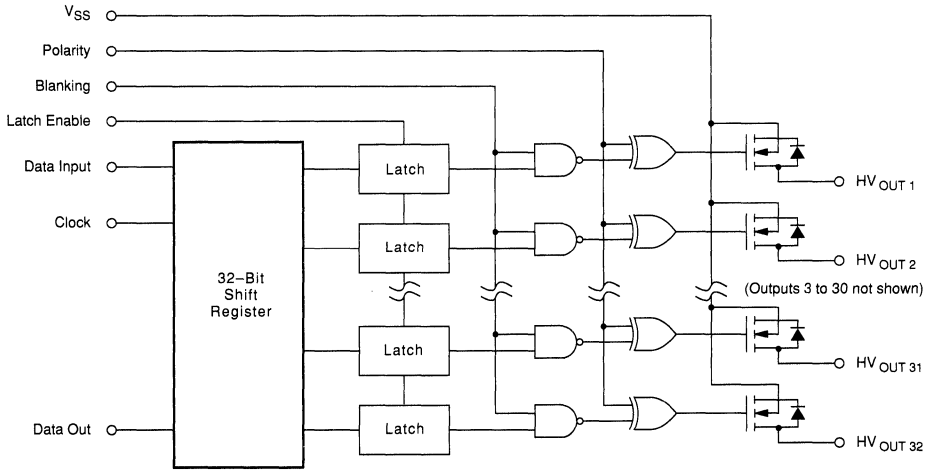
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L	*...*	L	*...*	*
	H	↓	H	H	H	H	*...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↓ = low-to-high transition, -12V to V_{SS}.
* = dependent on previous stage's state before the last CLK ↓ or last LE high.

Pin Configurations

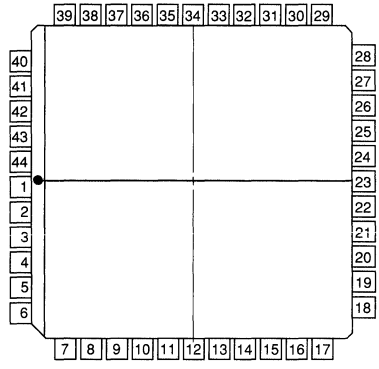
HV45
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Clock
2	HVout 18	24	V_{SS}
3	HVout 19	25	V_{DD}
4	HVout 20	26	Latch Enable
5	HVout 21	27	Data In
6	HVout 22	28	Blanking
7	HVout 23	29	HVout 1
8	HVout 24	30	HVout 2
9	HVout 25	31	HVout 3
10	HVout 26	32	HVout 4
11	HVout 27	33	HVout 5
12	HVout 28	34	HVout 6
13	HVout 29	35	HVout 7
14	HVout 30	36	HVout 8
15	HVout 31	37	HVout 9
16	HVout 32	38	HVout 10
17	N/C	39	HVout 11
18	Data Out	40	HVout 12
19	N/C	41	HVout 13
20	N/C	42	HVout 14
21	N/C	43	HVout 15
22	Polarity	44	HVout 16

HV46
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Clock
2	HVout 15	24	V_{SS}
3	HVout 14	25	V_{DD}
4	HVout 13	26	Latch Enable
5	HVout 12	27	Data In
6	HVout 11	28	Blanking
7	HVout 10	29	HVout 32
8	HVout 9	30	HVout 31
9	HVout 8	31	HVout 30
10	HVout 7	32	HVout 29
11	HVout 6	33	HVout 28
12	HVout 5	34	HVout 27
13	HVout 4	35	HVout 26
14	HVout 3	36	HVout 25
15	HVout 2	37	HVout 24
16	HVout 1	38	HVout 23
17	N/C	39	HVout 22
18	Data Out	40	HVout 21
19	N/C	41	HVout 20
20	N/C	42	HVout 19
21	N/C	43	HVout 18
22	Polarity	44	HVout 17

Package Outline



top view

44-pin J-lead Package