Preliminary

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options				
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die
HV500	HV500D	HV500P	HV500DJ	HV500PJ	HV500X

Features

- ☐ Processed with HVCMOS® Technology
- ☐ Output voltage of up to 100V
- ☐ CMOS push-pull output buffers
- ☐ Low-power level shifting
- ☐ Source/sink current minimum of 15mA
- ☐ Shift register speed 8MHz
- ☐ CMOS compatible inputs
- ☐ Output clamp diodes to V_{PP} and GND
- ☐ Direct replacement for the SN75500 and SN55500 series devices
- ☐ 44-lead plastic and ceramic surface mount packages available
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.3V to +15V
Supply voltage, V_{PP}[1]	-0.3V to +100V
Logic input levels[1]	-0.3V to V_{DD} + 0.3V
Ground currrent[2]	1.2A
Continuous total power dissipation[3]	1850mW
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV500 is a monolithic low-voltage logic to high-voltage output 32-channel driver for AC plasma flat panel displays. It is manufactured using the HVCMOS process, providing the high output voltages and currents possible with DMOS structures and the low power dissipation of CMOS logic.

The HV500 is comprised of an 8-stage DMOS shift register, four groups of eight high-voltage output buffers, and logic to select which group of outputs will reflect the status of the data in the shift register and strobe functions. When the strobe input is high, all outputs are held low independent of any other logic input. When strobe is brought low, the group of outputs selected by the state of the select inputs reflects the data in the shift register, and all non-selected outputs are held low.

The high-voltage output buffers have level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	I_{OH} = -1mA[1]
			90		V	I_{OH} = -15mA[1]
		Serial out	9		V	I_{OH} = -100µA[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	I_{OL} = 1mA
				5	V	I_{OL} = 15mA
		Serial out		1	V	I_{OL} = 100µA[2]
V_{OK}	High voltage output			2.5	V	I_{OK} = 20mA[3]
	Clamp voltage			-2.5	V	I_{OK} = -20mA[3]

Notes: 1. V_{PP} = 100V
2. V_{DD} = 10.8V
3. V_{PP} = 0V

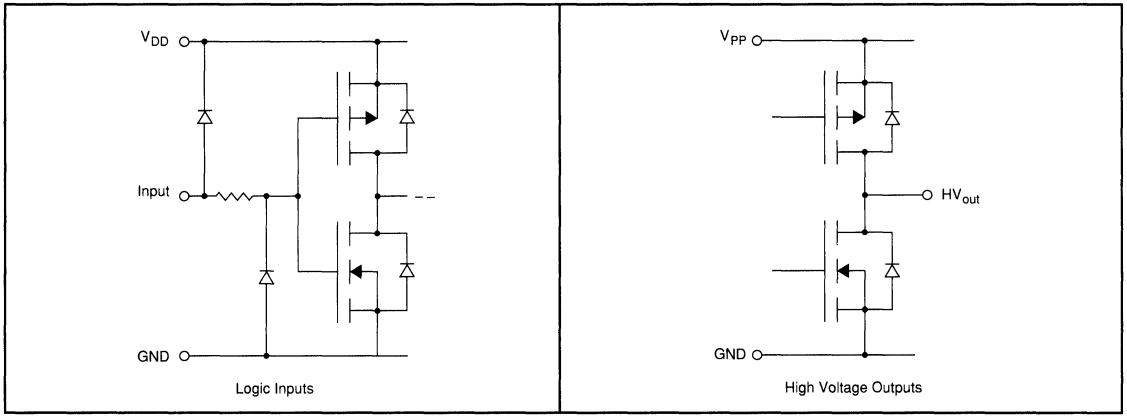
AC Characteristics (V_{DD} = 12V, V_{PP} = 100V, T_C = 25°C)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{DHL}	Delay time strobe to HV_{out} high to low		250		ns	C_L = 30pF
t_{DLH}	Delay time strobe to HV_{out} low to high		250		ns	
t_{SU}	Set-up time	Data in to clock ↑	20		ns	
		Select before strobe ↓	50		ns	
t_H	Hold time	Data after clock ↑	50		ns	
		Strobe high after clock ↑	50		ns	
		Select after strobe ↑	50		ns	
t_R	Rise time low to high HV_{out}			300	ns	C_L = 30pF
t_F	Fall time high to low HV_{out}			200	ns	C_L = 30pF

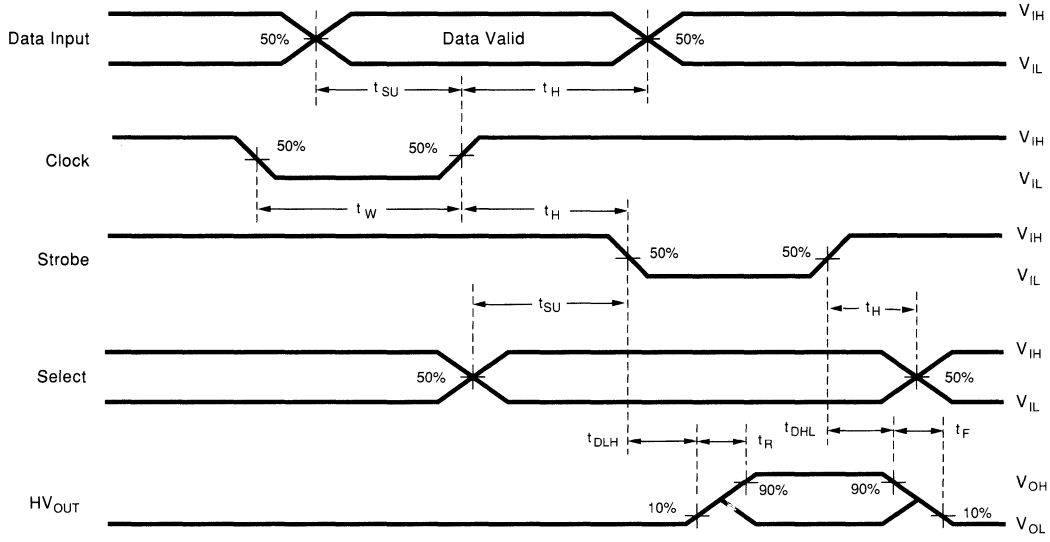
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+80	°C
		Military Hi-Rel (RB)	-55	+125	°C

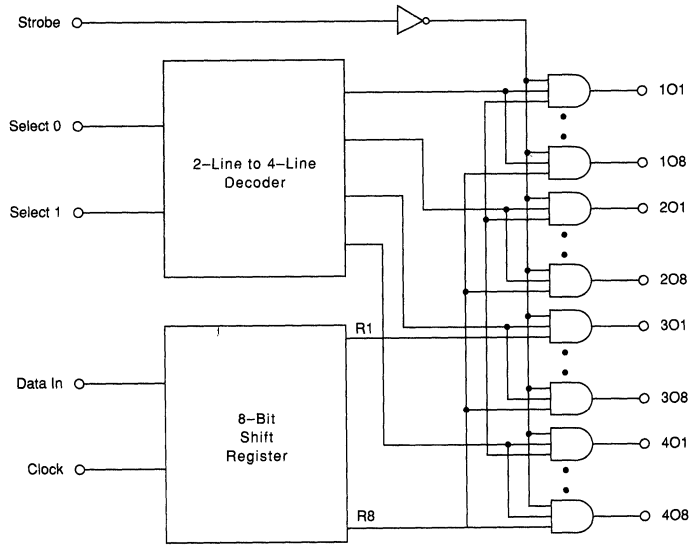
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Internal Levels			HV Outputs			
			Select			Shift Register						
	Data	Clk	S1	S0	Strb	R1	R2	R3...R8	1O1...1O8	2O1...2O8	3O1...3O8	4O1...4O8
Load	H	↑	X	X	H	L	R1n	R2n...R7n	L...L	L...L	L...L	L...L
	L	↑	X	X	H	H	R1n	R2n...R7n	L...L	L...L	L...L	L...L
Strobe	X	X	X	X	H	R1n	R2n	R3n...R8n	L...L	L...L	L...L	L...L
	X	H	L	L	L	R1n	R2n	R3n...R8n	R1...R8	L...L	L...L	L...L
	X	H	L	H	L	R1n	R2n	R3n...R8n	L...L	R1...R8	L...L	L...L
	X	H	H	L	L	R1n	R2n	R3n...R8n	L...L	L...L	R1...R8	L...L
	X	H	H	H	L	R1n	R2n	R3n...R8n	L...L	L...L	L...L	R1...R8

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1...R8 = levels currently at internal outputs of shift registers one through eight, respectively.
R1n...R8n = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

Pin Configurations

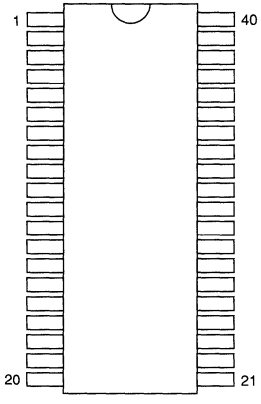
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Select 0	21	V_{PP}
2	Data In	22	3O8
3	Clock	23	3O7
4	1O1	24	3O6
5	1O2	25	3O5
6	1O3	26	3O4
7	1O4	27	3O3
8	1O5	28	3O2
9	1O6	29	3O1
10	1O7	30	4O8
11	1O8	31	4O7
12	2O1	32	4O6
13	2O2	33	4O5
14	2O3	34	4O4
15	2O4	35	4O3
16	2O5	36	4O2
17	2O6	37	4O1
18	2O7	38	Strobe
19	2O8	39	Select 1
20	GND	40	V_{DD}

44 Pin J-Lead

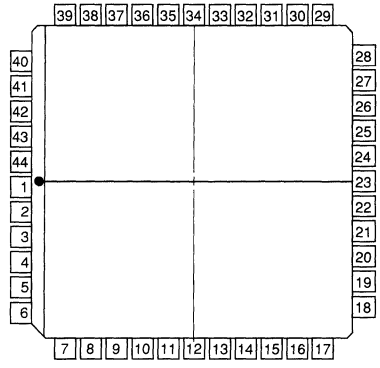
Pin	Function	Pin	Function
1	N/C	23	N/C
2	Select 0	24	V_{PP}
3	Data In	25	3O8
4	Clock	26	3O7
5	N/C	27	3O6
6	1O1	28	3O5
7	1O2	29	3O4
8	1O3	30	3O3
9	1O4	31	3O2
10	1O5	32	3O1
11	1O6	33	4O8
12	1O7	34	4O7
13	1O8	35	4O6
14	2O1	36	4O5
15	2O2	37	4O4
16	2O3	38	4O3
17	2O4	39	4O2
18	2O5	40	4O1
19	2O6	41	N/C
20	2O7	42	Strobe
21	2O8	43	Select 1
22	GND	44	V_{DD}

Package Outlines



top view

40-pin DIP



top view

44-pin J-lead Package