Preliminary

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options				
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die
HV501	HV501D	HV501P	HV501DJ	HV501PJ	HV501X

Features

- ☐ Processed with HVCMOS® Technology
- ☐ Output voltage of up to 100V
- ☐ DMOS push-pull output buffers
- ☐ Low-power level shifting
- ☐ Source/sink current minimum of 15mA
- ☐ Shift register speed 8MHz
- ☐ CMOS compatible inputs
- ☐ Output clamp diodes to V_{PP} and GND
- ☐ Direct replacement for the SN75501 and SN55501 series devices
- ☐ 44-lead plastic and ceramic surface mount packages available
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.3V to +15V
Supply voltage, V_{PP}[1]	-0.3V to +100V
Logic input levels[1]	-0.3V to V_{DD} + 0.3V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1850mW
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV501 is a 32-channel low-voltage serial to high-voltage parallel converter designed for use in matrix-addressable display applications. It is manufactured with the HVCMOS technology for enhanced ruggedness and performance. This device is a direct replacement for the SN75501 family of devices.

These devices are comprised of a 32-bit shift register with a serial data out, strobe and sustain control logic, and level shifters with high-voltage DMOS output buffers. When the strobe and sustain outputs are held high the outputs are held high. Data can then be clocked into the shift register without changing the state of the outputs. When the strobe input is brought low with the sustain input remaining high, the outputs will change state to reflect the status of the data in each output's corresponding shift register bit. A logic "1" in the shift register will cause the corresponding output to pull up to V_{PP}, and a logic "0" will cause the output to pull to GND. The sustain input is used to bring all the outputs low. When the sustain input is low, all outputs are low, independent of any other control input.

The high-voltage output buffers have low power level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	I_{OH} = -1mA[1]
			90		V	I_{OH} = -15mA[1]
		Data out	9		V	I_{OH} = -100µA[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	I_{OL} = 1mA
				5	V	I_{OL} = 15mA
		Data out		1	V	I_{OL} = 100µA[2]
V_{OK}	High voltage output			2.5	V	I_{OK} = 20mA[3]
	Clamp voltage			-2.5	V	I_{OK} = -20mA[3]

Notes: 1. V_{PP} = 100V
2. V_{DD} = 10.8V
3. V_{PP} = 0V

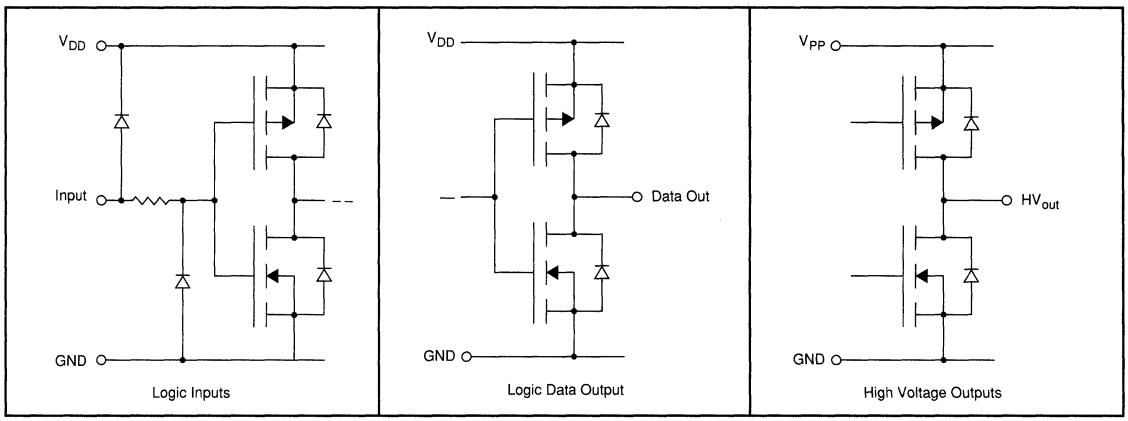
AC Characteristics (V_{DD} = 12V, V_{PP} = 80V)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{SU}	Data input set-up time before CLK		20		ns	
t_H	Data input hold time after CLK		50		ns	
t_{DHL}	Delay time High to low Level outputs	Strobe to HV_{out}		250	ns	C_L = 30pF
		Sustain to HV_{out}		250	ns	C_L = 30pF
		Serial out		147	ns	C_L = 30pF
t_{DLH}	Delay time Low to high Level outputs	Strobe to HV_{out}		450	ns	C_L = 30pF
		Sustain to HV_{out}		450	ns	C_L = 30pF
		Serial out		147	ns	C_L = 30pF
t_R	Rise time low to high HV_{out}			300	ns	C_L = 30pF
t_F	Fall time high to low HV_{out}			200	ns	C_L = 30pF

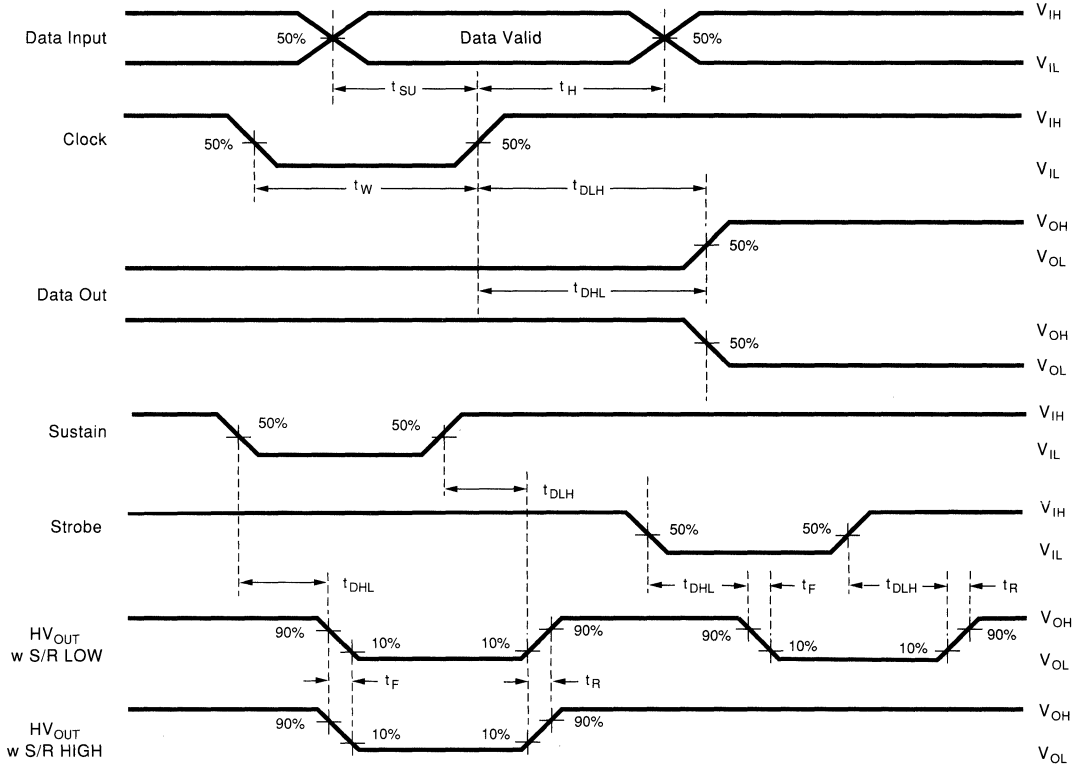
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+80	°C
		Military Hi-Rel (RB)	-55	+125	°C

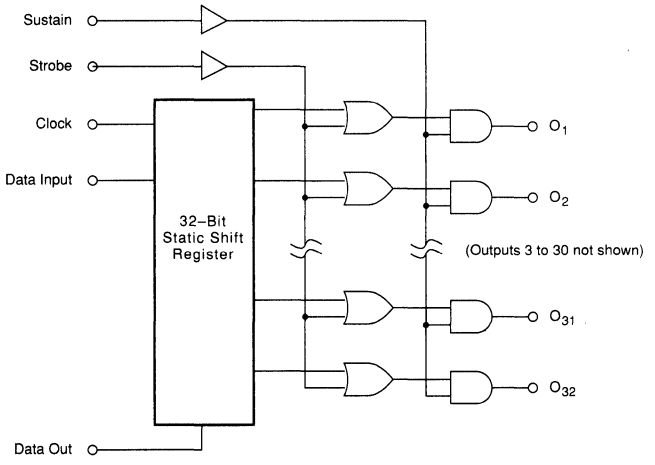
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Shift Register			HV Outputs		
	Data	Clock	Strobe	Sustain	R1	R2	R3...R32	1	2	3...32
Load	H	↑	H	H	H	R1n	R2n...R31n	H	H	H...H
	L	↑	H	H	L	R1n	R2n...R31n	H	H	H...H
Strobe	X	X	H	H	R1n	R2n	R3n...R32n	H	H	H...H
	X	H	L	H	R1n	R2n	R3n...R32n	R1	R2	R3...R32
Sustain	X	X	X	L	R1n	R2n	R3n...R32n	L	L	L...L

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1...R32 = levels currently at internal outputs of shift registers one through 32, respectively.
R1n...R32n = levels at shift-register outputs R1 through R32, respectively, before the most recent ↑ transition of the clock input.

Pin Configurations

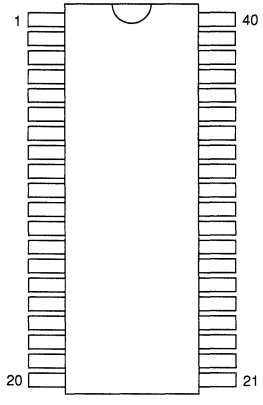
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Clock	21	V_{PP}
2	Sustain	22	HVout 17
3	Strobe	23	HVout 18
4	HVout 1	24	HVout 19
5	HVout 2	25	HVout 20
6	HVout 3	26	HVout 21
7	HVout 4	27	HVout 22
8	HVout 5	28	HVout 23
9	HVout 6	29	HVout 24
10	HVout 7	30	HVout 25
11	HVout 8	31	HVout 26
12	HVout 9	32	HVout 27
13	HVout 10	33	HVout 28
14	HVout 11	34	HVout 29
15	HVout 12	35	HVout 30
16	HVout 13	36	HVout 31
17	HVout 14	37	HVout 32
18	HVout 15	38	Data Out
19	HVout 16	39	Data In
20	GND	40	V_{DD}

44 Pin J-Lead Package

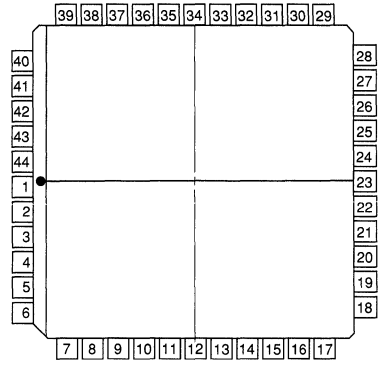
Pin	Function	Pin	Function
1	N/C	23	N/C
2	Clock	24	V_{PP}
3	Sustain	25	HVout 17
4	Strobe	26	HVout 18
5	N/C	27	HVout 19
6	HVout 1	28	HVout 20
7	HVout 2	29	HVout 21
8	HVout 3	30	HVout 22
9	HVout 4	31	HVout 23
10	HVout 5	32	HVout 24
11	HVout 6	33	HVout 25
12	HVout 7	34	HVout 26
13	HVout 8	35	HVout 27
14	HVout 9	36	HVout 28
15	HVout 10	37	HVout 29
16	HVout 11	38	HVout 30
17	HVout 12	39	HVout 31
18	HVout 13	40	HVout 32
19	HVout 14	41	N/C
20	HVout 15	42	Data Out
21	HVout 16	43	Data In
22	GND	44	V_{DD}

Package Outlines



top view

40-pin DIP



top view

44-pin J-lead Package