32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV51	HV5122DJ	HV5122PJ	HV5122X
HV52	HV5222DJ	HV5222PJ	HV5222X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages to 225V using a ramped supply voltage
- ☐ Sink current minimum 100mA
- ☐ Shift register speed 8MHz
- ☐ Strobe and enable inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Replacements for SN75551 (HV5122) and SN75552 (HV5222) Row Drivers
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Output voltage, V_{PP}[2]	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} + 0.5V
Ground currrent[3]	1.5A
Continuous total power dissipation[4]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV51 and HV52 are low voltage serial to high voltage parallel converters wtih open drain outputs. These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the high to low transition of the clock. The HV51 shifts in the counterclockwise direction when viewed from the top of the package and the HV52 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

The HV51 and HV52 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

These devices are pin for pin replacements for the SN75551 and SN75552 devices. In addition, Supertex HVCMOS technology provides significantly higher speed and higher sink current capability in the HV51 and HV52 devices.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				15	mA	f_{CLK} = 8MHz F_{DATA} = 4MHz
I_{DDQ}	Quiescent V_{DD} supply current				0.5	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off state output current				10	µA	All outputs high All SWS parallel
I_{IH}	High-level logic input current				1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current				-1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} - 1.0V			V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}			15.0	V	I_{HVout} = +100mA
		Data out			1.0	V	I_{Dout} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

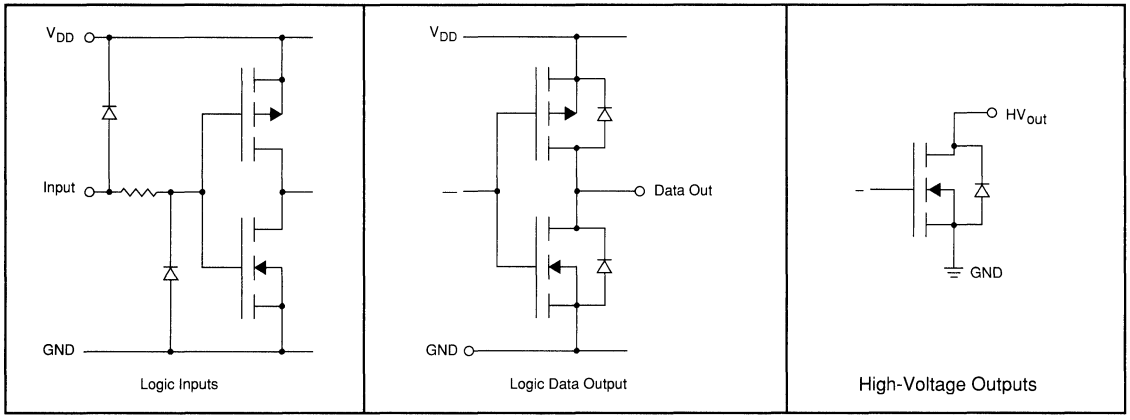
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			8	MHz	
t_W	Clock width high or low	62			ns	
t_{SU}	Data set-up time before clock falls	25			ns	
t_H	Data hold time after clock falls	10			ns	
t_{ON}	Turn ON time, HV_{OUT} from enable			500	ns	R_L = 2KΩ to 200V
t_{DHL}	Delay time clock to data high to low			100	ns	
t_{DLH}	Delay time clock to data low to high			100	ns	

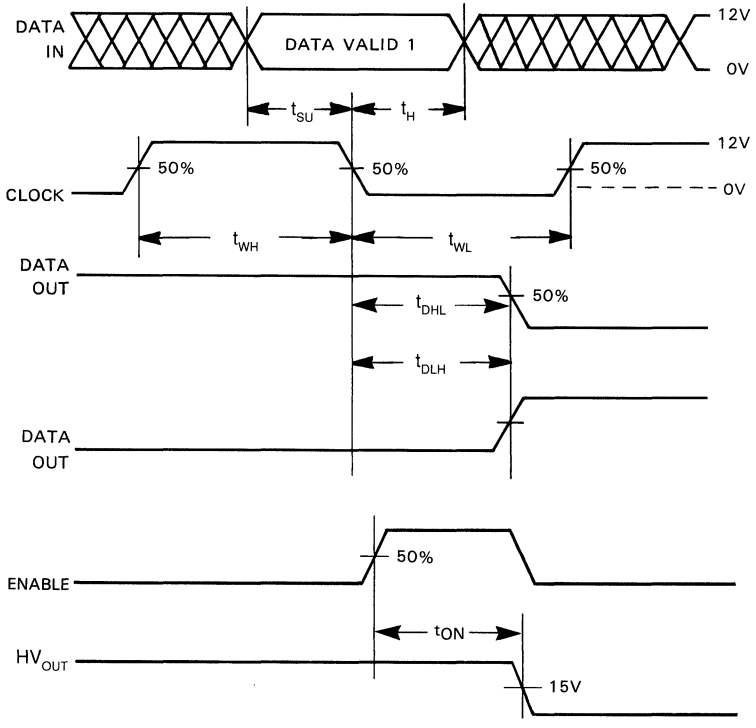
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	15	V
V_{PP}	High voltage supply		-0.3		225	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
f_{CLK}	Clock frequency				8	MHz
T_A	Operating free-air temperature	Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

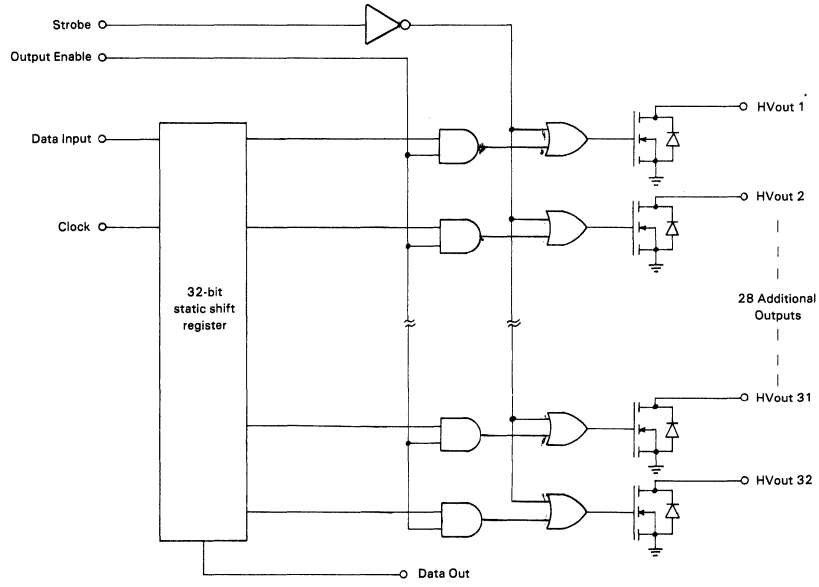
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs		
	DI	CLK	OE	STR	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out *
All on	X	X	X	L	* *...*	L L...L	*
All off	X	X	L	H	* *...*	H H...H	*
Load S/R	H or L	↓	L	H	H or L *...*	H H...H	
Output enable	X	H or L	H	H	H or L *...*	L or H *...*	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK : High to low transition.
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

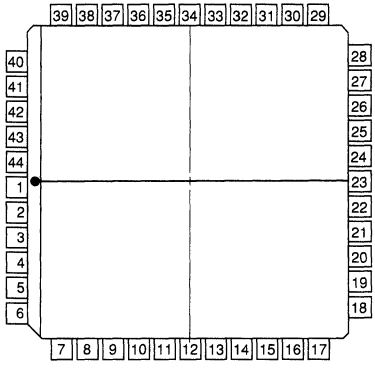
HV51
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Output Enable
2	HVout 17	24	Clock
3	HVout 18	25	GND
4	HVout 19	26	V_{DD}
5	HVout 20	27	Strobe
6	HVout 21	28	Data In
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	N/C	44	HVout 15

HV52
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Output Enable
2	HVout 16	24	Clock
3	HVout 15	25	GND
4	HVout 14	26	V_{DD}
5	HVout 13	27	Strobe
6	HVout 12	28	Data In
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	N/C	44	HVout 18

Package Outline



top view

44-pin J-lead Package