



# HY51V(S)17403HG/HGL 4M x 4Bit EDO DRAM

PRELIMINARY

## DESCRIPTION

The HY51V(S)17403HG/HGL is the new generation dynamic RAM organized 4,194,304 words x 4bit. HY51V(S)17403HG/HGL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The HY51V(S)17403HG/HGL offers Extended Data Out Page-Mode as a high speed access mode. Multiplexed address inputs permit the HY51V(S)17403HG/HGL to be packaged in standard 300mil 24(26)pin SOJ and 24(26) pin TSOP-II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 3.3V +/- 0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

- Extended Data Out Mode capability
- Read-modify-write capability
- Multi-bit parallel test capability
- TTL(3.3V) compatible inputs and outputs
- /RAS only, CAS-before-/RAS, Hidden and self refresh(L-version) capability
- Fast access time and cycle time**
- JEDEC standard pinout
- 24(26)pin plastic SOJ / 24(26)pin TSOP-II
- Single power supply of 3.3V +/- 0.3V
- Battery back up operation(L-version)

Part No	tRAC	tCAC	tRC	tHPC
HY51V(S)17403HG/HGL-5	50ns	13ns	84ns	20ns
HY51V(S)17403HG/HGL-6	60ns	15ns	104ns	25ns
HY51V(S)17403HG/HGL-7	70ns	18ns	124ns	30ns

### Power dissipation

	50ns	60ns	70ns
Active	432mW	369mW	360mW
Standby	7.2mW(CMOS level Max) 0.36mW (L-version : Max)		

### Refresh cycle

Part No	Ref	Normal	L-part
HY51V17403HG	2K	32ms	
HY51V17403HGL	2K		128ms

## ORDERING INFORMATION

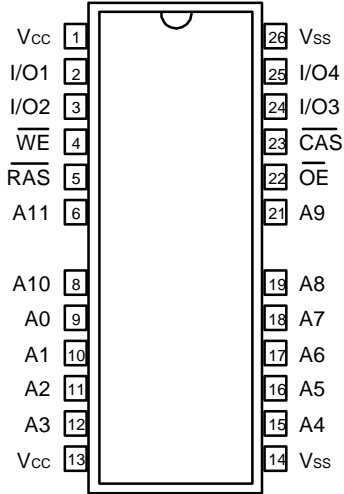
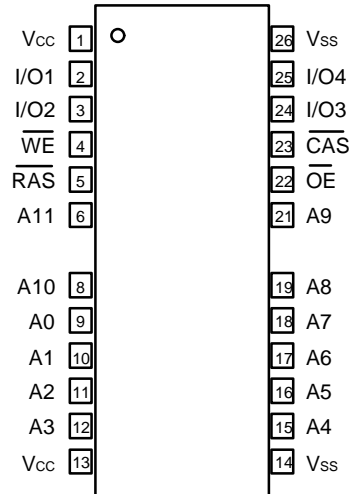
Part Number	Access Time	Package
HY51V(S)17403HGJ/HG(L)J-5 HY51V(S)17403HGJ/HG(L)J-6 HY51V(S)17403HGJ/HG(L)J-7	50ns 60ns 70ns	300mil 24(26)pin SOJ
HY51V(S)17403HGT/HG(L)T-5 HY51V(S)17403HGT/HG(L)T-6 HY51V(S)17403HGT/HG(L)T-7	50ns 60ns 70ns	300mil 24(26)pin TSOP-II

(S) : Self refresh,

(L) : Low power

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**PIN CONFIGURATION**

**24(26) Pin Plastic SOJ**

**24(26) Pin Plastic TSOP-II**
**PIN DESCRIPTION**

Pin	Function
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs
A0-A11	Refresh Address Inputs
I/O 1- I/O 4	Data Input / Output
Vcc	Power (3.3V)
Vss	Ground
NC	No connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to Vss	VT	-0.5 ~ Vcc + 0.5 (Max 4.6V)	V
Voltage on Vcc relative to Vss	Vcc	-0.5 ~ 4.6	V
Short Circuit Output Current	IOUT	50	mA
Power Dissipation	PT	1	W

**Recommended DC OPERATING CONDITIONS** (TA=0 to 70 °C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	-	Vcc + 0.3	V	
Input Low Voltage	VIL	-0.3	-	0.8	V	

**Note :** All voltages are referenced to Vss

**DC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = 0$  to  $70^\circ C$ )

Symbol	Parameter	Min	Max	Unit	Note	
VOH	Output Level Output Level voltage( $I_{out} = -2mA$ )	2.4	$V_{CC}$	V		
VOL	Output Level Output Level voltage( $I_{out} = 2mA$ )	0	0.4	V		
ICC1	Operating current Average power supply operating current ( $/RAS, /CAS$ Cycling : $t_{RC} = t_{RC \min}$ )	50ns	-	100	mA	1, 2
		60ns	-	90		
		70ns	-	80		
ICC2	Standby current (TTL interface) Power supply standby current ( $/RAS, /CAS = V_{IH}$ , $D_{out} = High-Z$ )	-	2	mA		
ICC3	$/RAS$ only refresh current Average power supply current $/RAS$ only refresh mode ( $t_{RC} = t_{RC \min}$ )	50ns	-	100	mA	2
		60ns	-	90		
		70ns	-	80		
ICC4	Fast page mode current Average power supply current Fast page mode ( $t_{PC} = t_{PC \min}$ )	50ns	-	90	mA	1, 3
		60ns	-	80		
		70ns	-	75		
ICC5	CMOS interface ( $/RAS, /CAS \geq V_{CC} - 0.2V$ , $D_{out} = High-Z$ )	-	1	mA		
	Standby current (L-version)	-	100	$\mu A$	4	
ICC6	$/CAS$ -before- $/RAS$ refresh current ( $t_{RC} = t_{RC \min}$ )	50ns	-	100	mA	
		60ns	-	90		
		70ns	-	80		
ICC7	Battery back up operating current (standby with CBR refresh) ( $t_{RC} = 31.3\mu s$ , $t_{RAS} \leq 0.3\mu s$ , $D_{out} = High-Z$ )	-	300	$\mu A$	4	
ICC8	Standby current ( $/RAS = V_{IH}$ , $/CAS = V_{IL}$ , $D_{out} = Enable$ )	-	5	$\mu A$	1	
ICC9	Self refresh current ( $/RAS, /CAS \leq 0.2V$ , $D_{out} = High-Z$ , CMOS interface)	-	200	$\mu A$	4	
II(L)	Input leakage current, Any input ( $0V \leq V_{in} \leq 4.6V$ )	-10	10	$\mu A$		
IO(L)	Output leakage current, ( $D_{out}$ is disabled, $0V \leq V_{out} \leq 4.6V$ )	-10	10	$\mu A$		

**Note :**

1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC(max)}$  is specified at the output open condition
2. Address can be changed once or less while  $/RAS = V_{IL}$
3. Address can be changed once or less while  $/CAS = V_{IH}$
4.  $/CAS = L$  ( $\leq 0.2$ ) while  $/RAS = L$  ( $\leq 0.2$ )
5. L-Version

**CAPACITANCE** ( $V_{CC}=3.3V \pm 10\%$ ,  $T_A=25^\circ C$ )

Parameter	Symbol	Min.	Max	Unit	Note
Input capacitance (Address)	CI1	-	5	pF	1
Input capacitance (Clocks)	CI2	-	7	pF	1
Output capacitance (Data-in, Data-out)	CI/O	-	7	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2. /CAS =  $V_{IH}$  to disable  $D_{out}$

**AC CHARACTERISTICS** ( $V_{CC}=3.3V \pm 10\%$ ,  $T_A=0\sim 70^\circ C$ , Note 1, 2, 18)

**Test Condition**

- Input rise and fall times = 2ns
- Input levels :  $V_{IL}=0V$ ,  $V_{IH}=3V$
- Input timing reference level :  $V_{IL}/V_{IH} = 0.8/2.0V$
- Output timing reference level :  $V_{OL}/V_{OH}=0.8/0.2V$
- Output load : 1 TTL gate + CL (100pF)  
( including scope and jig )

**Read, Write, Read-modify-Write and Refresh Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84	-	104	-	124	-	ns	
/RAS precharge time	tRP	30	-	40	-	50	-	ns	
/CAS precharge time	tCP	8	-	10	-	13	-	ns	
/RAS pulse width	tRAS	50	10,000	60	10,000	70	10,000	ns	
/CAS pulse width	tCAS	8	10,000	10	10,000	13	10,000	ns	
Row address set-up time	tASR	0	-	0	-	0	-	ns	
Row address hold time	tRAH	8	-	10	-	10	-	ns	
Column address set-up time	tASC	0	-	0	-	0	-	ns	
Column address hold time	tCAH	8	-	10	-	13	-	ns	
/RAS to /CAS delay time	tRCD	12	37	14	45	14	52	ns	3
/RAS to Column address delay time	tRAD	10	25	12	30	12	35	ns	4
/RAS hold time	tRSH	10	-	13	-	13	-	ns	
/CAS hold time	tCSH	35	-	40	-	45	-	ns	
/CAS to /RAS precharge time	tCRP	5	-	5	-	5	-	ns	

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Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/OE to Din delay time	tODD	13	-	15	-	18	-	ns	5
/OE delay time from Din	tDZO	0	-	0	-	0	-	ns	6
/CAS delay time from Din	tDZC	0	-	0	-	0	-	ns	6
Transition time ( Rise and Fall)	tT	2	50	2	50	2	50	ns	7
Refresh period	tREF	-	32	-	32	-	32	ms	2K Ref.
Refresh period (L-version)		-	128	-	128	-	128	ms	2K Ref.

## Read Cycle

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from /RAS	tRAC	-	50	-	60	-	70	ns	8,9,19
Access time from /CAS	tCAC	-	13	-	15	-	18	ns	9,10,17,19
Access time from column address	tAA	-	25	-	30	-	35	ns	9,11,17,19
Access time from /OE	tOAC	-	13	-	15	-	18	ns	9
Read command set-up time	tRCS	0	-	0	-	0	-	ns	
Read command hold time to /CAS	tRCH	0	-	0	-	0	-	ns	12
Read command hold time from /RAS	tRCHR	50	-	60	-	70	-	ns	
Read command hold time to /RAS	tRRH	5	-	5	-	5	-	ns	12
Column address to /RAS lead time	tRAL	25	-	30	-	35	-	ns	
Column address to /CAS lead time	tCAL	15	-	18	-	23	-	ns	
/CAS to output in low-Z	tCLZ	0	-	0	-	0	-	ns	
Output data hold time	tOH	3	-	3	-	3	-	ns	
Output data hold time from /OE	tOHO	3	-	3	-	3	-	ns	
Output buffer turn off time to /OE	tOEZ	-	13	-	15	-	15	ns	13
Output buffer turn off time	tOFF	-	13	-	15	-	15	ns	13
/CAS to Din delay time	tCDD	13	-	15	-	18	-	ns	5
Output data hold time from /RAS	tOHR	3	-	3	-	3	-	ns	
Output buffer turn-off time to /RAS	tOFR	-	13	-	15	-	15	ns	
Output buffer turn off time to /WE	tWEZ	-	13	-	15	-	15	ns	
/WE to DIN delay time	tWDD	13	-	15	-	18	-	ns	
/RAS to DIN delay time	tRDD	13	-	15	-	18	-	ns	

**Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command set-up time	tWCS	0	-	0	-	0	-	ns	14
Write command hold time	tWCH	8	-	10	-	13	-	ns	
Write command pulse width	tWP	8	-	10	-	10	-	ns	
Write command to /RAS lead time	tRWL	8	-	10	-	13	-	ns	
Write command to /CAS lead time	tCWL	8	-	10	-	13	-	ns	
Data-in set-up time	tDS	0	-	0	-	0	-	ns	15
Data-in hold time	tDH	8	-	10	-	13	-	ns	15

**Read-Modify-Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	111	-	136	-	161	-	ns	
/RAS to /WE delay time	tRWD	67	-	79	-	92	-	ns	14
/CAS to /WE delay time	tCWD	30	-	34	-	40	-	ns	14
Column address to /WE delay time	tAWD	42	-	49	-	57	-	ns	14
/OE hold time from /WE	tOEH	13	-	15	-	18	-	ns	

**Refresh cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/CAS set-up time ( /CAS-before-/RAS Refresh Cycle)	tCSR	5	-	5	-	5	-	ns	
/CAS hold time ( /CAS-before-/RAS Refresh Cycle)	tCHR	8	-	10	-	10	-	ns	
/WE setup time ( /CAS-before-/RAS Refresh Cycle)	tWRP	0	-	0	-	0	-	ns	
/WE hold time ( /CAS-before-/RAS Refresh Cycle)	tWRH	10	-	10	-	10	-	ns	
/RAS precharge to /CAS hold time ( /CAS-before-/RAS Refresh Cycle)	tRPC	5	-	5	-	5	-	ns	

**EDO Page Mode Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO mode cycle time	tHPC	20	-	25	-	30	-	ns	20
EDO mode /RAS pulse width	tRASP	-	100K	-	100K	-	100K	ns	16
Access time from /CAS precharge	tACP	-	30	-	35	-	40	ns	9,17,19
/RAS hold time from /CAS precharge	tRHCP	30	-	35	-	40	-	ns	
Output data hold time from /CAS low	tDOH	3	-	3	-	3	-	ns	9
/CAS hold time referred /OE	tCOL	8	-	10	-	13	-	ns	
/CAS to /OE setup time	tCOP	5	-	5	-	5	-	ns	
Read command hold time from /CAS precharge	tRHCP	30	-	35	-	40	-	ns	

**EDO Page Mode Read-Modify-Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO Page read-modify-write cycle time	tHPRWC	57	-	68	-	79	-	ns	
EDO mode read-modify-write cycle /CAS precharge to /WE delay time	tCPW	45	-	54	-	62	-	ns	14

**TEST Mode cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test mode /WE setup time	tWTS	0	-	0	-	0	-	ns	
Test mode /WE hold time	tWTH	10	-	10	-	10	-	ns	

**Self Refresh Mode(L-version)**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/RAS pulse width (self refresh)	tRASS	100	-	100	-	100	-	us	
/RAS precharge time(self refresh)	tRPS	90	-	110	-	130	-	ns	
/CAS hold time(self refresh)	tCHS	-50	-	-50	-	-50	-	ns	



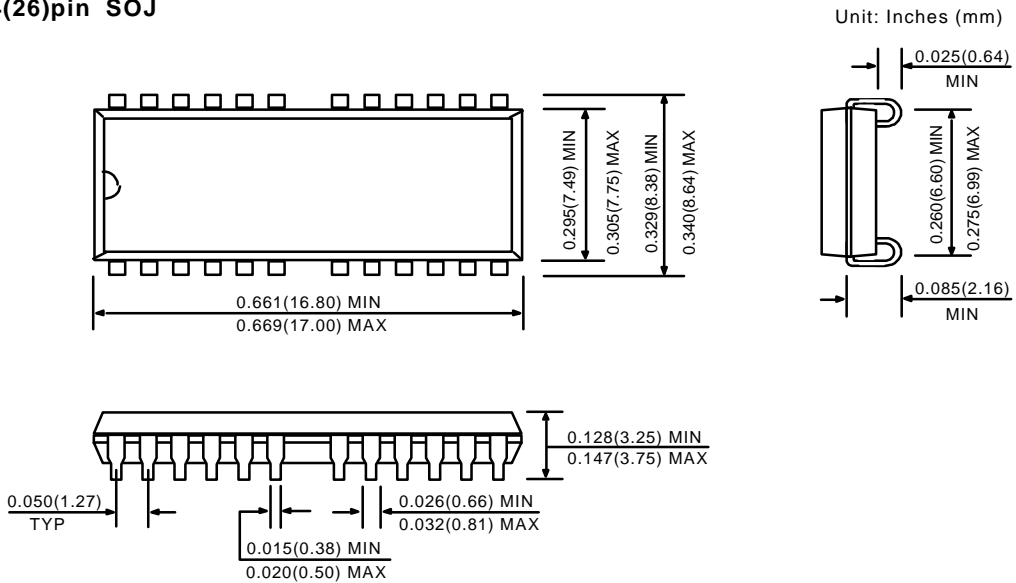
**Notes :**

1. AC measurements assume  $t_T = 2\text{ns}$
2. AC initial pause of 200us is required after power up followed by a minimum of eight initialization cycles ( any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh)  
If the internal refresh counter is used, a minimum of eight /CAS-before-/RAS refresh cycle are required.
3. Operation with the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only : if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
4. Operation with the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only : if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
5. Either  $t_{\text{ODD}}$  or  $t_{\text{CDD}}$  must be satisfied.
6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
7.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals, also transition times are measured between  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$
8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown
9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.(  $V_{\text{OH}}=2.0\text{V}$ ,  $V_{\text{OL}}=0.8\text{V}$ )
10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$
11. Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles
13.  $t_{\text{OFF}}(\text{max})$ ,  $t_{\text{OEZ}}(\text{max})$ ,  $t_{\text{OFR}}(\text{max})$  and  $t_{\text{WEZ}}(\text{max})$  define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle :  
If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles
16.  $t_{\text{RASP}}$  defines /RAS pulse width in EDO page mode cycles

17. Access time is determined by the longest among  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$
18. The 16M DRAM offers 16 bit time saving parallel test mode. Address CA0 and CA1 for the 4Mx4 are don't care during test mode. Test mode is set by performing a /WE-and-/CAS-before-/RAS(WCBR) cycle. In 16bit parallel test mode, data is written into 4 bits in parallel at each I/O(I/O 1 to I/O4) and read out from each I/O. If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, Data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular /CAS-before-/RAS refresh cycle or /RAS-only refresh cycle.
19. In a test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$  is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet
20.  $t_{HPC}(\min)$  can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode /RAS cycle(EDO page mode mix cycle (1)(2)), minimum value of /CAS cycle( $t_{CAS}+t_{CP}+2t_T$ ) becomes greater than the specified  $t_{HPC}(\min)$  value. The value of /CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2)

## PACKAGE INFORMATION

### 24(26)pin SOJ



### 24(26)pin TSOP-II

