

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV55	300V	HV5530DJ	HV5530PJ	HV5530X
	220V	HV5522DJ	HV5522PJ	HV5522X
HV56	300V	HV5630DJ	HV5630PJ	HV5630X
	220V	HV5622DJ	HV5622PJ	HV5622X

Features

- Processed with HVCOS[®] technology
- Output voltages up to 300V using a ramped supply voltage
- Sink current minimum 100mA
- Shift register speed 8MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to VPP allows efficient power recovery
- 44-lead ceramic surface mount package
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD} ¹	-0.5V to +18V
Output voltage, V_{PP} ¹	HV5530/HV5630 -0.5V to +315V HV5522/HV5622 -0.5V to +220V
Logic input levels ¹	-0.5V to $V_{DD} + 0.5V$
Ground current ²	1.5A
Continuous total power dissipation ³	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

- Notes: 1. All voltages are referenced to V_{SS}
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV55 and HV56 are low-voltage serial to high-voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV55 shifts in the counterclockwise direction when viewed from the top of the package, and the HV56 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} (latch enable) input is high. The data in the latch is stored when \overline{LE} is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		15	mA	$f_{CLK} = 8\text{MHz}$ $F_{DATA} = 4\text{MHz}$
I_{DDQ}	Quiescent V_{DD} supply current		0.05	mA	$V_{IN} = 0\text{V}$
$I_{O(OFF)}$	Off state output current		10	μA	All outputs high All SWS parallel
I_{IH}	High-level logic input current		1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-1	μA	$V_{IL} = 0\text{V}$
V_{OH}	High-level output data out	$V_{DD} - 1.0\text{V}$		V	$I_{Dout} = -100\mu\text{A}$
V_{OL}	Low-level output voltage	HV _{OUT}	15.0	V	$I_{HVout} = +100\text{mA}$
		Data out		V	$I_{Dout} = +100\mu\text{A}$
V_{OC}	HV _{OUT} clamp voltage		-1.5	V	$I_{OL} = -100\text{mA}$

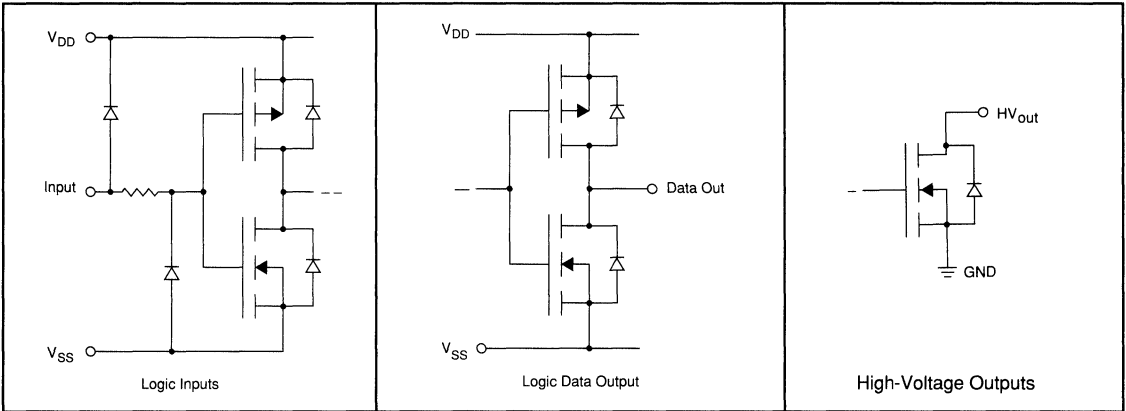
AC Characteristics ($V_{DD} = 12\text{V}$, $T_C = 25^\circ\text{C}$)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock falls	25		ns	
t_H	Data hold time after clock falls	10		ns	
t_{ON}	Turn on time, HV _{OUT} from enable		500	ns	$R_L = 2\text{K}\Omega$ to V_{PP} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	$C_L = 15\text{pF}$
t_{DLH}	Delay time clock to data low to high		100	ns	$C_L = 15\text{pF}$
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

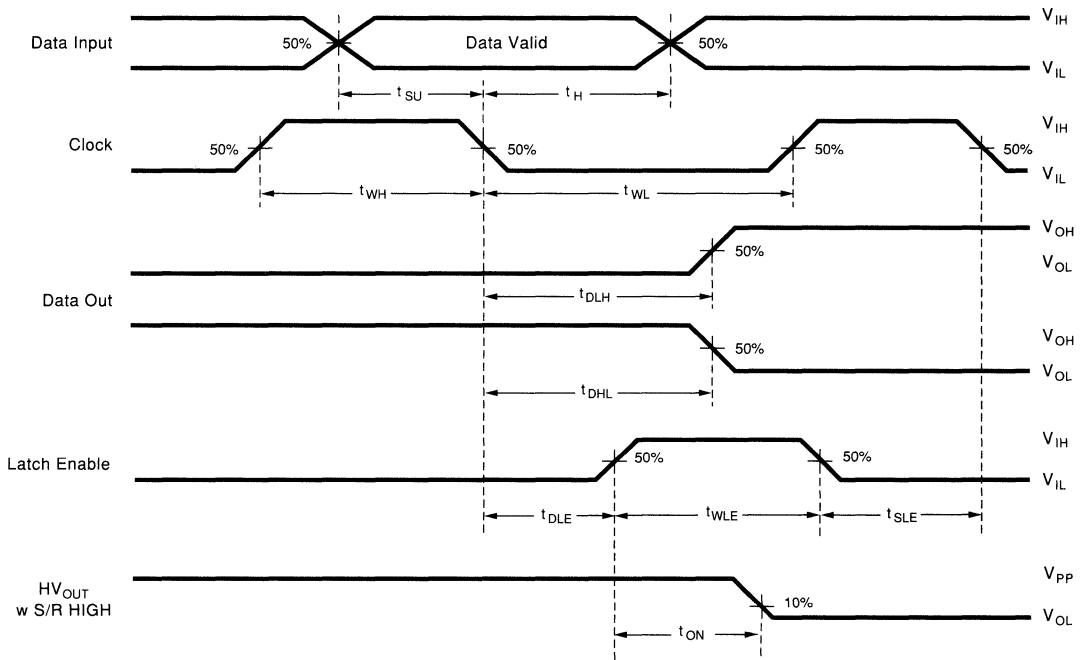
Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	10.8	15	V
V_{PP}	High voltage supply	HV5530 and HV5630	-0.3	+300
		HV5522 and HV5622	-0.3	+200
V_{IH}	High-level input voltage	$V_{DD} - 2\text{V}$	V_{DD}	V
V_{IL}	Low-level input voltage	0	2.0	V
f_{CLK}	Clock frequency		8	MHz
T_A	Operating free-air temperature	Commercial	0	+70
		Military Hi-Rel (RB)	-55	+125

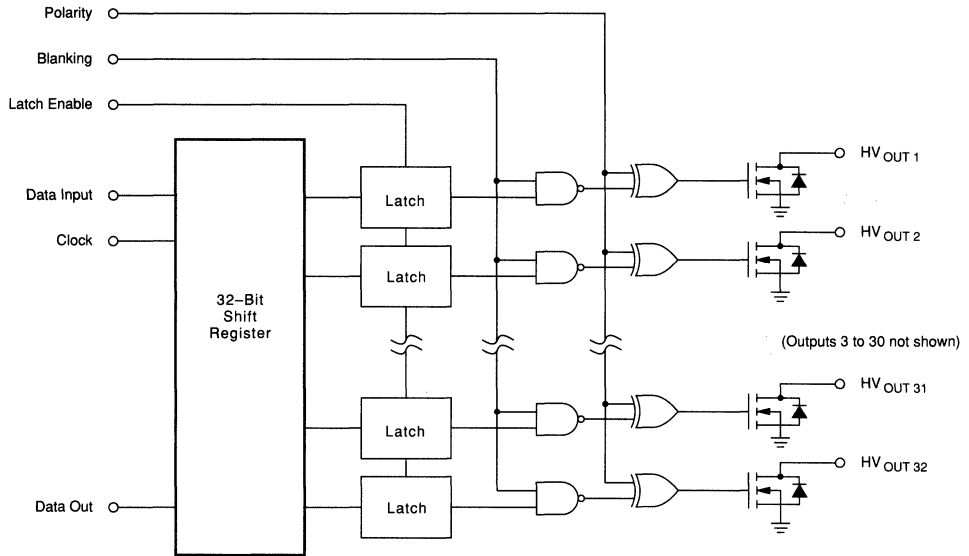
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs		
	Data	CLK	\overline{LE}	\overline{BL}	\overline{POL}	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out
All on	X	X	X	L	L	* *...*	On On...On	*
All off	X	X	X	L	H	* *...*	Off Off...Off	*
Invert mode	X	X	L	H	L	* *...*	* *...*	*
Load S/R	H or L	↓	L	H	H	H or L *...*	* *...*	*
Load Latches	X	H or L	↑	H	H	* *...*	* *...*	*
	X	H or L	↑	H	L	* *...*	* *...*	*
Transparent Latch mode	L	↓	H	H	H	L *...*	Off *...*	*
	H	↓	H	H	H	H *...*	On *...*	*

Notes:

H = high level, L = low level, X = irrelevant, ↓ = low-to-high transition.

* = dependent on previous stage's state before the last CLK ↓ or last LE high.

Pin Configurations

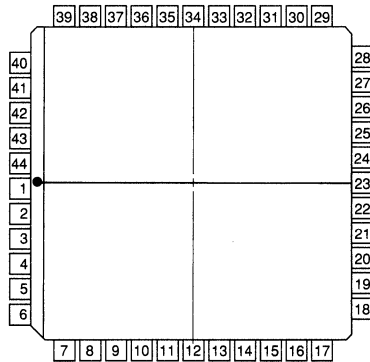
HV55 44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	Clock
2	HVout 17	24	V _{SS}
3	HVout 18	25	V _{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Blanking
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	Polarity	44	HVout 15

HV56 44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	Clock
2	HVout 16	24	V _{SS}
3	HVout 15	25	V _{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Blanking
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	Polarity	44	HVout 18

Package Outline



top view

44-pin J-lead Package