32-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV57	HV5708DJ	HV5708PJ	HV5708X
HV58	HV5808DJ	HV5808PJ	HV5808X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Output voltage, V_{PP}	-0.5V to +80V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV57 and HV58 are low-voltage serial to high-voltage parallel converters wtih push-pull outputs.These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic high to low transition of the clock. The HV57 shifts data in the rclockwise direction when viewed from the top of the package and the HV58 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			0.5	mA	Outputs high
				0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	Q	52		V	I_O= -20mA
		Data out	10.5		V	I_O= -100µA
V_{OL}	Low-level output	Q		8	V	I_O= 20mA
		Data out		1	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

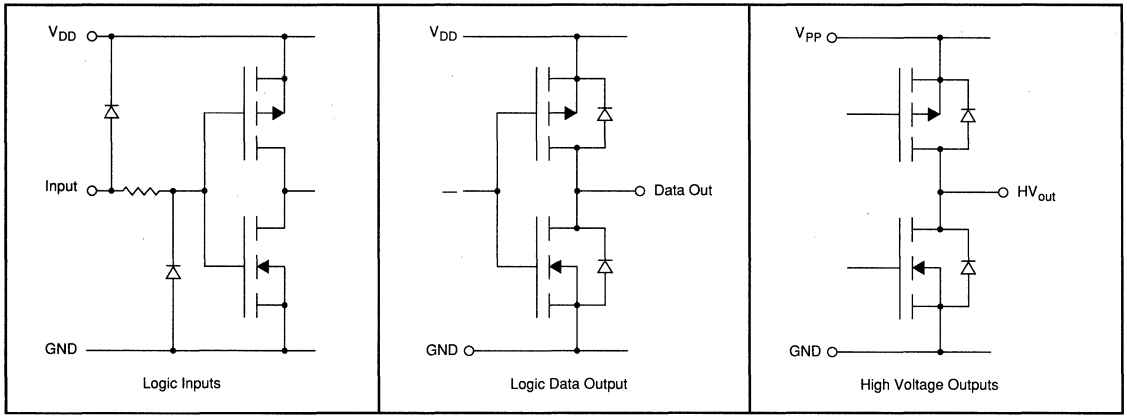
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50		ns	

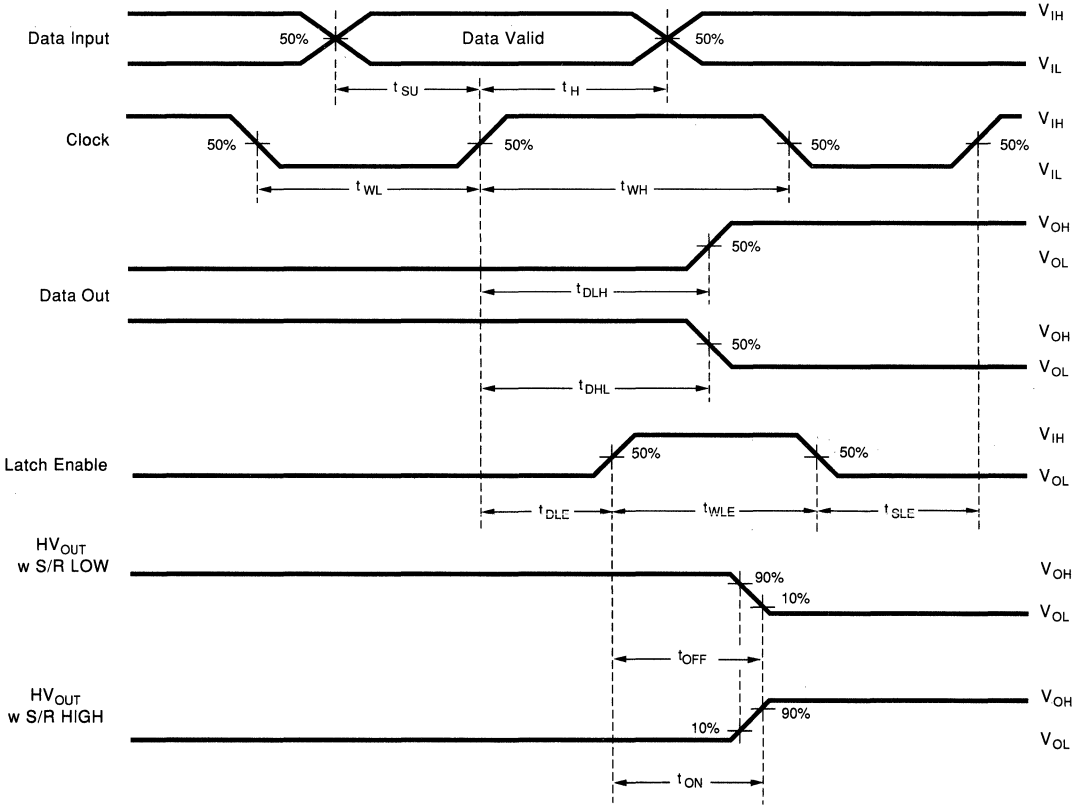
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	15	V
V_{PP}	Output off voltage		-0.3	75	V
V_{IH}	High-level input voltage		V_{DD} - 2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

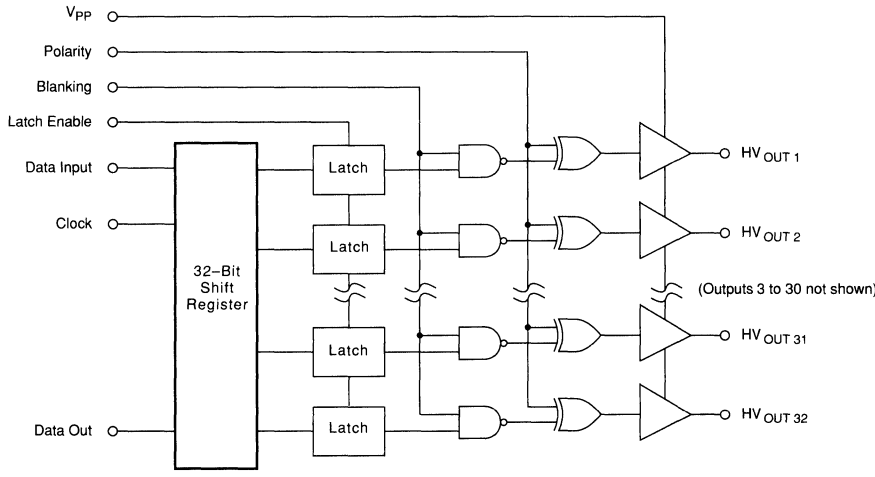
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	*...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high,

Pin Configurations

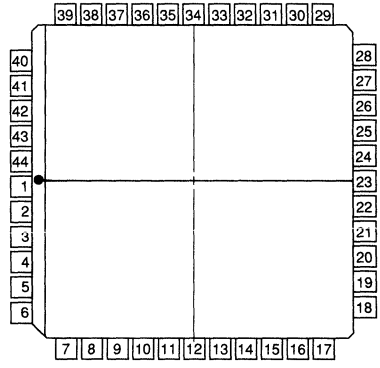
HV53
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	GND
2	HVout 16	24	V_{PP}
3	HVout 15	25	V_{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Blanking
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	Polarity	43	HVout 19
22	Clock	44	HVout 18

HV58
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 16	23	GND
2	HVout 17	24	V_{PP}
3	HVout 18	25	V_{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Blanking
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	$\overline{\text{Polarity}}$	43	HVout 14
22	Clock	44	HVout 15

Package Outline



top view

44-pin J-lead Package