Advance Information

96-Channel AC Plasma Display Data Driver with High Voltage Push-Pull Outputs

Features

- ❑ HVCMOS© technology
- ❑ Operating output voltage of 90V
- ❑ Data clock speed 30MHz @ V_{DD}=5V
- ❑ Six interleaved inputs and outputs
- ❑ Data directional loading control
- ❑ Outputs: enable, polarity, all Hi, all Lo
- ❑ CMOS compatible inputs

Application

- ❑ AC plasma display data column driver

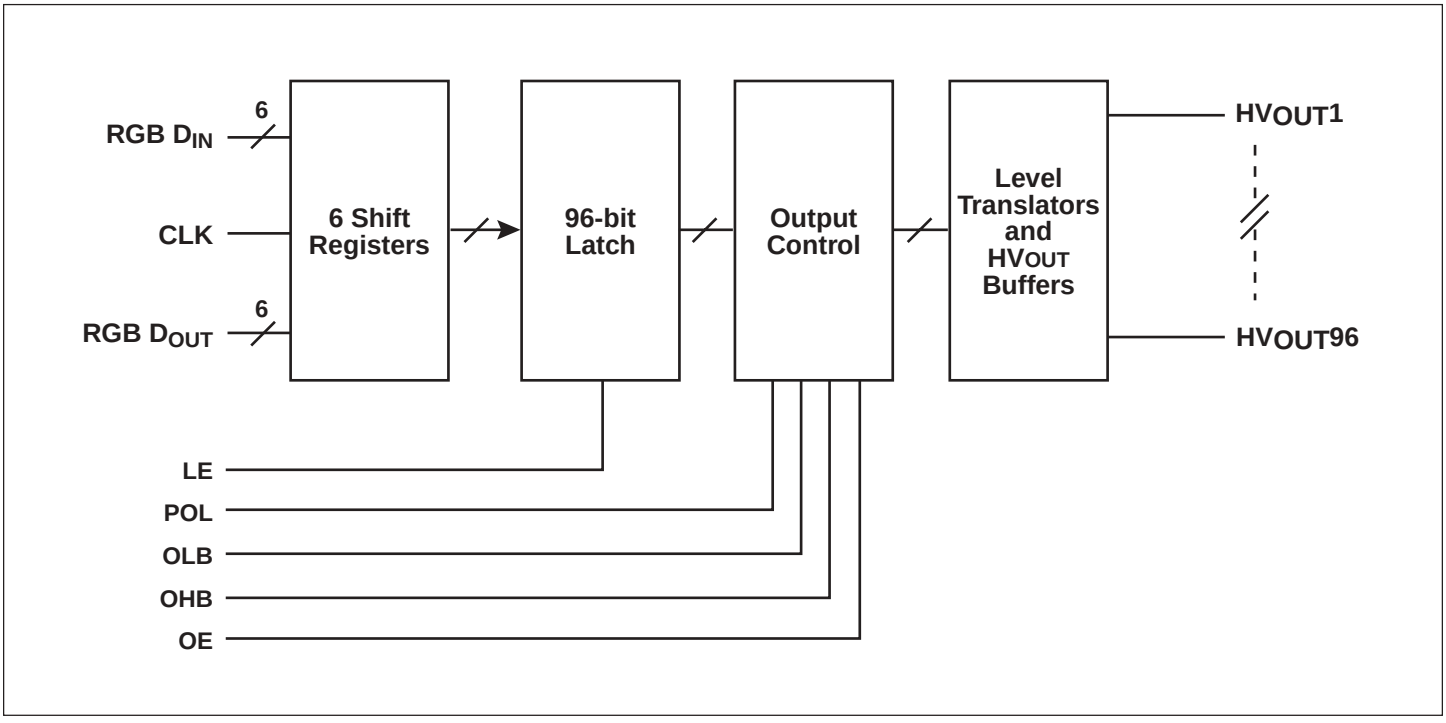
General Description

The HV582 is a low voltage to high voltage converter with 96 high voltage push-pull outputs. This device has been designed to operate as a data driver for AC plasma display panels.

The device is loaded at up to 30MHz using six parallel data inputs, achieving an effective 180MHz data load rate. A direction pin (DIR) is provided to control the data load sequence. Once data is latched into the output latches, the outputs will be controlled based on the latch contents, polarity (POL) pin and output enable (OE) pin inputs. All outputs may be temporarily forced high by asserting a 'low' on the OHB input. Alternatively, all outputs may be temporarily forced low by asserting a 'low' on the OLB input. This versatility allows the outputs to be individually controlled, all set high or low, or all set to a high-Z state.

Circuitry assures a break-before-make interval when switching the output transistors, preventing output cross-conduction, thereby increasing power efficiency.

Functional Block Diagram



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Absolute Maximum Ratings*

Supply Voltage, V_{DD}	-0.5V to 6V
Supply Voltage, V_{PP}	V_{DD} to 100V
Logic input levels	-0.5V to V_{DD}+0.5V
Ground current	TBD A
High voltage supply current	TBD A
Continuous total power dissipation	TBD mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C +150°C

* All voltages are referenced to device ground.

Notes:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Ordering Info

Device	Recommended Operating V_{PP} Max	Package Options
		Die
HV582	90V	HV582X

* Contact Factory

DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				25	mA	f_{CLK}=30MHz, LE*=LOW
I_{DDQ}	Quiescent V_{DD} supply current				100	µA	All V_{IN}=0V or V_{DD}
I_{PP}	High voltage supply current				TBD	mA	V_{PP}=90V, all outputs high
					TBD		V_{PP}=90V, all outputs low
I_{IH}	High-level logic input current				1.0	µA	V_{IH}=V_{DD}
I_{IL}	Low-level logic input current				-1.0	µA	V_{IL}=0V
R_{IN}	Pull-down resistance (DIR, POL, [not]OE, OH, OL)						
V_{OH}	High-level output	HV_{OUT}	V_{PP-10}			V	V_{PP} =90V, I_{HVOUT}=-75mA
		Data out	V_{DD-1}				I_{DOUT}=-4.0mA
V_{OL}	Low-level output	HV_{OUT}			10	V	VDD =5.0V, IHVOUT=75mA
		Data out			1.0		I_{DOUT}=-4.0mA
V_{OC}	HV_{OUT} clamp voltage					V	I_{OH}=75mA
							I_{OL}=-75mA
I_{OH}	Output source current		100			mA	V_{PP}=100V

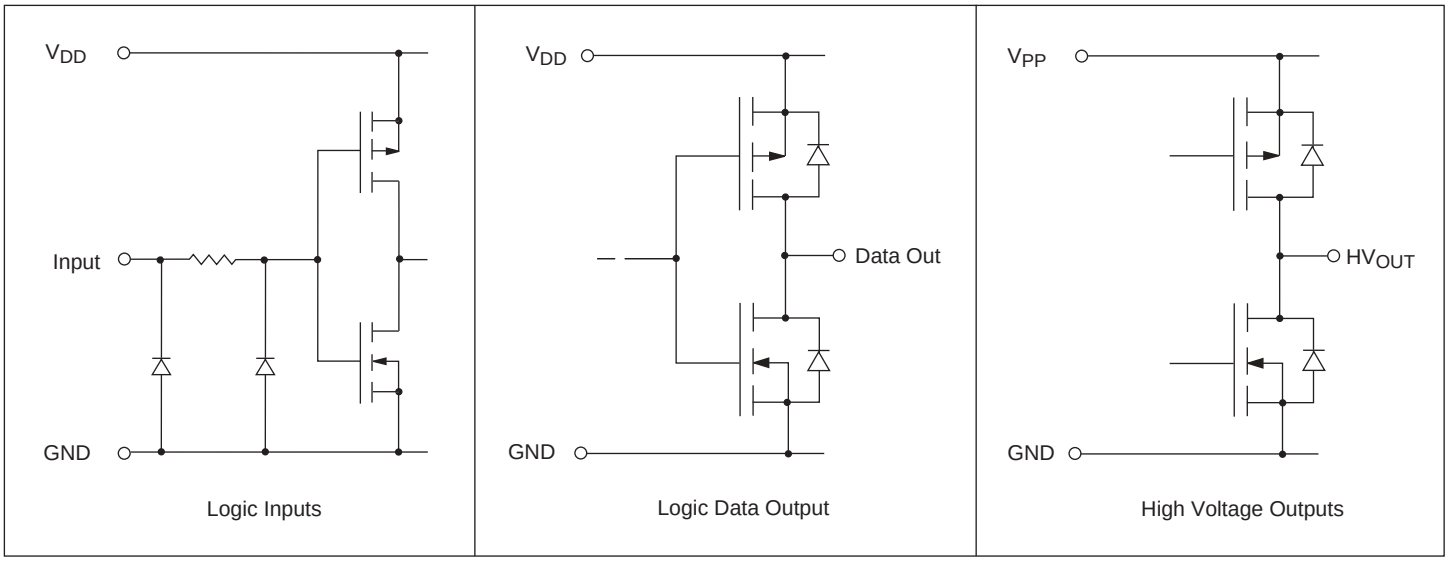
AC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			30	MHz	
t_W	Clock width high and low	16.5			ns	
t_{SU}	Data setup time before clock rises	5.0			ns	
t_H	Data hold time after clock rises	15			ns	
t_{DO}	Delay time for Data Out			25	ns	C_L=20pF
t_{WLE}	Width of latch enable pulse	15			ns	
t_{DLE}	LE delay time after rising edge of clock	15			ns	
t_{SLE}	LE setup time before rising edge of clock	15			ns	
t_D	Delay time for output to start rise/fall			TBD	ns	
t_R	Output rise time, 10% to 90%			200	ns	C_L=170pF, V_{PP}=80V
t_F	Output fall time, 90% to 10%			200	ns	C_L=170pF, V_{DD}=4.5V
t_{DPOL}	Delay time for 10% output change from POL			TBD	ns	
t_{DHIZ}	Delay time for 10% output change from HI-Z			TBD	ns	
	Logic input rise/fall time			5.0	ns	

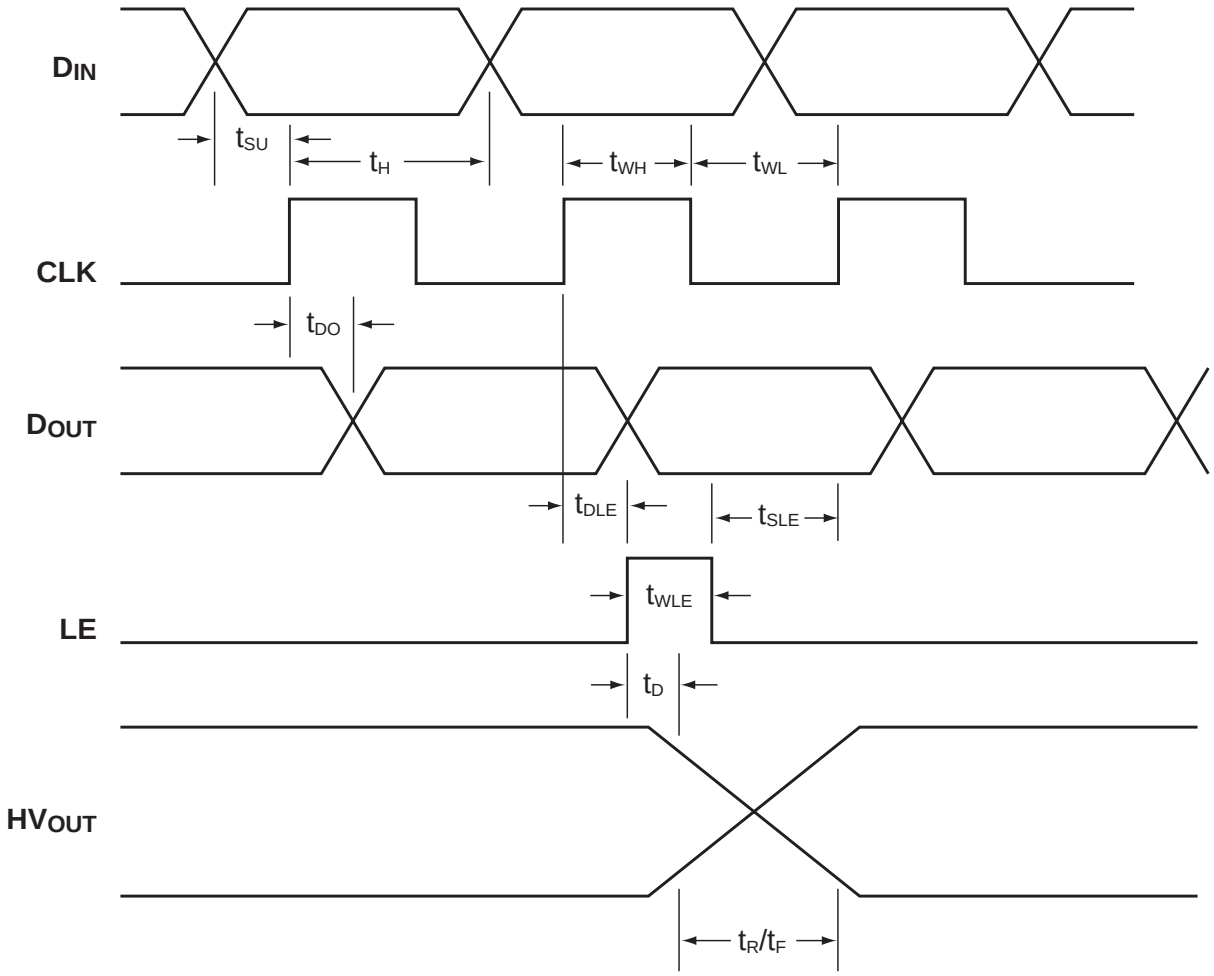
Operating Supply Voltages

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage, V_{DD}	4.5	5.0	5.5	V
V_{PP}	High voltage supply, V_{PP}	60		90	V
V_{IH}	High-level input voltage	V_{DD} – 0.9		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.9	V
T_A	Operating free-air temperature	-40		+85	° C

Input and Output Equivalent Circuits

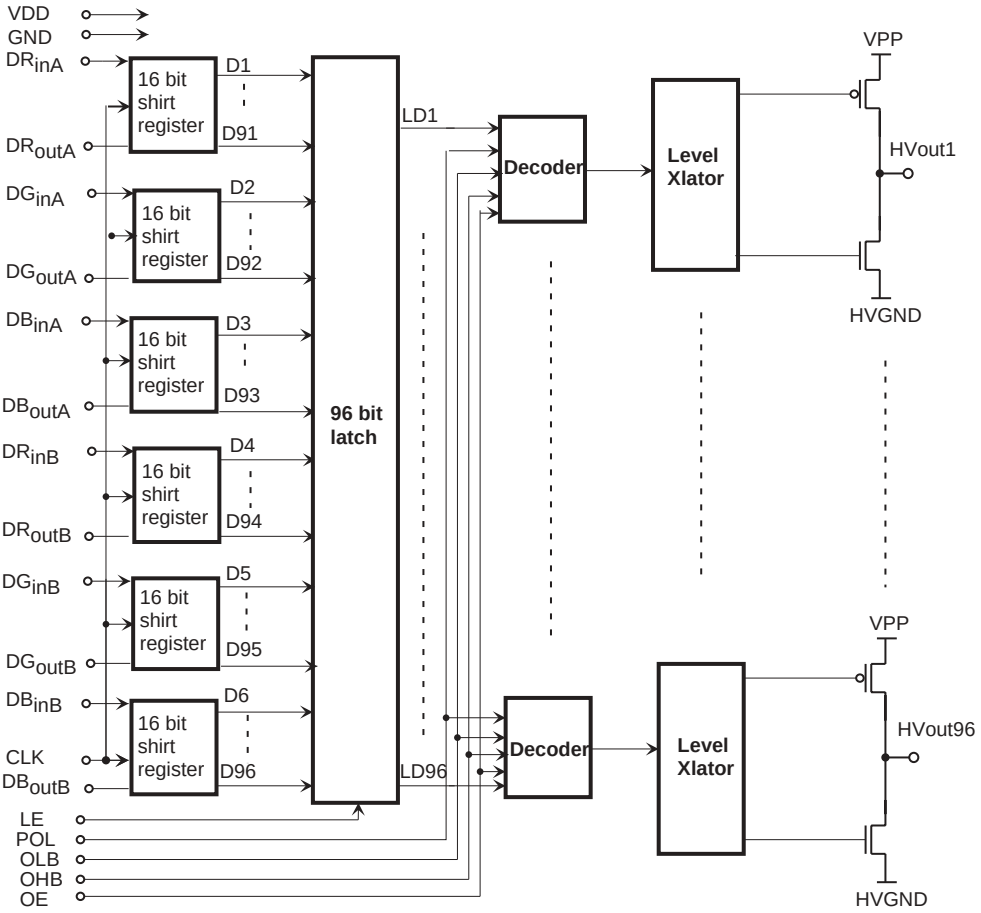


Switching Waveforms



Note: Waveform levels are arbitrary and subject to change.

Functional Block Diagram



Function Table

Function	Input							Outputs		
	Data	CLK	LE	OE	POL	OLB	OHB	Shift Reg 1 2...16	HV Outputs 1 2...6	Data Out
All low	X	X	X	H	X	L	X	* *…*	L L…L	*
All high	X	X	X	H	X	H	L	* *…*	H H…H	*
Outputs Hi-Z	X	X	X	L	X	X	X	* *…*	Z Z…Z	*
Invert mode	X	X	L	H	H	H	H	* *…*	* *…* (b)	*
Load S/R	H or L	↑	L	H	L	H	H	H or L *…*	* *…*	*
Store Data in latches	X	X	↑	H	L	H	H	* *…*	* *…*	*
	X	X	↑	H	H	H	H	* *…*	* *…* (b)	*
Transparent Mode	L	↑	H	H	L	H	H	L *…*	L *…*	*
	H	↑	H	H	L	H	H	H *…*	H *…*	*

DIR is direction control: L shifts in CCW direction, $Q_N \rightarrow Q_{N-1}$; H shifts in CW direction, $Q_N \rightarrow Q_{N+1}$

Notes:

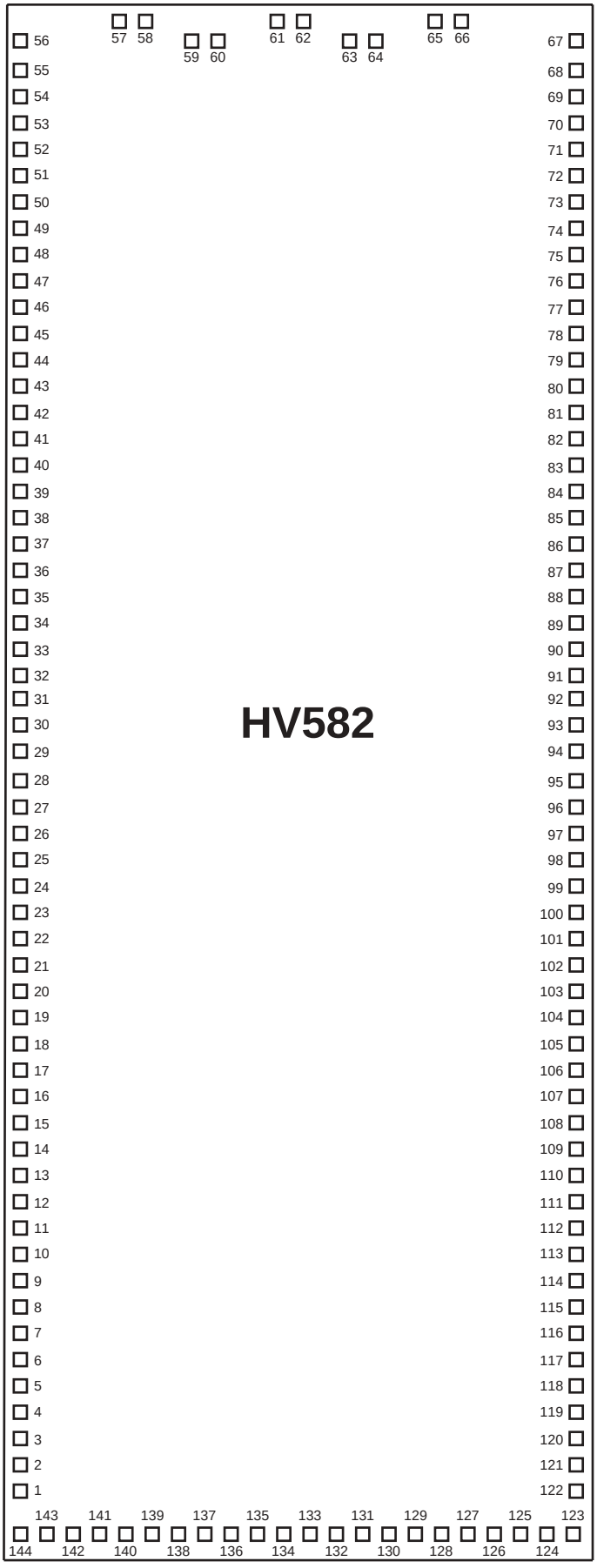
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, (b) indicates inversion

* = dependent on previous stage's state before the last CLK or last LE high.

Pad Coordinates

Pin	Function	Coord
1	VDD	-2052, -3892
2	HVGND	-2052, -3692
3	HVGND	-2052, -3492
4	VPP	-2051, -3293
5	VPP	-2051, -3093
6	VPP	-2051, -2893
7	HVOUT96	-2066, -2705
8	HVOUT95	-2066, -2570
9	HVOUT94	-2066, -2435
10	HVOUT93	-2066, -2300
11	HVOUT92	-2066, -2165
12	HVOUT91	-2066, -2030
13	HVOUT90	-2066, -1895
14	HVOUT89	-2066, -1760
15	HVOUT88	-2066, -1625
16	HVOUT87	-2066, -1490
17	HVOUT86	-2066, -1355
18	HVOUT85	-2066, -1220
19	HVOUT84	-2066, -1085
20	HVOUT83	-2066, -950
21	HVOUT82	-2066, -815
22	HVOUT81	-2066, -680
23	HVOUT80	-2066, -545
24	HVOUT79	-2066, -410
25	HVOUT78	-2066, -275
26	HVOUT77	-2066, -140
27	HVOUT76	-2066, -5
28	HVOUT75	-2066, +130
29	HVOUT74	-2066, +265
30	HVOUT73	-2066, +400
31	HVOUT72	-2066, +535
32	HVOUT71	-2066, +670
33	HVOUT70	-2066, +805
34	HVOUT69	-2066, +940
35	HVOUT68	-2066, +1075
36	HVOUT67	-2066, +1210
37	HVOUT66	-2066, +1345
38	HVOUT65	-2066, +1480
39	HVOUT64	-2066, +1615
40	HVOUT63	-2066, +1750
41	HVOUT62	-2066, +1885
42	HVOUT61	-2066, +2020
43	HVOUT60	-2066, +2155
44	HVOUT59	-2066, +2290
45	HVOUT58	-2066, +2425
46	HVOUT57	-2066, +2560
47	HVOUT56	-2066, +2695
48	HVOUT55	-2066, +2830
49	HVOUT54	-2066, +2965
50	HVOUT53	-2066, +3100
51	HVOUT52	-2066, +3235
52	HVOUT51	-2066, +3370
53	HVOUT50	-2066, +3505
54	HVOUT49	-2066, +3640
55	VPP	-2052, +3828
56	VPP	-2052, +4028
57	VPP	-1728, +4028
58	VPP	-1403, +4028
59	HVGND	-832, +3884
60	HVGND	-632, +3884
61	HVGND	-79, +3884
62	HVGND	+121, +3884
63	HVGND	+686, +3884
64	HVGND	+886, +3884
65	VPP	+1457, +4028
66	VPP	+1782, +4028
67	VPP	+2106, +4028
68	VPP	+2106, +3828
69	HVOUT48	+2121, +3640
70	HVOUT47	+2121, +3505
71	HVOUT46	+2121, +3370
72	HVOUT45	+2121, +3235
73	HVOUT44	+2121, +3100
74	HVOUT43	+2121, +2965
75	HVOUT42	+2121, +2830
76	HVOUT41	+2121, +2695
77	HVOUT40	+2121, +2560
78	HVOUT39	+2121, +2425
79	HVOUT38	+2121, +2290
80	HVOUT37	+2121, +2155
81	HVOUT36	+2121, +2020
82	HVOUT35	+2121, +1885
83	HVOUT34	+2121, +1750
84	HVOUT33	+2121, +1615
85	HVOUT32	+2121, +1480
86	HVOUT31	+2121, +1345
87	HVOUT30	+2121, +1210
88	HVOUT29	+2121, +1075
89	HVOUT28	+2121, +940
90	HVOUT27	+2121, +805
91	HVOUT26	+2121, +670
92	HVOUT25	+2121, +535
93	HVOUT24	+2121, +400
94	HVOUT23	+2121, +265
95	HVOUT22	+2121, +130
96	HVOUT21	+2121, -5
97	HVOUT20	+2121, -140
98	HVOUT19	+2121, -275
99	HVOUT18	+2121, -410
100	HVOUT17	+2121, -545
101	HVOUT16	+2121, -680
102	HVOUT15	+2121, -815
103	HVOUT14	+2121, -950
104	HVOUT13	+2121, -1085
105	HVOUT12	+2121, -1220
106	HVOUT11	+2121, -1355
107	HVOUT10	+2121, -1490
108	HVOUT09	+2121, -1625
109	HVOUT08	+2121, -1760
110	HVOUT07	+2121, -1895
111	HVOUT06	+2121, -2030
112	HVOUT05	+2121, -2165
113	HVOUT04	+2121, -2300
114	HVOUT03	+2121, -2435
115	HVOUT02	+2121, -2570
116	HVOUT01	+2121, -2705
117	VPP	+2106, -2893
118	VPP	+2106, -3093
119	VPP	+2106, -3293
120	HVGND	+2106, -3492
121	HVGND	+2106, -3692
122	GND	+2106, -3892
123	DRINA	+1650, -4087
124	DGINA	+1505, -4087
125	DBINA	+1360, -4087
126	DRINB	+1215, -4087
127	DGINB	+1070, -4087
128	DBINB	+925, -4087
129	CLK	+780, -4087
130	LE	+635, -4087
131	RESET	+490, -4087
132	GND	+300, -4086
133	DIR	+110, -4085
134	VDD	-80, -4086
135	OHB	-270, -4087
136	OLB	-415, -4087
137	OE	-560, -4087
138	POL	-705, -4087
139	DROUTA	-850, -4087
140	DGOUTA	-995, -4087
141	DBOUTA	-1140, -4087
142	DROUTB	-1285, -4087
143	DGOUTB	-1430, -4087
144	DBOUTB	-1575, -4087

Pad Layout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Pin List

Name	Function	Description
CLK	Shift register clock	Rising edge triggered
LE	Transparent latch enable input	L = Hold data, H = Transparent
RESET	Power on reset	1 = Resets all shift registers and latches to Low
DIR	Shift register direction input	L = CCW, Q96->Q1; H = CW, Q1->Q96
POL	Polarity input	Invert output of latches
OE	High impedance control	L = HV output in Hi-Z state, H = normal
OLB	All outputs low	Active low
OHB	All outputs high	Active low
DR_{INA}, DR_{INB}, DG_{INA}, DG_{INB}, DB_{INA}, DB_{INB}	Red/green/blue A/B input/output	DIR = 0 "input", DIR = 1 "output"
DR_{OUTA}, DR_{OUTB}, DG_{OUTA}, DG_{OUTB}, DB_{OUTA}, DB_{OUTB}	Red/green/blue A/B output/input	DIR = 0 "output", DIR = 1 "input"
HV_{OUT}1-96	High voltage outputs	
GND	Logic ground	
V_{DD}	Logic power	
HVGND	High voltage ground	
V_{PP}	High voltage power	

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