Demo Kit Available

128 Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- ❏ Processed with HVCMOS technology
- ❏ 128 Channels
- ❏ 4 Separate shift registers
- ❏ 5V CMOS logic
- ❏ Output voltages up to 80V
- ❏ ±30mA output current capability
- ❏ Low power level shifting
- ❏ 40MHz data shifting
- ❏ Latched data outputs
- ❏ Forward and reverse shifting option via DIR pin
- ❏ Output diode to ground and V_{PP} for efficient power recovery
- ❏ Outputs can be hot switched

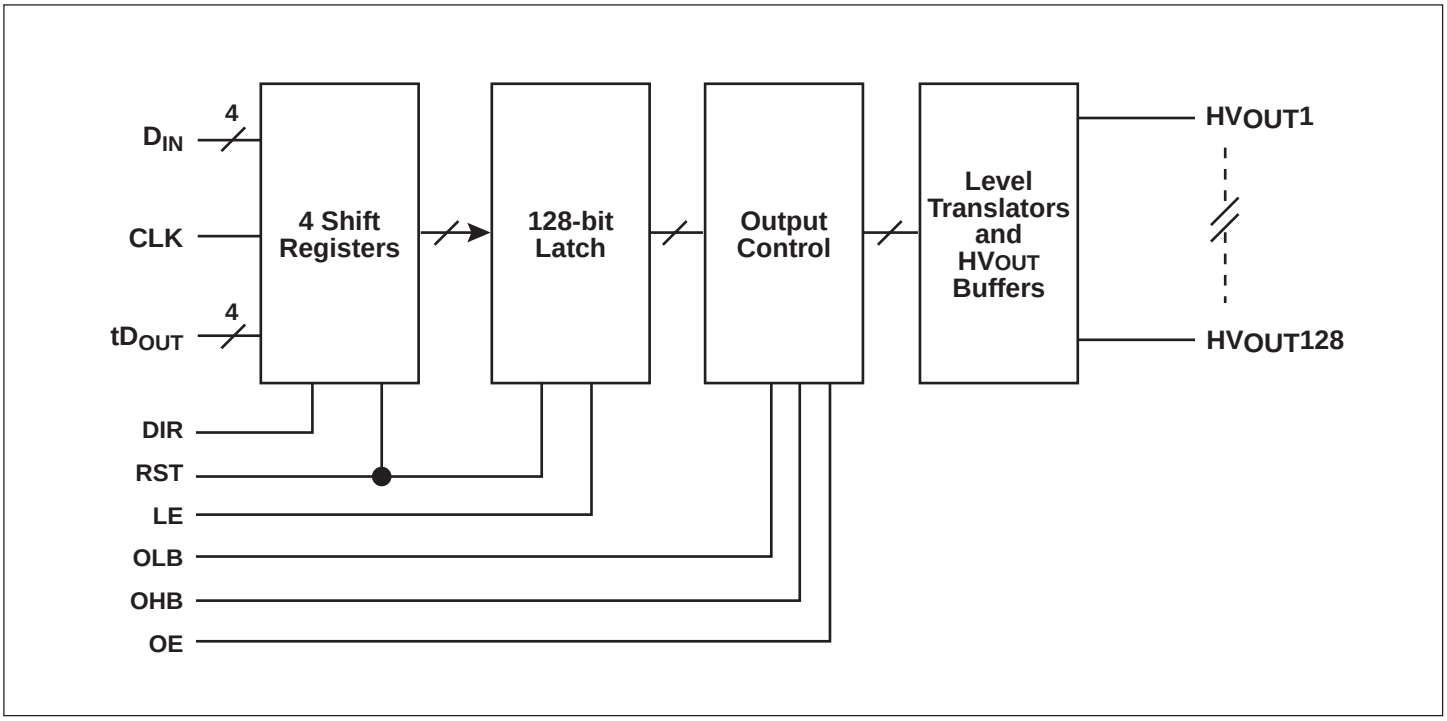
General Description

The Supertex HV583 is a 128 channel low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a display driver. It can also be used in any application requiring multiple output, high voltage current sourcing and sinking capability such as plasma displays and inkjet printers. The device has 4 parallel 32-bit shift registers, permitting data rates 4X the speed of one. The data are shifted in during the low to high clock transition. There are also 128 latches and control logic to shift clockwise or counterclockwise. The outputs can be in a high impedance state via the output enable logic pin.

Applications

- ❏ Plasma Displays
- ❏ Inkjet Printers

Functional Block Diagram



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Absolute Maximum Ratings*

V_{PP}, High voltage supply	-0.5V to +90V
V_{DD}, Logic supply voltage	-0.5V to +7.0V
Iout, Output source and sink current	-65mA to +40mA
Idiode, Output body diode current	-65mA to +65mA
Logic input voltages	-0.5V to V_{DD}+0.5V
Tj, Junction temperature	-25°C to +150°C
Storage temperature	-40°C to +150°C

*All voltages are referenced to device ground. Absolute maximum ratings are those values which damage to the device may occur. Functional operation under these conditions is not implied. Continous operation of the device at the absolute rating level may affect device reliability.

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options
		Die
HV583	80V	HV583X

Notes:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High voltage supply	15		80	V	Cload = 300pF
V_{DD}	Low voltage supply	4.5	5.0	5.5	V	
Iout	HVout peak output current	-30		30	mA	
SR	V_{PP} power supply slew rate			8.0	V/µs	
fclk	Clock frequency			40	MHz	Data read
				25	MHz	Cascade connection
Tj	Operating junction temperature	-25		+125	°C	

Electrical Characteristics

DC Characteristics (Tj = 25°C, V_{DD} = 5V, V_{PP} = 80V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{PPQ}	V_{PP} quiescent supply current			10	µA	
I_{DDQ}	V_{DD} quiescent supply current			10	µA	
HVoh	High level output voltage	73	76		V	Iout = 30mA, V_{PP} = 80V
		10				Iout = 10mA, V_{PP} = 20V
HVohd	Output p-channel body diode			81.5	V	Iout = -30mA, V_{PP} =80V
HVol	Low level output voltage		3	6	V	Iout = -30mA
HVold	Output n-channel body diode	-1.5			V	Iout = +30mA
Vih	Logic input high voltage	2.0		V_{DD}	V	V_{DD} = 4.5V to 5.5V
Vil	Logic input low voltage	0		0.8	V	V_{DD} = 4.5V to 5.5V
Iih	Logic input high current			1.0	µA	Vih = 5.3V, V_{DD} = 5.0V
		10	30	50	µA	Vih = 5.0V, For DIR only
Iil	Logic input low current	-1.0			µA	Vil = -0.3V
Voh	Logic output high	4.5V			V	Iout = 1.0mA
Vil	Logic output low			0.5V	V	Iout = -1.0mA

AC Electrical Characteristics (Tj = 25°C, V_{DD} = 5V, V_{PP} = 80V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
twclk	Clock pulse width, high and low	10			ns	V_{DD} =4.5V to 5.5V, Tj=-25°C to 125°C
twLE	LE pulse width, high and low	10			ns	
tsu1	Setup time, DAs, DBs to clk	5			ns	
tsu2	Setup time, clk to LE	10			ns	
tsu3	Setup time, LE to $\overline{OL}$, $\overline{OH}$	25			ns	
th1	Hold time, clk to DAs, DBs	5			ns	
th2	Hold time, LE to clk	10			ns	
tpdHL	Clk to DAs, DBs			25	ns	C=15pF
tpdLH	Clk to DAs, DBs			25	ns	C=15pF
tpHL	LE, $\overline{OH}$, $\overline{OL}$ to HVout			150	ns	C=50pF
tpLH	LE, $\overline{OH}$, $\overline{OL}$ to HVout	Typ -20	tpHL+tf	Typ +40	ns	C=80pF
tpHZL	$\overline{OE}$ to HVout			150	ns	C=50pF
tpLZH	$\overline{OE}$ to HVout	Typ -20	tpHL+tf	Typ +40	ns	C=80pF
tpHZ	$\overline{OE}$ to HVout			300	ns	Rl=10K, C=50pF
tpLZ	$\overline{OE}$ to HVout			300	ns	Rl=10K, C=50pF
tr	HVout			120	ns	C=50pF
tf	HVout			120	ns	C=50pF

Shift Register Truth Table

DIR	Clk	State of Shift Register	Shift Direction
L or open	L to H	Shift	D_{XB} to D_{XA}
L or open	H to L	Hold	D_{XB} to D_{XA}
H	L to H	Shift	D_{XA} to D_{XB}
H	H to L	Hold	D_{XA} to D_{XB}

Latch Truth Table

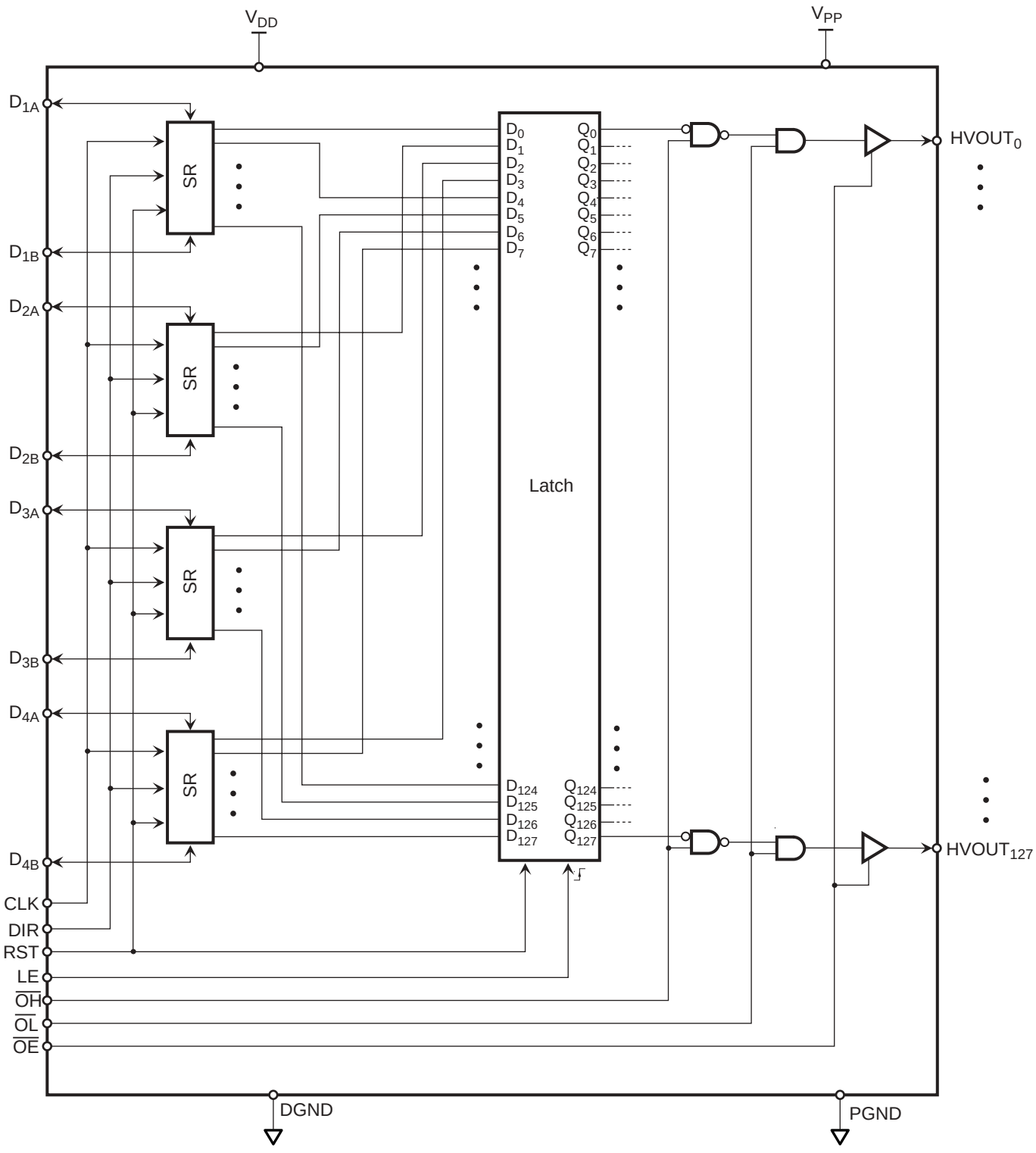
LE	Output State of Latch
L to H	Latch execution
H to L	Hold

HVout Truth Table

$\overline{OE}$	$\overline{OL}$	$\overline{OH}$	DA/DB	HVout
L	X	X	X	Z
H	L	X	X	L
H	H	L	X	H
H	H	H	L	L
H	H	H	H	H

H = Level High
L = Level Low
X = Don't care. Can be High or Low
Z = High impedance. Open circuit.

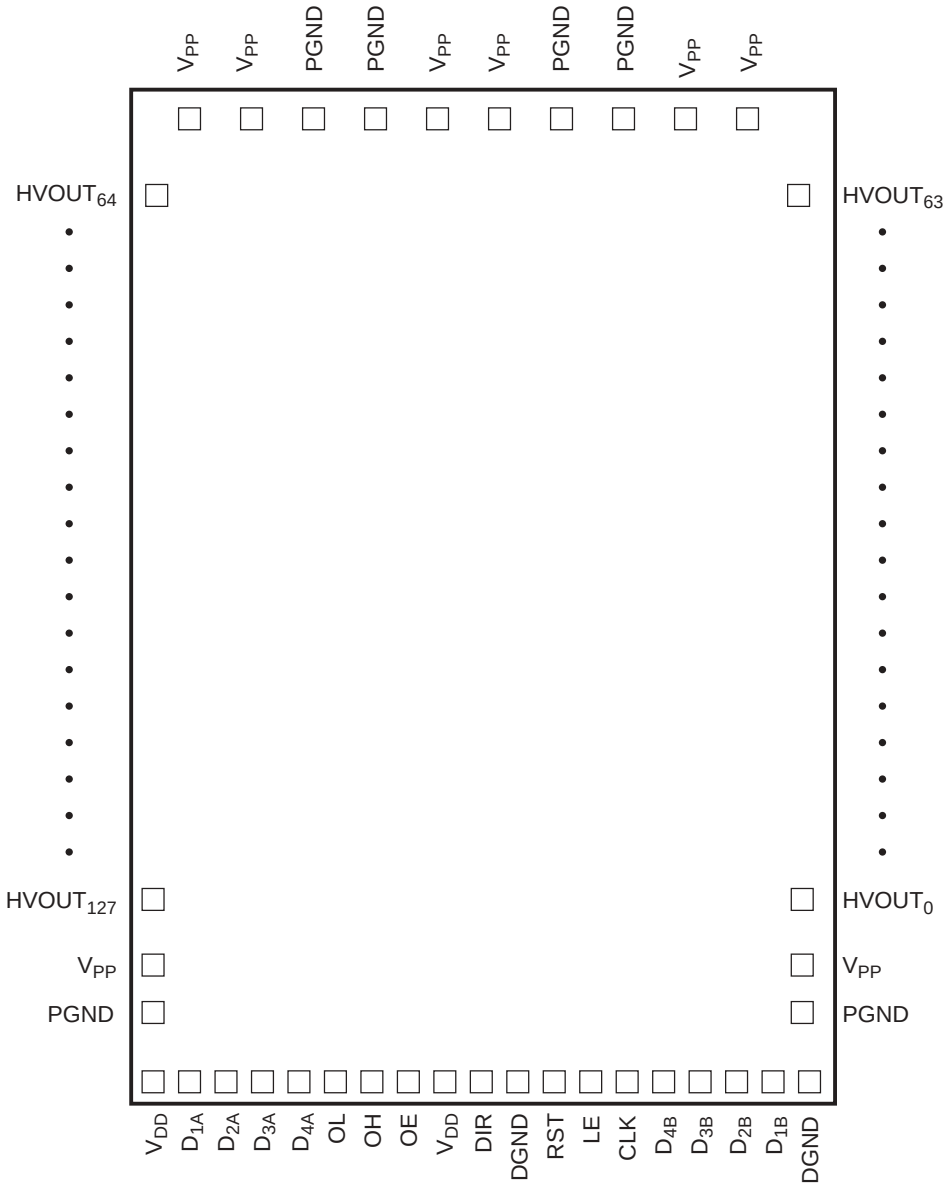
Block Diagram



Pad Description

Vpp	High voltage supply for outputs.
Vdd	Low voltage logic supply
D1A to D4A	Right data input/output. Input when Dir=H, Output when Dir=L.
D1B to D4B	Left data input/output. Input when Dir=L, Output when Dir=H.
Dir	Dir=L or open, D_{XB} to D_{XA} shift. Dir=H, D_{XA} to D_{XB} shift.
Clk	Clock input. Data shifted from low to high transition.
RST	Resets latches.
LE	Latch enable. Data latches during rising edge LE.
$\overline{OE}$	Output enable bar. HVout high impedance control.
$\overline{OL}$	Output low bar. HVout=low when this pin is low.
$\overline{OH}$	OH bar input.
DGND	Digital logic ground.
PGND	HVout output ground.
HVout0 to HVout127	High voltage outputs.

Pad Location



Pad Coordinates

VPP	-741.5	4079.6
VPP	-631.5	4079.6
PGND	-397.5	3918.6
PGND	-287.5	3918.6
VPP	-27.5	4079.6
VPP	82.5	4079.6
PGND	342.5	3918.6
PGND	452.5	3918.6
VPP	686.5	4079.6
VPP	796.5	4079.6
HVout63	1059.6	3716.1
HVout62	1059.6	3606.1
HVout61	1059.6	3496.1
HVout60	1059.6	3386.1
HVout59	1059.6	3276.1
HVout58	1059.6	3166.1
HVout57	1059.6	3056.1
HVout56	1059.6	2946.1
HVout55	1059.6	2836.1
HVout54	1059.6	2726.1
HVout53	1059.6	2616.1
HVout52	1059.6	2506.1
HVout51	1059.6	2396.1
HVout50	1059.6	2286.1
HVout49	1059.6	2176.1
HVout48	1059.6	2066.1
HVout47	1059.6	1956.1
HVout46	1059.6	1846.1
HVout45	1059.6	1736.1
HVout44	1059.6	1626.1
HVout43	1059.6	1516.1
HVout42	1059.6	1406.1
HVout41	1059.6	1296.1
HVout40	1059.6	1186.1
HVout39	1059.6	1076.1
HVout38	1059.6	966.1
HVout37	1059.6	856.1
HVout36	1059.6	746.1
HVout35	1059.6	636.1
HVout34	1059.6	526.1
HVout33	1059.6	416.1
HVout32	1059.6	306.1
HVout31	1059.6	196.1
HVout30	1059.6	86.1
HVout29	1059.6	-23.9
HVout28	1059.6	-133.9
HVout27	1059.6	-243.9
HVout26	1059.6	-353.9
HVout25	1059.6	-463.9
HVout24	1059.6	-573.9
HVout23	1059.6	-683.9
HVout22	1059.6	-793.9
HVout21	1059.6	-903.9
HVout20	1059.6	-1013.9
HVout19	1059.6	-1123.9
HVout18	1059.6	-1233.9
HVout17	1059.6	-1343.9
HVout16	1059.6	-1453.9
HVout15	1059.6	-1563.9
HVout14	1059.6	-1673.9

HVout13	1059.6	-1783.9
HVout12	1059.6	-1893.9
HVout11	1059.6	-2003.9
HVout10	1059.6	-2113.9
HVout9	1059.6	-2223.9
HVout8	1059.6	-2333.9
HVout7	1059.6	-2443.9
HVout6	1059.6	-2553.9
HVout5	1059.6	-2663.9
HVout4	1059.6	-2773.9
HVout3	1059.6	-2883.9
HVout2	1059.6	-2993.9
HVout1	1059.6	-3103.9
HVout0	1059.6	-3213.9
VPP	1059.6	-3363.9
VPP	1059.6	-3473.9
PGND	1059.6	-3623.9
PGND	1059.6	-3733.9
DGND	1059.6	-3883.9
D1B	935.6	-4094
D2B	820.9	-4094
D3B	706.2	-4094
D4B	591.5	-4094
CLK	476.9	-4094
LE	362.2	-4094
RST	247.5	-4094
DGND	137.5	-4094
DIR	27.5	-4094
VDD	-82.5	-4094
OEB	-192.5	-4094
OHB	-307.2	-4094
OLB	-421.9	-4094
D4A	-536.6	-4094
D3A	-651.3	-4094
D2A	-766	-4094
D1A	-880.7	-4094
VDD	-1004.6	-3883.9
PGND	-1004.6	-3733.9
PGND	-1004.6	-3623.9
VPP	-1004.6	-3473.9
VPP	-1004.6	-3363.9
HVout127	-1004.6	-3213.9
HVout126	-1004.6	-3103.9
HVout125	-1004.6	-2993.9
HVout124	-1004.6	-2883.9
HVout123	-1004.6	-2773.9
HVout122	-1004.6	-2663.9
HVout121	-1004.6	-2553.9
HVout120	-1004.6	-2443.9
HVout119	-1004.6	-2333.9
HVout118	-1004.6	-2223.9
HVout117	-1004.6	-2113.9
HVout116	-1004.6	-2003.9
HVout115	-1004.6	-1893.9
HVout114	-1004.6	-1783.9
HVout113	-1004.6	-1673.9
HVout112	-1004.6	-1563.9
HVout111	-1004.6	-1453.9
HVout110	-1004.6	-1343.9
HVout109	-1004.6	-1233.9

HVout108	-1004.6	-1123.9
HVout107	-1004.6	-1013.9
HVout106	-1004.6	-903.9
HVout105	-1004.6	-793.9
HVout104	-1004.6	-683.9
HVout103	-1004.6	-573.9
HVout102	-1004.6	-463.9
HVout101	-1004.6	-353.9
HVout100	-1004.6	-243.9
HVout99	-1004.6	-133.9
HVout98	-1004.6	-23.9
HVout97	-1004.6	86.1
HVout96	-1004.6	196.1
HVout95	-1004.6	306.1
HVout94	-1004.6	416.1
HVout93	-1004.6	526.1
HVout92	-1004.6	636.1
HVout91	-1004.6	746.1
HVout90	-1004.6	856.1
HVout89	-1004.6	966.1
HVout88	-1004.6	1076.1
HVout87	-1004.6	1186.1
HVout86	-1004.6	1296.1
HVout85	-1004.6	1406.1
HVout84	-1004.6	1516.1
HVout83	-1004.6	1626.1
HVout82	-1004.6	1736.1
HVout81	-1004.6	1846.1
HVout80	-1004.6	1956.1
HVout79	-1004.6	2066.1
HVout78	-1004.6	2176.1
HVout77	-1004.6	2286.1
HVout76	-1004.6	2396.1
HVout75	-1004.6	2506.1
HVout74	-1004.6	2616.1
HVout73	-1004.6	2726.1
HVout72	-1004.6	2836.1
HVout71	-1004.6	2946.1
HVout70	-1004.6	3056.1
HVout69	-1004.6	3166.1
HVout68	-1004.6	3276.1
HVout67	-1004.6	3386.1
HVout66	-1004.6	3496.1
HVout65	-1004.6	3606.1
HVout64	-1004.6	3716.1

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