Preliminary

32-Channel ±40V Liquid Crystal Display Driver

Ordering Information

Device	Package Options			
	Plastic 48-Pin DIP	Ceramic 48-Pin DIP	80-Lead Plastic Quad Gullwing	Die
HV6008	HV6008P	HV6008D	HV6008PG	HV6008X

Features

- ☐ Symmetrical ±40V output swing
- ☐ Active return to GND
- ☐ 15mA peak source/sink/GND current per channel
- ☐ ±5V control logic
- ☐ Special shift register with clear
- ☐ Phase shift control
- ☐ Output enable
- ☐ Data out enable
- ☐ 1MHz shift register
- ☐ Surface mount package available

Absolute Maximum Ratings

Supply voltage, V_{DD1}[1]	-6
Supply voltage, V_{DD2}[1]	+6
Supply voltage, V_{PP}[1,2]	+42V
Supply voltage, V_{NN}[1,2]	-42V
Logic input levels	V_{DD} + 0.3V to V_{DD2} + 0.3V
Ground currrent[2]	700mA
Continuous total power dissipation[3]	1W
Operating temperature range	
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV60 is a 32-channel liquid crystal display driver with 3-state DMOS outputs. Each output can be set to +40V, -40V, or ground. A symmetric waveform can be applied to a capacitive load using the phase shift feature of the HV60.

The HV60 consists of a 32-bit shift register with Clear, Enable, and Phase Shift logic, and 32 high voltage output buffers. With the Enable pin held low, all outputs are placed in the return to zero (GND) state. When Enable is high, each output reflects the data in its shift register bit. All outputs with a logic "0" in their shift register will be in the return to zero state. Outputs with a logic "1" in their shift register will reflect the state of the phase shift pin. These outputs will be switched to V_{PP} when phase shift is high and V_{NN} when phase shift is logic "0".

Additional functions provided are shift register clear and data out. All bits of the shift register are changed to logic "0" when clear is pulled low. With clear at a logic "1", normal shift register operation proceeds. The data output reflects the status of the 32nd shift register stage.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
$I_{DD1,2}$	V_{DD} supply current	V_{DD1}			500	µA	V_I = 4V, V_{DD1} = -6V
		V_{DD2}					V_I = 4V, V_{DD2} = +6V
V_{IH}	Logic input high		+2		V_{DD2}	V	V_{DD1} = -4.5V
V_{IL}	Logic input low		V_{DD1}		-2	V	V_{DD2} = +4.5V
V_{OH}	Logic output high		+2			V	V_{DD1} = -4.5V V_{DD2} = +4.5V
V_{OL}	Logic output low				-2	V	I_{OH} = -15µA I_{OL} = 250µA
I_{IH}	High-level logic input current				+3	µA	$V_I = V_{DD}$, $V_{DD1,2}$ = max
I_{IL}	Low-level logic input current				-50	µA	V_I = 0V, $V_{DD1,2}$ = max
I_{PP}	High voltage supply current				+1	mA	Static, no load
I_{NN}	High voltage supply current				+1	mA	Static, no load
V_{OH}	Output voltage high		+39			V	V_{PP}, V_{NN} = ±40 I_{output} = 0.0
V_{CL}	Output voltage clamp		-20		+20	mV	
V_{OL}	Output voltage low				-39	V	
Z_{OH}	Output switch impedence high			1000		Ω	V_{PP}, V_{NN} = ±40 I_O = ±15mA
Z_{CL}	Output switch impedance clamp			500			
Z_{OL}	Output switch impedance low			700			
I_O	DC output current	Output H or L			5	mA	1 output only
		Data out H or L			150	µA	

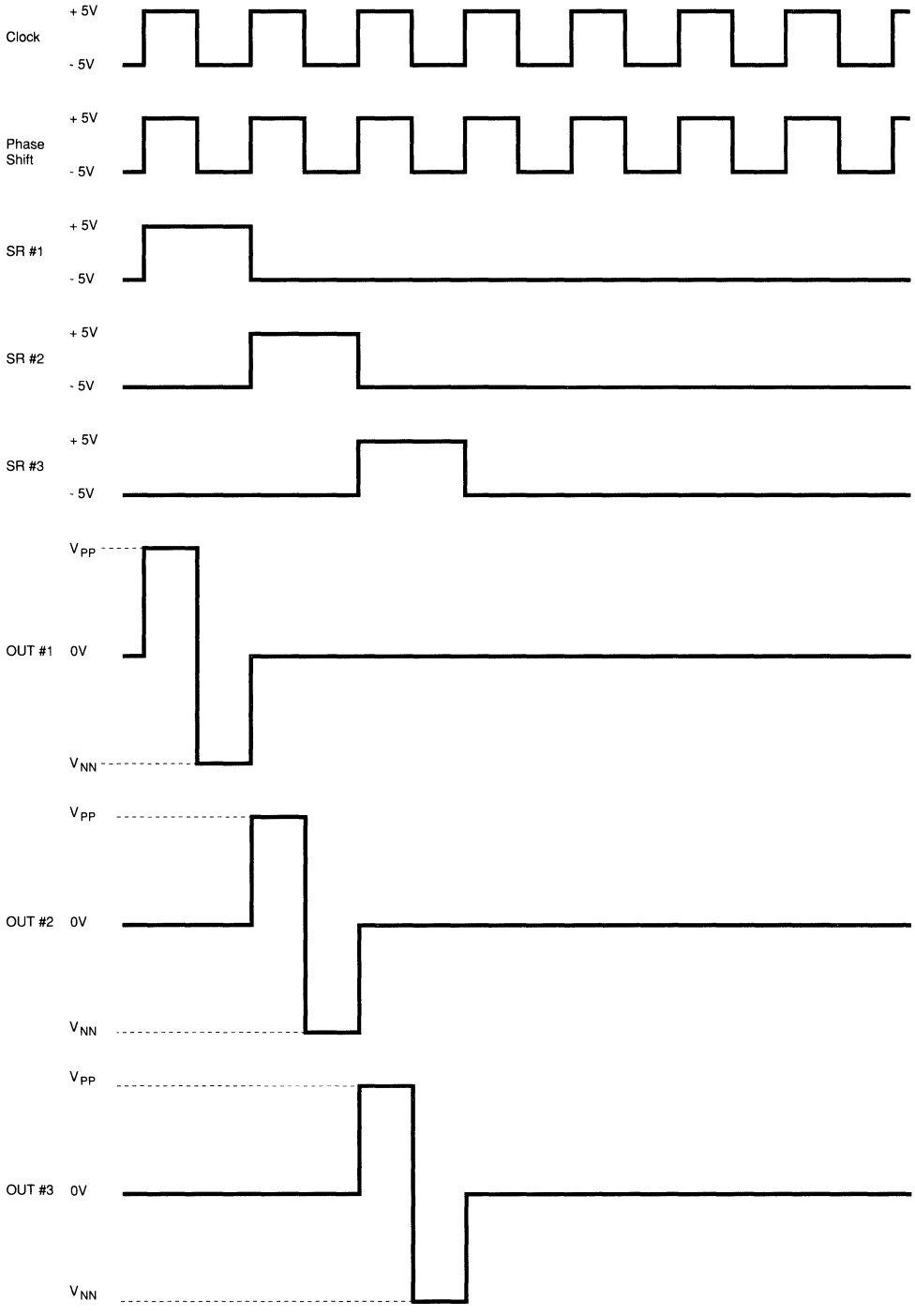
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{WH}	Width of high clock phase		TBD			
t_{WL}	Width of low clock phase		TBD			
t_{SU}	Data set-up time before clock rises		TBD			
t_H	Data hold time after clock rises	0			ns	
	Phase shift duty cycle		50		%	

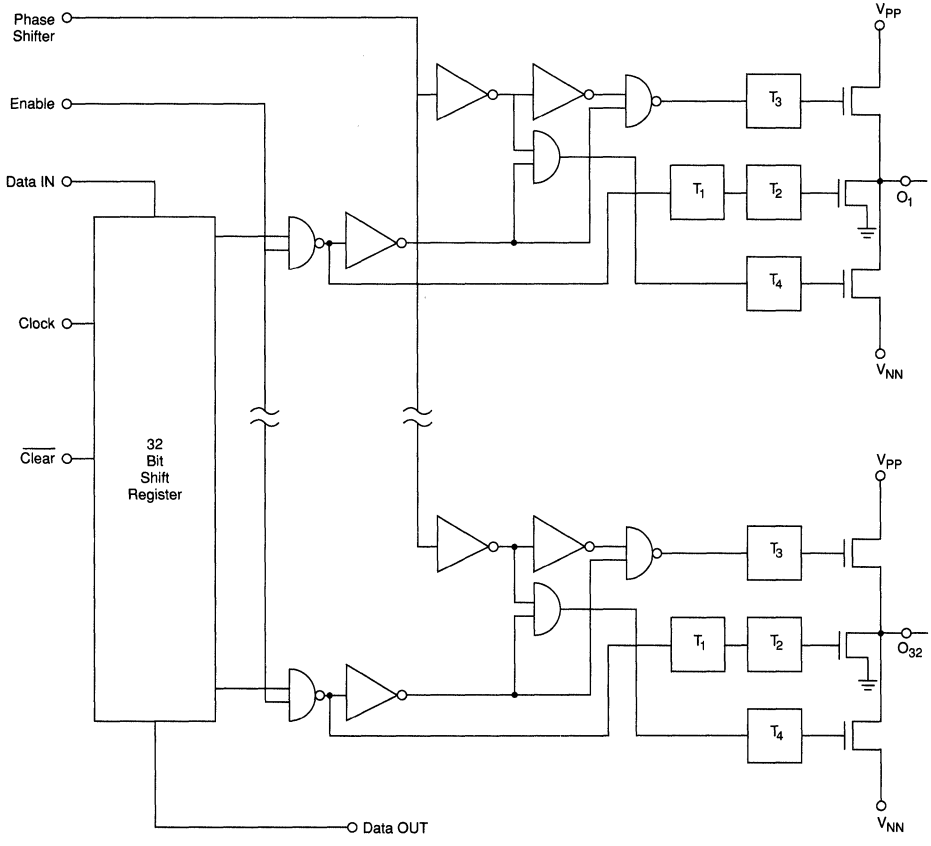
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD1}	Logic supply voltage	-4		-6	V
V_{DD2}	Logic supply voltage	+4		+6	V
V_{PP}	High voltage supply	+10		+40	V
V_{NN}	High voltage supply	-10		-40	V
V_{IH}	High-level input voltage	+2V		V_{DD2}	V
V_{IL}	Low-level input voltage	-2V		V_{DD1}	V
$I_{O\ Pk.}$	Peak output current (any state)			±80	mA
T_A	Operating free-air temperature	-10		+70	°C
f_{DIN}	Input data rate			1	MHz
f_{PS}	Phase shift rate			1	MHz

Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs	
	Data In	CLK	$\overline{CLR}$	Enable	Phase Shift	Shift Reg 1 2...32	HV Outputs 1 2...32	Data Out
CLR Reg	X	X	L	X	X	ALL L	ALL GND	L
All output GND	X	X	X	L	X	* *...*	ALL GND	*
Load S/R	H or L	↑	H	L	X	H or L *...*	ALL GND	*
Output State	X	H or L	H	H	X	L L...L	GND GND...GND	*
					H	H H...H	V_{PP} V_{PP}...V_{PP}	*
					L	L L...L	V_{NN} V_{NN}...V_{NN}	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK
↑ = Low to high transition
H = High level
L = Low level

Pin Configurations

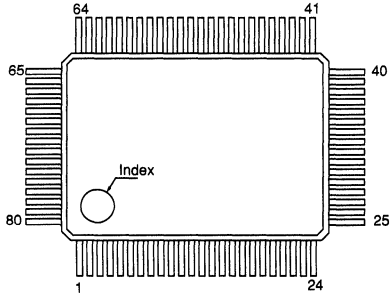
28-Pin J-Lead

Pin	Function	Pin	Function	Pin	Function
1	GND	28	Phase Shift	55	N/C
2	N/C	29	N/C	56	+40V
3	N/C	30	Clock	57	N/C
4	N/C	31	N/C	58	-40V
5	N/C	32	N/C	59	N/C
6	N/C	33	$\overline{\text{Clear}}$	60	N/C
7	-40V	34	N/C	61	N/C
8	N/C	35	-5V	62	N/C
9	+40V	36	Enable	63	N/C
10	N/C	37	N/C	64	GND
11	N/C	38	+5V	65	N/C
12	HVout 9	39	N/C	66	HVout 23
13	HVout 8	40	GND	67	HVout 22
14	HVout 7	41	N/C	68	HVout 21
15	HVout 6	42	Data Out	69	HVout 20
16	HVout 5	43	N/C	70	HVout 19
17	HVout 4	44	N/C	71	HVout 18
18	HVout 3	45	HVout 32	72	HVout 17
19	HVout 2	46	HVout 31	73	HVout 16
20	HVout 1	47	HVout 30	74	HVout 15
21	N/C	48	HVout 29	75	HVout 14
22	N/C	49	HVout 28	76	HVout 13
23	Data In	50	HVout 27	77	HVout 12
24	N/C	51	HVout 26	78	HVout 11
25	GND	52	HVout 25	79	HVout 10
26	N/C	53	HVout 24	80	N/C
27	N/C	54	N/C		

48-Pin DIP

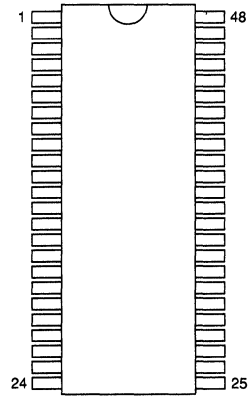
Pin	Function	Pin	Function
1	HVout 16	25	V_{DD1} (-5V)
2	HVout 15	26	Enable
3	HVout 14	27	V_{DD2} (+5V)
4	HVout 13	28	GND
5	HVout 12	29	Data Out
6	HVout 11	30	HVout 32
7	HVout 10	31	HVout 31
8	GND	32	HVout 30
9	V_{NN}	33	HVout 29
10	V_{PP}	34	HVout 28
11	HVout 9	35	HVout 27
12	HVout 8	36	HVout 26
13	HVout 7	37	HVout 25
14	HVout 6	38	HVout 24
15	HVout 5	39	V_{PP}
16	HVout 4	40	V_{NN}
17	HVout 3	41	GND
18	HVout 2	42	HVout 23
19	HVout 1	43	HVout 22
20	Data In	44	HVout 21
21	GND	45	HVout 20
22	Phase Shift	46	HVout 19
23	Clock	47	HVout 18
24	$\overline{\text{Clear}}$	48	HVout 17

Package Outlines



top view

80-pin Gullwing Package



top view

48-pin DIP