Hynix Semiconductor Inc.

CMOS Image Sensor With 8-bit ADC

HV7131E1

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DESCRIPTION

HV7131E1 is a highly integrated single chip color image sensor using Hynix 0.5um CMOS process developed for image application to realize high efficiency with R/G/B photo sensor. The sensor has 648X488-pixel array. Each compact active pixel element with high photosensitivity converts photon energy to analog voltage signal. The on-chip 8 bit Analog to Digital Converter (ADC) with built-in R/G/B gain control converts analog voltage signal to digital code. Hynix proprietary on-chip Correlated Double Sampling (CDS) circuit can significantly reduce Fixed Pattern Noise (FPN). The 8 bit RGB raw data is directly available on the package pins and just a few control signals are needed for whole chip control so that it is very easy to configure CMOS imaging system.

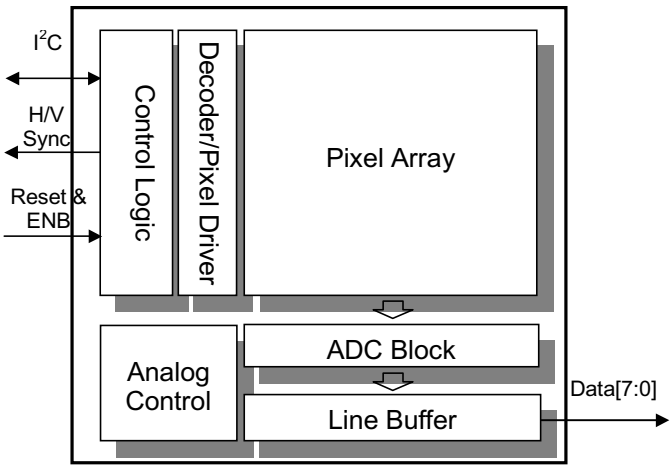
FEATURES

- VGA resolution
- 1/3 inch optical format
- High efficiency R/G/B color photo sensors
- Bayer RGB color pattern
- Anti-blooming circuit
- Integrated 8-bit ADC for direct digital output
- Programmable pan/tilt and window size
- Clock speed up to 15MHz
- Low power 3.3V operation
- Programmable power down mode
- Strobe control signal generation
- Automatic reset level control
- Controllable full function through standard I^2C bus
- Programmable Gain Control
- Flexible exposure time control
- Integrated on-chip timing and drive control
- Programmable image mirroring
- 48Pin CLCC Package

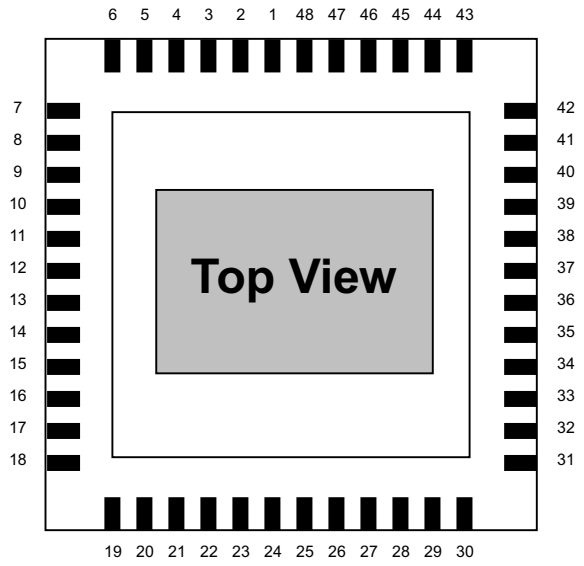
TECHNICAL SPECIFICATION

Total Pixel Array	648x488
Effective Pixel Array	644x484
Pixel size	8x8μm²
Fill factor	30%
Sensitivity	2.7V/lux.sec@Gr.
Power Supply	3.3V
Power Consumption (max.)	< 90mW @ 3.3V, 10MHz
Operating temperature	0 ~ 40 ℃

FUNCTIONAL BLOCK DIAGRAM



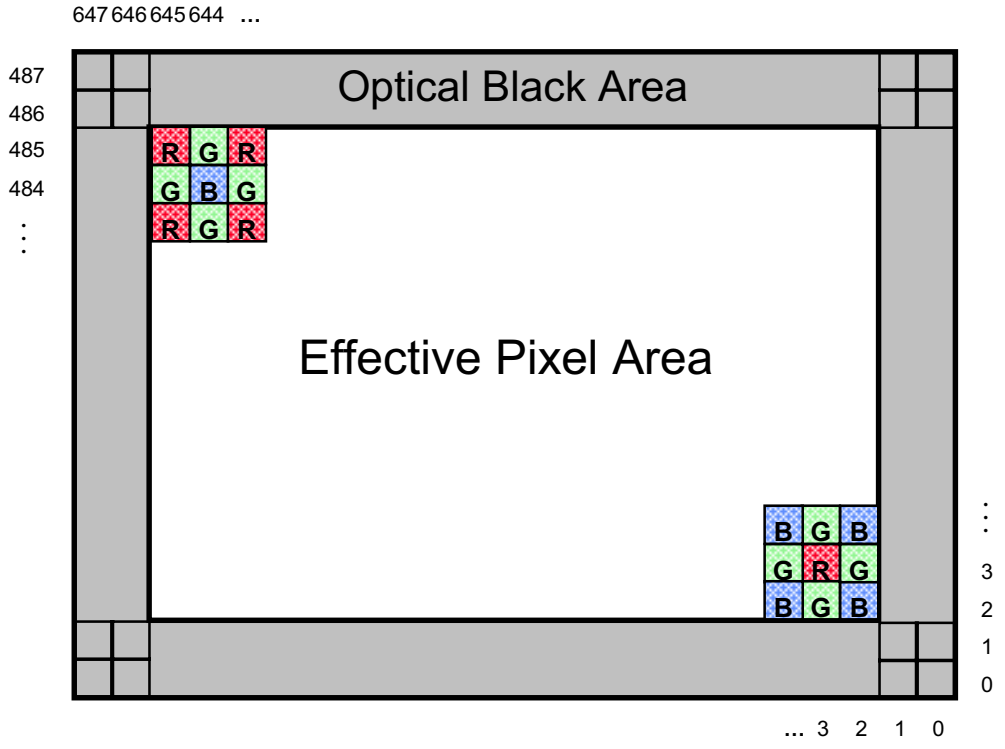
PIN CONFIGURATION (48 pin CLCC)



PIN NO.	NAME	PIN NO.	NAME
1	SCK	25	DATA4
2	DGND	26	DGND
3	ENB	27	DATA3
4	DGND	28	DATA2
5	MCLK	29	DATA1
7	AVDD	30	DATA0
8	AGND	32	DGND
17	AGND	42	DVDD
18	AVDD	43	RESET
20	Strobe	44	VSYNC
21	DGND	45	HSYNC
22	DATA7	46	DGND
23	DATA6	47	SDA
24	DATA5	48	DGND

Note: Pin6, Pin9~16, Pin19, Pin31, Pin33~41: No Connection

COLOR PATTERN



PIN DESCRIPTION (48Pin CLCC)

PIN	NAME	I/O	DESCRIPTION
1	SCK	I	I^2C clock ; I^2C clock control from I^2C master
2	DGND	I	I/O Digital Ground
3	ENB	I	Sensor Enable Signal (Active High) ; 'H' normal operation, 'L' disable
4	DGND	I	I/O Digital Ground
5	MCLK	I	Master Clock (up to 15MHz) ; Global master clock for image sensor internal timing control
6	N.C	I	No Connection
7	AVDD	I	Analog Supply Voltage 3.3V
8	AGND	I	Analog Ground
9 ~ 16	N.C	-	No Connection
17	AGND	I	Analog Ground
18	AVDD	I	Analog Supply Voltage 3.3V
19	N.C	-	No Connection
20	STROBE	O	Strobe Signal
21	DGND	I	I/O Digital Ground
22	DATA7	O	Image Data bit 7
23	DATA6	O	Image Data bit 6
24	DATA5	O	Image Data bit 5
25	DATA4	O	Image Data bit 4
26	DGND	I	I/O Digital Ground
27	DATA3	O	Image Data bit 3
28	DATA2	O	Image Data bit 2
29	DATA1	O	Image Data bit 1
30	DATA0	O	Image Data bit 0
31	N.C	-	No Connection
32	DGND	I	Core Digital Ground
33 ~ 41	N.C	-	No Connection
42	DVDD	I	Digital Supply Voltage 3.3V
43	/RESET	I	Hardware Reset Signal (Active Low).
44	VSYNC	O	Vertical synchronization signal / Frame start output ; Signal pulses at the start of image data frame, VSYNC duration is programmable.
45	HSYNC	O	Horizontal synchronization signal / Data valid output ; Data is valid, when HSYNC is 'H', HSYNC signal remains high, during horizontal data window width.
46	DGND	I	I/O Digital Ground
47	SDA	I/O	I^2C Data ; I^2C standard data I/O port
48	DGND	I	I/O Digital Ground

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

- Supply voltage (Analog, Digital) : 3.3V +/– 5%
- Voltage on any input pins : 0V ~ 3.3V + 5%
- Operating Temperature (Celsius) : 0 ~ 40
- Storage Temperature (Celsius) : -30 ~ 80

Note: Stresses exceeding the absolute maximum ratings may induce failure.

DC PARAMETERS

Symbol	Parameter	Unit	Min.	Max.	Load[pF]	Notes
V_{DD}	Operation supply voltage	V	3.14	3.47		
V_{ih}	Input voltage logic "1"	V	2.0	3.47	6.5	
V_{il}	Input voltage logic "0"	V	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	V	2.15		60	
V_{ol}	Output voltage logic "0"	V		0.4	60	
T_a	Ambient operating temperature	Celsius	0	40		

AC PARAMETERS

Symbol	Parameter	Unit	Min.	Max.	Notes
MCLK	Main clock frequency	MHz		15	
SCK	I^2C clock frequency	KHz		400	1
I_{NORMAL}	Current in Normal mode	mA	15	25	3.3V, 10MHz
I_{DOWN}	Current in Power Down mode	mA		1	

Note: 1. SCK is driven by host processor. For the detailed serial bus timing, refer to I^2C Specification.

ELECTRO-OPTICAL CHARACTERISTICS

Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

Clock Frequency: 10MHz, Operating Voltage: V_{DD} =3.3V

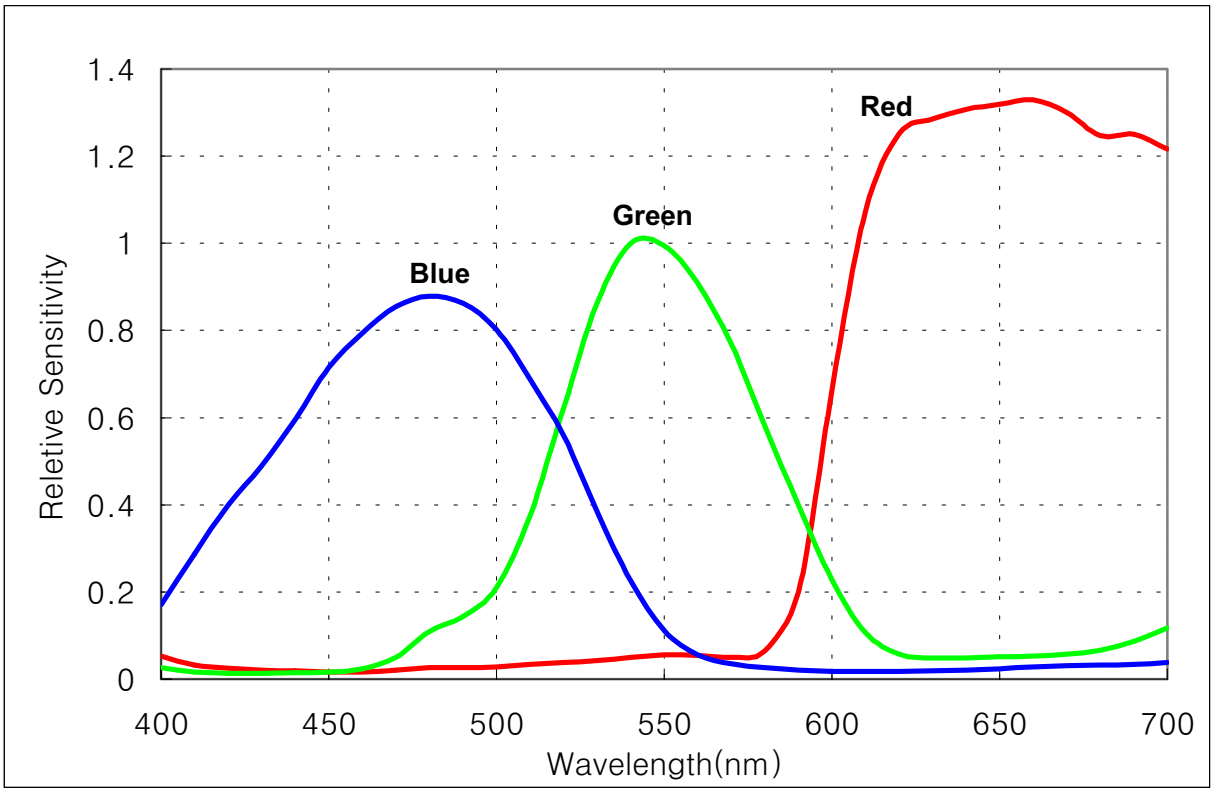
Parameter	Unit	Min.	Typical	Max.	Note
Red Sensitivity	mV / lux·sec	1400	2100		1
Green Sensitivity	mV/lux·sec	2000	2700		1
Blue Sensitivity	mV/lux·sec	1150	2000		1
Dark Signal	mV/sec		100	120	2
Output Saturation Signal	1mV	960		1000	3
Maximum Dynamic Range	dB			48	4
Output Signal Shading	%		4.3	12.8	5
Dark Signal Shading	mV/sec		85	276	6
Frame Rate (@15MHz)	Fps			45	7

Note:

1. **Measured the slope at the standard output (128code) under 11lux illumination.**
2. **Measured at zero illumination for exposure time 100ms. (T_{temp} = 40 Celsius)**
3. **Measured at 100lux illumination for exposure time 50ms.**
4. **48dB is limited by 8-bit ADC.**
5. **Adjust the average value of Green signal output to 128code then measure V_{max} and V_{min} block value (10x14 pixels) of the Green signal output and substitute the values into the following formula:**

   Output Signal Shading = (V_{max} - V_{min}) / 128 x 100 [%]
6. **Range between V_{max} and V_{min} at zero illumination for exposure time 100ms, where V_{max} and V_{min} block value (10x14 pixels) of the signal output.**
7. **Measured at MCLK 15MHz with 640x480 window size. Maximum frame rate is measured when integration time is less than effective window time [Refer to Frame Timing]**

SPECTRAL CHARACTERISTICS

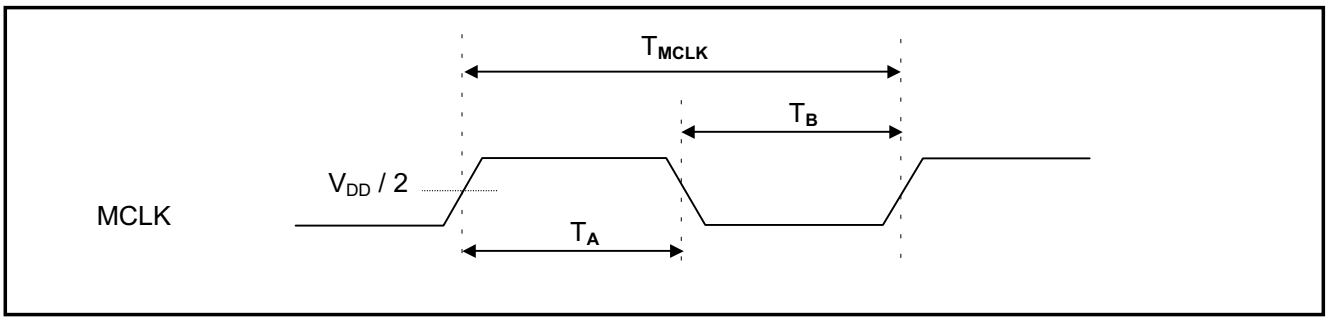


Note : We recommend the 630nm IR cut-off filter for the applications.

INPUT / OUTPUT AC CHARACTERISTICS

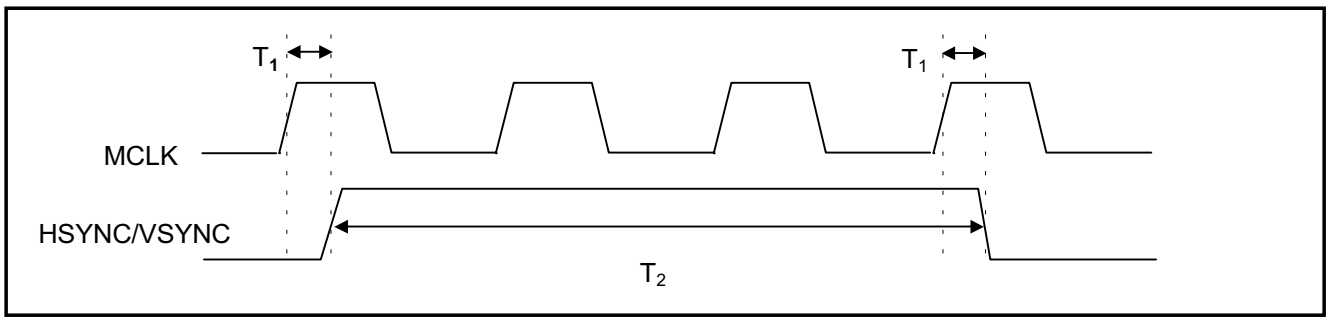
All output timing delays are measured with output load 60[pF].
Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design.
Due to the variable valid time delay of the output, output signals may be latched in the negative edge of MCLK for the stable data transfer between the image sensor and a host for less than 15MHz operation.

MCLK Duty Cycle



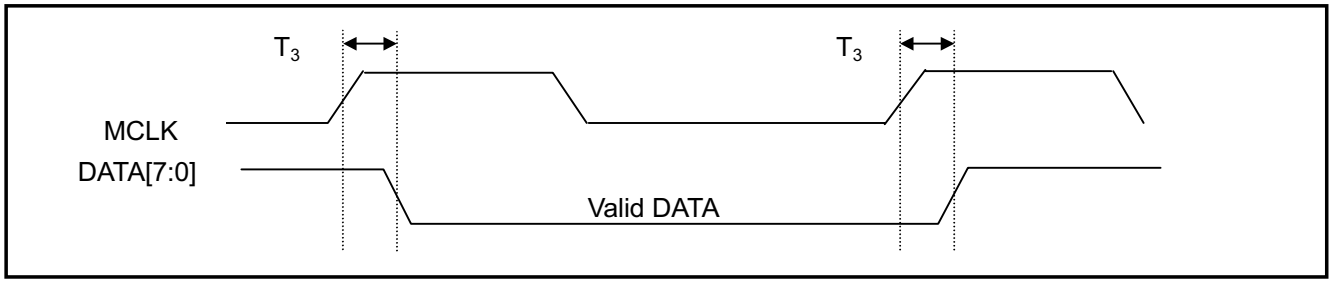
T_A = 40% ~ 60% of T_{MCLK}, T_B = 40% ~ 60% of T_{MCLK}
$T_A + T_B = T_{MCLK}$

MCLK to HSYNC/VSYNC Timing



T_1: Rising edge of MCLK to HSYNC/VSYNC valid maximum time: 18ns [output load: 60pF]
T_2: HSYNC/VSYNC valid time: minimum 1clock(subject to T_1, T_2 timing rule)

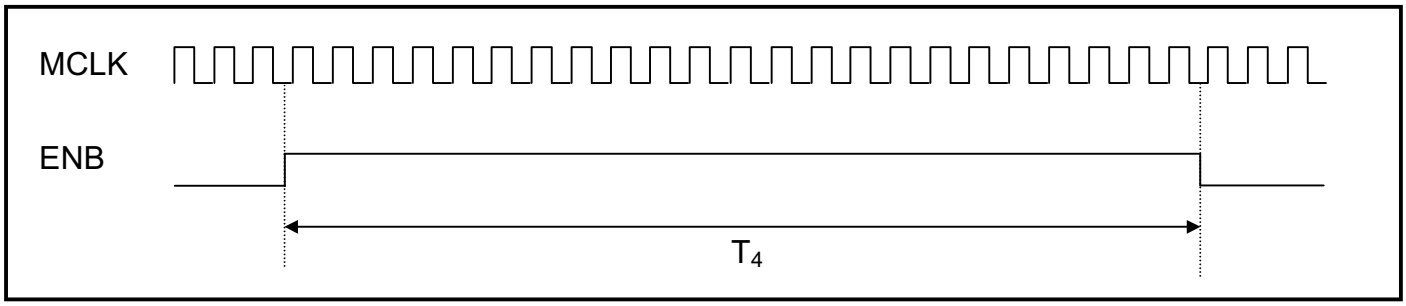
MCLK to DATA Timing



T_3: Rising edge of MCLK to DATA valid maximum time: 18ns [output load: 60pF]

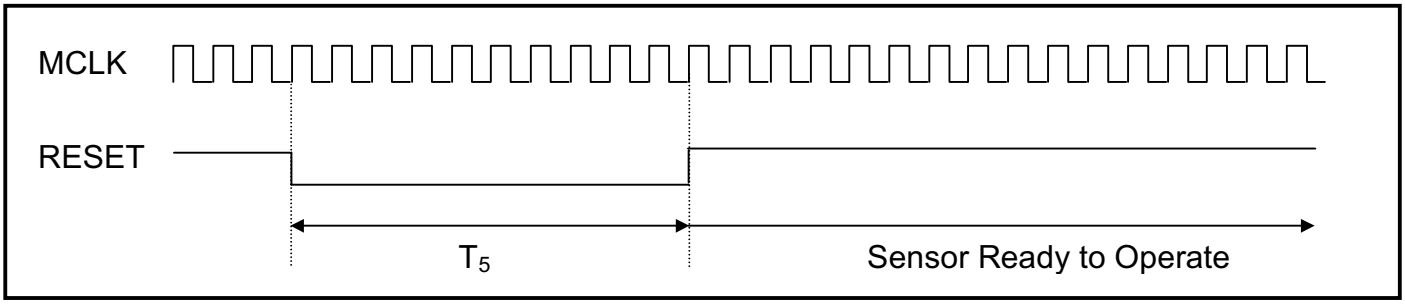
Note: HSYNC signal is high when valid data is on the DATA bus.

ENB Timing



T_4: ENB valid minimum time: 2 MCLK periods.

RESET Timing



T_5: RESET valid minimum time: 10 MCLK periods.

REGISTER DESCRIPTION

Note: I2C Device Address of CMOS Image Sensor: 22H

Group	Symbol	Address	Description	Default	Recomm-endation
Configuration Registers	Mode A	00H	Device Type and Revision (Read Only)	01H	01H
	Mode B	01H	Operating Mode B	04H	04H
	Mode C	02H	Operating Mode C	00H	D5H
Frame Registers	FRSU	10H	Row Starting Value (Upper byte)	00H	00H
	FRSL	11H	Row Starting Value (Lower byte)	03H	03H
	FCSU	12H	Column Starting Value (Upper byte)	00H	00H
	FCSL	13H	Column Starting Value (Lower byte)	03H	03H
	FWHU	14H	Window Height Value (Upper byte)	01H	01H
	FWHL	15H	Window Height Value (Lower byte)	E2H	E2H
	FWWU	16H	Window Width Value (Upper byte)	02H	02H
	FWWL	17H	Window Width Value (Lower byte)	82H	82H
Timing Register	THBU	20H	HSYNC Blanking Time Value (Upper byte)	00H	00H
	THBL	21H	HSYNC Blanking Time Value (Lower byte)	03H	03H
	TVBU	22H	VSYNC Blanking Time Value (Upper byte)	00H	00H
	TVBL	23H	VSYNC Blanking Time Value (Lower byte)	03H	03H
	TITU	25H	Exposure(Integration) Time Value (Upper byte)	06H	06H
	TITM	26H	Exposure(Integration) Time Value (Middle byte)	1AH	1AH
	TITL	27H	Exposure(Integration) Time Value (Lower byte)	80H	80H
Adjust Register	ARLV	30H	Reset Level Value	38H	38H
	ARCG	31H	Red Color Gain Value	1EH	1EH
	AGCG	32H	Green Color Gain Value	1EH	1EH
	ABCG	33H	Blue Color Gain Value	1EH	1EH
	APBV	34H	Pixel Bias Voltage Control Value	02H	02H
Reset Level Statistics Register	LoREfNOH	57H	Low Reset Counter Value [value<5] (Upper byte)	(Read Only)	
	LoREfNOL	58H	Low Reset Counter Value [value<5] (Lower byte)	(Read Only)	
	HiRefNOH	59H	High Reset Counter Value [value>123] (Upper byte)	(Read Only)	
	HiRefNOL	5AH	High Reset Counter Value [value>123] (Lower byte)	(Read Only)	
	RLVTH	5BH	Reset Counter Threshold Value	0AH	01H

CONFIGURATION REGISTERS

Device Type and Revision[00H] – Read Only — Default : 01H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	1

Represent device type and revision. High Nibble: Sensor Array Size, Low Nibble: Revision Number

For HV7131E1, identity value is 01H, [VGA: 0, Revision 1]

MODE_B[01H] – Read / Write — Default : 04H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	Operation Mode		Output Data Type		HSYNC Output Mode	Window Mode	Frame Mode	-
Default	0	0	0	0	0	1	0	-

B<7:6> - Selects sensor operation mode.

Always should be 0.

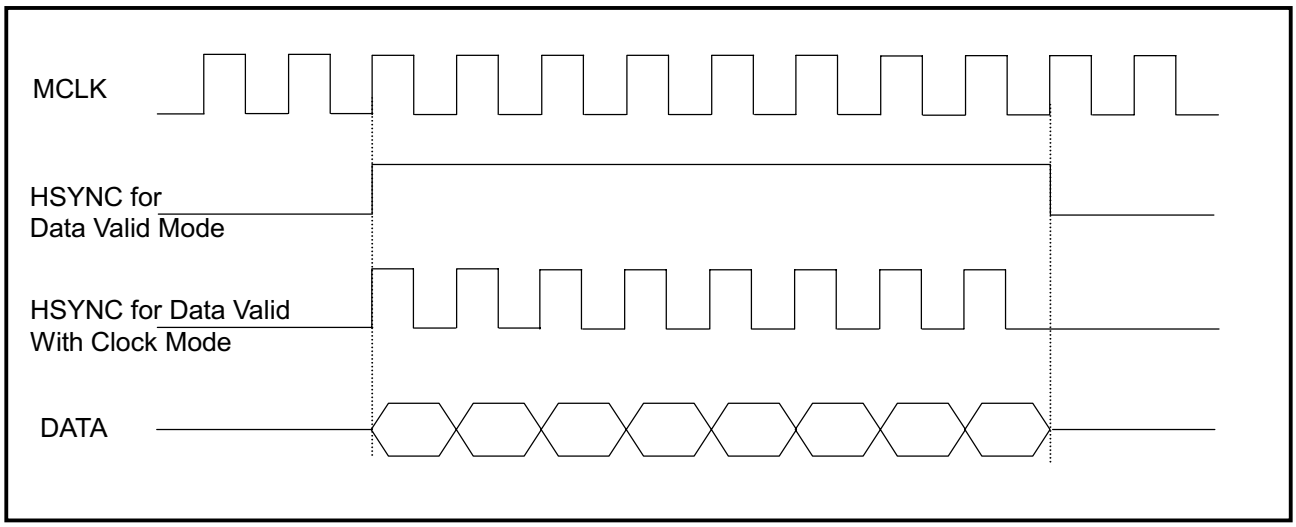
B<5:4> - Selects output data type.

Always should be 0.

B<3> - Selects HSYNC output mode between “Data valid mode” and “Data valid with clock mode”.

0: Data valid mode [Refer to following Figure]

1: Data valid with clock mode [Refer to following Figure]



B<2> - Window mode.

Always should be 1, Current default window image size is 642x482.

B<1> - Frame mode.

Always should be 0.

MODE_C[02H] – Read / Write **Default : 00H**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	Auto Reset	Adaptive Mode1	Strobe Mode	Image Mirroring	Reserved	Power Down	Display Mode	Adaptive Mode0
Default	0	0	0	0	0	0	0	0

B<7> - When Auto Reset is enabled, Sensor itself can find appropriate reset level automatically using reset counter threshold values register. [Refer to reset counter threshold value register] Do not control reset level externally when auto reset function is enabled.

0: Disable

1: Enable (Recommended)

B<6> - When Adaptive mode0 and mode1 are enabled, sensor has a high speed frame rate for updating integration time on normal operation. However, we recommend that the appropriate frequency of updating integration time is every three or four frame.

0: Disable

1: Enable (Recommended)

B<5> - Though sensor has enough integration time to capture image, sensor can't obtain good image quality in dark environment. For this situation, Our CMOS Image sensor can generate strobe signal for driving external strobe circuit.

The strobe output is active high when integration time is over than effective window height time(Window Height Value X (648 + HSYNC Blanking Time Value)). Because sensor uses progressive exposure method, strobe signal should cover all line(all pixels). The following figure shows that the relationships between strobe signal and exposure time. In this example picture, we set Window Width =642, Window Height = 480, Integration Time = 316,498 clocks and HSYNC Blanking Time = 10, VSYNC Blanking Time = 658 [Refer to application note for detail information].

0: Disable

1: Enable

Notes

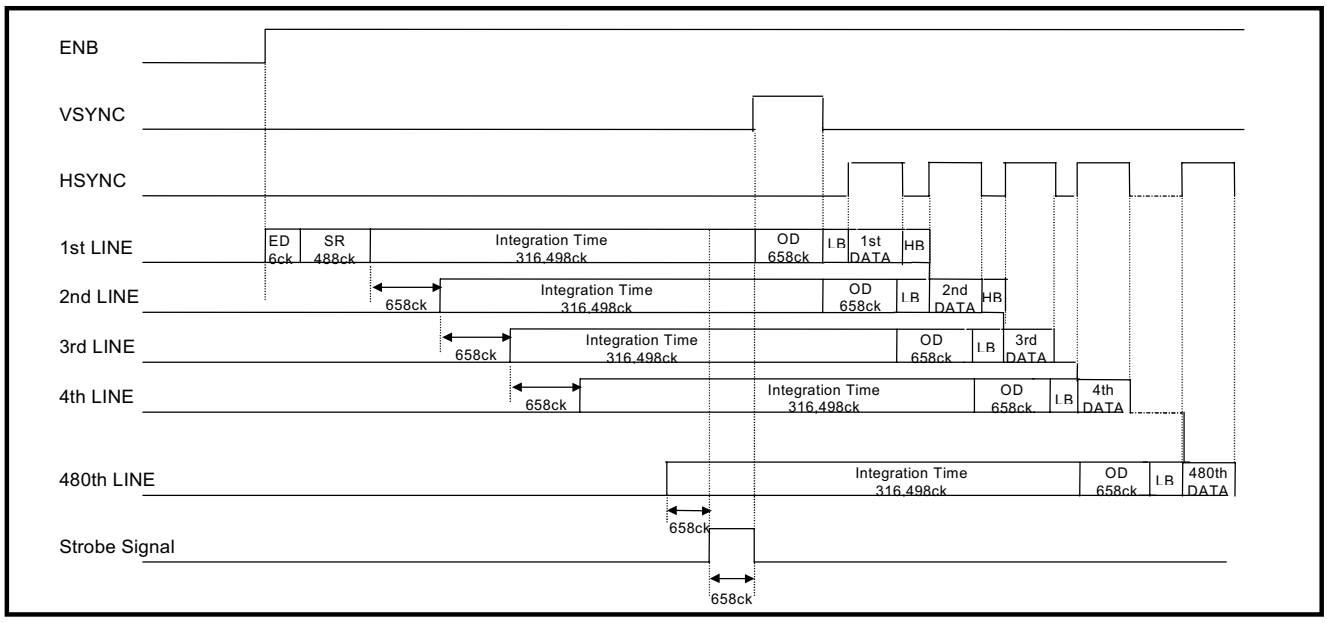
SR : Sensor Reset Time = 488 clocks

ED : Enable Sensor = 6 clcoks

OD : One Line Delay = (648 + HSYNC Blanking Time) = 658 clcoks

LB : Line Blanking Time = (648 – Window Width)/2 = 3 clocks

HB : Horizontal Blanking Time = 2*LB + HSYNC Blanking Time = 16 clocks



B<4> - When Image mirroring mode is enabled, origin of pixel array is changed from the right of bottom to left of bottom. In this case, Column starting value indicates a last pixel of valid data output line. The value(Window Width value + Column starting value – 1) indicates a first pixel of valid data output line. Therefore, you should change Column starting value to Column starting value +1 or –1 if you want a same color data output as default origin.

0: Origin of pixel array is the right of bottom.

1: Origin of pixel array is the left of bottom.

B<3> - Reserved.

Always should be 0.

B<2> - When power down is enabled and ENB is low, sensor goes to power down state for saving power. However, sensor goes to normal operation without disabling or enabling power down mode when ENB goes to HIGH.

0: Disable 1: Enable

B<1> - Selects Three Gain Control mode or One Gain Control mode. In Gain mode, gain control is controlled by G Gain register value.

0: Three Gain Control mode 1: One Gain Control mode

B<0> - Adaptive Mode0 should be enabled together with Adaptive Mode1 to enhance frame rate(Refer to Adaptive Mode1)

0: Disable 1: Enable (Recommended)

FRAME SIZE CONTROL REGISTERS

Row Starting Value Upper Byte[10H] – Read / Write — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	-	-	-	-	-	0

Row Starting Value Lower Byte[11H] – Read / Write — Default : 03H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	1	1

B<8:0> - Row Starting register selects Row Starting point of window image. [Refer to following figure] Programmable range is from 2 to (486-Window Height Value). However, we recommend the value 2~4 for VGA resolution.

Column Starting Value Upper Byte[12H] – Read / Write — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	-	-	-	-	0	0

Column Starting Value Lower Byte[13H] – Read / Write — Default : 03H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	1	1

B<9:0> - Column Starting Value register selects Column Starting point of window image. [Refer to following figure] Programmable range is from 2 to (646–Window Width Value). However, we recommend the value 2~4 for VGA resolution.

Window Height Value Upper Byte[14H] – Read / Write — Default : 01H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	-	-	-	-	-	1

Window Height Value Lower Byte[15H] – Read / Write — Default : E2H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	1	1	1	0	0	0	1	0

B<8:0> - Window Height Value register selects valid height of window image. [Refer to following figure] Programmable range is from 2 to 484 . However, we recommend the value 482 for VGA resolution, since general color interpolation algorithm using 3X3 spatial mask requires additional pixels around edges. This value should be even number. In addition, Row Starting value + Window Height value should never be over 488.

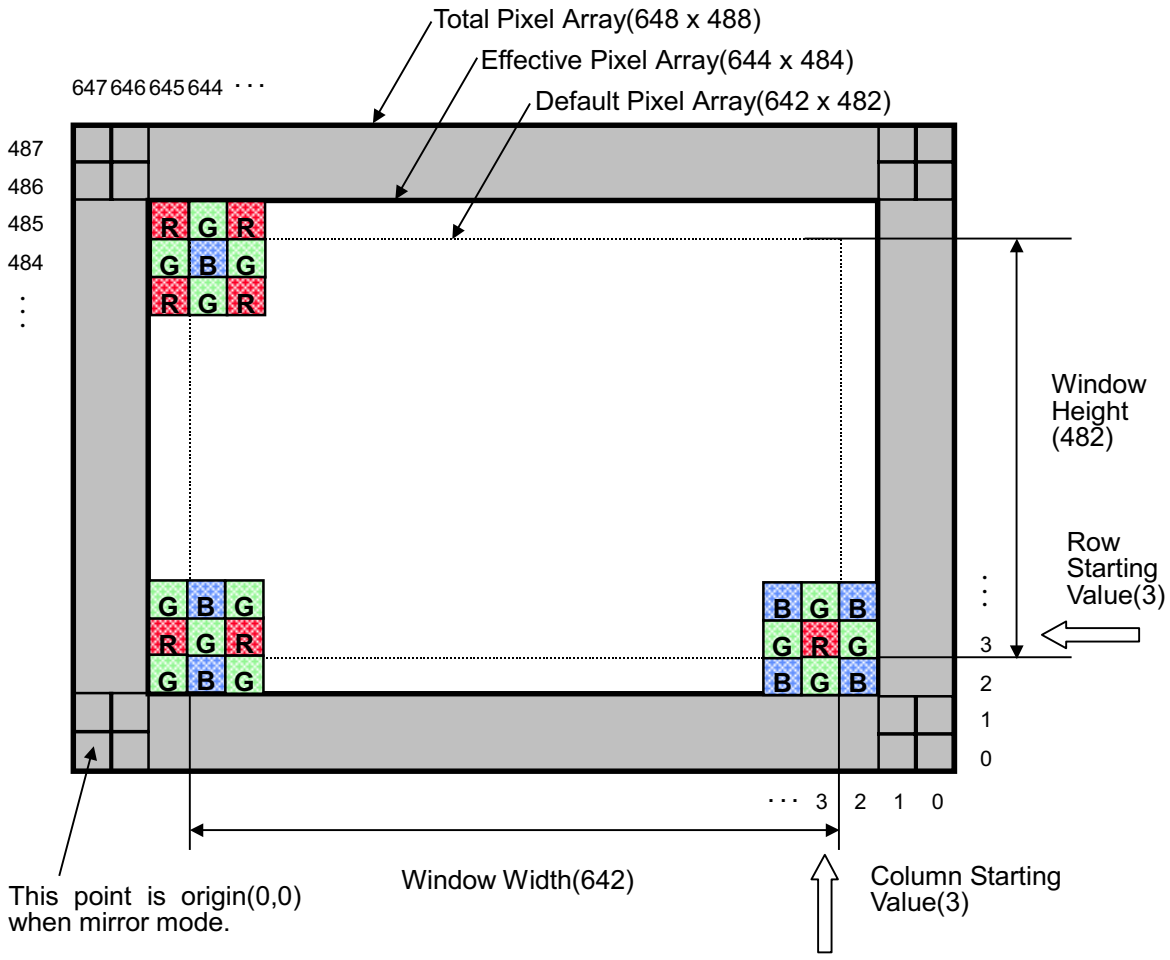
Window Width Value Upper Byte[16H] – Read / Write **Default : 02H**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	-	-	-	-	1	0

Window Width Value Lower Byte[17H] – Read / Write **Default : 82H**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	1	0	0	0	0	0	1	0

B<9:0> - Window Width Value register selects valid width of window image. [Refer to following figure] Programmable range is from 2 to 644. However, we recommend 642 for VGA resolution, since general color interpolation algorithm using 3X3 spatial mask requires additional pixels around edges. This value should be even number. In addition, Column Starting value + Window Width value should never be over 648.



Note: HV7131E1 can image any user specified window area within image sensor array (648x488). This is called pan/tilt function, and for this function, Row Starting Value, Column Starting Value,

Window Height Value, and Window Width Value are used. Panning window can be programmed as above. Two line pixel of each side produce black level data, and effective image array size 644 x 484. In general, color interpolation algorithm using 3x3 spatial mask for mosaic Color Filter Array(CFA) single sensor requires that pixels around the edge of a programmed image window are used for just color interpolation of neighbor pixels. Accounting for this fact, image array window should be programmed to larger value than the size that is to be displayed. For example, in order to make 640X480 24bit color image data, 642X482 pixel array is necessary. That is to say, you can use the window size as 642(Window Width)X482(Window Height) and you must use Row Address and Column Address from (3, 3) to (644, 484) for getting 642X482 raw image data.

TIMING CONTROL REGISTERS

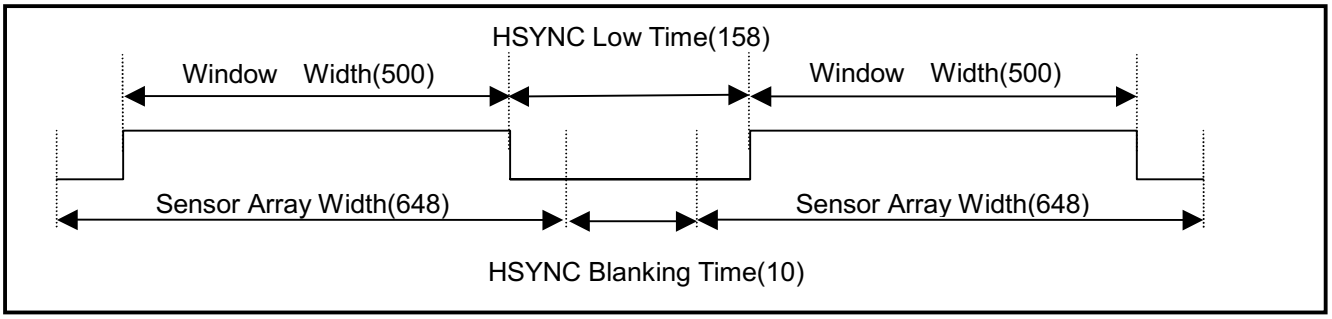
HSYNC Blanking Time Value Upper Byte[20H] – Read / Write — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	0	0	0	0	0	0	0

HSYNC Blanking Time Value Lower Byte[21H] – Read / Write — Default : 03H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	1	1

B<15:0> - HSYNC Blanking Time Value register defines data blank time between current line and next line by pixel clock unit. HSYNC Low Time is (Sensor Array Width – Window Width) plus HSYNC Blanking Time Value. For example, if Window Width = 500, HSYNC Blank = 10, then HSYNC Low Time is HSYNC Blank + (Sensor Array Width – Window Width), 10 + (648 – 500) = 158 clocks.



For more timing details, refer to Frame Timing Diagram section.

VSYNC Blanking Time Value Upper Byte[22H] – Read / Write — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	0	0	0	0	0	0	0

VSYNC Blanking Time Value Lower Byte[23H] – Read / Write — Default : 03H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	1	1

B<15:0> - The VSYNC Blanking Time register defines the active high duration of VSYNC output by pixel clock unit. The active high VSYNC indicates frame boundary between continuous frames. Programable range is from 3 to 2^{15} - 1. However, When VSYNC Blanking Time is over (Integration Time + 648 + HSYNC Blanking), VSYNC is appear after first frame. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing Diagram section.

Integration Time Value Upper Byte[25H] – Read / Write — Default : 06H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	1	1	0

Integration Time Value Middle Byte[26H] – Read / Write — Default : 1AH

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	1	1	0	1	0

Integration Time Value Lower Byte[27H] – Read / Write — Default : 80H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	1	0	0	0	0	0	0	0

B<23:0> -Integration Time Value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time in general film camera so that integration time need to be increased in dark environment and decreased in light environment. Unit of Integration time is main clock time unit. Because whole three bytes value are used for integration time, Maximum Integration Time Value(25H - 27H) is Maximum Value(2^{24}-1) * Clock Period. For example, if you use 10MHz MCLK, the total maximum integration time will be Maximum Value(2^{24}-1) * Clock Period(100ns) = 1.677sec

CHARATERISTICS ADJUSTMENT REGISTERS

Each sensor has a little different photo-diode characteristics due to power variation. The sensor provides registers that calibrate internal sensing circuit in order to get optimal performance.

Reset Level Value [30H] – Read / Write **Default : 38H**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	1	1	1	0	0	0

B<5:0> The purpose of the reset level control is to set the appropriate DC level to sampling hold of analog pixel output. The default value, [38H], is initial value to reset calibration. Refer to reset counter threshold value register[5BH] for reset level control.

We recommend the following procedure in case of manual setting:

Step1 : Check High Reset Counter Value

if > 0 Go to Step2

= 0 Go to Step 3

Step2 : Decrease Reset level(-2) and Go to step1

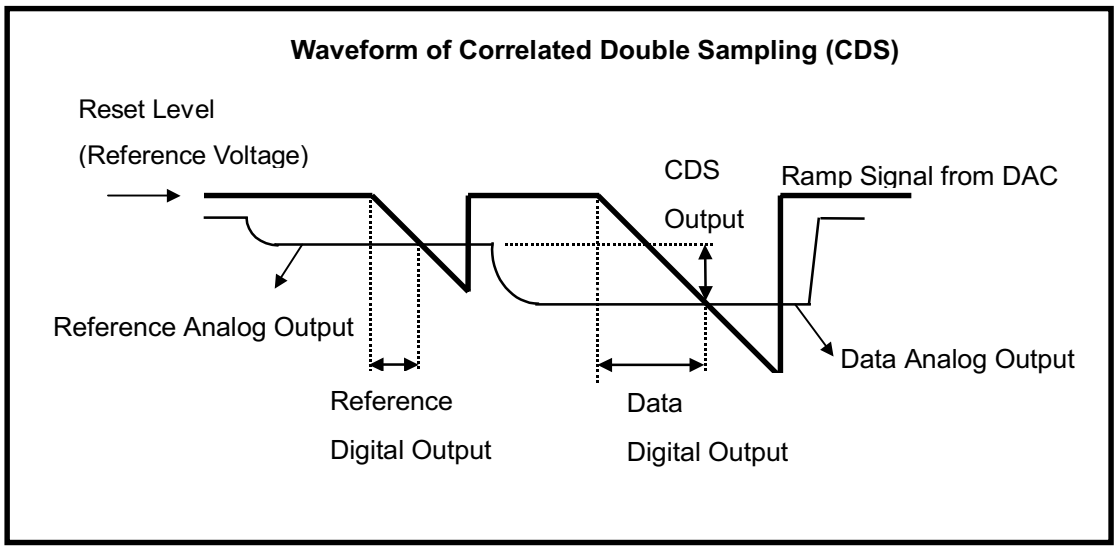
Step3 : Check Low Reset Counter Value

if > 0 Go to Step4

= 0 Go to Step 5

Step4 :Increase Reset Level(+2) and Go to Step3

Step5 : Finish



Red Color Gain Value [31H]– Read / Write — Default : 1EH

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	0	1	1	1	1	0

Green Color Gain Value[32H]– Read / Write — Default : 1EH

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	0	1	1	1	1	0

Blue Color Gain Value[33H]– Read / Write — Default : 1EH

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	0	1	1	1	1	0

B<5:0> Three Gain Mode:

There are three color gain registers for each R, G, and B pixels. These registers may be used for white balance and color effect with independent R, G, and B color gain control. Programmable value range is 0~63. However, we recommend that the range should be 30~63 for capturing good image quality.

B<5:0> One Gain Mode:

All three color gain values will be replaced by Green color gain value. If the gain register value is decreased, data output value is increased. That is, under low luminance light condition the pixel output is not enough to get right image so that we must amplify the output value by decreasing the gain value to get good image quality. In this case, auto white balance will be performed at image signal processor.

Pixel Bias Voltage Control Value[34H]– Read / Write — Default : 02H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	-	-	-	-	-	0	1	0

B<2:0> -The register controls bias current of load transistor sensing the pixel output. You should to set the default value.

RESET LEVEL STATISTICS REGISTER

Low Reset Counter Value Upper Byte[57H]– Read Only — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Low Reset Counter Value Lower Byte[58H]– Read Only — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

B<15:0>-This two-byte register has a value representing one eighth (1/8) of pixels that have reset count value less than 5 during one frame time and is updated when VSYNC gets active. With high reset counter value register it can be used as a parameter for external automatic reset level control logic that update the appropriate reset level register(30H) to automatically compensate chip to chip overall reset level variation.

High Reset Level Count Value Upper Byte[59H]– Read Only — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

High Reset Level Count Value Lower Byte[5AH]– Read Only — Default : 00H

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

B<15:0>-This two byte register has a value representing a eighth (1/8) of pixels that have reset count value larger than 123 during one frame time and is updated when VSYNC gets active. With low reset counter value register it can be used as a parameter for external automatic reset level control logic that update the appropriate reset level (30H) register to automatically compensate chip to chip overall reset level variation.

Reset Count Threshold Value [5BH]– Read/Write — Default : 0AH

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	1	0	1	0

B<7:0> - This register is used as a parameter for internal automatic reset level control. When you enable auto reset function of Mode C register, sensor compares Reset Counter Threshold Value(R_{th}) with Low Reset Counter Value(low count) and High Reset Counter Value(high count) and then adjust reset level as following cases. As R_{th} is increased, sensor converges to appropriate reset value with fast speed but accuracy is degraded. In other case, R_{th} is decreased, convergence of reset level in sensor is slower but accuracy is upgraded. Therefore, This register should be programmed to appropriate value except 0. We recommend that the range should be 1H for capturing good image quality.

Case1) low count > R_{th} and high count < R_{th}

Sensor increases the reset level internally because reset voltages of pixels are distributed at high voltage level.

Case2) low count < R_{th} and high count > R_{th}

Sensor decreases the reset level internally because reset voltages of pixels are distributed at low voltage level.

Case3) low count < R_{th} and high count < R_{th}

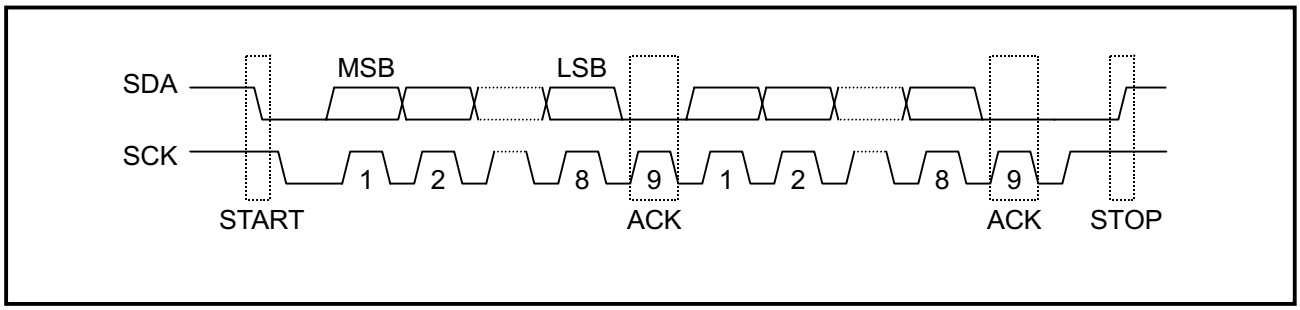
Sensor holds the reset level internally because reset voltages of pixels are distributed at appropriate voltage level.

Case4) low count > R_{th} and high count > R_{th}

Sensor holds the reset level internally because reset voltages of pixels are distributed at broad range. Because this case is extraordinary case, it seldom occurs. However, R_{th} should be increased to get the normal case.

I2C PROGRAMMING FOR CMOS IMAGE SENSOR

The serial bus interface consists of the SDA(serial data) and SCK(serial clock) pins. HV7131E1 Sensor can operate only as a slave. The SCK only controls the serial interface. However, MCLK should be supplied and RESET should be high signal during controlling the serial interface.



The Start condition is that logic transition (High to Low) on the SDA pin while the SCK pin is at high.

The Stop condition is that logic transition (Low to High) on the SDA pin while the SCK pin is at high.

To generate Acknowledge signal, the Sensor drives the SDA low when the SCK is high.

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an Acknowledge. The most significant bit of the byte should always be transmitted first.

SINGLE REGISTER BYTE PROGRAMMING

S	22H	A	01H	A	04H	A	P
*1	*2	*3	*4	*5	*6	*7	*8

Example) Set "Operating Mode" register into Window mode

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 04H [mode information]

*7. Read: acknowledge from sensor

*8. Drive: I^2C stop condition

MULTIPLE REGISTER BYTE PROGRAMMING USING AUTO INCREMENT MODE

S	22H	A	10H	A	00H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

You can program multiple configuration registers with single I2C bus cycle.

Example) Set "Row Start Address" register as 0003H

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 10H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 00H [row start address upper byte]

*7. Read: acknowledge from sensor

*8. Drive: 03H [row start address lower byte]

*9. Read: acknowledge from sensor

*10. Drive: I^2C stop condition

READING REGISTER VALUE

S	22H	A	30H	A	S	23H	A	Read Data	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Single Read or Auto-Increment Read

Example) Set "Reset Level Value" register

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 30H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

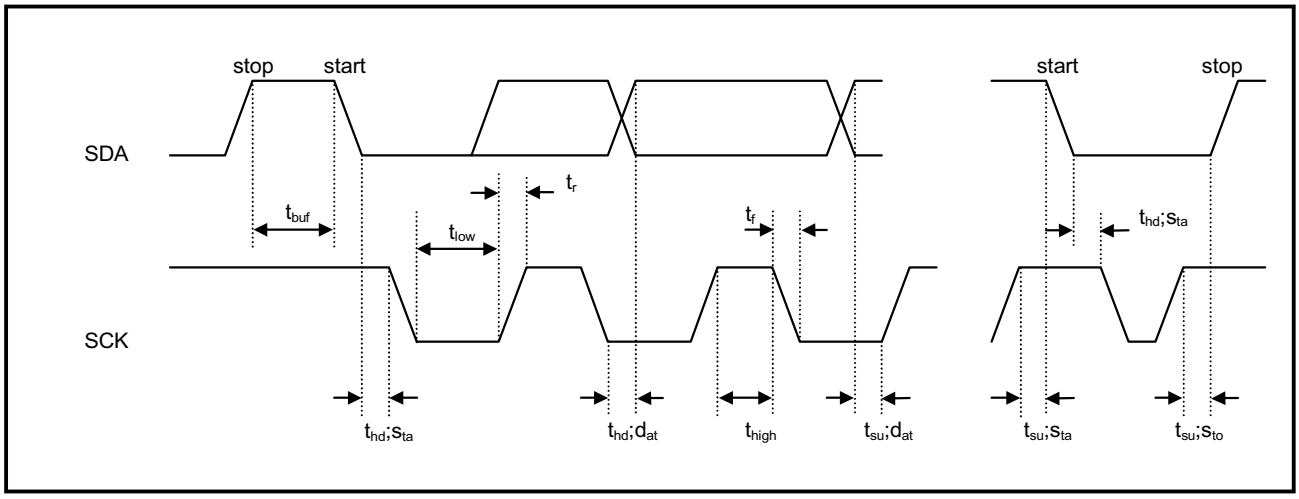
*8. Read: acknowledge from sensor

*9. Read: Read Data from sensor

*10. Drive: acknowledge to sensor(if there is no more read data Ack=1, else Ack=0)

*11. Drive: I^2C stop condition

I²C Bus Interface Timing



Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I²C bus must be free before a new transmission can start	t_{buf}	1.2	-	µs
Hold time for a START	$t_{hd};s_{ta}$	1.0	-	µs
LOW period of SCK	t_{low}	1.2	-	µs
HIGH period of SCK	t_{high}	1.0	-	µs
Setup time for START	$t_{su};s_{ta}$	1.2	-	µs
Data hold time	$t_{hd};d_{at}$	1.3	-	µs
Data setup time	$t_{su};d_{at}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2	-	µs
Capacitive load of each bus lines(SDA,SCK)	C_b	-	-	pF

FRAME TIMING DIAGRAMS

There are two Frame Timing cases.

Case 1) Integration Time <= Effective Window Height Time

Case 2) Integration Time > Effective Window Height Time

Effective Window Height Time = Window Height Value X (648 + HSYNC Blanking Time Value).

Each Frame Timing of the above cases may be decomposed into four timing segments.

1. Initial Data Setup Time: refer to following Figure 2
2. Data Line (Odd / Even) Time: 648 clocks + HSYNC Blanking time
3. Idle Time: 5120CLK for Case 1

   : Integration Time – Effective Window Height Time + 5120 clocks for Case 2
4. VSYNC Time: VSYNC Blanking Time

Note: Idle Time depends on the Frame Timing cases

FRAME TIMING DIAGRAM FOR CASE 1 (Integration Time <= Effective Window Height Time)

Frame timing related registers are programmed to suit for the above condition as follows

Row Starting Value = 3, Window Height = 482, HSYNC Blanking Time = 10,

Column Starting Value = 3, Window Width = 642, VSYNC Blanking Time = 3,

Integration Time = 300,000

From above registers value, we can calculate the Effective Window Height Time.

Effective Window Height Time = 482 X (648 + 10) clocks = 317,156 clocks

Because Effective Window Height Time is over Integration Time, Idle Time is 5,120 clocks and frame timing is as following figure.

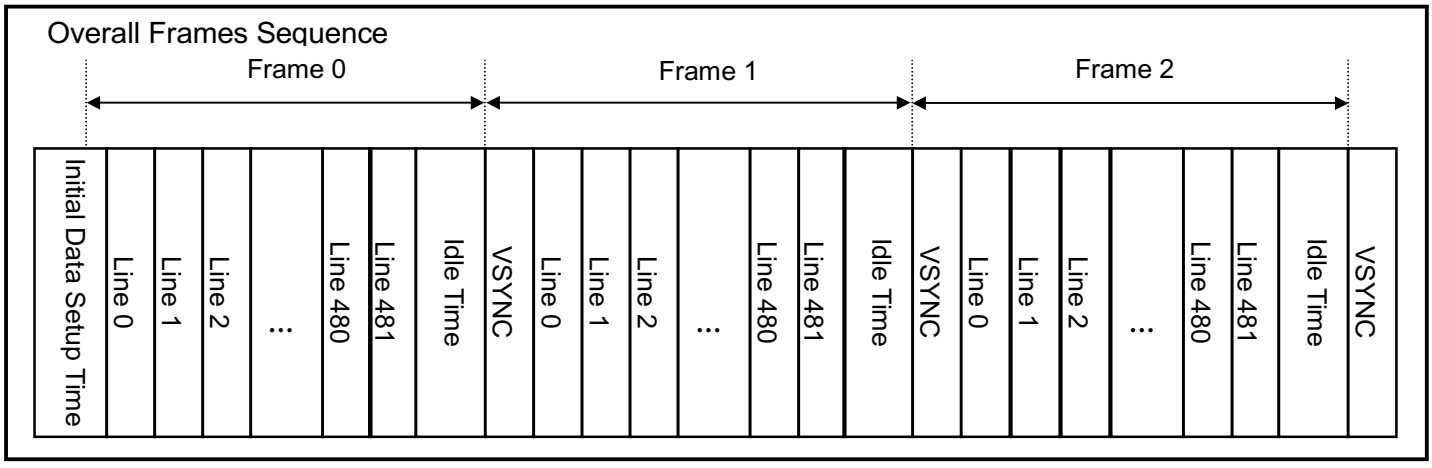


Fig. 1 Frame timing

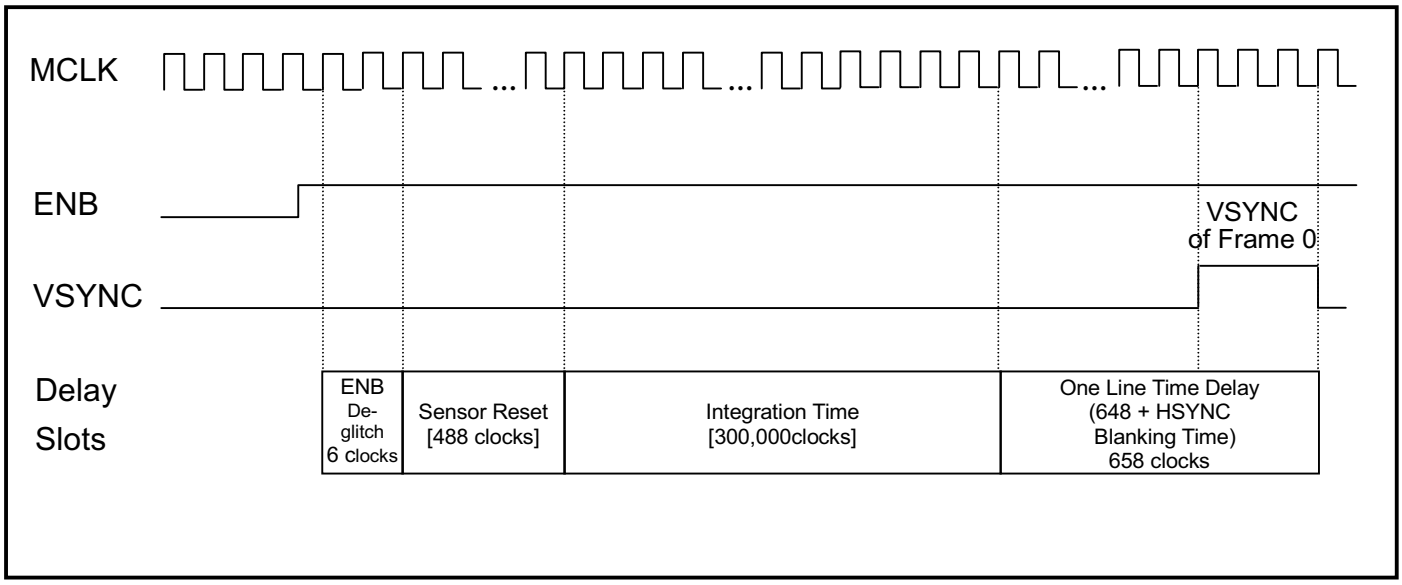


Fig. 2 Initial Data Setup Time after ENB gets active

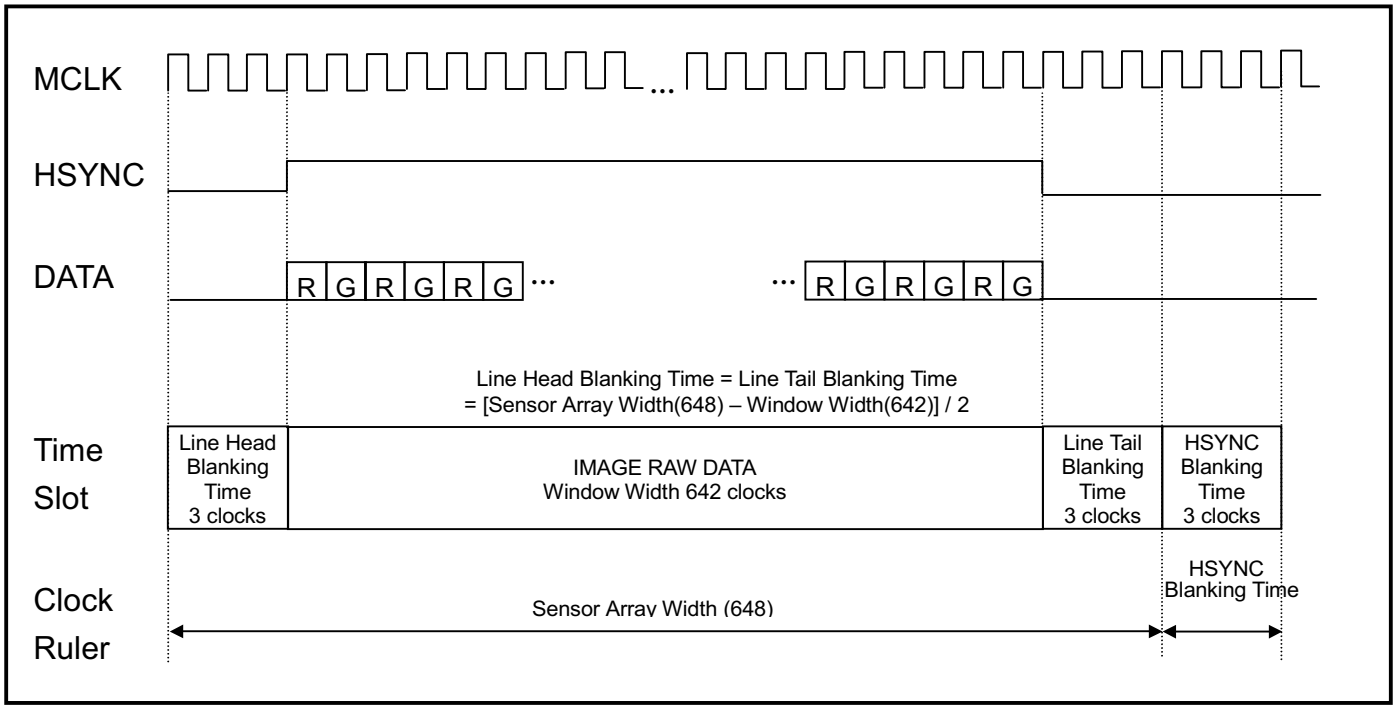


Fig. 3 Even Line Data Timing

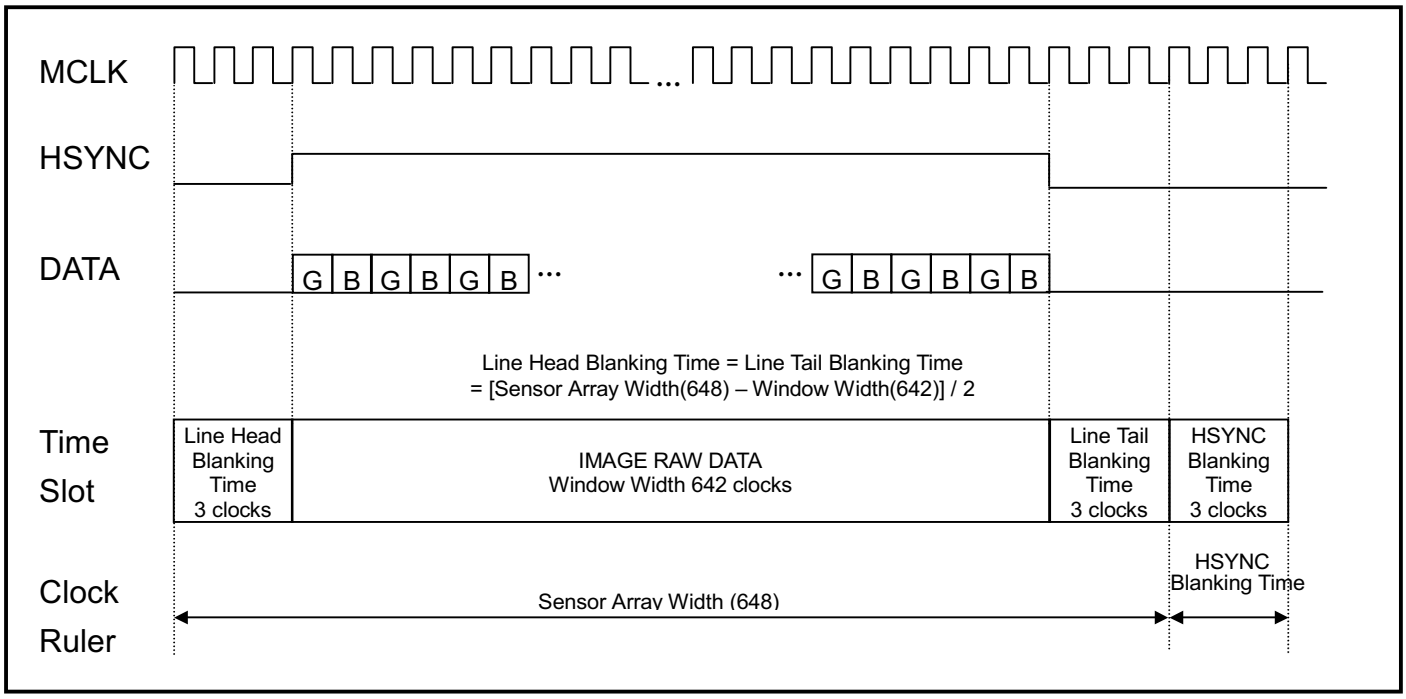


Fig.4 Odd Line Data Timing

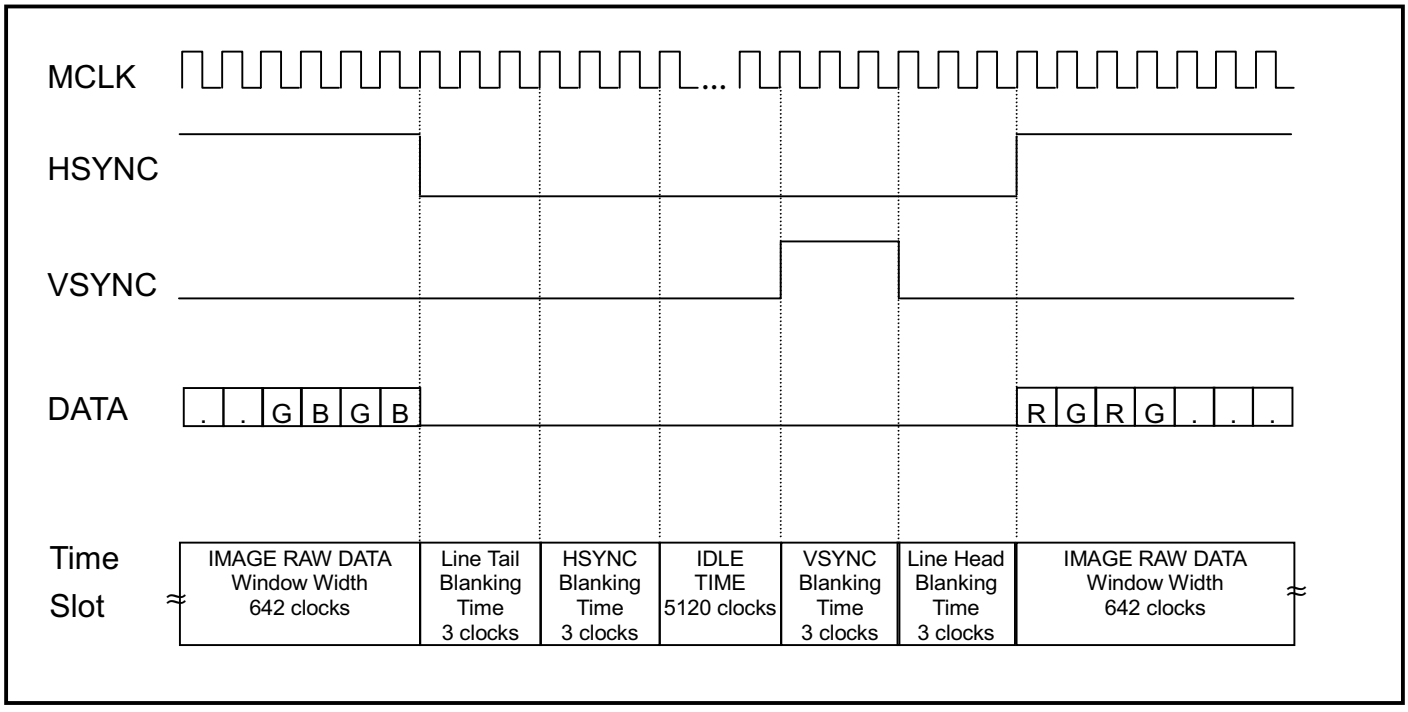


Fig.5 Frame Transition Timing

FRAME TIMING DIAGRAM FOR CASE 2 (Integration Time > Effective Window Height Time)

Frame timing related registers are programmed to suit for the above condition as follows

Row Starting Address = 3, Window Height = 482, HSYNC Blanking Time = 10,

Column Starting Address = 3, Window Width = 642, VSYNC Blanking Time = 3,

Integration Time = 400,000

From above registers value, we can calculate the Effective Window Height Time.

Effective Window Height Time = 482 X (648 + 10) clocks = 317,156 clocks

Because Integration Time is over Effective Window Height Time, Idle Time is 87,964(400,000 – 317,156 + 5120) clocks.

Timing Diagrams of Case 2 are as same as those of Case 1(Figure 1-5) except that idle time is 87,964 clocks and Integration Time is 400,000 clocks.

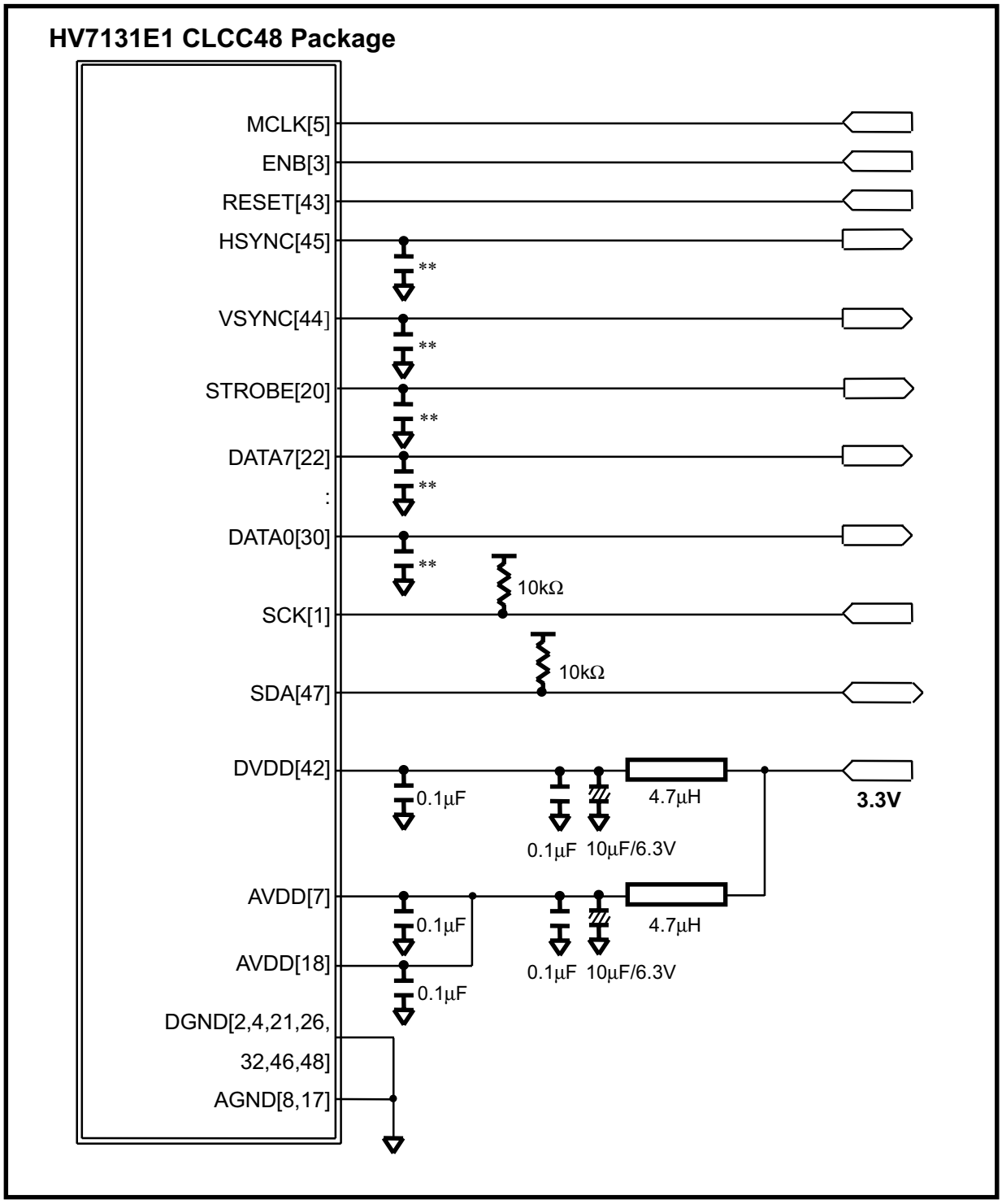
TYPICAL APPLICATION CIRCUIT

RECOMMENDED COMPONENTS SPECIFICATION

High Pass Filter	0.1μF Multi-Layer Ceramic Chip Capacitors(MLCC) Type
	Temperature Characteristics: Y5V(+22,-82%) or C0G(0+/-30ppm),
	Rated Voltage: 50V
Inductor	4.7μH(Leadless Magnetic Shielded Type)
	Tolerance: +/-5%
	Rated Current (max): 285mA
Electronic Capacitor	10μF/6.3V(Tantalum)
EMI Suppression(**)	Unknown

Notes On Use:

In order to reduce wiring impedance, use short, thick wires. In particular, locate and wire the high pass filter capacitor on each power pin as close as possible and strengthen the ground wiring sufficiently. Take care to ensure that external components absolute maximum ratings is not exceeded.



SOLDERING

SOLDER RE-FLOW EQUIPMENT

- (Preferred) 100% Convection re-flow system capable of maintaining the re-flow profiles required by EIA/JEDEC standard (JESD22-A113-B).
- VPR (Vapor Phase Re-flow) chamber capable of operating from 215 Celsius - 219 Celsius and/or (235±5) Celsius with appropriate fluids.
- Infrared (IR)/Convection solder re-flow equipment capable of maintaining the re-flow profiles required by EIA/JEDEC standard (JESD22-A113-B).

RE-FLOW PROFILE

	Convection or IR/Convection	VPR
Average ramp-up rate (183 Celsius to Peak)	3 Celsius/second max.	10 Celsius/second max.
Preheat temperature 125(±25) Celsius	120 second max.	
Temperature maintained above 183 Celsius	60-150 seconds	
Time within 5 Celsius of actual peak temperature	10-20 seconds	10 seconds
Peak temperature range	(220+5/-0) Celsius or (235+5/-0) Celsius	215-219 Celsius or (235+5/-0) Celsius
Ramp-down rate	6 Celsius/second max.	10 Celsius/second max.
Time 25 Celsius to peak temperature	6 minutes max.	

FLUX APPLICATION

After the re-flow solder cycles are completed, allow the devices to cool at room ambient for 15 minutes minimum. Apply an activated water-soluble flux to the device leads by bulk immersion of the entire parts in flux at room ambient for 10 seconds minimum.

CLEANING

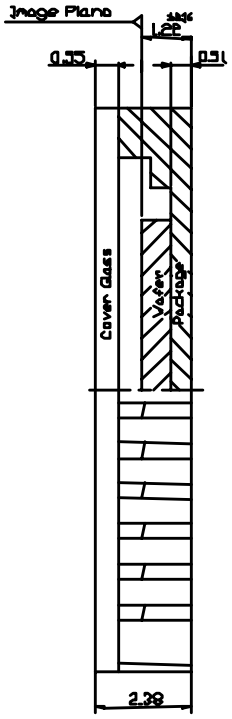
Clean devices externally using multiple agitated de-ionized water rinses. No waiting time is required between flux application and cleaning

DRYING

Devices should be dried at room ambient prior to submission to reliability testing.

PACKAGE DISMENSION

(48 PIN CLCC) UNIT: mm



MEMO

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