

Eight-Channel, High Speed, $\pm 60V$, $\pm 1.0A$, Ultrasound RTZ Pulser

Features

- ▶ HVCMOS technology for high performance
- ▶ High density integrated ultrasound transmitter
- ▶ 0 to $\pm 60V$ output voltage
- ▶ $\pm 1.0A$ source and sink current in pulse mode
- ▶ $\pm 1.0A$ source and sink current in RTZ mode
- ▶ Up to 20MHz operating frequency
- ▶ Matched delay times
- ▶ Optional clock re-alignment
- ▶ 3.3V CMOS logic interface and reference
- ▶ +3.3V low voltage supply for V_{DD}
- ▶ Built-in linear regulators for floating gate driver
- ▶ Built-in output drain diodes & bleed resistors

Application

- ▶ Portable medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Pulse waveform generator

General Description

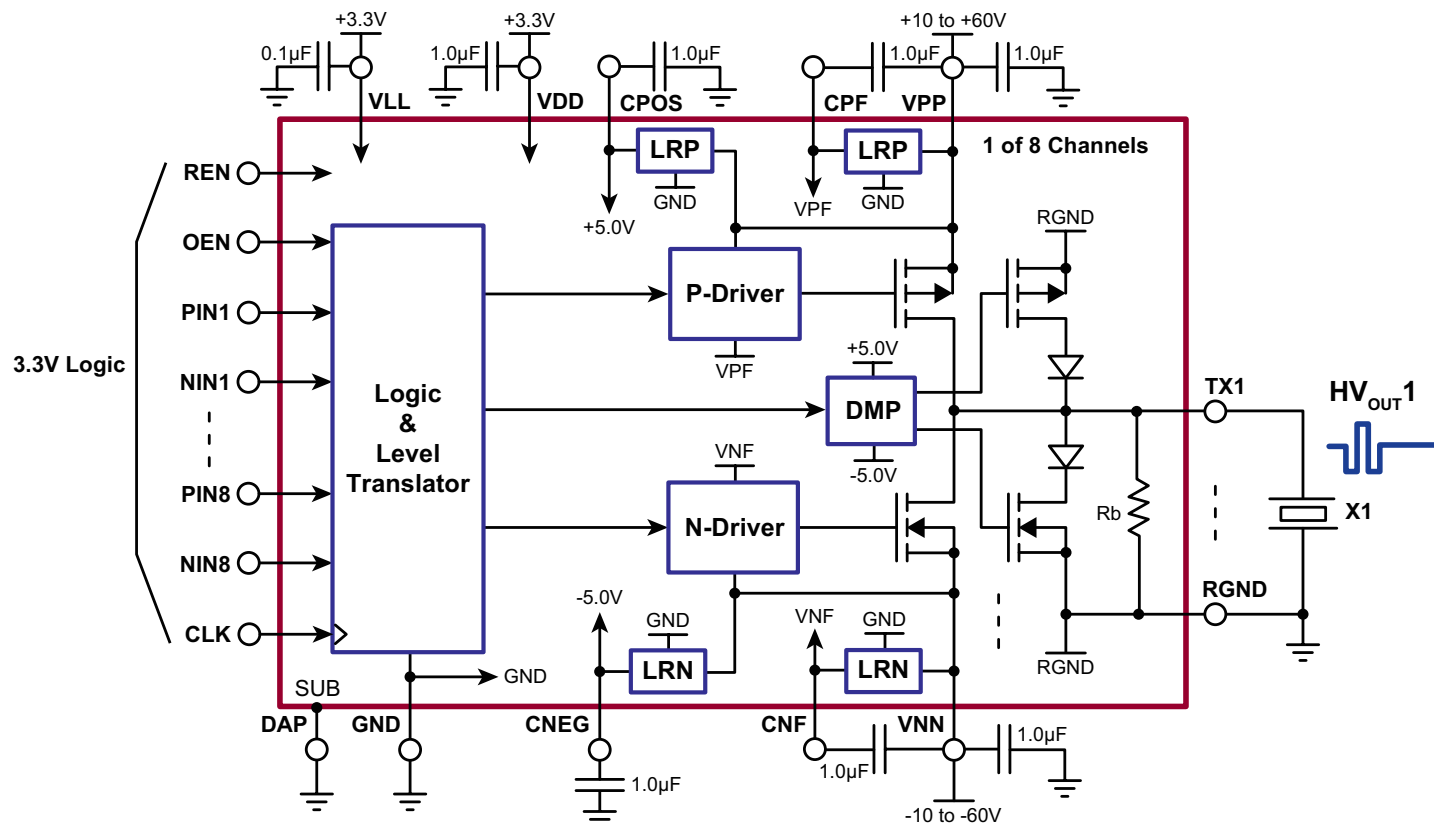
The Supertex HV7350 is an eight channel monolithic high voltage high-speed pulse generator with built-in fast return to zero damping FETs. This high voltage and high-speed integrated circuit is designed for portable medical ultrasound image devices.

HV7350 consists of a controller logic interface circuit, level translators, MOSFET gate drives, and high current power P-channel and N-channel MOSFETs as the output stage for each channel.

The output peak currents of each channel are guaranteed to be over $\pm 1.0A$ with up to $\pm 60V$ pulse swings as well as return-to-zero (RTZ) mode. The gate drivers for the output MOSFETs are powered by built-in linear 5.0V regulators referenced to V_{PP} and V_{NN} . This direct coupling topology of the gate drivers not only saves four floating voltage supplies or AC coupling capacitors per channel, but also makes the PCB layout smaller and easier.

An input clock pin is available to realign all the logic input control lines to a master clock. Precise logic timing is always essential in any ultrasound systems.

Typical Application Circuit



Ordering Information

| Part Number | Package | Packing |
|-----------------|-------------------|-----------|
| HV7350K6-G | 56-Lead (8x8) QFN | 250/ Tray |
| HV7350K6-G M937 | 56-Lead (8x8) QFN | 2000/Reel |

-G denotes a lead (Pb)-free / RoHS compliant package



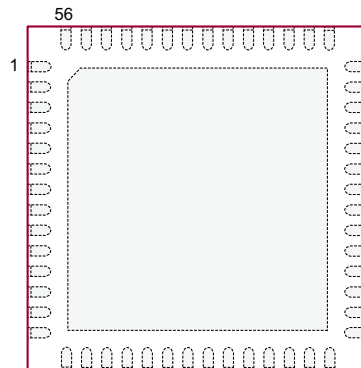
ESD Sensitive Device

Absolute Maximum Ratings

| Parameter | Value |
|--|----------------|
| V _{SUB} , substrate voltage is GND | 0V |
| V _{LL} , Positive logic supply | -0.5V to +5.5V |
| V _{DD} , Positive logic and level translator supply | -0.5V to +5.5V |
| C _{POS} to GND, Positive level translator circuit | -0.5V to +5.5V |
| C _{NEG} to GND, Negative level translator circuit | +0.5V to -5.5V |
| (V _{PP} - C _{PF}), Positive gate driver circuit | -0.5V to +5.5V |
| (C _{NF} - V _{NN}), Negative gate driver circuit | -0.5V to +5.5V |
| (V _{PP} - V _{NN}) Differential high voltage supply | +130V |
| V _{PP} , High voltage positive supply | -0.5V to +65V |
| V _{NN} , High voltage negative supply | +0.5V to -65V |
| All logic input PIN _x , NIN _x , OEN and REN voltages | -0.5V to +5.5V |
| Operating temperature | -40°C to 125°C |
| Storage temperature | -65°C to 150°C |

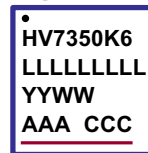
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



56-Lead QFN
(top view)

Package Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
— = "Green" Packaging

Package may or may not include the following marks: Si or

56-Lead QFN

Typical Thermal Resistance

| Package | θ_{ja} |
|-------------------|---------------|
| 56-Lead (8x8) QFN | 21°C/W |

Output Current & R_{on}

| I _{SC} | R _{onP} | R _{onN} | I _{DMP} | R _{onDP} | R _{onDN} |
|-----------------|------------------|------------------|------------------|-------------------|-------------------|
| 1.5A | 13Ω | 6.5Ω | 1.5A | 13Ω | 8.0Ω |

Notes:

1. V_{PP}/V_{NN} = +/-60V, V_{DD} = +3.3V; REN = 1
2. I_{SC} is current into 1.0Ω to GND;

3. I_{DMP} is current from +/-30V connected to T_x pin.
4. Max pulse width for current measurement on T_x pin is 100ns.

Power-Up Sequence

| Step | Description |
|------|---------------------------------------|
| 1 | V _{LL} with logic signal low |
| 2 | V _{DD} |
| 3 | REN = 1 (external supplies on) |
| 4 | V _{PP} and V _{NN} |
| 5 | Logic control signals active |

Note:

Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering up/down sequence is only recommended in order to minimize possible inrush current.

Power-Down Sequence

| Step | Description |
|------|-------------------------------------|
| 1 | All logic signals go to low |
| 2 | V _{PP} and V _{NN} |
| 3 | REN = 0 (external supplies off) |
| 4 | V _{DD} |
| 5 | V _{LL} |

Operating Supply Voltages and Current (Eight Active Channels)

(Operating conditions, unless otherwise specified, $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|------------------------------|------|------|------|---------|--|
| V_{DD} | V_{DD} voltage supply | 2.97 | 3.30 | 5.20 | V | --- |
| $UVLO_{DD}$ | V_{DD} UVLO | 2.30 | 2.60 | 2.80 | V | --- |
| V_{LL} | Logic voltage reference | 2.50 | 3.30 | 5.00 | V | --- |
| $UVLO_{LL}$ | V_{LL} UVLO | 1.30 | 1.55 | 1.70 | V | --- |
| V_{PP} | Positive high voltage supply | +10 | - | +60 | V | --- |
| V_{NN} | Negative high voltage supply | -60 | - | -10 | V | --- |
| I_{LLQ} | V_{LL} current | - | 8.0 | - | μA | OEN = REN = 0 |
| I_{DDQ} | V_{DD} current | - | 1.0 | - | | |
| I_{PPQ} | V_{PP} current | - | 5.0 | 10 | | |
| I_{NNQ} | V_{NN} current | - | 5.0 | 10 | | |
| I_{LLEN} | V_{LL} current | - | 13 | 20 | μA | OEN = REN = 1 5.0ms after f = 0MHz |
| I_{DDEN} | V_{DD} current | - | 480 | 700 | | |
| I_{PPEN} | V_{PP} current | - | 220 | 350 | | |
| I_{NNEN} | V_{NN} current | - | 300 | 400 | | |
| I_{DDCW} | V_{DD} current | - | 2.3 | - | mA | f = 5.0MHz, Continuous, no loads, for calculation reference only. |
| I_{PPCW} | V_{PP} current | - | 80 | - | | |
| I_{NNCW} | V_{NN} current | - | 80 | - | | |
| $I_{LL,CLK}$ | V_{LL} current | - | 33 | - | μA | $f_{CLK} = 10MHz$, PIN = NIN = 0 |

Electrical Characteristics

(Operating conditions, unless otherwise specified, $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$)

Pulsar P-Channel MOSFET

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|---------------------------|-----|------|-----|----------|------------------|
| I_{OUT} | Output saturation current | 1.0 | 1.5 | - | A | --- |
| R_{ON} | Channel resistance | - | 13.2 | - | Ω | $I_{SD} = 100mA$ |

Pulsar N-Channel MOSFET

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|---------------------------|-----|-----|-----|----------|------------------|
| I_{OUT} | Output saturation current | 1.0 | 1.5 | - | A | --- |
| R_{ON} | Channel resistance | - | 8.0 | - | Ω | $I_{SD} = 100mA$ |

Damping P-Channel MOSFET

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|---------------------------|-----|-----|-----|----------|------------------|
| I_{OUT} | Output saturation current | 1.0 | 1.5 | - | A | --- |
| R_{ON} | Channel resistance | - | 13 | - | Ω | $I_{SD} = 100mA$ |

Damping N-Channel MOSFET

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|---------------------------|-----|-----|-----|----------|------------------|
| I_{OUT} | Output saturation current | 1.0 | 1.5 | - | A | --- |
| R_{ON} | Channel resistance | - | 9.0 | - | Ω | $I_{SD} = 100mA$ |

Logic Inputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--------------------------|--------------------|-----|--------------------|---------|--------------------------|
| V_{IH} | Input logic high voltage | $0.7 \cdot V_{LL}$ | - | V_{LL} | V | $V_{LL} = 2.5$ to $3.3V$ |
| V_{IL} | Input logic low voltage | 0 | - | $0.3 \cdot V_{LL}$ | V | |
| V_{IH} | Input logic high voltage | $0.8 \cdot V_{LL}$ | - | V_{LL} | V | $V_{LL} = 5.0V$ |
| V_{IL} | Input logic low voltage | 0 | - | $0.2 \cdot V_{LL}$ | V | |
| I_{IH} | Input logic high current | - | - | 10 | μA | --- |
| I_{IL} | Input logic low current | -10 | - | - | μA | --- |
| C_{IN} | Input logic capacitance | - | - | 5.0 | pF | --- |

MOSFET Drain Bleed Resistor

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-------------|-----------------------------|-----|-----|-----|------------|------------|
| R_{B1-8} | Output Bleed Resistance | 12 | 17 | 25 | k Ω | --- |
| P_{RB1-8} | Bleed Resistors Power Limit | - | - | 50 | mW | --- |

AC Electrical Characteristics

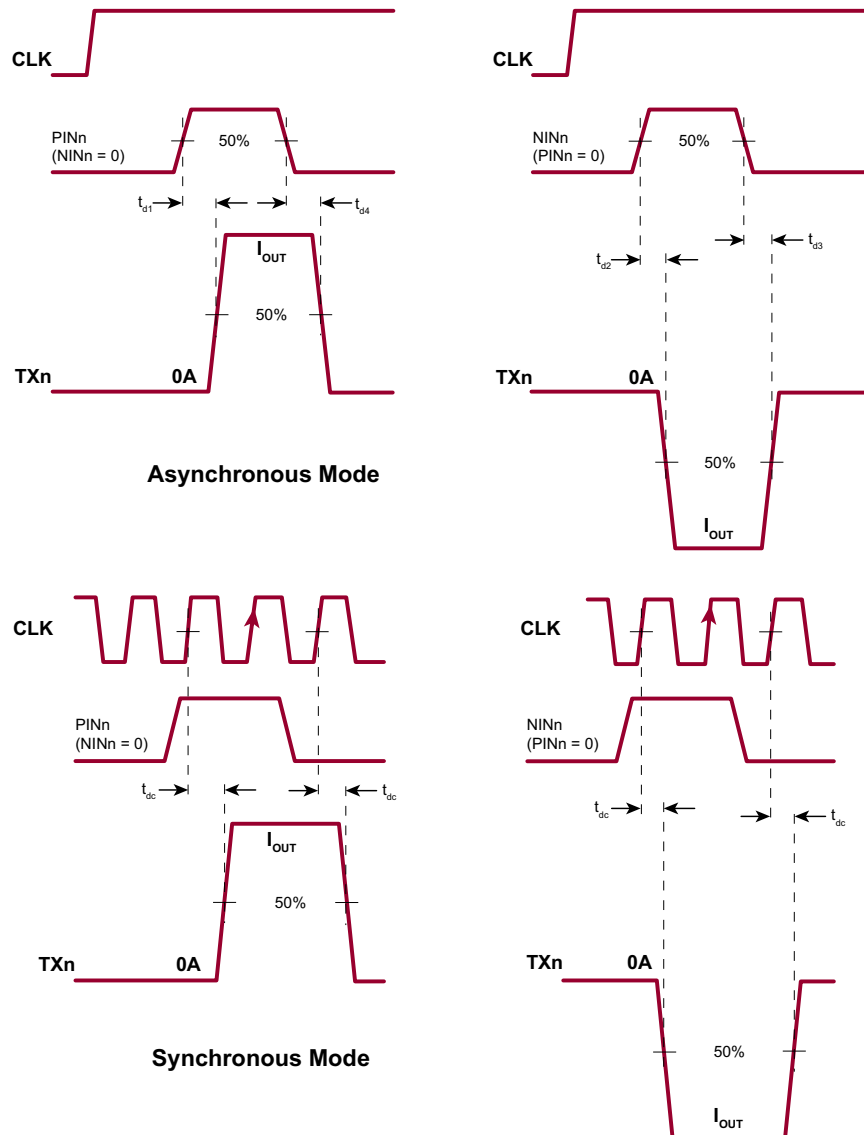
(Operating conditions, unless otherwise specified, $V_{LL} = +3.3V$, $V_{DD} = +3.3V$, $V_{PP} = +60V$, $V_{NN} = -60V$, $V_{CLK} = +3.3V$, $T_A = 25^\circ C$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------------|-------------------------------------|-----|-----------|-----|---------|--|
| t_r | Output rise time | - | 30 | - | ns | 330pF//2.5k Ω load 10 - 90% |
| t_f | Output fall time | - | 30 | - | ns | |
| t_{EN} | Enable time | - | 300 | 500 | μs | Cap value see page 1 diagram. OEN = REN |
| t_{DIS} | Disable time | - | 2.8 | 10 | μs | |
| t_{d1} | Delay time on PIN _x rise | - | 12 | - | ns | 1.0 Ω resistor load, D%<1% (See timing diagram) 50% inputs to 50% T _x current |
| t_{d2} | Delay time on NIN _x rise | - | 12 | - | | |
| t_{d3} | Delay time on damping rise | - | 12 | - | | |
| t_{d4} | Delay time on damping fall | - | 12 | - | | |
| t_{dc} | Delay time on CLK rise | - | 9.0 | - | | |
| Δt_{DELAY} | Delay time matching | - | ± 3.0 | - | ns | P to N, channel to channel |
| t_j | Delay jitter on rise or fall | - | TBD | - | ps | $V_{PP}/V_{NN} = +/-25V$, input tr 50% to HV _{OUT} t_r or t_f 50%, with 330pF//2.5k Ω load |
| t_{rr} | RTZ FETs drain diode t_{rr} | - | 25 | - | ns | $I_F = 1.0A$, $I_R = 1.0A$, $R_L = 10\Omega$ |
| f_{CLK} | Re-timing clock frequency | 10 | 220 | - | MHz | --- |
| t_{RC} , t_{FC} | Re-timing clock rise & fall times | - | 0.5 | 5.0 | ns | --- |
| t_{su} | Set-up time, PIN/NIN to CLK | 2.0 | - | - | ns | --- |
| t_H | Hold time, CLK to PIN/NIN | 1.0 | - | - | ns | --- |
| t_{CLK_LO} | Clock time low | 2.0 | - | 100 | ns | CLK input must have at least one pulse before PIN and NIN inputs are not zero. Be sure to return inputs to zero before stopping clock. |
| t_{CLK_HI} | Clock time high | 2.0 | - | 100 | ns | |
| t_{CLK_REC} | Clock recognition time | - | 2.0 | - | ns | |
| t_{CLK_RLS} | Clock release time | 150 | 300 | 800 | ns | |
| f_{OUT} | Output frequency range | - | - | 20 | MHz | 100 Ω resistor load |
| HD2 | Second harmonic distortion | - | -40 | - | dB | |
| C_{OSS} | Output capacitance | - | 50 | - | pF | $V_{DS} = 25V$, $f = 1.0MHz$, of T _x pin total |

Truth Table

| Logic Inputs | | | | TX _n Output | | | Note |
|--------------|-----|------------------|------------------|------------------------|-----|------|---|
| OEN | CLK | PIN _x | NIN _x | VPP | VNN | RGND | |
| 1 | VLL | 0 | 0 | OFF | OFF | ON | Asynchronous Mode Output change on PIN/NIN |
| 1 | VLL | 1 | 0 | ON | OFF | OFF | |
| 1 | VLL | 0 | 1 | OFF | ON | OFF | |
| 1 | VLL | 1 | 1 | OFF | OFF | OFF | |
| 1 | ⌄ | 0 | 0 | OFF | OFF | ON | Synchronous Mode Output change at retiming clock(CLK) rising edge, registered by PIN/NIN |
| 1 | ⌄ | 1 | 0 | ON | OFF | OFF | |
| 1 | ⌄ | 0 | 1 | OFF | ON | OFF | |
| 1 | ⌄ | 1 | 1 | OFF | OFF | OFF | |
| 0 | X | X | X | OFF | OFF | OFF | Disabled |

Switching Time Diagram



Pin Description

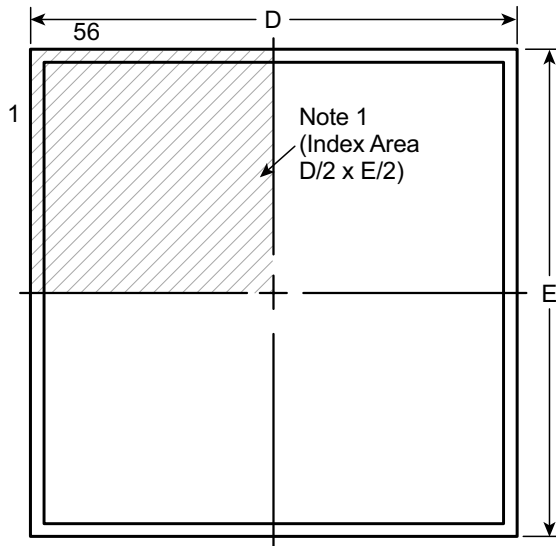
| Pin | Name | Description |
|-----|------|---|
| 1 | PIN2 | Input logic control of high voltage output P-FET for channel 2, Hi = on, Low = off. (see logic table) |
| 2 | NIN2 | Input logic control of high voltage output N-FET for channel 2, Hi = on, Low = off. (see logic table) |
| 3 | PIN3 | Input logic control of high voltage output P-FET for channel 3, Hi = on, Low = off. (see logic table) |
| 4 | NIN3 | Input logic control of high voltage output N-FET for channel 3, Hi = on, Low = off. (see logic table) |
| 5 | PIN4 | Input logic control of high voltage output P-FET for channel 4, Hi = on, Low = off. (see logic table) |
| 6 | NIN4 | Input logic control of high voltage output N-FET for channel 4, Hi = on, Low = off. (see logic table) |
| 7 | OEN | Output enable Hi = on, Low = off. See logic truth table |
| 8 | REN | Built-in positive and negative 5V voltage regulators enable. Hi = on, Low = off. If REN = 0, external floating 5V power supplies may be supplied across CPF, CNF CPOS and CNEG capacitors |
| 9 | PIN5 | Input logic control of high voltage output P-FET for channel 5, Hi = on, Low = off. (see logic table) |
| 10 | NIN5 | Input logic control of high voltage output N-FET for channel 5, Hi = on, Low = off. (see logic table) |
| 11 | PIN6 | Input logic control of high voltage output P-FET for channel 6, Hi = on, Low = off. (see logic table) |
| 12 | NIN6 | Input logic control of high voltage output N-FET for channel 6, Hi = on, Low = off. (see logic table) |
| 13 | PIN7 | Input logic control of high voltage output P-FET for channel 7, Hi = on, Low = off. (see logic table) |
| 14 | NIN7 | Input logic control of high voltage output N-FET for channel 7, Hi = on, Low = off. (see logic table) |
| 15 | PIN8 | Input logic control of high voltage output P-FET for channel 8, Hi = on, Low = off. (see logic table) |
| 16 | NIN8 | Input logic control of high voltage output N-FET for channel 8, Hi = on, Low = off. (see logic table) |
| 17 | VLL | Logic supply voltage and reference input (+3.3V) |
| 18 | GND | Logic and circuit return ground (0V) |
| 19 | VDD | Positive voltage power supply (+3.3V) |
| 20 | VPP | Positive high voltage power supply (+10 to +60V) |
| 21 | VPP | |
| 22 | VPP | |
| 23 | CPF | Built-in linear voltage VPF regulator output decoupling capacitor pin, 1uF from VPP to CPF per each |
| 24 | CNF | Built-in linear voltage VNF regulator output decoupling capacitor pin, 1uF from CNF to VNN per each |
| 25 | VNN | Negative high voltage power supply (-10 to -60V) |
| 26 | VNN | |
| 27 | VNN | |
| 28 | TX8 | T _x pulser channel 8 output |
| 29 | RGND | Damping ground and bleed resistors common return ground |
| 30 | TX7 | T _x pulser channel 7 output |
| 31 | RGND | Damping ground and bleed resistors common return ground |
| 32 | TX6 | T _x pulser channel 6 output |

Pin Description (cont.)

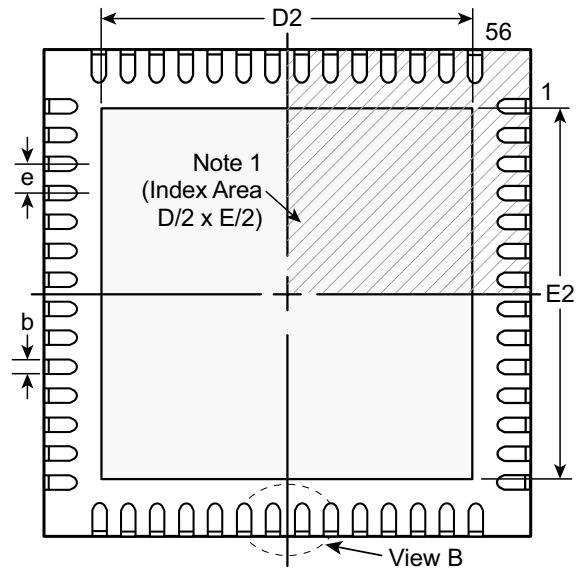
| Pin | Name | Description |
|--------------------|------|---|
| 33 | RGND | Damping ground and bleed resistors common return ground |
| 34 | TX5 | T _x pulser channel 5 output |
| 35 | CNEG | Built-in linear voltage -5V regulator output decoupling capacitor pin, 1.0uF from CNEG to GND |
| 36 | CPOS | Built-in linear voltage +5V regulator output decoupling capacitor pin, 1.0uF from CPOS to GND |
| 37 | TX4 | T _x pulser channel 4 output |
| 38 | RGND | Damping ground and bleed resistors common return ground |
| 39 | TX3 | T _x pulser channel 3 output |
| 40 | RGND | Damping ground and bleed resistors common return ground |
| 41 | TX2 | T _x pulser channel 2 output |
| 42 | RGND | Damping ground and bleed resistors common return ground |
| 43 | TX1 | T _x pulser channel 1 output |
| 44 | VNN | Negative high voltage power supply (-10 to -60V) |
| 45 | VNN | |
| 46 | VNN | |
| 47 | CNF | Built-in linear voltage VNF regulator output decoupling capacitor pin, 1uF from CNF to VNN per each |
| 48 | CPF | Built-in linear voltage VPF regulator output decoupling capacitor pin, 1uF from VPP to CPF per each |
| 49 | VPP | Positive high voltage power supply (+10 to +60V) |
| 50 | VPP | |
| 51 | VPP | |
| 52 | VDD | Positive voltage power supply (+3.3V) |
| 53 | GND | Logic and circuit return ground (0V) |
| 54 | CLK | Re-timing register clock input. Connect to V _{LL} to disable the re-timing function |
| 55 | PIN1 | Input logic control of high voltage output P-FET for channel 1, Hi = on, Low = off. (see logic table) |
| 56 | NIN1 | Input logic control of high voltage output N-FET for channel 1, Hi = on, Low = off. (see logic table) |
| VSUB (Thermal Pad) | | Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to GND (0V) externally |

56-Lead QFN Package Outline (K6)

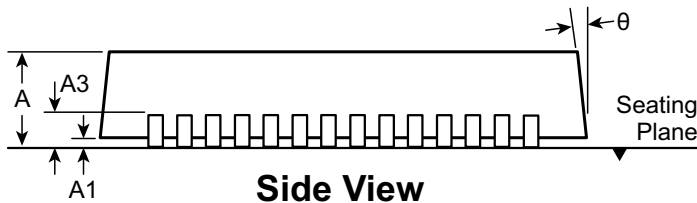
8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



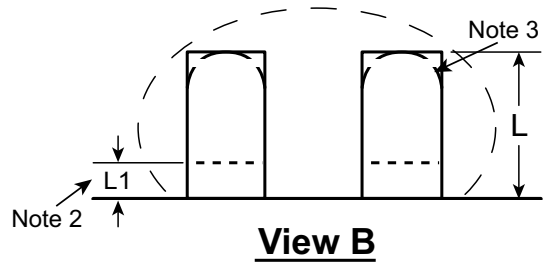
Top View



Bottom View



Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ | |
|----------------|-----|------|------|----------|------|-------|-------|-------|-------|----------|------|------|-----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 7.85* | 2.75 | 7.85* | 2.75 | 0.50 BSC | 0.30 | 0.00 | 0° |
| | NOM | 0.90 | 0.02 | | 0.25 | 8.00 | 5.70 | 8.00 | 5.70 | | 0.40 | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 8.15* | 6.70† | 8.15* | 6.70† | | 0.50 | 0.15 | 14° |

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-56QFNK68X8P050, Version A031010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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