High Voltage, Dimmable EL Lamp Driver

Features

- $360V_{PP}$ output voltage for high brightness
- Large output load capability of up to 150nF
- 2.7 to 5.5V operating supply voltage
- Single lithium ion cell compatible
- Adjustable output regulation for dimming
- External switching MOSFET
- Low audible noise
- Output discharge slew rate control
- 1.5V logic
- Dedicated Enable pin
- Two EL frequency controls
- Independent lamp and converter frequency setting
- Split supply capability
- Available in 16-Lead 4x4 QFN package

Applications

- Laptop keyboards
- Netbook keyboards
- Display signs
- Portable instrumentation equipment
- Electronic organizers

General Description

The Supertex HV816 is a high voltage Electroluminescent (EL) lamp driver designed for driving a lamp capacitance of up to 150nF, or an area of approximately 42 square inches. It is comprised of a boost converter followed by an H-bridge. The boost converter produces a regulated output voltage, which is set at a nominal value of 180V using an internal reference voltage. The H-bridge is used to produce a differential output drive and the EL lamp will therefore see ±180V (360V peak-to-peak). The HV816 has two internal oscillators, one for controlling the boost converter switching frequency and the other for controlling the H-bridge switching frequency. Having separate control of each switching frequency allows flexibility in the circuit design.

The operating input supply voltage is 2.7 to 5.5V, but the Enable (EN) and Select (SEL) interface to the device will accept logic high levels down to 1.5V. The EN input is for turning the device ON and OFF. The SEL input is for external logic control of the H-bridge switching frequency, if required.

The HV816 boost converter stage uses a single inductor and a minimum number of external components. The input voltage to the inductor can be different from the input voltage to the HV816 (split supply). The external inductor is connected either between the LX and VDD pins or, for split supply applications, between the LX pin and a higher voltage supply (shown as V_{IN} in the Block Diagram). An external MOSFET has to be driven by the switch oscillator to generate a high voltage. The switching frequency for this MOSFET is set by an external resistor connected between the RSW-Osc pin and the supply pin VDD. During operation, the external switching MOSFET turns on and allows energy to be stored in the inductor; this energy is transferred into the capacitor C_S when the MOSFET turns off. The voltage at the CS pin will increase with every switching cycle. Once the voltage at the CS pin reaches the desired regulation limit, nominally 180V, the external switching MOSFET is turned OFF to conserve power.

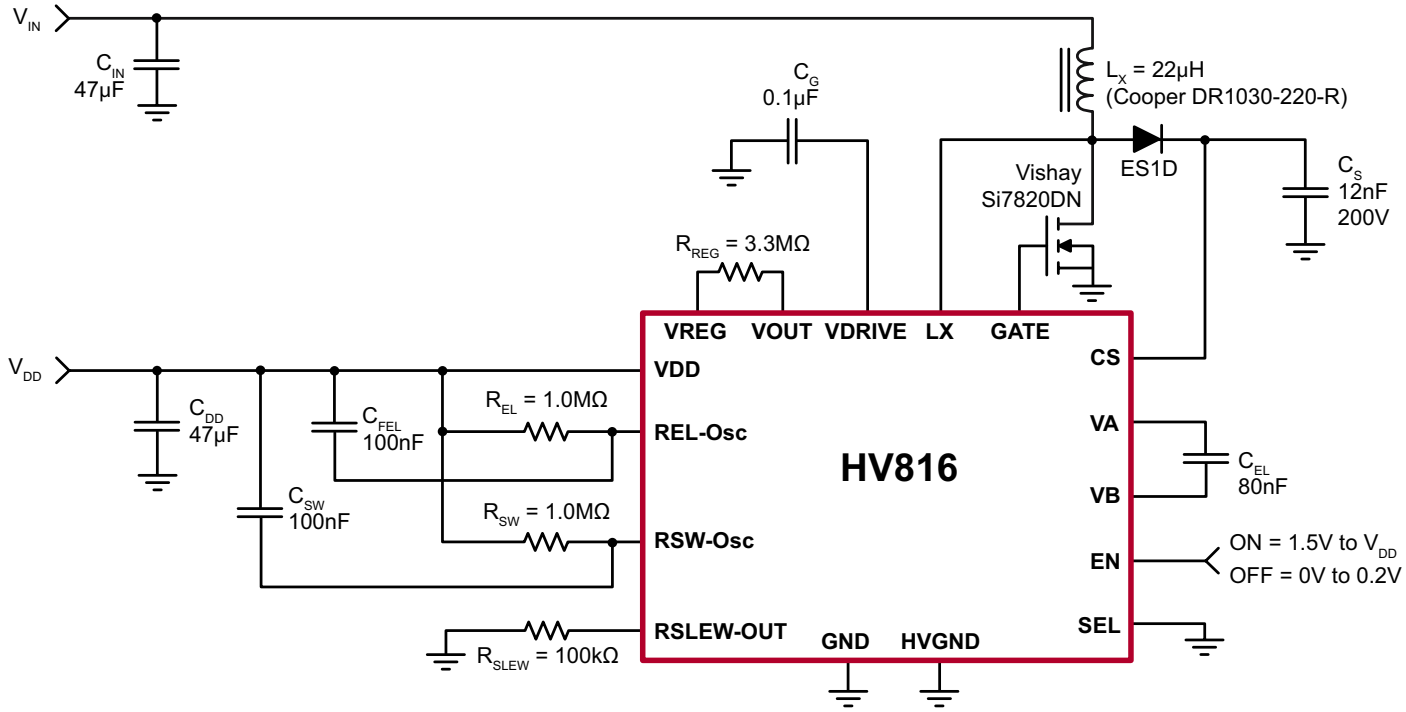
The C_S capacitor is connected between the CS pin and ground; the CS pin is internally connected to the H-bridge. Energy from the boost converter stage is stored in the capacitor before being transferred to the EL lamp. Depending on the EL lamp sizes, a 1.0nF to 15nF capacitor should be used for C_S.

The EL lamp switching frequency can be in the range of 100Hz to 1.0kHz. This frequency can be set by either an external logic signal at the SEL pin, with a frequency that is 4 times the desired EL lamp switching frequency, or by an external resistor connected between the REL-Osc and VDD pins. If external frequency is input to the device at the SEL pin, the REL-Osc pin should be connected to ground.

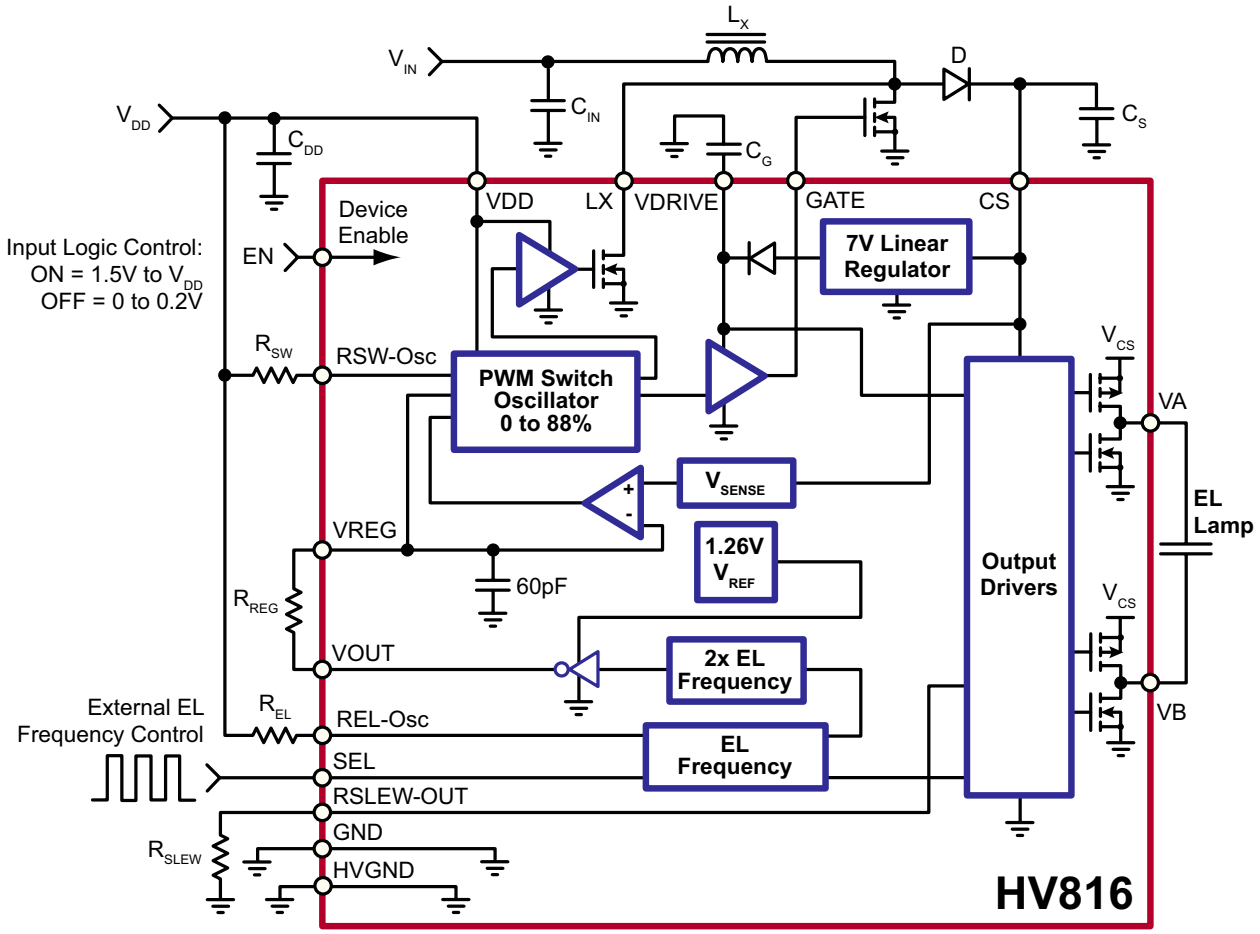
The HV816 has the provision to control the discharge rate of the output to minimize audible noise emitted by the EL lamp, which is connected between the VA and VB pins. An external resistor from the RSLEW-OUT pin to ground controls the VA, VB output discharge rate.

EL lamp dimming can be accomplished by changing the input voltage to the VREG pin. The VREG pin allows an external voltage source to control the V_{CS} amplitude. The V_{CS} voltage is approximately 143 times the voltage at the VREG pin.

Fig. 1 : Typical Application Circuit



Block Diagram



Ordering Information

Part Number	Package	Packing
HV816K6-G	16-Lead (4x4) QFN	3000/Reel

-G indicates package is RoHS compliant ('Green')

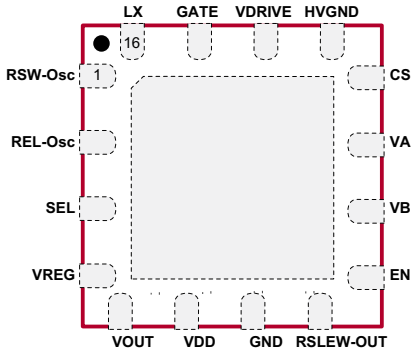
ESD Sensitive Device

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.5 to +7.0V
Output voltage, V_{CS}	-0.5 to +215V
Junction temperature	+125°C
Storage temperature	-65°C to +150°C
Power dissipation: 16-Lead QFN	1.6W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



16-Lead QFN (K6)
(top view)
Center heat slug is at ground potential.
Pads are at the bottom of the package.

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
——— = "Green" Packaging

Package may or may not include the following marks: Si or

16-Lead QFN (K6)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	2.7	-	5.5	V	---
f_{SW}	Switching frequency	50	-	200	kHz	---
f_{EL}	EL output frequency	100	-	1000	Hz	---
S_{EL}	Input for EL output frequency	400	-	4000	Hz	SEL = 4* (f_{EL}) and 50% duty cycle
R_{SLEW}	Output discharge slew rate control resistor	100	-	500	kΩ	---
C_{EL}	EL lamp load capacitance	0	-	150	nF	---
T_j	Operating temperature	-40	-	+85	°C	---

Electrical Characteristics

DC Characteristics *(Over recommended operating conditions unless otherwise specified - T_J = 25°C)*

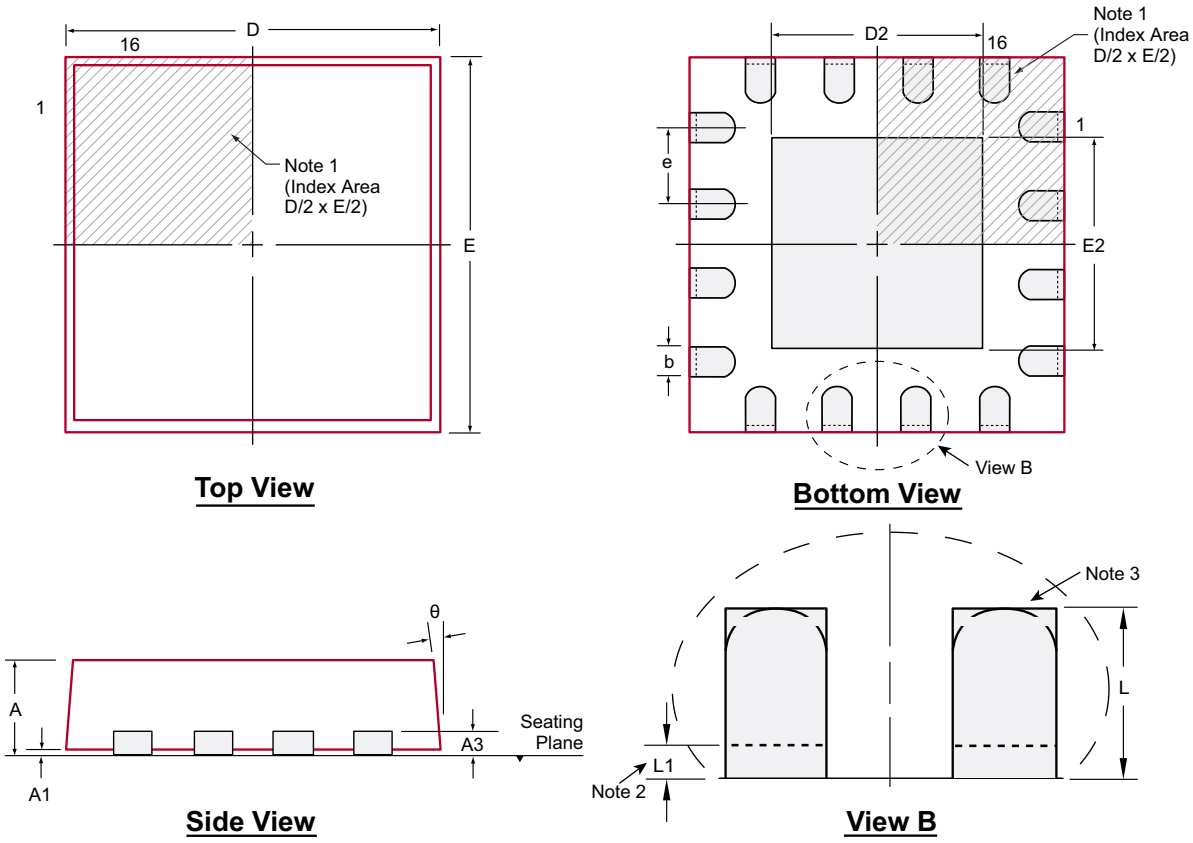
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{CS}	Output regulation voltage	160	180	200	V	V_{DD} = 2.7 to 5.5V
V_{LAMP}	Differential output voltage	320	360	400	V	V_{DD} = 2.7 to 5.5V
I_{DDQ}	Quiescent V_{DD} supply current	-	-	2.0	µA	V_{DD} = 5.5V, EN = Low
I_{DD}	Input current going into the VDD pin	-	-	3.0	mA	V_{DD} = 2.7 to 5.5V, V_{IN} = 5.0V, C_{EL} = 80nF, see Fig. 1
$I_{IN-LOAD}$	Input current including inductor current with load	-	-	380	mA	V_{DD} = 5.5V, V_{IN} = 5.0V, R_{EL} = 1.0MΩ, R_{SW} = 1.0MΩ, see Fig. 1
$I_{IN-NOLOAD}$	Input current including inductor current without load	-	-	80	mA	V_{DD} = 2.7 to 5.5V, V_{IN} = 5.0V No Load, see Fig. 1
I_{INQ}	Quiescent V_{IN} (inductor input voltage) supply current	-	-	10	µA	V_{IN} = 10V, EN = Low, see Fig. 1
V_{REG}	External input voltage range	0	-	1.33	V	V_{DD} = 2.7 to 5.5V
f_{EL}	EL lamp frequency	-	200	-	Hz	R_{EL} = 1.0MΩ
f_{SW}	External MOSFET switching frequency	-	90	-	kHz	R_{SW} = 1.0MΩ
D	External MOSFET duty cycle	-	-	88	%	---
V_{IH}	EN, SEL logic pins input high level	1.5	-	V_{DD}	V	V_{DD} = 2.7 to 5.5V
V_{IL}	EN, SEL logic pins input low level	0	-	0.2	V	V_{DD} = 2.7 to 5.5V
I_{LOGIC}	EN, SEL logic pins high current	-1.0	-	1.0	µA	V_{DD} = 2.7 to 5.5V
V_{GATE}	External MOSFET gate voltage	-	7.0	-	V	V_{DD} = 2.7 to 5.5V
$t_{GATE-RISE}$	External MOSFET gate voltage rise time	-	100	200	ns	V_{DD} = 2.7 to 5.5V, C_{LOAD} = 500pF
$t_{GATE-FALL}$	External MOSFET gate voltage fall time	-	-	20	ns	V_{DD} = 2.7 to 5.5V, C_{LOAD} = 500pF
$t_{VA-FALL}$ or $t_{VB-FALL}$	Output fall time	-	180	-	µs	C_{EL} = 150nF, V_{CS} = 180V, R_{SLEW} = 100kΩ
R_{ON}	On-resistance of internal n-channel MOSFET at LX pin	-	-	30	Ω	Guaranteed by design.

Pin Configuration and External Component Description

Pin #	Pin Name	Description
1	RSW-Osc	External resistor, R_{SW}, from the RSW-Osc to VDD pins sets the switch converter frequency. The switch converter frequency is inversely proportional to the external R_{SW} resistor value. Reducing the resistor value by a factor of two will result in increasing the switch converter frequency by two. A C_{SW} capacitor is recommended from RSW-Osc to the VDD pin to shunt any switching noise that may couple into the RSW-Osc pin. A C_{SW} capacitor with a value of 100nF is typically recommended.
2	REL-Osc	External resistor, R_{EL}, from the REL-Osc to VDD pins sets the EL frequency. The EL frequency is inversely proportional to the external R_{EL} resistor value. Reducing the resistor value by a factor of two will result in increasing the EL frequency by two. The SEL pin should be connected to ground if the R_{EL} resistor is used to set the EL frequency. A C_{FEL} capacitor is recommended from the REL-Osc to VDD pins to shunt any switching noise that may couple into the REL-Osc pin. A C_{FEL} capacitor with a value of 100nF is typically recommended.
3	SEL	External logic signal input to set the EL frequency. The REL-Osc pin should be connected to ground to use this pin. The output EL frequency is ¼ of the frequency input at this pin. This pin if not used, should be connected to ground. Input logic high is 1.5V to V_{DD}. Input logic low is 0 to 0.2V.
4	VREG	Input voltage to set V_{CS} regulation voltage. This pin allows an external voltage source to control the V_{CS} amplitude. The V_{CS} voltage = (143 ± 5%) x V_{REG}. An external resistor, R_{REG}, connected between the VREG and VOUT pins controls the V_{CS} charging rate. The charging rate is inversely proportional to the R_{REG} resistor value.
5	VOUT	Switched internal reference voltage.
6	VDD	Device low voltage input supply pin.
7	GND	Device ground.
8	RSLEW-OUT	An external resistor, R_{SLEW}, from this pin to ground controls the slew rate of VA and VB output discharge. The output discharge slew rate is inversely proportional to the R_{SLEW} resistor value. The VA, VB output discharge time is given by the equation $t_{VA\text{-}fall}$ or $t_{VB\text{-}fall} = \frac{(R_{SLEW} \times C_{EL})\ sec}{43.73}$
9	EN	Enable logic pin to turn the device ON/OFF. Input logic high is 1.5V to V_{DD}. Input logic low is 0 to 0.2V.
10	VA	Lamp connections. The polarity is irrelevant. The EL load capacitance is up to 150nF.
11	VB	
12	CS	High voltage regulated output. Connection for an external high voltage capacitor to ground. A 0.001µF to 0.015µF 200V capacitor can be used to store the energy transferred from the inductor.
13	HVGND	High Voltage Ground. Connect it to device ground
14	VDRIVE	Drive voltage for the Gate voltage and also internal regulated voltage for the output drivers. An external capacitor (C_G) is required at this pin to ground.
15	GATE	Gate control pin for the switching MOSFET. Connection for an external MOSFET. The external MOSFET is used to boost the low input voltage by inductive flyback. When the MOSFET is ON, the inductor is being charged. When the MOSFET is OFF, the charge stored in the inductor will be transferred to the high voltage capacitor C_S. The energy stored in the capacitor is transferred to the internal H-bridge, and therefore to the EL lamp. In general, low R_{ON} MOSFET's, which can handle more current, are more suitable to drive larger size lamps. Also, a small value inductor should be used. But as the R_{ON} value and the inductor value decrease, the switching frequency of the inductor (controlled by R_{SW}) should be increased to avoid inductor saturation. The inductor input voltage (V_{IN}) is recommended to be minimum 4.5V to get the 180V output regulation voltage with 150nF EL load.
16	LX	Drain of the internal N-channel MOSFET. The internal MOSFET is used to generate the GATE pin voltage at startup.

16-Lead QFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.65mm pitch



Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	2.50	3.85*	2.50	0.65 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40†	-	-
	MAX	1.00	0.05		0.35	4.15*	2.80	4.15*	2.80		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-16QFNK64X4P065, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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