HV9985

3-Channel Closed-Loop Switch-Mode LED Driver IC

Features

- Switch Mode Controller for Single-Switch Converters
- Gate Drivers Optimized for Driving Logic Level FETs
  - 0.25A Sourcing
  - 0.5A Sinking
- Typical ±2% Absolute and String-to-String Current Accuracy (with ±1% Sense Resistors)
- High Pulse-Width Modulation (PWM) Dimming Ratio up to 5000:1
- 10V to 40V Input Range
- Constant Frequency Operation up to 1 MHz
- On-Chip Clock or External Clock Option
- Programmable Slope Compensation
- Linear and PWM Dimming
- Output LED Short-Circuit Protection
- Output Overvoltage Protection
- Hiccup Mode Protection

Applications

- RGB Backlight Applications
- Boost, Buck, and SEPIC Topologies
- Multiple String White LED Driver Applications

General Description

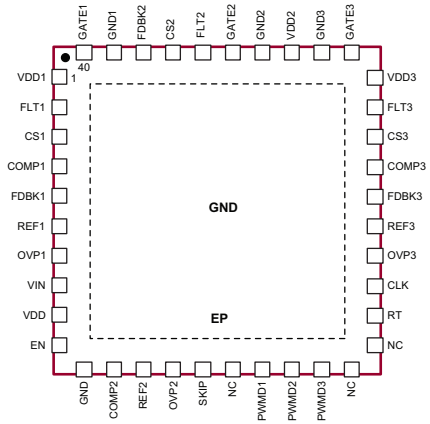
The HV9985 is a 3-channel Peak Current mode PWM controller for driving single-switch converters in a constant output Current mode. It can be used for driving either RGB LEDs or multiple channels of white LEDs.

The HV9985 features a 40V linear regulator, which provides a 5V supply to power the IC. The switching frequencies of the three converters in the IC are controlled either with an external clock signal (the channels operate at a switching frequency of 1/12th of the external clock frequency) or using the internal oscillator. The three channels are positioned 120° out-of-phase to reduce the input current ripple. Each converter is driven by a Peak Current mode controller with output current feedback.

The three output currents can be individually dimmed using either linear or PWM dimming. The IC also includes three disconnect FET drivers, which enable high PWM dimming ratios and disconnect the LED load in case of an output LED Short-circuit condition. The HV9985 includes Hiccup mode protection for both open LED and Short-circuit condition to prevent the IC from shutting down in cases of intermittent Fault conditions.

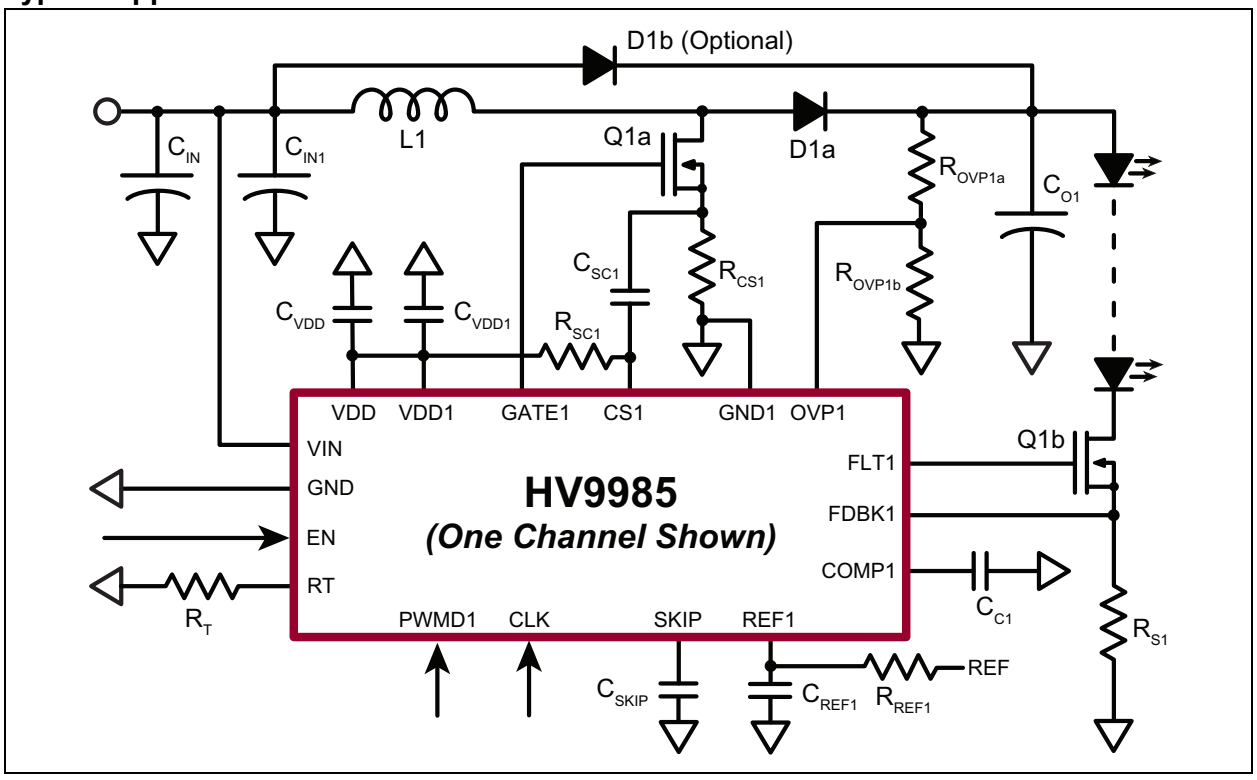
Package Type

40-lead QFN
(Top view)

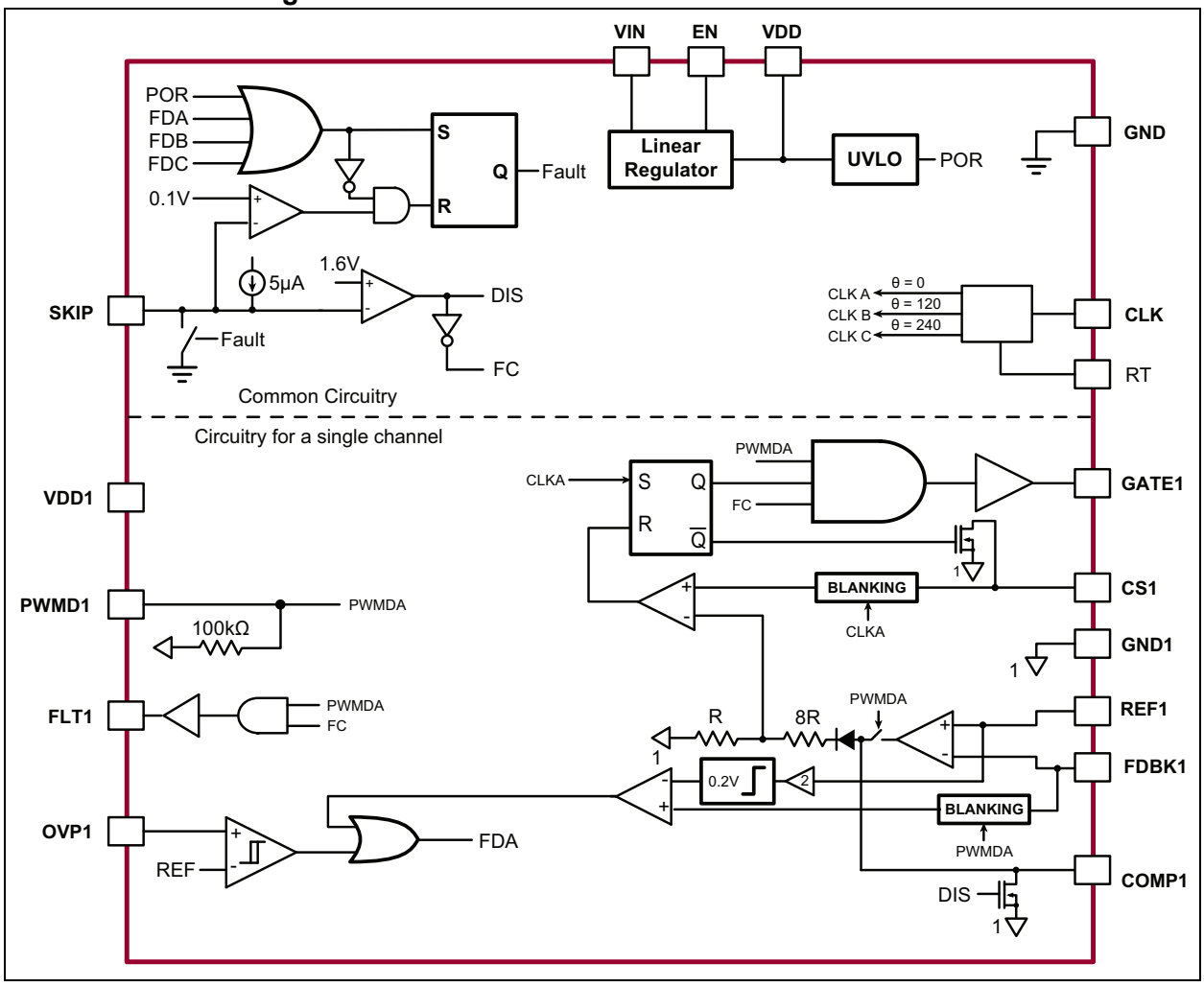


Refer to Table 2-1 for pin information.

Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} to GND .....–0.3V to +45V
V_{DD} to GND, V_{DD1-3} to GND .....–0.3V to +6V
All other pins to GND .....–0.3V to (V_{DD} +0.3V)
Junction Temperature, T_J ..... –40°C to +150°C
Storage Ambient Temperature, T_S ..... –65°C to +150°C
Continuous Power Dissipation (T_A= +25°C) ..... 4000 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C.
V_{IN} = 24V, V_{DD1} = V_{DD2} = V_{DD3} = V_{DD} unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input DC Supply Voltage	V_{INDC}	10	—	40	V	DC input voltage (**Note 1**)
Shutdown Mode Supply Current	I_{INSD}	—	—	200	µA	V_{EN} ≤ 0.8V (**Note 1**)
Supply Current	I_{IN}	—	—	1.5	mA	V_{EN} ≥ 2V, PWMD1 = PWMD2 = PWMD3 = GND
INTERNAL REGULATOR						
Internally Regulated Voltage	V_{DD}	4.75	5	5.25	V	V_{IN} = 10V to 40V, EN = HIGH, PWMD1-3 = V_{DD}; GATE1-3 = 2 nF; CLK = 6 MHz (**Note 1**)
V_{DD} Undervoltage Lockout Threshold	$UVLO_{RISE}$	4.25	—	4.75	V	V_{DD} rising
V_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	—	250	—	mV	V_{DD} falling
ENABLE INPUT						
EN Input Low Voltage	$V_{EN(LO)}$	—	—	0.8	V	**Note 1**
EN Input High Voltage	$V_{EN(HI)}$	2	—	—	V	**Note 1**
EN Pull-Down Resistor	R_{EN}	50	100	150	kΩ	V_{EN} = 5V
PWM DIMMING (PWMD1, PWMD2, AND PWMD3)						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	**Note 1**
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	**Note 1**
PWMD Pull-Down Resistor	R_{PWMD}	50	100	150	kΩ	V_{PWMD} = 5V
GATE (GATE1, GATE2, AND GATE3)						
GATE Short-Circuit Current, Sourcing	I_{SOURCE}	0.25	—	—	A	V_{GATE} = 0V (**Note 2**)
GATE Sinking Current	I_{SINK}	0.5	—	—	A	V_{GATE} = V_{DD} (**Note 2**)
GATE Output Rise Time	T_{RISE}	—	—	85	ns	C_{GATE} = 2 nF (**Note 1**)
GATE Output Fall Time	T_{FALL}	—	—	45	ns	C_{GATE} = 2 nF (**Note 1**)
Maximum Duty Cycle	D_{MAX}	—	91.7	—	%	**Note 2**

Note 1: Specifications apply over the full operating ambient temperature range of –40°C < T_A < +85ºC. Limits are obtained by design and characterization.

2: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C. V_{IN} = 24V, V_{DD1} = V_{DD2} = V_{DD3} = V_{DD} unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
OVERVOLTAGE PROTECTION (OVP1, OVP2, AND OVP3)						
Overvoltage Rising Trip Point	$V_{OVP,RISING}$	1.13	1.25	1.37	V	OVP rising (**Note 1**)
Overvoltage Hysteresis	$V_{OVP,HYST}$	—	125	—	mV	OVP falling
CURRENT SENSE (CS1, CS2, and CS3)						
Leading Edge Blanking	T_{BLANK}	100	—	250	ns	**Note 1**
Delay to Output of GATE	T_{DELAY}	—	—	200	ns	100 mV overdrive to the current sense comparator
Discharge Resistance for Slope Compensation	R_{DIS}	—	—	100	Ω	GATE = Low (**Note 1**)
INTERNAL TRANSCONDUCTANCE OP-AMP (OTA1, OTA2, AND OTA3)						
Gain Bandwidth Product	GBW	—	1	—	MHz	75 pF capacitance at COMP pin (**Note 2**)
Open-Loop DC Gain	A_V	65	—	—	dB	Output open
Input Common-Mode Range	V_{CM}	–0.3	—	3	V	**Note 2**
Output Voltage Range	V_O	—	—	V_{DD}	—	**Note 2**
Transconductance	g_m	500	625	750	µA/V	
Input Offset Voltage	V_{OFFSET}	–5	—	5	mV	
Input Bias Current	I_{BIAS}	—	0.5	1	nA	**Note 2**
Resistor Divider Ratio ($\Delta V_{CS}/\Delta V_{COMP}$)	R_{RATIO}	—	0.11	—	—	**Note 2**
EXTERNAL CLOCK INPUT						
Oscillator Frequency	f_{OSC1}	—	500	—	kHz	F_{CLOCK} = 6 MHz
Oscillator Divider Ratio	K_{SW}	—	12	—	—	**Note 2**
GATE1–GATE2 Phase Delay	$P_{HI}1$	—	120	—	°	**Note 2**
GATE1–GATE3 Phase Delay		—	240	—	°	**Note 2**
Minimum CLOCK Low Time	$T_{OFF,MIN}$	50	—	—	ns	**Note 2**
Minimum CLOCK High Time	$T_{ON,MIN}$	50	—	—	ns	**Note 2**
CLOCK Input High	$V_{CLOCK,HI}$	2	—	—	V	**Note 1**
CLOCK Input Low	$V_{CLOCK,LO}$	—	—	0.8	V	**Note 1**
OSCILLATOR						
Switching Frequency (Common for all Channels)	F_{OSC1}	110	125	140	kHz	R_T = 400 kΩ
	F_{OSC2}	440	500	560	kHz	R_T = 100 kΩ
Switching Frequency Range	F_{OSC}	—	—	1000	kHz	**Note 2**
DISCONNECT DRIVER (FLT1, FLT2, AND FLT3)						
Fault Output Rise Time	$T_{RISE,FAULT}$	—	—	300	ns	500 pF capacitor at FLT pin (**Note 1**)
Fault Output Fall Time	$T_{FALL,FAULT}$	—	—	200	ns	500 pF capacitor at FLT pin (**Note 1**)
SHORT-CIRCUIT PROTECTION (ALL THREE CHANNELS)						
Blanking Time	$T_{BLANK,SC}$	400	—	700	ns	PWMD changes from low to high. (**Note 1**)
Gain for Short-Circuit Comparator	G_{SC}	1.85	2	2.15	—	
Minimum Current Limit Threshold	$V_{CL(MIN)}$	0.15	—	0.25	V	REF = GND

Note 1: Specifications apply over the full operating ambient temperature range of –40°C < T_A < +85ºC. Limits are obtained by design and characterization.

2: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C. V_{IN} = 24V, V_{DD1} = V_{DD2} = V_{DD3} = V_{DD} unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Propagation Time for Short-Circuit Detection	T_{OFF}	—	—	250	ns	V_{FDBK} = 2 • V_{REF} + 0.1V (**Note 1**)
SKIP TIMER						
Current Source at SKIP Pin used for Hiccup Mode Protection	$I_{HC,SOURCE}$	—	5	—	µA	
Voltage Swing at SKIP Pin	ΔV_{SKIP}	—	1.5	—	V	**Note 2**

Note 1: Specifications apply over the full operating ambient temperature range of –40°C < T_A < +85ºC. Limits are obtained by design and characterization.

2: For design guidance only

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGES						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Operating Junction Temperature	T_J	–40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Ambient Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCES						
40-lead QFN	θ_{JA}	—	24	—	°C/W	**Note 1**

Note 1: θ_{JA} for QFN package is based on a four-layer PCB as per JESD51-9.

2.0 PIN DESCRIPTION

The details on the pins of HV9985 40-lead QFN are listed in Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VDD1	These pins are the power supply pins of the three channels. They can either be connected to the VDD pin or powered by an external power supply. They must be bypassed with a low-ESR capacitor to their respective GNDs (at least 0.1 µF). All VDD pins (VDD, VDD1-3) must be connected together externally when the internal 5V linear regulator is used. An external 5V supply can be connected to these pins to power the IC if the internal regulator is not used.
33	VDD2	
30	VDD3	
2	FLT1	These pins are used to drive external logic-level disconnect switches. The disconnect switches are used to protect the LEDs in case of Fault conditions and serve to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
36	FLT2	
29	FLT3	
3	CS1	These pins are used to sense the source current of the external power FETs. They include a built-in 100 ns (minimum) blanking timer. Connecting an RC-network to these pins programs the slope compensation. Refer to **Section 3.5 "Slope Compensation"** for additional information.
37	CS2	
28	CS3	
4	COMP1	Stable closed-loop control can be accomplished by connecting a compensation network between each COMP pin and its respective GND.
12	COMP2	
27	COMP3	
5	FDBK1	These pins are the output current feedback inputs for each channel. They receive voltage signal from external sense resistors.
38	FDBK2	
26	FDBK3	
6	REF1	The voltage at these pins sets the output current level for each channel. The recommended voltage range for these pins is 0V to 1.25V.
13	REF2	
25	REF3	
7	OVP1	These pins provide the overvoltage protection for the three channels. When the voltage at any of these pins exceeds 1.25V, the HV9985 is turned off. The fault timer starts when the voltage drops below 1.125V. Upon completion of the fault timer, the IC attempts to restart.
14	OVP2	
24	OVP3	
8	VIN	This is the input of the internal 40V maximum input linear regulator with 5V regulated output.
9	VDD	This pin is the output of the linear regulator. It maintains a regulated 5V as long as the voltage of the VIN pin is between 10V and 40V. It must be bypassed with a low-ESR capacitor to GND (at least 0.1 µF). This pin can be used as a power supply for the three channels.
10	EN	When the pin is pulled below 0.8V, the IC goes into a Standby mode and draws minimal current.
11	GND	Ground connection for the common circuitry in the HV9985
15	SKIP	This pin programs the hiccup timer for Fault conditions. A capacitor to GND programs the hiccup time.
16	NC	No connect
17	PWMD1	PWM dimming of the three channels is accomplished by using the PWMD pins. The three pins directly control the PWM dimming of the three channels, and a square wave input should be applied to these pins.
18	PWMD2	
19	PWMD3	
20	NC	No connect
21		

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
22	RT	A resistor at this pin programs the on-board oscillator. If an external clock is being used, this pin should be either left open or connected to GND.
23	CLK	This pin is the clock input for the HV9985. The input to the CLK pin should be a TTL-compatible square wave signal. The three channels will switch at 1/12th the frequency of the signal applied at the CLK pin. This pin is used if multiple HV9985s are being used in a system. If the on-chip oscillator is being used, this pin should be connected to GND.
40	GATE1	These pins are the gate drivers which drive the external logic-level N-channel boost converter MOSFETs.
35	GATE2	
31	GATE3	
39	GND1	Ground return for each of the channels. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
34	GND2	
32	GND3	
EP	GND	Exposed backside pad. It must be connected to pin 11 and GND plane on PCB to maximize the thermal performance of the package.

3.0 FUNCTIONAL DESCRIPTION

3.1 Power Topology

The HV9985 is a 3-channel Switch-mode converter LED driver designed to control a boost, a buck, or a SEPIC converter in a constant frequency, Peak Current-controlled mode. The IC includes an internal linear regulator, which operates from input voltage 10V to 40V and provides a 5V supply to power the IC. The IC can also be powered directly with the V_{DD} pins and bypassing the internal linear regulator. The IC includes features typically required in LED drivers like open LED protection, output LED string short-circuit protection, linear and PWM dimming, and accurate control of the LED current. The IC is ideally suited for backlight application using either RGB or multi-channel white LED configurations.

3.2 Power Supply to the IC (V_{IN}, V_{DD}, and $V_{DD1–3}$)

The device can be powered directly from its V_{IN} pin that takes a voltage up to 40V. When a voltage is applied to the V_{IN} pin, the HV9985 tries to maintain a constant 5V (typical) at the V_{DD} pin. The regulator also has a built-in under-voltage lockout which shuts off the IC if the voltage at the V_{DD} pin falls below the UVLO threshold. By connecting this V_{DD} pin to the individual V_{DD} pins of the three channels, the internal regulator can be used to power all three channels in the IC.

If the internal regulator is not utilized, an external power supply (5V +/– 10%) can be used to power the IC. In this case, the power supply is directly connected to the V_{DD} pins and the V_{IN} pin.

All four V_{DD} pins must be bypassed by a low-ESR capacitor (≥0.1 µF) to provide a low impedance path for the high frequency current of the output gate driver. These capacitors must be referenced to the individual grounds for proper noise rejection (see Figure 3-5 for more information). Also, in all cases, the four V_{DD} pins must be connected together externally.

The input current drawn from the external power supply or V_{IN} pin is the sum of the 1 mA (maximum) current drawn by the internal circuitry for all three channels and the current drawn by the gate drivers. In turn, the current drawn by the gate drivers depends on the switching frequency and the gate charge of the external FET.

EQUATION 3-1:

$$I_{IN} = 1mA + (Q_{G1} + Q_{G2} + Q_{G3}) \bullet f_S$$

In Equation 3-1, f_S is the switching frequency of the converters, and Q_{G1-3} are the gate charges of the external FETs which can be obtained from the FET data sheets.

The EN pin is a TTL-compatible input used to disable the IC. Pulling the EN pin to GND will shut down the IC and reduce the quiescent current drawn by the IC to less than 200 µA. If the enable function is not required, the EN pin can be connected to V_{DD}.

3.3 Clock Input (CLK)

The switching frequency of the converters can be set in two ways. The first is by using the on-chip oscillator with a resistor at the RT pin. In this case, the CLK pin should be connected to GND. If the on-chip clock is used, two or more HV9985s cannot be synchronized with each other.

The second is by using a TTL compatible square wave input at the CLK pin. The switching frequencies of the 3 converters will be 1/12th the frequency of the external clock. By using the same clock for multiple ICs, all the ICs can be synchronized together. In this case, the RT pin can either be left open or connected to GND.

3.4 Current Sense (CS1–CS3)

The current sense input is used to sense the source current of the switching FET. Each CS input of the HV9985 includes a built-in 100 ns (minimum) blanking time to prevent spurious turn-off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 9. This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is approximately (V_{DD}–1V), this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The current sense resistor R_{CS} should be chosen, so that the input inductor current is limited to below the saturation current level of the input inductor. For Discontinuous Conduction mode, no slope compensation is necessary. In this case, the current sense resistor is chosen with Equation 3-2.

EQUATION 3-2:

$$R_{CS} = \frac{V_{DD} - 1V}{9 \bullet I_{IN,PK}}$$

Where:

"$I_{IN,PK}$" is the maximum desired peak input current

For Continuous Conduction mode converters operating in Constant Frequency mode, slope compensation becomes necessary to ensure the stability of the Peak Current mode controller if the operating duty cycle is

greater than 50%. This factor must also be accounted for when determining R_{CS}. (Refer to **Section 3.5 "Slope Compensation"**.)

3.5 Slope Compensation

Choosing a slope compensation that is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

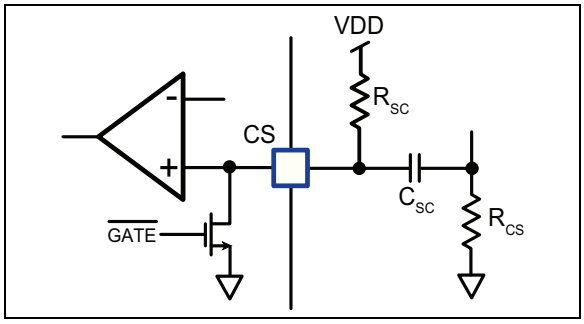


FIGURE 3-1: *Slope Compensation.*

As illustrated in Figure 3-1, slope compensation in HV9985 can be programmed by two external components. A resistor for V_{DD} sets a current, which is almost constant since the V_{DD} voltage is much larger than the voltage at the CS pin. This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns off, an internal pull-down FET discharges the capacitor. The 100Ω resistance of the internal FET (R_{DIS}) will prevent the voltage at the CS pin from going all the way to zero. Equation 3-3 shows how much the minimum value of the voltage will become.

EQUATION 3-3:

$$V_{CS,MIN} = \frac{V_{DD}}{R_{SC}} \bullet R_{DIS}$$

The slope compensation capacitor is chosen, so that it can be completely discharged by the internal FET at the CS pin when FET is switched off. Assuming the worst case switch duty cycle of 92%, C_{SC} may be determined with Equation 3-4.

EQUATION 3-4:

$$C_{SC} = \frac{0.08}{3 \bullet R_{DIS} \bullet f_S}$$

Assuming a down slope current slew rate of DS (A/µs) for the inductor current, the current sense resistor and the slope compensation resistor can be computed as demonstrated in Equation 3-5.

EQUATION 3-5:

$$R_{CS} = \frac{V_{DD} - 1}{9} \bullet \frac{1}{\left[\frac{DS \bullet 10^6 \bullet 0.92}{2 \bullet f_S}\right] + I_{IN,PK}}$$

$$R_{SC} = \frac{2 \bullet V_{DD}}{DS \bullet 10^6 \bullet C_{SC} \bullet R_{CS}}$$

Note that sometimes excessive stray inductance in the current sense path may cause the slope compensation circuit to mistrigger. Figure 3-2 shows the detailed slope compensation circuit with a parasitic inductance LP between the ground of the boost converter power stage and the ground of the respective controller channel in HV9985. The figure also includes the drain capacitance of the boost FET Q1, which is the total capacitance at the drain node.

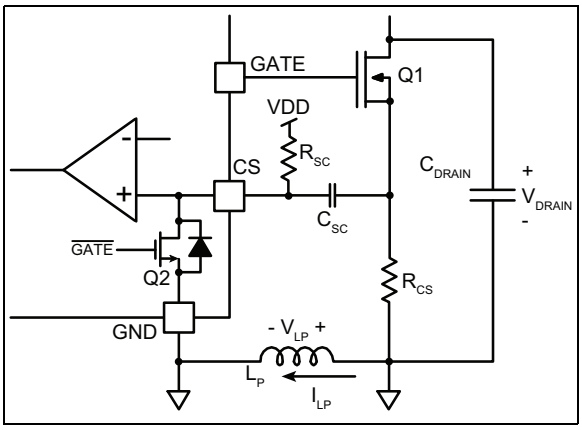


FIGURE 3-2: *Slope Compensation Circuit Operation.*

When the boost FET Q1 is turned off, the internal discharge FET Q2 is turned on and capacitor C_{SC} is discharged. Also, C_{DRAIN} is charged to the output voltage V_O. When the FET Q1 is turned on, the drain node of the FET Q1 is pulled to ground. (Q2 is turned off just before Q1 is turned on.) This causes the drain capacitance to discharge through the FET, leading to a current spike as illustrated in Figure 3-3. This current spike causes a voltage to develop across the parasitic inductance. As long as the current is increasing through the inductance, the voltage developed across parasitic inductance is successfully blocked by the body diode of Q2. However, during the falling edge of the current spike, the voltage across the parasitic inductor causes the body diode to become forward biased. This conduction path through the body diode of

Q2 causes pre-charge of C_{SC}. The pre-charge voltage can be fairly high since the rate of fall of the current is very large.

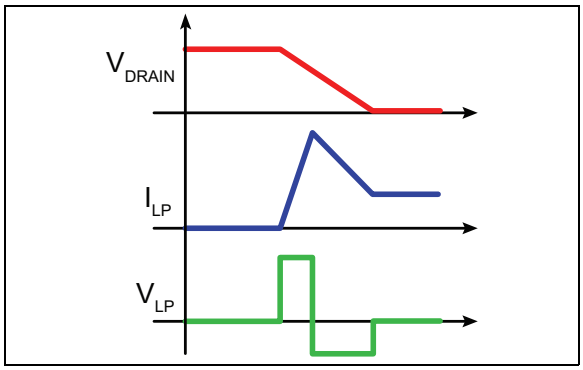


FIGURE 3-3: *Waveforms during Turn-on.*

For example, a typical current spike usually lasts about 100 ns. Assuming a 3A peak current, which is the FET's typical saturation current, and equal distribution between the rise and fall times, a 10 nH parasitic inductance causes a pre-charge voltage. Refer to Equation 3-6.

EQUATION 3-6:

$$V_{PRE-CHARGE} = 10nH \bullet \frac{3A}{50ns} = 600mV$$

As shown in the equation, a very optimistic estimate of the pre-charge voltage is already larger than the Steady state peak current sense voltage. This will cause the converter to false trip.

To prevent this behavior, a resistor R_{EXT} (typically 500Ω to 800Ω) can be added in series with the capacitor C_{SC} as shown in Figure 3-4. This resistor limits the charging current from parasitic inductance into the capacitor. However, the resistor will also slow down the discharge of the capacitor during the FET off-time, so a smaller C_{SC} will be necessary. The component values for the slope compensation design that include R_{EXT} can be computed by substituting R_{EXT} + R_{DIS} in place of R_{DIS} in Equation 3-3 to Equation 3-5.

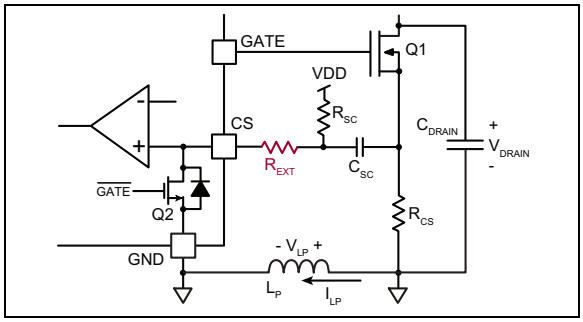


FIGURE 3-4: *Modified Slope Compensation Circuit.*

3.6 LED Current Control

The LED currents in the HV9985 are controlled using three independent current feedbacks. The reference voltage inputs, which set the three LED currents, should be provided at each REF pin (REF1-3). These reference voltages are compared to the voltage from the LED current sense resistors at the corresponding FDBK pins (FDBK1-3) by the respective transconductance amplifiers. HV9985 includes three 1 MHz transconductance amplifiers with tri-state output, which are used to close the feedback loops and provide accurate current control. The compensation networks are connected to the COMP pins (COMP1-3).

The full brightness LED current in each channel can be set by Equation 3-7.

EQUATION 3-7:

$$I_{On} = \frac{V_{REFn}}{R_{Sn}}$$

Where n is the channel number.

The output of each op-amp is buffered and connected to the current sense comparators using an 8:1 divider.

The outputs of the op-amps are controlled by the signal applied to the PWMD pins (PWMD1-3). When PWMD is high, the op-amp output is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge and the voltage at the COMP pin unchanged when the PWMD signal is low, and the gate driver output (GATE1-3) is off. When PWMD is changed from low back to high again, the voltage on the integrating capacitor will force the converter into Steady state almost instantly.

3.7 Linear Dimming

Linear dimming can be achieved by varying the voltages at the REF pins. Since the HV9985 is a Peak Current mode controller, it has a minimum on-time for the GATE outputs. This minimum on-time prevents the converters from completely turning off even when the REF pins are pulled to GND. Thus, linear dimming cannot accomplish true zero-LED current. To get zero-LED current, PWM dimming has to be used for this IC device. Different signals can be connected to the three REF pins if desired, and these inputs need not be connected together.

Due to the offset voltage of the short-circuit comparator and the non-linearity of the X2 gain stage, pulling the REF pin very close to GND would cause the internal short-circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 125 mV (minimum), allowing the REF pin to be pulled all the way to 0V without triggering the short-circuit comparator.

3.8 PWM Dimming

PWM dimming in the HV9985 can be done using TTL compatible square wave sources at the PWMD pins (PWMD1-3). All three channels can be individually PWM dimmed as desired.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching, and the FLT pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines its PWM dimming response since it has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, for a boost converter, the output current is discontinuous, and a large output capacitor is required to reduce the ripple in the LED current. Therefore, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged, and the PWM dimming response of the boost converter improves dramatically.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The chosen filter capacitor should be large enough, so that it can absorb the inductor energy without causing any significant change in voltage across it.

3.9 Fault Conditions

HV9985 is a robust controller which can protect the LEDs and the LED driver in Fault conditions. The outputs of the HV9985 LED driver are protected from both Open and Short LED conditions. In both cases, the HV9985 shuts down and attempts to restart. The hiccup time can be programmed by a single external capacitor at the SKIP pin.

During start-up or when a Fault condition is detected, both GATE and FLT outputs are disabled, the COMP and SKIP pins are pulled to GND. Once the voltage at the SKIP pin falls below 0.1V, and the Fault condition(s) have disappeared, the capacitor at the SKIP pin is released, and it begins charging slowly from a 5 µA current source. Once the capacitor is charged to 1.6V, the COMP pins are released, and the gate driver outputs (GATE and FLT) are allowed to turn on. If the hiccup time is long enough, it will ensure that the compensation networks are all completely discharged and that the converters start at a minimum duty cycle.

The hiccup timing capacitor can be programmed as demonstrated in Equation 3-8:

EQUATION 3-8:

$$C_{SKIP} = \frac{5\mu A \bullet t_{HICCUP}}{1.5V}$$

3.10 Output LED Short-Circuit Protection

When an output LED string Short-circuit condition is detected (i.e. output current becomes higher than twice the Steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the Short-circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the Fault condition still persists, the converter shuts down and goes through the cycle again. If the Fault condition is cleared (a momentary output short), the converter will start regulating the output current. This allows the LED driver to recover from accidental shorts without the need to reset the IC.

During Short-circuit conditions, there are two factors that determine the hiccup time. First is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C), $t_{COMP,n}$ is calculated as shown in Equation 3-9:

EQUATION 3-9:

$$t_{COMP,n} = 3 \bullet R_{Zn} \bullet C_{Zn}$$

Where:

n refers to the channel number

When the compensation networks are only of Type 1 (single capacitor), the computation in Equation 3-10 is used.

EQUATION 3-10:

$$t_{COMP,n} = 3 \bullet 300\Omega \bullet C_{Zn}$$

Therefore, the maximum COMP discharge time required can be calculated as specified in Equation 3-11:

EQUATION 3-11:

$$t_{COMP,MAX} = max(t_{COMP1}, t_{COMP2}, t_{COMP3})$$

The second factor is the time required for the inductors to discharge completely after the Short-circuit condition has been cleared. The time can be computed as illustrated in Equation 3-12:

EQUATION 3-12:

$$t_{IND,\,n} = \frac{\Pi}{4}\sqrt{L_n \bullet C_{On}}$$

Where:

L and C_O are input inductor and output capacitor of each power stage. n refers to the channel number.

The hiccup time is then chosen as shown in Equation 3-13:

EQUATION 3-13:

$$t_{HICCUP} > max(t_{COMP,\,MAX}, t_{IND,\,MAX})$$

3.11 False Triggering of the Short-Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short-circuit comparator, it will cause the IC to falsely detect an Overcurrent condition and shut down.

In HV9985, to prevent these false triggerings, a built-in 500 ns blanking network for the short-circuit comparator is included. This blanking network is activated when the PWMD input goes high. Thus, the short-circuit comparator will not see the spike in the LED current during the turn-on transition of the PWM Dimming. Once the blanking time is over, the short-circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short-circuit will depend on the condition of the PWMD input.

If the output short-circuit exists before the PWM dimming signal goes high, the total detection time is computed as shown in Equation 3-14:

EQUATION 3-14:

$$t_{DETECT1} = t_{BLANK} + t_{DELAY} \approx 900ns(max)$$

If the short-circuit occurs when the PWM dimming signal is already high, the time to detect will be calculated as illustrated in Equation 3-15:

EQUATION 3-15:

$$t_{DETECT1} = t_{DELAY} \approx 200ns(max)$$

3.12 Overvoltage Protection

HV9985 provides hysteretic overvoltage protection, allowing the IC to recover in case the LED load is disconnected momentarily.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, HV9985 detects an Overvoltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold, which is 10% lower than the rising threshold. This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense overvoltage (R_{OVP1}+ R_{OVP2}). In case of a persistent Open Circuit condition, this cycle maintains the output voltage within a 10% band.

In most designs, the falling OVP threshold is more than the LED string voltage. Therefore, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage results in a spike in output current. This leads to the detection of a short circuit, and the short-circuit protection in the HV9985 is triggered. This behavior continues until the output voltage becomes lower than the LED string voltage. When this occurs, no Fault condition will be detected, and the normal operation of the circuit will commence.

Note: The overvoltage thresholds for the three channels in the HV9985 are derived using resistor dividers from the respective V_{DD}s. The resistor dividers are adjusted to give a 1.25V OVP rising trip point and a 1.125V OVP falling trip point at V_{DD} = 5V. The OVP trip points mentioned in the electrical characteristics table of the data sheet assume a V_{DD} voltage generated by the linear regulator of the HV9985. Using an external voltage source at V_{DD} will change the OVP trip points proportionally.

3.13 Layout Considerations

For multi-channel Peak Current mode controller IC to work properly with minimum interference between the channels, it is important to have a good PCB layout which minimizes noise. (Refer to Figure 3-5.) Following the layout rules stated below will help ensure proper performance of all three channels.

3.13.1 GND CONNECTION

The IC has four separate ground connections—one for each of the three channels and one analog ground for the common circuitry. It is recommended that four

separate ground planes be used in the PCB, and all the GND planes be connected together at the return terminal of the input power lines.

3.13.2 V_{DD} CONNECTION

Each V_{DD} pin should be bypassed with a low-ESR capacitor to its OWN ground (i.e. V_{DD1} is bypassed to GND1 and so on). The common V_{DD} pin can be bypassed to the common GND.

3.13.3 REF CONNECTION

In case all the references are going to be driven from a single voltage source, it is recommended to have a small R-C low pass filter (1k, 1 nF) at each REF pin with the filter being referenced to the appropriate channel's ground (as in the case of the V_{DD} pins). If the REF pins are driven with three individual voltage sources, then a small capacitor (1 nF) at each pin would be suitable.

3.13.4 GATE AND CS CONNECTION

The connection from GATE output to the gate of the external FET and the connection from the CS pin to the external sense resistor are designed to be short to avoid false trigerrings.

3.13.5 OVP PROTECTION

Typically, the OVP resistor dividers are located away from the IC. To prevent false trigerrings of the IC due to noise at the OVP pin, placing a small bypass capacitor (1 nF) right at the OVP pin is recommended.

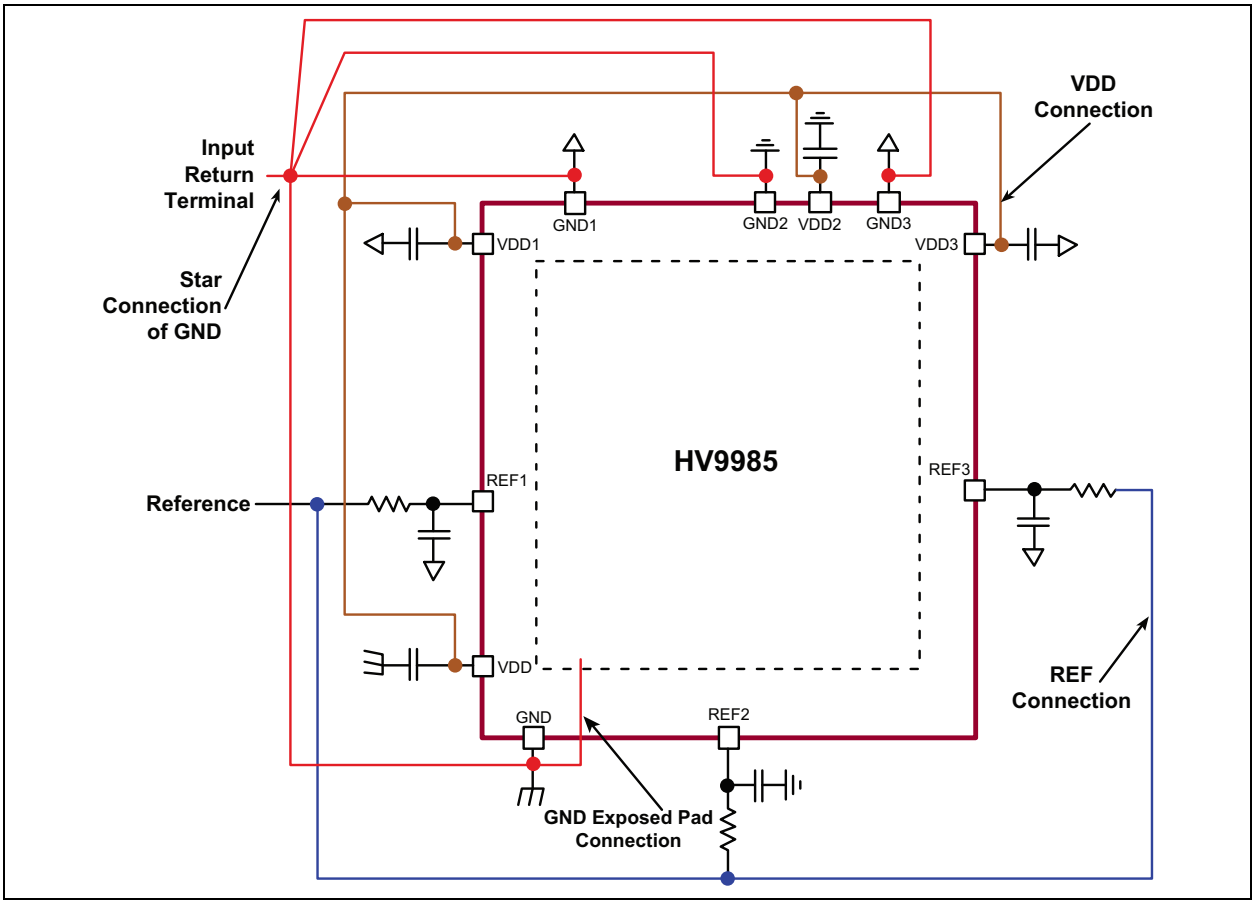
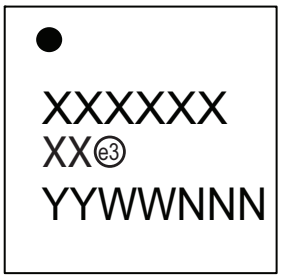


FIGURE 3-5: *Layout Guidelines.*

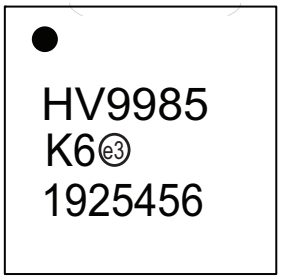
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

40-lead QFN



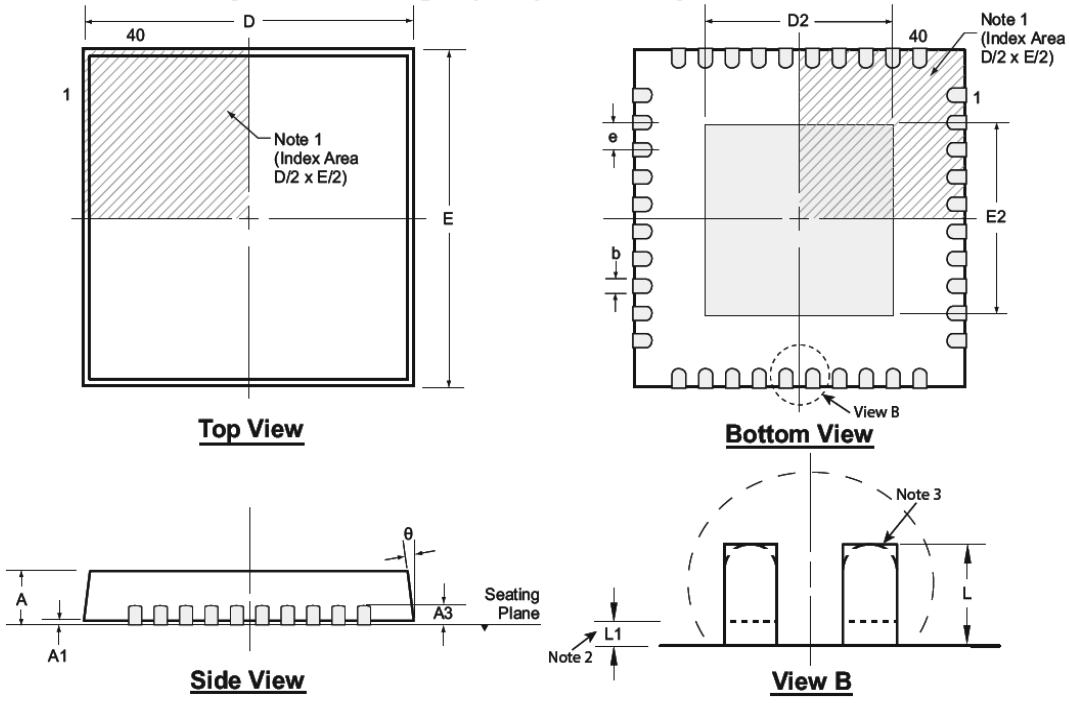
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

40-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (August 2019)

- Converted Supertex Doc #s DSFP-HV9985 to Microchip DS20005558B
- Removed the 44-lead QSOP Package and the K6 M935 media type
- Made minor text changes throughout the document

Revision B (September 2019)

- Changed "PWMD changes from low to high (Note 1)" to "Note 2" in Switching Frequency Range conditions under the Electrical Characteristics Table
- Changed “Note 1” to “PWMD changes from low to high (Note 1)” in Blanking Time conditions under the Electrical Characteristics Table

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9985	=	3-Channel Closed-Loop Switch-Mode LED Driver IC
Package:	K6	=	40-lead QFN (6x6)
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	490/Tray for K6 Package

Example:

a) HV9985K6-G: 3-Channel Closed-Loop Switch-Mode LED Driver IC, 40-lead QFN (6x6), 490/Tray

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