HVL192

Silicon Epitaxial Planar Pin Diode for Wireless LAN

REJ03G0417-0100
Rev.1.00
Nov 24, 2005

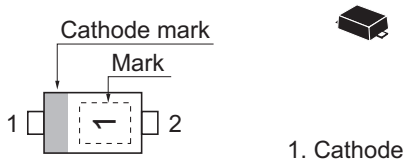
Features

- Suitable for an antenna switches of wireless LAN and a cordless telephone.
- Super -Low capacitance.(C = 0.30 pF max)
- Low forward resistance. (rf = 3.2 Ω max)
- Extremely small Flat Lead Package (EFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code (Previous Code)
HVL192	1	EFP	PXSF0002ZA-A (EFP)

Pin Arrangement



1. Cathode
2. Anode

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	30	V
Forward current	I_F	50	mA
Power dissipation	Pd	100	mW
Junction temperature	Tj	125	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I_R	—	—	100	nA	V_R = 30 V
Forward voltage	V_F	—	—	1.0	V	I_F = 10 mA
Capacitance	C	—	—	0.30	pF	V_R = 1 V, f = 1 MHz
Forward resistance	r_f	—	—	3.2	Ω	I_F = 10 mA, f = 100 MHz

Note: For EFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

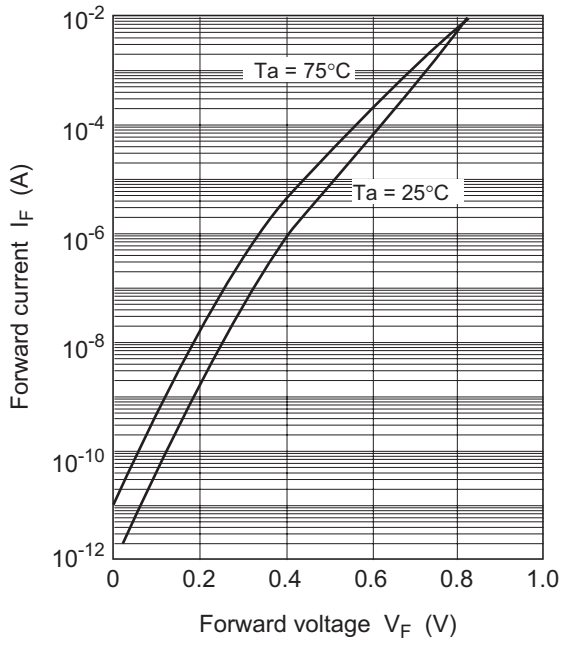


Fig.1 Forward current vs. Forward voltage

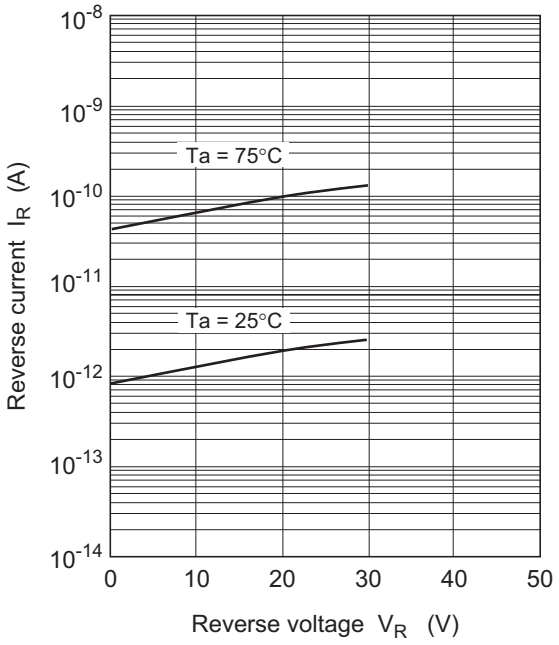


Fig.2 Reverse current vs. Reverse voltage

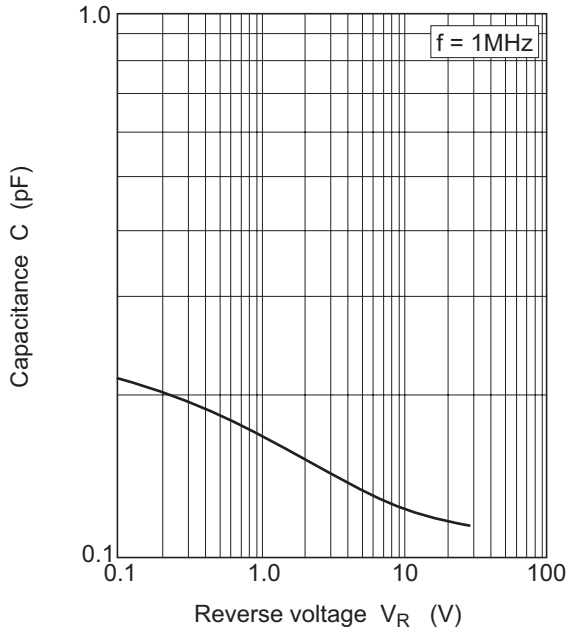


Fig.3 Capacitance vs. Reverse voltage

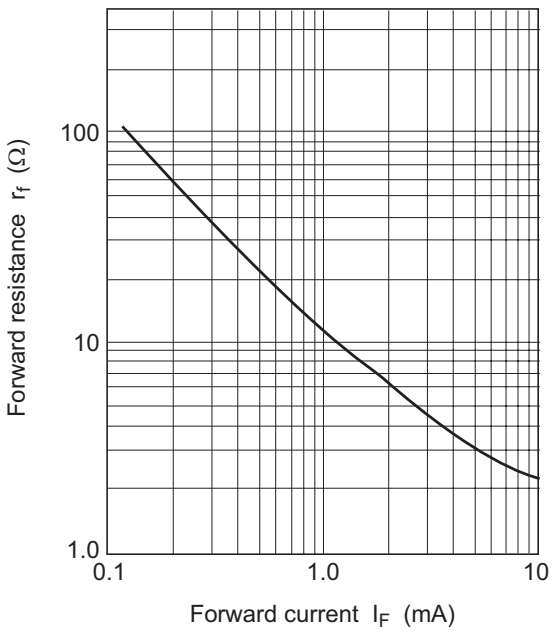
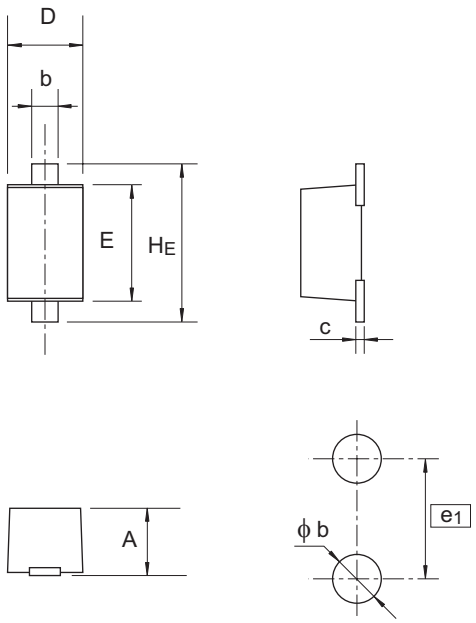


Fig.4 Forward resistance vs. Forward current

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
EFP	—	PXSF0002ZA-A	EFP / EFPV	0.0007g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.44	0.47	0.50
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.75	0.80	0.85
H_E	0.95	1.00	1.05
ϕ b	—	0.40	—
e1	—	1.00	—

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Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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