• Revision Record

REV. NO.	REV.DATE	DESCRIPTION OF REVISION	PAGE	REMARK
0	2008.07.22	Initial Release	ALL	23PAGE
0.1	2009.06.10	PANEL, Drive IC Change	ALL	24PAGE

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NOTE: When using this specification, the reader should keep the followings in mind.

1. This specification may, wholly or partially, be subjected to change without notice.
2. Information contained herein is proprietary information of Humantech Display.
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1. Features

Item	Specification	Remarks
Screen Size	2.4” QVGA	
Display Mode	Transmissive, Normally Black, HFFS	
Display Colors	262K / 65K	
Number of Dots	240(H) × RGB × 320(V)	
Pixel Arrangement	RGB Vertical Stripe	
Driving Method	a-Si TFT Active Matrix	
Viewing Direction	Wide Viewing Angle	
Drive IC	R61505V by RENESAS	
Interface	80 System 16-bit CPU Interface	

2. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Notes.
Power Supply Voltage 1	VCC, IOVCC	-0.3	4.6	V	1,2
Power Supply Voltage 2	VCI - AGND	-0.3	4.6	V	1,3
Power Supply Voltage 3	DDVDH - AGND	-0.3	6.5	V	1,4
Power Supply Voltage 4	AGND - VCL	-0.3	4.6	V	1
Power Supply Voltage 5	DDVDH - VCL	-0.3	9.0	V	1,5
Power Supply Voltage 6	AGND - VGL	-0.3	13.0	V	1,6
Power Supply Voltage 7	VGH - VGL	-0.3	30.0	V	1
Power Supply Voltage 8	VPP1	-0.3	10.0	V	1
Power Supply Voltage 9	VPP2	-0.3	10.0	V	1
Power Supply Voltage 10	VPP3A	-10.0	0.3	V	1
Input Voltage	Vt	-0.3	IOVCC + 0.3	V	1
Operating Temperature	Topr	-20	70	°C	
Storage Temperature	Tstg	-30	80	°C	

Notes 1. If the R61505V is used beyond the absolute maximum ratings, the LSI may be permanently damaged.
It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation.
If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure VCC(high) ≥ GND(low), IOVCC(high) ≥ GND(low).
3. Make sure VCI(high) ≥ AGND(low).
4. Make sure DDVDH(high) ≥ AGND(low).
5. Make sure DDVDH(high) ≥ VCL(low).
6. Make sure AGND(high) ≥ VGL(low).

3. Mechanical Specifications

Item	Specification	Unit
Dimensional Outline	44.52 × 63.38 × 3.5±0.1	mm
Number of Dots	240(H) × RGB × 320(V)	dots
Active Area	36.72(H) × 48.96(V)	mm
Pixel Pitch	0.153(H) × 0.153(V)	mm

4. Electrical Characteristics

(VCC = 2.5V ~ 3.3V, IOVCC = 1.65V ~ 3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input “High” voltage 1 Except RESETX pin	V_{IH1}	IOVCC = 1.65 ~ 3.3V	0.8IOVCC	-	IOVCC	V
Input ”Low” voltage 1 Except RESETX pin	V_{IL1}		-0.3	-	0.2IOVCC	V
Input ”High” voltage 2 RESETX pin	V_{IH2}		0.9IOVCC	-	IOVCC	V
Input ”Low” voltage 2 RESETX pin	V_{IL2}		-0.3	-	0.1IOVCC	V
Output “High” voltage 1 (DB0-17, FMARK)	V_{OH1}	IOVCC = 1.65V ~ 3.3V, IOH = -0.1mA	0.8IOVCC	-	-	V
Output “Low” voltage 1 (DB0-17, FMARK)	V_{OL1}	IOVCC = 1.65 ~ 3.3V IOL = 0.1mA	-	-	0.2IOVCC	V
I/O leakage current	I_{LI}	Vin = 0 ~ IOVCC	-1	-	1	µA
Current Consumption ((IOVCC - GND) + (VCC - GND)) Normal operation mode (260k-color, display operation)	I_{OP1}	fosc = 600kHz (320-line drive), IOVCC = VCC = 3.00V, fFLM = 70Hz, Ta=25℃, RAM data : 18’ h000000 See below for other data.	-	190	400	µA
Current Consumption ((IOVCC - GND) + (VCC - GND)) 8-color mode, 64-line partial display operation	I_{OP2}	fosc = 600kHz (64-line, partial display), IOVCC = VCC = 3.00V, fFLM = 40Hz, Ta = 25℃, RAM data: 18h’ 000000 See below for other data.	-	140	-	µA
Current Consumption ((IOVCC - GND) + (VCC - GND)) Deep standby mode	I_{DST}	IOVCC = VCC = 3.00V, Ta = 25	-	0.1	1.0	µA
Current Consumption ((IOVCC - GND) + (VCC - GND)) RAM access mode	I_{RAM1}	IOVCC = 2.40V, VCC = 3.00V, tCYCW = 125ns, Ta = 25℃, I80-8bit-I/F, TRIREG=1’h1, Consecutive RAM access during display operation.	-	2.0	-	mA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD Power Supply current (VCI - GND) 260-k color display operation	I_{ci1}	IOVCC = 1.8V, VCC = VCI = 2.8V, 320-line drive, fFLM = 60Hz, Ta = 25℃, Frame memory data: 18'h00000, REV = 0, BC0 = 0, FP0 = 8, BP0 = 8, VC = 3'h1, BT = 3'h4, VRH = 5'h18, VCM = 7'h7F, VDV = 5'h11, AP0 = 2'h3, DC00 = 3'h4, DC10 = 3'h4, PR*P00 = PR*N00 = 5'h00, PR*P01 = PR*N01 = 5'h02, PR*P02 = PR*N02 = 5'h04, PR*P03 = PR*N03 = 4'h8, PR*P04 = PR*N04 = 4'hF, PR*P05 = PR*N05 = 4'h8, PR*P06 = PR*N06 = 5'h04, PR*P07 = PR*N07 = 5'h02, PR*P08 = PR*N08 = 5'h04, PIR*P0 = PIR*P1 = PIR*P2 = PIR*P3 = 2'h0, PIR*N0 = PIR*N1 = PIR*N2 = PIR*N3 = 2'h0 (*: 0, 1, 2) No load on the panel, COL = 0	-	3.2	5.0	mA
LCD Power Supply current (VCI-GND) 8-color (64-line partial) display operation	I_{ci2}	IOVCC = 1.8V, VCC = VCI = 2.8V, 64-line partial display, fFLM = 40Hz, Ta = 25℃, Frame memory data: 18'h00000, REV = 0, BC2 = 0, FP2 = 5, BP2 = 8, VC = 3'h1, BT = 3'h4, VRH = 5'h18, VCM = 7'h7F, VDV = 5'h11, AP2 = 2'h3, DC02 = 3'h4, DC12 = 3'h2, PR*P00 = PR*N00 = 5'h00, PR*P01 = PR*N01 = 5'h02, PR*P02 = PR*N02 = 5'h04, PR*P03 = PR*N03 = 4'h8, PR*P04 = PR*N04 = 4'hF, PR*P05 = PR*N05 = 4'h8, PR*P06 = PR*N06 = 5'h04, PR*P07 = PR*N07 = 5'h02, PR*P08 = PR*N08 = 5'h04, PIR*P0 = PIR*P1 = PIR*P2 = PIR*P3 = 2'h0, PIR*N0 = PIR*N1 = PIR*N2 = PIR*N3 = 2'h0 (*: 0, 1, 2) No load on the panel, COL = 1	-	0.8	-	mA
Output voltage dispersion	Δ VO	-	-	5	-	μA
Average output voltage variance	Δ VΔ	-	-35	-	35	mV

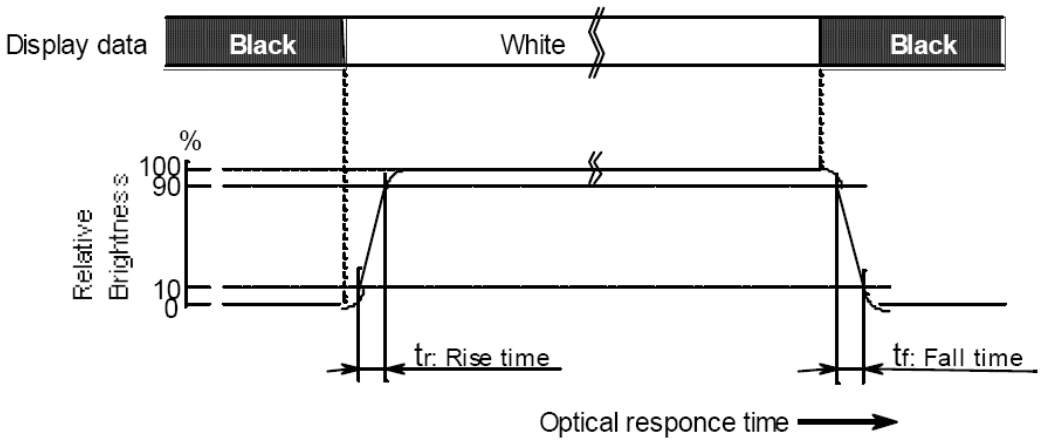
5. Electro-Optical Characteristics

5.1 Main LCD

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Response Time		tr + tf	θ=0°,Ø=0°	-	40	-	ms	1
Contrast Ratio		Cr	θ=0°,Ø=0°	400	600	-	-	2
Transmittance		T	-	4.1	4.4	-	%	3
Color gamut		S		-	71.6	-	%	-
Brightness		B	θ=0°,Ø=0°	170	250	-	cd/m^2	3
Viewing Angle Range		Θ_{X+}	Cr ≥ 10	-	85	-	deg	4
		Θ_{X-}		-	85	-		
		Θ_{Y+}		-	85	-		
		Θ_{Y-}		-	85	-		
CIE(x.y) Chromaticity	Red	X	θ = 0° Ø = 0°	0.642	0.662	0.682	-	3
		Y		0.296	0.316	0.336		
	Green	X		0.242	0.262	0.282		
		Y		0.560	0.580	0.600		
	Blue	X		0.116	0.136	0.156		
		Y		0.076	0.096	0.116		
	White	X		0.271	0.291	0.311		
		Y		0.298	0.318	0.338		

Note 1. The Definition of Response Time

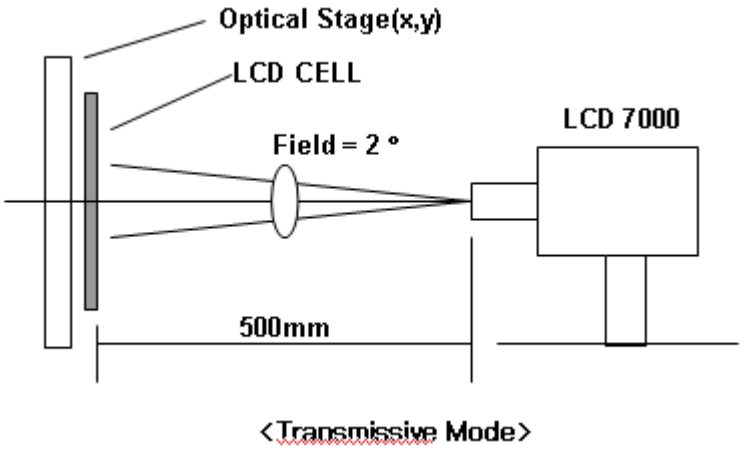
The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



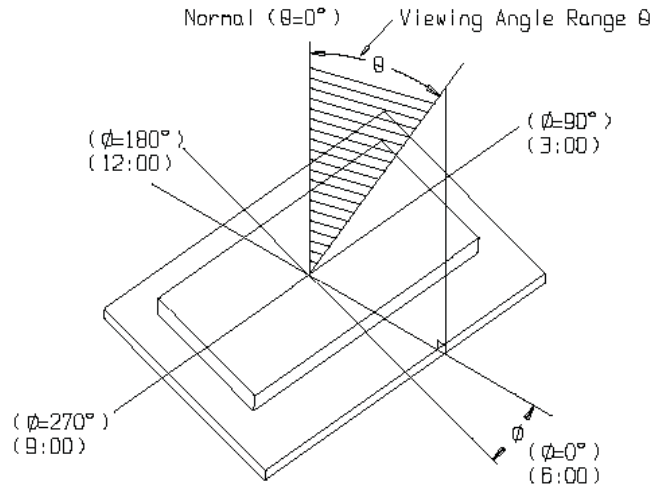
Note 2. The Definition of Contrast Ratio(C/R) : measured at the center of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 3. Optical Characteristic Measurement Equipment and Method

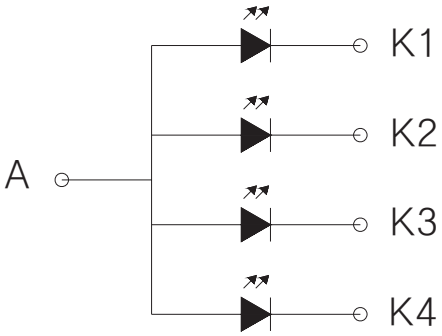


Note 4. The Definition of Viewing Angle



5.2 Back Light Units

Item	Symbol	Min.	Typ.	Max.	Unit
Forward Current	If	-	20	30	mA
Forward Voltage	V_F	3.0	-	3.4	V
Uniformity	△W	80	-	-	%



6. Touch Screen Panel Specifications

6.1 Features

Item		Specification
Panel Type		4-Wire Analog Resistive
Film Type		Clear
Structure	ITO Film	175 / 188 ㎛
	ITO Glass	0.7(t)

6.2 Electrical Characteristics

Item	Min.	Typ.	Max.	Unit	Note
Linearity	-1.5	-	1.5	%	Analog X and Y Directions
Terminal Resistance	200	-	900	Ω	X
	200	-	900	Ω	Y
Insulation Resistance	20	-	-	MΩ	DC 25V
Voltage	-	-	7	V	DC
Chattering Time	-	-	10	ms	100kΩ Pull-up
Transmittance	-	80	-	%	JIS-K7105, ASTM D1003, @550nm

Caution) Do not operate it with a thing except a polyacetal pen(tip R0.8mm or more) or a finger, especially those with hard or sharp tips such as a ball point pen or a mechanical pencil.

6.2 Mechanical & Reliability Characteristics

Item	Min.	Typ.	Max.	Unit	Note
Actuation Force	-	-	80	g	(1)
Durability (surface scratching)	-	-	Write 100,000	Characters	(2)
Durability (surface hitting)	-	-	1,000,000	Touches	(3)
Surface Hardness	3	-	-	H	JIS-K5400

Note) (1) Stylus pen input : R0.8mm polyacetal pen or finger

(2) Measurement for surface area
- Force : 250gf
- Speed : 60mm/sec
- Stylus : R0.8 polyacetal tip

(3) Hit 1,000,000 times on the film with a R8.0 silicon rubber
- Force : 250gf
- Speed : 2 times/sec

7. Module Model No. Expression

H V T 0 2 4 C L T 07
① ② ③ ④ ⑤ ⑥ ⑦

① LCD Module of Humantech Display :
Code Value :

② LCD Mode

LCD Mode	Code Value
TAB	A
COF	F
COG	G
FPC	C
PCB	P
DUAL	D

③ LCD Size (Active Area)

LCD Size	Code Value
1.5”	015
2.0:	020
10”	100

④ Connecting Method

Connect Type	Code Value
Connector	C
Pin	P
None	N

⑤ Backlight Type

Backlight Type	Code Value
CCFL	C
EL	E
LED Backlight	L
LED Frontklight	F
None	N

⑥ Panel Mode

Panel Type	Code Value
TN	N
STN (BLUE, GRAY, YELLOW)	S
FSTN	B
STN Color	C
TFT	T
LTPS	L
FS LCD	F
OLED MONO	O
OLED COLOR	E

⑦ Development No. or LCD Size
Code Value:001 – 999

8. Input Pin Description

Pin NO.	Symbol	Discription	Pin NO.	Symbol	Discription
1	GND	Ground	24	D13	Data 13
2	GND	Ground	25	D14	Data 14
3	VCI	Analog Supply Power	26	D15	Data 15
4	VCI	Analog Supply Power	27	NC	NC
5	VDD	Logic Supply Power	28	NC	NC
6	VDD	Logic Supply Power	29	/RESET	Reset Signal
7	/CS	Chip Select for LCD	30	NC	NC
8	RS	Register Select Signal	31	NC	NC
9	/WR	Write Signal	32	NC	NC
10	/RD	Read Signal	33	GND	Ground
11	D0	Data 0	34	LED+	LED Anode (+)
12	D1	Data 1	35	LED+	LED Anode (+)
13	D2	Data 2	36	LED4-	LED Cathode 4 (-)
14	D3	Data 3	37	LED3-	LED Cathode 3 (-)
15	D4	Data 4	38	LED2-	LED Cathode 2 (-)
16	D5	Data 5	39	LED1-	LED Cathode 1 (-)
17	D6	Data 6	40	GND	Ground
18	D7	Data 7	41	XL	TSP Left
19	D8	Data 8	42	YT	TSP Top
20	D9	Data 9	43	XR	TSP Right
21	D10	Data 10	44	YB	TSP Bottom
22	D11	Data 11	45	GND	Ground
23	D12	Data 12			

Main Category		Sub Category		Upper Code								Lower Code								Note
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index	-	Index	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
0*		00h	Device Code Read	ALMID1[7]	ALMID1[6]	ALMID1[5]	ALMID1[4]	ALMID1[3]	ALMID1[2]	ALMID1[1]	ALMID1[0]	ALMID0[7]	ALMID0[6]	ALMID0[5]	ALMID0[4]	ALMID0[3]	ALMID0[2]	ALMID0[1]	ALMID0[0]	
			(Default)	1	0	1	1	0	1	0	1	0	0	0	0	0	1	0	1	Device Code "B505"
		01h	Driver Output Control						SM		SS									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		02h	LCD Driving Wave Control							BC0									NW0	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		03h	Entry Mode	TRIREG	DFM		BGR					ORG		I/D[1]	I/D[0]	AM				
			(Default)	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	
		07h	Display Control 1				PTDE				BASEE					COL				
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		08h	Display Control 2	FP0[7]	FP0[6]	FP0[5]	FP0[4]	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[7]	BP0[6]	BP0[5]	BP0[4]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	
			(Default)	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	
		09h	Display Control 3						PTS[2]	PTS[1]	PTS[0]			PTG		ISC[3]	ISC[2]	ISC[1]	ISC[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
		0Ah	Display Control 4													FMARKOE	FMI[2]	FMI[1]	FMI[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Ch	External Display Interface Control 1		ENC[2]	ENC[1]	ENC[0]				RM			DM[1]	DM[0]			RIM[1]	RIM[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Dh	Frame Marker Position								FMP[8]	FMP[7]	FMP[6]	FMP[5]	FMP[4]	FMP[3]	FMP[2]	FMP[1]	FMP[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Eh	VCOM Low Power Control											VEM[1]	VEM[0]					
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		0Fh	External Display Interface Control 2												VSPL	HSPL		DEPL	PCKPL	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1*	Power Control	10h	Power Control 1						BT[2]	BT[1]	BT[0]			AP0[1]	AP0[0]		DSTB			
			(Default)	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	
		11h	Power Control 2						DC1[2]	DC1[1]	DC1[0]		DC0[2]	DC0[1]	DC0[0]		VC[2]	VC[1]	VC[0]	
			(Default)	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1	
		12h	Power Control 3				VRH[0]				VCMR			PSON	PON	VRH[4]	VRH[3]	VRH[2]	VRH[1]	
			(Default)	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	
		13h	Power Control 4				VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]									
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2*	RAM Access Control	20h	RAM Address Set (Horizontal Address)									AD[7]	AD[6]	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		21h	RAM Address Set(Vertical Address)								AD[16]	AD[15]	AD[14]	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]	AD[8]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		22h	RAM Data Write / RAM Data Read	RAM write data WD[17:0] / RAM write data WD[17:0] is transferred via different data bus in different interface operations.																
		28h	NVM Data Read 1													UID[3]	UID[2]	UID[1]	UID[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
		29h	NVM Data Read 2										VCM1[6]	VCM1[5]	VCM1[4]	VCM1[3]	VCM1[2]	VCM1[1]	VCM1[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		2Ah	NVM Data Read 3									VCMSEL	VCM2[6]	VCM2[5]	VCM2[4]	VCM2[3]	VCM2[2]	VCM2[1]	VCM2[0]	
			(Default)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
3*	γ Control	30h	γ Control 1				PR0P01[4]	PR0P01[3]	PR0P01[2]	PR0P01[1]	PR0P01[0]				PR0P00[4]	PR0P00[3]	PR0P00[2]	PR0P00[1]	PR0P00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		31h	γ Control 2	PR0P04[3]	PR0P04[2]	PR0P04[1]	PR0P04[0]	PR0P03[3]	PR0P03[2]	PR0P03[1]	PR0P03[0]				PR0P02[4]	PR0P02[3]	PR0P02[2]	PR0P02[1]	PR0P02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		32h	γ Control 3				PR0P06[4]	PR0P06[3]	PR0P06[2]	PR0P06[1]	PR0P06[0]					PR0P05[3]	PR0P05[2]	PR0P05[1]	PR0P05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		33h	γ Control 4				PR0P08[4]	PR0P08[3]	PR0P08[2]	PR0P08[1]	PR0P08[0]				PR0P07[4]	PR0P07[3]	PR0P07[2]	PR0P07[1]	PR0P07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		34h	γ Control 5			PI0P3[1]	PI0P3[0]			PI0P2[1]	PI0P2[0]			PI0P1[1]	PI0P1[0]			PI0P0[1]	PI0P0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		35h	γ Control 6				PR0N01[4]	PR0N01[3]	PR0N01[2]	PR0N01[1]	PR0N01[0]				PR0N00[4]	PR0N00[3]	PR0N00[2]	PR0N00[1]	PR0N00[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		36h	γ Control 7	PR0N04[3]	PR0N04[2]	PR0N04[1]	PR0N04[0]	PR0N03[3]	PR0N03[2]	PR0N03[1]	PR0N03[0]				PR0N02[4]	PR0N02[3]	PR0N02[2]	PR0N02[1]	PR0N02[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		37h	γ Control 8				PR0N06[4]	PR0N06[3]	PR0N06[2]	PR0N06[1]	PR0N06[0]					PR0N05[3]	PR0N05[2]	PR0N05[1]	PR0N05[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		38h	γ Control 9				PR0N08[4]	PR0N08[3]	PR0N08[2]	PR0N08[1]	PR0N08[0]				PR0N07[4]	PR0N07[3]	PR0N07[2]	PR0N07[1]	PR0N07[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		39h	γ Control 10			PI0N3[1]	PI0N3[0]			PI0N2[1]	PI0N2[0]			PI0N1[1]	PI0N1[0]			PI0N0[1]	PI0N0[0]	
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

5*	Window Address Control	50h	Window Horizontal RAM Address (Start Address)									HAS[7]	HAS[6]	HAS[5]	HAS[4]	HAS[3]	HAS[2]	HAS[1]	HAS[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		51h	Window Horizontal RAM Address (End Address)									HEA[7]	HEA[6]	HEA[5]	HEA[4]	HEA[3]	HEA[2]	HEA[1]	HEA[0]
			(Default)	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
		52h	Window Vertical RAM Address (Start Address)								VSA[8]	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		53h	Window Vertical RAM Address (End Address)								VEA[8]	VEA[7]	VEA[6]	VEA[5]	VEA[4]	VEA[3]	VEA[2]	VEA[1]	VEA[0]
			(Default)	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
6*	Base Image Display Control	60h	Driver Output Control	GS		NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]			SCN[6]	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]
			(Default)	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
		61h	Base Image Display Control														NDL	VLE	REV
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		6Ah	Vertical Scroll Control								VL[8]	VL[7]	VL[6]	VL[5]	VL[4]	VL[3]	VL[2]	VL[1]	VL[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial Display Control	80h	Partial Image Display Position								PTDP[8]	PTDP[7]	PTDP[6]	PTDP[5]	PTDP[4]	PTDP[3]	PTDP[2]	PTDP[1]	PTDP[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		81h	Partial Image RAM Address (Start Line Address)								PTSA[8]	PTSA[7]	PTSA[6]	PTSA[5]	PTSA[4]	PTSA[3]	PTSA[2]	PTSA[1]	PTSA[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		82h	Partial Image RAM Address (End Line Address)								PTEA[8]	PTEA[7]	PTEA[6]	PTEA[5]	PTEA[4]	PTEA[3]	PTEA[2]	PTEA[1]	PTEA[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel Interface Control	90h	Panel Interface Control 1							DIVI[1]	DIVI[0]				RTNI[4]	RTNI[3]	RTNI[2]	RTNI[1]	RTNI[0]
			(Default)	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
		91h	Panel Interface Control 1-1													SPCWI[3]	SPCWI[2]	SPCWI[1]	SPCWI[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		92h	Panel Interface Control 2						NOWI[2]	NOWI[1]	NOWI[0]								
			(Default)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		93h	Panel Interface Control 3						VEQWI[2]	VEQWI[1]	VEQWI[0]						MCPI[2]	MCPI[1]	MCPI[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		94h	Panel Interface Control 4														SDTI[2]	SDTI[1]	SDTI[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		95h	Panel Interface Control 5							DIVE[1]	DIVE[0]			RTNE[5]	RTNE[4]	RTNE[3]	RTNE[2]	RTNE[1]	RTNE[0]
			(Default)	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1
		96h	Panel Interface Control 5-1													SPCWE[3]	SPCWE[2]	SPCWE[1]	SPCWE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		97h	Panel Interface Control 6						NOWE[2]	NOWE[1]	NOWE[0]								
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		98h	Panel Interface Control 7														MCPE[2]	MCPE[1]	MCPE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		99h	Panel Interface Control 8														SDTE[2]	SDTE[1]	SDTE[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		9Ch	Panel Interface Control 9										PCDIVH[2]	PCDIVH[1]	PCDIVH[0]		PCDIVL[2]	PCDIVL[1]	PCDIVL[0]
			(Default)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
A*	NVM Control	A0h	NVM Control 1									TE		EOP[1]	EOP[0]			NVAD[1]	NVAD[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A1h	NVM Control 2	NVDAT[15]	NVDAT[14]	NVDAT[13]	NVDAT[12]	NVDAT[11]	NVDAT[10]	NVDAT[9]	NVDAT[8]	NVDAT[7]	NVDAT[6]	NVDAT[5]	NVDAT[4]	NVDAT[3]	NVDAT[2]	NVDAT[1]	NVDAT[0]
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A3h	NVM Control 3													NVVRF			
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A4h	NVM Control 4																CALB
			(Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

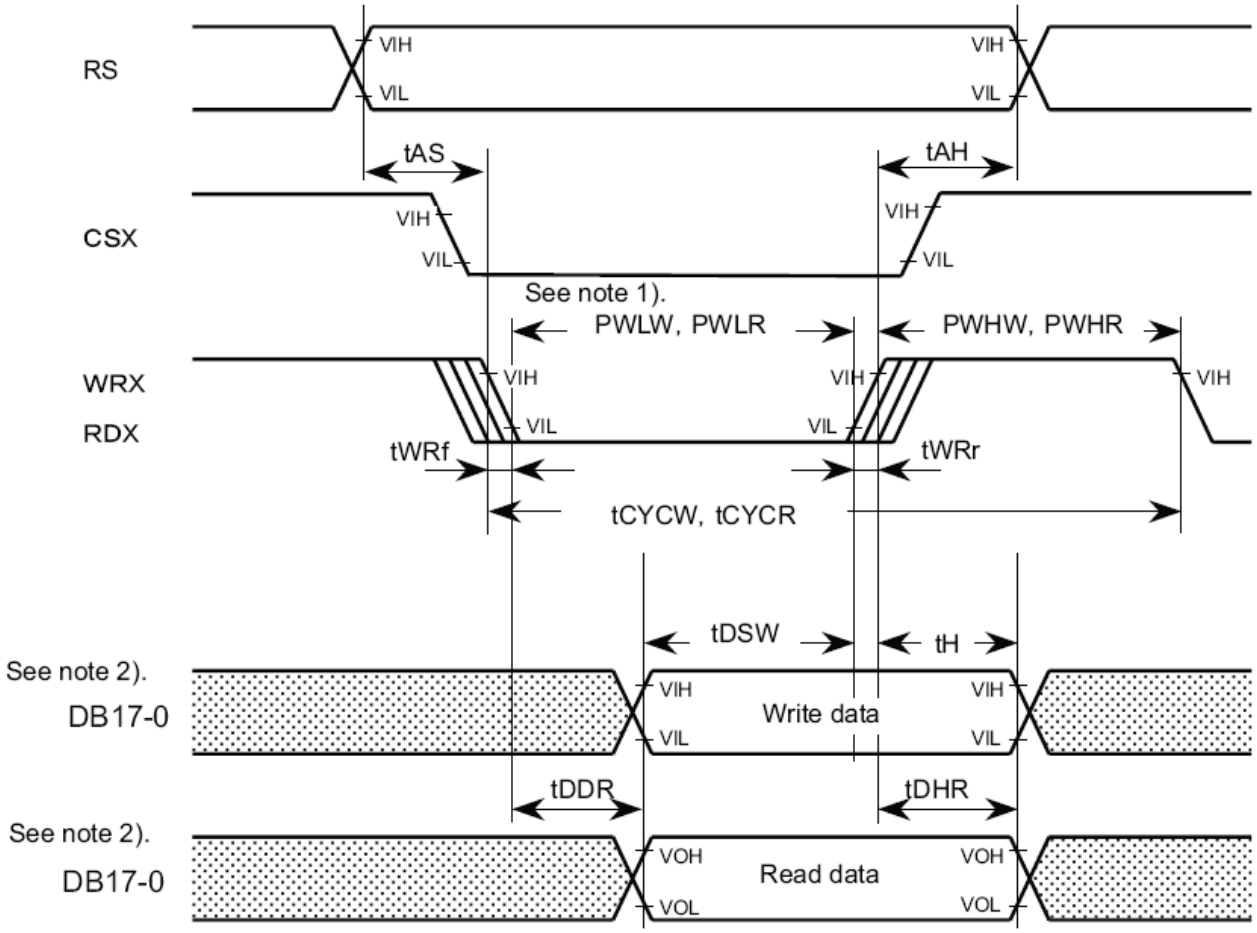
10. Timing Characteristic

10.1 80-System Bus Interface Timing Characteristics (18-/16-bit Interface) (IOVCC = 1.65 ~ 3.3V)

Item		Symbol	Min.	Typ.	Max.	Unit
Bus Cycle Time	Write	t_{CYCW}	75	-	-	ns
	Read	t_{CYCR}	450	-	-	
Write Low Level Pulse Width		PW_{LW}	40	-	-	
Write High Level Pulse Width		PW_{HW}	25	-	-	
Read Low Level Pulse Width		PW_{LR}	170	-	-	
Read High Level Pulse Width		PW_{HR}	250	-	-	
Write/Read Rise/Fall Time		$t_{WRr,\ WRf}$	-	-	25	
Setup Time	Write (RS to CSX, WRX)	t_{AS}	0	-	-	
	Read (RS to CSX, RDX)		10	-	-	
Address Hold Time		t_{AH}	2	-	-	
Write Data Setup Time		t_{DSW}	25	-	-	
Write Data Hold Time		t_{H}	10	-	-	
Read Data Delay Time		t_{DDR}	-	-	150	
Read Data Hold Time		t_{DHR}	5	-	-	

10.2 80-System Bus Interface Timing Characteristics (9-/8-bit Interface) (IOVCC = 1.65 ~ 3.3V)

Item		Symbol	Min.	Typ.	Max.	Unit
Bus Cycle Time	Write	t_{CYCW}	70	-	-	ns
	Read	t_{CYCR}	450	-	-	
Write Low Level Pulse Width		PW_{LW}	30	-	-	
Write High Level Pulse Width		PW_{HW}	25	-	-	
Read Low Level Pulse Width		PW_{LR}	170	-	-	
Read High Level Pulse Width		PW_{HR}	250	-	-	
Write/Read Rise/Fall Time		$t_{WRr,\ WRf}$	-	-	25	
Setup Time	Write (RS to CSX, WRX)	t_{AS}	0	-	-	
	Read (RS to CSX, RDX)		10	-	-	
Address Hold Time		t_{AH}	2	-	-	
Write Data Setup Time		t_{DSW}	25	-	-	
Write Data Hold Time		t_{H}	10	-	-	
Read Data Delay Time		t_{DDR}	-	-	150	
Read Data Hold Time		t_{DHR}	5	-	-	



Note 1) PWLW and PWLR are defined by the overlap period when CSX is "low" and WRX or RDX is "low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

10.3 Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
Reset Rise Time	tr_{RES}	-	-	10	µs
Reset Low Level Width	t_{RES_L}	1	-	-	ms
Reset Wait Time	t_{RW}	1	-	-	ms

Figure C-1 Reset timing when power supply is input

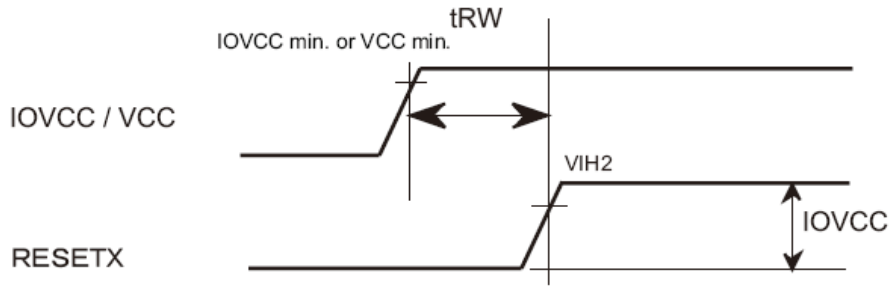
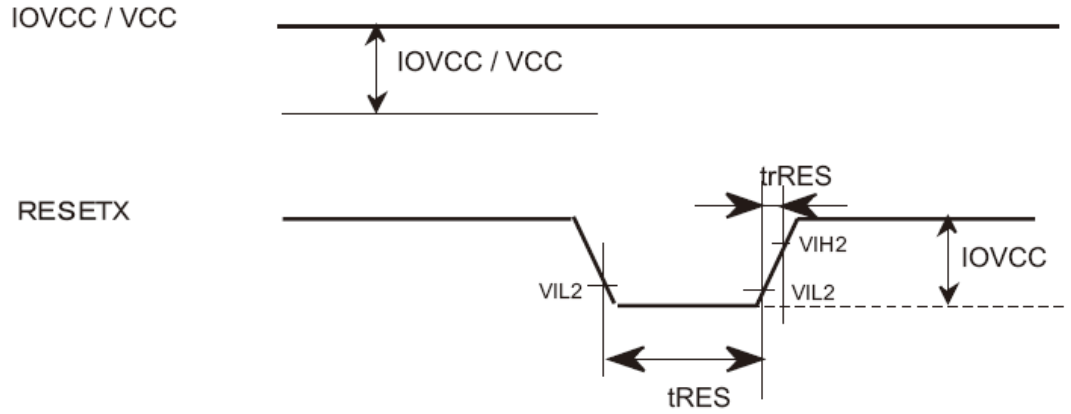


Figure C-2 Reset timing during normal operation



11. Quality Standard

11.1Acceptable Quality Level

INSPECTION ITEM	SAMPLING PROCEDURES	A.Q.L
MAJOR	MIL-STD-105E Inspection Level II Normal Inspection Single sample inspection	0.65
MINOR	MIL-STD-105E Inspection Level II Normal Inspection Single sample inspection	1.0

Major defect :

A major defect is a defect that could result in failure or maternally reduce that the usability of the unit of product for its intended purpose.

Minor defect :

A minor defect is one that does not materially reduce the usability of the product for its intended purpose or is a departure from established standards giving no significant bearing on the effective use or operation of the unit.

11.2 Inspection Conditions

1) The environmental conditions for inspection shall be as follows

-Room Temperature : 25±5

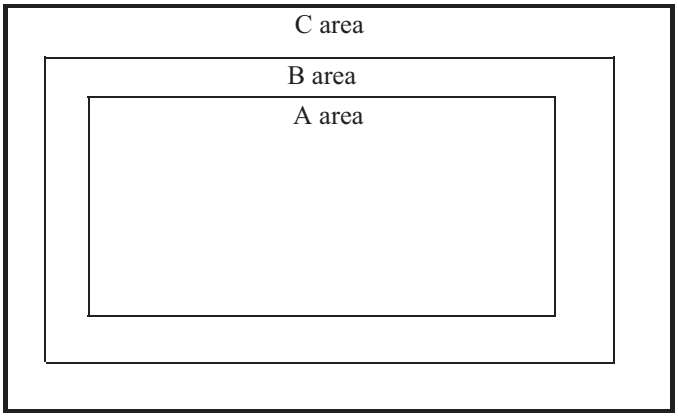
-Humidity Temperature : 65±20%RH

-Room illumination : 300~500[lux]

2) The external visual inspection

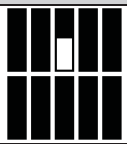
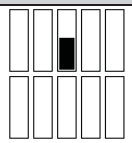
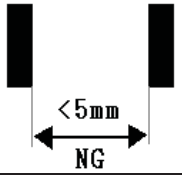
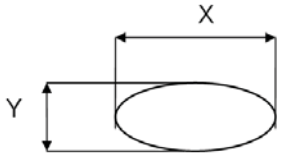
-The inspection shall be performed by using 40Watts fluorescent lamp for illumination and the distance between LCD and eyes of the inspector shall be 30cm or more.

11.3 Definition of the Area

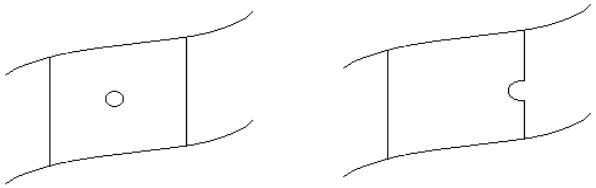


A area: Active Area
B area: Viewing Area
C area: Out of Viewing Area

11.4 Inspection Standards

<table>
<tr><th>Class of Defects</th><th>Inspection Item</th><th>Criteria of Defects</th><th>Remarks</th></tr>
<tr><td rowspan="2">Major</td><td>Display on Inspection</td><td>1) No Display
2) Abnormal Operation
3) Short Circuit
4) Pattern Open
5) Off Viewing angle</td><td></td></tr>
<tr><td>Missing</td><td>Component Missing</td><td></td></tr>
<tr><td>Minor</td><td>Dot Defect I
(A area)</td><td>
<table>
<tr><th>Item</th><th>Symptom</th><th colspan="2">Judgment criteria</th></tr>
<tr><td rowspan="5">Electrical Defect</td><td>Bright dot</td><td colspan="2">Not allowed</td></tr>
<tr><td>Dark dot</td><td colspan="2">2</td></tr>
<tr><td>Distance between Dark-dark</td><td colspan="2">≥5mm</td></tr>
<tr><td>Line defect</td><td colspan="2">Not allowed</td></tr>
<tr><td>No Function</td><td colspan="2">Not allowed</td></tr>
<tr><td rowspan="7">Visual Defect</td><td rowspan="3">Black or white spot / particle</td><td>D≤0.1mm</td><td>Ignore</td></tr>
<tr><td>0.1m<D≤0.2mm</td><td>N≤1</td></tr>
<tr><td>D>0.2mm</td><td>Not allowed</td></tr>
<tr><td rowspan="3">Black or white line/particle(line)</td><td>W≤0.1mm</td><td>Ignore</td></tr>
<tr><td>0.1mm≤W≤0.15mm</td><td>N≤1</td></tr>
<tr><td>W>0.15mm</td><td>Not allowed</td></tr>
<tr><td>Mura</td><td colspan="2">ND 8%</td></tr>
</table>
<table>
<tr><th colspan="4">Bright, Dark dot defect description</th></tr>
<tr><td>Bright area is more than 50% of one dot</td><td>  </td><td>Dark area is more than 50% of one dot</td><td>  </td></tr>
<tr><td colspan="4">Minimun distance between dot defect</td></tr>
<tr><td colspan="2">Dark dot to dark dot</td><td colspan="2"> 
</td></tr>
</table>
Cell Size (Viewing Area Criteria)
※ A area (Spot size) D= (X+Y)/2
B area
Note 1) distance of spot to spot : acceptable over 10mm(blue color drawing)
 

</td><td></td></tr>
</table>

<table>
<tr><th>Class of Defects</th><th>Inspection Item</th><th>Criteria of Defects</th><th>Remarks</th></tr>
<tr><td rowspan="6">Minor</td><td>Dot Defect II
(B,C area)</td><td>
<table>
<tr><th>Defect size</th><th>Acceptable Number</th></tr>
<tr><td>Φ≤0.3 mm</td><td>Ignore</td></tr>
<tr><td>0.30< Φ≤0.50 mm</td><td>2</td></tr>
<tr><td>0.5< Φ≤0.80 mm</td><td>1</td></tr>
<tr><td>0.80 < Φ</td><td>0</td></tr>
</table>
<table>
<tr><th>Item</th><th>Symptom</th><th>Width, Length</th><th>Acceptable number</th></tr>
<tr><td rowspan="4">Visual Defect</td><td rowspan="4">Black or white line/particle (line)</td><td>20<L, 0.03<W<0.04</td><td>5</td></tr>
<tr><td>10<L≤20,0.04<W≤0.06</td><td>3</td></tr>
<tr><td>5.0<L≤10,0.06<W≤0.07</td><td>2</td></tr>
<tr><td>L≤5.0, 0.07<W≤0.09</td><td>1</td></tr>
</table>
※ Scratches should be separated more than 10mm each other(Anti-Glare)
</td><td></td></tr>
<tr><td>Polarizer Nick & Dent</td><td>
<table>
<tr><th>Area</th><th>Defect Size</th><th>Acceptable Number</th></tr>
<tr><td rowspan="2">A, B area</td><td>0.10< Φ ≤0.15 mm</td><td>1</td></tr>
<tr><td>Φ > 0.15</td><td>0</td></tr>
</table>
</td><td></td></tr>
<tr><td>Polarizer Air bubbles</td><td>
<table>
<tr><td rowspan="4">A, B area</td><td>Φ ≤0.10 mm</td><td>Ignore</td></tr>
<tr><td>0.1 < Φ ≤0.15mm</td><td>2</td></tr>
<tr><td>0.15 < Φ ≤0.2 mm</td><td>1</td></tr>
<tr><td>Φ > 0.2 mm</td><td>0</td></tr>
</table>
</td><td>Pol. Between glass</td></tr>
<tr><td>Polarizer Scratch (Linear)</td><td>
<table>
<tr><th>Width(mm)</th><th>Length(mm)</th><th>Acceptable Number</th></tr>
<tr><td>W ≤ 0.03</td><td>Ignore</td><td>3</td></tr>
<tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L ≤ 1.0</td><td>1</td></tr>
</table>
</td><td></td></tr>
<tr><td>Polarizer Dirt and Defect</td><td>
<table>
<tr><th>Size Φ (mm)</th><th>Acceptable Number</th></tr>
<tr><td>Φ < 0.10 mm</td><td>Ignore</td></tr>
<tr><td>0.1mm< Φ ≤0.2 mm</td><td>3</td></tr>
<tr><td>0.2mm< Φ ≤0.25 mm</td><td>1</td></tr>
<tr><td>0.25mm< Φ</td><td>0</td></tr>
</table>
</td><td></td></tr>
<tr><td>Bubble</td><td>1) Round bubble should be treated as spot(positive)
2) Line bubble should be treated as scratch(positive)</td><td></td></tr>
<tr><td>Pattern Miss alignment</td><td>Voids in segment
  </td><td></td></tr>
</table>

Class of Defects	Inspection Item	Criteria of Defects	Remarks
	Stain	This standard will not allow the pollution which is not remove using the soft cloths	
	Rainbow	More than 2 colors are noticeable in the viewing direction.	
	PCB damage	Damage on gold or copper foil	
	Parts alignment	1) IC lead width is more than 70% beyond land pattern(Good). 2) Chip component is off center and more than 30% of the leads is off the pad out line(NG).	
	Conductive foreign matter (solder ball, Solder splash)	Conductive foreign matter is not allowed	
	Bezel claw	Bezel claw missing or not bent	

12. Reliability Condition for LCD

Not to be conspicuous fall of LCD panel function, ability and appearance after following test.

12.1 Reliability Test

The test conditions mentioned above are adopted only to the proto type, and the test per model is conducted once a year.

No.	Item	Condition	Test Time	Sample Numbers	Acc./Rej.	Note
1	High Temp. Operation	70±2℃	96 HRS	5	0/1	
2	Low Temp. Operation	-20±2℃	96 HRS	5	0/1	
3	High Temp. Storage	80±2℃	96 HRS	5	0/1	
4	Low Temp. Storage	-30±2℃	96 HRS	5	0/1	
5	High Humidity Operation	60℃,90% RH	96 HRS	5	0/1	
6	High Humidity Storage	70℃,65% RH	96 HRS	5	0/1	
7	Vibration Test	To be measured after subjecting to total fixed amplitude of 1.5㎜, vibrating frequency of 10～55㎐, 3 direction of X/Y/Z for each 15 minutes (total 45 minutes)				
8	Thermal Shock (Storage)	-30℃ → 80℃ / 10Cycles (30min) (30min)				
9	Static Electricity Test (User-Set state)	Human body model : Contact ± 4 kV, Air ± 8 kV (10 times)				
10	Drop Test	Height 100㎝, 6sides, 10cycles from corner part already edge Region of 1th 3 places each 1th.				

12.2 In case of outgoing products, 1 lot/model/week of it should be applied to the following condition

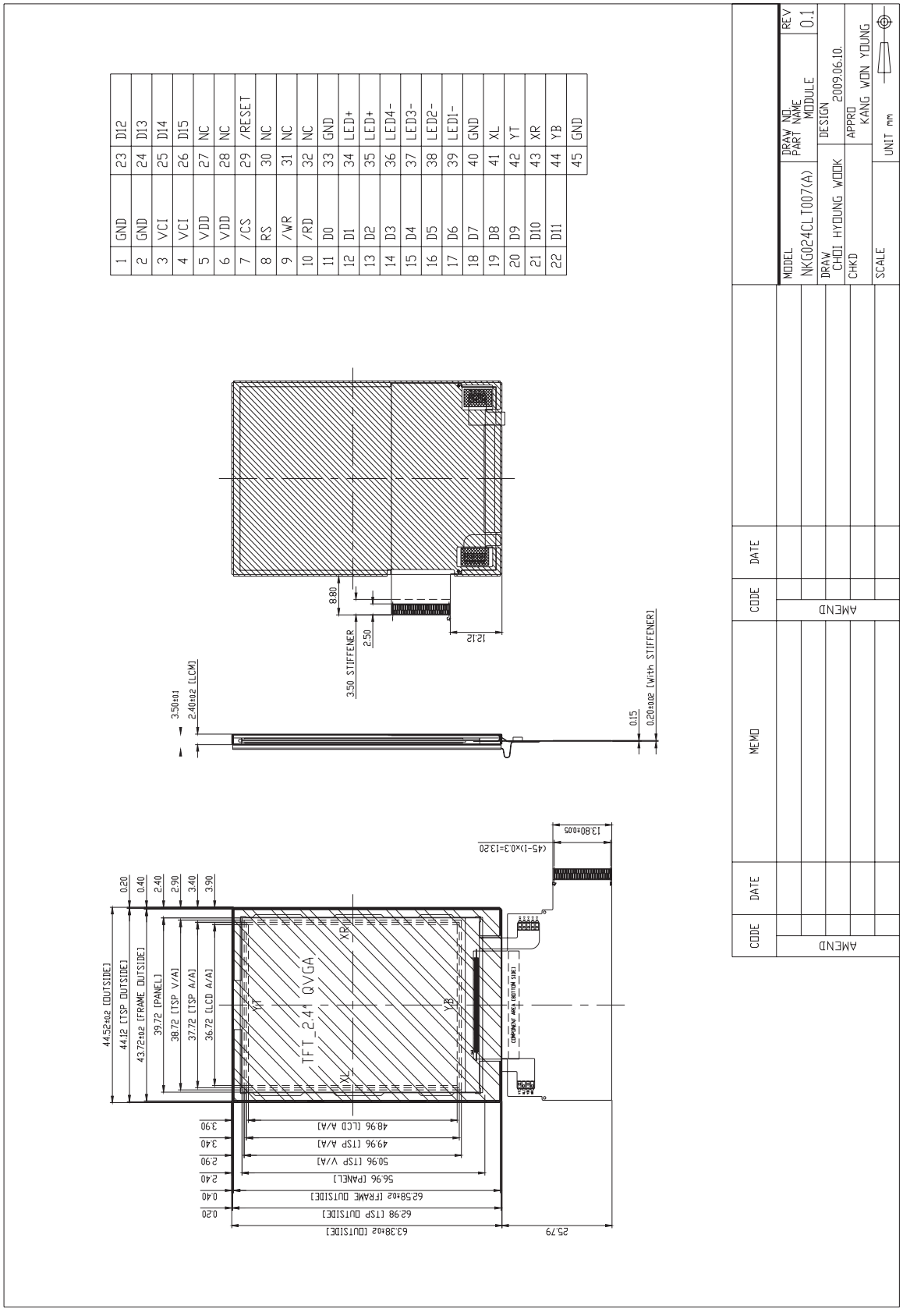
No.	Item	Condition	Test time	Sample numbers	Acc./Rej.	Note
1	High temp. storage	80±2℃	24 HRS	5	0/1	
2	High humidity storage	60, 90% RH	24 HRS	5	0/1	

Pressure under high temperature and high humidity as stipulated above should be conducted with the cell no polarizer attached on.

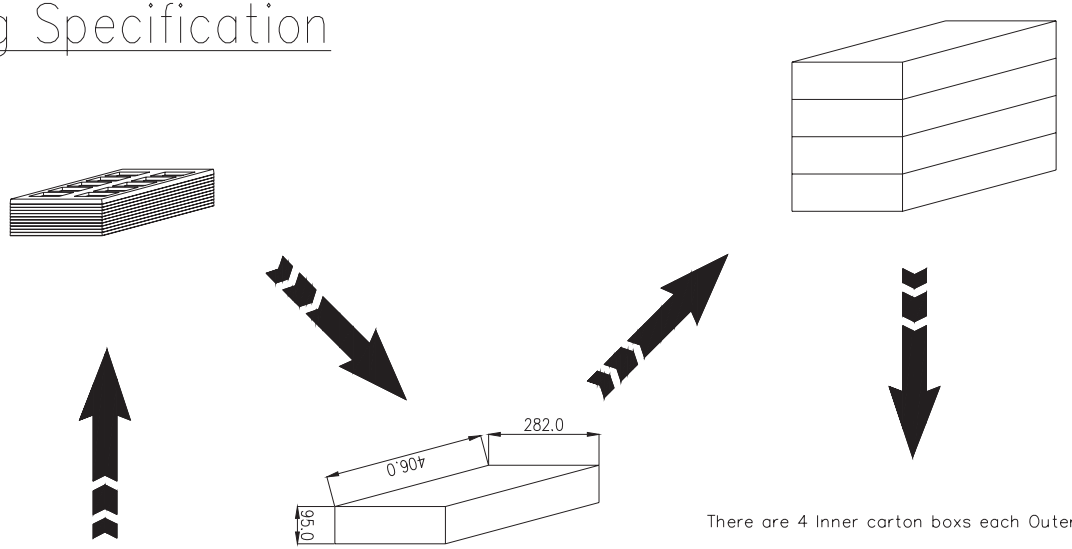
12.3 Criteria

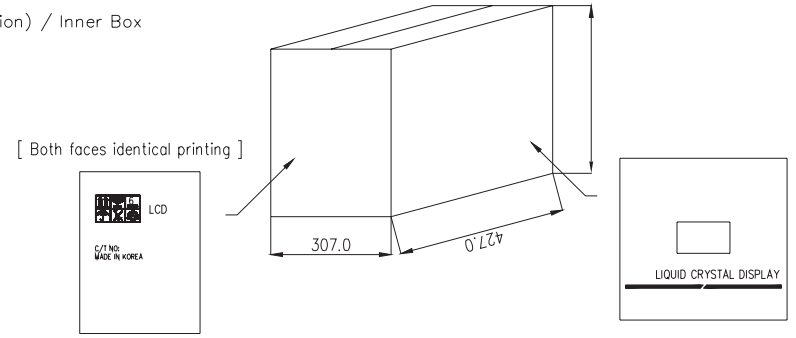
1. The test should be done after the sample staying in the normal environment for more than 24 hours.
2. The function test is ok.
3. No addition to the defect.
4. Current consumption : within ±50% of initial value.

13. Module Dimension



Packing Specification





NOTE

1. 16 modules / CPSTray
2. 11 CPS Trays (Empty 1Tray Inclusion) / Inner Box
3. 4Inner Boxs / Carton Box
4. 640pcs modules / Carton Box
5. 18 Carton Boxs / Master-Carton Box
6. Each CPS Tray 180° rotation.
7. CPS Material : Antistatic , 0.8T

AMEND	CODE	DATE	MEMO	AMEND	CODE	DATE	
	1				6		
	2				7		
	3				8		
	4				9		
	5				10		

MODEL	DRAW NO. PART NAME	REV
DRAW	DESIGN	
CHKD	APPRO	
SCALE	UNIT mm	