300mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The 6219 is designed for portable RF and wireless applications with demanding performance and space requirements. The 6219 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. The 6219 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The 6219 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 and TSOT23-5 packages.

Ordering Information

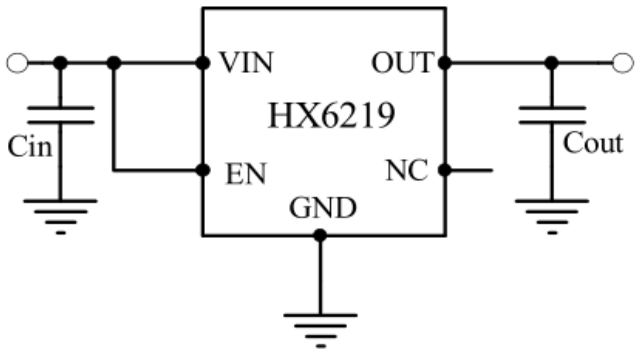
HX6219 □ □ □ □ □

- F: Pb-Free
- Package Type
  - B3: SOT23-3
  - B5: SOT23-5
  - J5: TSOT23-5
- Output Voltage Type
  - 18: 1.8V
  - 25: 2.5V
  - 28: 2.8V
  - 30: 3.0V
  - 33: 3.3V

Features

- Ultra-Low-Noise for RF Application
- 2.5V- 5.5V Input Voltage Range
- Low Dropout : 220mV @ 300mA
- 1.8V, 2.8V,3.0V and 3.3V Fixed
- 300mA Output Current, 550mA Peak Current
- High PSSR:-76dB at 1KHz
- < 0.01uA Standby Current When Shutdown
- Available in SOT23-5 and TSOT23-5 Package
- TTL-Logic-Controlled Shutdown Input
- Ultra-Fast Response in Line/Load transient
- Current Limiting and Thermal Shutdown Protection
- Quick start-up (typically 50uS)

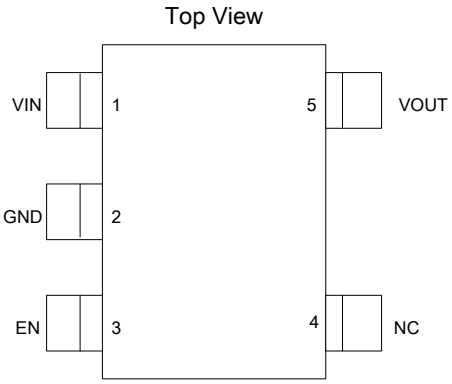
Typical Application Circuit



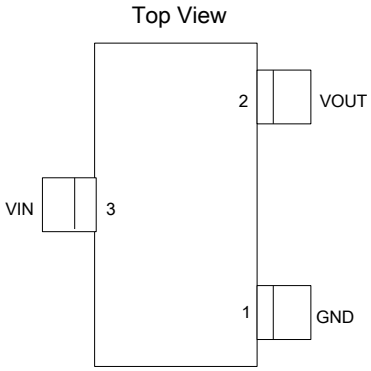
Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Pin Configurations



TSOT23-5/SOT-23-5

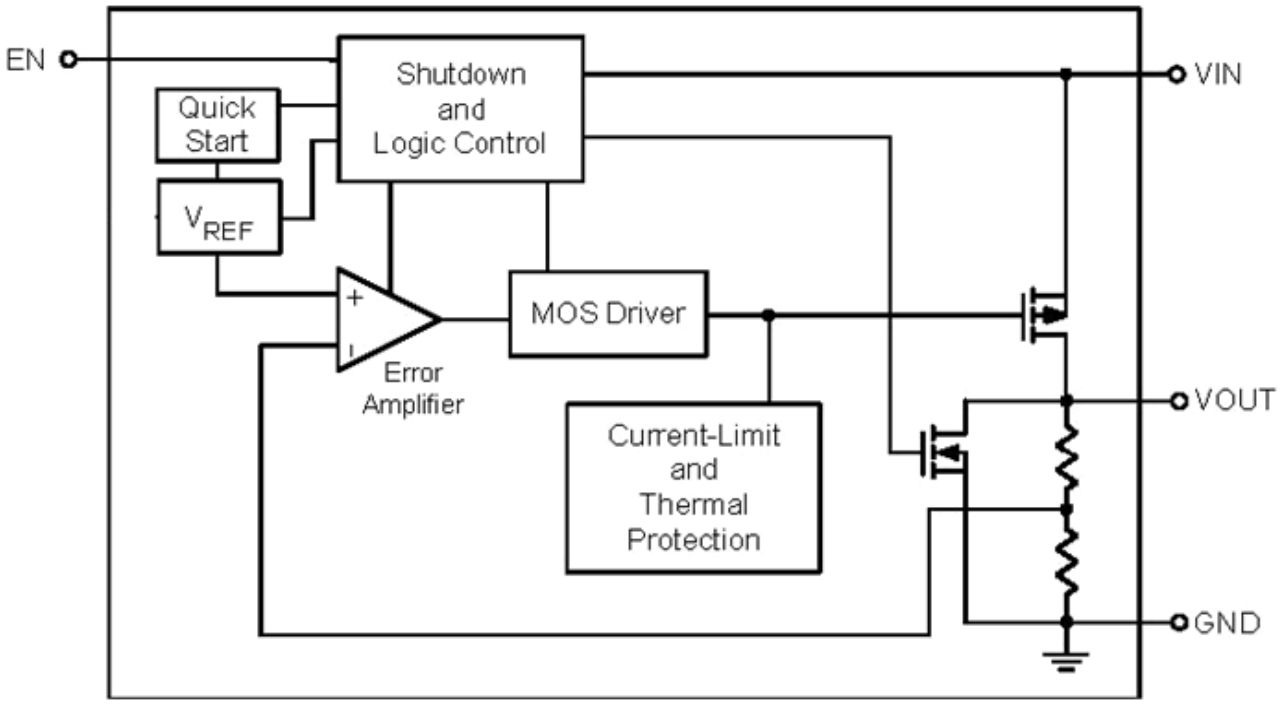


SOT-23-3

Functional Pin Description

SOT23-5	SOT23-3	Pin Name	Pin Function
1	3	VIN	Power Input Voltage.
2	1	GND	Ground.
3	-	EN	Chip Enable (Active High).
4	-	NC	No Connection.
5	2	VOUT	Output Voltage.

Function Block Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- 6.5V
- ✧ Other Pin Voltage ---------- -0.3V to VIN+0.3V

Power Dissipation, PD @ TA = 25°C

- ✧ T/SOT23-5 ---------- 500mW
- ✧ SOT23-3 ---------- 500mW

Package Thermal Resistance

- ✧ Thermal Resistance(SOT23-5/SOT23) (JA) ---------- 195℃/W
- ✧ Thermal Resistance(SOT23-5/SOT23) (JC) ---------- 60℃/W
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Storage Temperature Range ---------- −65℃ to 150℃

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2KV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Supply Input Voltage ---------- 2.5V to 5.5V
- ✧ EN Input Voltage ---------- 0V toVin+0.3V
- ✧ Operation Junction Temperature Range ---------- −40°C to 125°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to 85°C

Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, TA = 25° C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT}=1mA	−2	--	+2	%
Output Loading Current		I_{LOAD}	V_{EN}=V_{IN}, V_{IN}>2.5V		300		mA
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	420	450		mA
Quiescent Current		I_Q	V_{EN}≥1.2V, I_{OUT}=0mA		100	130	μA
Dropout Voltage		V_{DROP}	I_{OUT}=200mA, V_{OUT}>2.8V		130	200	mV
			I_{OUT}=300mA, V_{OUT}>2.8V		220	300	
Line Regulation		ΔV_{LINE}	V_{IN}=(V_{OUT}+1V) to 5.5V, I_{OUT}=50mA			0.2	%/V
Load Regulation		ΔI_{LOAD}	1mA<I_{OUT}<300mA			2	%/A
Standby Current		I_{STBY}	V_{EN}=GND, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN}=3V		1.5	3.5	μA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN}=3V to 5.5V, Start-Up	1.4		V_{IN}+0.3	
Output Noise Voltage			10Hz to 100kHz, I_{OUT}=200mA, C_{OUT}=1μF		300		uVRMS
Power Supply Rejection Rate	f=1KHz		C_{OUT}=1μF, I_{OUT}=100mA		-76		dB
	f=10KHz				−65		
Thermal Shutdown Temperature		TSD			150		℃

Applications Information

Like any low-dropout regulator, the external capacitors used with the 6219 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the 6219 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The 6219 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the 6219 output ensures stability. The 6219 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the 6219 and returned to a clean analog ground.

Start-up Function Enable Function

The 6219 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the 6219 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in 6219. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 20°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C.

The power dissipation definition in device is:

$$PD = (VIN - VOUT) \times IOUT + VIN \times IQ$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula:

$$PD(MAX) = (TJ(MAX) - TA) / \theta JA$$

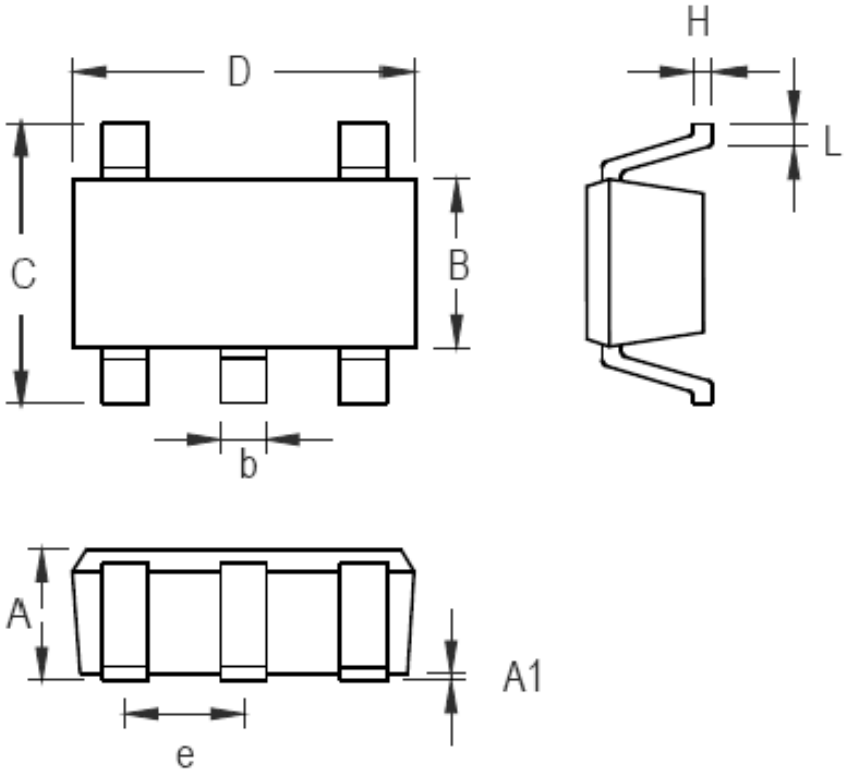
Where TJ(MAX) is the maximum operation junction temperature 125°C, TA is the ambient temperature and the θJA is the junction to ambient thermal resistance. For recommended operating conditions specification of 6219, where TJ(MAX) is the maximum junction temperature of the die (125°C) and TA is the maximum ambient temperature. The junction to ambient thermal resistance (θJA is layout dependent) for SOT23-5 package is 195°C/W.

$$PD(MAX) = (125°C - 25°C) / 195 = 500mW$$

The maximum power dissipation depends on operating ambient temperature for fixed TJ(MAX) and thermal resistance θJA.

Packaging Information

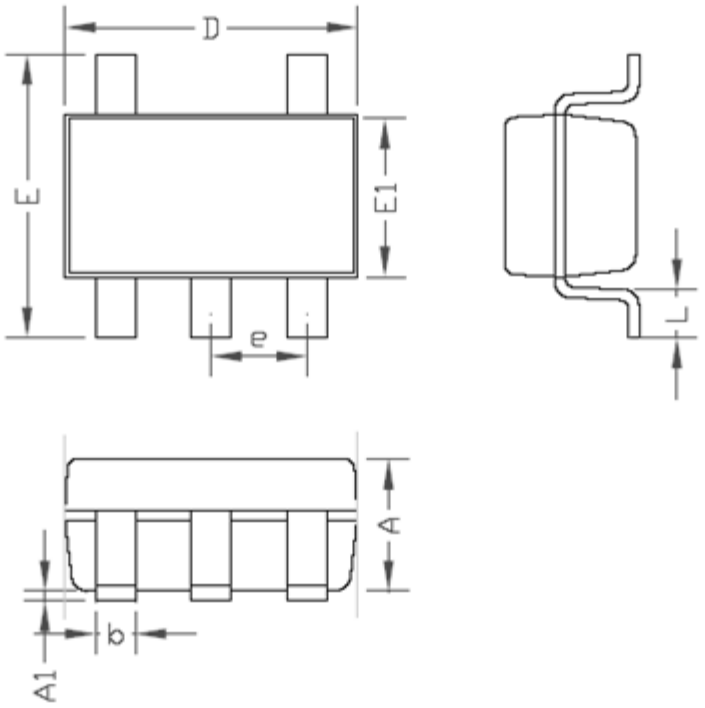
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

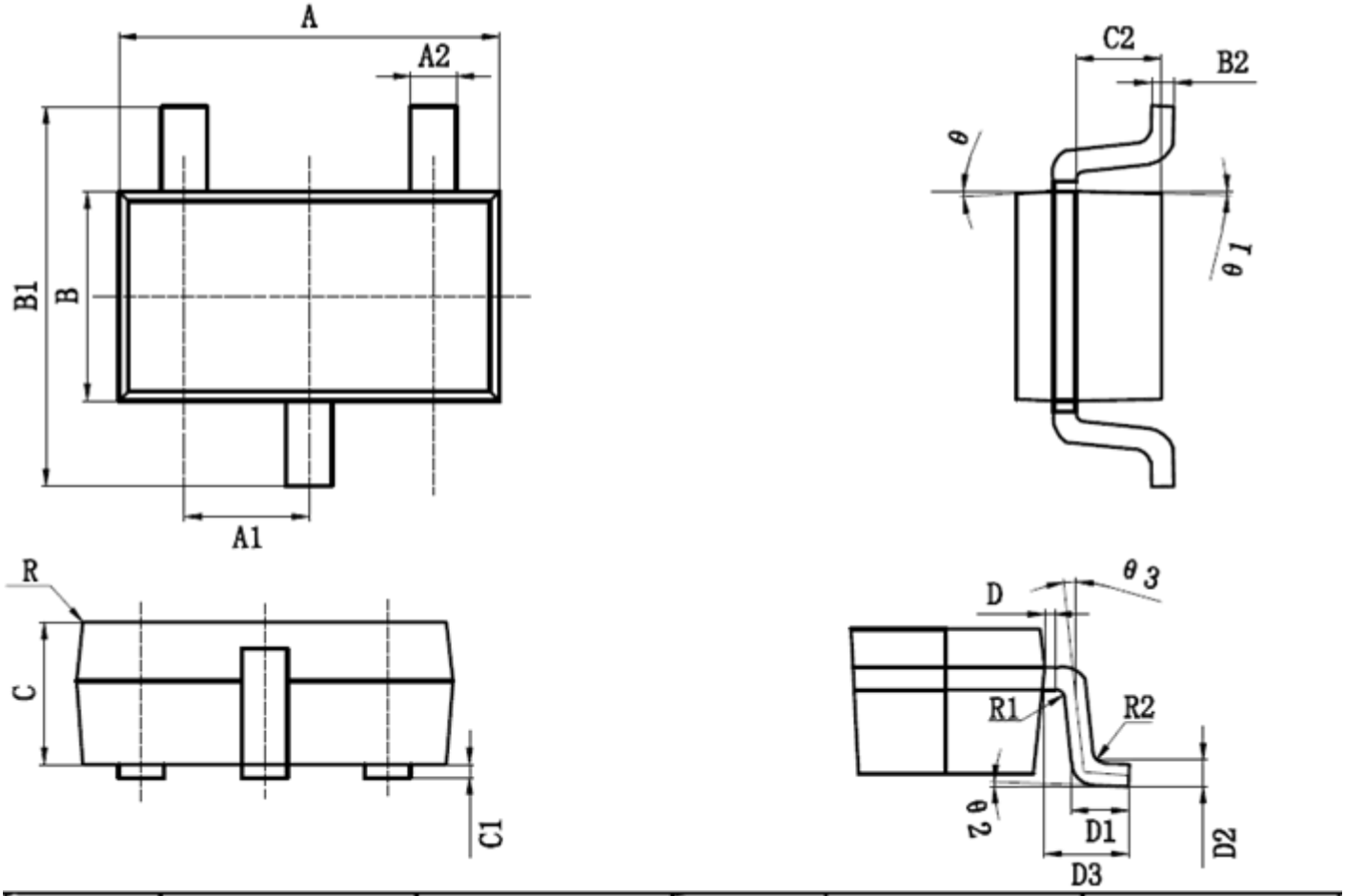
SOT-23-5 Surface Mount Package

TSOT23-5



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.00	-	0.039
A1	0.00	0.15	0.000	0.006
D	2.90		0.114	
E1	1.60		0.063	
E	2.60	3.00	0.102	0.118
L	0.30	0.60	0.012	0.024
b	0.30	0.50	0.012	0.020
e	0.95		0.037	

SOT23-3



Symbol	MIN(mm)	MAX(mm)	Symbol	MIN(mm)	MAX(mm)
A	2.82	3.02	D1	0.40	0.50
A1	0.90	1.00	**D2**	0.254TYP	
A2	0.35	0.45	**D3**	**0.60**	**0.70**
B	1.52	1.72	**θ**	9° TYP4	
B1	2.80	3.00	**θ1**	10° TYP4	
B2	0.119	0.135	**θ2**	0° ~ 8°	
C	1.05	1.15	**θ3**	6° TYP	
C1	0.03	0.13	R	<0.2TYP4	
C2	0.60	0.70	R1	0.08TYP	
D	0.03	0.13	R2	0.08TYP	