



»» **DATA SHEET**

(DOC No. HX8224-B-DS)

»» **HX8224-B**

480x240 TFT LCD Single Chip
Digital Driver

Version 01 October, 2008

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1. General Description

HX8224-B is a 480x240 single chip, which is used for driving TFT LCD panel by 480 source drivers and 240 gate drivers. The HX8224-B could receive 3 types of data format, such as Serial RGB, YUV mode and CCIR656. A wide range supply voltage and small output deviation are designed in this chip to get better performance. This chip also supports SPI commands setting. And the power dissipation on the gamma correction resistors is also concerned, that makes this chip more suitable for middle or small size of color TFT panels.

2. Features

Source Driver

- Support 480 LCD source output. (Delta or Strip Type)
- Supply voltage:
 - Analog Power VDD: 3.0V to 3.6V
 - Logic I/O Power VDDIO: 1.8V to 3.6V
 - Charge Pump Power PVDD: 3.0V to 3.6V
- Line-inversion driving method
- Right and left shift capability
- Support stand-by mode

Timing Controller

- Support serial RGB, serial RGB dummy mode, YUV mode, CCIR656 data input format
- Internal dithering 8-bit data to 6-bit data for source driver circuit
- Support the SPI commands setting

Gate Driver

- 240 LCD gate output
- Up and down scan

Power

- Power circuit supplies VDDA/VGH/VGL/VCOM voltage
- Support VCOM swing driving and DC level adjustment
- SPI setting to support the power circuit control
- Support LED power

Other

- Source Driver Output Pad Pitch: 15 μ m
- Gate Driver Output Pad Pitch: 15 μ m
- Support Cs on common structure
- Support OTP for VCOMDC calibration
- COG package

3. Application

- 480*240 dot Delta panel. 1.7" to 2.4" panel size

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4. Pin Description

Name	I/O	Description
D0	Input	
D1	Input	
D2	Input	
D3	Input	
D4	Input	
D5	Input	
D6	Input	
D7	Input	
DCLK	Input	Input dot clock sync. Data will be fed at the rising edge.
VSYNC	Input	Input frame sync. Low active as default. Normally pull high.
HSYNC	Input	Input line sync. Low active as default. Normally pull high.
DE	Input	Data input enable. Active High to enable the data input. Normally pull Low.
QXH	Output	Test pin for data input sequence control pin.
SPCK	Input	Input reference clock for serial interface. Data is fed at the rising edge of the clock. Normally pull High.
SPDA	Input	Input for data of serial interface. Normally pull Low.
SPENA	Input	Input the chip select signal for serial interface. Normally pull High. Low: select (Enable) High: non-select (disable)
VPSW	Input	Test pin. Keep open in operation. Normally pull Low.
VDDIO	Power	Voltage input pin for I/O logic. (1.8V ~ 3.6V)
REGVDD	Input	Test pin. Keep open in operation. Normally pull High.
VSS	Power	Digital ground. (0V)
RESETZ	Input	Global reset. Keep VDD during operation. Normally pull High.
VDD	Power	Voltage supply pin for analog circuit. (3.0V ~ 3.6V) This pin requires a noise free path for providing accurate LCD driving voltages.
FB	Input	Input for the switching regulator to get the feed back signal for LED driving control. This is the input to sense the voltage level centered at 0.6V and the duty of DRV output is controlled by this level.
VSSA	Power	Analog ground. (0V)
DRV	Output	Output the control signal for switching regulator for LED driving. The Duty is controlled by the FB voltage level.

Name	I/O	Description
PVDD	Power	Charge Pump power. (3.0V ~ 3.6V)
PVSS	Power	Charge Pump ground. (0V)
C1N	I/O	Pin to connect capacitance for power circuit.
C1P	I/O	Pin to connect capacitance for power circuit.
VCC	I/O	Voltage for logic circuit. (2.0V)
C2N	I/O	Pin to connect capacitance for power circuit.
C2P	I/O	Pin to connect capacitance for power circuit.
VINT	I/O	Voltage for source driver and reference voltage. (5.4V)
C3N	I/O	Pin to connect capacitance for power circuit.
C3P	I/O	Pin to connect capacitance for power circuit.
VDDA	I/O	Voltage for source driver and reference voltage. (5V)
VCAC	I/O	VCOM amplitude swing voltage definition. (4V)
FRP	Output	Frame polarity output for VCOM.
VGH	I/O	Positive power supply for gate driver output. (15V)
C4N	I/O	Pin to connect capacitance for power circuit.
C4P	I/O	Pin to connect capacitance for power circuit.
VGL	I/O	Negative power supply for gate driver output. (-10V)
VCOMDC	I/O	VCOM DC voltage output pin for DC re-construction. (0.8V)
S1~S480	Output	Output the driving voltage for the source of LCD panel. (0V ~ 5V)
G1~G240	Output	Output the driving voltage for the gate of LCD panel. (-10V ~ +15V)
TP[7:0]	Output	Test pin (Digital). Keep open in operation.
TP[9:8]	Input	Test pin. Keep open in operation. Normally pull Low.
TP10	Output	Test pin (Gamma). Keep open in operation.
TP11	Output	Test pin (Bandgap). Keep open in operation.

Note: ⁽¹⁾ The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommendations as below.

Pin name	Wiring resistance value(Ω)
VDDIO	< 50
VSS, VSSA	< 20
VDD	< 20
DCLK, D7 ~ D0, DRV	< 100
VSYNC, HSYNC, DE, QXH, SPCK, SPDA, SPENA, RESETZ	< 200
VPSW, REGVDD, FB	< 500

Table 4. 1 The Input Wiring Resistance Values

⁽²⁾ This is generated for the Charge Pump circuit, the external capacitor and maximum wiring resistance is required on those pins as follow:

Cap No.	Pin name	Resistance of Wire (Ω)	Capacitor value (μF)
C01	C1P/C1N	<15	1
C02	VCC	<15	1
C03	C2P/C2N	<15	1
C04	VINT	<15	1
C05	C3P/C3N	<20	1
C06	VDDA	<20	1
C07	VCAC	<20	1
C08	VGH	<20	1
C09	C4P/C4N	<20	1
C10	VGL	<20	1
-	PVDD	<8	-
-	PVSS	<8	-

Table 4. 2 Charge Pump Circuit Capacitor and Wiring Resistance

5. Block Diagram

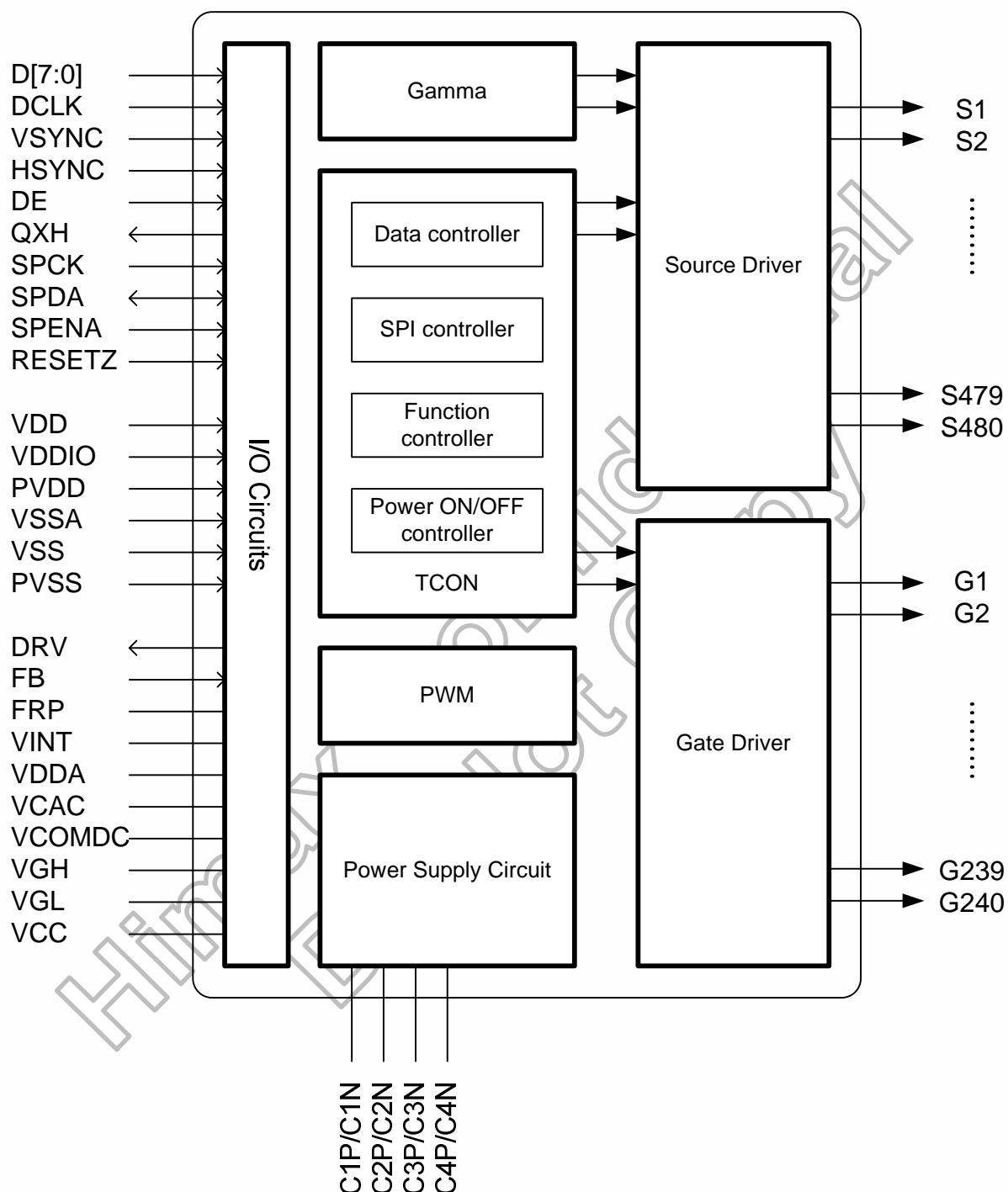


Figure 5. 1 Block Diagram

6. Function Description

6.1 Input data sequence

HX8224-B supports serial RGB、serial RGB dummy, YUV mode、CCIR656 input data formats. When serial RGB data format, the input data sequence is decided by SHL and UD setting, and others data format does not.

		D[7:0] input sequence			
SEL[2:0]	SHL	L	L	H	H
	UD	L	H	L	H
000	ODD Line	Input sequence = color filter sequence			
	EVEN Line				
001 010	X	D, R, G, B ...			
011 100 111	X	Cb, Y, Cr, Y ...			
101 110	X	Cr, Y, Cb, Y ...			

Table 6. 1 Input Data Sequence

6.2 Power relationship

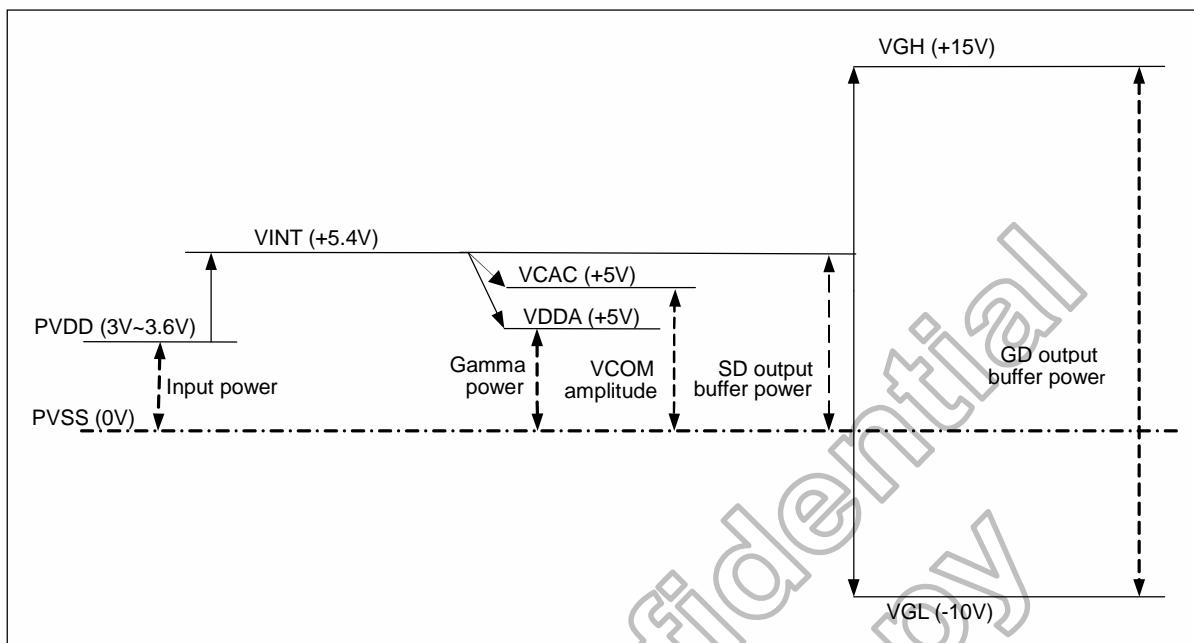


Figure 6.1 Power Relationship

6.3 Power on/off sequence

Specially take care that the large current may cause a permanent damage to the IC when voltage is applied to the Charge Pump Power supply in the condition that the logic power supply is floating.

Please refer to the following timing and command setting, concerning the power supply on and the power supply off. PVDD, VDD and VDDIO must be power on at the same time. And power source (PVDD, VDD and VDDIO) slew time must be less than 1000 us.

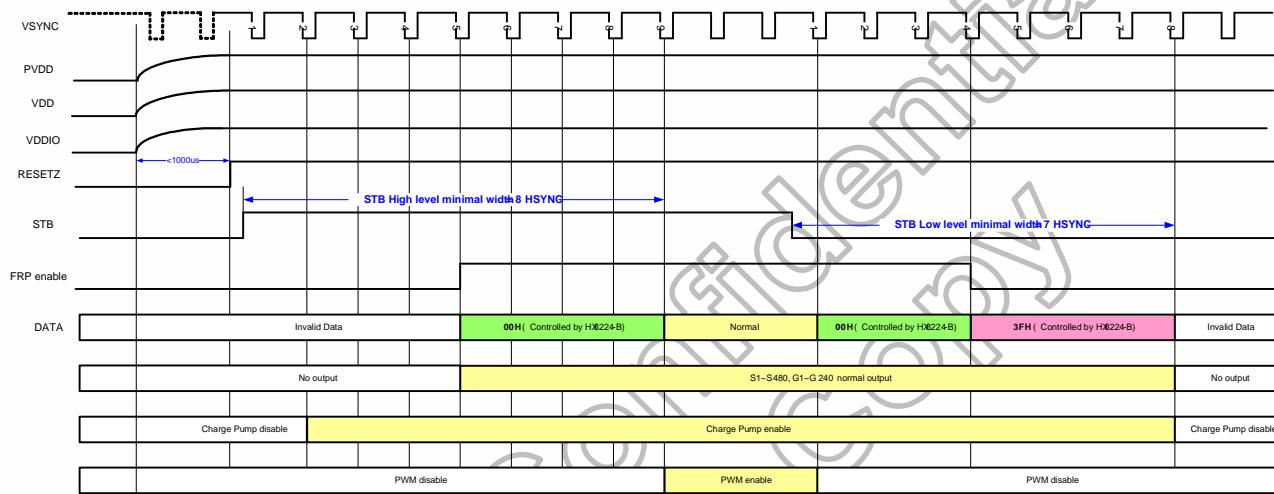


Figure 6.2 Power on/off Sequence Timing Diagram

6.4 VCOM and Charge Pump application circuits

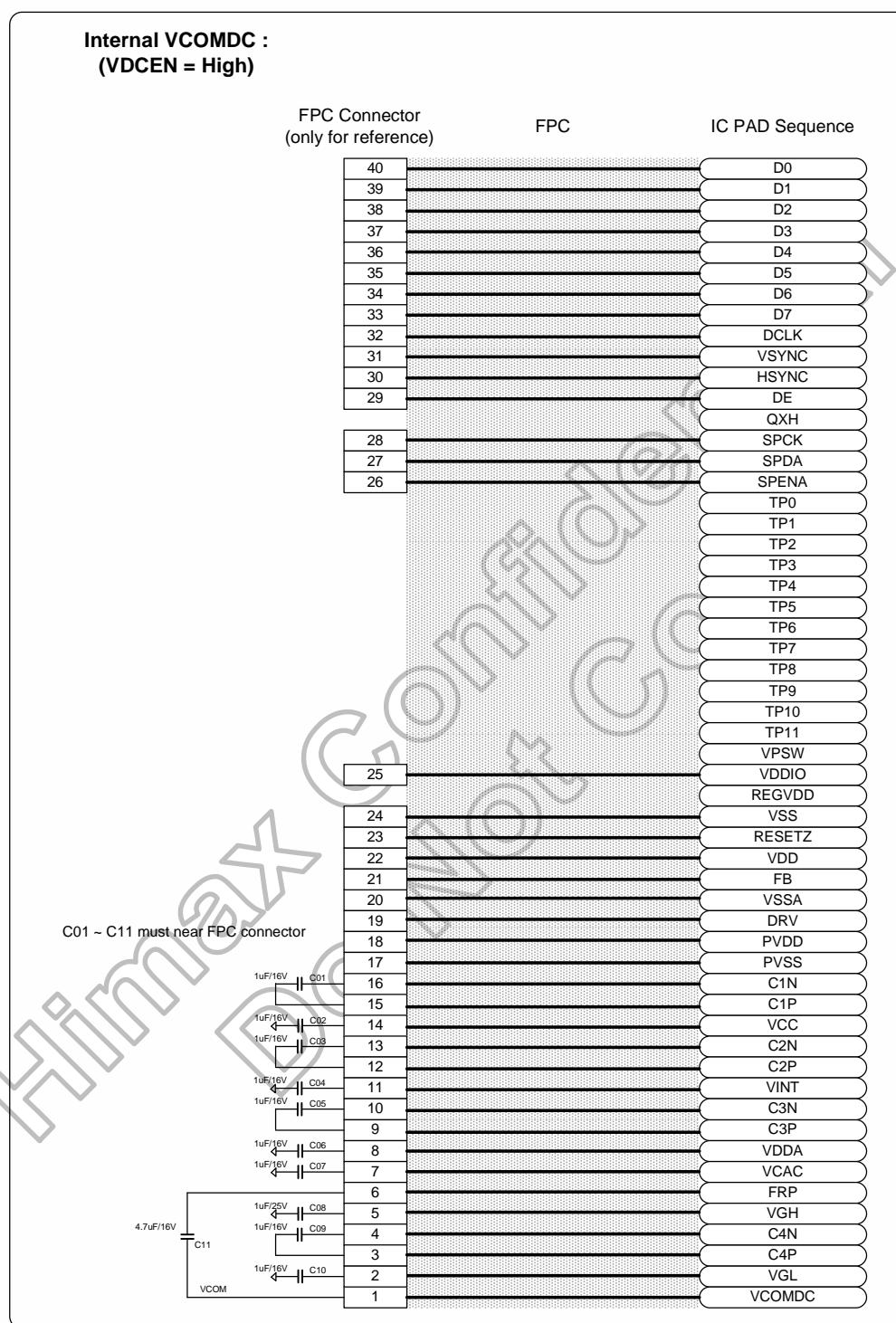


Figure 6. 3 Internal VCOM and Charge Pump Application Circuits

External VCOMDC :
(VDCEN = Low)

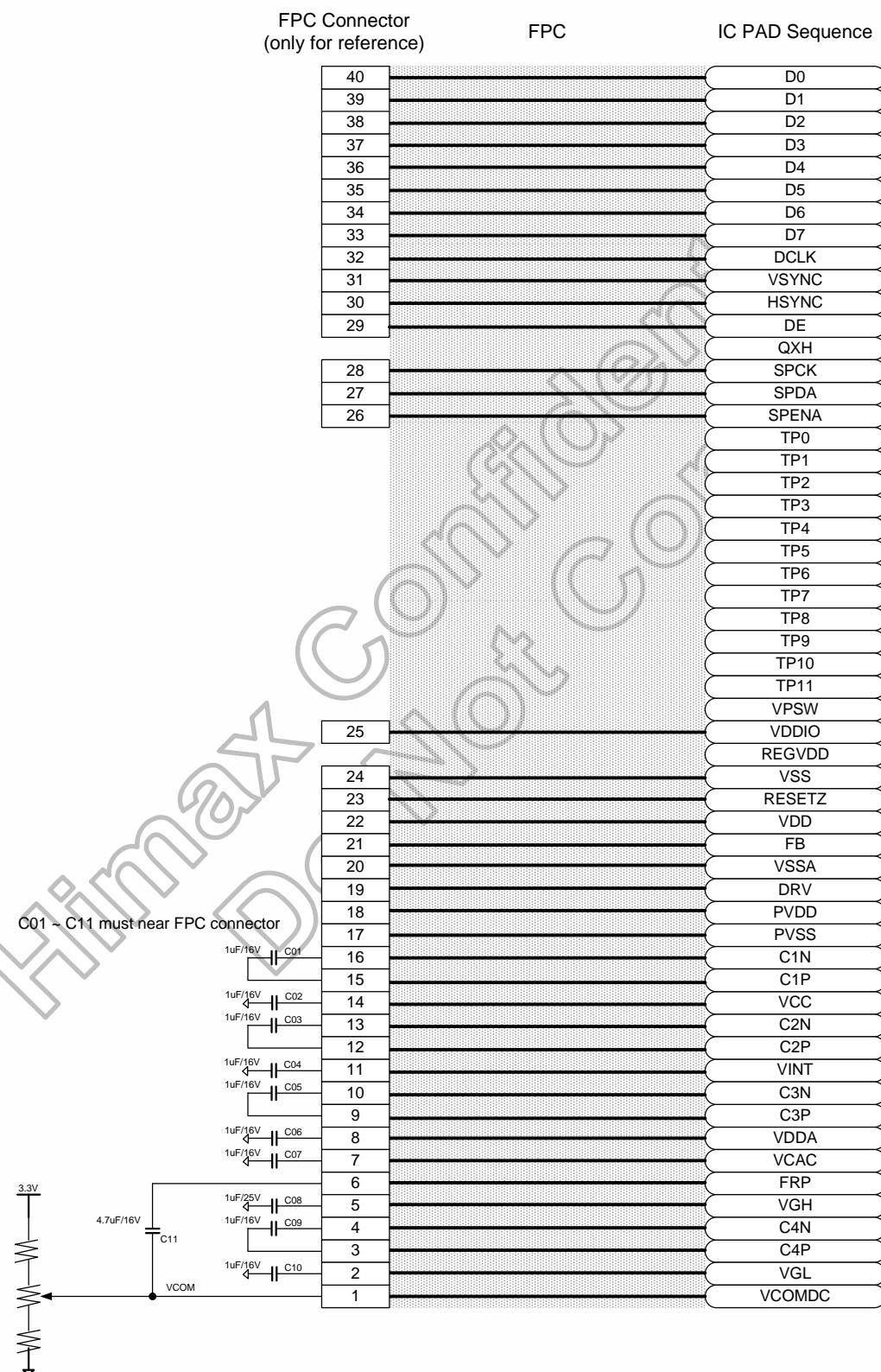


Figure 6. 4 External VCOM and Charge Pump Application Circuits

7. Register Description

Register	Function Description
R00	System Setting Register
R01	Timing Control Setting Register
R02	Operation Setting Register
R03	Data Format Setting Register
R04	Source Delay Setting Register
R05	Gate Delay Setting Register
R06	VCAC Setting Register
R07	Internal Function Setting Register
T00	PWM Function Setting Register
T02	VCOM DC Level Setting Register
T06	For OTP Read Only
T07	OTP Setting Register

Table 7. 1 Function Description

	Address							R/W	Data							
	D15	D14	D13	D12	D11	D10	D9		D8	D7	D6	D5	D4	D3	D2	D1
R00	0	0	0	0	0	0	1	—	—	—	—	—	SHDB	SHCB	STB	GRB
	—	—	—	—	—	—	—	—	—	—	—	0	1	1	1	1
R01	0	0	0	0	0	1	1	—	—	—	—	SWD2	SWD1	SWD0	DITB	DS
	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0	1
R02	0	0	0	0	1	0	1	—	—	—	—	—	Reserved	FPOL	UD	SHL
	—	—	—	—	—	—	—	—	—	—	0	0	0	1	1	1
R03	0	0	0	0	1	1	1	—	—	—	HSP	VSP	PAL	SEL2	SEL1	SELO
	—	—	—	—	—	—	—	—	—	0	0	0	0	0	0	1
R04	0	0	0	1	0	0	1	—	—	—	—	DDL4	DDL3	DDL2	DDL1	DDLO
	—	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0
R05	0	0	0	1	0	1	1	—	—	—	FRAD1	FRADO	HDL3	HDL2	HDL1	HDLO
	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R06	0	0	0	1	1	0	1	—	Reserved	Reserved	Reserved	Reserved	—	VSCL2	VSCL1	VSCL0
	—	—	—	0	0	0	0	—	0	0	0	0	—	1	0	1
R07	0	0	0	1	1	1	1	—	Reserved	Reserved	—	—	PALM	PFON	VLNC	LPF
	—	—	—	0	0	—	—	—	0	0	0	0	1	0	1	1
T00	0	0	1	0	0	0	1	—	—	—	—	PDTY1	PDTY0	FBV2	FBV1	FBV0
	—	—	—	—	—	—	—	—	—	0	0	0	1	0	0	0
T02	0	0	1	0	1	0	1	—	—	VDCEN	VCOMDC5	VCOMDC4	VCOMDC3	VCOMDC2	VCOMDC1	VCOMDC0
	—	—	—	—	0	1	—	—	0	1	0	0	0	0	0	0
T06	0	0	1	1	1	0	0	—	—	—	—	—	Reserved	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
T7	0	0	1	1	1	1	1	—	SET_VCC1	SET_VCC0	SEL_VCM	GHLENB	PPR	VPS	PWE	POR
	—	—	0	0	0	0	—	—	0	0	0	0	0	0	0	0

Note 1 : “—” = don't care

Note 2 : Please keep all the reserved registers at the default value.

Note 3 : T06 is read only for OTP.

Table 7. 2 Register Description

7.1 Function control register (R00h)

	Address						RW	Data								
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0
R00	0	0	0	0	0	0	1	—	—	—	—	—	SHDB	SHCB	STB	GRB

GRB	Global Reset
L	The Controller is resets, the Charge Pump and PWM is off.
H	Normal operation; Default setting .

STB	Stand By Mode
L	TCON, SD, GD, Charge Pump and PWM are off.
H	Normal operation; Default setting .

SHCB	Charge Pump shutdown signal
L	The Charge Pump is off
H	The Charge Pump is on; Default setting .

SHDB	PWM shutdown signal
L	The PWM is off. Default Setting .
H	The PWM is on.

Note: The function disable, the DRV output be VSS.

7.2 Function control register (R01h)

	Address						R/W	Data								
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0
R01	0	0	0	0	0	1	1	—	—	—	—	SWD2	SWD1	SWD0	DITB	DS

SWD [2:0] Control and switch the relationship between the R, G, B and outputs.
(Default = 000)

SWD[2:0]=000, DS=1				SWD[2:0]=001, DS=1				SWD[2:0]=01X, DS=1							
G1	G	B	R	G	B	R	G	G1	B	R	G	B	R	G	B
G2	R	G	B	R	G	B	R	G2	G	B	R	G	B	R	G
G3	G	B	R	G	B	R	G	G3	B	R	G	B	R	G	B
G4	R	G	B	R	G	B	R	G4	G	B	R	G	B	R	G
G237	G	B	R	G	B	R	G	G237	B	R	G	B	R	G	B
G238	R	G	B	R	G	B	R	G238	G	B	R	G	B	R	G
G239	G	B	R	G	B	R	G	G239	B	R	G	B	R	G	B
G240	R	G	B	R	G	B	R	G240	G	B	R	G	B	R	G
SWD[2:0]=100, DS=1				SWD[2:0]=101, DS=1				SWD[2:0]=11X, DS=1							
G1	R	G	B	R	G	B	R	G1	G	B	R	G	B	R	G
G2	G	B	R	G	B	R	G	G2	B	R	G	B	R	G	B
G3	R	G	B	R	G	B	R	G3	G	B	R	G	B	R	G
G4	G	B	R	G	B	R	G	G4	B	R	G	B	R	G	B
G237	R	G	B	R	G	B	R	G237	G	B	R	G	B	R	G
G238	G	B	R	G	B	R	G	G238	B	R	G	B	R	G	B
G239	R	G	B	R	G	B	R	G239	G	B	R	G	B	R	G
G240	G	B	R	G	B	R	G	G240	B	R	G	B	R	G	B
SWD[2:0]=XXX, DS=0															
G1	R	G	B	R	G	B	R	G1	B	R	G	B	R	G	B
G2	R	G	B	R	G	B	R	G2	R	G	B	R	G	B	G
G3	R	G	B	R	G	B	R	G3	B	R	G	B	R	G	B
G4	R	G	B	R	G	B	R	G4	R	G	B	R	G	B	G
G237	R	G	B	R	G	B	R	G237	B	R	G	B	R	G	B
G238	R	G	B	R	G	B	R	G238	R	G	B	R	G	B	G
G239	R	G	B	R	G	B	R	G239	B	R	G	B	R	G	B
G240	R	G	B	R	G	B	R	G240	R	G	B	R	G	B	G

Figure 6. 1 SWD [2:0] V.S. Color Filter Arrangement

DITB	Delta/Stripe Mode Setting
L	Dithering enable. Default setting.
H	Dithering disable.

DS	Delta/Stripe Mode Setting
L	Stripe mode.
H	Delta mode. Default setting. Default setting.

7.3 Function control register (R02h)

	Address						R/W	Data									
	D15	D14	D13	D12	D11	D10		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R02	0	0	0	0	1	0	1	—	—	—	—	—	—	Reserved	FPOL	UD	SHL

FPOL	Control the Inversion of FRP Depending on the Polarity of the Gamma Correction
L	FRP inverted with respect to the polarity of the gamma correction. Default setting.
H	FRP in phase with the polarity of the gamma correction.

UD	UP/DOWN Scan Control of Gate Driver
L	Scan up. G240->G239->.....->G2->G1.
H	Scan down. G1->G2->.....->G239->G240. Default setting.

SHL	Left/Right Selection
L	Shift left. S480->S479->.....->S2->S1.
H	Shift right. S1->S2->.....->S479->S480. Default setting.

7.4 Function control register (R03h)

	Address						R/W	Data									
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0	
R03	0	0	0	0	1	1	1	—	—	—	HSP	VSP	PAL	SEL2	SEL1	SEL0	

HSP Hsync Polarity Control	
L	Negative polarity. Default setting.
H	Positive polarity.

VSP Vsync Polarity Control	
L	Negative polarity. Default setting.
H	Positive polarity.

PAL NTSC/PAL Selection Signal	
L	Input data format is NTSC. Default setting.
H	Input data format is PAL.

Select Input Data Format, **Default = 000**.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Serial-RGB data format	9.7MHz
0	0	1	Serial-320RGB data format (dummy mode)	24.54MHz
0	1	0	Serial-360RGB data format (dummy mode)	27MHz
0	1	1	YUV mode A data format	24.54MHz
1	0	0	YUV mode A data format	27MHz
1	0	1	YUV mode B data format	24.54MHz
1	1	0	YUV mode B data format	27MHz
1	1	1	CCIR 656 data format(720RGB)	27MHz

7.5 Function control register (R04h)

	Address						R/W	Data									
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0	
R04	0	0	0	1	0	0	1	—	—	—	—	DDL4	DDL3	DDL2	DDL1	DDL0	

Select the data delay timing, Default = 00000.

DDL4	DDL3	DDL2	DDL1	DDL0	Delay	Unit
0	0	0	0	0	0	
0	0	0	0	1	1	
0	0	0	1	0	2	
0	0	0	1	1	3	
0	0	1	0	0	4	
0	0	1	0	1	5	
0	0	1	1	0	6	
0	0	1	1	1	7	
0	1	0	0	0	8	
0	1	0	0	1	9	
0	1	0	1	0	10	
0	1	0	1	1	11	
0	1	1	0	0	12	
0	1	1	0	1	13	
0	1	1	1	0	14	
0	1	1	1	1	15	
1	0	0	0	0	-1	
1	0	0	0	1	-2	
1	0	0	1	0	-3	
1	0	0	1	1	-4	
1	0	1	0	0	-5	
1	0	1	0	1	-6	
1	0	1	1	0	-7	
1	0	1	1	1	-8	
1	1	0	0	0	-9	
1	1	0	0	1	-10	
1	1	0	1	0	-11	
1	1	0	1	1	-12	
1	1	1	0	0	-13	
1	1	1	0	1	-14	
1	1	1	1	0	-15	
1	1	1	1	1	-16	

DCLK Period

7.6 Function control register (R05h)

	Address						R/W	Data								
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0
R05	0	0	0	1	0	1	1	—	—	—	FRAD1	FRAD0	HDL3	HDL2	HDL1	HDL0

FRAD1	FRAD0	OEA Function
0	0	Display Start @ HDL delay for Odd field and @ HDL for Even field. Default setting
0	1	Display Start @ HDL delay for Odd field and @ HDL+1 for Even field.
1	X	Display Start @ HDL+1 delay for Odd field and @ HDL+1 for Even field.

Select the first active line delay timing, **Default = 0000**.

HDL3	HDL2	HDL1	HDL0	Delay	Unit
0	0	0	0	0	HSYNC. Period.
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	-1	
1	0	1	0	-2	
1	0	1	1	-3	
1	1	0	0	-4	
1	1	0	1	-5	
1	1	1	0	-6	
1	1	1	1	-7	

7.7 Function control register (R06h)

	Address						R/W	Data								
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0
R06	0	0	0	1	1	0	1	—	Reserved	Reserved	Reserved	Reserved	—	VSCL2	VSCL1	VSCL0
								0	0	0	0	0	—	1	0	1

VCOM amplitude control, Default = 101.

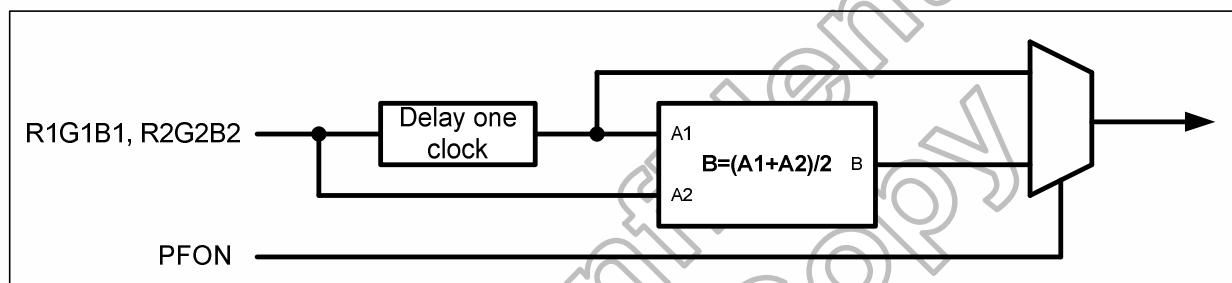
VSCL2	VSCL1	VSCL0	VCAC Level	Unit
0	0	0	5.0	V
0	0	1	4.8	
0	1	0	4.6	
0	1	1	4.4	
1	0	0	4.2	
1	0	1	4.0	
1	1	0	3.8	
1	1	1	3.6	

7.8 Function control register (R07h)

	Address						R/W	Data									
	D15	D14	D13	D12	D11	D10		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R07	0	0	0	1	1	1	1	—	Reserved	Reserved	—	—	PALM	PFON	VLINC	LPF	

PALM PAL Selection Signal (only available when PAL=H)	
L	Input data format is PAL 1/6, 8(280 active lines). Default setting.
H	Input data format is PAL 1/6(288 active lines).

PFON Pre-filter setting	
L	Pre-filter off.
H	Pre-filter on. Default setting.



VLINC YUV Vertical Line Function	
L	Vertical are 240 lines. Default setting.
H	Vertical are 234 lines. NTSC : 240 lines scaling to 234 – skip 6 lines. (1/40) PAL : 288 lines scaling to 234 – skip 54 lines. (3/16) (PALM='H') PAL : 280 lines scaling to 234 – skip 46 lines. (1/16) (PALM='L')

LPF YUV Low Pass Filter Function	
L	YUV Low Pass Filter disable
H	YUV Low Pass Filter enable. Default setting.

7.9 Function control register (T00h)

	Address							R/W	Data								
	D15	D14	D13	D12	D11	D10	D9		D8	D7	D6	D5	D4	D3	D2	D1	D0
T00	0	0	1	0	0	0	1		—	—	—	—	PDTY1	PDTY0	FBV2	FBV1	FBV0
									—	—	—	—	0	0	1	0	0

PWM maximal duty control, **Default = 00**.

PDTY1	PDTY0	PWM Duty Cycle	Unit
0	0	75	% V
0	1	55	
1	0	60	
1	1	65	

FB voltage adjust, **Default = 100**.

FBV2	FBV1	FBV0	FB Voltage Level	Unit
0	0	0	0.45	V
0	0	1	0.50	
0	1	0	0.55	
0	1	1	0.59	
1	0	0	0.64	
1	0	1	0.69	
1	1	0	0.73	
1	1	1	0.78	

7.10 Function control register (T02h)

	Address						RW	Data									
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0	
T02	0	0	1	0	1	0	1	—	—	VDCEN	VCOMDC5	VCOMDC4	VCOMDC3	VCOMDC2	VCOMDC1	VCOMDC0	

VDCEN	Setting FRP Output to Add DC Level
L	External VCOM DC. Default setting.
H	Internal VCOM DC.

VCOM DC level adjustment. Default =010000.

VCOMDC5	VCOMDC4	VCOMDC3	VCOMDC2	VCOMDC1	VCOMDC0	VCOM DC level adjustment	Unit
0	0	0	0	0	0	0.48	
0	0	0	0	0	1	0.50	
0	0	0	0	1	0	0.52	
0	0	0	0	1	1	0.54	
0	0	0	1	0	0	0.56	
0	0	0	1	0	1	0.58	
0	0	0	1	1	0	0.60	
0	0	0	1	1	1	0.62	
0	0	1	0	0	0	0.64	
0	0	1	0	0	1	0.66	
0	0	1	0	1	0	0.68	
0	0	1	0	1	1	0.70	
0	0	1	1	0	0	0.72	
0	0	1	1	0	1	0.74	
0	0	1	1	1	0	0.76	
0	0	1	1	1	1	0.78	
0	1	0	0	0	0	0.80	
0	1	0	0	0	1	0.82	
0	1	0	0	1	0	0.84	
0	1	0	0	1	1	0.86	
0	1	0	1	0	0	0.88	
0	1	0	1	0	1	0.90	
0	1	0	1	1	0	0.92	
0	1	0	1	1	1	0.94	
0	1	1	0	0	0	0.96	
0	1	1	0	0	1	0.98	
0	1	1	0	1	0	1.00	
0	1	1	0	1	1	1.02	
0	1	1	1	0	0	1.04	
0	1	1	1	0	1	1.06	
0	1	1	1	1	0	1.08	
0	1	1	1	1	1	1.10	
1	0	0	0	0	0	1.12	
1	0	0	0	0	1	1.14	
1	0	0	0	1	0	1.16	
1	0	0	0	1	1	1.18	
1	0	0	1	0	0	1.20	
1	0	0	1	0	1	1.22	
1	0	0	1	1	0	1.24	
1	0	0	1	1	1	1.26	
1	0	1	0	0	0	1.28	
1	0	1	0	0	1	1.30	
1	0	1	0	1	0	1.32	
1	0	1	0	1	1	1.34	
1	0	1	1	0	0	1.36	
1	0	1	1	0	1	1.38	
1	0	1	1	1	0	1.40	
1	0	1	1	1	1	1.42	
1	1	0	0	0	0	1.44	
1	1	0	0	0	1	1.46	
1	1	0	0	1	0	1.48	
1	1	0	0	1	1	1.50	
1	1	0	1	0	0	1.52	
1	1	0	1	0	1	1.54	
1	1	0	1	1	0	1.56	
1	1	0	1	1	1	1.58	
1	1	1	0	0	0	1.60	
1	1	1	0	0	1	1.62	
1	1	1	0	1	0	1.64	
1	1	1	0	1	1	1.66	
1	1	1	1	0	0	1.68	
1	1	1	1	0	1	1.70	
1	1	1	1	1	0	1.72	
1	1	1	1	1	1	1.74	

V

7.11 Function control register (T06h)

	Address						R/W	Data								
	D15	D14	D13	D12	D11	D10		D9	D8	D7	D6	D5	D4	D3	D2	D1
T06	0	0	1	1	1	0	0	—	IND1	IND0	VCOMDC5	VCOMDC4	VCOMDC3	VCOMDC2	VCOMDC1	VCOMDC0

You can read T06 to check the VCOMDC [5:0] values of the OTP.

IND [1:0] = 11 → you can write OTP three times.

IND [1:0] = 10 → you can write OTP two times.

IND [1:0] = 01 → you can write OTP one times.

IND [1:0] = 00 → you can not write OTP again.

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7.12 Function control register (T07h)

	Address						R/W	Data								
	D15	D14	D13	D12	D11	D10		D8	D7	D6	D5	D4	D3	D2	D1	D0
T07	0	0	1	1	1	1	1	-	SET_VCC1	SET_VCC0	SEL_VCM	GHLENB	PPR	VPS	PWE	POR
								0	0	0	0	0	0	0	0	0

OTP Write sequence :

Step	Operation
01	Set T02 of the VCOMDC[5:0] values .
02	Set T07 = 8'hD0 .
03	Connect VGH=7.5V and VGL=0V . (VGH range = 7.25V ~ 7.75V) .
04	Set T07 = 8'hD8 .
05	Set T07 = 8'hDC .
06	Set T07 = 8'hDE . Wait 300us . (minimal time=300us)
07	Set T07 = 8'hDC .
08	Remove 7.5V from VGH and 0V from VGL .
00	Set T07 = 8'hD8 .
10	Set T07 = 8'hD0 .
11	Set T07 = 8'hD1 .
12	Set T07 = 8'h00 .

Note : Set T07 = **8'h00** ➔ the VCOMDC is adjusted by OTP. (Default setting)

Set T07 = **8'h20** ➔ the VCOMDC is adjusted by SPI.

8. Gamma Table

The output voltage is determined by the 6-bit digital input data and the 6γ correction reference voltage.

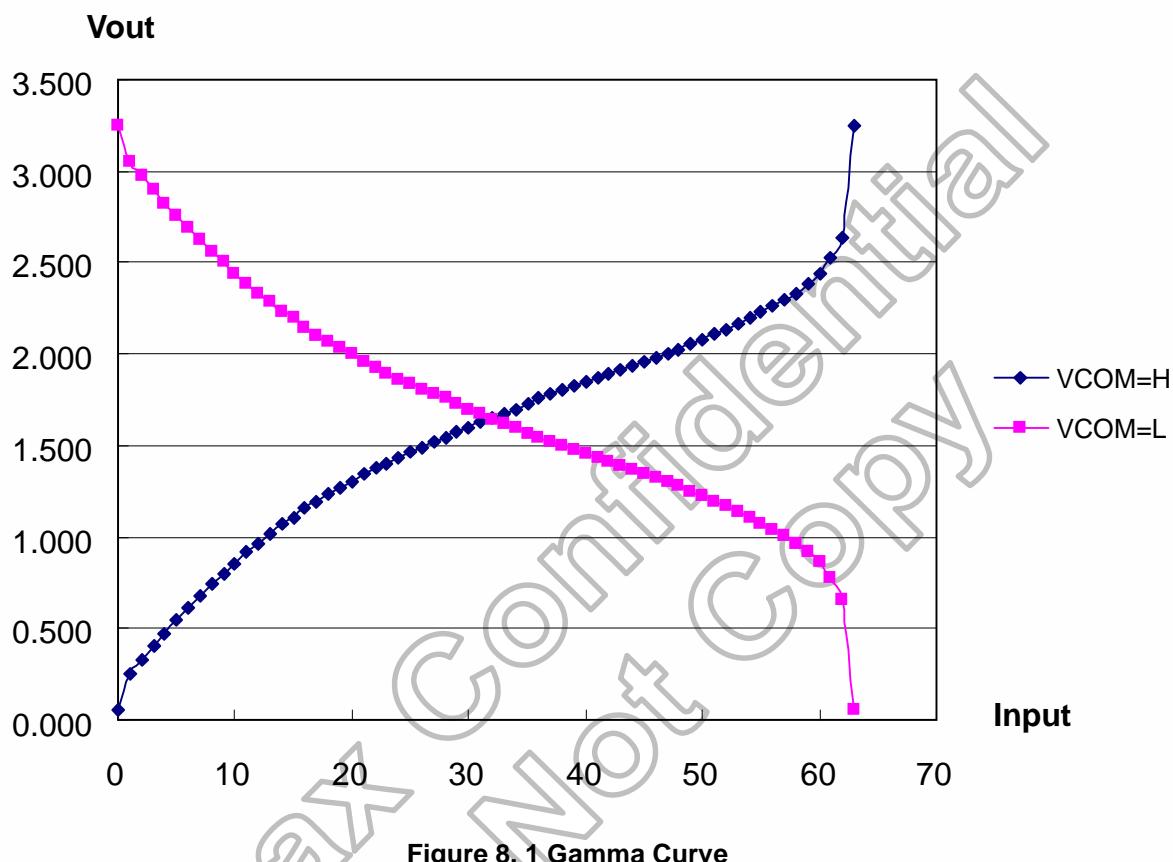


Figure 8.1 Gamma Curve

The actual output voltages for all 64 input data at positive and negative polarity is as shown on the following page.

※VDD=3.3V

Gray Level	VCOM=H
0	VDD X 0.016 = 0.0528
1	VDD X 0.076 = 0.2508
2	VDD X 0.100 = 0.3300
3	VDD X 0.122 = 0.4026
4	VDD X 0.144 = 0.4752
5	VDD X 0.166 = 0.5478
6	VDD X 0.184 = 0.6072
7	VDD X 0.206 = 0.6798
8	VDD X 0.224 = 0.7392
9	VDD X 0.242 = 0.7986
10	VDD X 0.260 = 0.8580
11	VDD X 0.278 = 0.9174
12	VDD X 0.294 = 0.9702
13	VDD X 0.310 = 1.0230
14	VDD X 0.326 = 1.0758
15	VDD X 0.336 = 1.1088
16	VDD X 0.350 = 1.1550
17	VDD X 0.362 = 1.1946
18	VDD X 0.374 = 1.2342
19	VDD X 0.386 = 1.2738
20	VDD X 0.396 = 1.3068
21	VDD X 0.406 = 1.3398
22	VDD X 0.416 = 1.3728
23	VDD X 0.426 = 1.4058
24	VDD X 0.436 = 1.4388
25	VDD X 0.442 = 1.4586
26	VDD X 0.452 = 1.4916
27	VDD X 0.458 = 1.5114
28	VDD X 0.468 = 1.5444
29	VDD X 0.478 = 1.5774
30	VDD X 0.484 = 1.5972
31	VDD X 0.494 = 1.6302
32	VDD X 0.504 = 1.6632
33	VDD X 0.510 = 1.6830
34	VDD X 0.516 = 1.7028
35	VDD X 0.526 = 1.7358
36	VDD X 0.532 = 1.7556
37	VDD X 0.542 = 1.7886
38	VDD X 0.548 = 1.8084
39	VDD X 0.554 = 1.8282
40	VDD X 0.560 = 1.8480
41	VDD X 0.566 = 1.8678
42	VDD X 0.572 = 1.8876
43	VDD X 0.578 = 1.9074
44	VDD X 0.588 = 1.9404
45	VDD X 0.594 = 1.9602
46	VDD X 0.600 = 1.9800
47	VDD X 0.606 = 1.9998
48	VDD X 0.612 = 2.0196
49	VDD X 0.622 = 2.0526
50	VDD X 0.628 = 2.0724
51	VDD X 0.638 = 2.1054
52	VDD X 0.648 = 2.1384
53	VDD X 0.654 = 2.1582
54	VDD X 0.664 = 2.1912
55	VDD X 0.674 = 2.2242
56	VDD X 0.684 = 2.2572
57	VDD X 0.694 = 2.2902
58	VDD X 0.706 = 2.3298
59	VDD X 0.722 = 2.3826
60	VDD X 0.738 = 2.4354
61	VDD X 0.764 = 2.5212
62	VDD X 0.800 = 2.6400
63	VDD X 0.984 = 3.2472

Gray Level	VCOM=L
0	VDD X 0.984 = 3.2472
1	VDD X 0.924 = 3.0492
2	VDD X 0.900 = 2.9700
3	VDD X 0.878 = 2.8974
4	VDD X 0.856 = 2.8248
5	VDD X 0.834 = 2.7522
6	VDD X 0.816 = 2.6928
7	VDD X 0.794 = 2.6202
8	VDD X 0.776 = 2.5608
9	VDD X 0.758 = 2.5014
10	VDD X 0.740 = 2.4420
11	VDD X 0.722 = 2.3826
12	VDD X 0.706 = 2.3298
13	VDD X 0.690 = 2.2770
14	VDD X 0.674 = 2.2242
15	VDD X 0.664 = 2.1912
16	VDD X 0.650 = 2.1450
17	VDD X 0.638 = 2.1054
18	VDD X 0.626 = 2.0658
19	VDD X 0.614 = 2.0262
20	VDD X 0.604 = 1.9932
21	VDD X 0.594 = 1.9602
22	VDD X 0.584 = 1.9272
23	VDD X 0.574 = 1.8942
24	VDD X 0.564 = 1.8612
25	VDD X 0.558 = 1.8414
26	VDD X 0.548 = 1.8084
27	VDD X 0.542 = 1.7886
28	VDD X 0.532 = 1.7556
29	VDD X 0.522 = 1.7226
30	VDD X 0.516 = 1.7028
31	VDD X 0.506 = 1.6698
32	VDD X 0.496 = 1.6368
33	VDD X 0.490 = 1.6170
34	VDD X 0.484 = 1.5972
35	VDD X 0.474 = 1.5642
36	VDD X 0.468 = 1.5444
37	VDD X 0.458 = 1.5114
38	VDD X 0.452 = 1.4916
39	VDD X 0.446 = 1.4718
40	VDD X 0.440 = 1.4520
41	VDD X 0.434 = 1.4322
42	VDD X 0.428 = 1.4124
43	VDD X 0.422 = 1.3926
44	VDD X 0.412 = 1.3596
45	VDD X 0.406 = 1.3398
46	VDD X 0.400 = 1.3200
47	VDD X 0.394 = 1.3002
48	VDD X 0.388 = 1.2804
49	VDD X 0.378 = 1.2474
50	VDD X 0.372 = 1.2276
51	VDD X 0.362 = 1.1946
52	VDD X 0.352 = 1.1616
53	VDD X 0.346 = 1.1418
54	VDD X 0.336 = 1.1088
55	VDD X 0.326 = 1.0758
56	VDD X 0.316 = 1.0428
57	VDD X 0.306 = 1.0098
58	VDD X 0.294 = 0.9702
59	VDD X 0.278 = 0.9174
60	VDD X 0.262 = 0.8646
61	VDD X 0.236 = 0.7788
62	VDD X 0.200 = 0.6600
63	VDD X 0.016 = 0.0528

9. DC Characteristics

9.1 Absolute maximum rating (VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDDIO	-0.3	-	+7.0	V
Power supply voltage 2	VDD	-0.3	-	+7.0	V
Power supply voltage 3	PVDD	-0.3	-	+7.0	V
Logic Output Voltage	V_{OUT1}	-0.3	-	+7.0	V
Input voltage	V_{IN}	-0.3	-	$VDDIO+0.3$	V
Operation temperature	T_{OPR}	-35	-	+85	°C
Storage temperature	T_{STG}	-55	-	+125	°C

Note: ⁽¹⁾ All of the voltages listed above are with respective to VSS=0V.

⁽²⁾ Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

9.2 DC electrical characteristics (VSS=0V, TA=25°C)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage (1)	VDDIO	1.8	3.3	3.6	V	-
Power supply voltage (2)	VDD	3.0	3.3	3.6	V	-
Power supply voltage (3)	PVDD	3.0	3.3	3.6	V	-
Digital Standby current 1	I_{STBY1}	-	-	100	µA	VDDIO, STB="0", all functions are shutdown
Digital Standby current 2	I_{STBY2}	-	-	10	µA	VDD, STB="0", all functions are shutdown
Analog Standby current	I_{STBY3}	-	-	100	µA	PVDD, STB="0", all functions are shutdown
Digital operating current 1	I_{VDDIO}	-	-	2	mA	VDDIO=3.3V, CCIR656 NTSC mode, $f_{DCLK}=27MHz$, pixel on/off pattern
Digital operating current 2	I_{VDD}	-	-	2	mA	VDD=3.3V, $f_{DCLK}=27MHz$,
Analog operating current	I_{PVDD}	-	-	4	mA	PVDD=3.3V, $f_{DCLK}=27MHz$, black pattern.
LED Current	I_{LED}	-	25	28	mA	-
VFB	V_{FB}	0.40	0.60	0.75	V	-

(VDD1=VDD2=2.7V~3.3V, PVDD=3.0V~3.6V, VSS=PVSS=0V, TA=25°C)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VINT Output Voltage	VINT	5.2	5.4	5.6	V	VDV[1:0]=00 I-load=1μA~3mA
VDDA Adjust voltage	VDDA	4.4	5.0	5.0	V	I-load=1μA~1mA
VDDA Margin of error		-	+/- 100	-	mV	
VGH Output Voltage	VGH	14.0	15.0	16.0	V	I-load=1μA~100μA, when VPSW=0
VGL Output Voltage	VGL	-11.0	-10.0	-9.0	V	I-load=-1μA~-100μA, when VPSW=0
VCAC Adjust voltage	VCAC	3.6	4.0	5.0	V	I-load=1μA~1.5mA
VCAC Margin of error		-	+/- 100	-	mV	
VCOMDC Adjust voltage	VCOMDC	0.48	0.80	1.74	V	
VCOMDC Margin of error		-	+/- 100	-	mV	
Low level input voltage (VDDIO=2.5V~3.6V)	V _{IL}	0	-	0.3 VDDIO	V	DCLK, HSYNC, VSYNC, D[7:0], DE, SPCK, SPDA, SPENA, RESETZ, VPSW, REGVDD.
High level input voltage (VDDIO=2.5V~3.6V)	V _{IH}	0.7 VDDIO	-	VDDIO	V	DCLK, HSYNC, VSYNC, D[7:0], DE, SPCK, SPDA, SPENA, RESETZ, VPSW, REGVDD.
Low level input voltage (VDDIO=1.8V~2.5V)	V _{IL}	0	-	0.2 VDDIO	V	DCLK, HSYNC, VSYNC, D[7:0], DE, SPCK, SPDA, SPENA, RESETZ, VPSW, REGVDD.
High level input voltage (VDDIO=1.8V~2.5)	V _{IH}	0.8 VDDIO	-	VDDIO	V	DCLK, HSYNC, VSYNC, D[7:0], DE, SPCK, SPDA, SPENA, RESETZ, VPSW, REGVDD.
High level input leakage current 1	I _{IH1}	-	-	1	μA	DCLK, HSYNC, VSYNC, REGVDD, RESTEZ, SPCK, SPENA
High level input leakage current 2	I _{IH2}	-	-	100	μA	D[7:0], DE, SPDA, VPSW, TP9, TP8.
Low level input leakage current 1	I _{IL1}	-1	-	-	μA	DCLK, D[7:0], DE, SPDA, VPSW, TP9, TP8.
Low level input leakage current 2	I _{IL2}	-100	-	-	μA	HSYNC, VSYNC, REGVDD, RESTEZ, SPCK, SPENA
Pull high resistance	R _H	50	100	200	kΩ	HSYNC, VSYNC, REGVDD, RESTEZ, SPCK, SPENA
Pull low resistance	R _L	50	100	200	kΩ	D[7:0], DE, SPDA, VPSW, TP9, TP8.
High Level Output Voltage	V _{OH}	0.9 VDDIO	-	-	V	QXH
Low Level Output Voltage	V _{OL}	-	-	0.1 VDDIO	V	QXH
Output voltage deviation	V _{VD}	-	±20	-	mV	S1 ~ S480, V _O =0.1~4.9V,
DC offset	V _{OS}	-	±20	-	mV	S1 ~ S480, V _O =0.1~4.9V,
Output leakage current	I _O	-	-	±1	μA	S1 to S480 at high impedance
Source high-level output current	I _{OHS}	20	40	-	μA	S1 ~ S480, V _O =4.0V vs. 3.5V, VDDA=5V
Source low-level output current	I _{OHS}	20	40	-	μA	S1 ~ S480, V _O =1.0V vs. 1.5V, VDDA=5V
Gate high-level output resistance	R _{OHG}	-	-	1000	Ω	G1 ~ G240, V _O =VGH-0.5V
Gate low-level output resistance	R _{OLG}	-	-	1000	Ω	G1 ~ G240, V _O =VGL+0.5V
FRP high-level output resistance	R _{OHF}	-	-	90	Ω	FRP, I _O = 1mA
FRP low-level output resistance	R _{OLF}	-	-	90	Ω	FRP, I _O = -1mA

10. AC Characteristics

10.1 Timing conditions

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Delay between Hsync and DCLK	Thc	-	-	1	DCLK
Hsync width	Twh	1	-	-	DCLK
Vsync width	Twv	1	-	-	DCLK
Vsync setup time	Tvst	12	-	-	ns
Vsync hold time	Tvh	12	-	-	ns
Hsync setup time	Thst	12	-	-	ns
Hsync hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
DE set-up time	Tesu	12	-	-	ns
Vsync period NTSC	Tv	250	262/262.5	360	Th
Vsync period PAL	Tv	300	312/312.5	360	Th
Hsync to Vsync time for ODD field	T _{HV_O}	-4	-	+4	DCLK
Hsync to Vsync time for EVEN field	T _{HV_E}	-	0.5	-	Th
S/D output stable time	Tst	-	-	30	μs
G/D output stable time	Tgst	-	-	2	μs

Serial communication

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial clock period	Tsck	100	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	40	-	-	ns
Serial data setup time	Tist	40	-	-	ns
Serial data hold time	Tihd	40	-	-	ns
SPENB setup time	Tcst	40	-	-	ns
SPENB data hold time	Tchd	40	-	-	ns
Chip select distinguish	Tcd	1	-	-	μs

10.2 Operating mode dependent AC characteristic

Serial RGB Mode, SEL [2:0]=[000]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	8	9.7	12	MHz
HSYNC period	Th	580	616	800	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	56	-	DCLK
Delay from Hsync to Gate output	Thgo	-	45	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	19	-	DCLK
Delay from Hsync to FRP	Thf	-	56	-	DCLK
Delay from Hsync to first dot data input (SYNC mode)	Ths	84	100	115	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

Serial 320RGB Mode, SEL [2:0]=[001]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	16	24.54	27	MHz
HSYNC period	Th	1472	1560	2000	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	143	-	DCLK
Delay from Hsync to Gate output	Thgo	-	113	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	48	-	DCLK
Delay from Hsync to FRP	Thf	-	143	-	DCLK
Delay from Hsync to 1st data input (for SYNC mode)	Ths	237	253	268	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

Serial 360RGB Mode, SEL [2:0]=[010]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	16	27	29.7	MHz
HSYNC period at NTSC Mode	Th	1620	1716	2000	DCLK
HSYNC period at NTSC PAL	Th	1620	1728	2000	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	143	-	DCLK
Delay from Hsync to Gate output	Thgo	-	113	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	48	-	DCLK
Delay from Hsync to FRP	Thf	-	143	-	DCLK
Delay from Hsync to 1st data input (for SYNC mode)	Ths	237	253	268	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

10.3 Operating mode dependent AC characteristic

YUV Mode, SEL [2:0]=[011, 101]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	16	24.54	27	MHz
Hsync period	Th	1472	1560	2000	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	143	-	DCLK
Delay from Hsync to Gate output	Thgo	-	113	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	48	-	DCLK
Delay from Hsync to FRP	Thf	-	143	-	DCLK
Delay from Hsync to 1st data input	Ths	236	252	267	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

YUV Mode, SEL [2:0]=[100, 110]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	16	27	29.7	MHz
Hsync period at NTSC Mode	Th	1620	1716	2000	DCLK
Hsync period at NTSC PAL	Th	1620	1728	2000	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso	-	143	-	DCLK
Delay from Hsync to Gate output	Thgo	-	113	-	DCLK
Delay from Hsync to Gate output off	Thgz	-	48	-	DCLK
Delay from Hsync to FRP	Thf	-	143	-	DCLK
Delay from Hsync to 1st data input	Ths	236	252	267	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

10.4 Operating mode dependent AC characteristic

CCIR656 Mode, SEL [2:0]=[111]

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fclk	16	27	29.7	MHz
Hsync period at NTSC Mode	Th	1620	1716	2000	DCLK
Hsync period at NTSC PAL	Th	1620	1728	2000	DCLK
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso	-	171	-	DCLK
Delay from CCIR_H to Gate output	Thgo	-	141	-	DCLK
Delay from CCIR_H to Gate output off	Thgz	-	76	-	DCLK
Delay from CCIR_H to FRP	Thf	-	171	-	DCLK
Delay from Hsync to 1st data input	Ths	260	273	291	DCLK
Delay from Vsync to first line data input	Tvbp_o	6	13	21	Th
Delay from Vsync to first line data input	Tvbp_e	6.5	13.5	21.5	Th

11. Waveform

11.1 Timing format: serial communication timing:

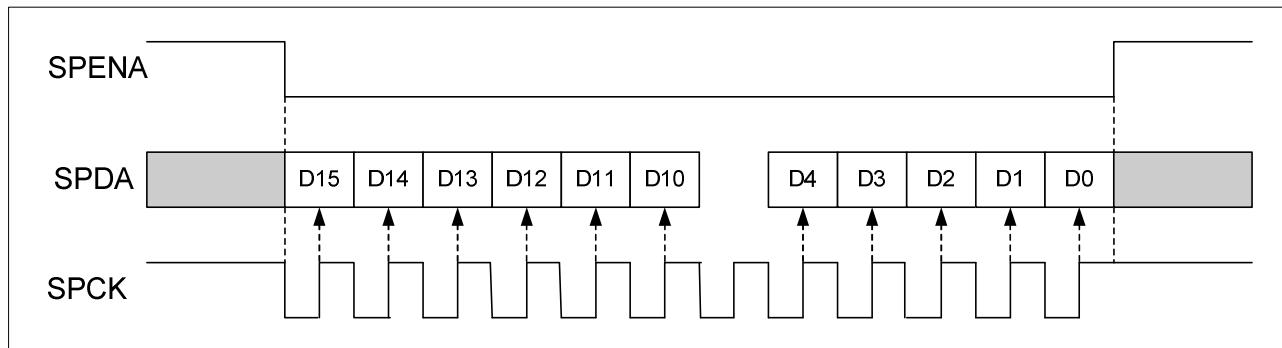


Figure 11.1 SPI Timing Diagram

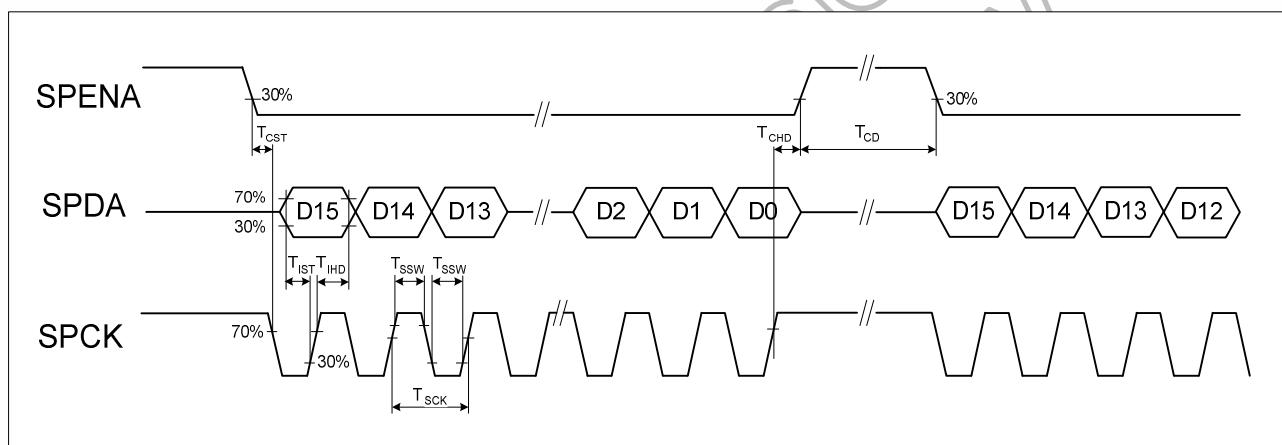


Figure 11.2 SPI Timing Diagram

11.2 Clock and data input timing diagram

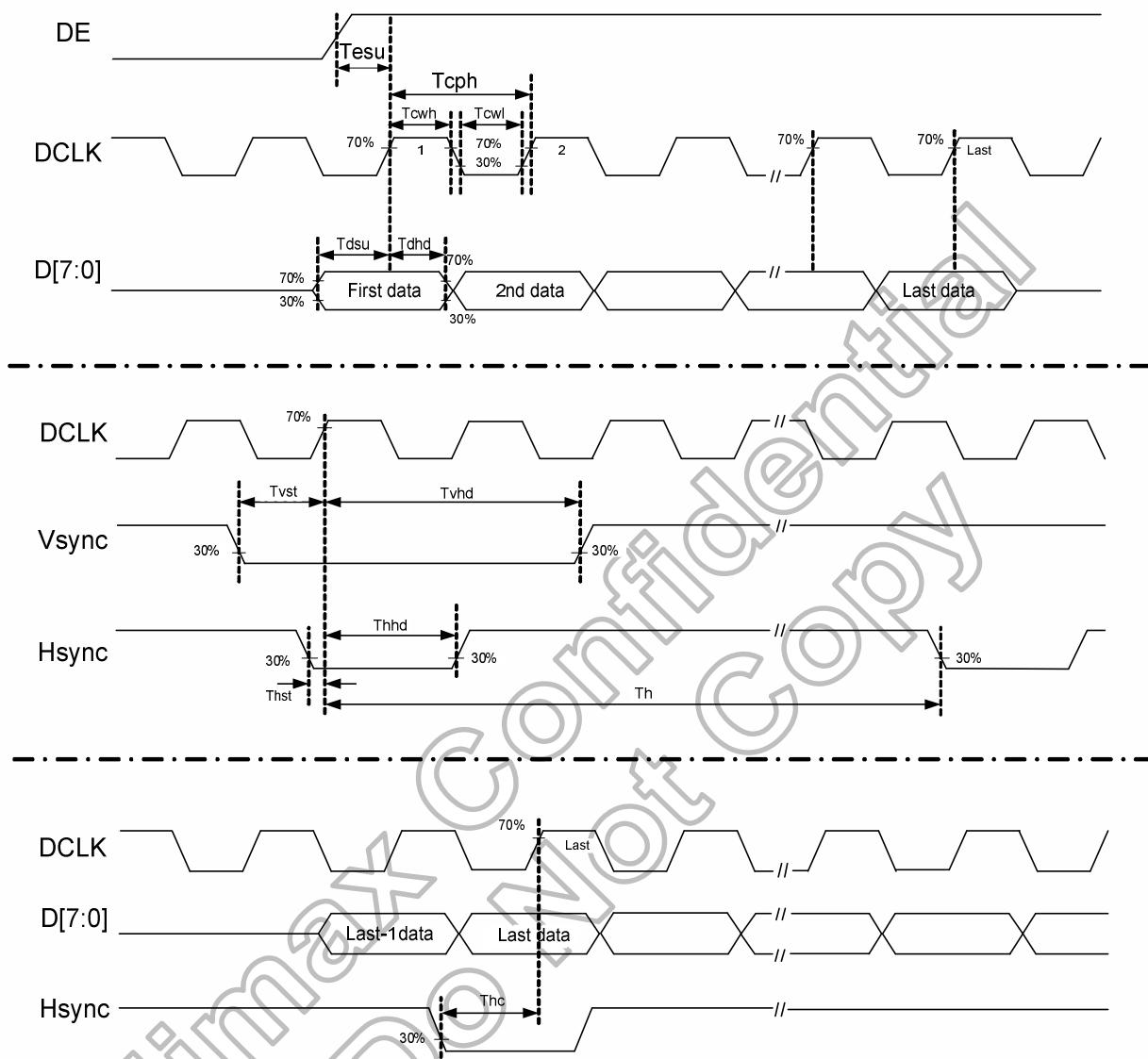


Figure 11.3 Clock and Data Input Timing Diagram

11.3 Source driver output timing chart

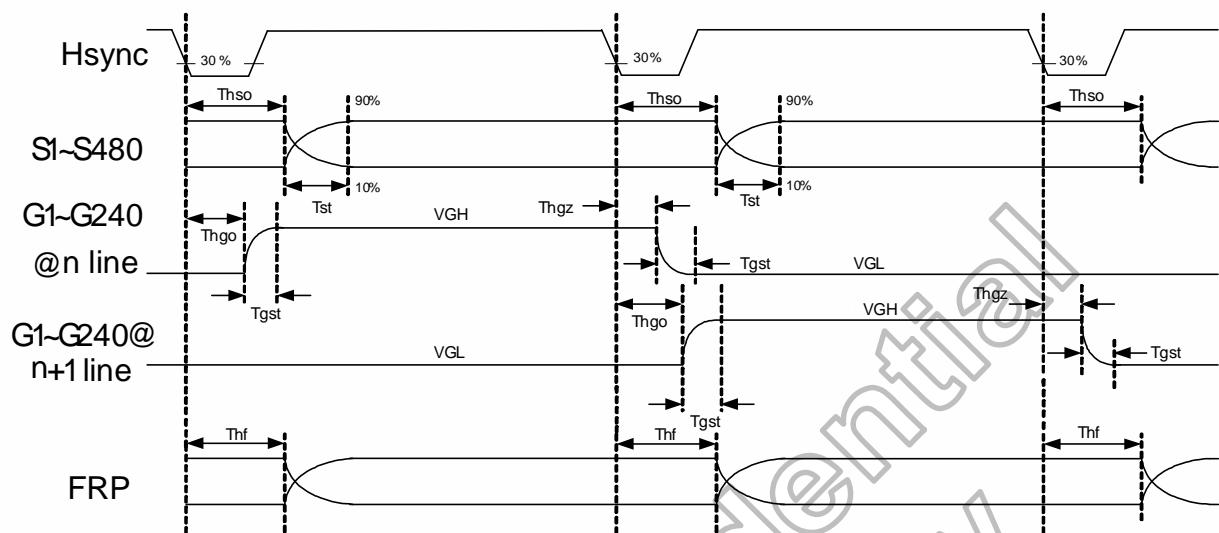


Figure 11. 4 Source Driver and VCOM Output Timing Chart

11.4 Vertical input timing

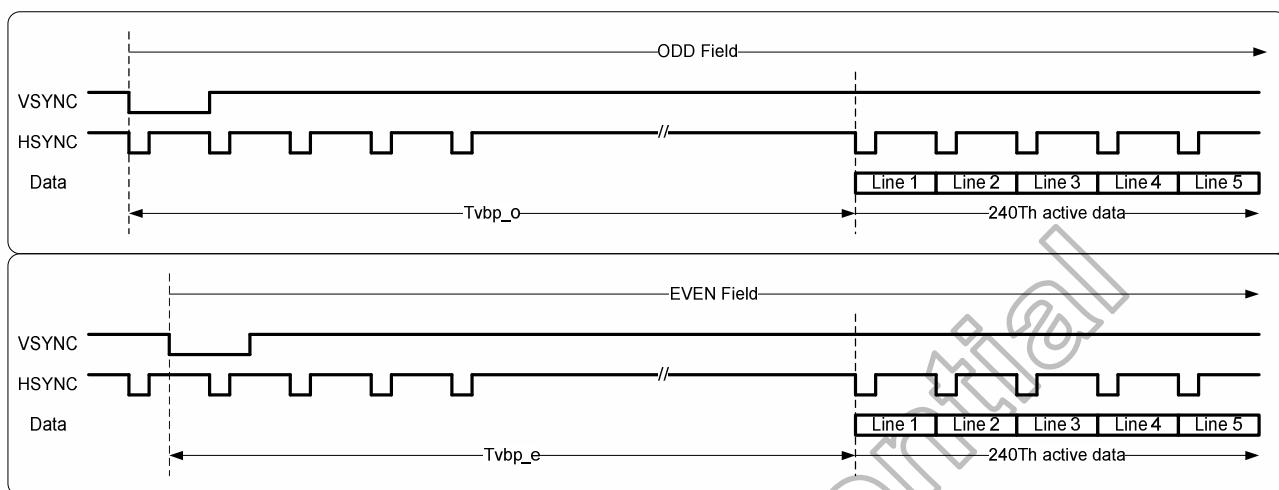


Figure 11.5 Vertical Input Timing (RGB, RGBD, YUV mode, CCIR656)

11.5 Input data format timing

11.5.1 Serial RGB data format

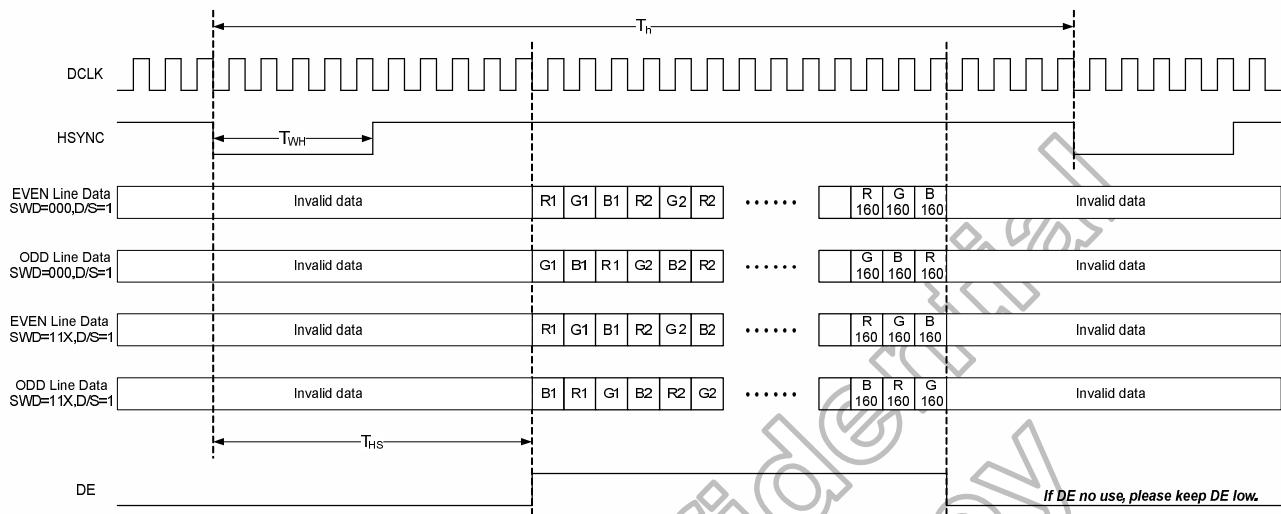


Figure 11. 6 Serial RGB Data Format

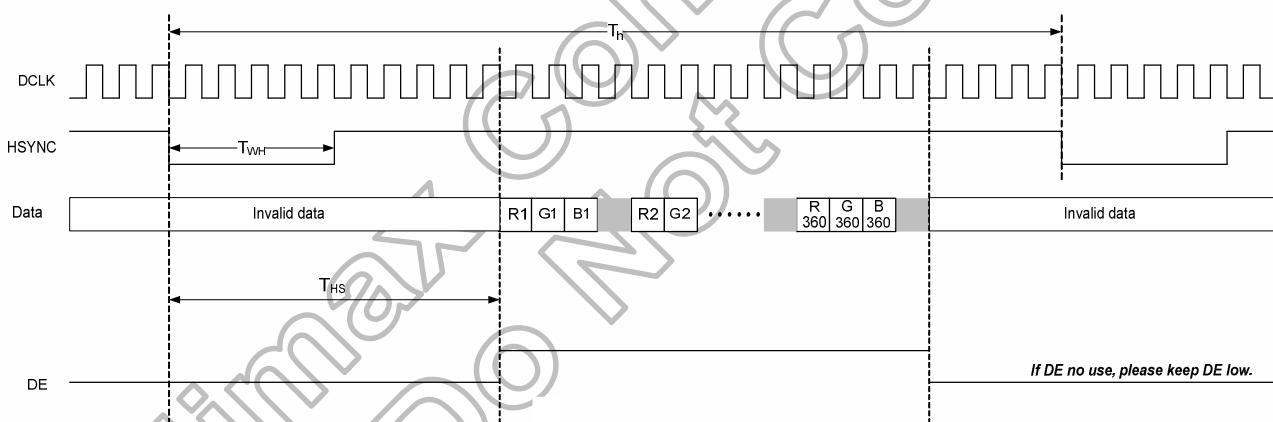


Figure 11. 7 Serial 360RGB Data Format

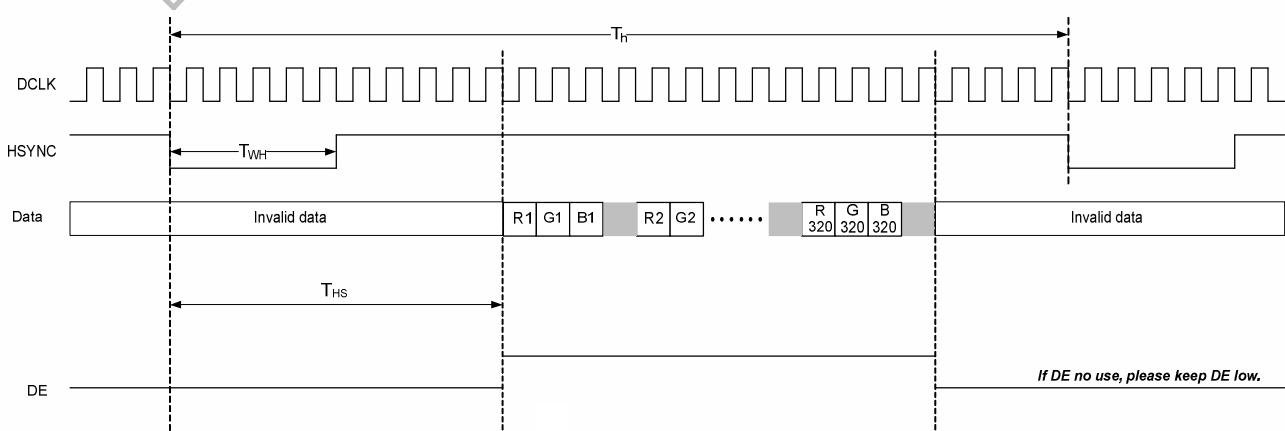
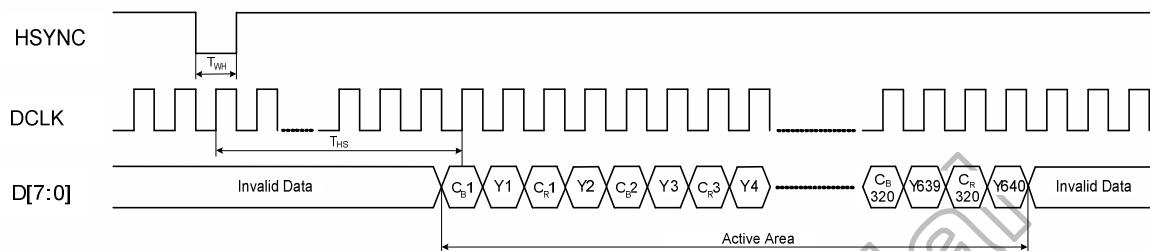


Figure 11. 8 Serial 320RGB Data Format

11.5.2 YUV mode data format

YUV mode A timing



YUV mode B timing

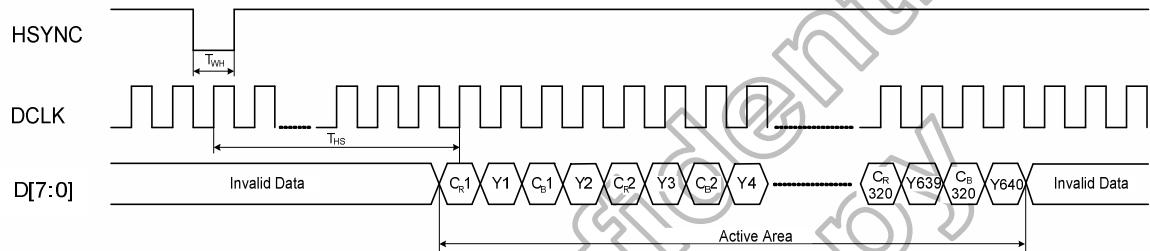


Figure 11. 9 YUV Mode Data Format.

Input format	DCLK Freq (MHz)	Display Data	Active Area (DCLK)
YUV mode	24.54	640	1280
	27	720	1440

11.5.3 CCIR656 data format

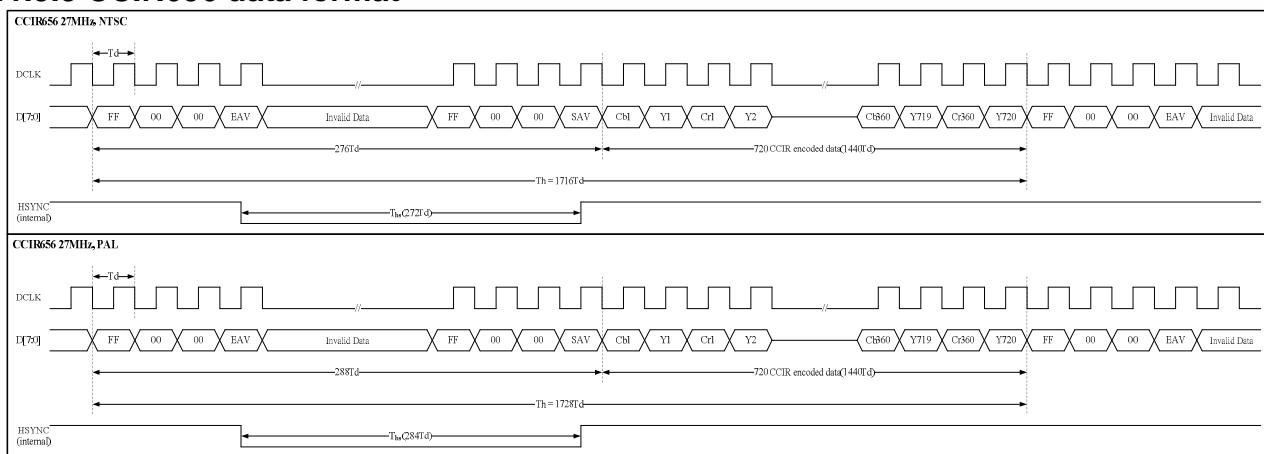


Figure 11. 10 CCIR656 Data Format

11.6 The HSYNC & VSYNC timing of the ODD/EVEN field.

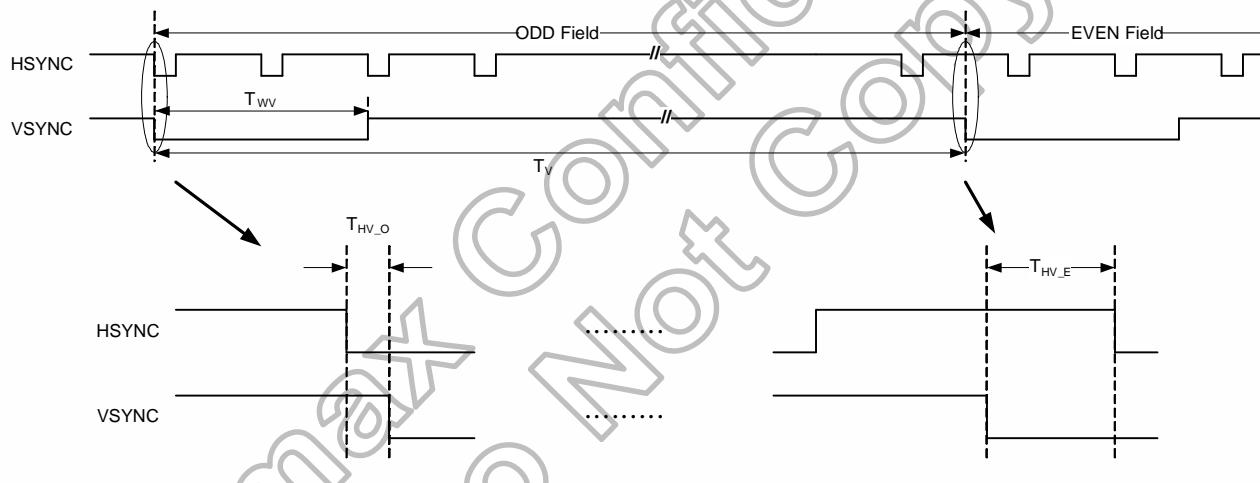
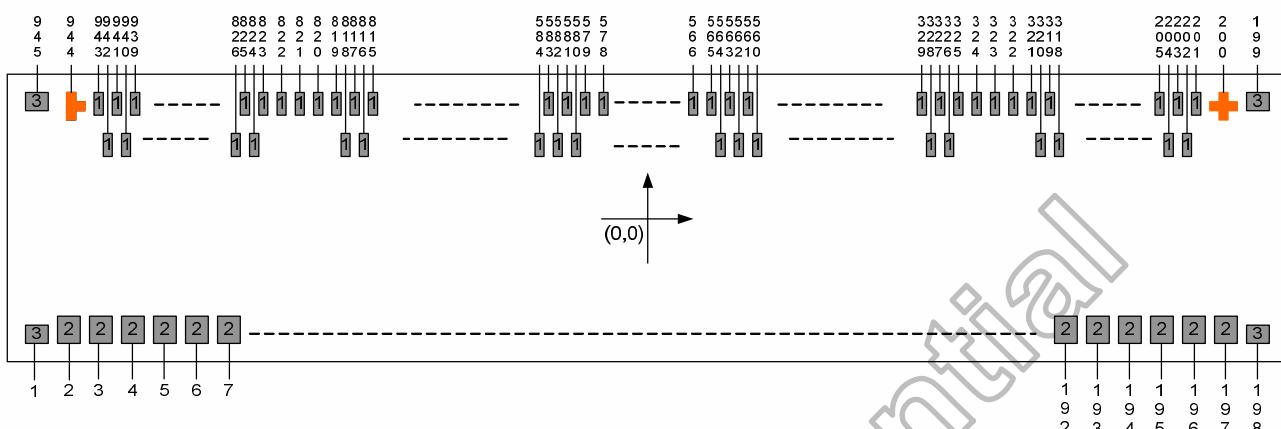


Figure 11. 11 Define the HSYNC to VSYNC timing for RGB and YUV mode

12. Pin Assignment (IC face view)

DUMMY (1)	DUMMY (1)
	
DUMMY (1)	DUMMY (1)
G2	D0 (2)
G4	D1 (2)
G6	D2 (2)
G8	D3 (2)
	D4 (2)
G236	D5 (2)
G238	D6 (2)
G240	D7 (2)
DUMMY (4)	DCLK (2)
S1	VSYNC (2)
S2	HSYNC (2)
S3	DE (2)
S4	DUMMY (1)
	QXH (2)
S237	DUMMY (1)
S238	SPCK (2)
S239	SPDA (2)
S240	SPENA (2)
DUMMY (15)	DUMMY (1)
S241	TP0 (1)
S242	TP1 (1)
S243	TP2 (1)
S244	TP3 (1)
	TP4 (1)
S477	TP5 (1)
S478	TP6 (1)
S479	TP7 (1)
S480	TP8 (2)
DUMMY (4)	TP9 (2)
G239	TP10 (1)
G237	TP11 (1)
G235	DUMMY (1)
G233	VPSW (2)
	VDDIO (5)
G7	REGVDD (2)
G5	VSS (5)
G3	DUMMY (1)
G1	RESETZ (2)
DUMMY (1)	DUMMY (1)
	VDD (5)
DUMMY (1)	FB (2)
	VSSA (5)
S477	DUMMY (1)
S478	DRV (2)
S479	DUMMY (1)
S480	PVDD (8)
DUMMY (4)	PVSS (8)
G239	DUMMY (1)
G237	C1N (6)
G235	C1P (6)
G233	DUMMY (1)
	VINT (6)
G7	DUMMY (1)
G5	C2N (6)
G3	C2P (6)
G1	DUMMY (1)
DUMMY (1)	VINT (6)
	DUMMY (1)
DUMMY (1)	DUMMY (1)
	C3N (4)
S477	C3P (4)
S478	DUMMY (1)
S479	VDDA (5)
S480	VCAC (5)
DUMMY (4)	DUMMY (1)
G239	FRP (5)
G237	DUMMY (1)
G235	VGH (5)
G233	DUMMY (1)
	C4N (4)
G7	C4P (4)
G5	DUMMY (1)
G3	VGL (5)
G1	DUMMY (1)
DUMMY (1)	VCOMDC (5)
	DUMMY (2)
DUMMY (1)	DUMMY (1)

13. Package Outline



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-P.44-
October, 2008

13.1 Pad diagram

NO.	NAME	X	Y	Bump Size
1	DUMMY	-5915	-260	50x50
2	DUMMY	-5850	-230	40x110
3	DUMMY	-5790	-230	40x110
4	VCOMDC	-5730	-230	40x110
5	VCOMDC	-5670	-230	40x110
6	VCOMDC	-5610	-230	40x110
7	VCOMDC	-5550	-230	40x110
8	VCOMDC	-5490	-230	40x110
9	DUMMY	-5430	-230	40x110
10	VGL	-5370	-230	40x110
11	VGL	-5310	-230	40x110
12	VGL	-5250	-230	40x110
13	VGL	-5190	-230	40x110
14	VGL	-5130	-230	40x110
15	DUMMY	-5070	-230	40x110
16	C4P	-5010	-230	40x110
17	C4P	-4950	-230	40x110
18	C4P	-4890	-230	40x110
19	C4P	-4830	-230	40x110
20	C4N	-4770	-230	40x110
21	C4N	-4710	-230	40x110
22	C4N	-4650	-230	40x110
23	C4N	-4590	-230	40x110
24	DUMMY	-4530	-230	40x110
25	VGH	-4470	-230	40x110
26	VGH	-4410	-230	40x110
27	VGH	-4350	-230	40x110
28	VGH	-4290	-230	40x110
29	VGH	-4230	-230	40x110
30	DUMMY	-4170	-230	40x110
31	FRP	-4110	-230	40x110
32	FRP	-4050	-230	40x110
33	FRP	-3990	-230	40x110
34	FRP	-3930	-230	40x110
35	FRP	-3870	-230	40x110
36	DUMMY	-3810	-230	40x110
37	VCAC	-3750	-230	40x110
38	VCAC	-3690	-230	40x110
39	VCAC	-3630	-230	40x110
40	VCAC	-3570	-230	40x110
41	VCAC	-3510	-230	40x110
42	VDDA	-3450	-230	40x110
43	VDDA	-3390	-230	40x110
44	VDDA	-3330	-230	40x110
45	VDDA	-3270	-230	40x110
46	VDDA	-3210	-230	40x110
47	DUMMY	-3150	-230	40x110
48	C3P	-3090	-230	40x110
49	C3P	-3030	-230	40x110
50	C3P	-2970	-230	40x110

NO.	NAME	X	Y	Bump Size
51	C3P	-2910	-230	40x110
52	C3N	-2850	-230	40x110
53	C3N	-2790	-230	40x110
54	C3N	-2730	-230	40x110
55	C3N	-2670	-230	40x110
56	DUMMY	-2610	-230	40x110
57	VINT	-2550	-230	40x110
58	VINT	-2490	-230	40x110
59	VINT	-2430	-230	40x110
60	VINT	-2370	-230	40x110
61	VINT	-2310	-230	40x110
62	VINT	-2250	-230	40x110
63	DUMMY	-2190	-230	40x110
64	C2P	-2130	-230	40x110
65	C2P	-2070	-230	40x110
66	C2P	-2010	-230	40x110
67	C2P	-1950	-230	40x110
68	C2P	-1890	-230	40x110
69	C2P	-1830	-230	40x110
70	C2N	-1770	-230	40x110
71	C2N	-1710	-230	40x110
72	C2N	-1650	-230	40x110
73	C2N	-1590	-230	40x110
74	C2N	-1530	-230	40x110
75	C2N	-1470	-230	40x110
76	DUMMY	-1410	-230	40x110
77	VCC	-1350	-230	40x110
78	VCC	-1290	-230	40x110
79	VCC	-1230	-230	40x110
80	VCC	-1170	-230	40x110
81	VCC	-1110	-230	40x110
82	DUMMY	-1050	-230	40x110
83	C1P	-990	-230	40x110
84	C1P	-930	-230	40x110
85	C1P	-870	-230	40x110
86	C1P	-810	-230	40x110
87	C1P	-750	-230	40x110
88	C1P	-690	-230	40x110
89	C1N	-630	-230	40x110
90	C1N	-570	-230	40x110
91	C1N	-510	-230	40x110
92	C1N	-450	-230	40x110
93	C1N	-390	-230	40x110
94	C1N	-330	-230	40x110
95	DUMMY	-270	-230	40x110
96	PVSS	-210	-230	40x110
97	PVSS	-150	-230	40x110
98	PVSS	-90	-230	40x110
99	PVSS	-30	-230	40x110
100	PVSS	30	-230	40x110

NO.	NAME	X	Y	Bump Size
101	PVSS	90	-230	40x110
102	PVSS	150	-230	40x110
103	PVSS	210	-230	40x110
104	PVDD	270	-230	40x110
105	PVDD	330	-230	40x110
106	PVDD	390	-230	40x110
107	PVDD	450	-230	40x110
108	PVDD	510	-230	40x110
109	PVDD	570	-230	40x110
110	PVDD	630	-230	40x110
111	PVDD	690	-230	40x110
112	DUMMY	750	-230	40x110
113	DRV	810	-230	40x110
114	DRV	870	-230	40x110
115	DUMMY	930	-230	40x110
116	VSSA	990	-230	40x110
117	VSSA	1050	-230	40x110
118	VSSA	1110	-230	40x110
119	VSSA	1170	-230	40x110
120	VSSA	1230	-230	40x110
121	VFB	1290	-230	40x110
122	VFB	1350	-230	40x110
123	VDD	1410	-230	40x110
124	VDD	1470	-230	40x110
125	VDD	1530	-230	40x110
126	VDD	1590	-230	40x110
127	VDD	1650	-230	40x110
128	DUMMY	1710	-230	40x110
129	RESETZ	1770	-230	40x110
130	RESETZ	1830	-230	40x110
131	DUMMY	1890	-230	40x110
132	VSS	1950	-230	40x110
133	VSS	2010	-230	40x110
134	VSS	2070	-230	40x110
135	VSS	2130	-230	40x110
136	VSS	2190	-230	40x110
137	REGVDD	2250	-230	40x110
138	REGVDD	2310	-230	40x110
139	VDDIO	2370	-230	40x110
140	VDDIO	2430	-230	40x110
141	VDDIO	2490	-230	40x110
142	VDDIO	2550	-230	40x110
143	VDDIO	2610	-230	40x110
144	VPSW	2670	-230	40x110
145	VPSW	2730	-230	40x110
146	DUMMY	2790	-230	40x110
147	TP11	2850	-230	40x110
148	TP10	2910	-230	40x110
149	TP9	2970	-230	40x110
150	TP9	3030	-230	40x110

NO.	NAME	X	Y	Bump Size
151	TP8	3090	-230	40x110
152	TP8	3150	-230	40x110
153	TP7	3210	-230	40x110
154	TP6	3270	-230	40x110
155	TP5	3330	-230	40x110
156	TP4	3390	-230	40x110
157	TP3	3450	-230	40x110
158	TP2	3510	-230	40x110
159	TP1	3570	-230	40x110
160	TP0	3630	-230	40x110
161	DUMMY	3690	-230	40x110
162	SPENA	3750	-230	40x110
163	SPENA	3810	-230	40x110
164	SPDA	3870	-230	40x110
165	SPDA	3930	-230	40x110
166	SPCK	3990	-230	40x110
167	SPCK	4050	-230	40x110
168	DUMMY	4110	-230	40x110
169	QXH	4170	-230	40x110
170	QXH	4230	-230	40x110
171	DUMMY	4290	-230	40x110
172	DE	4350	-230	40x110
173	DE	4410	-230	40x110
174	HSYNC	4470	-230	40x110
175	HSYNC	4530	-230	40x110
176	VSYNC	4590	-230	40x110
177	VSYNC	4650	-230	40x110
178	DCLK	4710	-230	40x110
179	DCLK	4770	-230	40x110
180	D7	4830	-230	40x110
181	D7	4890	-230	40x110
182	D6	4950	-230	40x110
183	D6	5010	-230	40x110
184	D5	5070	-230	40x110
185	D5	5130	-230	40x110
186	D4	5190	-230	40x110
187	D4	5250	-230	40x110
188	D3	5310	-230	40x110
189	D3	5370	-230	40x110
190	D2	5430	-230	40x110
191	D2	5490	-230	40x110
192	D1	5550	-230	40x110
193	D1	5610	-230	40x110
194	D0	5670	-230	40x110
195	D0	5730	-230	40x110
196	DUMMY	5790	-230	40x110
197	DUMMY	5850	-230	40x110
198	DUMMY	5915	-260	50x50
199	DUMMY	5915	260	50x50
200	MARK_R	5817.5	222.5	

NO.	NAME	X	Y	Bump Size
201	DUMMY	5730	235	15x100
202	G2	5715	105	15x100
203	G4	5700	235	15x100
204	G6	5685	105	15x100
205	G8	5670	235	15x100
206	G10	5655	105	15x100
207	G12	5640	235	15x100
208	G14	5625	105	15x100
209	G16	5610	235	15x100
210	G18	5595	105	15x100
211	G20	5580	235	15x100
212	G22	5565	105	15x100
213	G24	5550	235	15x100
214	G26	5535	105	15x100
215	G28	5520	235	15x100
216	G30	5505	105	15x100
217	G32	5490	235	15x100
218	G34	5475	105	15x100
219	G36	5460	235	15x100
220	G38	5445	105	15x100
221	G40	5430	235	15x100
222	G42	5415	105	15x100
223	G44	5400	235	15x100
224	G46	5385	105	15x100
225	G48	5370	235	15x100
226	G50	5355	105	15x100
227	G52	5340	235	15x100
228	G54	5325	105	15x100
229	G56	5310	235	15x100
230	G58	5295	105	15x100
231	G60	5280	235	15x100
232	G62	5265	105	15x100
233	G64	5250	235	15x100
234	G66	5235	105	15x100
235	G68	5220	235	15x100
236	G70	5205	105	15x100
237	G72	5190	235	15x100
238	G74	5175	105	15x100
239	G76	5160	235	15x100
240	G78	5145	105	15x100
241	G80	5130	235	15x100
242	G82	5115	105	15x100
243	G84	5100	235	15x100
244	G86	5085	105	15x100
245	G88	5070	235	15x100
246	G90	5055	105	15x100
247	G92	5040	235	15x100
248	G94	5025	105	15x100
249	G96	5010	235	15x100
250	G98	4995	105	15x100

NO.	NAME	X	Y	Bump Size
251	G100	4980	235	15x100
252	G102	4965	105	15x100
253	G104	4950	235	15x100
254	G106	4935	105	15x100
255	G108	4920	235	15x100
256	G110	4905	105	15x100
257	G112	4890	235	15x100
258	G114	4875	105	15x100
259	G116	4860	235	15x100
260	G118	4845	105	15x100
261	G120	4830	235	15x100
262	G122	4815	105	15x100
263	G124	4800	235	15x100
264	G126	4785	105	15x100
265	G128	4770	235	15x100
266	G130	4755	105	15x100
267	G132	4740	235	15x100
268	G134	4725	105	15x100
269	G136	4710	235	15x100
270	G138	4695	105	15x100
271	G140	4680	235	15x100
272	G142	4665	105	15x100
273	G144	4650	235	15x100
274	G146	4635	105	15x100
275	G148	4620	235	15x100
276	G150	4605	105	15x100
277	G152	4590	235	15x100
278	G154	4575	105	15x100
279	G156	4560	235	15x100
280	G158	4545	105	15x100
281	G160	4530	235	15x100
282	G162	4515	105	15x100
283	G164	4500	235	15x100
284	G166	4485	105	15x100
285	G168	4470	235	15x100
286	G170	4455	105	15x100
287	G172	4440	235	15x100
288	G174	4425	105	15x100
289	G176	4410	235	15x100
290	G178	4395	105	15x100
291	G180	4380	235	15x100
292	G182	4365	105	15x100
293	G184	4350	235	15x100
294	G186	4335	105	15x100
295	G188	4320	235	15x100
296	G190	4305	105	15x100
297	G192	4290	235	15x100
298	G194	4275	105	15x100
299	G196	4260	235	15x100
300	G198	4245	105	15x100

NO.	NAME	X	Y	Bump Size
301	G200	4230	235	15x100
302	G202	4215	105	15x100
303	G204	4200	235	15x100
304	G206	4185	105	15x100
305	G208	4170	235	15x100
306	G210	4155	105	15x100
307	G212	4140	235	15x100
308	G214	4125	105	15x100
309	G216	4110	235	15x100
310	G218	4095	105	15x100
311	G220	4080	235	15x100
312	G222	4065	105	15x100
313	G224	4050	235	15x100
314	G226	4035	105	15x100
315	G228	4020	235	15x100
316	G230	4005	105	15x100
317	G232	3990	235	15x100
318	G234	3975	105	15x100
319	G236	3960	235	15x100
320	G238	3945	105	15x100
321	G240	3930	235	15x100
322	DUMMY	3900	235	15x100
323	DUMMY	3870	235	15x100
324	DUMMY	3840	235	15x100
325	S1	3810	235	15x100
326	S2	3795	105	15x100
327	S3	3780	235	15x100
328	S4	3765	105	15x100
329	S5	3750	235	15x100
330	S6	3735	105	15x100
331	S7	3720	235	15x100
332	S8	3705	105	15x100
333	S9	3690	235	15x100
334	S10	3675	105	15x100
335	S11	3660	235	15x100
336	S12	3645	105	15x100
337	S13	3630	235	15x100
338	S14	3615	105	15x100
339	S15	3600	235	15x100
340	S16	3585	105	15x100
341	S17	3570	235	15x100
342	S18	3555	105	15x100
343	S19	3540	235	15x100
344	S20	3525	105	15x100
345	S21	3510	235	15x100
346	S22	3495	105	15x100
347	S23	3480	235	15x100
348	S24	3465	105	15x100
349	S25	3450	235	15x100
350	S26	3435	105	15x100

NO.	NAME	X	Y	Bump Size
351	S27	3420	235	15x100
352	S28	3405	105	15x100
353	S29	3390	235	15x100
354	S30	3375	105	15x100
355	S31	3360	235	15x100
356	S32	3345	105	15x100
357	S33	3330	235	15x100
358	S34	3315	105	15x100
359	S35	3300	235	15x100
360	S36	3285	105	15x100
361	S37	3270	235	15x100
362	S38	3255	105	15x100
363	S39	3240	235	15x100
364	S40	3225	105	15x100
365	S41	3210	235	15x100
366	S42	3195	105	15x100
367	S43	3180	235	15x100
368	S44	3165	105	15x100
369	S45	3150	235	15x100
370	S46	3135	105	15x100
371	S47	3120	235	15x100
372	S48	3105	105	15x100
373	S49	3090	235	15x100
374	S50	3075	105	15x100
375	S51	3060	235	15x100
376	S52	3045	105	15x100
377	S53	3030	235	15x100
378	S54	3015	105	15x100
379	S55	3000	235	15x100
380	S56	2985	105	15x100
381	S57	2970	235	15x100
382	S58	2955	105	15x100
383	S59	2940	235	15x100
384	S60	2925	105	15x100
385	S61	2910	235	15x100
386	S62	2895	105	15x100
387	S63	2880	235	15x100
388	S64	2865	105	15x100
389	S65	2850	235	15x100
390	S66	2835	105	15x100
391	S67	2820	235	15x100
392	S68	2805	105	15x100
393	S69	2790	235	15x100
394	S70	2775	105	15x100
395	S71	2760	235	15x100
396	S72	2745	105	15x100
397	S73	2730	235	15x100
398	S74	2715	105	15x100
399	S75	2700	235	15x100
400	S76	2685	105	15x100

NO.	NAME	X	Y	Bump Size
401	S77	2670	235	15x100
402	S78	2655	105	15x100
403	S79	2640	235	15x100
404	S80	2625	105	15x100
405	S81	2610	235	15x100
406	S82	2595	105	15x100
407	S83	2580	235	15x100
408	S84	2565	105	15x100
409	S85	2550	235	15x100
410	S86	2535	105	15x100
411	S87	2520	235	15x100
412	S88	2505	105	15x100
413	S89	2490	235	15x100
414	S90	2475	105	15x100
415	S91	2460	235	15x100
416	S92	2445	105	15x100
417	S93	2430	235	15x100
418	S94	2415	105	15x100
419	S95	2400	235	15x100
420	S96	2385	105	15x100
421	S97	2370	235	15x100
422	S98	2355	105	15x100
423	S99	2340	235	15x100
424	S100	2325	105	15x100
425	S101	2310	235	15x100
426	S102	2295	105	15x100
427	S103	2280	235	15x100
428	S104	2265	105	15x100
429	S105	2250	235	15x100
430	S106	2235	105	15x100
431	S107	2220	235	15x100
432	S108	2205	105	15x100
433	S109	2190	235	15x100
434	S110	2175	105	15x100
435	S111	2160	235	15x100
436	S112	2145	105	15x100
437	S113	2130	235	15x100
438	S114	2115	105	15x100
439	S115	2100	235	15x100
440	S116	2085	105	15x100
441	S117	2070	235	15x100
442	S118	2055	105	15x100
443	S119	2040	235	15x100
444	S120	2025	105	15x100
445	S121	2010	235	15x100
446	S122	1995	105	15x100
447	S123	1980	235	15x100
448	S124	1965	105	15x100
449	S125	1950	235	15x100
450	S126	1935	105	15x100

NO.	NAME	X	Y	Bump Size
451	S127	1920	235	15x100
452	S128	1905	105	15x100
453	S129	1890	235	15x100
454	S130	1875	105	15x100
455	S131	1860	235	15x100
456	S132	1845	105	15x100
457	S133	1830	235	15x100
458	S134	1815	105	15x100
459	S135	1800	235	15x100
460	S136	1785	105	15x100
461	S137	1770	235	15x100
462	S138	1755	105	15x100
463	S139	1740	235	15x100
464	S140	1725	105	15x100
465	S141	1710	235	15x100
466	S142	1695	105	15x100
467	S143	1680	235	15x100
468	S144	1665	105	15x100
469	S145	1650	235	15x100
470	S146	1635	105	15x100
471	S147	1620	235	15x100
472	S148	1605	105	15x100
473	S149	1590	235	15x100
474	S150	1575	105	15x100
475	S151	1560	235	15x100
476	S152	1545	105	15x100
477	S153	1530	235	15x100
478	S154	1515	105	15x100
479	S155	1500	235	15x100
480	S156	1485	105	15x100
481	S157	1470	235	15x100
482	S158	1455	105	15x100
483	S159	1440	235	15x100
484	S160	1425	105	15x100
485	S161	1410	235	15x100
486	S162	1395	105	15x100
487	S163	1380	235	15x100
488	S164	1365	105	15x100
489	S165	1350	235	15x100
490	S166	1335	105	15x100
491	S167	1320	235	15x100
492	S168	1305	105	15x100
493	S169	1290	235	15x100
494	S170	1275	105	15x100
495	S171	1260	235	15x100
496	S172	1245	105	15x100
497	S173	1230	235	15x100
498	S174	1215	105	15x100
499	S175	1200	235	15x100
500	S176	1185	105	15x100

NO.	NAME	X	Y	Bump Size
501	S177	1170	235	15x100
502	S178	1155	105	15x100
503	S179	1140	235	15x100
504	S180	1125	105	15x100
505	S181	1110	235	15x100
506	S182	1095	105	15x100
507	S183	1080	235	15x100
508	S184	1065	105	15x100
509	S185	1050	235	15x100
510	S186	1035	105	15x100
511	S187	1020	235	15x100
512	S188	1005	105	15x100
513	S189	990	235	15x100
514	S190	975	105	15x100
515	S191	960	235	15x100
516	S192	945	105	15x100
517	S193	930	235	15x100
518	S194	915	105	15x100
519	S195	900	235	15x100
520	S196	885	105	15x100
521	S197	870	235	15x100
522	S198	855	105	15x100
523	S199	840	235	15x100
524	S200	825	105	15x100
525	S201	810	235	15x100
526	S202	795	105	15x100
527	S203	780	235	15x100
528	S204	765	105	15x100
529	S205	750	235	15x100
530	S206	735	105	15x100
531	S207	720	235	15x100
532	S208	705	105	15x100
533	S209	690	235	15x100
534	S210	675	105	15x100
535	S211	660	235	15x100
536	S212	645	105	15x100
537	S213	630	235	15x100
538	S214	615	105	15x100
539	S215	600	235	15x100
540	S216	585	105	15x100
541	S217	570	235	15x100
542	S218	555	105	15x100
543	S219	540	235	15x100
544	S220	525	105	15x100
545	S221	510	235	15x100
546	S222	495	105	15x100
547	S223	480	235	15x100
548	S224	465	105	15x100
549	S225	450	235	15x100
550	S226	435	105	15x100

NO.	NAME	X	Y	Bump Size
551	S227	420	235	15x100
552	S228	405	105	15x100
553	S229	390	235	15x100
554	S230	375	105	15x100
555	S231	360	235	15x100
556	S232	345	105	15x100
557	S233	330	235	15x100
558	S234	315	105	15x100
559	S235	300	235	15x100
560	S236	285	105	15x100
561	S237	270	235	15x100
562	S238	255	105	15x100
563	S239	240	235	15x100
564	S240	225	105	15x100
565	DUMMY	210	235	15x100
566	DUMMY	180	235	15x100
567	DUMMY	150	235	15x100
568	DUMMY	120	235	15x100
569	DUMMY	90	235	15x100
570	DUMMY	60	235	15x100
571	DUMMY	30	235	15x100
572	DUMMY	0	235	15x100
573	DUMMY	-30	235	15x100
574	DUMMY	-60	235	15x100
575	DUMMY	-90	235	15x100
576	DUMMY	-120	235	15x100
577	DUMMY	-150	235	15x100
578	DUMMY	-180	235	15x100
579	DUMMY	-210	235	15x100
580	S241	-225	105	15x100
581	S242	-240	235	15x100
582	S243	-255	105	15x100
583	S244	-270	235	15x100
584	S245	-285	105	15x100
585	S246	-300	235	15x100
586	S247	-315	105	15x100
587	S248	-330	235	15x100
588	S249	-345	105	15x100
589	S250	-360	235	15x100
590	S251	-375	105	15x100
591	S252	-390	235	15x100
592	S253	-405	105	15x100
593	S254	-420	235	15x100
594	S255	-435	105	15x100
595	S256	-450	235	15x100
596	S257	-465	105	15x100
597	S258	-480	235	15x100
598	S259	-495	105	15x100
599	S260	-510	235	15x100
600	S261	-525	105	15x100

NO.	NAME	X	Y	Bump Size
601	S262	-540	235	15x100
602	S263	-555	105	15x100
603	S264	-570	235	15x100
604	S265	-585	105	15x100
605	S266	-600	235	15x100
606	S267	-615	105	15x100
607	S268	-630	235	15x100
608	S269	-645	105	15x100
609	S270	-660	235	15x100
610	S271	-675	105	15x100
611	S272	-690	235	15x100
612	S273	-705	105	15x100
613	S274	-720	235	15x100
614	S275	-735	105	15x100
615	S276	-750	235	15x100
616	S277	-765	105	15x100
617	S278	-780	235	15x100
618	S279	-795	105	15x100
619	S280	-810	235	15x100
620	S281	-825	105	15x100
621	S282	-840	235	15x100
622	S283	-855	105	15x100
623	S284	-870	235	15x100
624	S285	-885	105	15x100
625	S286	-900	235	15x100
626	S287	-915	105	15x100
627	S288	-930	235	15x100
628	S289	-945	105	15x100
629	S290	-960	235	15x100
630	S291	-975	105	15x100
631	S292	-990	235	15x100
632	S293	-1005	105	15x100
633	S294	-1020	235	15x100
634	S295	-1035	105	15x100
635	S296	-1050	235	15x100
636	S297	-1065	105	15x100
637	S298	-1080	235	15x100
638	S299	-1095	105	15x100
639	S300	-1110	235	15x100
640	S301	-1125	105	15x100
641	S302	-1140	235	15x100
642	S303	-1155	105	15x100
643	S304	-1170	235	15x100
644	S305	-1185	105	15x100
645	S306	-1200	235	15x100
646	S307	-1215	105	15x100
647	S308	-1230	235	15x100
648	S309	-1245	105	15x100
649	S310	-1260	235	15x100
650	S311	-1275	105	15x100

NO.	NAME	X	Y	Bump Size
651	S312	-1290	235	15x100
652	S313	-1305	105	15x100
653	S314	-1320	235	15x100
654	S315	-1335	105	15x100
655	S316	-1350	235	15x100
656	S317	-1365	105	15x100
657	S318	-1380	235	15x100
658	S319	-1395	105	15x100
659	S320	-1410	235	15x100
660	S321	-1425	105	15x100
661	S322	-1440	235	15x100
662	S323	-1455	105	15x100
663	S324	-1470	235	15x100
664	S325	-1485	105	15x100
665	S326	-1500	235	15x100
666	S327	-1515	105	15x100
667	S328	-1530	235	15x100
668	S329	-1545	105	15x100
669	S330	-1560	235	15x100
670	S331	-1575	105	15x100
671	S332	-1590	235	15x100
672	S333	-1605	105	15x100
673	S334	-1620	235	15x100
674	S335	-1635	105	15x100
675	S336	-1650	235	15x100
676	S337	-1665	105	15x100
677	S338	-1680	235	15x100
678	S339	-1695	105	15x100
679	S340	-1710	235	15x100
680	S341	-1725	105	15x100
681	S342	-1740	235	15x100
682	S343	-1755	105	15x100
683	S344	-1770	235	15x100
684	S345	-1785	105	15x100
685	S346	-1800	235	15x100
686	S347	-1815	105	15x100
687	S348	-1830	235	15x100
688	S349	-1845	105	15x100
689	S350	-1860	235	15x100
690	S351	-1875	105	15x100
691	S352	-1890	235	15x100
692	S353	-1905	105	15x100
693	S354	-1920	235	15x100
694	S355	-1935	105	15x100
695	S356	-1950	235	15x100
696	S357	-1965	105	15x100
697	S358	-1980	235	15x100
698	S359	-1995	105	15x100
699	S360	-2010	235	15x100
700	S361	-2025	105	15x100

NO.	NAME	X	Y	Bump Size
701	S362	-2040	235	15x100
702	S363	-2055	105	15x100
703	S364	-2070	235	15x100
704	S365	-2085	105	15x100
705	S366	-2100	235	15x100
706	S367	-2115	105	15x100
707	S368	-2130	235	15x100
708	S369	-2145	105	15x100
709	S370	-2160	235	15x100
710	S371	-2175	105	15x100
711	S372	-2190	235	15x100
712	S373	-2205	105	15x100
713	S374	-2220	235	15x100
714	S375	-2235	105	15x100
715	S376	-2250	235	15x100
716	S377	-2265	105	15x100
717	S378	-2280	235	15x100
718	S379	-2295	105	15x100
719	S380	-2310	235	15x100
720	S381	-2325	105	15x100
721	S382	-2340	235	15x100
722	S383	-2355	105	15x100
723	S384	-2370	235	15x100
724	S385	-2385	105	15x100
725	S386	-2400	235	15x100
726	S387	-2415	105	15x100
727	S388	-2430	235	15x100
728	S389	-2445	105	15x100
729	S390	-2460	235	15x100
730	S391	-2475	105	15x100
731	S392	-2490	235	15x100
732	S393	-2505	105	15x100
733	S394	-2520	235	15x100
734	S395	-2535	105	15x100
735	S396	-2550	235	15x100
736	S397	-2565	105	15x100
737	S398	-2580	235	15x100
738	S399	-2595	105	15x100
739	S400	-2610	235	15x100
740	S401	-2625	105	15x100
741	S402	-2640	235	15x100
742	S403	-2655	105	15x100
743	S404	-2670	235	15x100
744	S405	-2685	105	15x100
745	S406	-2700	235	15x100
746	S407	-2715	105	15x100
747	S408	-2730	235	15x100
748	S409	-2745	105	15x100
749	S410	-2760	235	15x100
750	S411	-2775	105	15x100

NO.	NAME	X	Y	Bump Size
751	S412	-2790	235	15x100
752	S413	-2805	105	15x100
753	S414	-2820	235	15x100
754	S415	-2835	105	15x100
755	S416	-2850	235	15x100
756	S417	-2865	105	15x100
757	S418	-2880	235	15x100
758	S419	-2895	105	15x100
759	S420	-2910	235	15x100
760	S421	-2925	105	15x100
761	S422	-2940	235	15x100
762	S423	-2955	105	15x100
763	S424	-2970	235	15x100
764	S425	-2985	105	15x100
765	S426	-3000	235	15x100
766	S427	-3015	105	15x100
767	S428	-3030	235	15x100
768	S429	-3045	105	15x100
769	S430	-3060	235	15x100
770	S431	-3075	105	15x100
771	S432	-3090	235	15x100
772	S433	-3105	105	15x100
773	S434	-3120	235	15x100
774	S435	-3135	105	15x100
775	S436	-3150	235	15x100
776	S437	-3165	105	15x100
777	S438	-3180	235	15x100
778	S439	-3195	105	15x100
779	S440	-3210	235	15x100
780	S441	-3225	105	15x100
781	S442	-3240	235	15x100
782	S443	-3255	105	15x100
783	S444	-3270	235	15x100
784	S445	-3285	105	15x100
785	S446	-3300	235	15x100
786	S447	-3315	105	15x100
787	S448	-3330	235	15x100
788	S449	-3345	105	15x100
789	S450	-3360	235	15x100
790	S451	-3375	105	15x100
791	S452	-3390	235	15x100
792	S453	-3405	105	15x100
793	S454	-3420	235	15x100
794	S455	-3435	105	15x100
795	S456	-3450	235	15x100
796	S457	-3465	105	15x100
797	S458	-3480	235	15x100
798	S459	-3495	105	15x100
799	S460	-3510	235	15x100
800	S461	-3525	105	15x100

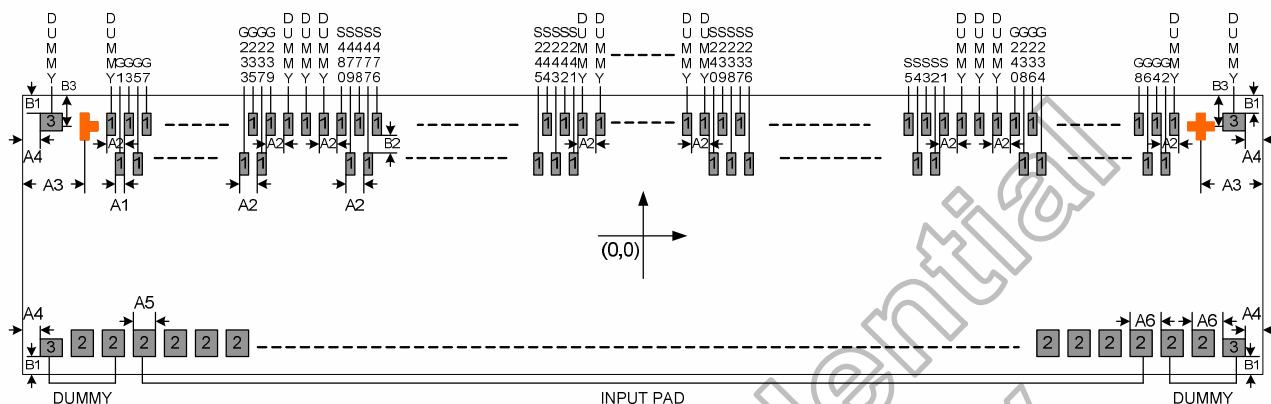
NO.	NAME	X	Y	Bump Size
801	S462	-3540	235	15x100
802	S463	-3555	105	15x100
803	S464	-3570	235	15x100
804	S465	-3585	105	15x100
805	S466	-3600	235	15x100
806	S467	-3615	105	15x100
807	S468	-3630	235	15x100
808	S469	-3645	105	15x100
809	S470	-3660	235	15x100
810	S471	-3675	105	15x100
811	S472	-3690	235	15x100
812	S473	-3705	105	15x100
813	S474	-3720	235	15x100
814	S475	-3735	105	15x100
815	S476	-3750	235	15x100
816	S477	-3765	105	15x100
817	S478	-3780	235	15x100
818	S479	-3795	105	15x100
819	S480	-3810	235	15x100
820	DUMMY	-3840	235	15x100
821	DUMMY	-3870	235	15x100
822	DUMMY	-3900	235	15x100
823	G239	-3930	235	15x100
824	G237	-3945	105	15x100
825	G235	-3960	235	15x100
826	G233	-3975	105	15x100
827	G231	-3990	235	15x100
828	G229	-4005	105	15x100
829	G227	-4020	235	15x100
830	G225	-4035	105	15x100
831	G223	-4050	235	15x100
832	G221	-4065	105	15x100
833	G219	-4080	235	15x100
834	G217	-4095	105	15x100
835	G215	-4110	235	15x100
836	G213	-4125	105	15x100
837	G211	-4140	235	15x100
838	G209	-4155	105	15x100
839	G207	-4170	235	15x100
840	G205	-4185	105	15x100
841	G203	-4200	235	15x100
842	G201	-4215	105	15x100
843	G199	-4230	235	15x100
844	G197	-4245	105	15x100
845	G195	-4260	235	15x100
846	G193	-4275	105	15x100
847	G191	-4290	235	15x100
848	G189	-4305	105	15x100
849	G187	-4320	235	15x100
850	G185	-4335	105	15x100

NO.	NAME	X	Y	Bump Size
851	G183	-4350	235	15x100
852	G181	-4365	105	15x100
853	G179	-4380	235	15x100
854	G177	-4395	105	15x100
855	G175	-4410	235	15x100
856	G173	-4425	105	15x100
857	G171	-4440	235	15x100
858	G169	-4455	105	15x100
859	G167	-4470	235	15x100
860	G165	-4485	105	15x100
861	G163	-4500	235	15x100
862	G161	-4515	105	15x100
863	G159	-4530	235	15x100
864	G157	-4545	105	15x100
865	G155	-4560	235	15x100
866	G153	-4575	105	15x100
867	G151	-4590	235	15x100
868	G149	-4605	105	15x100
869	G147	-4620	235	15x100
870	G145	-4635	105	15x100
871	G143	-4650	235	15x100
872	G141	-4665	105	15x100
873	G139	-4680	235	15x100
874	G137	-4695	105	15x100
875	G135	-4710	235	15x100
876	G133	-4725	105	15x100
877	G131	-4740	235	15x100
878	G129	-4755	105	15x100
879	G127	-4770	235	15x100
880	G125	-4785	105	15x100
881	G123	-4800	235	15x100
882	G121	-4815	105	15x100
883	G119	-4830	235	15x100
884	G117	-4845	105	15x100
885	G115	-4860	235	15x100
886	G113	-4875	105	15x100
887	G111	-4890	235	15x100
888	G109	-4905	105	15x100
889	G107	-4920	235	15x100
890	G105	-4935	105	15x100
891	G103	-4950	235	15x100
892	G101	-4965	105	15x100
893	G99	-4980	235	15x100
894	G97	-4995	105	15x100
895	G95	-5010	235	15x100
896	G93	-5025	105	15x100
897	G91	-5040	235	15x100
898	G89	-5055	105	15x100
899	G87	-5070	235	15x100
900	G85	-5085	105	15x100

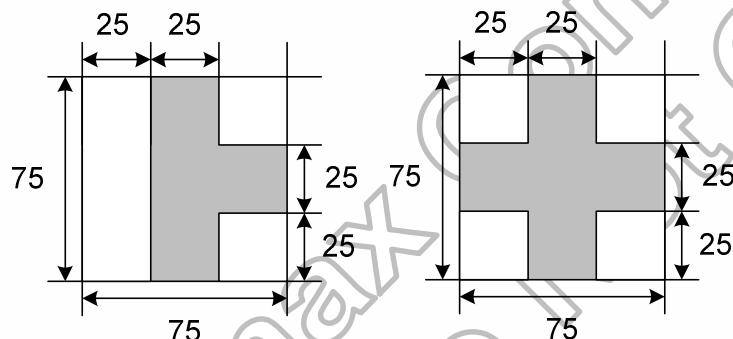
NO.	NAME	X	Y	Bump Size
901	G83	-5100	235	15x100
902	G81	-5115	105	15x100
903	G79	-5130	235	15x100
904	G77	-5145	105	15x100
905	G75	-5160	235	15x100
906	G73	-5175	105	15x100
907	G71	-5190	235	15x100
908	G69	-5205	105	15x100
909	G67	-5220	235	15x100
910	G65	-5235	105	15x100
911	G63	-5250	235	15x100
912	G61	-5265	105	15x100
913	G59	-5280	235	15x100
914	G57	-5295	105	15x100
915	G55	-5310	235	15x100
916	G53	-5325	105	15x100
917	G51	-5340	235	15x100
918	G49	-5355	105	15x100
919	G47	-5370	235	15x100
920	G45	-5385	105	15x100
921	G43	-5400	235	15x100
922	G41	-5415	105	15x100
923	G39	-5430	235	15x100
924	G37	-5445	105	15x100
925	G35	-5460	235	15x100
926	G33	-5475	105	15x100
927	G31	-5490	235	15x100
928	G29	-5505	105	15x100
929	G27	-5520	235	15x100
930	G25	-5535	105	15x100
931	G23	-5550	235	15x100
932	G21	-5565	105	15x100
933	G19	-5580	235	15x100
934	G17	-5595	105	15x100
935	G15	-5610	235	15x100
936	G13	-5625	105	15x100
937	G11	-5640	235	15x100
938	G9	-5655	105	15x100
939	G7	-5670	235	15x100
940	G5	-5685	105	15x100
941	G3	-5700	235	15x100
942	G1	-5715	105	15x100
943	DUMMY	-5730	235	15x100
944	MARK_L	-5817.5	222.5	
945	DUMMY	-5915	260	50x50

14. Bump Mask Information

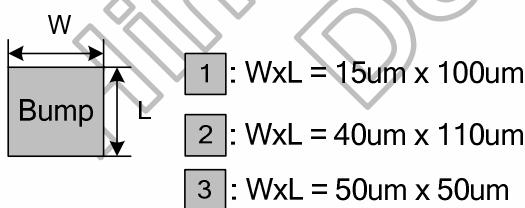
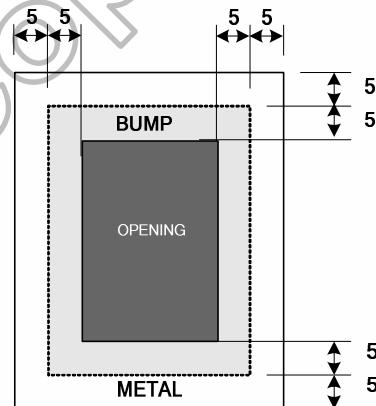
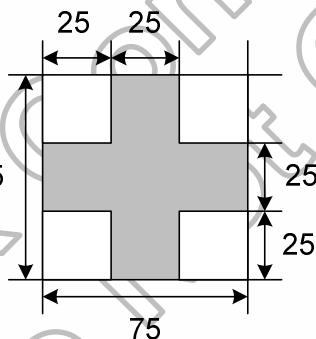
- Chip size : 12010 μm x 700 μm (Include seal ring and scribe line)
- Bump height : 15 $\mu\text{m} \pm 3 \mu\text{m}$
- Bump hardness : 60 H_V $\pm 15 \text{ H}_V$



L-alignment Mark
unit : um

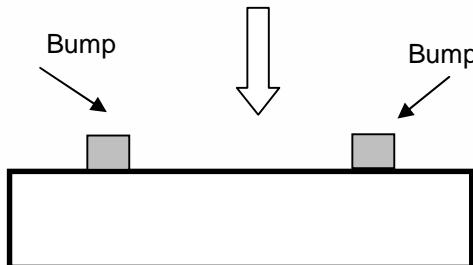


R-alignment Mark
unit : um



Symbol	Dimension (μm)
A1	15
A2	30
A3	187.5
A4	65
A5	40
A6	60
B1	65
B2	30
B3	127.5

View Angle



15. Ordering Information

PART NO.	PACKAGE TYPE
HX8224-B00B <u>PD</u> xxx-B	PD : mean COG xxx : mean chip thickness (μm) , (default 300 μm)

16. Revision History

Version	Date	Description of Changes
01	2008/10/15	New setup.

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