DATA SHEET

(DOC No. HX8249-A01-DS)

HX8249-A01

2400CH TFT LCD Source Driver with TCON

Version 02 February, 2016

Himax Technologies, Inc.
http://www.himax.com.tw

Revision History

February, 2016

Version	Date	Description of changes
01	2016/12/26	New setup.
02	0217/02/14	Page 40 1. Add Note (4)

List of Contents

1. General Description 8
2. Features 9
3. Block Diagram and DC/DC Construction 10
3.1 Block diagram 10
3.2 DC/DC voltage construction 11
3.3 Circuit for external components 12
4. Pin Description 14
4.1 Pin description 14
4.2 Group 2 input pins vs. registers 20
4.3 Display interface 21
4.3.1 LVDS interface 21
4.3.1.1 LVDS 6-bit vs. 8-bit mode 21
4.3.1.2 On-chip LVDS termination resistors 22
4.3.2 TTL interface 23
4.3.3 Data mapping from 6-bit to 8-bit 23
4.4 Recommended wiring resistance values 24
5. Resolution and Cascade Design 25
5.1.1 Typical resolutions 25
5.1.2 Adjustable resolution: Master/Slave setting and valid source channels 27
5.2 Cascade and gate driver control 29
5.2.1 Driver arrangement on panel 29
5.2.2 Cascade and gate driver control interface connections 31
5.2.3 Gate driver type definition 32
5.2.4 Gate driver control signal definition 34
5.2.5 Cascade design: Voltage outputs 37
6. Fuction Description 40
6.1 Power on/off sequence with internal PFM 40
6.1.1 Power on sequence 40
6.1.2 Power off sequence 41
6.2 Power on/off sequence with external AVDDP/AVDDN 42
6.2.1 Power on sequence 42
6.2.2 Power off sequence 43
6.3 BIST function 44
6.4 Protection modes 46
6.4.1 GAS mode 46
6.4.2 Self protection mode 46
6.5 PFM settings and VDD level detection 47
6.6 Data processing 47
6.6.1 Contrast adjustment 48
6.6.2 Brightness adjustment 48
6.6.3 Digital gamma correction 49
6.6.4 NB/NW selection 49
6.7 Interlaced input 50
6.8 TPSYNC 50
6.9 SPI Interface 51
6.9.1 SPI normal read/write mode 51
6.9.2 SPI burst write mode 52
6.10 OTP Function 53
6.10.1 First time OTP program sequence 54
6.10.2 Second time OTP program sequence 55
6.10.3 OTP marginal read 56
7. Input/Output Timing 57
7.1 Input signal timing 57
7.1.1 TTL interface 57

List of Contents

7.1.2 LVDS interface 58
7.1.3 LVDS with SSC 60
7.1.4 Reset timing 60
7.1.5 SPI timing 61
7.2 TTL Input timing 62
7.2.1 Parallel RGB at Sync mode 62
7.2.2 Parallel RGB at DE mode 65
8. Gamma Description 67
8.1 Gamma circuit 67
8.2 Equation for gamma code 69
8.3 Resistor ratio for gamma code 70
9. Register Description 72
9.1 Register table 72
9.1.1 Register page 0: Normal function 72
9.1.2 Register page 1: Analog gamma voltage reference 74
9.1.3 Register page 2: Digital gamma settings (Red) 75
9.1.4 Register page 3: Digital gamma settings (Green) 76
9.1.5 Register page 4: Digital gamma settings (Blue) 77
9.1.6 Register page 8: LVDS setting 78
9.1.7 Register page 9: OTP control 78
9.2 Page 0: Normal function setting 79
9.3 Page 8: LVDS setting 103
9.4 Page 9: OTP control 105
10. AC/DC Characteristics 106
10.1 Absolute maximum ratings 106
10.2 Electrical characteristics 106
10.2.1 TTL interface 106
10.2.2 LVDS interface 107
10.2.3 Analog circuit 108
11. Chip Information 110
11.1 Chip size 110
11.2 Bump information 110
11.3 Alignment mark 111
11.4 Chip outline 112
12. Pad Coordinates 114
13. Ordering Information 143

List of Figures

Figure 3.1: Block diagram 10
Figure 3.2: DC/DC voltage construction 11
Figure 3.3: External components for built-in PFM and charge pumps 12
Figure 3.4: External components for external AVDDP, AVDDN, VGH, VGL 13
Figure 4.1: LVDS 6-bit 21
Figure 4.2: LVDS 8-bit (VESA format) 21
Figure 4.3: LVDS 8-bit (JEIDA format) 22
Figure 4.4: LVDS termination resistor selection 22
Figure 5.1: Valid source output for typical resolutions 26
Figure 5.2: Gate driver(s) at the left side of the panel 29
Figure 5.3: Gate driver(s) is at the right side of the panel 29
Figure 5.4: Gate driver(s) at both sides of the panel, interlaced driving 30
Figure 5.5: Gate driver(s) at both sides of the panel, dual-side driving 30
Figure 5.6: Cascade and gate driver control interface 31
Figure 5.7: Gate control interface for type-1 gate drivers 32
Figure 5.8: Gate control interface for type-2 gate drivers 33
Figure 5.9: Cascade design for regulator outputs 37
Figure 5.10: Cascade design for gamma reference voltages 38
Figure 5.11: Cascade design for PFM 38
Figure 5.12: Cascade design for charge pumps 39
Figure 5.13: Cascade design for VCOM 39
Figure 6.1: Power on sequence with internal PFM 40
Figure 6.2: Power off sequence with internal PFM 41
Figure 6.3: Power on sequence with external AVDDP/AVDDN 42
Figure 6.4: Power off sequence with external AVDDP/AVDDN 43
Figure 6.5: BIST patterns 45
Figure 6.6: Self-protection detection 46
Figure 6.7: PFM power on and settings 47
Figure 6.8: Data processing 47
Figure 6.9: Contrast adjustment 48
Figure 6.10: Brightness adjustment 48
Figure 6.11: Digital gamma correction 49
Figure 6.12: INTL=0: Polarity changes by frame 50
Figure 6.13: INTL=1: Polarity changes by two frames 50
Figure 6.14: SPI format 51
Figure 6.15: SPI signals, normal write mode 51
Figure 6.16: SPI signals, normal read mode 52
Figure 6.17: SPI signals, burst write mode 52
Figure 6.18: OTP 1st program sequence (OTP table1) 54
Figure 6.19: OTP 2nd program sequence (OTP table2) 55
Figure 6.20: OTP marginal read sequence 56
Figure 7.1: TTL input timing 57
Figure 7.2: LVDS input timing 58
Figure 7.3: LVDS wake up time 58
Figure 7.4: LVDS input eye diagram 59
Figure 7.5: Reset timing 60
Figure 7.6: SPI signal timing 61
Figure 7.7: Horizontal input timing at Sync mode 62
Figure 7.8: Vertical input timing at Sync mode 62
Figure 7.9: Horizontal input timing at DE only mode 65
Figure 7.10: Vertical input timing at DE only mode 65
Figure 8.1: Positive gamma circuit 67
Figure 8.2: Negative gamma circuit 68
Figure 9.1: Gate control signals output and PFM timing 86

List of Figures

Figure 9.2: Source output timing 87
Figure 9.3: TPSYNC timing adjustment 89
Figure 9.4: PFM settings for DRVP 91
Figure 9.5: PFM settings for DRVN 92

List of Tables

Table 4.1: Group 2 input pins vs. registers 20
Table 4.2: LVDS input modes 21
Table 4.3: LVDS termination resistor selection 22
Table 4.4: TTL input modes 23
Table 4.5: Input pins for TTL 6-bit mode 23
Table 4.6: Data mapping for 6-bit mode 23
Table 5.1: Typical resolution table 25
Table 5.2: Valid source output table for typical resolutions 26
Table 5.3: Valid source output for single source driver 27
Table 5.4: Valid source output for two source drivers 28
Table 5.5: Gate driver signal definition table, single chip 34
Table 5.6: Gate driver signal definition table, master in cascade 35
Table 5.7: Gate driver signal definition table, slave in cascade 36
Table 6.1: BIST patterns 44
Table 6.2: PFM settings and VDD level detection 47
Table 6.3: Serial Interface timing parameters 51
Table 6.4: OTP program time 53
Table 7.1: TTL input timing parameters 57
Table 7.2: LVDS input timing parameters 59
Table 7.3: SSC limitation of LVDS interface 60
Table 7.4: Reset timing parameters 60
Table 7.5: SPI timing parameters 61
Table 11.1: Chip Information 110
Table 11.2: Alignment mark dimension 111
Table 11.3: Chip outline dimension 113

1. General Description

HX8249-A01 is a highly integrated source driver with built-in timing controller for color TFT LCD panels. This driver supports multiple display resolutions, with functions of 2400-channel 8-bit dot-inversion source driver **(SD)**, timing controller **(TCON)**, power circuits, and serial peripheral interface **(SPI)**. This driver is for industrial or automotive products.

2. Features

General:
- COG **(Chip on glass)** package
- Support Normally Black and Normally White panels
- 8-bit per color true resolution **(16 million colors)**
- Cascade mode for high resolution
- Closed loop for FPC connection checking
- On-chip OTP **(one-time-programming)** memory for all registers
- Able to auto-reload OTP periodically

Timing controller:
- Panel resolution:
  - 600RGBx1024, 640RGBx480, 720RGBx480/1280, 768RGBx1024/1280/1366, 800RGBx480/1280, 960RGBx160, 1024RGBx600, 1280RGBx720, 1440RGBx540, 1600RGBx720, or adjustable resolutions **(adjustable resolutions do not support Bist mode)**
- Support 24-bit **(RGB x 8bits)** or 18-bit **(RGB x 6bits)** 1 port LVDS /TTL interface
- Support HS+VS mode and DE only mode
- 3-wire SPI command setting **(support burst write)**
- Support digital gamma processing and contrast / brightness control on RGB data separately
- Provide control signals for gate driver
- Internal pattern generator for Built-in Self Testing **(BIST)**, but Bist only support for 14 typical resolution
- Support symmetrical gate routing

Source driver:
- Support maximum 2400 source output channels with 8-bit DAC **(256 levels)**
- Support “dot inversion”, “1+2 dot inversion”, “4 dot inversion” and “column inversion”
- Maximun output swing from VGMPH= 5.9V to VGMNH= -5.9V
- Right and left shift capability
- Staggered pad with 11-μm pitch

DC/DC:
- Main power supply VDD1/VDD2=2.7V~3.6V
- Source / gamma power supplies AVDDP=5.2V~6.3V and AVDDN= -6.3V~ -5.2V can be generated by Built-in PFM circuit or external power supplies
- Built-in regulators for gamma reference, TCON power supplies
- Built-in charge pumps for gate driver power supplies VGH=12V~19V and VGL= -14 ~ -7V
- Internal driving circuit for VCOM **(-3.0V ~ -0.2V)** with SPI selection

Others:
- Self-protection mode to prevent CLK, HS, VS or DE input missing
- GAS **(Gate all select)** mode to prevent image sticking when abnormal power off
- Built-in oscillator for BIST and self-protection operation

3. Block Diagram and DC/DC Construction

3.1 Block diagram

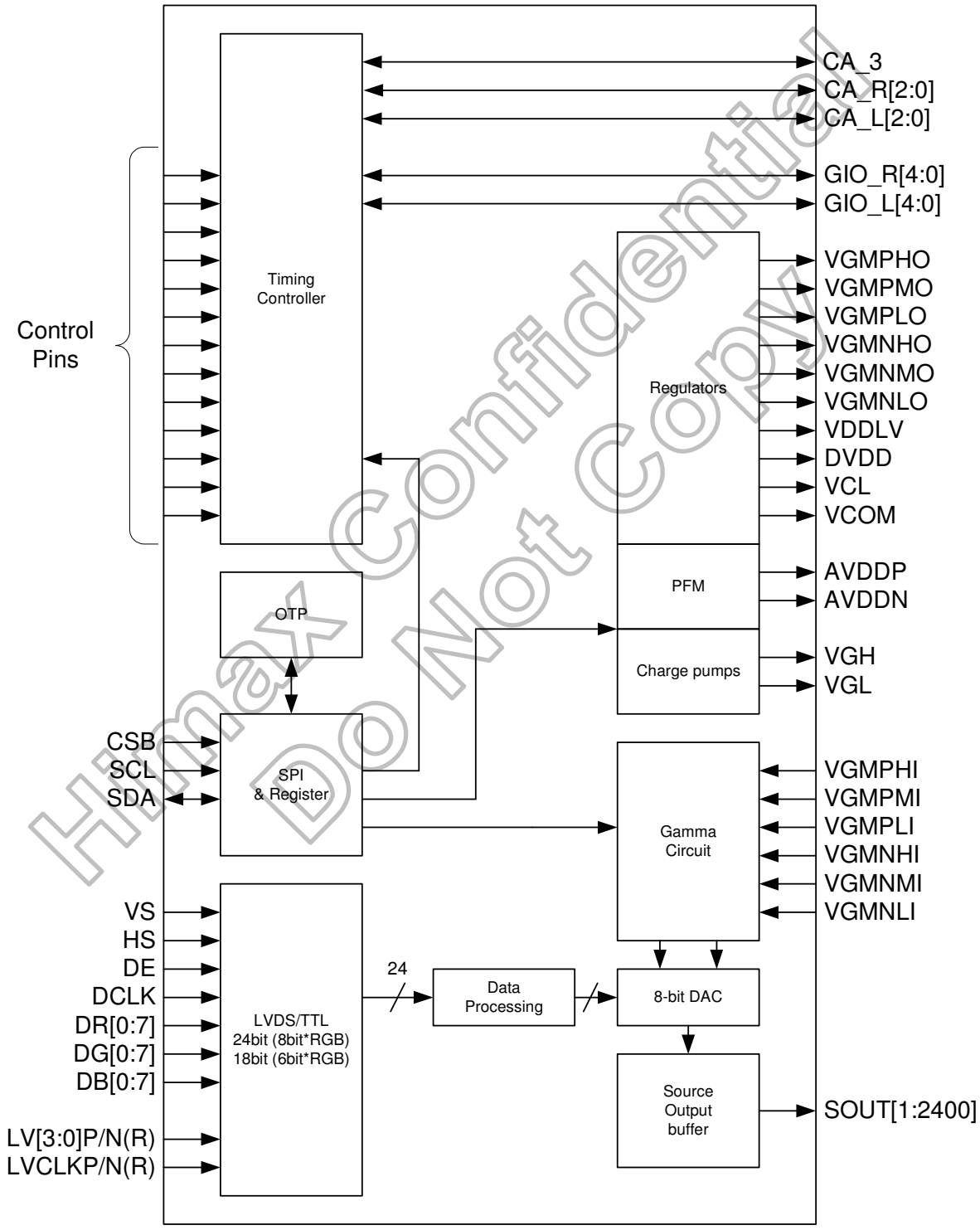


Figure 3.1: Block diagram

3.2 DC/DC voltage construction

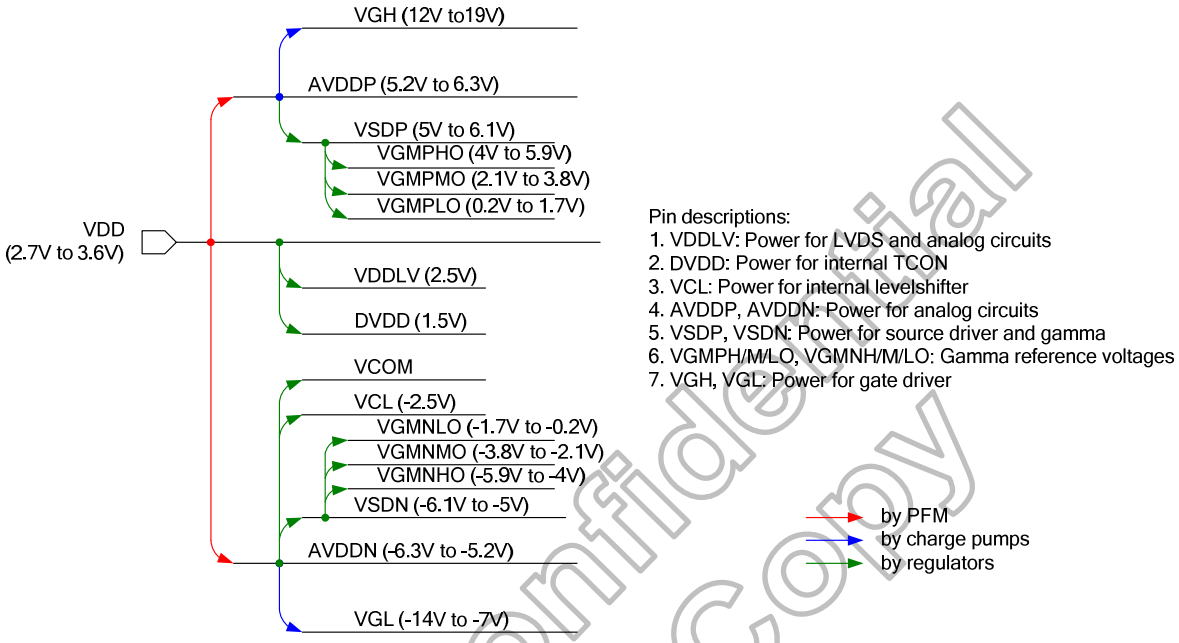


Figure 3.2: DC/DC voltage construction

3.3 Circuit for external components

A. If AVDDP, AVDDN are generated by PFM, relating components are shown in the blue area. If VGH and VGL are generated by charge pumps, relating components are shown in the red area.

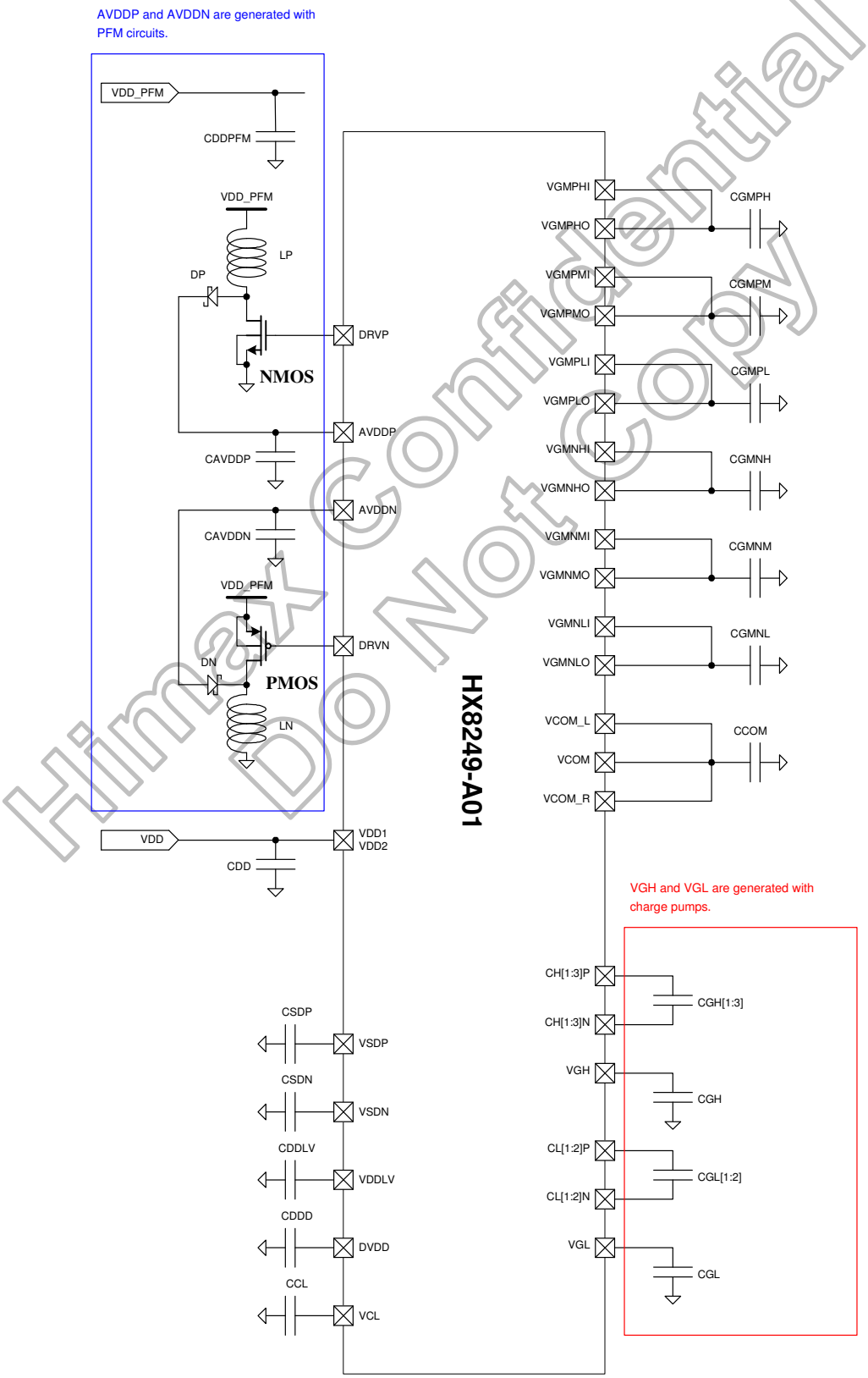


Figure 3.3: External components for built-in PFM and charge pumps

B. If AVDDP, AVDDN are given externally, change the relating circuits in the blue area. If VGH and VGL are given externally, it is not necessary to connect them to HX8249-A01.

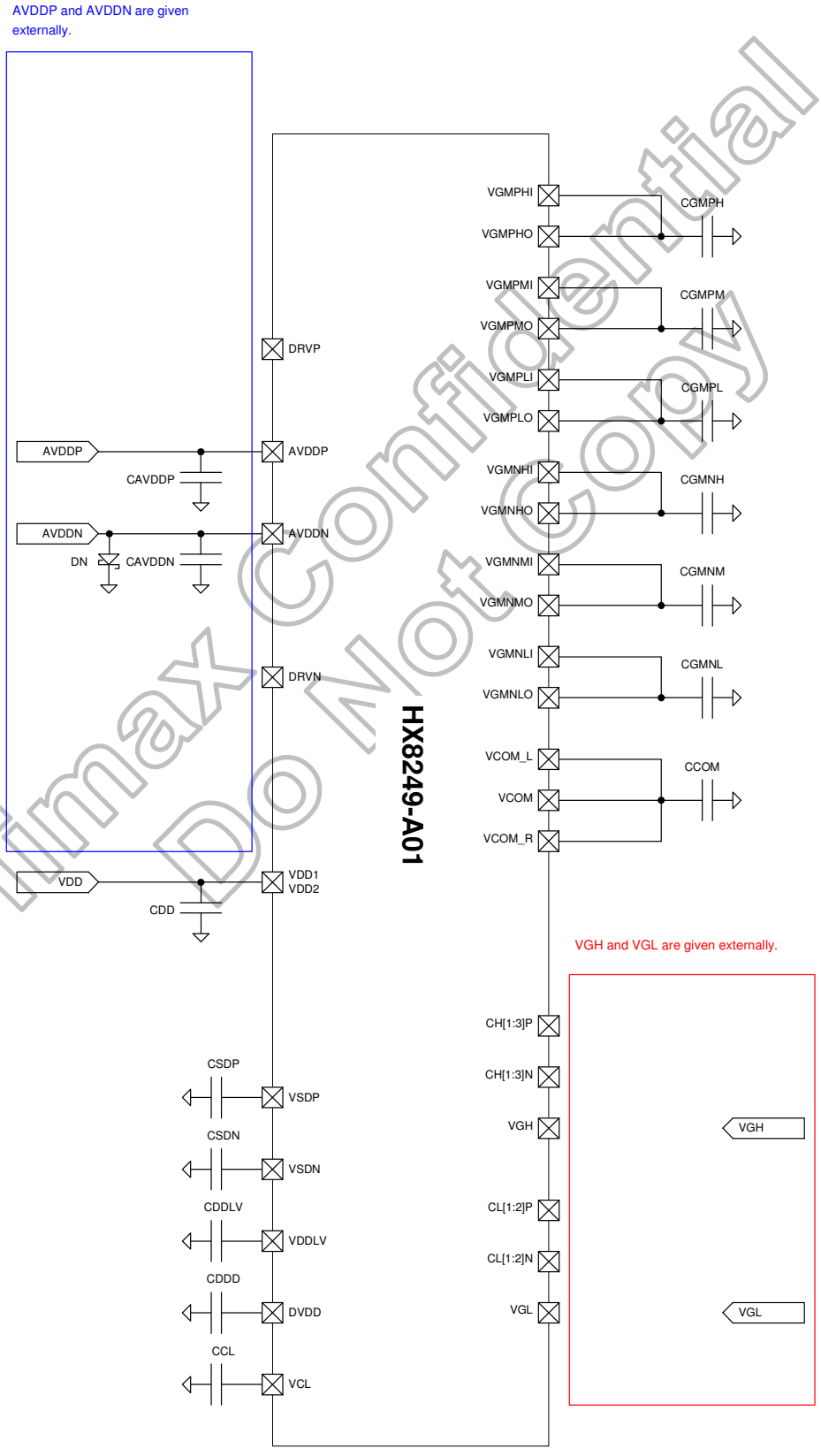


Figure 3.4: External components for external AVDDP, AVDDN, VGH, VGL

4. Pin Description

4.1 Pin description

LVDS interface pins (Refer to "Display interface")

Pad name	Type	Pulled internally	Description
LV[3:0]P LV[3:0]N LVCLKP LVCLKN	I	-	Input pins without termination resistor for LVDS mode. Keep these pins floating or connect to VSS1 if not used.
LV[3:0]PR LV[3:0]NR LVCLKPR LVCLKNR	I	-	Input pins with termination resistor for LVDS mode. Keep these pins floating or connect to VSS1 if not used

TTL interface pins (VDD1 / VSS1 level) (Refer to "Display interface")

Pad name	Type	Pulled internally	Description
DR[7:0] DG[7:0] DB[7:0] DCLK	I	L	Data/clock input pins for TTL mode. Keep these pins floating or connect to VSS1 for LVDS mode.
HS	I	H	Horizontal sync signal for TTL mode. Keep this pin floating or connect to VDD1 for LVDS mode.
VS	I	H	Vertical sync signal for TTL mode. Keep this pin floating or connect to VDD1 for LVDS mode.
DE	I	L	Data enable signal for TTL mode. Keep this pin floating or connect to VSS1 for LVDS mode.

Input control pins, group 1 (Function controlled by hardware only) (VDD1 / VSS1 level)

Pad name	Type	Pulled internally	Description
RESETB	I	H	Reset pin. The chip is in reset state when RESETB=0.
STBYB	I	H	Standby mode setting pin. The chip is in standby mode when STBYB=0.
FCS	I	H	Function control by Hardware/Software selection. **FCS** / **Function control** / **Note** 1 / Hardware pin **(Group 2)** / Default 0 / Software register / -
SID	I	-	Source driver chip ID **(position in chain)** selection. Please refer to "Master / slave setting and valid source channels". **SID** / **Function control** / **Note** 0 / Master / - 1 / Slave / -
SIDEN	I	H	Enable chip ID identification in SPI. Please refer to "SPI Interface". **SIDEN** / **Function** / **Note** 1 / Chip SPI R/W by CHIP ID setting / Default 0 / SPI write to all chip, and read from Master only / -
GSQ	I	L	Gate driver type selection. Please refer to "Gate driver type definition". **GSQ** / **Function** / **Note** 1 / Type 2 / - 0 / Type 1 / Default

Pad name	Type	Pulled internally	Description
ATREN	I	H	Auto reload OTP in operation mode every 64 frames. When programming OTP or changing register values by SPI, ATREN should be kept 0. **ATREN** / **Function** / **Note** 1 / Enabled / Default 0 / Disabled / -
RTERMEN	I	L	LVDS input pair selection. Please refer to ”On-chip LVDS termination resistors”. **RTERMEN** / **Function** / **Note** 1 / Select input pins with termination resistor **(LVCLKP/NR, LV[3:0]P/NR)** / - 0 / Select input pins without termination resistor **(LVCLKP/N, LV[3:0]P/N)** / Default

Input control pins, group 2 (Function controlled by hardware or software setting) (VDD1 / VSS1 level)

Pad name	Type	Pulled internally	Description
TR	I	H	Interface selection. Effective when FCS=1. **TR** / **Function** / **Note** 1 / TTL / Default 0 / LVDS / -
DINT	I	H	Input data format selection. Effective when FCS=1. **DINT** / **Function** / **Note** 1 / 8-bit / Default 0 / 6-bit / -
MODE	I	H	Input timing mode selection. Effective when FCS=1. **MODE** / **Function** / **Note** 0 / DE only / - 1 / HS+VS / Default
NB	I	H	Panel type NB/NW selection. Effective when FCS=1. **NB** / **Function** / **Note** 1 / Normally black / Default 0 / Normally white / -
RL	I	H	Horizontal shift direction **(source output)** selection. Effective when FCS=1. **RL** / **Source output sequence and data order** / **Note** 1 / SOUT1→SOUT2→ …→ SOUT2400 / Default 0 / SOUT2400→SOUT2399→ …→ SOUT1 /
TB	I	H	Vertical shift direction **(gate output)** selection. Effective when FCS=1. **TB** / **Function** / **Note** 1 / Top→bottom / Default 0 / Bottom→top / -
INV[1:0]	I	H	Inversion type selection. Effective when FCS=1. **INV[1:0]** / **Function** / **Note** 00 / 1+2 dot inversion / - 01 / Column inversion / - 10 / 4 dot inversion / - 11 / Dot inversion / Default
RS[3:0]	I	-	Panel resolution selection. Effective when FCS=1. Please refer to “Typical resolutions”.

<table>
<tr><td>GPOS[1:0]</td><td>I</td><td>L</td><td>Gate driver location select. Effective when FCS=1. Please refer to “Gate driver type definition”.
<table>
<tr><th>GPOS[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>00</td><td>Left side</td><td>Default</td></tr>
<tr><td>01</td><td>Right side</td><td>-</td></tr>
<tr><td>10</td><td>Interlaced driving at dual side</td><td>-</td></tr>
<tr><td>11</td><td>Progressive driving the same line at dual side</td><td>-</td></tr>
</table></td></tr>
<tr><td>BISTEN</td><td>I</td><td>L</td><td>Enable bult-in self test (BIST) function. Effective when FCS=1.
<table>
<tr><th>BISTEN</th><th>Function</th><th>Note</th></tr>
<tr><td>1</td><td>BIST mode</td><td>-</td></tr>
<tr><td>0</td><td>Normal mode</td><td>Default</td></tr>
</table></td></tr>
<tr><td>INTL</td><td>I</td><td>L</td><td>For interlaced signal input. Effective when FCS=1.
<table>
<tr><th>INTL</th><th>Function</th><th>Note</th></tr>
<tr><td>1</td><td>Interlaced input</td><td>-</td></tr>
<tr><td>0</td><td>Normal input</td><td>Default</td></tr>
</table></td></tr>
</table>

Serial interface pins (VDD1 / VSS1 level)

Pad name	Type	Pulled internally	Description
CSB	I	H	Serial Interface chip enable signal. CSB=0: Selected **(accessible)** CSB=1: Not selected **(inaccessible)**
SCL	I	L	Serial Interface clock input.
SDA	I/O	L	Serial Interface address and data input/output.

Cascade and gate driver control pins (VDD1 / VSS1 level)
(Leave these pins open if not used. Refer to “cascade and gate driver control”.)

Pad name	Type	Pulled internally	Description
CA_L0 **(UD)** CA_L2 **(UD)**	/IO	L	Cascade signal input pins, also used as “UD” output pins for gate driver control on the master chip.
GIO_L[4:0]	I/O	L	Gate driver control pins at the left side.
CA_L1	I	L	Cascade signal input pin.
CA3	I/O	L	Cascade signal pin.
CA_R0 **(UD)** CA_R2 **(UD)**	I/O	L	Cascade signal output pins, also used as “UD” output pins for gate driver control on the last slave chip.
GIO_R2	O	-	Gate driver control output pin.
CA_R1	O	-	Cascade signal output pin.
GIO_R[1:0] GIO_R[4:3]	I/O	L	Gate driver control pins at the right side.

Source out pins

Pad name	Type	Description
SOUT[1:2400]	O	Source driver outputs.

Power supply pins: Connected to power supply

Pad name	Type	Description
VDD1	P	Power input for main and I/O power.
VSS1	P	Ground pin for logic circuit and I/O.
VDD1P	P	Power input for PFM output DRVP and DRVN. Shorted to VDD1, but must be conntected when PFM and/or charge pumps are used, else just floating.
VSS1P	P	Ground pin for PFM output **(DRVP and DRVN)** and charge pumps. Shorted to VSS1, but must be conntected when PFM and/or charge pumps are used, else just floating.
VDD2	P	Power pin for internal references.

VSS2	P	Ground pin for internal reference circuit.
VSSA	P	Analog circuit ground.
AVDDP	P	Power input for power circuits.
AVDDN	P	Power input for power circuits.
VDDOTP	P	Power input for OTP programming. Power input for OTP programming. Keep this pin floating when not programming OTP.

Regulator output and voltage reference input pins: Connected to capacitors

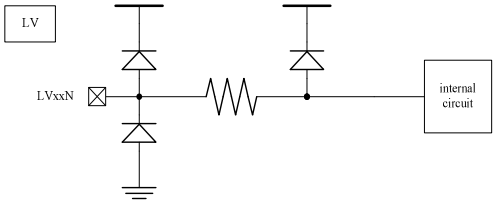
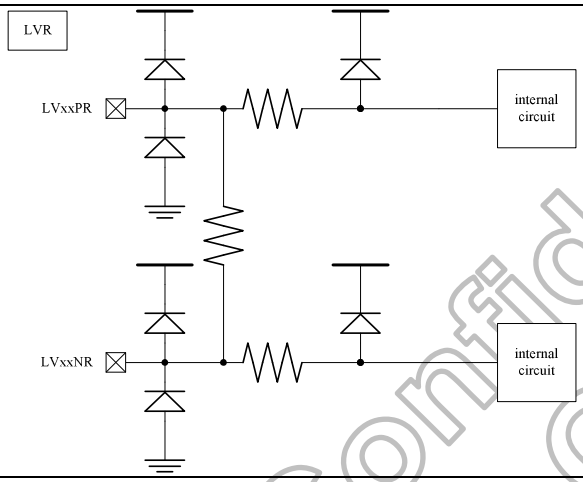
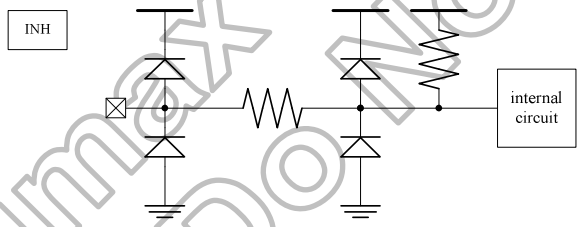
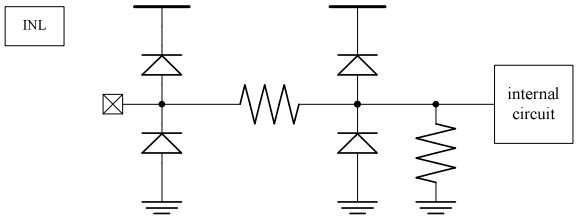
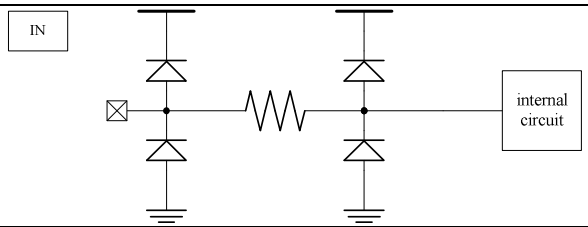
Pad name	Type	Description
VGMPHO	O	Internal regulator output for positive gamma reference voltage. **(VSDP-0.2V≧VGMPHO)**
VGMPMO	O	Internal regulator output for positive gamma reference voltage.
VGMPLO	O	Internal regulator output for positive gamma reference voltage.
VGMNHO	O	Internal regulator output for negative gamma reference voltage. **(|VSDN|-0.2V≧ |VGMNHO|)**
VGMNMO	O	Internal regulator output for negative gamma reference voltage.
VGMNLO	O	Internal regulator output for negative gamma reference voltage.
VGMPHI	I	Positive gamma reference voltage.
VGMPMI	I	Positive gamma reference voltage.
VGMPLI	I	Positive gamma reference voltage.
VGMNHI	I	Negative gamma reference voltage.
VGMNMI	I	Negative gamma reference voltage.
VGMNLI	I	Negative gamma reference voltage.
DVDD	I/O	Internal regulator output for logic power supply.
VSDP	I/O	Internal regulator output for source driver. **(AVDDP-0.2V≧VSDP)**
VSDN	I/O	Internal regulator output for source driver. **(|AVDDN|-0.2V≧|VSDN|)**
VDDLV	I/O	Internal regulator output for reference circuits.
VCOM	O	Internal driving circuit for VCOM.
VCL	I/O	Internal regulator output for negative level shifter.

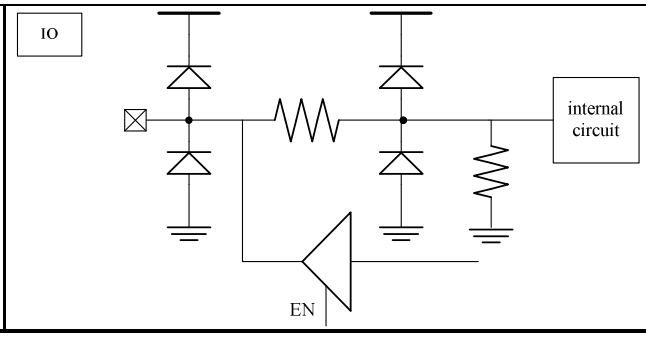
Charge pump and PFM pins: Connected to external components

Pad name	Type	Description
VGH	O	Charge pump output for gate driver.
VGL	O	Charge pump output for gate driver.
CH[1:3]P, CH[1:3]N	C	Capacitor connection pin for VGH charge pump.
CL[1:2]P, CL[1:2]N	C	Capacitor connection pin for VGL charge pump.
DRVP	O	PFM output for AVDDP.
DRVN	O	PFM output for AVDDN.

Test pins, through pins and dummy pins

Pad name	Type	Description
TEST[7:0]	O	Logic test pins, leave these pins open.
TPSYNC	O	Output signal for touch panel. **(VDD1/VSS1 level)**
TO[3:0]	O	Internal reference voltage test pin, leave these pins open.
THROUGH_[2:1]	-	These sets of pins can be used for resistance measurement.
VCOM_R VCOM_L	-	Thses sets of pins can be used for VCOM connection to the panel.
DUMMY	-	These pins are open and separated to each other.

Input pin type	Pin structure	Pins
PIN_LV		LV[3:0]P LV[3:0]N LVCLKP LVCLKN
PIN_LVR		LV[3:0]PR LV[3:0]NR LVCLKPR LVCLKNR
PIN_INH		VS HS RESETB STBYB FCS SIDEN ATREN TR DINT MODE NB RL TB INV[1:0] CSB
PIN_INL		DCLK DR[7:0] DG[7:0] DB[7:0] DE GSQ RTERMEN GPOS[1:0] BISTEN INTL SCL CA_L1
PIN_IN		SID RS[3:0]

PIN_IO		SDA CA_L0 CA_L2 GIO_L[4:0] CA3 CA_R0 CA_R2 GIO_R[1:0] GIO_R[4:3]

Note: (1) Pin structure (VDD1/VSS1 level)

(2) Besides RESETB and STBYB pins, for input control pins listed in group 1 and 2 with PIN_INH or PIN_INL structure, it's recommended to use external pull L/H resistor with a value less than 1K ohms for optimal pin L/H setting respectively.

4.2 Group 2 input pins vs. registers

The following settings can be chosen to be controlled by hardware input pin **(group 2)** or by values in register page 0. When FCS is set to 0, the chip is controlled by registers. Otherwise, the chip is controlled by hardware pin.

Pin name	Register (Page 0)
INTL	R02h[7]
TR	R02h[6]
DINT	R02h[5]
MODE	R02h[4]
NB	R02h[0]
RL	R03h[7]
TB	R03h[6]
INV[1:0]	R03h[5:4]
RS[3:0]	R03h[3:0]
GPOS[1:0]	R04h[7:6]
BISTEN	R05h[4]

Table 4.1: Group 2 input pins vs. registers

4.3 Display interface

HX8249-A01 supports LVDS and TTL interface.

4.3.1 LVDS interface

4.3.1.1 LVDS 6-bit vs. 8-bit mode

LVDS interface is selected by setting TR to 0. Three modes are available.

TR	DINT	LVDS_FMT	Interface
0	0	-	LVDS 6-bit
	1	0	LVDS 8-bit **(VESA)**
		1	LVDS 8-bit **(JEDIA)**

Table 4.2: LVDS input modes

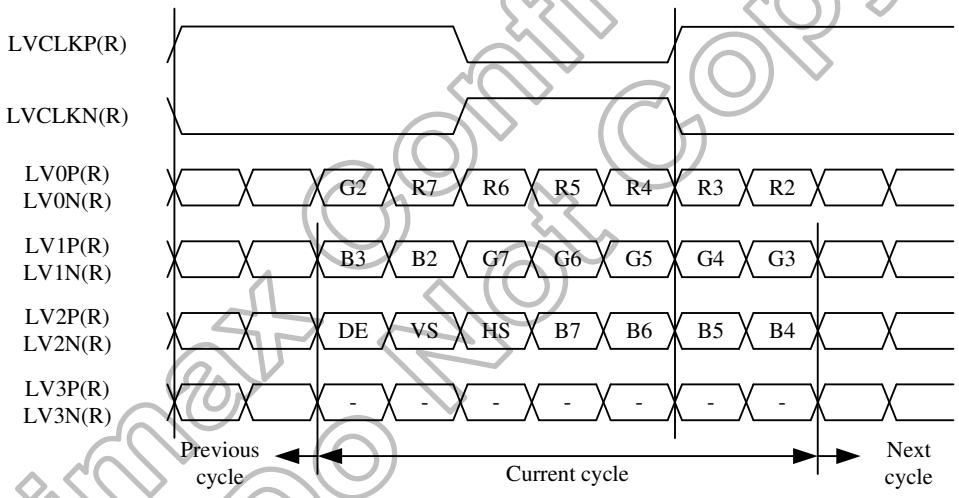


Figure 4.1: LVDS 6-bit

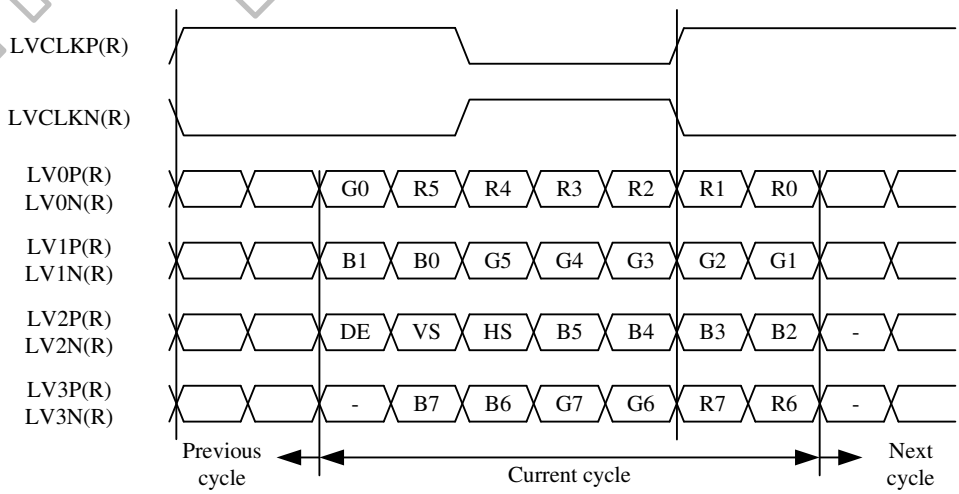


Figure 4.2: LVDS 8-bit (VESA format)

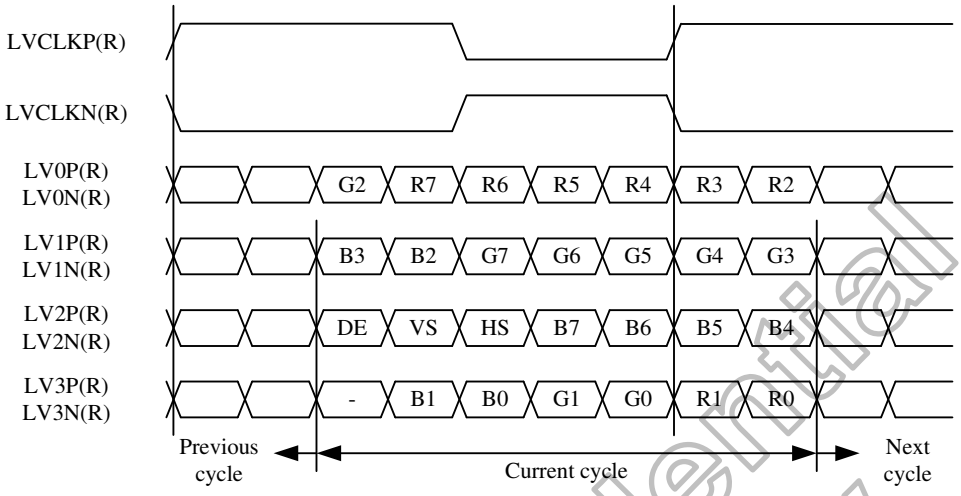


Figure 4.3: LVDS 8-bit (JEIDA format)

4.3.1.2 On-chip LVDS termination resistors

Two sets of LVDS input pair are provided. There are termination resistors on LV[3:0]P/NR, LVCLKP/NR input pins, and no termination resistors on LV[3:0]P/N, LVCLKP/N input pins. These input pairs are selected by input pin RTERMEN.

TR	RTERMEN	Input pins
0	0	LV[3:0]P/N, LVCLKP/N
	1	LV[3:0]P/NR, LVCLKP/NR

Table 4.3: LVDS termination resistor selection

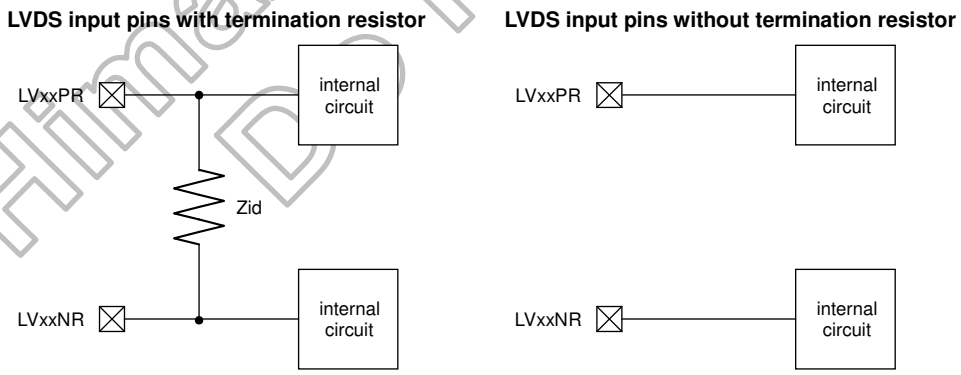


Figure 4.4: LVDS termination resistor selection

4.3.2 TTL interface

TTL interface is selected by setting TR to 1. Two modes are available.

TR	DINT	LVDS_FMT	Interface
1	0	-	TTL, 6-bit
	1	-	TTL, 8-bit

Table 4.4: TTL input modes

In 6-bit mode, input pins DR[1:0], DG[1:0] and DB[1:0] are not used. It is suggested to connect these pins to VSS1.

Pin name	Input Data	Pin name	Input Data	Pin name	Input Data
DR0	-	DG0	-	DB0	-
DR1	-	DG1	-	DB1	-
DR2	DR0	DG2	DG0	DB2	DB0
DR3	DR1	DG3	DG1	DB3	DB1
DR4	DR2	DG4	DG2	DB4	DB2
DR5	DR3	DG5	DG3	DB5	DB3
DR6	DR4	DG6	DG4	DB6	DB4
DR7	DR5	DG7	DG5	DB7	DB5

Table 4.5: Input pins for TTL 6-bit mode

4.3.3 Data mapping from 6-bit to 8-bit

Data mapping for 6-bit mode is the same for both LVDS and TTL mode. 6-bit input data DI[5:0] will be mapped to 8-bit data DO[7:0], where DO[7:2]=DI[5:0], and DO[1:0]=DI[5:4].

Mapped 8-bit data	Input Data	Mapped 8-bit data	Input Data	Mapped 8-bit data	Input Data
DR0	DR4	DG0	DG4	DB0	DB4
DR1	DR5	DG1	DG5	DB1	DB5
DR2	DR0	DG2	DG0	DB2	DB0
DR3	DR1	DG3	DG1	DB3	DB1
DR4	DR2	DG4	DG2	DB4	DB2
DR5	DR3	DG5	DG3	DB5	DB3
DR6	DR4	DG6	DG4	DB6	DB4
DR7	DR5	DG7	DG5	DB7	DB5

Table 4.6: Data mapping for 6-bit mode

4.4 Recommended wiring resistance values

Recommended wiring resistance values are listed below as reference. Wiring resistance values affect the current capacity of the power supply, thus they are relating to panel loading.

Pad type	Pad	Resistance
Input interface pins	DCLK HS VS DE DR[7:0] DG[7:0] DB[7:0]	< 50Ω
	LVCLKP/N LVD3P/N LVD2P/N LVD1P/N LVD0P/N LVCLKP/NR LVD3P/NR LVD2P/NR LVD1P/NR LVD0P/NR	< 20Ω
Input control pins	RESETB STBYB FCS SID SIDEN GSQ ATREN RTERMEN TR DINT MODE NB RL TB INV[1:0] RS[3:0] GPOS[1:0] BISTEN INTL	< 100Ω
serial interface pins	CSB SCL	< 100Ω
	SDA	< 20Ω
Cascade and gate driver control pins	CA_L[2:0] CA_R[2:0] CA3 GIO_L[4:0] GIO_R[4:0]	< 100Ω

Pad type	Pad	Resistance
Power supply pins	VDD1 VDD1P VSS1 VSS1P VDD2 VSS2 VDDOTP	< 10Ω
	VSSA AVDDP AVDDN	< 5.5Ω
Regulator output and reference input pins	VGMPHI/VGMPHO VGMPMI/VGMPMO VGMPLI/VGMPLO VGMNHI/VGMNHO VGMNMI/VGMNMO VGMNLI/VGMNLO	< 20Ω
	DVDD VDDLV VCOM	< 10Ω
	VSDP VSDN	< 5.5Ω
	VCL	< 15Ω
Charge pump and PFM pins	VGH VGL DRVP DRVN CH[1:3]P CH[1:3]N CL[1:2]P CL[1:2]N	< 20Ω
Through pins	VCOM_R VCOM_L	< 10Ω
	THROUGH_[2:1]	**Note**(1)
Others	TPSYNC	< 20Ω

Note: (1) Resistance of THROUGH_[2:1] does not cause any effect on display or driver. User can choose proper values for bonding resistance measurement.

5. Resolution and Cascade Design

5.1.1 Typical resolutions

14 typical resolutions are selected with RS[3:0]. The source drivers can be cascaded to support resolution up to 1600xRGBx720 with two chips.

Settings	Resolution		Source driver	
RS[3:0]	RGB (Hactive)	Line (Vactive)	Chips cascaded (N)	Channels per chip (X)
0000	600	1024	1	1800
0001	720	480	1	2160
0010	720	1280	1	2160
0011	768	1024	1	2304
0100	768	1280	1	2304
0101	768	1366	1	2304
0110	800	480	1	2400
0111	800	1280	1	2400
1000	960	160	2	1440
1001	1024	600	2	1536
1010	1280	720	2	1920
1011	1440	540	2	2160
1100	1600	720	2	2400
1101	640	480	1	1920
1110	720	1280	1	2160
1111	720	1280	1	2160

Table 5.1: Typical resolution table

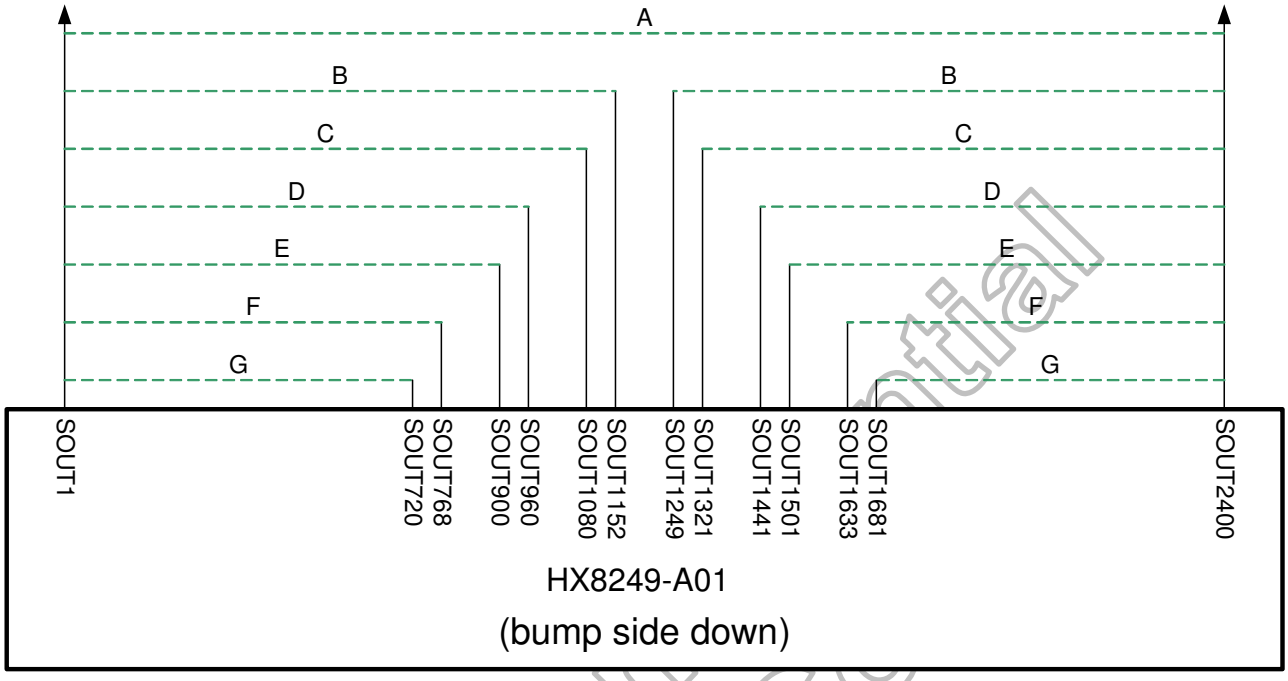


Figure 5.1: Valid source output for typical resolutions

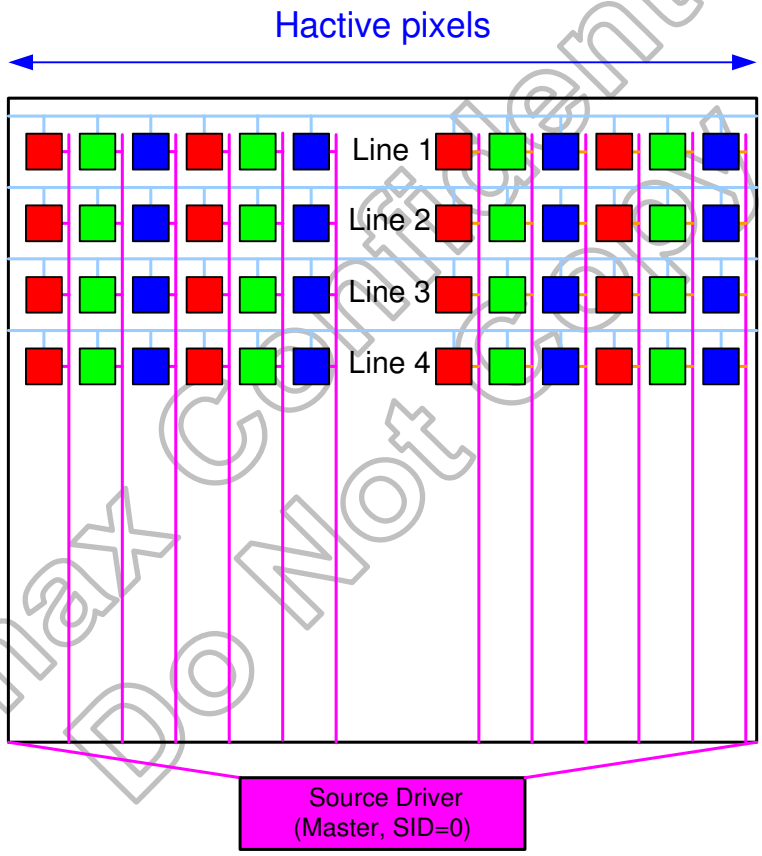
Channels		Valid source output
A	2400	SOUT1~SOUT2400
B	2304	SOUT1~SOUT1152, SOUT1249~SOUT2400
C	2160	SOUT1~SOUT1080, SOUT1321~SOUT2400
D	1920	SOUT1~SOUT960, SOUT1441~SOUT2400
E	1800	SOUT1~SOUT900, SOUT1501~SOUT2400
F	1536	SOUT1~SOUT768, SOUT1633~SOUT2400
G	1440	SOUT1~SOUT720, SOUT1681~SOUT2400

Table 5.2: Valid source output table for typical resolutions

5.1.2 Adjustable resolution: Master/Slave setting and valid source channels

HX8249-A01 support resolutions to be Hactive **(RGB)** x Vactive, where Hactive is an even number ranging from 240 to 1600, and Vactive is an even number ranging from 100 to 2000. Hactive and Vactive can be selected with RS[3:0], or set with register HSETNUM[10:0] and GATENUM[9:0].

A. Hactive=240~800: single source driver **(N=1)**. It should be set to be master **(SID=0)**.

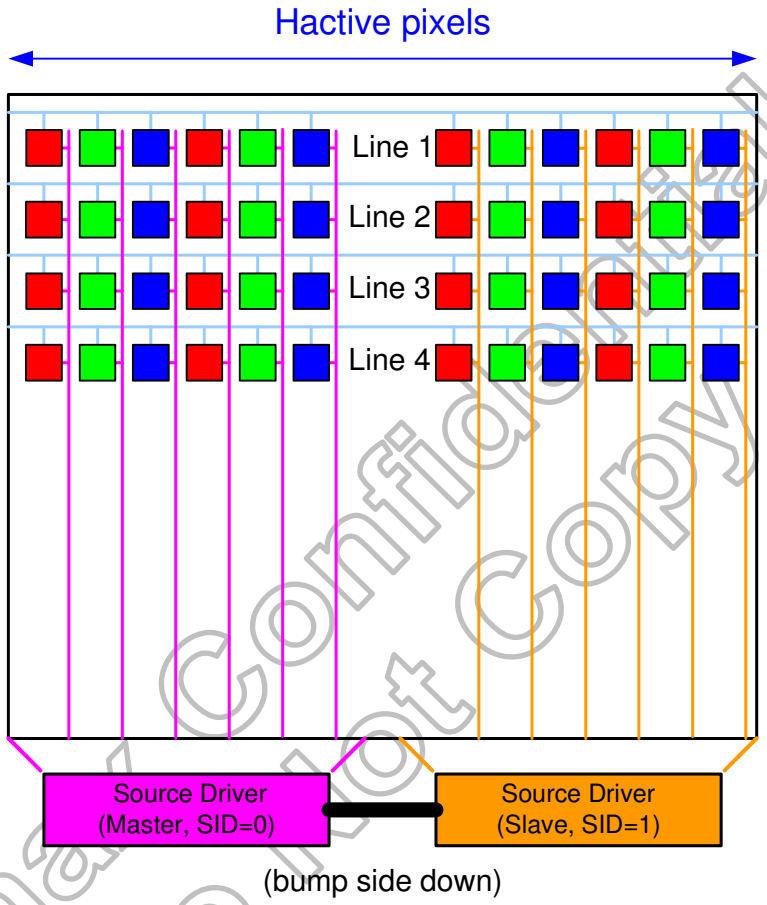


(bump side down)

Hactive=240~800	Master output channel	
If Hactive=4K	S1~S **(6K)**	S **(2401-6K)**~S2400
If Hactive=4K+2	S1~S **(6K+3)**	S **(2398-6K)**~S2400

Table 5.3: Valid source output for single source driver

B. Hactive=802~1600: Two source drivers in cascade mode **(N=2)**. The left chip should be set to be master **(SID=0)**, and the right chip is set to be slave **(SID=1)**.



Hactive=802~1600	Master output channel		Slave output channel	
If Hactive=8K	S1~S **(6K)**	S **(2401-6K)**~S2400	S1~S **(6K)**	S **(2401-6K)**~S2400
If Hactive=8K+2	S1~S **(6K)**	S **(2401-6K)**~S2400	S1~S **(6K+3)**	S **(2398-6K)**~S2400
If Hactive=8K+4	S1~S **(6K+6)**	S **(2395-6K)**~S2400	S1~S **(6K)**	S **(2401-6K)**~S2400
If Hactive=8K+6	S1~S **(6K+6)**	S **(2395-6K)**~S2400	S1~S **(6K+3)**	S **(2398-6K)**~S2400

Table 5.4: Valid source output for two source drivers

5.2 Cascade and gate driver control

5.2.1 Driver arrangement on panel

The below pictures show how source drivers and gate drivers are located on panel. For example, if panel resolution is 1600xRGBx720 and it needs two chips **(N=2)**. "X" represents output channels per chip. For this case, X is equal to 2400 channels.

A. Gate driver(s) at the left side of the panel.

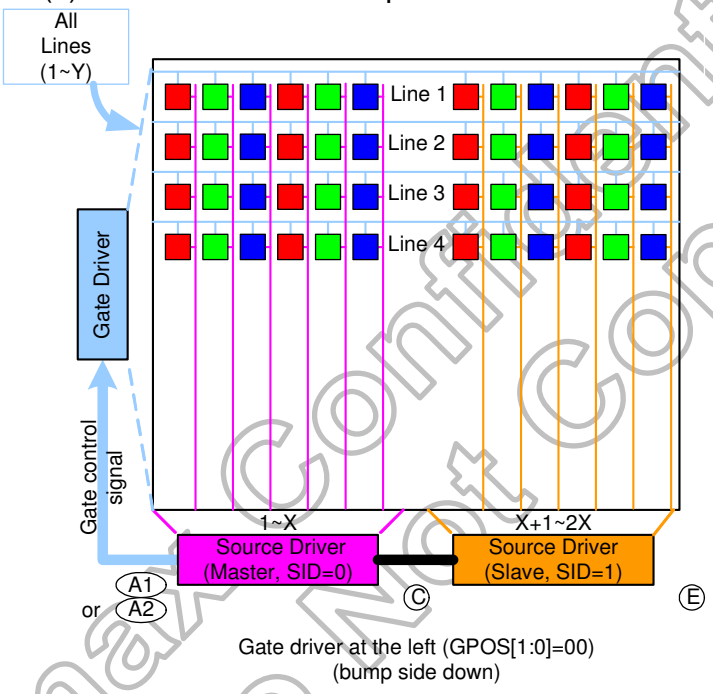


Figure 5.2: Gate driver(s) at the left side of the panel

B. Gate driver(s) at the right side of the panel.

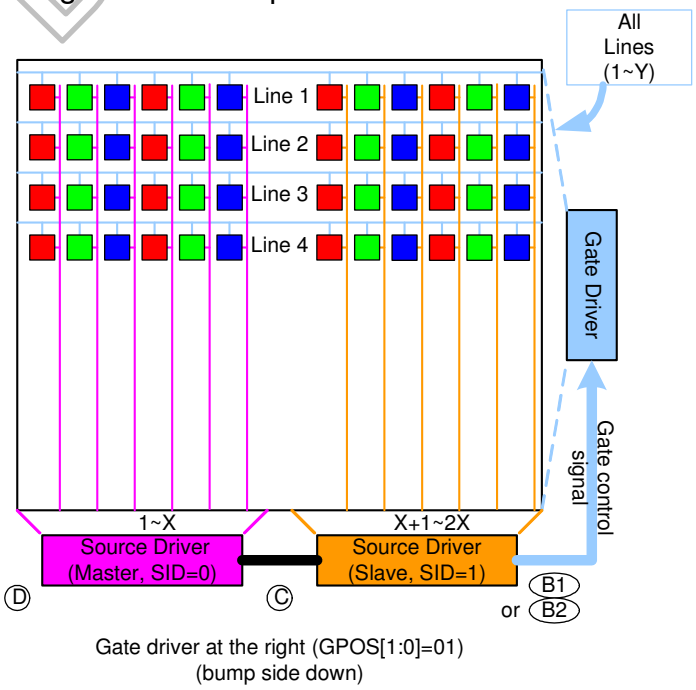


Figure 5.3: Gate driver(s) is at the right side of the panel

C. Gate drivers at the dual side of the panel. The left gate driver(s) controls the odd lines, and the right gate driver(s) controls the even lines.

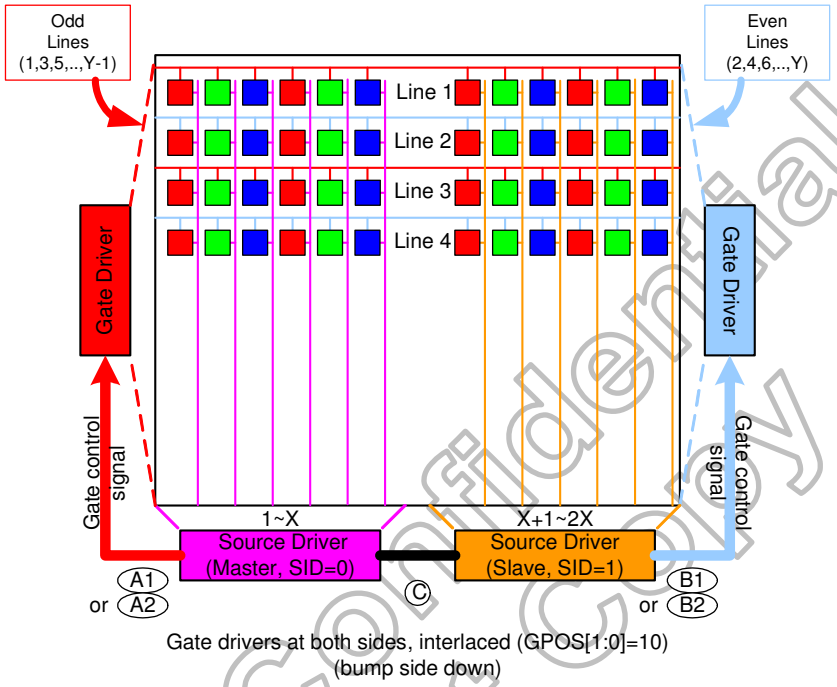


Figure 5.4: Gate driver(s) at both sides of the panel, interlaced driving

D. Gate drivers at both sides of the panel. The left and the right gate drivers control the same lines at the same time.

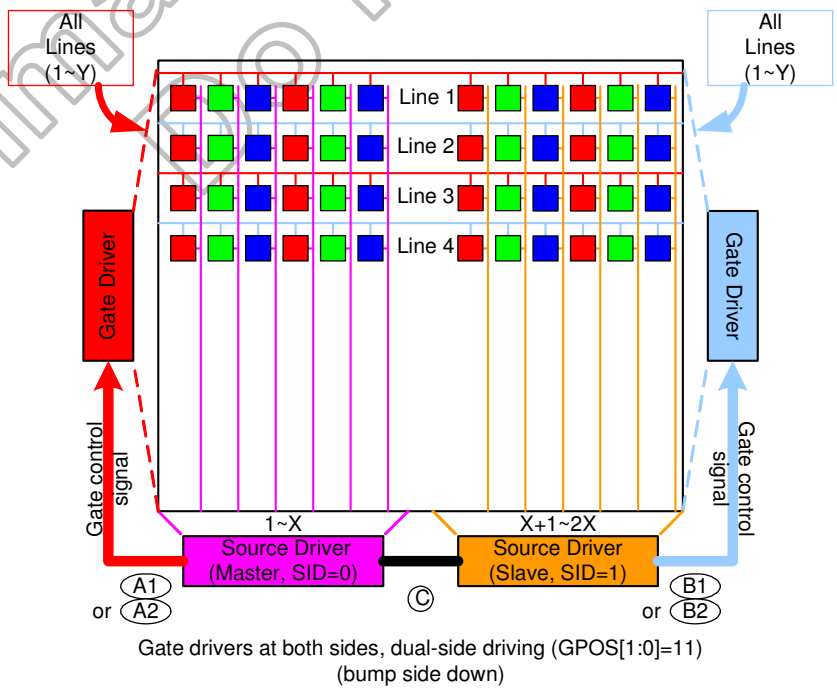
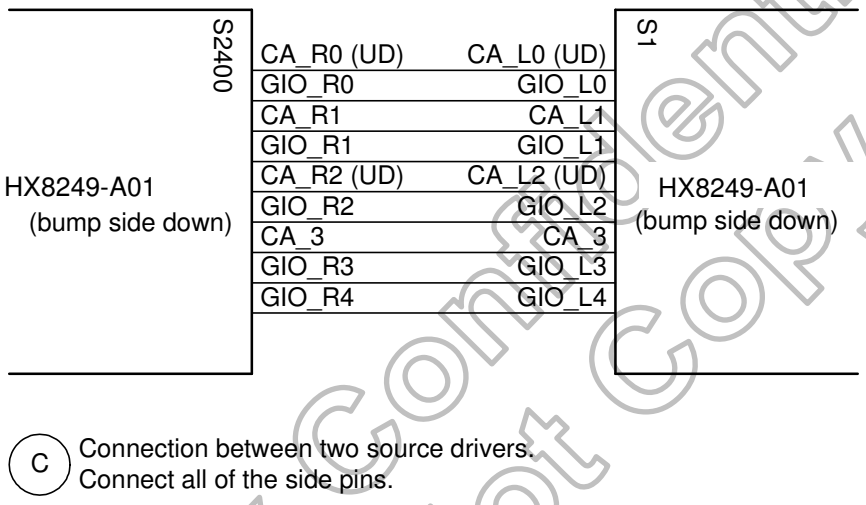


Figure 5.5: Gate driver(s) at both sides of the panel, dual-side driving

5.2.2 Cascade and gate driver control interface connections

A. Connections to the gate driver(s) depend on the type of the gate driver(s). Refer to “Gate driver type definition”.
B. Between each source drivers, it is suggested to connect all of the side pins **(case C)**.
C. Leave all of the side pins of the master chip floating if the gate driver(s) is at the right side **(case D)**. Leave all of the side pins of the slave chip floating if the gate driver(s) is at the left side **(case E)**.



C Connection between two source drivers.
Connect all of the side pins.

D Connection to nothing at the left side.
Leave all of the side pins open.

E Connection to nothing at the right side.
Leave all of the side pins open.

Figure 5.6: Cascade and gate driver control interface

5.2.3 Gate driver type definition

Two type sequences of gate driver control pins are supported.

A. Type 1: GSQ should be set to 0 when using this type of gate driver, such as HX8660-B, HX8677-C and HX8678-A. Note that CA_L2 and CA_R2 pins are used as up/down control.

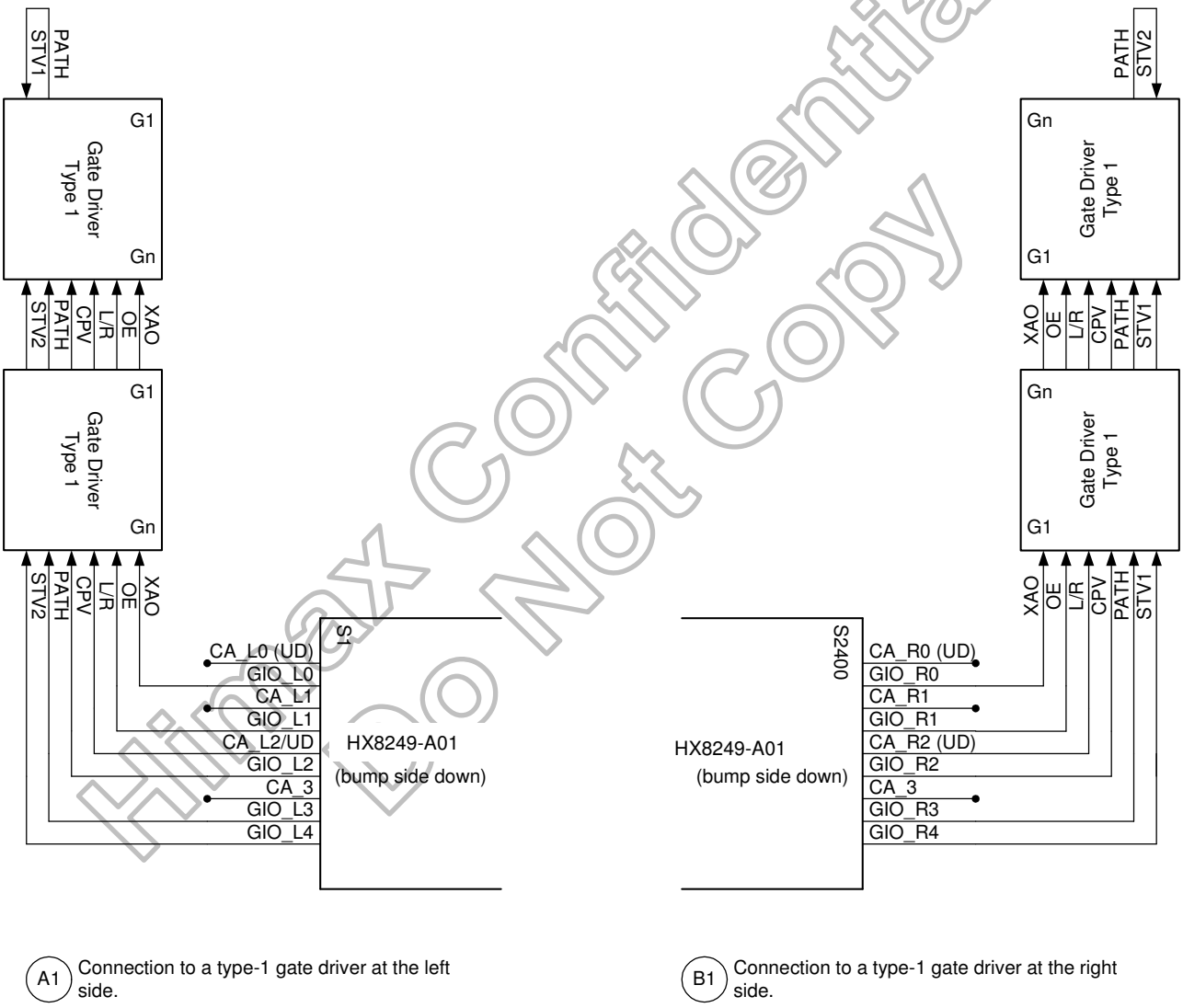


Figure 5.7: Gate control interface for type-1 gate drivers

B. Type 2: GSQ should be set to 1 when using this type of gate driver. Note that CA_L0 and CA_R0 are used as up/down control.

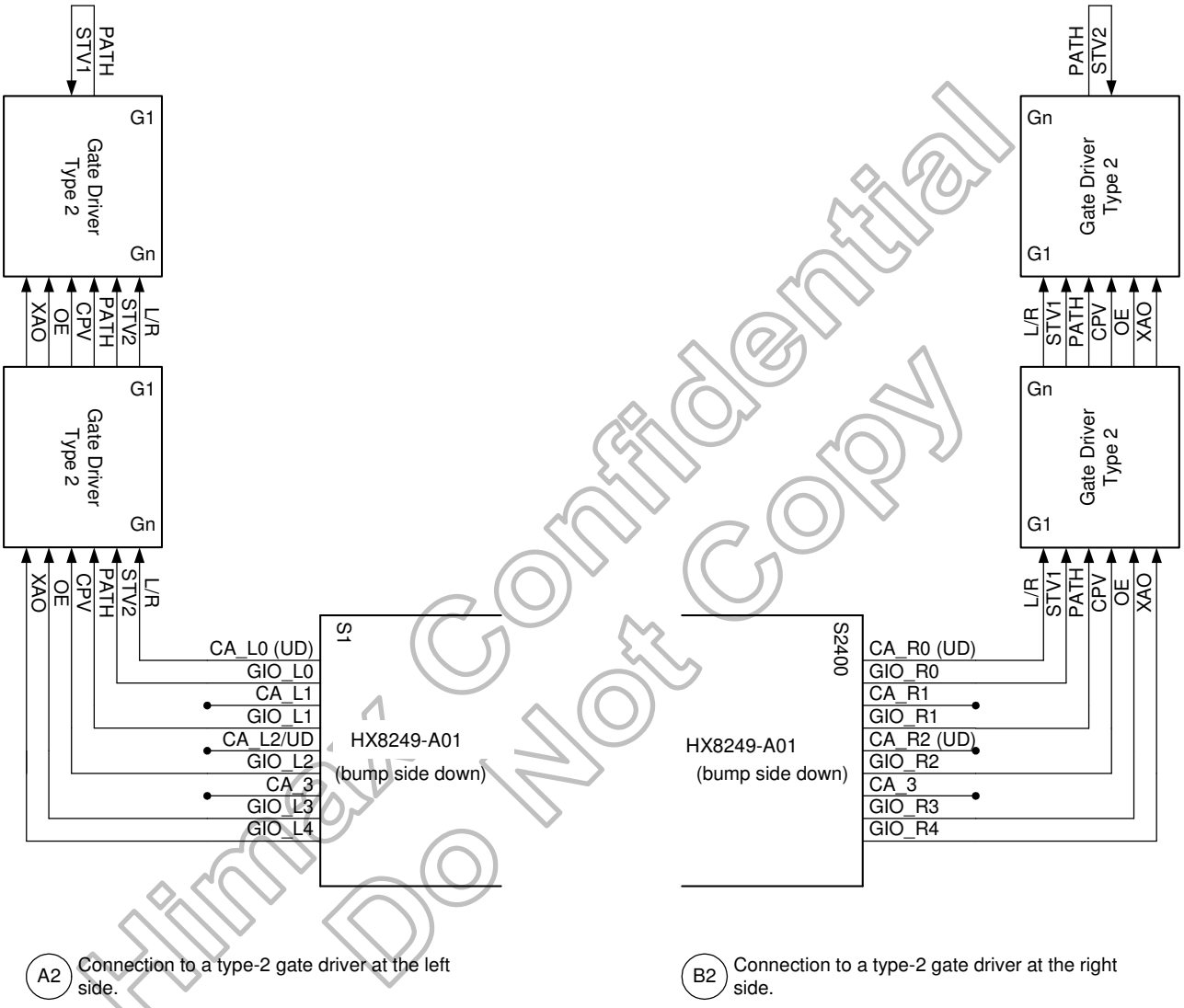


Figure 5.8: Gate control interface for type-2 gate drivers

5.2.4 Gate driver control signal definition

A. When only one source driver is used, CA_L0/CA_L2/CA_R0/CA_R2 of the chip are used as UD.

	GSQ	GPOS[1:0]	TB	CA_L0/UD	GIO_L0	GIO_L1	CA_L2/UD	GIO_L2	GIO_L3	GIO_L4	CA_R0/U	GIO_R0	GIO_R1	CA_R2/U	GIO_R2	GIO_R3	GIO_R4
master (single chip)	0	00	0	0	XAO	OEV	0	CPV	input (HZ)	STV	1	XAO	0	1	0	0	0
			1	1	XAO	OEV	1	CPV	STV	input (HZ)	0	XAO	0	0	0	0	0
		01	0	0	0	0	0	0	0	0	1	XAO	OEV	1	CPV	input (HZ)	STV
			1	1	0	0	1	0	0	0	0	XAO	OEV	0	CPV	STV	input (HZ)
		10	0	0	XAO	OEV_B	0	CPV_B	input (HZ)	STV_B	1	XAO	OEV_A	1	CPV_A	input (HZ)	STV_A
			1	1	XAO	OEV_A	1	CPV_A	STV_A	input (HZ)	0	XAO	OEV_B	0	CPV_B	STV_B	input (HZ)
		11	0	0	XAO	OEV	0	CPV	input (HZ)	STV	1	XAO	OEV	1	CPV	input (HZ)	STV
			1	1	XAO	OEV	1	CPV	STV	input (HZ)	0	XAO	OEV	0	CPV	STV	input (HZ)
	1	00	0	0	STV	input (HZ)	0	CPV	OEV	XAO	1	0	0	1	0	0	XAO
			1	1	input (HZ)	STV	1	CPV	OEV	XAO	0	0	0	0	0	0	XAO
		01	0	0	0	0	0	0	0	0	1	STV	input (HZ)	1	CPV	OEV	XAO
			1	1	0	0	1	0	0	0	0	input (HZ)	STV	0	CPV	OEV	XAO
		10	0	0	STV_B	input (HZ)	0	CPV_B	OEV_B	XAO	1	STV_A	input (HZ)	1	CPV_A	OEV_A	XAO
			1	1	input (HZ)	STV_A	1	CPV_A	OEV_A	XAO	0	input (HZ)	STV_B	0	CPV_B	OEV_B	XAO
		11	0	0	STV	input (HZ)	0	CPV	OEV	XAO	1	STV	input (HZ)	1	CPV	OEV	XAO
			1	1	input (HZ)	STV	1	CPV	OEV	XAO	0	input (HZ)	STV	0	CPV	OEV	XAO

Table 5.5: Gate driver signal definition table, single chip

B. When source drivers are cascaded: CA_L0 and CA_L2 of the master chip are used as UD. CA_R0 and CA_R2 are used as cascade control.

	GSQ	GPOS[1:0]	TB	CA_L0/UD	GIO_L0	GIO_L1	CA_L2/UD	GIO_L2	GIO_L3	GIO_L4	CA_R0/U	GIO_R0	GIO_R1	CA_R2/U	GIO_R2	GIO_R3	GIO_R4
master (cascaded)	0	00	0	0	XAO	OEV	0	CPV	input (HZ)	STV	CA0	XAO	0	CA2	0	0	0
			1	1	XAO	OEV	1	CPV	STV	input (HZ)	CA0	XAO	0	CA2	0	0	0
		01	0	0	0	0	0	0	0	0	CA0	XAO	OEV	CA2	CPV	input (HZ)	STV
			1	1	0	0	1	0	0	0	CA0	XAO	OEV	CA2	CPV	STV	input (HZ)
		10	0	0	XAO	OEV_B	0	CPV_B	input (HZ)	STV_B	CA0	XAO	OEV_A	CA2	CPV_A	input (HZ)	STV_A
			1	1	XAO	OEV_A	1	CPV_A	STV_A	input (HZ)	CA0	XAO	OEV_B	CA2	CPV_B	STV_B	input (HZ)
		11	0	0	XAO	OEV	0	CPV	input (HZ)	STV	CA0	XAO	OEV	CA2	CPV	input (HZ)	STV
			1	1	XAO	OEV	1	CPV	STV	input (HZ)	CA0	XAO	OEV	CA2	CPV	STV	input (HZ)
	1	00	0	0	STV	input (HZ)	0	CPV	OEV	XAO	CA0	0	0	CA2	0	0	XAO
			1	1	input (HZ)	STV	1	CPV	OEV	XAO	CA0	0	0	CA2	0	0	XAO
		01	0	0	0	0	0	0	0	0	CA0	STV	input (HZ)	CA2	CPV	OEV	XAO
			1	1	0	0	1	0	0	0	CA0	input (HZ)	STV	CA2	CPV	OEV	XAO
		10	0	0	STV_B	input (HZ)	0	CPV_B	OEV_B	XAO	CA0	STV_A	input (HZ)	CA2	CPV_A	OEV_A	XAO
			1	1	input (HZ)	STV_A	1	CPV_A	OEV_A	XAO	CA0	input (HZ)	STV_B	CA2	CPV_B	OEV_B	XAO
		11	0	0	STV	input (HZ)	0	CPV	OEV	XAO	CA0	STV	input (HZ)	CA2	CPV	OEV	XAO
			1	1	input (HZ)	STV	1	CPV	OEV	XAO	CA0	input (HZ)	STV	CA2	CPV	OEV	XAO

Table 5.6: Gate driver signal definition table, master in cascade

CA_R0 and CA_R2 of the slave chip are used as UD.

	GSQ	GPOS[1:0]	TB	CA_L0/UD	GIO_L0	GIO_L1	CA_L2/UD	GIO_L2	GIO_L3	GIO_L4	CA_R0/U	GIO_R0	GIO_R1	CA_R2/U	GIO_R2	GIO_R3	GIO_R4
slave (cascaded)	0	00	0	input (HZ)							1	GIO_L0	GIO_L1	1	GIO_L2	input (HZ)	GIO_L4
			1								0			0		GIO_L3	input (HZ)
		01	0								1			1		input (HZ)	GIO_L4
			1								0			0		GIO_L3	input (HZ)
		1X	0								1			1		input (HZ)	GIO_L4
			1								0			0		GIO_L3	input (HZ)
	1	00	0	input (HZ)							1	GIO_L0	input (HZ)	1	GIO_L2	GIO_L3	GIO_L4
			1								0	input (HZ)	GIO_L1	0			
		01	0								1	GIO_L0	input (HZ)	1			
			1								0	input (HZ)	GIO_L1	0			
		1X	0								1	GIO_L0	input (HZ)	1			
			1								0	input (HZ)	GIO_L1	0			

Table 5.7: Gate driver signal definition table, slave in cascade

5.2.5 Cascade design: Voltage outputs

A. The following voltages are provided by the master chip and should be connected to the slave chip:
AVDDP, AVDDN, VGMPH, VGMPM, VGMPL, VGMNH, VGMNM, VGMNL.
B. The following voltages are provided by the master chip and do not need to connect to slave chip:
VGH, VGL, VCOM.
C. The following voltages are provided by each chip with separate capacitors:
VSDP, VSDN
D. The following voltages are provided by each chip with common capacitors:
DVDD, VDDLV, VCL.
E. Set the following registers of the master to 1, and registers of the slave to 0:
AVDDPEN, AVDDNEN, VGMREFEN, VGHEN, VGLEN, VCOMEN.
F. Note that for the master chip, do not connect gamma voltage inputs VGMPHI / VGMPMI / VGMPLI / VGMNHI / VGMNMI / VGMNLI to VGMPHO / VGMPMO / VGMPLO / VGMNHO / VGMNMO / VGMNLO on panel, but connect them through FPC or PCB traces. This helps to reduce difference between gamma voltages of each chip.
G. VCOM can be connected to the panel through VCOM_L and VCOM_R pins of each chip.

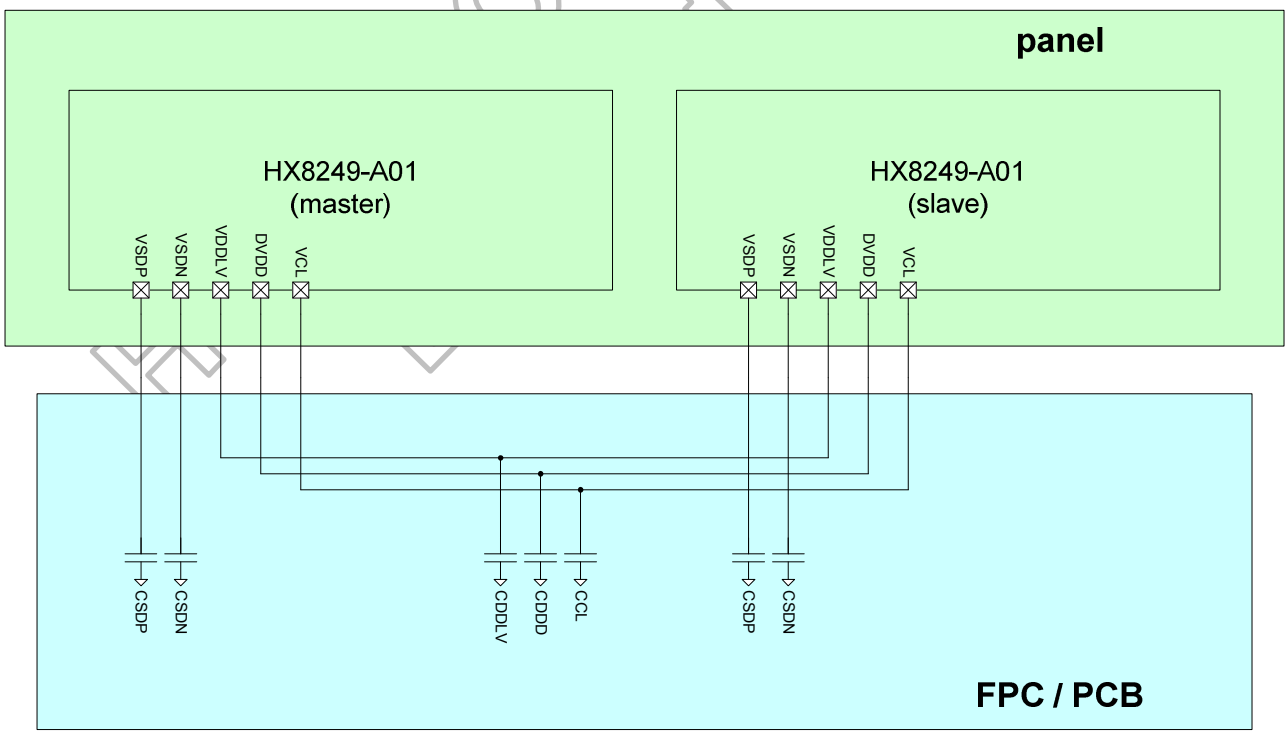


Figure 5.9: Cascade design for regulator outputs

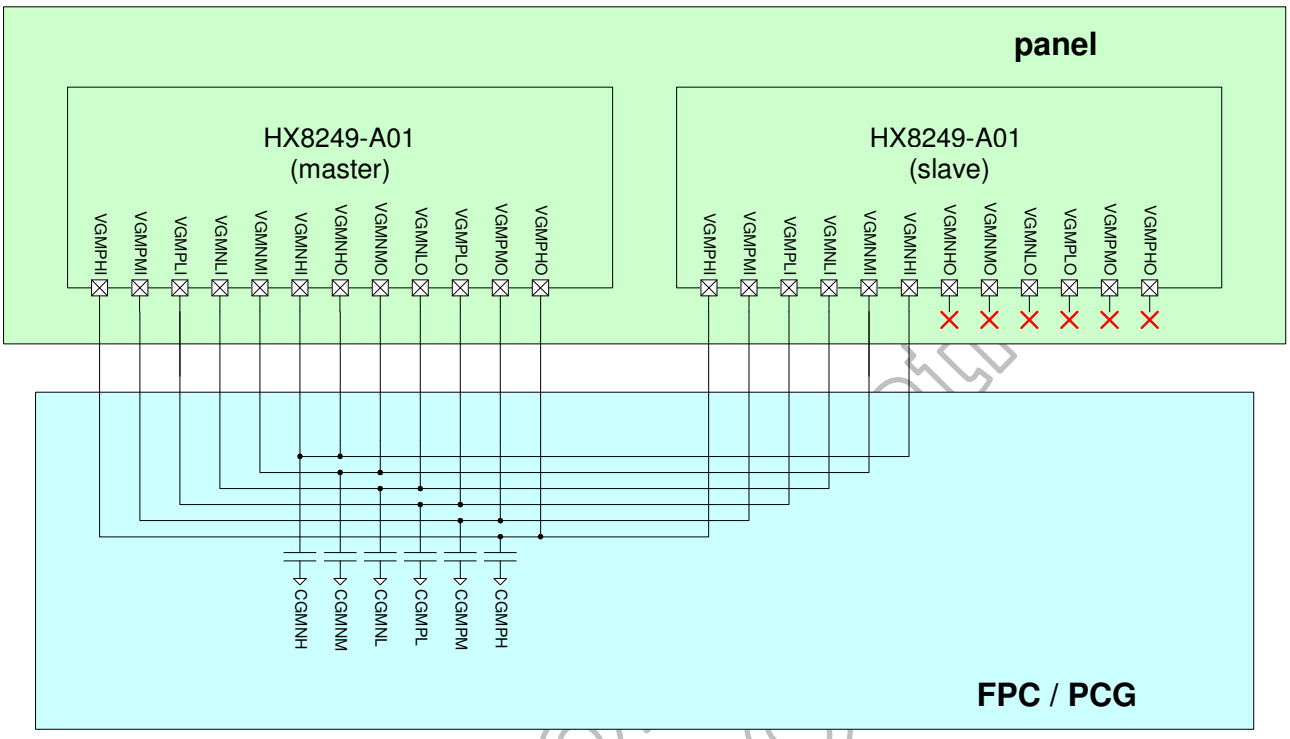


Figure 5.10: Cascade design for gamma reference voltages

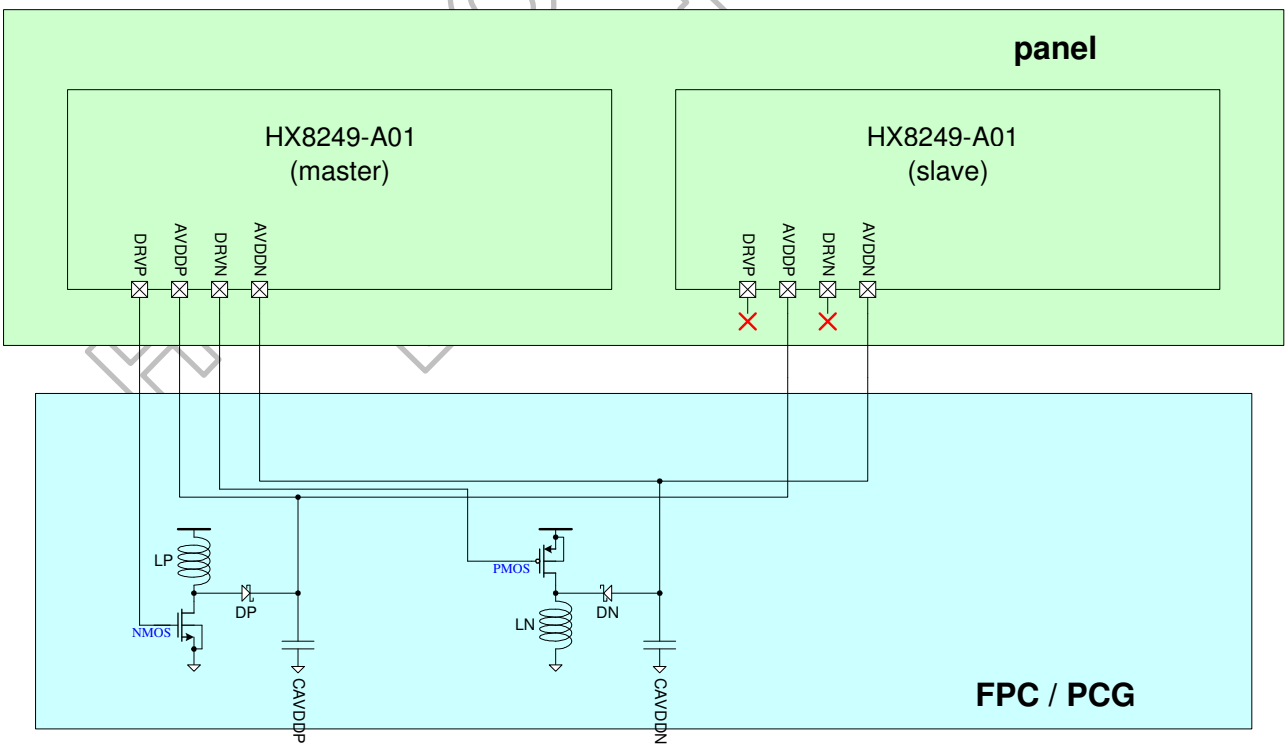


Figure 5.11: Cascade design for PFM

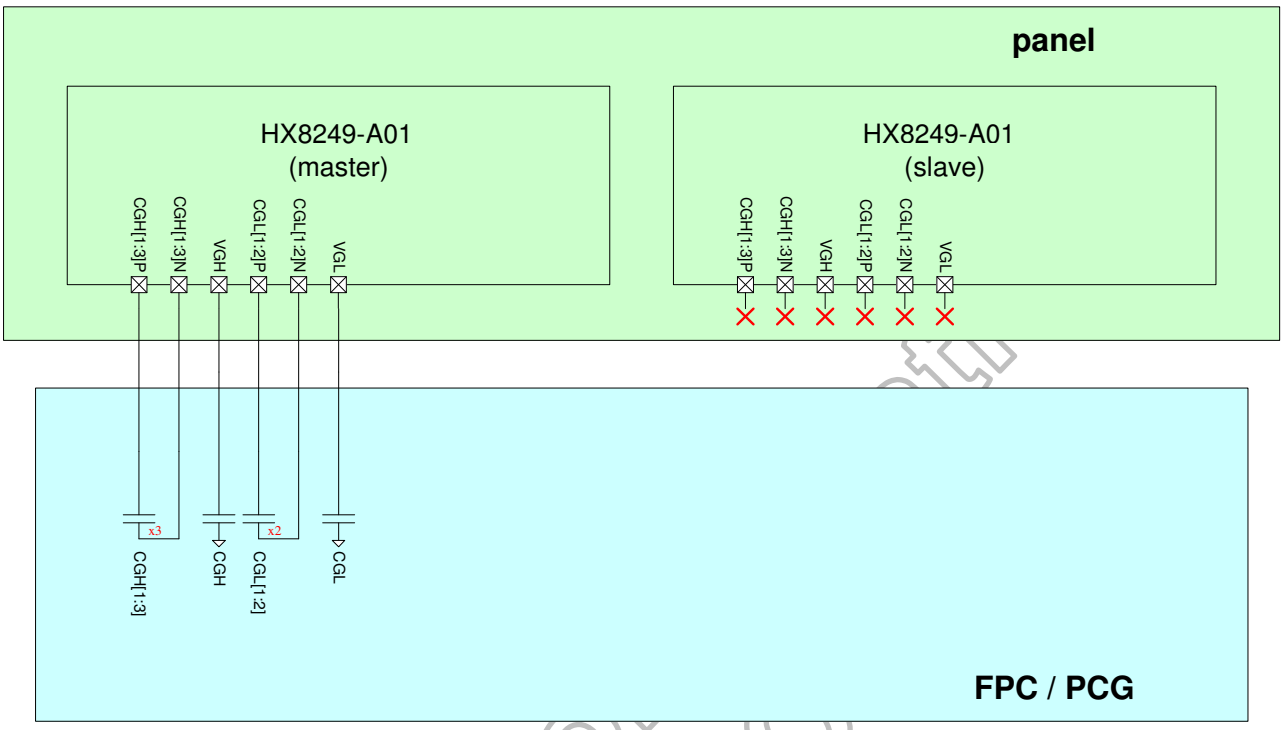


Figure 5.12: Cascade design for charge pumps

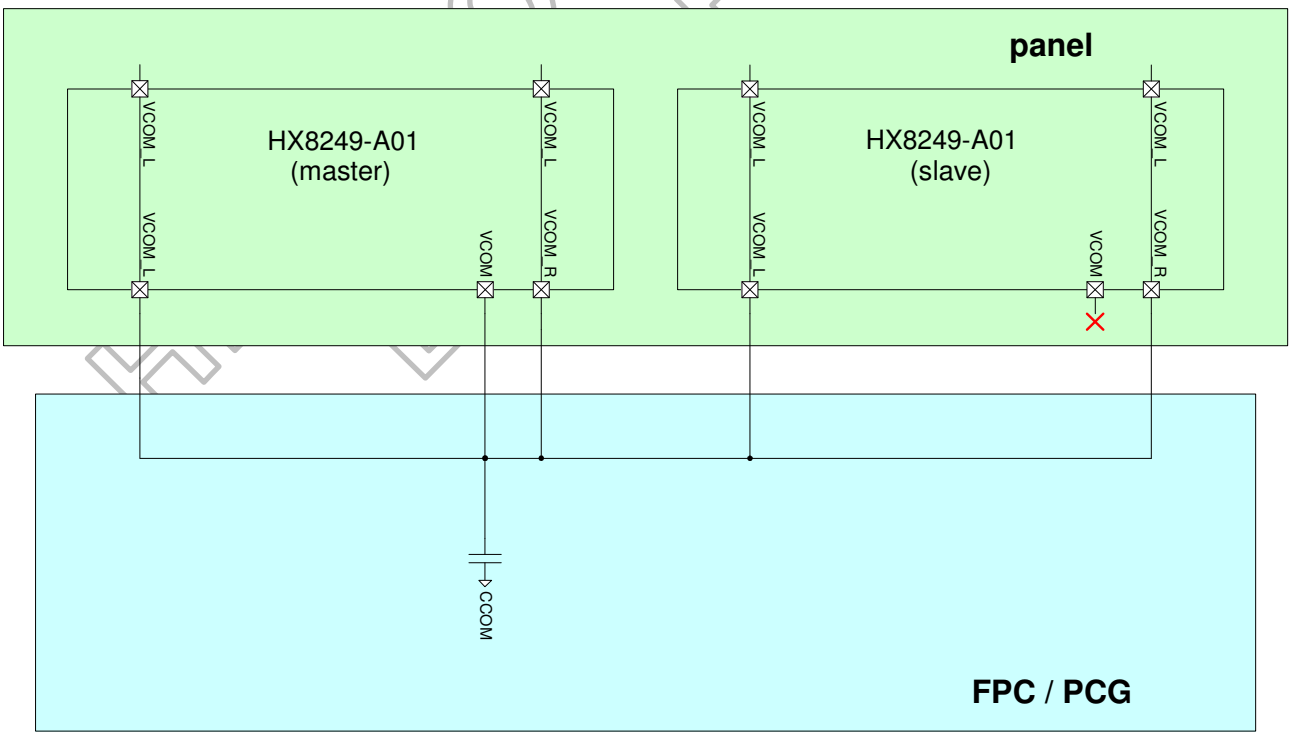
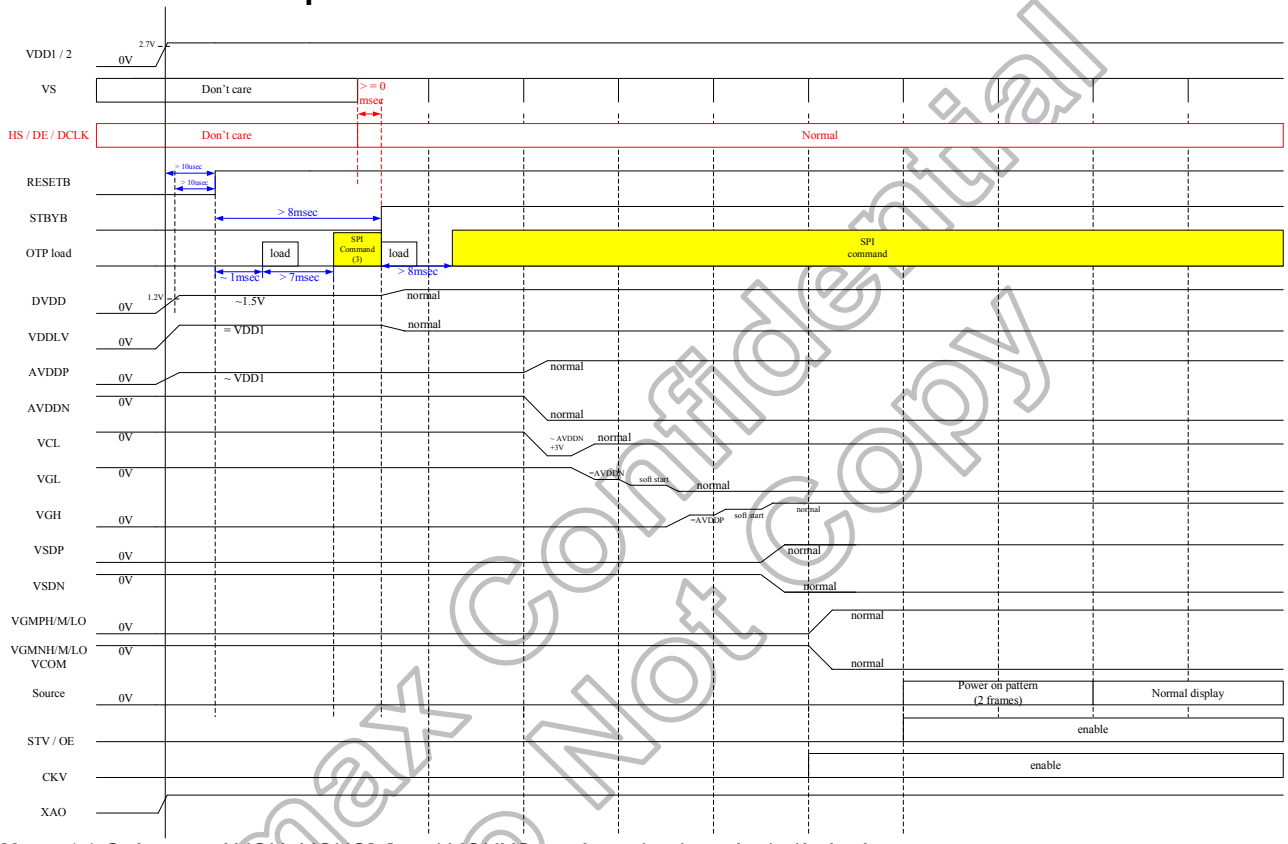


Figure 5.13: Cascade design for VCOM

6. Fuction Description

6.1 Power on/off sequence with internal PFM

6.1.1 Power on sequence



Note: (1) Soft start of VGH: VGHS[2] and VGHXS are forced to be 0 for half of a frame .
(2) Soft start of VGL: VGLS[2] and VGLXS are forced to be 0 for half of a frame.
(3) Registers RS[3:0], GATEPASS[3:0], GATENUM[9:0], MODE and all registers in page 8 **(LVDS settings)** should be set before STBYB is pulled to 1.
(4) If the application system is not able to completely follow the power on sequence shown above, please contact Himax for suggestions.

Figure 6.1: Power on sequence with internal PFM

6.1.2 Power off sequence

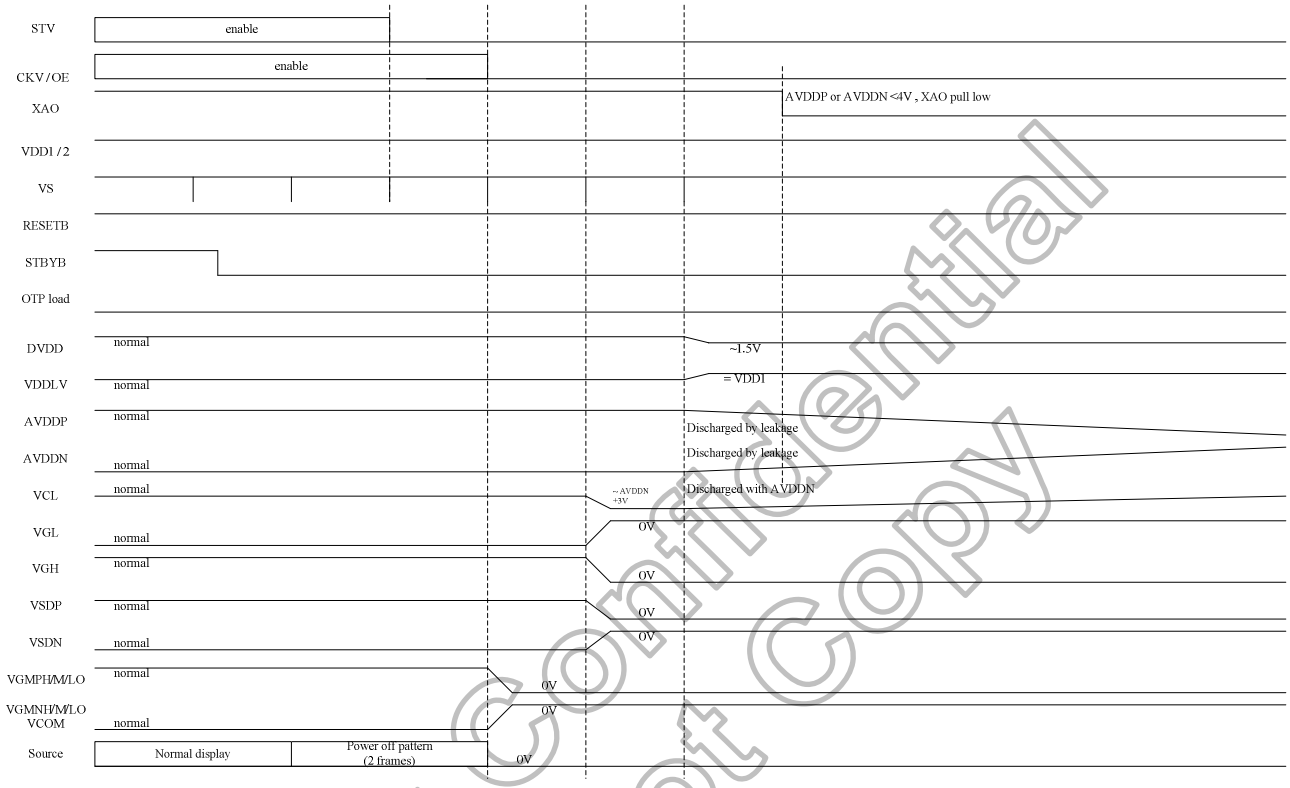


Figure 6.2: Power off sequence with internal PFM

6.2 Power on/off sequence with external AVDDP/AVDDN

6.2.1 Power on sequence

External power AVDDP/AVDDN need to be supplied before point A.

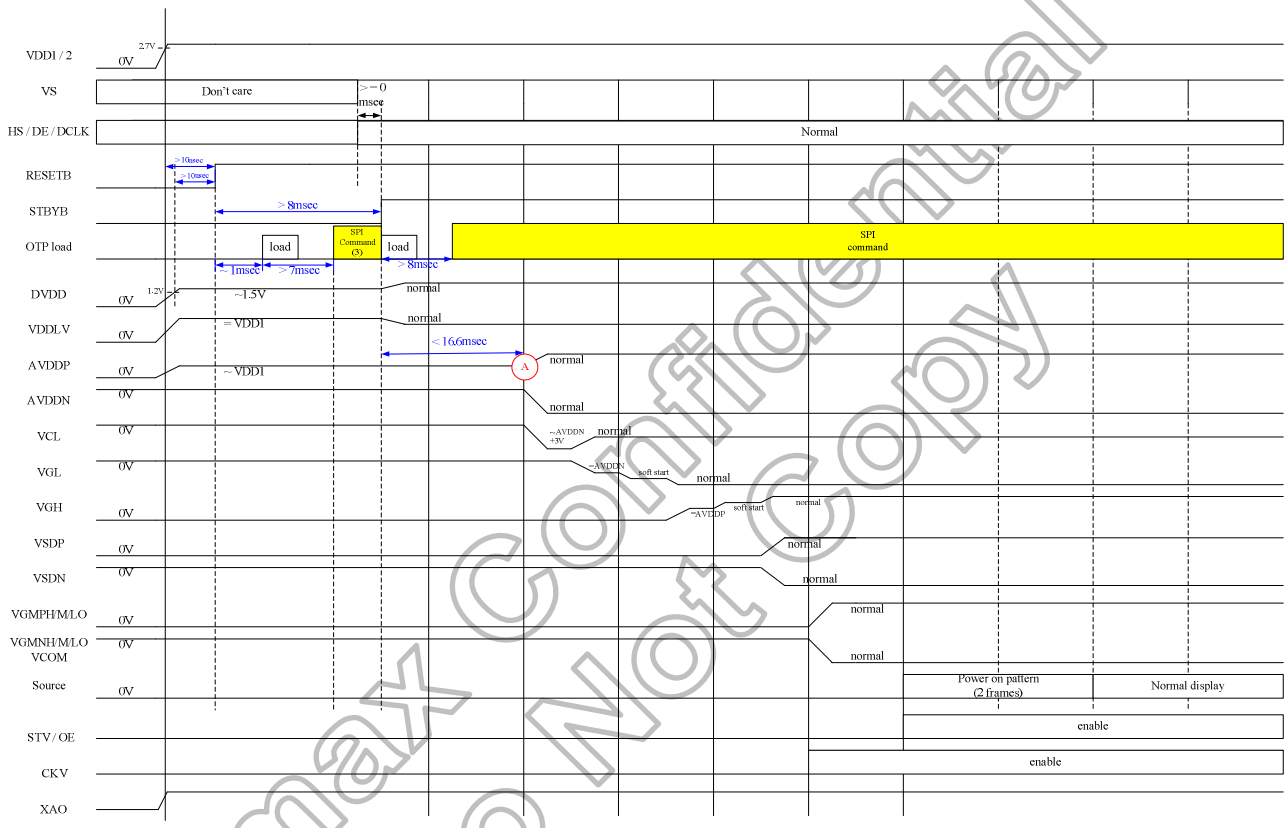


Figure 6.3: Power on sequence with external AVDDP/AVDDN

6.2.2 Power off sequence

External power AVDDP/AVDDN need to be removed after point B.

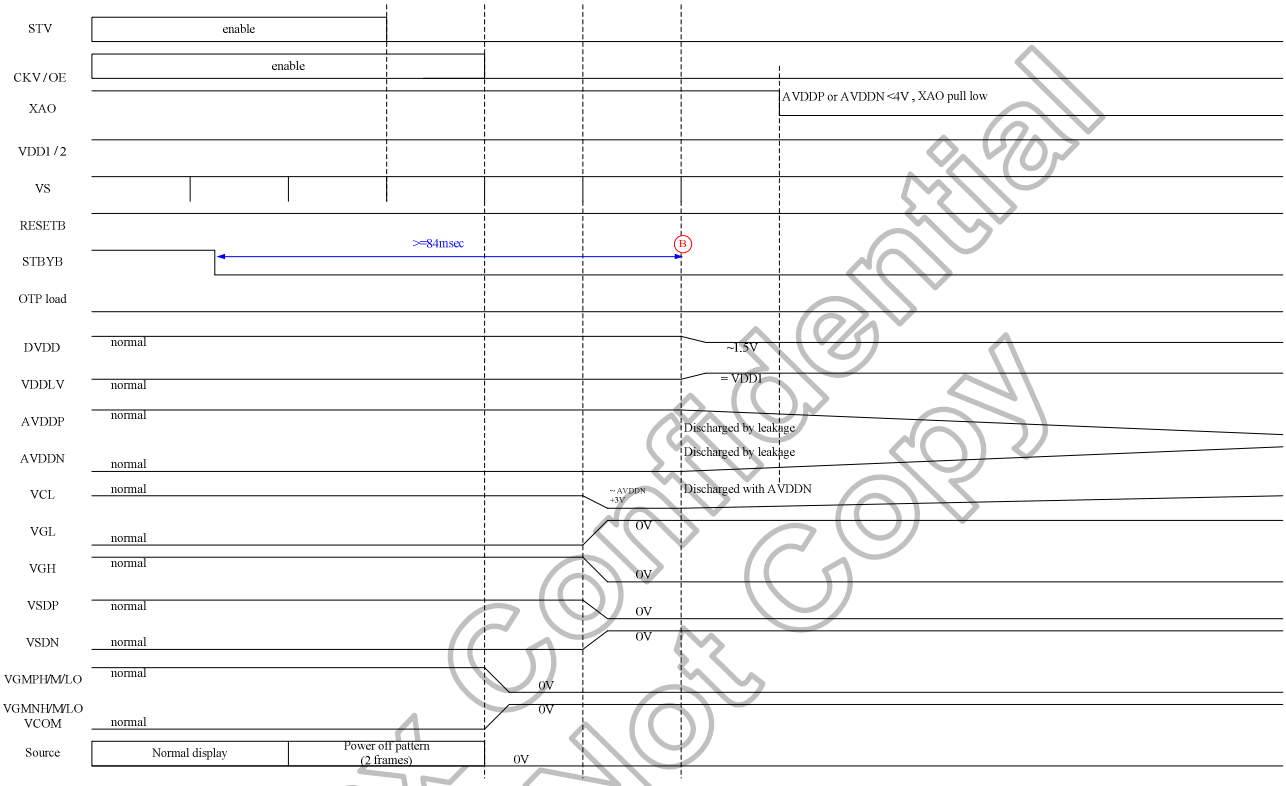


Figure 6.4: Power off sequence with external AVDDP/AVDDN

6.3 BIST function

A pattern generator is embedded for BIST **(Built-In Self Test)** mode. When BISTEN is set to 1 **(by input pin or register)**, built-in patterns will be displayed. These patterns can be selected by register PTSEL[3:0]. When PTSEL[3:0] is set to 1010~1111, pattern 0 to 9 will be displayed sequentially and periodically. Frame rate in BIST mode is set to 60Hz, but only for the 14 typical resolutions selected by RS[3:0].

Pattern number	Pattern name	Color	R	G	B
0	Full black	C1	0	0	0
1	Full white	C1	255	255	255
2	Full red	C1	255	0	0
3	Full green	C1	0	255	0
4	Full blue	C1	0	0	255
5~8	Vcom trimming 1~4	C1	127	0	127
		C2	0	127	0
9	Pixel on-off	C1	127	0	127
		C2	0	127	0

Note: (1) Source output shift direction is fixed **(SOUT1→SOUT2400, RL=1)** in BIST mode.
(2) If manual **(vertical or horizontal)** resolution selection is enabled, BIST function is not supported.

Table 6.1: BIST patterns

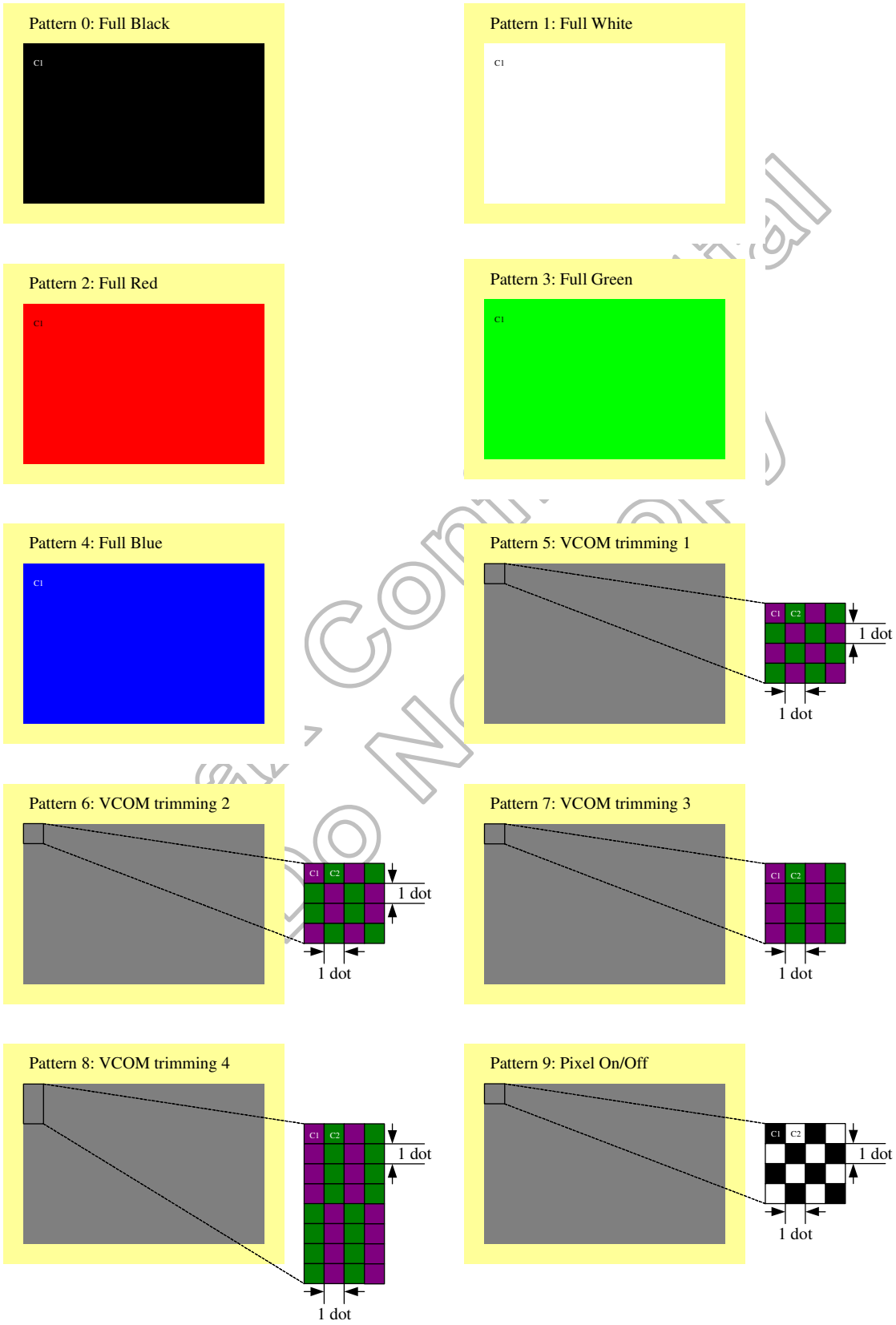


Figure 6.5: BIST patterns

6.4 Protection modes

6.4.1 GAS mode

When power is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS **(gate all select)** function can speed the process that image disappears.

HX8249-A01 can detect abnormally low voltage and send GAS signal **(/XAO)** to the gate driver to discharge residual potential in LCD panel and removes image.

Any one of the following cases with duration larger than 10usec will trigger GAS function. And /XAO signal will be pulled low for gate driver to set all gates output to high.

A. VDD1/2 is lower than 2V
B. AVDDP is lower than 4V
C. AVDDN is higher than -4V

6.4.2 Self protection mode

HX8249-A01 keeps detecting input signals DE, HS, VS, and DCLK. If any of these signals is missing, HX8249-A01 will enter self protection mode. In the self protection mode, it would display black or white pattern which are set with register SPFSEL. Frame rate in self protection mode is set to 60Hz, but only for the 14 typical resolutions selected by RS[3:0].

The open-drain pin CA3 can be used to indicate self protection mode. Normally CA3 is pulled low by an on-chip resistor, and it will become high when the chip is in self protection mode.

Please be aware that it's forbidden to power on HX8249-A01 with self protection mode. All input signals DE (DE only mode), HS (HS+VS mode), VS (HS+VS mode), and DCLK must be supplied before STBYB is set to H.

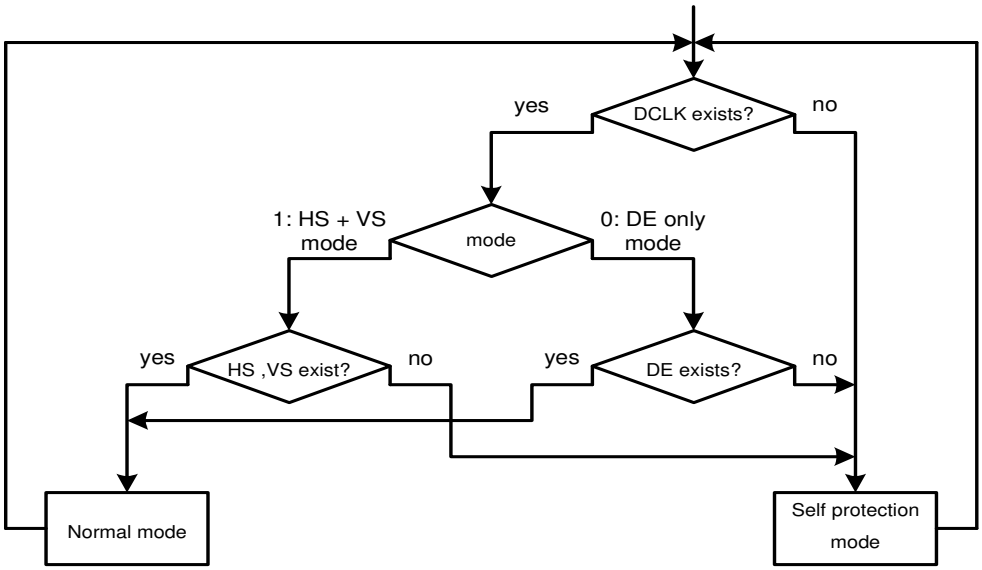


Figure 6.6: Self-protection detection

6.5 PFM settings and VDD level detection

VDD level detection is enabled when VDDTEN=1. A threshold Vthd is set by register VDDTS[1:0], and PFM applies different settings for high or low VDD level.

PFM also applies different settings for half of the first frame that PFM is enabled when power on.

VDDTEN	VDD level	PFM settings, power on	PFM settings, normal
0	＞Vthd	TON_PLS / TOFF_PLS TON_NLS / TOFF_NLS	TON_PL / TOFF_PL TON_NL / TOFF_NL
	≦Vthd		
1	＞Vthd	TON_PHS / TOFF_PHS TON_NHS / TOFF_NHS	TON_PH / TOFF_PH TON_NH / TOFF_NH
	≦Vthd	TON_PLS / TOFF_PLS TON_NLS / TOFF_NLS	TON_PL / TOFF_PL TON_NL / TOFF_NL

Table 6.2: PFM settings and VDD level detection

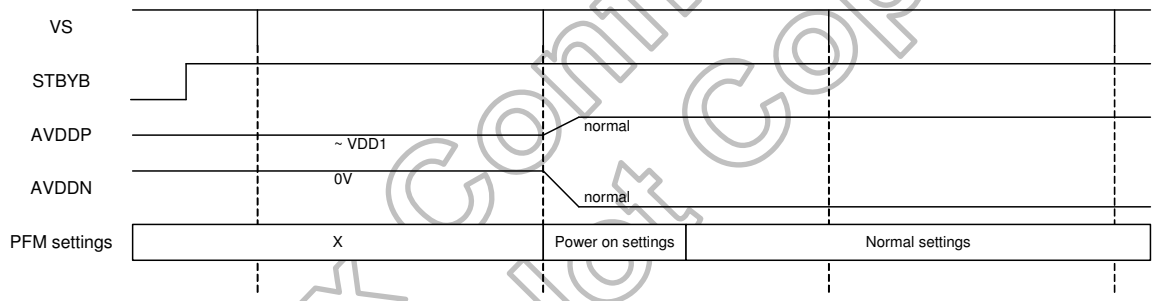


Figure 6.7: PFM power on and settings

6.6 Data processing

Input 8-bit RGB data from TTL or LVDS interface is processed in the following order.

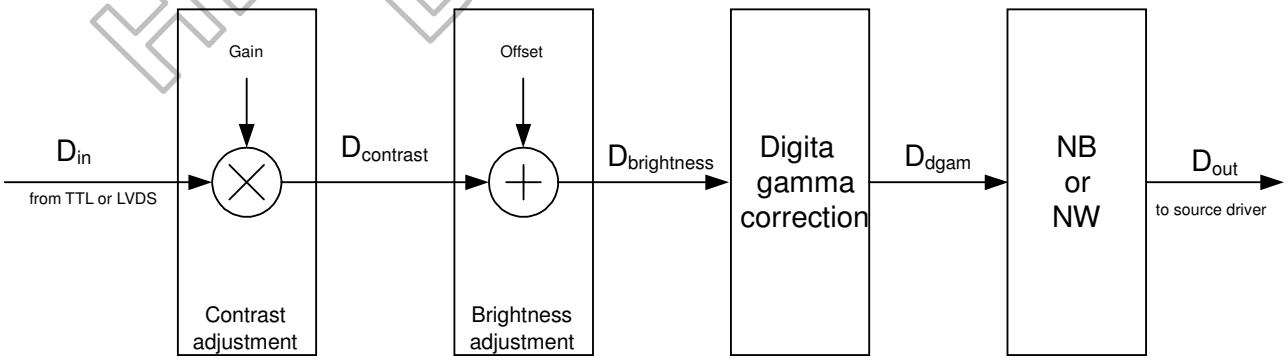


Figure 6.8: Data processing

6.6.1 Contrast adjustment

Contrast adjustment is done on RGB data separately by multiplying a gain ranging from 0.5 to 1.496. The gain for each color is set with 3 sets of 8-bit registers **(RGC [7:0], GGC[7:0], BGC[7:0])**. If the resulting output data exceeds 255, it will be clamped to 255. Default gain value is 1.0.

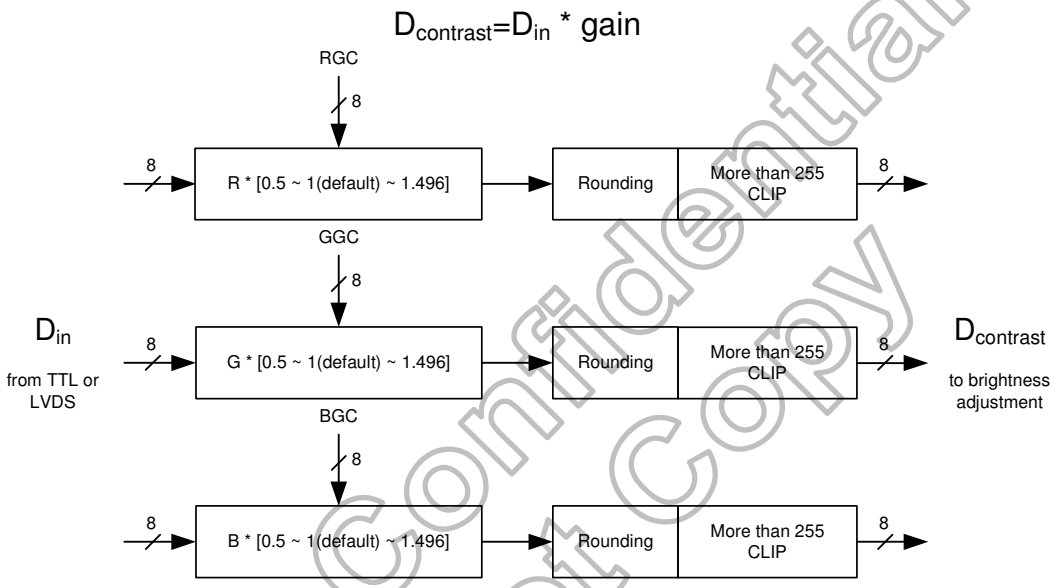


Figure 6.9: Contrast adjustment

6.6.2 Brightness adjustment

Brightness adjustment is done on RGB data separately by adding an offset ranging from -16 to +47. The offset of each color is set with 3 sets of 6-bit registers **(ROB[5:0], GOB[5:0], BOB[5:0])**. If the resulting output data exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

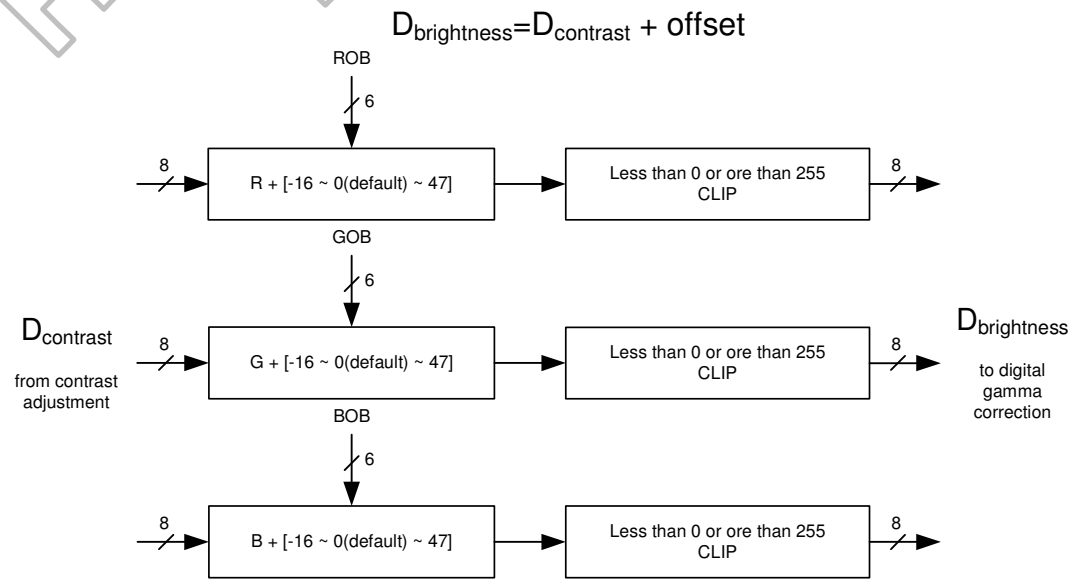


Figure 6.10: Brightness adjustment

6.6.3 Digital gamma correction

The digital gamma correction is done on RGB data separately with 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values Y1~Y24 **(in register page 2~4)** for level X1~X24=0, 1, 3, 7, 11, 15, 23, 31, 41, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. Y on X between Xn and Xn+1 is interpolated with the following equations.

$$Y = Y_n + (Y_{n+1} - Y_n) * (X-X_n) / (X_{n+1}-X_n)$$

The gamma correction output 10-bit data D_{dgam} is then fed to 8-bit DAC and OP to drive the source lines on the panel with dithering.

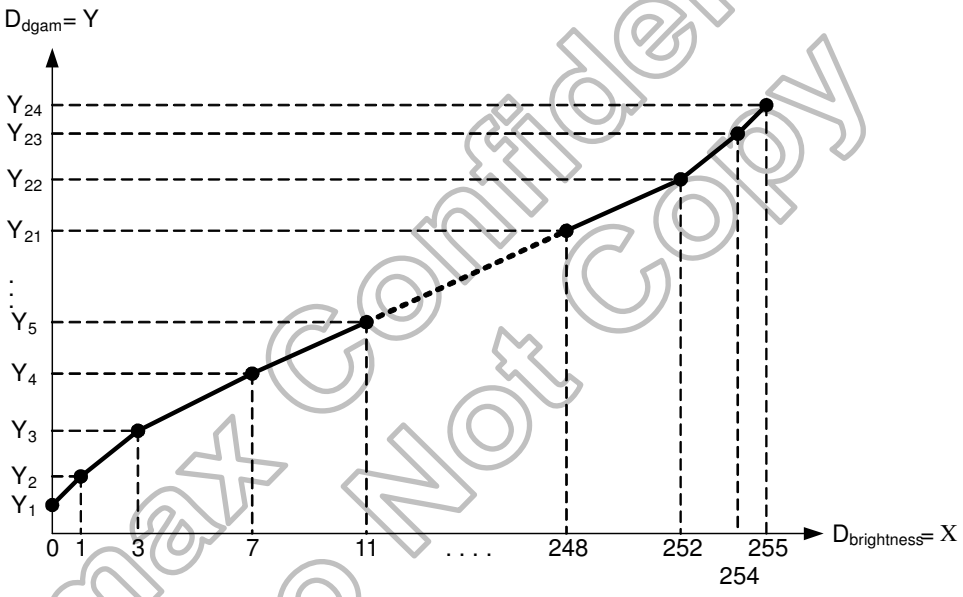


Figure 6.11: Digital gamma correction

6.6.4 NB/NW selection

The data after digital gamma processing D_{dgam} will go to NB/NW block. It will transfer input data to corresponding correct NB or NW data.

6.7 Interlaced input

Normally polarity changes by frame for LCD display. HX8249-A01 support two frame polarity change for interlaced data input. When INTL=1, polarity change by two frames.

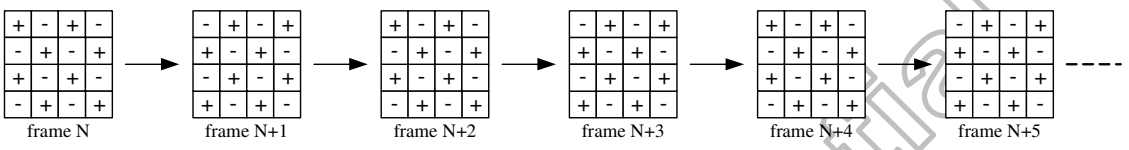


Figure 6.12: INTL=0: Polarity changes by frame

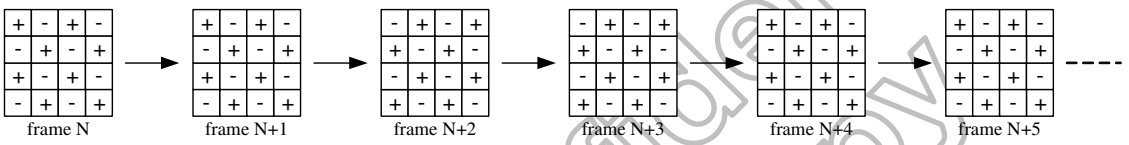


Figure 6.13: INTL=1: Polarity changes by two frames

6.8 TPSYNC

HX8249-A01 provides an output TPSYNC for tough panel synchronization. It can be adjusted by page 0 registers TPSEL & TPOFFSET.

6.9 SPI Interface

HX8249-A01 supports 3-wire SPI **(serial peripheral interface)** to set internal registers. Setting one command needs 16 SCL clocks.

A. The first bit R/W selects read/write mode. Setting R/W to 0 selects write mode, and setting R/W to 1 selects read mode.
B. If there are two chips cascaded, the second bit SID select chip being active. Note that when SIDEN=0 and R/W=1, only read from the master chip.

SIDEN	R/W	SID	Function	Target
0	1	X	Read	Master
	0	X	Write	Master and slave
1	1	0	Read	Master
		1		Slave
	0	0	Write	Master
		1		slave

Table 6.3: Serial Interface timing parameters

C. A[5:0] specify the address of the register to be read or writen.
D. D[7:0] is the 8-bit data of each register.

The address and data are transferred from the MSB to LSB edge sequentially at SCL rising edge.

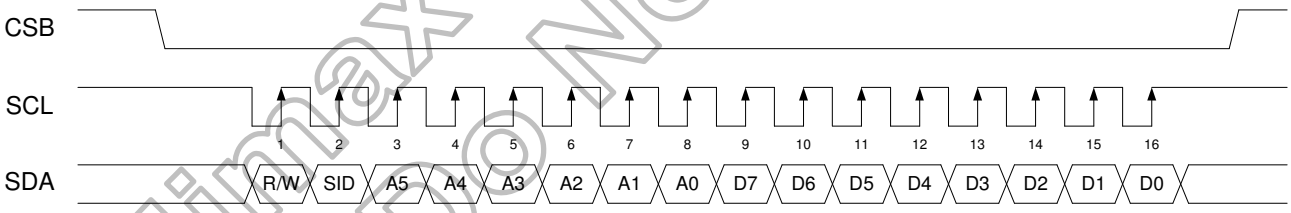


Figure 6.14: SPI format

6.9.1 SPI normal read/write mode

In normal write mode, the read/write control bit must be set to 0, and SDA is address input and data input pin.

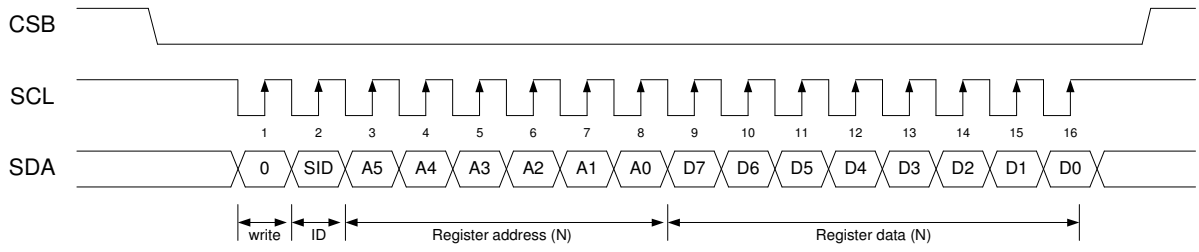


Figure 6.15: SPI signals, normal write mode

In normal read mode, the read/write control bit must be setting 1, and SDA is address input and data output pin.

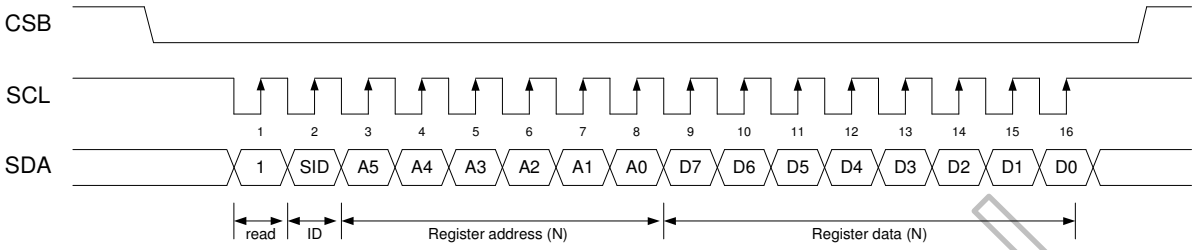


Figure 6.16: SPI signals, normal read mode

6.9.2 SPI burst write mode

HX8249-A01 supports burst mode for writing all registers one time. After choose page want to write , Only the start address is needed, and repeats one set of 8 SCL pulses to access the following registers sequentially.

In burst write mode, the read/write control bit must be set to 0, and SDA is address input and data input pin.

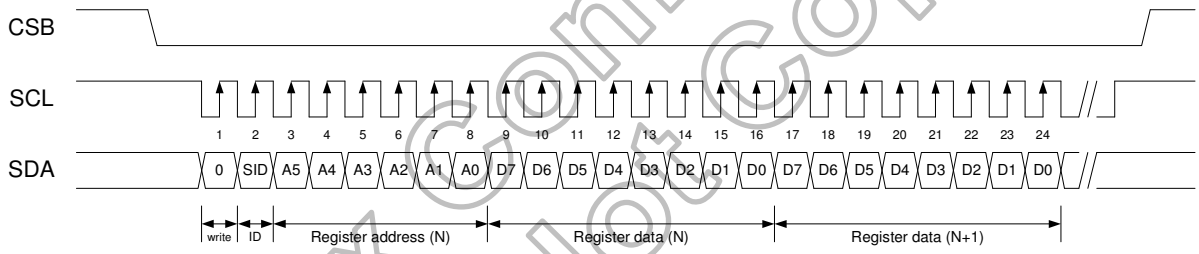


Figure 6.17: SPI signals, burst write mode

Note that burst read is not supported by HX8249-A01.

6.10 OTP Function

All HX8249-A01 registers **(except Vcom)** can be programed twice by OTP function. HX8249-A01 OTP memory is divided into address table1 and table2. Both table1 and table2 are assigned to all registers **(group 1h~ Dh and 19h~1Ah).** Besides OTP group 6, which stores value of register VCOMS[7:0], can be reprogrammed 5 times in each OTP table **(the information is stored in register VCOM_FLAG[4:0])** ; the other OTP groups **(group 1h ~ 5h and group 7h ~ Dh & 19h~1Ah)** can be programmed one time in each OTP table. The OTP programming time for each group **($T_{PROGRAM}$)** is different, and please refer to table 6.4.

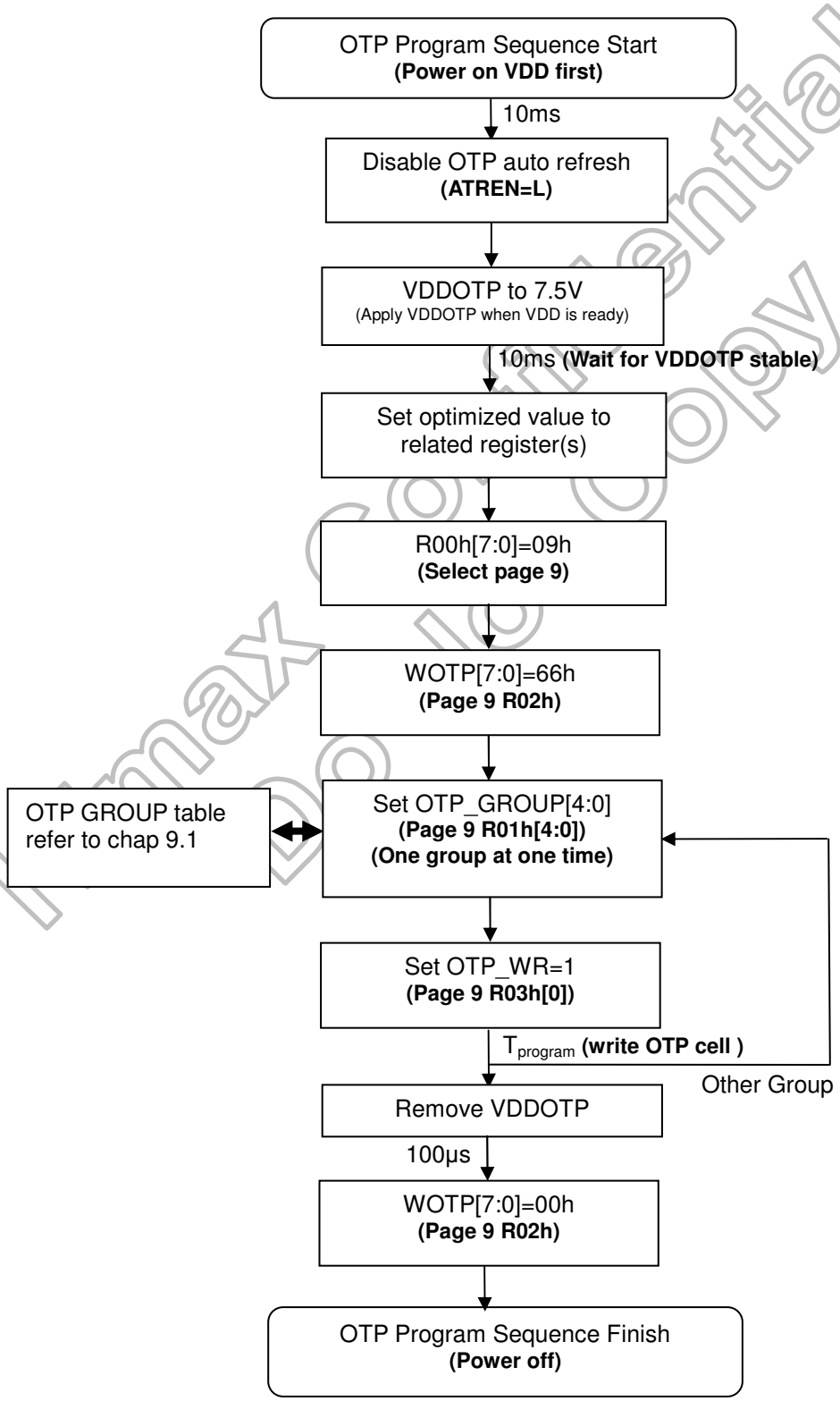
Group (Hex)	$T_{PROGRAM}$ (ms)
1	1.5
2	1.5
3	4.5
4	3.5
5	6
6	1
7	2.5
8	20
9	15.5
A	15.5
B	15.5
C	5
D	1.5
19	1
1A	2.5

Note: (1) It is forbidden to apply VDDOTP before VDD.

Table 6.4: OTP program time

6.10.1 First time OTP program sequence

The first time programming OTP function **(OTP table 1 is programmed)**, the initial value should be written by following steps.

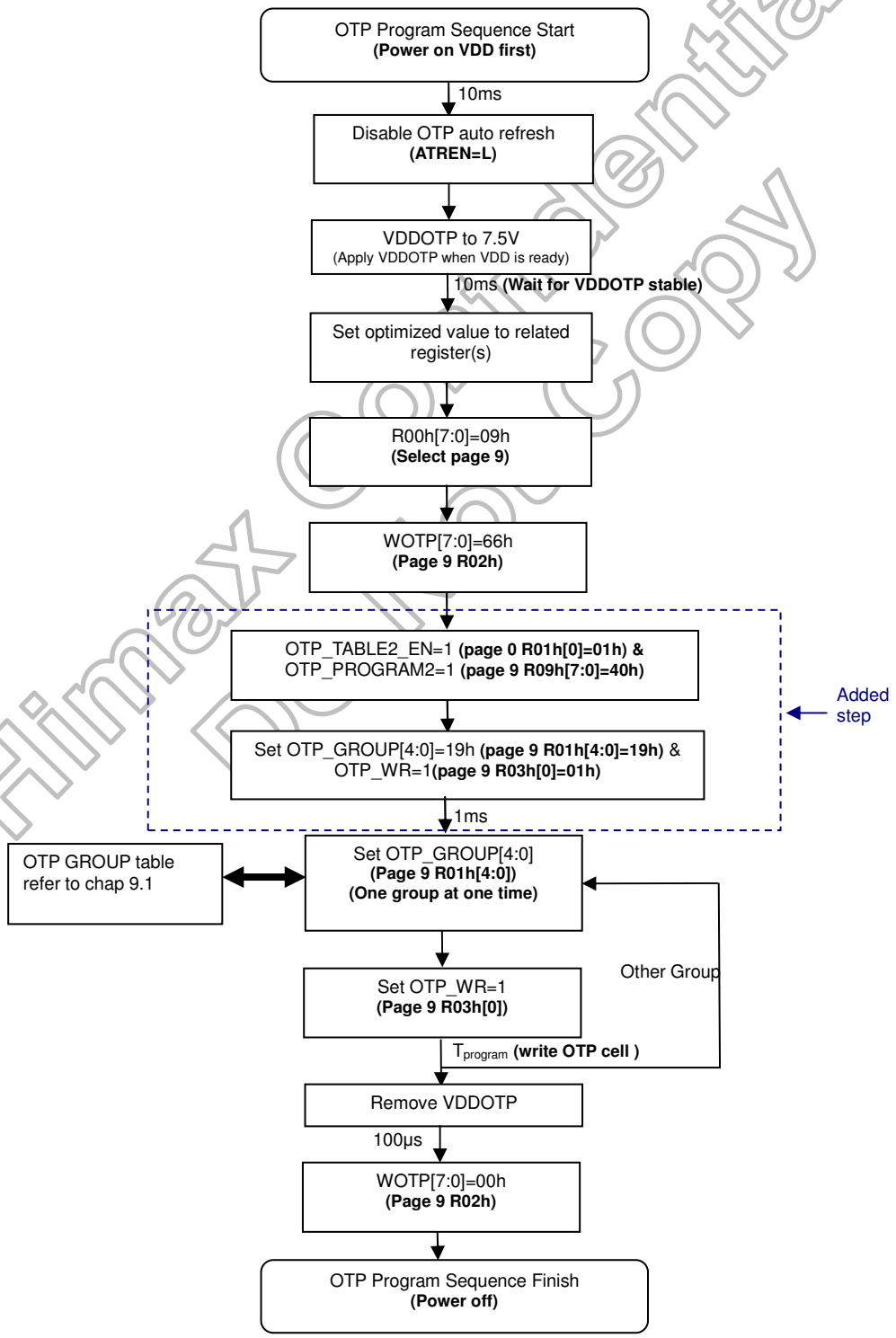


Note: (1) The whole OTP program sequence **(VDDOTP connected to 7.5V)** should finish in 60 seconds.

Figure 6.18: OTP 1st program sequence (OTP table1)

6.10.2 Second time OTP program sequence

For the Second time OTP programming function **(OTP table 2 is programmed)**, the flow is similar OTP table1 programming with the difference that OTP_PROGRAM2 bit **(page 9, R09h[6])** should be set to 1 before programming OTP table2 and OTP_TABLE2_EN bit **(page 0, R01h[0], OTP group 19h)** should be programmed to 1 for OTP just reload table2 when ATREN=H.



Note: (1) The whole OTP program sequence **(VDDOTP connected to 7.5V)** should finish in 60 seconds.

Figure 6.19: OTP 2nd program sequence (OTP table2)

6.10.3 OTP marginal read

OTP marginal reload provides a critical read condition to filter out “weak programmed” bits. To cover all worse corners, it should be implemented after programming OTP.

Example: Suppose OTP group 6h for VCOMS[7:0] is programmed to be AAh. Default value is 80h.

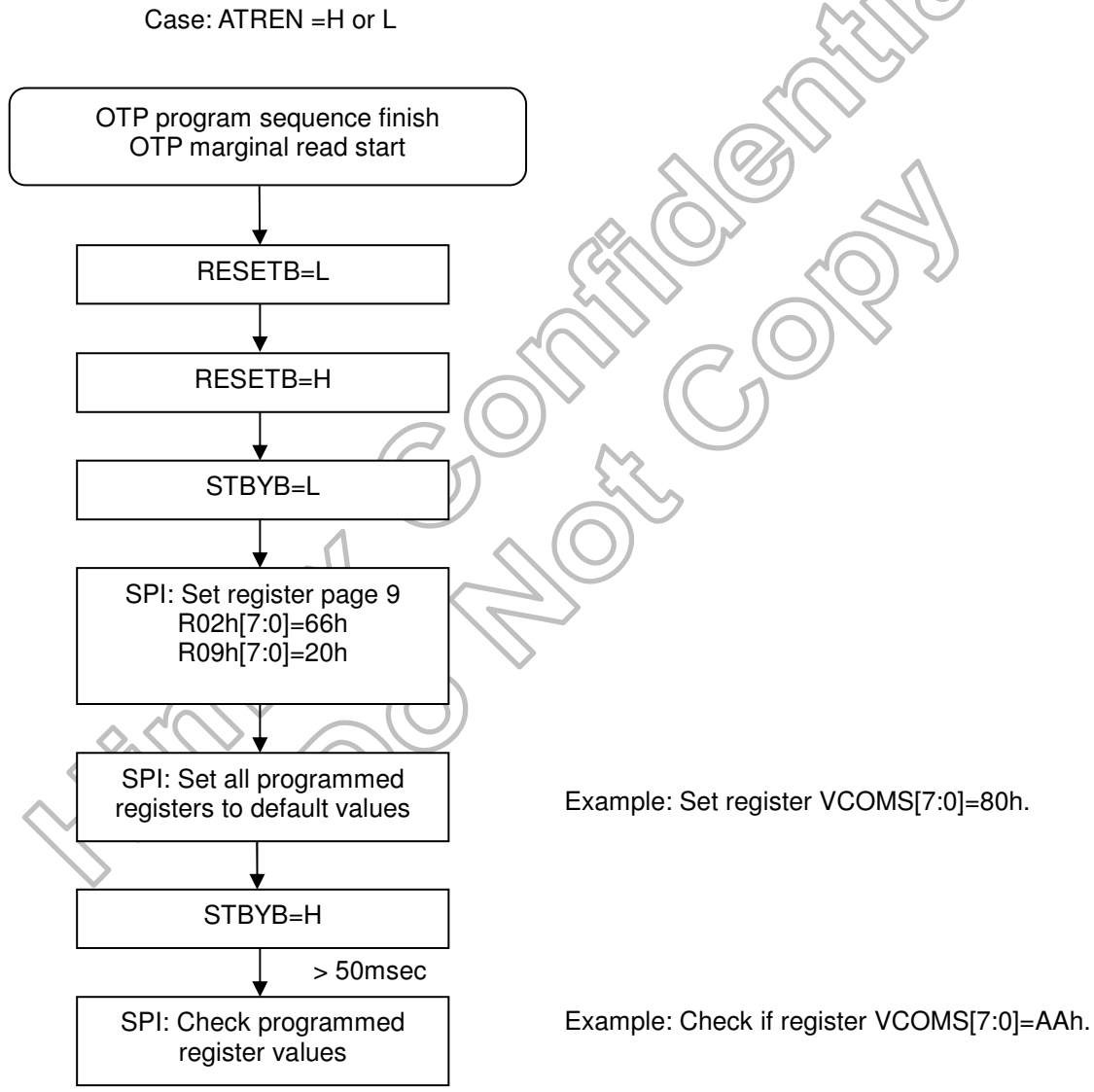


Figure 6.20: OTP marginal read sequence

7. Input/Output Timing

7.1 Input signal timing

7.1.1 TTL interface

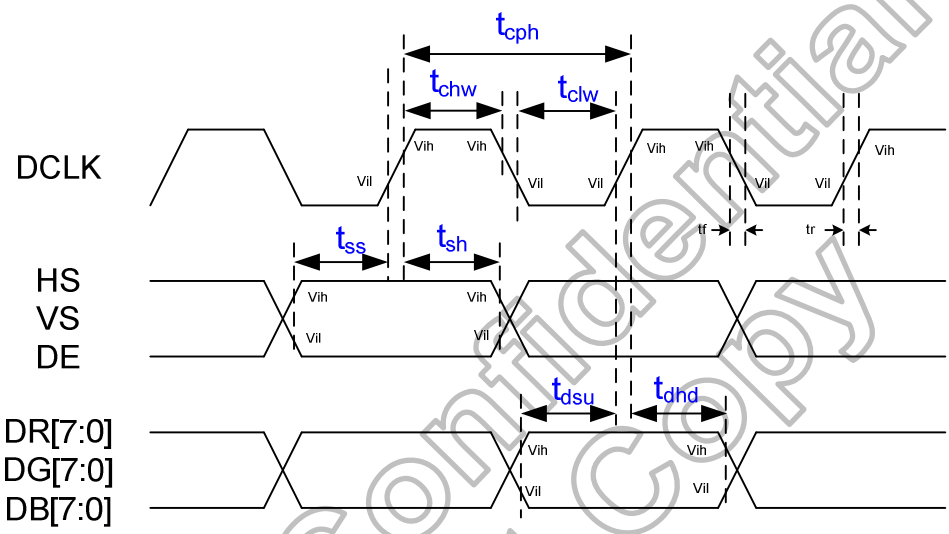


Figure 7.1: TTL input timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK period	T_{cph}	16.8	-	-	ns
DCLK clock high width	T_{chw}	6	-	-	ns
DCLK clock low width	T_{clw}	6	-	-	ns
VS setup time	T_{ss}	5	-	-	ns
VS hold time	T_{sh}	5	-	-	ns
HS setup time	T_{ss}	5	-	-	ns
HS hold time	T_{sh}	5	-	-	ns
DE setup time	T_{ss}	5	-	-	ns
DE hold time	T_{sh}	5	-	-	ns
Data setup time	T_{dsu}	5			ns
Data hold time	T_{dhd}	5			ns
Input signal rising time	Tr	-	-	10	ns
Input signal falling time	Tf	-	-	10	ns

Table 7.1: TTL input timing parameters

7.1.2 LVDS interface

LVDS input timing is described as below.

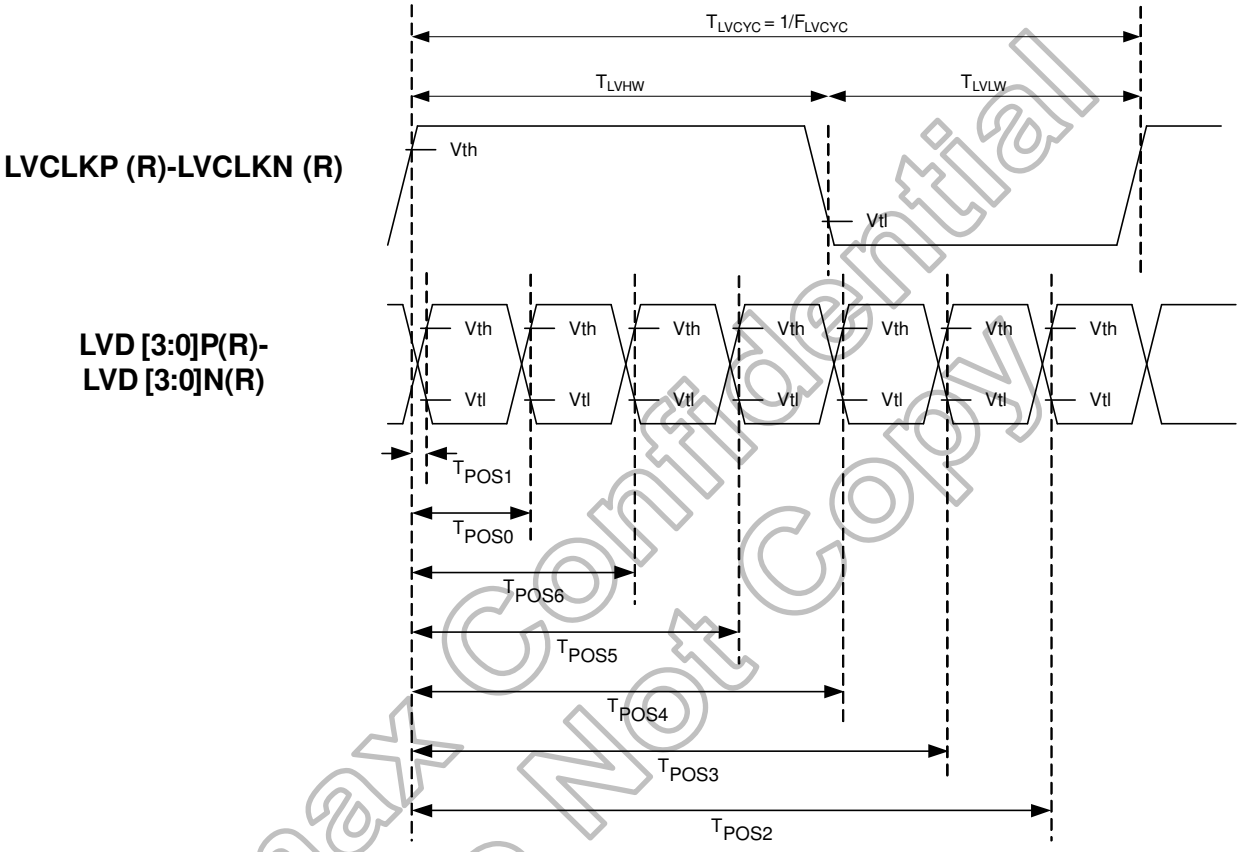


Figure 7.2: LVDS input timing

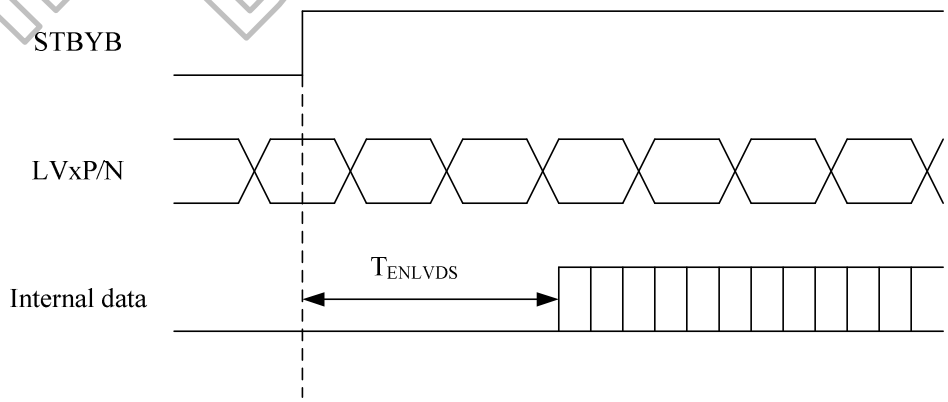
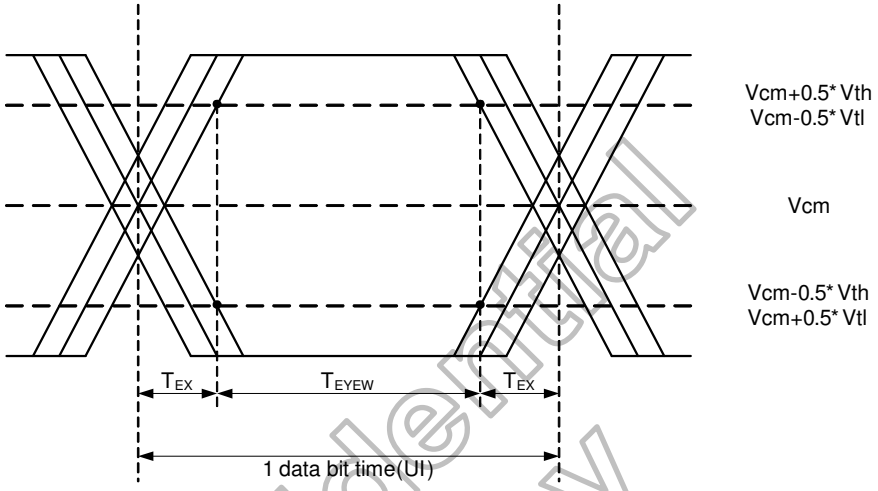


Figure 7.3: LVDS wake up time

Single-ended:
LVD [3:0]P,
LVD [3:0]N



Differential:
LVD [3:0]P-LVD [3:0]N

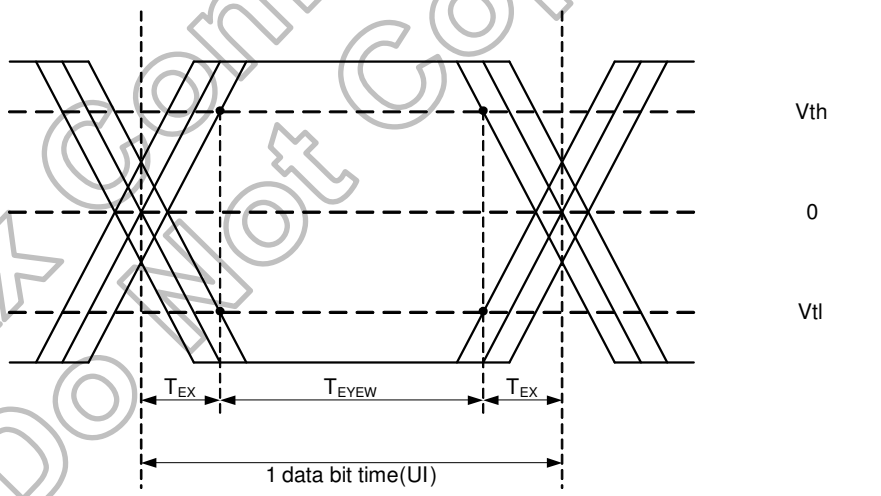


Figure 7.4: LVDS input eye diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	FLVCYC	10	-	85	MHz
Clock period	TLVCYC	11.76	-	100	nsec
1 data bit time	UI	-	1/7	-	TLVCYC
Clock high time	LVHW	2.9	4	4.1	UI
Clock low time	LVLW	2.9	3	4.1	UI
Position 1	TPOS1	-0.2	0	0.2	UI
Position 0	TPOS0	0.8	1	1.2	UI
Position 6	TPOS6	1.8	2	2.2	UI
Position 5	TPOS5	2.8	3	3.2	UI
Position 4	TPOS4	3.8	4	4.2	UI
Position 3	TPOS3	4.8	5	5.2	UI
Position 2	TPOS2	5.8	6	6.2	UI
Input eye width	TEYEW	0.6	-	-	UI
Input eye border	TEX	-	-	0.2	UI
LVDS wake up time	TENLVDS	-	-	150	μs

Table 7.2: LVDS input timing parameters

7.1.3 LVDS with SSC

The LVDS receiver can support spread spectrum clock **(SSC)** .Limitation is listed as below. Note that modulation frequency is proportional to LVDS clock frequency.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Modulation frequency	SSC_{MF}	LVDS clock frequency centered at 80MHz.	-	-	200	KHz
		LVDS clock frequency centered at 60MHz.	-	-	150	KHz
		LVDS clock frequency centered at 40MHz.	-	-	100	KHz
		LVDS clock frequency centered at 20MHz.	-	-	50	KHz
Modulation rate	SSC_{MR}	LVDS clock frequency + SSC_{MR} is in the range of 10~85MHz.	-	-	±5	%

Table 7.3: SSC limitation of LVDS interface

7.1.4 Reset timing

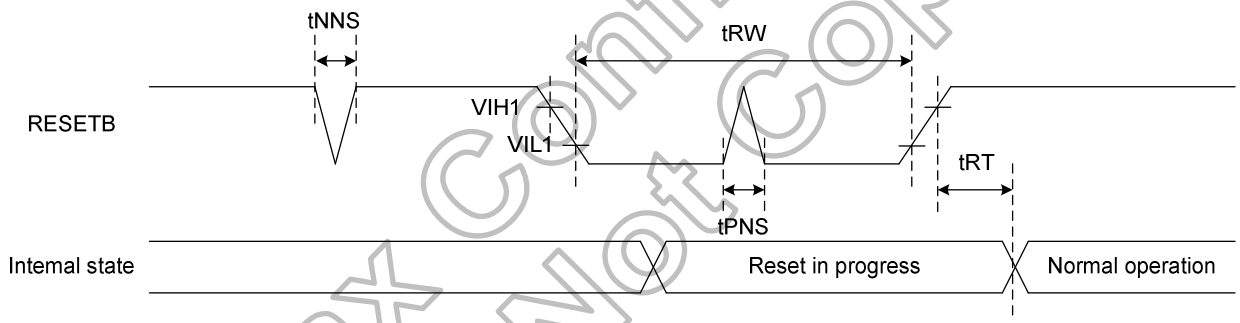


Figure 7.5: Reset timing

(VDD1=VDD2=2.7 to 3.6V, GND=0V, T_A=-40 to +95 ℃)

Signal	Paramete	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	tRW	10	-	-	μs
	Reset complete time	tRT	-	-	5	μs
	Positive spike noise width	tPNS	-	-	100	ns
	Negative spike noise width	tNNS	-	-	100	ns

Table 7.4: Reset timing parameters

7.1.5 SPI timing

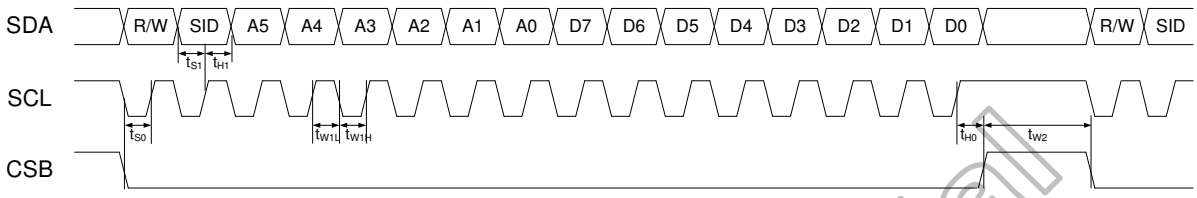


Figure 7.6: SPI signal timing

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
SDA setup time	t_{S0}	CSB to SCL	60	-	-	ns
	t_{S1}	SDA to SCL	60	-	-	ns
SDA hold time	t_{H0}	CSB to SCL	60	-	-	ns
	t_{H1}	SDA to SCL	60	-	-	ns
Pulse width	t_{W1L}	SCL pulse width	75	-	-	ns
	t_{W1H}	SCL pulse width	75	-	-	ns
	t_{W2}	CSB pulse width	1	-	-	µs
Clock duty	-	-	40	50	60	%

Table 7.5: SPI timing parameters

7.2 TTL Input timing

7.2.1 Parallel RGB at Sync mode

- Horizontal

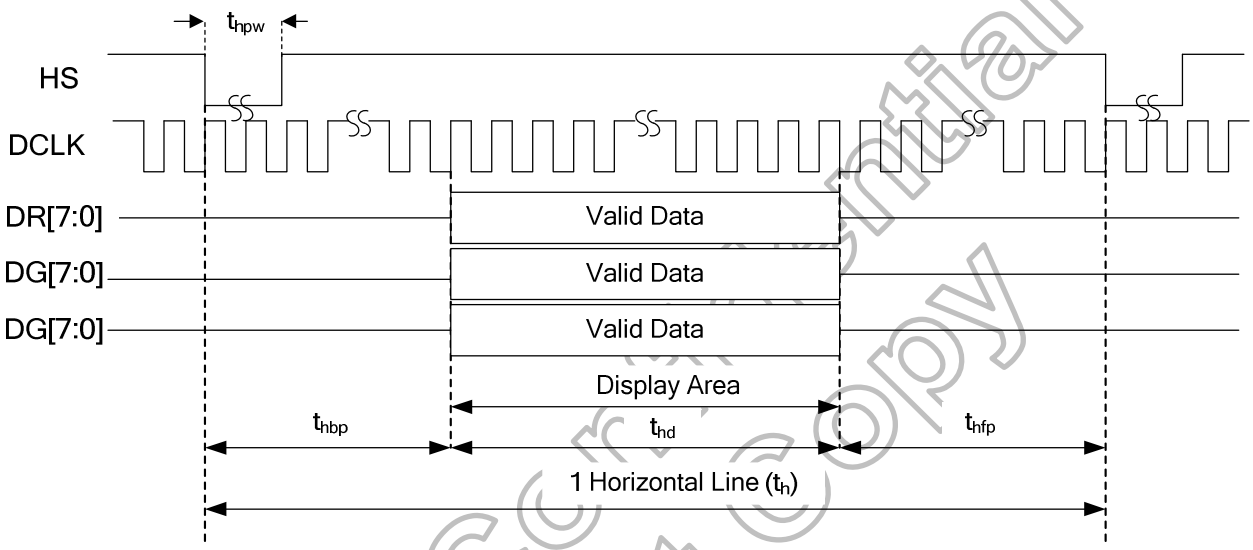


Figure 7.7: Horizontal input timing at Sync mode

- Vertical

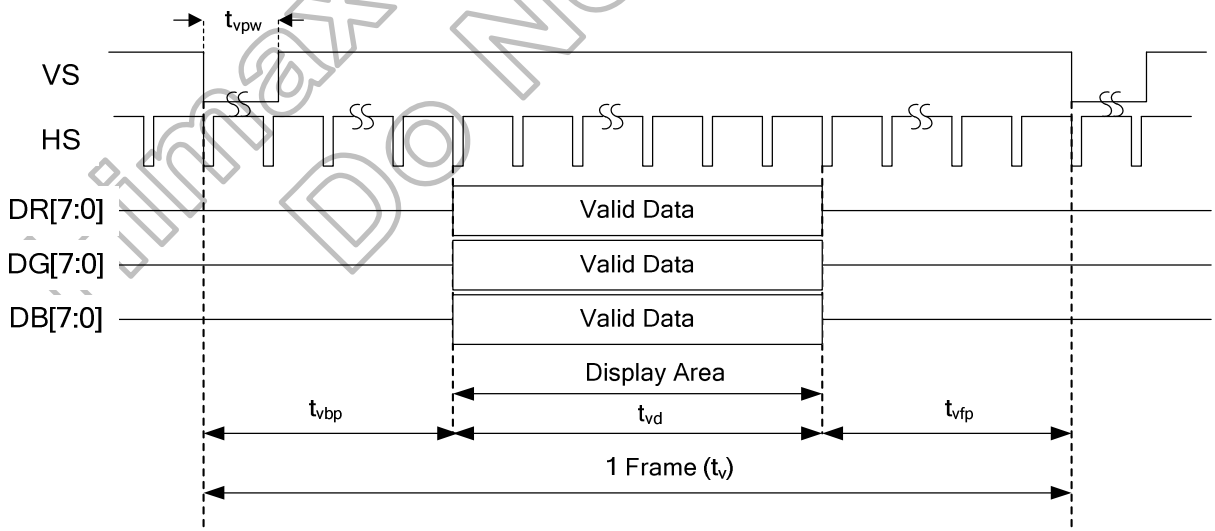


Figure 7.8: Vertical input timing at Sync mode

Parameter	Symbol	Panel resolution									Unit
		600xRGBx1024 (RS[3:0]=0h)			720xRGBx480 (RS[3:0]=1h			720xRGBx1280 (RS[3:0]=0x2h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	40.7	42.6	46.6	22.8	24.7	28.6	60.1	62.9	69.9	MHz
Horizontal valid data	t_{hd}		600			720			720		DCLK
Hsync pulse width	t_{hpw}	1	2	70	1	2	88	1	2	88	DCLK
Hsync back porch	t_{hbp}	5	16	71	5	16	89	5	16	89	DCLK
Hsync front porch	t_{hfp}	19	44	85	19	64	103	19	64	103	DCLK
1 horizontal line	t_h	656	660	690	776	780	828	776	780	828	DCLK
Vertical valid data	t_{vd}		1024			480			1280		H
Vsync pulse width	t_{vpw}	1	2	96	1	2	90	1	2	122	H
Vsync back porch	t_{vbp}	5	5	97	5	5	91	5	5	123	H
Vsync front porch	t_{vfp}	5	46	97	5	43	91	5	59	123	H
1 vertical field	t_v	1034	1075	1126	490	528	576	1290	1344	1408	H

Parameter	Symbol	Panel resolution									Unit
		768xRGBx1024 (RS[3:0]=3h)			768xRGBx1280 (RS[3:0]=4h)			768xRGBx1366 (RS[3:0]=5h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	51.1	53.4	59.7	63.8	66.8	74.6	68.0	71.2	79.6	MHz
Horizontal valid data	t_{hd}		768			768			768		DCLK
Hsync pulse width	t_{hpw}	1	2	95	1	2	95	1	2	95	DCLK
Hsync back porch	t_{hbp}	5	16	96	5	16	96	5	16	96	DCLK
Hsync front porch	t_{hfp}	19	44	110	19	44	110	19	44	110	DCLK
1 horizontal line	t_h	824	828	883	824	828	883	824	828	883	DCLK
Vertical valid data	t_{vd}		1024			1280			1366		H
Vsync pulse width	t_{vpw}	1	2	96	1	2	122	1	2	130	H
Vsync back porch	t_{vbp}	5	5	97	5	5	123	5	5	131	H
Vsync front porch	t_{vfp}	5	46	97	5	59	123	5	63	131	H
1 vertical field	t_v	1034	1075	1126	1290	1344	1408	1376	1434	1502	H

Parameter	Symbol	Panel resolution									Unit
		800xRGBx480 (RS[3:0]=6h)			800xRGBx1280 (RS[3:0]=7h)			960xRGBx160 (RS[3:0]=8h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	25.2	27.2	30.5	66.3	69.4	77.7	10.4	11.8	14.8	MHz
Horizontal valid data	t_{hd}		800			800			960		DCLK
Hsync pulse width	t_{hpw}	1	2	100	1	2	100	1	2	124	DCLK
Hsync back porch	t_{hbp}	5	16	101	5	16	101	5	16	125	DCLK
Hsync front porch	t_{hfp}	19	44	115	19	44	115	19	44	139	DCLK
1 horizontal line	t_h	856	860	920	856	860	920	1016	1020	1104	DCLK
Vertical valid data	t_{vd}		480			1280			160		H
Vsync pulse width	t_{vpw}	1	2	66	1	2	122	1	2	58	H
Vsync back porch	t_{vbp}	5	5	67	5	5	123	5	5	59	H
Vsync front porch	t_{vfp}	5	43	67	5	59	123	5	27	59	H
1 vertical field	t_v	490	528	552	1290	1344	1408	170	192	224	H

Parameter	Symbol	Panel Resolution									Unit
		1024xRGBx600 (RS[3:0]=9h)			1280xRGBx720 (RS[3:0]=Ah)			1440xRGBx540 (RS[3:0]=Bh)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	39.5	42.9	50.8	58.5	63.7	76.3	49.4	53.5	61.7	MHz
Horizontal valid data	t_{hd}		1024			1280			1440		DCLK
Hsync pulse width	t_{hpw}	1	2	133	1	2	172	1	2	196	DCLK
Hsync back porch	t_{hbp}	5	16	134	5	16	173	5	16	197	DCLK
Hsync front porch	t_{hfp}	19	44	148	19	44	187	19	44	211	DCLK
1 horizontal line	t_h	1080	1084	1177	1336	1340	1472	1496	1500	1656	DCLK
Vertical valid data	t_{vd}		600			720			540		H
Vsync pulse width	t_{vpw}	1	2	114	1	2	138	1	2	75	H
Vsync back porch	t_{vbp}	5	5	115	5	5	139	5	5	76	H
Vsync front porch	t_{vfp}	5	55	115	5	67	139	5	49	76	H
1 vertical field	t_v	610	660	720	730	792	864	550	594	621	H

Parameter	Symbol	Panel Resolution									Unit
		1600xRGBx720 (RS[3:0]=Ch)			640xRGBx480 (RS[3:0]=Dh)			-			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	72.5	78.9	91.2	20.5	22.2	25.4	-	-	-	MHz
Horizontal valid data	t_{hd}		1600			640			-		DCLK
Hsync pulse width	t_{hpw}	1	2	140	1	2	76	-	-	-	DCLK
Hsync back porch	t_{hbp}	5	16	141	5	16	77	-	-	-	DCLK
Hsync front porch	t_{hfp}	19	44	155	19	44	91	-	-	-	DCLK
1 horizontal line	t_h	1656	1660	1760	696	700	736	-	-	-	DCLK
Vertical valid data	t_{vd}		720			480			-		H
Vsync pulse width	t_{vpw}	1	2	138	1	2	90	-	-	-	H
Vsync back porch	t_{vbp}	5	5	139	5	5	91	-	-	-	H
Vsync front porch	t_{vfp}	5	67	139	5	43	91	-	-	-	H
1 vertical field	t_v	730	792	864	490	528	576	-	-	-	H

Note: (1) thd is same to Hactive, and tvd is same to Vactive in chapter 5.1.
(2) DCLK frequency min/max value is base on frame rate 60 Hz.
(3) thbp+thpw+thfp≧56 DCLK, tvbp+tvpw+tvfp≧10.

7.2.2 Parallel RGB at DE mode

- **Horizontal**

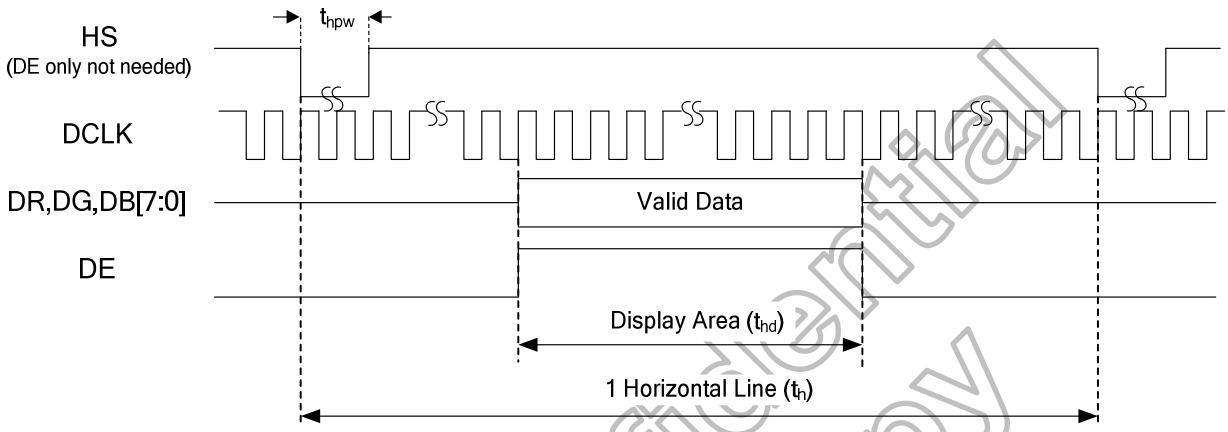


Figure 7.9: Horizontal input timing at DE only mode

- Vertical

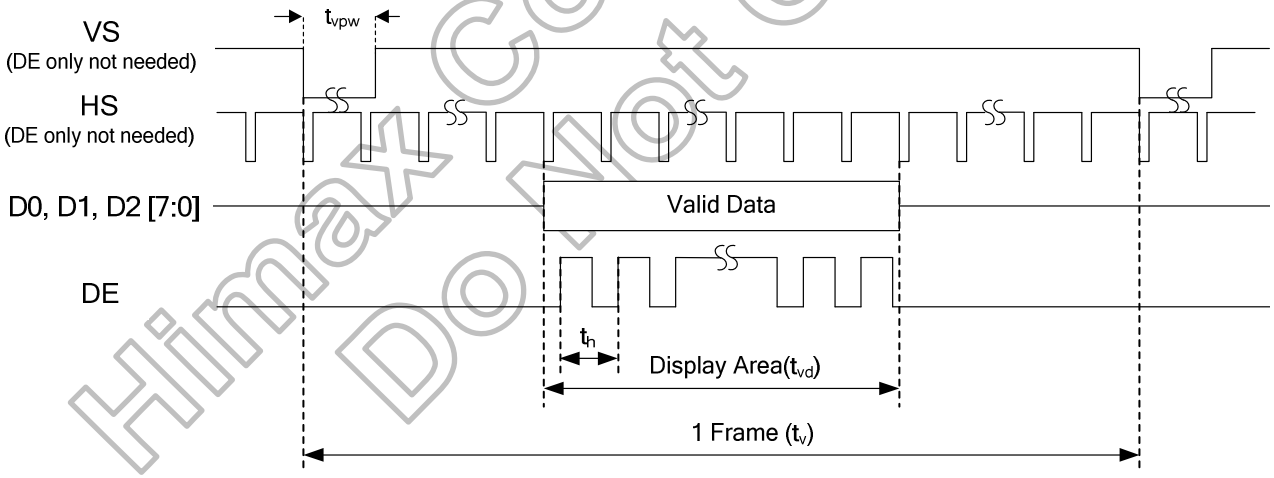


Figure 7.10: Vertical input timing at DE only mode

Parameter	Symbol	Panel Resolution									Unit
		600xRGBx1024 (RS[3:0]=0h)			720xRGBx480 (RS[3:0]=1h)			720xRGBx1280 (RS[3:0]=2h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	40.7	42.6	46.6	22.8	24.7	28.6	60.1	62.9	69.9	MHz
Horizontal valid data	t_{hd}		600			720			720		
1 horizontal line	t_h	656	660	690	776	780	828	776	780	828	DCLK
Vertical valid data	t_{vd}		1024			480			1280		
1 vertical field	t_v	1034	1075	1224	490	528	576	1290	1344	1536	H

Parameter	Symbol	Panel Resolution									Unit
		768xRGBx1024 (RS[3:0]=3h)			768xRGBx1280 (RS[3:0]=4h)			768xRGBx1366 (RS[3:0]=5h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	51.1	53.4	59.7	63.8	66.8	74.6	68.0	71.2	79.6	MHz
Horizontal valid data	t_{hd}		768			768			768		
1 horizontal line	t_h	824	828	883	824	828	883	824	828	883	DCLK
Vertical valid data	t_{vd}		1024			1280			1366		
1 vertical field	t_v	1034	1075	1224	1290	1344	1536	1376	1434	1639	H

Parameter	Symbol	Panel Resolution									Unit
		800xRGBx480 (RS[3:0]=6h)			800xRGBx1280 (RS[3:0]=7h)			960xRGBx160 (RS[3:0]=8h)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	25.2	27.2	30.5	66.3	69.4	77.7	10.4	11.8	14.8	MHz
Horizontal valid data	t_{hd}		800			800			960		
1 horizontal line	t_h	856	860	920	856	860	920	1016	1020	1104	DCLK
Vertical valid data	t_{vd}		480			1280			160		
1 vertical field	t_v	490	528	552	1290	1344	1536	170	192	224	H

Parameter	Symbol	Panel Resolution									Unit
		1024xRGBx600 (RS[3:0]=9h)			1280xRGBx720 (RS[3:0]=Ah)			1440xRGBx540 (RS[3:0]=Bh)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	39.5	42.9	50.8	58.5	63.7	76.3	49.4	53.5	61.7	MHz
Horizontal valid data	t_{hd}		1024			1280			1440		
1 horizontal line	t_h	1080	1084	1177	1336	1340	1472	1496	1500	1656	DCLK
Vertical valid data	t_{vd}		600			720			540		
1 vertical field	t_v	610	660	720	730	792	864	550	594	648	H

Parameter	Symbol	Panel Resolution									Unit
		1600xRGBx720 (RS[3:0]=Ch)			640xRGBx480 (RS[3:0]=Dh)						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	72.5	78.9	91.2	20.5	22.2	25.4	-	-	-	MHz
Horizontal valid data	t_{hd}		1600			640			-		
1 horizontal line	t_h	1656	1660	1760	696	700	736	-	-	-	DCLK
Vertical valid data	t_{vd}		720			480			-		
1 vertical field	t_v	730	792	864	490	528	576	-	-	-	H

Note: (1) thd is same to Hactive, and tvd is same to Vactive in chapter 5.1.
(2) DCLK Frequency min/max value is base on frame rate 60 Hz.

8. Gamma Description

8.1 Gamma circuit

For positive polarity, three voltages VGMPH/M/LO are generated as gamma reference, where VGMPMO is equal to 0.5*(VGMPHO+VGMPLO).Theyare connected to VGMPH/M/LI and used to generate all gamma reference voltages GSH0/1/6/11/28/35/47/67/87/107/147/163/187/211/225/233/241/252/255, and all grayscale voltages are GSH[0:255].

For negative polarity, the structure is exactly the same to positive gamma circuit.

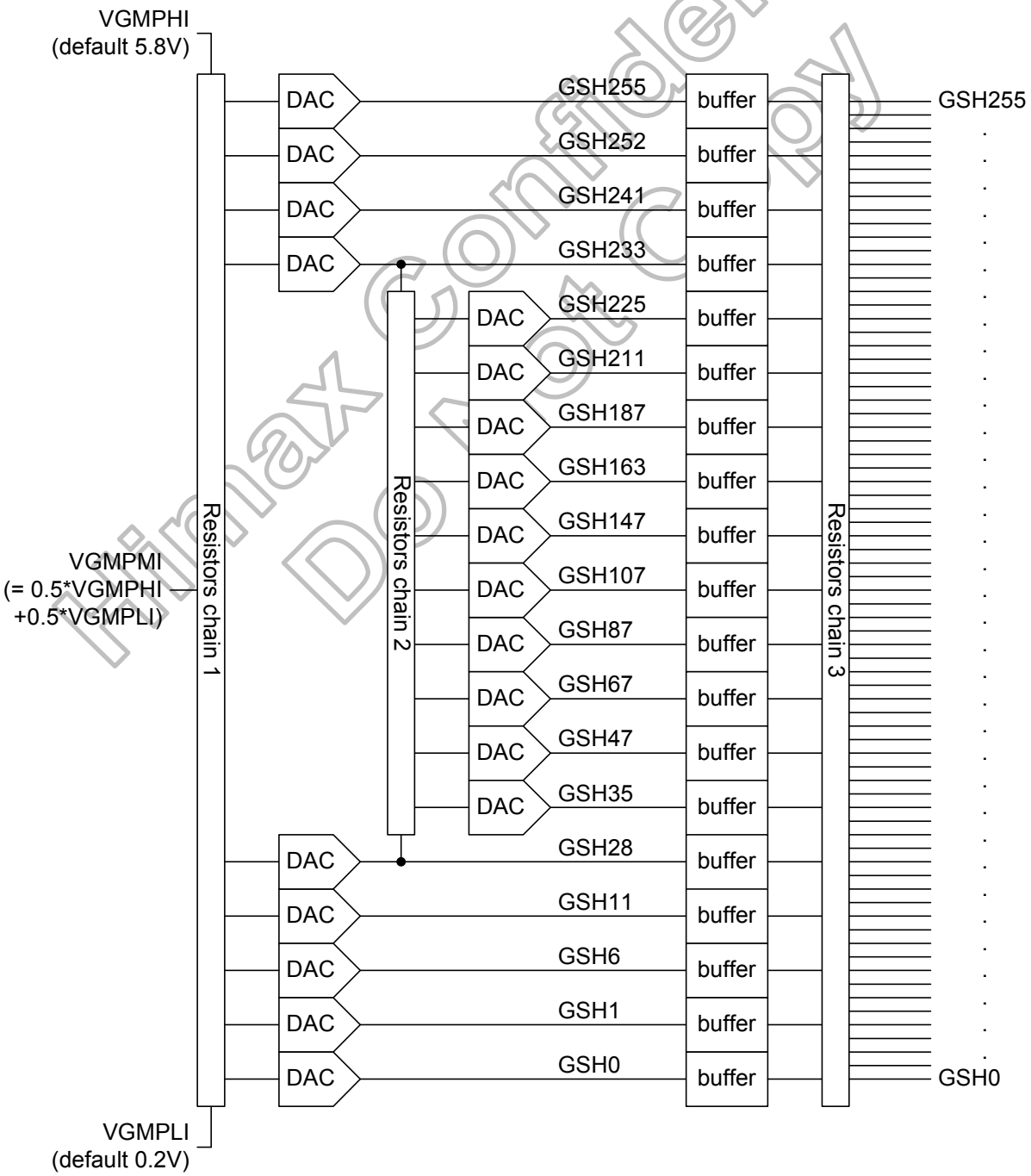


Figure 8.1: Positive gamma circuit

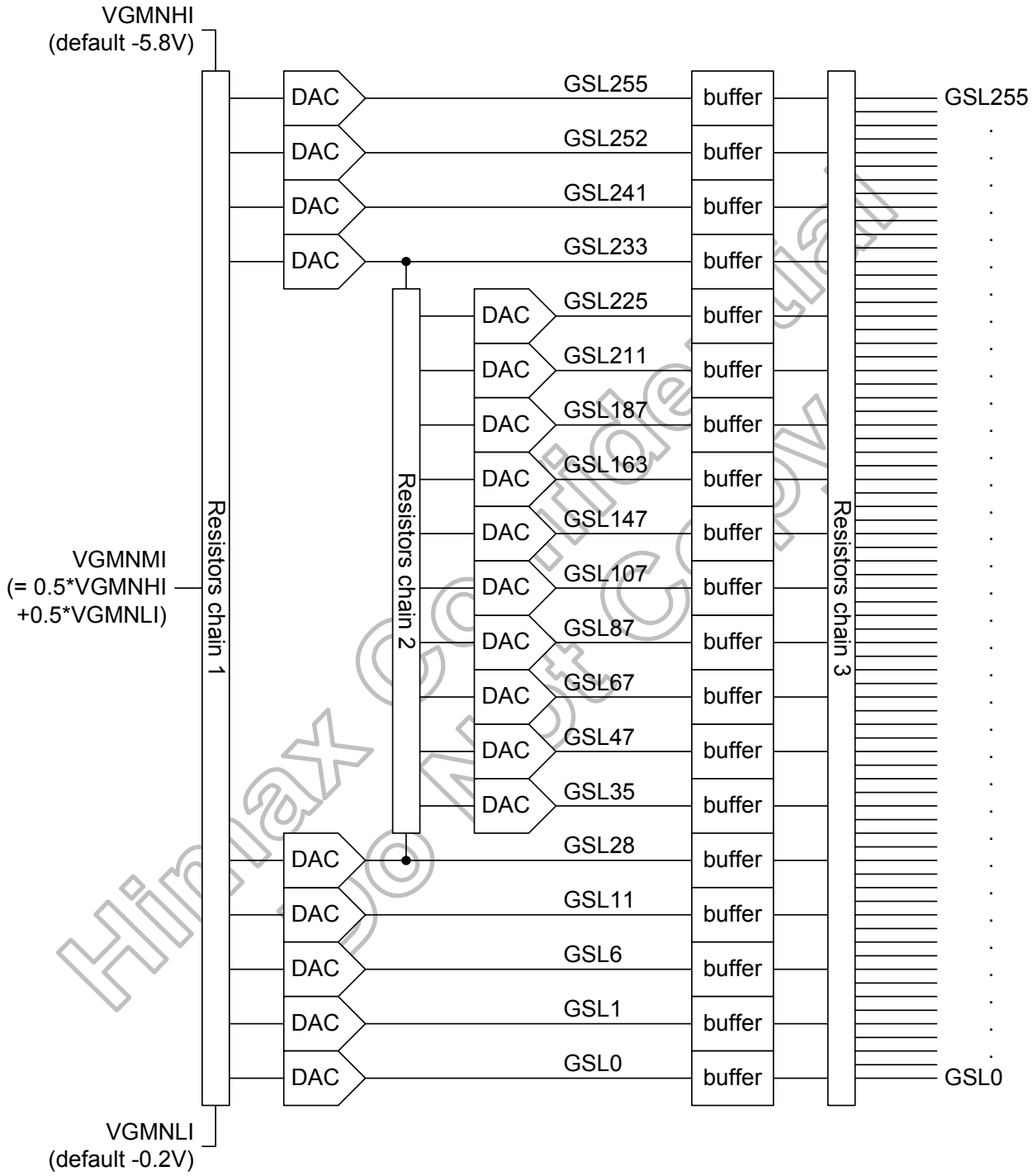


Figure 8.2: Negative gamma circuit

8.2 Equation for gamma code

The reference voltages can be set by page 1 registers, as described in the following table.

Settings for positive gamma voltage

Gamma code	Register	Reference voltage	Register range
GSH0	VP0_[2:0]	VGMPL + (1/256)*(VP0_[2:0])*(VGMPH - VGMPL)	0~7
GSH1	VP1_[3:0]	VGMPL + (1/128)*(VP1_[3:0] + 1)*(VGMPH - VGMPL)	0~15
GSH6	VP6_[5:0]	VGMPL + (1/256)*(VP6_[5:0] + 10)*(VGMPH - VGMPL)	0~53
GSH11	VP11_[5:0]	VGMPL + (1/256)*(VP11_[5:0] + 26)*(VGMPH - VGMPL)	0~53
GSH28	VP28_[6:0]	VGMPL + (1/512)*(VP28_[6:0] + 75)*(VGMPH - VGMPL)	0~127
GSH35	VP35_[3:0]	GSH28 + (1/250)*(VP35_[3:0] + 5)*(GSH233 - GSH28)	0~15
GSH47	VP47_[4:0]	GSH28 + (1/250)*(VP47_[4:0] + 15)*(GSH233 - GSH28)	0~31
GSH67	VP67_[5:0]	GSH28 + (1/250)*(VP67_[5:0] + 30)*(GSH233 - GSH28)	0~47
GSH87	VP87_[5:0]	GSH28 + (1/250)*(VP87_[5:0] + 45)*(GSH233 - GSH28)	0~47
GSH107	VP107_[5:0]	GSH28 + (1/250)*(VP107_[5:0] + 60)*(GSH233 - GSH28)	0~47
GSH147	VP147_[5:0]	GSH28 + (1/250)*(VP147_[5:0] + 90)*(GSH233 - GSH28)	0~47
GSH163	VP163_[5:0]	GSH28 + (1/250)*(VP163_[5:0] + 105)*(GSH233 - GSH28)	0~47
GSH187	VP187_[5:0]	GSH28 + (1/250)*(VP187_[5:0] + 132)*(GSH233 - GSH28)	0~47
GSH211	VP211_[5:0]	GSH28 + (1/250)*(VP211_[5:0] + 175)*(GSH233 - GSH28)	0~47
GSH225	VP225_[4:0]	GSH28 + (1/250)*(VP225_[4:0] + 215)*(GSH233 - GSH28)	0~31
GSH233	VP233_[6:0]	VGMPL + (1/512)*(VP233_[6:0] + 340)*(VGMPH - VGMPL)	0~103
GSH241	VP241_[4:0]	VGMPL + (1/256)*(VP241_[4:0] + 200)*(VGMPH - VGMPL)	0~31
GSH252	VP252_[3:0]	VGMPL + (1/256)*(VP252_[3:0] + 235)*(VGMPH - VGMPL)	0~15
GSH255	VP255_[3:0]	VGMPL + (1/256)*(VP255_[3:0] + 241)*(VGMPH - VGMPL)	0~15

Settings for negative gamma voltage

Gamma code	Register	Reference voltage	Register range
GSL0	VN0_[2:0]	VGMNL + (1/256)*(VN0_[2:0])*(VGMNH - VGMNL)	0~7
GSL1	VN1_[3:0]	VGMNL + (1/128)*(VN1_[3:0] + 1)*(VGMNH - VGMNL)	0~15
GSL6	VN6_[5:0]	VGMNL + (1/256)*(VN6_[5:0] + 10)*(VGMNH - VGMNL)	0~53
GSL11	VN11_[5:0]	VGMNL + (1/256)*(VN11_[5:0] + 26)*(VGMNH - VGMNL)	0~53
GSL28	VN28_[6:0]	VGMNL + (1/512)*(VN28_[6:0] + 75)*(VGMNH - VGMNL)	0~127
GSL35	VN35_[3:0]	GSL28 + (1/250)*(VN35_[3:0] + 5)*(GSL233 - GSL28)	0~15
GSL47	VN47_[4:0]	GSL28 + (1/250)*(VN47_[4:0] + 15)*(GSL233 - GSL28)	0~31
GSL67	VN67_[5:0]	GSL28 + (1/250)*(VN67_[5:0] + 30)*(GSL233 - GSL28)	0~47
GSL87	VN87_[5:0]	GSL28 + (1/250)*(VN87_[5:0] + 45)*(GSL233 - GSL28)	0~47
GSL107	VN107_[5:0]	GSL28 + (1/250)*(VN107_[5:0] + 60)*(GSL233 - GSL28)	0~47
GSL147	VN147_[5:0]	GSL28 + (1/250)*(VN147_[5:0] + 90)*(GSL233 - GSL28)	0~47
GSL163	VN163_[5:0]	GSL28 + (1/250)*(VN163_[5:0] + 105)*(GSL233 - GSL28)	0~47
GSL187	VN187_[5:0]	GSL28 + (1/250)*(VN187_[5:0] + 132)*(GSL233 - GSL28)	0~47
GSL211	VN211_[5:0]	GSL28 + (1/250)*(VN211_[5:0] + 175)*(GSL233 - GSL28)	0~47
GSL225	VN225_[4:0]	GSL28 + (1/250)*(VL225_[4:0] + 215)*(GSL233 - GSL28)	0~31
GSL233	VN233_[6:0]	VGMNL + (1/512)*(VN233_[6:0] + 340)*(VGMNH - VGMNL)	0~103
GSL241	VN241_[4:0]	VGMNL + (1/256)*(VN241_[4:0] + 200)*(VGMNH - VGMNL)	0~31
GSL252	VN252_[3:0]	VGMNL + (1/256)*(VN252_[3:0] + 235)*(VGMNH - VGMNL)	0~15
GSL255	VN255_[3:0]	VGMNL + (1/256)*(VN255_[3:0] + 241)*(VGMNH - VGMNL)	0~15

8.3 Resistor ratio for gamma code

Resistor ratio in the resistor chain 3 of both positive and negative gamma circuits is described in the following table. The resistor RGMA[k] is between GSH[k] and GSH[k-1], or GSL[k] and GSL[k-1].

Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[255]	6.5R	RGMA[223]	2.25R	RGMA[191]	1.5R	RGMA[159]	1.125R
RGMA[254]	6.5R	RGMA[222]	2.25R	RGMA[190]	1.5R	RGMA[158]	1.125R
RGMA[253]	5.5R	RGMA[221]	2.25R	RGMA[189]	1.5R	RGMA[157]	1.125R
RGMA[252]	5.5R	RGMA[220]	2.25R	RGMA[188]	1.3333R	RGMA[156]	1.125R
RGMA[251]	5.5R	RGMA[219]	2.2R	RGMA[187]	1.3333R	RGMA[155]	1.125R
RGMA[250]	5.5R	RGMA[218]	2.2R	RGMA[186]	1.3333R	RGMA[154]	1.125R
RGMA[249]	5.5R	RGMA[217]	2.2R	RGMA[185]	1.3333R	RGMA[153]	1.125R
RGMA[248]	4.5R	RGMA[216]	2.2R	RGMA[184]	1.3333R	RGMA[152]	1.125R
RGMA[247]	4.5R	RGMA[215]	2R	RGMA[183]	1.3333R	RGMA[151]	1R
RGMA[246]	4.25R	RGMA[214]	2R	RGMA[182]	1.3333R	RGMA[150]	1R
RGMA[245]	4.25R	RGMA[213]	2R	RGMA[181]	1.3333R	RGMA[149]	1R
RGMA[244]	4.125R	RGMA[212]	1.8333R	RGMA[180]	1.3333R	RGMA[148]	1R
RGMA[243]	4.125R	RGMA[211]	1.8333R	RGMA[179]	1.3333R	RGMA[147]	1R
RGMA[242]	3.5R	RGMA[210]	1.8333R	RGMA[178]	1.25R	RGMA[146]	1R
RGMA[241]	3.5R	RGMA[209]	1.8333R	RGMA[177]	1.25R	RGMA[145]	1R
RGMA[240]	3.5R	RGMA[208]	1.75R	RGMA[176]	1.25R	RGMA[144]	1R
RGMA[239]	3.5R	RGMA[207]	1.75R	RGMA[175]	1.25R	RGMA[143]	1R
RGMA[238]	2.8333R	RGMA[206]	1.75R	RGMA[174]	1.25R	RGMA[142]	1R
RGMA[237]	2.8333R	RGMA[205]	1.75R	RGMA[173]	1.25R	RGMA[141]	1R
RGMA[236]	2.8333R	RGMA[204]	1.75R	RGMA[172]	1.25R	RGMA[140]	1R
RGMA[235]	2.8333R	RGMA[203]	1.75R	RGMA[171]	1.25R	RGMA[139]	1R
RGMA[234]	2.8333R	RGMA[202]	1.75R	RGMA[170]	1.25R	RGMA[138]	1R
RGMA[233]	2.75R	RGMA[201]	1.75R	RGMA[169]	1.25R	RGMA[137]	1R
RGMA[232]	2.75R	RGMA[200]	1.5R	RGMA[168]	1.25R	RGMA[136]	1R
RGMA[231]	2.75R	RGMA[199]	1.5R	RGMA[167]	1.25R	RGMA[135]	1R
RGMA[230]	2.5R	RGMA[198]	1.5R	RGMA[166]	1.25R	RGMA[134]	1R
RGMA[229]	2.5R	RGMA[197]	1.5R	RGMA[165]	1.25R	RGMA[133]	1R
RGMA[228]	2.5R	RGMA[196]	1.5R	RGMA[164]	1.25R	RGMA[132]	1R
RGMA[227]	2.5R	RGMA[195]	1.5R	RGMA[163]	1.25R	RGMA[131]	1R
RGMA[226]	2.5R	RGMA[194]	1.5R	RGMA[162]	1.25R	RGMA[130]	1R
RGMA[225]	2.5R	RGMA[193]	1.5R	RGMA[161]	1.125R	RGMA[129]	1R
RGMA[224]	2.25R	RGMA[192]	1.5R	RGMA[160]	1.125R	RGMA[128]	1R

Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[127]	1R	RGMA[95]	1R	RGMA[63]	1.3333R	RGMA[31]	2.75R
RGMA[126]	1R	RGMA[94]	1R	RGMA[62]	1.3333R	RGMA[30]	2.75R
RGMA[125]	1R	RGMA[93]	1R	RGMA[61]	1.3333R	RGMA[29]	2.75R
RGMA[124]	1R	RGMA[92]	1R	RGMA[60]	1.3333R	RGMA[28]	3R
RGMA[123]	1R	RGMA[91]	1R	RGMA[59]	1.3333R	RGMA[27]	3R
RGMA[122]	1R	RGMA[90]	1R	RGMA[58]	1.3333R	RGMA[26]	3.25R
RGMA[121]	1R	RGMA[89]	1R	RGMA[57]	1.3333R	RGMA[25]	3.25R
RGMA[120]	1R	RGMA[88]	1R	RGMA[56]	1.5R	RGMA[24]	3.5R
RGMA[119]	1R	RGMA[87]	1.125R	RGMA[55]	1.5R	RGMA[23]	3.5R
RGMA[118]	1R	RGMA[86]	1.125R	RGMA[54]	1.75R	RGMA[22]	3.5R
RGMA[117]	1R	RGMA[85]	1.125R	RGMA[53]	1.75R	RGMA[21]	4R
RGMA[116]	1R	RGMA[84]	1.125R	RGMA[52]	1.75R	RGMA[20]	4.25R
RGMA[115]	1R	RGMA[83]	1.125R	RGMA[51]	1.75R	RGMA[19]	4.33R
RGMA[114]	1R	RGMA[82]	1.125R	RGMA[50]	1.75R	RGMA[18]	4.33R
RGMA[113]	1R	RGMA[81]	1.125R	RGMA[49]	1.75R	RGMA[17]	4.33R
RGMA[112]	1R	RGMA[80]	1.125R	RGMA[48]	1.75R	RGMA[16]	5.5R
RGMA[111]	1R	RGMA[79]	1.125R	RGMA[47]	1.75R	RGMA[15]	5.5R
RGMA[110]	1R	RGMA[78]	1.125R	RGMA[46]	1.8333R	RGMA[14]	5.75R
RGMA[109]	1R	RGMA[77]	1.25R	RGMA[45]	1.8333R	RGMA[13]	5.75R
RGMA[108]	1R	RGMA[76]	1.25R	RGMA[44]	1.8333R	RGMA[12]	5.75R
RGMA[107]	1R	RGMA[75]	1.25R	RGMA[43]	1.8333R	RGMA[11]	6.5R
RGMA[106]	1R	RGMA[74]	1.25R	RGMA[42]	1.8333R	RGMA[10]	7R
RGMA[105]	1R	RGMA[73]	1.25R	RGMA[41]	1.8333R	RGMA[9]	7.75R
RGMA[104]	1R	RGMA[72]	1.25R	RGMA[40]	2R	RGMA[8]	8.25R
RGMA[103]	1R	RGMA[71]	1.25R	RGMA[39]	2R	RGMA[7]	9.25R
RGMA[102]	1R	RGMA[70]	1.25R	RGMA[38]	2.25R	RGMA[6]	9.8333R
RGMA[101]	1R	RGMA[69]	1.25R	RGMA[37]	2.25R	RGMA[5]	10.5R
RGMA[100]	1R	RGMA[68]	1.25R	RGMA[36]	2.25R	RGMA[4]	15.5R
RGMA[99]	1R	RGMA[67]	1.3333R	RGMA[35]	2.25R	RGMA[3]	23.5R
RGMA[98]	1R	RGMA[66]	1.3333R	RGMA[34]	2.625R	RGMA[2]	20R
RGMA[97]	1R	RGMA[65]	1.3333R	RGMA[33]	2.625R	RGMA[1]	24R
RGMA[96]	1R	RGMA[64]	1.3333R	RGMA[32]	2.75R	-	-

9. Register Description

9.1 Register table

9.1.1 Register page 0: Normal function

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	-	[7:1]	Reserved	Reserved.	19h
		R/W	[0]	OTP_TABLE2_EN	Enable reload OTP table2.	
02h	71h	R/W	[7]	INTL	Interlaced or normal input.	1h
			[6]	TR	Interface selection. **(Effective when FCS=0)**	
			[5]	DINT	Input data 6 or 8 bits selection.	
			[4]	MODE	Sync or DE mode.	
			[3]	HSP	HS polarity selection.	
			[2]	VSP	VS polarity selection.	
			[1]	CLOCKP	Clock polarity selection.	
			[0]	NB	Normally white or black.	
03h	FCh	R/W	[7]	RL	Horizontal scan direction. **(Effective when FCS=0)**	
			[6]	TB	Vertical scan direction. **(Effective when FCS=0)**	
			[5:4]	INV[1:0]	Inversion algorithm selection. **(Effective when FCS=0)**	
			[3:0]	RS[3:0]	Resolution selection. **(Effective when FCS=0)**	
04h	00h	R/W	[7:6]	GPOS[1:0]	Gate driver location. **(Effective when FCS=0)**	2h
			[5]	DGAMEN	Digital gamma enable.	
			[4:3]	TPSEL[1:0]	TPSYNC signal output selection.	
			[2]	SD_GND_V	Source output state in vertical blanking.	
			[1]	PON	Power on pattern selection.	
			[0]	POFF	Power off pattern selection.	
05h	CFh	R/W	[7]	GASEN	GAS function enable.	
			[6]	SPFEN	Self-protection mode enable.	
			[5]	SPFSEL	Self protection mode pattern selection.	
			[4]	BISTEN	BIST mode enable.	
			[3:0]	PTSEL[3:0]	BIST pattern selection.	
06h	05h	R/W	[7:0]	VSTS[7:0]	Vertical back porch adjustment.	3h
07h	10h	R/W	[7:0]	HSTS[7:0]	Horizontal back porch adjustment.	
08h	09h	R/W	[5:0]	OEW[5:0]	Timing for gate driver control.	
09h	06h	R/W	[5:0]	GEQW[5:0]	Timing for gate driver control.	
0Ah	C6h	R/W	[7:6]	PCR[1:0]	Timing for source driver control.	
			[5:0]	EQW[5:0]	Timing for source driver control.	
0Bh	30h	R/W	[7]	ENDRV	Source driver capability selection.	
			[6:4]	BC[2:0]	Source driver bias current selection.	
			[3:2]	POCSD[1:0]	Source output offset cancelling selection.	
			[1:0]	POCGM[1:0]	Gamma offset cancelling selection.	
0Ch	20h	R/W	[7:0]	TPOFFSET[7:0]	TPSYNC timing adjustment.	
0Dh	03h	R/W	[7]	RL_POL	Select polarity of RL pin/register.	
			[6]	TB_POL	Select polarity of TB pin/register.	
			[5]	DINT_POL	Select polarity of DINT pin/register.	
			[4]	MODE_POL	Select polarity of MODE pin/register.	
			[3:2]	PFMFS[1:0]	PFM clock frequency selection.	
			[1:0]	PFMOFF[1:0]	Set period to stop PFM for each line.	
0Eh	80h	R/W	[7:0]	RGC[7:0]	Gain **(contrast)** setting for red color.	4h
0Fh	80h	R/W	[7:0]	GGC[7:0]	Gain **(contrast)** setting for green color.	
10h	80h	R/W	[7:0]	BGC[7:0]	Gain **(contrast)** setting for blue color.	
11h	10h	R/W	[5:0]	ROB[5:0]	Offset **(brightness)** setting for red color.	
12h	10h	R/W	[5:0]	GOB[5:0]	Offset **(brightness)** setting for green color.	
13h	10h	R/W	[5:0]	BOB[5:0]	Offset **(brightness)** setting for blue color.	
14h	3Ah	R/W	[5]	AVDDPEN	AVDDP PFM enable.	5h
			[4]	AVDDNEN	AVDDN PFM enable.	
			[3:2]	DRVPS[1:0]	DRVP capability selection.	
			[1:0]	DRVNS[1:0]	DRVN capability selection.	
15h	DDh	R/W	[7:4]	AVDDPS[3:0]	AVDDP level selection.	

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
			[3:0]	AVDDNS[3:0]	AVDDN level selection.	
16h	CBh	R/W	[7]	VGHEN	VGH charge pump enable.	
			[6:4]	VGHS[2:0]	VGH level selection.	
			[3]	VGLEN	VGL charge pump enable.	
			[2:0]	VGLS[2:0]	VGL level selection.	
17h	EEh	R/W	[7:4]	VSDPS[3:0]	VSDP level selection.	5h
			[3:0]	VSDNS[3:0]	VSDN level selection.	
18h	55h	R/W	[7:4]	TON_PH[3:0]	Pulse width of high state of DRVP adjustment.	
			[3:0]	TOFF_PH[3:0]	Pulse width of low state of DRVP adjustment.	
19h	55h	R/W	[7:4]	TON_NH[3:0]	Pulse width of low state of DRVN adjustment.	
			[3:0]	TOFF_NH[3:0]	Pulse width of high state of DRVN adjustment.	
1Ah	55h	R/W	[7:4]	TON_PL[3:0]	Pulse width of high state of DRVP adjustment.	
			[3:0]	TOFF_PL[3:0]	Pulse width of low state of DRVP adjustment.	
1Bh	55h	R/W	[7:4]	TON_NL[3:0]	Pulse width of low state of DRVN adjustment.	
			[3:0]	TOFF_NL[3:0]	Pulse width of high state of DRVN adjustment.	
1Ch	55h	R/W	[7:4]	TON_PHS[3:0]	Pulse width of high state of DRVP adjustment.	
			[3:0]	TOFF_PHS[3:0]	Pulse width of low state of DRVP adjustment.	
1Dh	55h	R/W	[7:4]	TON_NHS[3:0]	Pulse width of low state of DRVN adjustment.	
			[3:0]	TOFF_NHS[3:0]	Pulse width of high state of DRVN adjustment.	
1Eh	91h	R/W	[7]	VDDTEN	VDD level detection enable.	
			[6:5]	VDDTS[1:0]	VDD detection threshold voltage selection.	
			[4]	VCOMEN	VCOM regulator enable.	
			[1:0]	VCOMD[1:0]	VCOM driving capability selection.	
1Fh	0Fh	R/W	[3]	VGHXS	VGH boosting mode selection.	
			[2]	VGLXS	VGL boosting mode selection.	
			[1:0]	FCP[1:0]	VGH and VGL charge pump frequency selection.	
20h	80h	R/W	[7:0]	VCOMS[7:0]	VCOM level selection.	6h
21h	00h	R	[4:0]	VCOM_FLAG[4:0]	OTP flag of VCOMS register.	-
22h	32h	R/W	[5]	VGMREFEN	VGMPH/M/LO, VGMNH/M/LO regulators enable.	7h
			[4:0]	VGMPHS[4:0]	VGMPHO level selection.	
23h	00h	R/W	[3:0]	VGMPLS[3:0]	VGMPLO level selection.	
24h	12h	R/W	[4:0]	VGMNHS[4:0]	VGMNHO level selection.	
25h	00h	R/W	[3:0]	VGMNLS[3:0]	VGMNLO level selection.	
26h	A0h	R/W	[7:4]	GATEPASS[3:0]	Password to enable manual vertical resolution selection.	0Dh
			[1:0]	GATENUM[9:8]	Manual vertical resolution selection. **(MSB)**	
27h	00h	R/W	[7:0]	GATENUM[7:0]	Manual vertical resolution selection. **(LSB)**	
28h	A0h	R/W	[7:4]	HSETPASS[3:0]	Password to enable manual horizontal resolution selection.	1Ah
			[2:0]	HSETNUM[10:8]	Manual horizontal resolution selection. **(MSB)**	
29h	00h	R/W	[7:0	HSETNUM[7:0]	Manual horizontal resolution selection. **(LSB)**	
2Ah	55h	R/W	[7:4]	TON_PLS[3:0]	Pulse width of high state of DRVP adjustment.	1Ah
			[3:0]	TOFF_PLS[3:0]	Pulse width of low state of DRVP adjustment.	
2Bh	55h	R/W	[7:4]	TON_NLS[3:0]	Pulse width of low state of DRVN adjustment.	
			[3:0]	TOFF_NLS[3:0]	Pulse width of high state of DRVN adjustment.	
2Ch	00h	R	[7:4]	CHIPID[3:0]	Chip ID.	-
			[3:0]	REVID[3:0]	Version ID.	

9.1.2 Register page 1: Analog gamma voltage reference

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[2:0]	VP0_[2:0]	Postive gamma reference GSH0 selection.	8h
02h	01h	R/W	[3:0]	VP1_[3:0]	Postive gamma reference GSH1 selection.	
03h	1Ch	R/W	[5:0]	VP6_[5:0]	Postive gamma reference GSH6 selection.	
04h	1Dh	R/W	[5:0]	VP11_[5:0]	Postive gamma reference GSH11 selection.	
05h	62h	R/W	[6:0]	VP28_[6:0]	Postive gamma reference GSH28 selection.	
06h	0Ah	R/W	[3:0]	VP35_[3:0]	Postive gamma reference GSH35 selection.	
07h	15h	R/W	[4:0]	VP47_[4:0]	Postive gamma reference GSH47 selection.	
08h	1Fh	R/W	[5:0]	VP67_[5:0]	Postive gamma reference GSH67 selection.	
09h	24h	R/W	[5:0]	VP87_[5:0]	Postive gamma reference GSH87 selection.	
0ah	26h	R/W	[5:0]	VP107_[5:0]	Postive gamma reference GSH107 selection.	
0bh	2Ah	R/W	[5:0]	VP147_[5:0]	Postive gamma reference GSH147 selection.	
0ch	2Ah	R/W	[5:0]	VP163_[5:0]	Postive gamma reference GSH163 selection.	
0dh	2Ah	R/W	[5:0]	VP187_[5:0]	Postive gamma reference GSH187 selection.	
0eh	20h	R/W	[5:0]	VP211_[5:0]	Postive gamma reference GSH211 selection.	
0fh	12h	R/W	[4:0]	VP225_[4:0]	Postive gamma reference GSH225 selection.	
10h	5Ah	R/W	[6:0]	VP233_[6:0]	Postive gamma reference GSH233 selection.	
11h	1Ah	R/W	[4:0]	VP241_[4:0]	Postive gamma reference GSH241 selection.	
12h	0Dh	R/W	[3:0]	VP252_[3:0]	Postive gamma reference GSH252 selection.	
13h	0Fh	R/W	[3:0]	VP255_[3:0]	Postive gamma reference GSH255 selection.	
14h	00h	R/W	[2:0]	VN0_[2:0]	Negative gamma reference GSL0 selection.	
15h	03h	R/W	[3:0]	VN1_[3:0]	Negative gamma reference GSL1 selection.	
16h	1Ch	R/W	[5:0]	VN6_[5:0]	Negative gamma reference GSL6 selection.	
17h	1Dh	R/W	[5:0]	VN11_[5:0]	Negative gamma reference GSL11 selection.	
18h	62h	R/W	[6:0]	VN28_[6:0]	Negative gamma reference GSL28 selection.	
19h	0Ah	R/W	[3:0]	VN35_[3:0]	Negative gamma reference GSL35 selection.	
1ah	1Ah	R/W	[4:0]	VN47_[4:0]	Negative gamma reference GSL47 selection.	
1bh	1Fh	R/W	[5:0]	VN67_[5:0]	Negative gamma reference GSL67 selection.	
1ch	24h	R/W	[5:0]	VN87_[5:0]	Negative gamma reference GSL87 selection.	
1dh	26h	R/W	[5:0]	VN107_[5:0]	Negative gamma reference GSL107 selection.	
1eh	2Ah	R/W	[5:0]	VN147_[5:0]	Negative gamma reference GSL147 selection.	
1fh	2Ah	R/W	[5:0]	VN163_[5:0]	Negative gamma reference GSL163 selection.	
20h	2Ah	R/W	[5:0]	VN187_[5:0]	Negative gamma reference GSL187 selection.	
21h	20h	R/W	[5:0]	VN211_[5:0]	Negative gamma reference GSL211 selection.	
22h	12h	R/W	[4:0]	VN225_[4:0]	Negative gamma reference GSL225 selection.	
23h	5Ah	R/W	[6:0]	VN233_[6:0]	Negative gamma reference GSL233 selection.	
24h	1Ah	R/W	[4:0]	VN241_[4:0]	Negative gamma reference GSL241 selection.	
25h	0Dh	R/W	[3:0]	VN252_[3:0]	Negative gamma reference GSL252 selection.	
26h	0Fh	R/W	[3:0]	VN255_[3:0]	Negative gamma reference GSL255 selection.	

9.1.3 Register page 2: Digital gamma settings (Red)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	GMA1R[7:0]	Digital gamma reference Y1[7:0]: Red_gray 0.	9h
02h	04h	R/W	[7:0]	GMA2R[7:0]	Digital gamma reference Y2[7:0]: Red_gray 1.	
03h	0Ch	R/W	[7:0]	GMA3R[7:0]	Digital gamma reference Y3[7:0]: Red_gray 3.	
04h	1Ch	R/W	[7:0]	GMA4R[7:0]	Digital gamma reference Y4[7:0]: Red_gray 7.	
05h	2Ch	R/W	[7:0]	GMA5R[7:0]	Digital gamma reference Y5[7:0]: Red_gray 11.	
06h	3Ch	R/W	[7:0]	GMA6R[7:0]	Digital gamma reference Y6[7:0]: Red_gray 15.	
07h	5Ch	R/W	[7:0]	GMA7R[7:0]	Digital gamma reference Y7[7:0]: Red_gray 23.	
08h	7Ch	R/W	[7:0]	GMA8R[7:0]	Digital gamma reference Y8[7:0]: Red_gray 31.	
09h	BCh	R/W	[7:0]	GMA9R[7:0]	Digital gamma reference Y9[7:0]: Red_gray 47.	
0Ah	FCh	R/W	[7:0]	GMA10R[7:0]	Digital gamma reference Y10[7:0]: Red_gray 63.	
0Bh	7Ch	R/W	[7:0]	GMA11R[7:0]	Digital gamma reference Y11[7:0]: Red_gray 95.	
0Ch	FCh	R/W	[7:0]	GMA12R[7:0]	Digital gamma reference Y12[7:0]: Red_gray 127.	
0Dh	00h	R/W	[7:0]	GMA13R[7:0]	Digital gamma reference Y13[7:0]: Red_gray 128.	
0Eh	80h	R/W	[7:0]	GMA14R[7:0]	Digital gamma reference Y14[7:0]: Red_gray 160.	
0Fh	00h	R/W	[7:0]	GMA15R[7:0]	Digital gamma reference Y15[7:0]: Red_gray 192.	
10h	40h	R/W	[7:0]	GMA16R[7:0]	Digital gamma reference Y16[7:0]: Red_gray 208.	
11h	80h	R/W	[7:0]	GMA17R[7:0]	Digital gamma reference Y17[7:0]: Red_gray 224.	
12h	A0h	R/W	[7:0]	GMA18R[7:0]	Digital gamma reference Y18[7:0]: Red_gray 232.	
13h	C0h	R/W	[7:0]	GMA19R[7:0]	Digital gamma reference Y19[7:0]: Red_gray 240.	
14h	D0h	R/W	[7:0]	GMA20R[7:0]	Digital gamma reference Y20[7:0]: Red_gray 244.	
15h	E0h	R/W	[7:0]	GMA21R[7:0]	Digital gamma reference Y21[7:0]: Red_gray 248.	
16h	F0h	R/W	[7:0]	GMA22R[7:0]	Digital gamma reference Y22[7:0]: Red_gray 252.	
17h	F8h	R/W	[7:0]	GMA23R[7:0]	Digital gamma reference Y23[7:0]: Red_gray 254.	
18h	FCh	R/W	[7:0]	GMA24R[7:0]	Digital gamma reference Y24[7:0]: Red_gray 255.	
19h	00h	R/W	[7:6]	GMA1R[9:8]	Digital gamma reference Y1[9:8]: Red_gray 0_MSB.	
			[5:4]	GMA2R[9:8]	Digital gamma reference Y2[9:8]: Red_gray 1_MSB.	
			[3:2]	GMA3R[9:8]	Digital gamma reference Y3[9:8]: Red_gray 3_MSB.	
			[1:0]	GMA4R[9:8]	Digital gamma reference Y4[9:8]: Red_gray 7_MSB.	
1Ah	00h	R/W	[7:6]	GMA5R[9:8]	Digital gamma reference Y5[9:8]: Red_gray 11_MSB.	
			[5:4]	GMA6R[9:8]	Digital gamma reference Y6[9:8]: Red_gray 15_MSB.	
			[3:2]	GMA7R[9:8]	Digital gamma reference Y7[9:8]: Red_gray 23_MSB.	
			[1:0]	GMA8R[9:8]	Digital gamma reference Y8[9:8]: Red_gray 31_MSB.	
1Bh	05h	R/W	[7:6]	GMA9R[9:8]	Digital gamma reference Y9[9:8]: Red_gray 47_MSB.	
			[5:4]	GMA10R[9:8]	Digital gamma reference Y10[9:8]: Red_gray 63_MSB.	
			[3:2]	GMA11R[9:8]	Digital gamma reference Y11[9:8]: Red_gray 95_MSB.	
			[1:0]	GMA12R[9:8]	Digital gamma reference Y12[9:8]: Red_gray 127_MSB.	
1Ch	AFh	R/W	[7:6]	GMA13R[9:8]	Digital gamma reference Y13[9:8]: Red_gray 128_MSB.	
			[5:4]	GMA14R[9:8]	Digital gamma reference Y14[9:8]: Red_gray 160_MSB.	
			[3:2]	GMA15R[9:8]	Digital gamma reference Y15[9:8]: Red_gray 192_MSB.	
			[1:0]	GMA16R[9:8]	Digital gamma reference Y16[9:8]: Red_gray 208_MSB.	
1Dh	FFh	R/W	[7:6]	GMA17R[9:8]	Digital gamma reference Y17[9:8]: Red_gray 224_MSB.	
			[5:4]	GMA18R[9:8]	Digital gamma reference Y18[9:8]: Red_gray 232_MSB.	
			[3:2]	GMA19R[9:8]	Digital gamma reference Y19[9:8]: Red_gray 240_MSB.	
			[1:0]	GMA20R[9:8]	Digital gamma reference Y20[9:8]: Red_gray 244_MSB.	
1Eh	FFh	R/W	[7:6]	GMA21R[9:8]	Digital gamma reference Y21[9:8]: Red_gray 248_MSB.	
			[5:4]	GMA22R[9:8]	Digital gamma reference Y22[9:8]: Red_gray 252_MSB.	
			[3:2]	GMA23R[9:8]	Digital gamma reference Y23[9:8]: Red_gray 254_MSB.	
			[1:0]	GMA24R[9:8]	Digital gamma reference Y24[9:8]: Red_gray 255_MSB.	

9.1.4 Register page 3: Digital gamma settings (Green)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	GMA1G[7:0]	Digital gamma reference Y1[7:0]: Green_gray 0.	0Ah
02h	04h	R/W	[7:0]	GMA2G[7:0]	Digital gamma reference Y2[7:0]: Green_gray 1.	
03h	0Ch	R/W	[7:0]	GMA3G[7:0]	Digital gamma reference Y3[7:0]: Green_gray 3.	
04h	1Ch	R/W	[7:0]	GMA4G[7:0]	Digital gamma reference Y4[7:0]: Green_gray 7.	
05h	2Ch	R/W	[7:0]	GMA5G[7:0]	Digital gamma reference Y5[7:0]: Green_gray 11.	
06h	3Ch	R/W	[7:0]	GMA6G[7:0]	Digital gamma reference Y6[7:0]: Green_gray 15.	
07h	5Ch	R/W	[7:0]	GMA7G[7:0]	Digital gamma reference Y7[7:0]: Green_gray 23.	
08h	7Ch	R/W	[7:0]	GMA8G[7:0]	Digital gamma reference Y8[7:0]: Green_gray 31.	
09h	BCh	R/W	[7:0]	GMA9G[7:0]	Digital gamma reference Y9[7:0]: Green_gray 47.	
0Ah	FCh	R/W	[7:0]	GMA10G[7:0]	Digital gamma reference Y10[7:0]: Green_gray 63.	
0Bh	7Ch	R/W	[7:0]	GMA11G[7:0]	Digital gamma reference Y11[7:0]: Green_gray 95.	
0Ch	FCh	R/W	[7:0]	GMA12G[7:0]	Digital gamma reference Y12[7:0]: Green_gray 127.	
0Dh	00h	R/W	[7:0]	GMA13G[7:0]	Digital gamma reference Y13[7:0]: Green_gray 128.	
0Eh	80h	R/W	[7:0]	GMA14G[7:0]	Digital gamma reference Y14[7:0]: Green_gray 160.	
0Fh	00h	R/W	[7:0]	GMA15G[7:0]	Digital gamma reference Y15[7:0]: Green_gray 192.	
10h	40h	R/W	[7:0]	GMA16G[7:0]	Digital gamma reference Y16[7:0]: Green_gray 208.	
11h	80h	R/W	[7:0]	GMA17G[7:0]	Digital gamma reference Y17[7:0]: Green_gray 224.	
12h	A0h	R/W	[7:0]	GMA18G[7:0]	Digital gamma reference Y18[7:0]: Green_gray 232.	
13h	C0h	R/W	[7:0]	GMA19G[7:0]	Digital gamma reference Y19[7:0]: Green_gray 240.	
14h	D0h	R/W	[7:0]	GMA20G[7:0]	Digital gamma reference Y20[7:0]: Green_gray 244.	
15h	E0h	R/W	[7:0]	GMA21G[7:0]	Digital gamma reference Y21[7:0]: Green_gray 248.	
16h	F0h	R/W	[7:0]	GMA22G[7:0]	Digital gamma reference Y22[7:0]: Green_gray 252.	
17h	F8h	R/W	[7:0]	GMA23G[7:0]	Digital gamma reference Y23[7:0]: Green_gray 254.	
18h	FCh	R/W	[7:0]	GMA24G[7:0]	Digital gamma reference Y24[7:0]: Green_gray 255.	
19h	00h	R/W	[7:6]	GMA1G[9:8]	Digital gamma reference Y1[9:8]: Green_gray 0_MSB.	
			[5:4]	GMA2G[9:8]	Digital gamma reference Y2[9:8]: Green_gray 1_MSB.	
			[3:2]	GMA3G[9:8]	Digital gamma reference Y3[9:8]: Green_gray 3_MSB.	
			[1:0]	GMA4G[9:8]	Digital gamma reference Y4[9:8]: Green_gray 7_MSB.	
1Ah	00h	R/W	[7:6]	GMA5G[9:8]	Digital gamma reference Y5[9:8]: Green_gray 11_MSB.	
			[5:4]	GMA6G[9:8]	Digital gamma reference Y6[9:8]: Green_gray 15_MSB.	
			[3:2]	GMA7G[9:8]	Digital gamma reference Y7[9:8]: Green_gray 23_MSB.	
			[1:0]	GMA8G[9:8]	Digital gamma reference Y8[9:8]: Green_gray 31_MSB.	
1Bh	05h	R/W	[7:6]	GMA9G[9:8]	Digital gamma reference Y9[9:8]: Green_gray 47_MSB.	
			[5:4]	GMA10G[9:8]	Digital gamma reference Y10[9:8]: Green_gray 63_MSB.	
			[3:2]	GMA11G[9:8]	Digital gamma reference Y11[9:8]: Green_gray 95_MSB.	
			[1:0]	GMA12G[9:8]	Digital gamma reference Y12[9:8]: Green_gray 127_MSB.	
1Ch	AFh	R/W	[7:6]	GMA13G[9:8]	Digital gamma reference Y13[9:8]: Green_gray 128_MSB.	
			[5:4]	GMA14G[9:8]	Digital gamma reference Y14[9:8]: Green_gray 160_MSB.	
			[3:2]	GMA15G[9:8]	Digital gamma reference Y15[9:8]: Green_gray 192_MSB.	
			[1:0]	GMA16G[9:8]	Digital gamma reference Y16[9:8]: Green_gray 208_MSB.	
1Dh	FFh	R/W	[7:6]	GMA17G[9:8]	Digital gamma reference Y17[9:8]: Green_gray 224_MSB.	
			[5:4]	GMA18G[9:8]	Digital gamma reference Y18[9:8]: Green_gray 232_MSB.	
			[3:2]	GMA19G[9:8]	Digital gamma reference Y19[9:8]: Green_gray 240_MSB.	
			[1:0]	GMA20G[9:8]	Digital gamma reference Y20[9:8]: Green_gray 244_MSB.	
1Eh	FFh	R/W	[7:6]	GMA21G[9:8]	Digital gamma reference Y21[9:8]: Green_gray 248_MSB.	
			[5:4]	GMA22G[9:8]	Digital gamma reference Y22[9:8]: Green_gray 252_MSB.	
			[3:2]	GMA23G[9:8]	Digital gamma reference Y23[9:8]: Green_gray 254_MSB.	
			[1:0]	GMA24G[9:8]	Digital gamma reference Y24[9:8]: Green_gray 255_MSB.	

9.1.5 Register page 4: Digital gamma settings (Blue)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[7:0]	GMA1B[7:0]	Digital gamma reference Y1[7:0]: Blue_gray 0.	0Bh
02h	04h	R/W	[7:0]	GMA2B[7:0]	Digital gamma reference Y2[7:0]: Blue_gray 1.	
03h	0Ch	R/W	[7:0]	GMA3B[7:0]	Digital gamma reference Y3[7:0]: Blue_gray 3.	
04h	1Ch	R/W	[7:0]	GMA4B[7:0]	Digital gamma reference Y4[7:0]: Blue_gray 7.	
05h	2Ch	R/W	[7:0]	GMA5B[7:0]	Digital gamma reference Y5[7:0]: Blue_gray 11.	
06h	3Ch	R/W	[7:0]	GMA6B[7:0]	Digital gamma reference Y6[7:0]: Blue_gray 15.	
07h	5Ch	R/W	[7:0]	GMA7B[7:0]	Digital gamma reference Y7[7:0]: Blue_gray 23.	
08h	7Ch	R/W	[7:0]	GMA8B[7:0]	Digital gamma reference Y8[7:0]: Blue_gray 31.	
09h	BCh	R/W	[7:0]	GMA9B[7:0]	Digital gamma reference Y9[7:0]: Blue_gray 47.	
0Ah	FCh	R/W	[7:0]	GMA10B[7:0]	Digital gamma reference Y10[7:0]: Blue_gray 63.	
0Bh	7Ch	R/W	[7:0]	GMA11B[7:0]	Digital gamma reference Y11[7:0]: Blue_gray 95.	
0Ch	FCh	R/W	[7:0]	GMA12B[7:0]	Digital gamma reference Y12[7:0]: Blue_gray 127.	
0Dh	00h	R/W	[7:0]	GMA13B[7:0]	Digital gamma reference Y13[7:0]: Blue_gray 128.	
0Eh	80h	R/W	[7:0]	GMA14B[7:0]	Digital gamma reference Y14[7:0]: Blue_gray 160.	
0Fh	00h	R/W	[7:0]	GMA15B[7:0]	Digital gamma reference Y15[7:0]: Blue_gray 192.	
10h	40h	R/W	[7:0]	GMA16B[7:0]	Digital gamma reference Y16[7:0]: Blue_gray 208.	
11h	80h	R/W	[7:0]	GMA17B[7:0]	Digital gamma reference Y17[7:0]: Blue_gray 224.	
12h	A0h	R/W	[7:0]	GMA18B[7:0]	Digital gamma reference Y18[7:0]: Blue_gray 232.	
13h	C0h	R/W	[7:0]	GMA19B[7:0]	Digital gamma reference Y19[7:0]: Blue_gray 240.	
14h	D0h	R/W	[7:0]	GMA20B[7:0]	Digital gamma reference Y20[7:0]: Blue_gray 244.	
15h	E0h	R/W	[7:0]	GMA21B[7:0]	Digital gamma reference Y21[7:0]: Blue_gray 248.	
16h	F0h	R/W	[7:0]	GMA22B[7:0]	Digital gamma reference Y22[7:0]: Blue_gray 252.	
17h	F8h	R/W	[7:0]	GMA23B[7:0]	Digital gamma reference Y23[7:0]: Blue_gray 254.	
18h	FCh	R/W	[7:0]	GMA24B[7:0]	Digital gamma reference Y24[7:0]: Blue_gray 255.	
19h	00h	R/W	[7:6]	GMA1B[9:8]	Digital gamma reference Y1[9:8]: Blue_gray 0_MSB.	
			[5:4]	GMA2B[9:8]	Digital gamma reference Y2[9:8]: Blue_gray 1_MSB.	
			[3:2]	GMA3B[9:8]	Digital gamma reference Y3[9:8]: Blue_gray 3_MSB.	
			[1:0]	GMA4B[9:8]	Digital gamma reference Y4[9:8]: Blue_gray 7_MSB.	
1Ah	00h	R/W	[7:6]	GMA5B[9:8]	Digital gamma reference Y5[9:8]: Blue_gray 11_MSB.	
			[5:4]	GMA6B[9:8]	Digital gamma reference Y6[9:8]: Blue_gray 15_MSB.	
			[3:2]	GMA7B[9:8]	Digital gamma reference Y7[9:8]: Blue_gray 23_MSB.	
			[1:0]	GMA8B[9:8]	Digital gamma reference Y8[9:8]: Blue_gray 31_MSB.	
1Bh	05h	R/W	[7:6]	GMA9B[9:8]	Digital gamma reference Y9[9:8]: Blue_gray 47_MSB.	
			[5:4]	GMA10B[9:8]	Digital gamma reference Y10[9:8]: Blue_gray 63_MSB.	
			[3:2]	GMA11B[9:8]	Digital gamma reference Y11[9:8]: Blue_gray 95_MSB.	
			[1:0]	GMA12B[9:8]	Digital gamma reference Y12[9:8]: Blue_gray 127_MSB.	
1Ch	AFh	R/W	[7:6]	GMA13B[9:8]	Digital gamma reference Y13[9:8]: Blue_gray 128_MSB.	
			[5:4]	GMA14B[9:8]	Digital gamma reference Y14[9:8]: Blue_gray 160_MSB.	
			[3:2]	GMA15B[9:8]	Digital gamma reference Y15[9:8]: Blue_gray 192_MSB.	
			[1:0]	GMA16B[9:8]	Digital gamma reference Y16[9:8]: Blue_gray 208_MSB.	
1Dh	FFh	R/W	[7:6]	GMA17B[9:8]	Digital gamma reference Y17[9:8]: Blue_gray 224_MSB.	
			[5:4]	GMA18B[9:8]	Digital gamma reference Y18[9:8]: Blue_gray 232_MSB.	
			[3:2]	GMA19B[9:8]	Digital gamma reference Y19[9:8]: Blue_gray 240_MSB.	
			[1:0]	GMA20B[9:8]	Digital gamma reference Y20[9:8]: Blue_gray 244_MSB.	
1Eh	FFh	R/W	[7:6]	GMA21B[9:8]	Digital gamma reference Y21[9:8]: Blue_gray 248_MSB.	
			[5:4]	GMA22B[9:8]	Digital gamma reference Y22[9:8]: Blue_gray 252_MSB.	
			[3:2]	GMA23B[9:8]	Digital gamma reference Y23[9:8]: Blue_gray 254_MSB.	
			[1:0]	GMA24B[9:8]	Digital gamma reference Y24[9:8]: Blue_gray 255_MSB.	

9.1.6 Register page 8: LVDS setting

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	09h	R/W	[5]	LVDS_AGING	LVDS power saving enable.	0Ch
			[4]	LVDS_FMT	LVDS data format selection.	
			[3:2]	RX_VB[1:0]	LVDS receiver bias current adjustment.	
			[1:0]	LVDS_VBDLL[1:0]	LVDS DLL bias current adjustment.	
02h	01h	R/W	[5:4]	LVDS_BW[1:0]	LVDS DLL bandwidth selection.	
			[2:0]	LVDS_CPB[2:0]	LVDS DLL charge pump current selection.	
03h	00h	R/W	[6:4]	LVDS_TC[2:0]	LVDS clock lane skew adjustment.	
			[2:0]	LVDS_TD0[2:0]	LVDS data lane 0 skew adjustment.	
04h	00h	R/W	[6:4]	LVDS_TD1[2:0]	LVDS data lane 1 skew adjustment.	
			[2:0]	LVDS_TD2[2:0]	LVDS data lane 2 skew adjustment.	
05h	00h	R/W	[2:0]	LVDS_TD3[2:0]	LVDS data lane 3 skew adjustment.	

9.1.7 Register page 9: OTP control

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP group
00h	00h	R/W	[7:0]	PAGE[7:0]	Register page selection.	-
01h	00h	R/W	[4:0]	OTP_GROUP[4:0]	OTP control.	-
02h	00h	R/W	[7:0]	WOTP[7:0]		
03h	00h	R/W	[7:1]	Reserved		
			[0]	OTP_WR		
04h	00h	R/W	[7:0]	Reserved	Reserved for testing.	-
05h	00h	R/W	[7:0]	Reserved		
06h	00h	R	[7:0]	Reserved		
07h	00h	R/W	[7:0]	Reserved		
08h	5Ah	R/W	[7:0]	Reserved		
09h	00h	R/W	[7]	Reserved		
			[6]	OTP_PROGRAM2	OTP program table2.	
			[5]	PTM	For marginal read.	
			[4:0]	Reserved	Reserved for testing.	

9.2 Page 0: Normal function setting

R00h: Register page selection.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	00h	1/0	PAGE[7:0]							
			0	0	0	0	0	0	0	0

PAGE: Register page selection. Register R00h is defined as PAGE[7:0] for all pages. Only page 0~4 and 8~9 can be used, page 10 is reserved for testing.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page 0	Default
0	0	0	0	0	0	0	1	Page 1	-
0	0	0	0	0	0	1	0	Page 2	
0	0	0	0	0	0	1	1	Page 3	
0	0	0	0	0	1	0	0	Page 4	-
0	0	0	0	0	1	0	1	-	
0	0	0	0	0	1	1	0	-	-
0	0	0	0	0	1	1	1	-	
0	0	0	0	1	0	0	0	Page 8	
0	0	0	0	1	0	0	1	Page 9	-
0	0	0	0	1	0	1	0	Page 10, reserved	-

R01h: OTP_TABLE2_EN.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	01h	1/0	Reserved							OTP_TABLE2_EN
			0	0	0	0	0	0	0	0

OTP_Table2_EN: OTP reload table1 / table2 selection.

OTP_TABLE2_EN	Function	Note
0	Reload table1 when ATREN=H	Default
1	Reload table2 when ATREN=H	-

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	02h	1/0	INTL	TR	DINT	MODE	HSP	VSP	CLOCKP	NB
			0	1	1	1	0	0	0	1

INTL: Interlaced selection.

INTL	Function	Note
0	Normal input	Default
1	Interlaced input	-

TR: Interface format selection.

TR	Function	Note
0	LVDS	-
1	TTL	Default

DINT: Input data 6-bit or 8-bit selection.

DINT	Function	Note
0	6-bit	-
1	8-bit	Default

MODE: Sync or DE mode selection.

MODE	Function	Note
0	DE only mode	-
1	Sync mode	Default

NB: Normally white/black selection.

NB	Function	Note
0	Normally white	-
1	Normally black	Default

HSP: HS polarity.

HSP	Function	Note
0	Low pulse	Default
1	High pulse	-

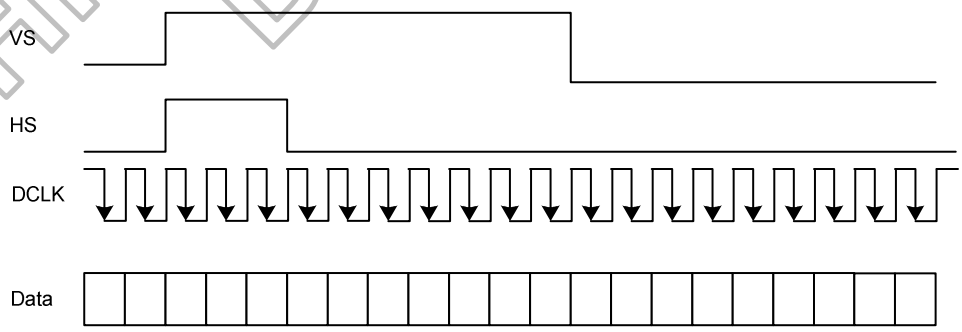
VSP: VS polarity.

VSP	Function	Note
0	Low pulse	Default
1	High pulse	-

CLOCKP: Clock latch data edge for TTL mode.

CLOCKP	Function	Note
0	Rising edge	Default
1	Falling edge	-

Example: CLOCKP=1,VSP=1,HSP=1



R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	03h	1/0	RL	TB	INV[1:0]		RS[3:0]			
			1	1	1	1	1	1	0	0

RL: Horizontal scan direction. **(Effective when FCS=0)**

RL	Function	Note
0	Reverse (**SOUT2400→SOUT1**)	-
1	Forward (**SOUT1→SOUT2400**)	Default

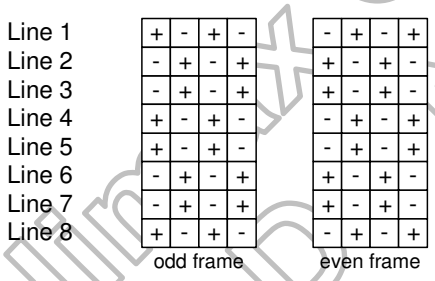
TB: Vertical scan direction. **(Effective when FCS=0)**

TB	Function	Note
0	Reverse (**Bottom→Top**)	-
1	Forward (**Top→Bottom**)	Default

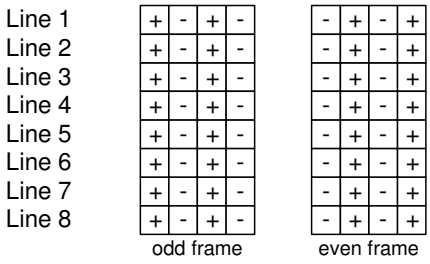
INV[1:0]: Inversion algorithm selection. **(Effective when FCS=0)**

INV[1:0]		Function	Note
0	0	1+2 line inversion	-
0	1	Column inversion	-
1	0	4 Dot inversion	-
1	1	Dot inversion	Default

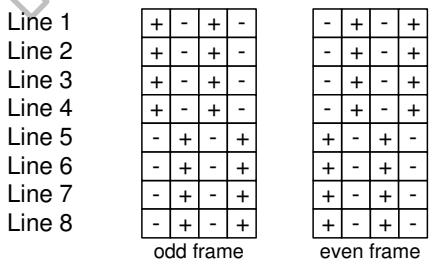
1+2 dot inversion



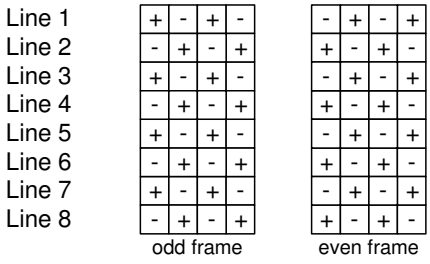
Column inversion



4 dot inversion



Dot inversion



RS[3:0]: Resolution selection. **(Effective when FCS=0)**

RS[3:0]				Function	Note
0	0	0	0	600RGBx1024	-
0	0	0	1	720RGBx480	-
0	0	1	0	720RGBx1280	-
0	0	1	1	768RGBx1024	Default
0	1	0	0	768RGBx1280	-
0	1	0	1	768RGBx1366	-
0	1	1	0	800RGBx480	-
0	1	1	1	800RGBx1280	-
1	0	0	0	960RGBx160	-
1	0	0	1	1024RGBx600	-
1	0	1	0	1280RGBx720	-
1	0	1	1	1440RGBx540	-
1	1	0	0	1600RGBx720	-
1	1	0	1	640RGBx480	-
1	1	1	0	720RGBx1280	-
1	1	1	1	720RGBx1280	-

R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	04h	1/0	GPOS[1:0]		DGAMEN	TPSEL[1:0]		SD_GND_V	PON	POFF
			0	0	0	0	0	0	0	0

GPOS[1:0]: Gate driver location. **(Effective when FCS=0)**

GPOS[1:0]		Function	Note
0	0	Left side	Default
0	1	Right side	-
1	0	Both sides, interlaced driving	-
1	1	Both sides, dual-side driving	-

DGAMEN: Digital gamma enable.

DGAMEN	Function	Note
0	Disable	Default
1	Enable	-

TPSEL: TPSYNC output selection.

TPSEL		Function	Note
0	0	For debug.	Default
0	1	TPSYNC is similar to VS can cannot be adjusted.	-
1	0	TPSYNC is similar to DE signal and can be adjusted by TPOFFSET.	-
1	1		-

SD_GND_V: Source output state in vertical blanking.

SD_GND_V	Function	Note
0	Source output keep the last data at V Blanking	Default
1	Source output pulled to ground at V Blanking	-

PON: Power on pattern selection.

PON	Function	Note
0	Black	Default
1	White	-

POFF: Power off pattern selection.

POFF	Function	Note
0	Black	Default
1	White	-

R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	05h	1/0	GASEN	SPFEN	SPFSEL	BISTEN	PTSEL[3:0]			
			1	1	0	0	1	1	1	1

GASEN: GAS function enable.

GASEN	Function	Note
0	Disable	-
1	Enable	Default

SPFEN: Self-protection mode enable.

SPFEN	Function	Note
0	Disable	-
1	Enable	Default

SPFSEL: Self protection mode pattern selection.

SPFSEL	Function	Note
0	Black	Default
1	White	-

BISTEN: BIST mode enable.

BISTEN	Function	Note
0	Disable	Default
1	Enable	-

PTSEL[3:0]: BIST pattern selection.

PTSEL[3:0]				Function	Note
0	0	0	0	Full black	-
0	0	0	1	Full white	-
0	0	1	0	Red	-
0	0	1	1	Green	-
0	1	0	0	Blue	-
0	1	0	1	VCOM trimming 1	-
0	1	1	0	VCOM trimming 2	-
0	1	1	1	VCOM trimming 3	-
1	0	0	0	VCOM trimming 4	-
1	0	0	1	Pixel On/Off	-
1	0	1	0	Auto run	-
1	0	1	1	Auto run	-
1	1	0	0	Auto run	-
1	1	0	1	Auto run	-
1	1	1	0	Auto run	-
1	1	1	1	Auto run	Default

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	06h	1/0	VSTS[7:0]							
			0	0	0	0	0	1	0	1

VSTS[7:0]: Vertical back porch adjustment.

VSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	2 H	-
0	0	0	0	0	0	0	1	2 H	-
0	0	0	0	0	0	1	0	2 H	-
0	0	0	0	0	0	1	1	3 H	-
:	:	:	:	:	:	:	:	:	-
0	0	0	0	0	1	0	1	5 H	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255 H	-

R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	07h	1/0	HSTS[7:0]							
			0	0	0	1	0	0	0	0

HSTS[7:0]: Horizontal back porch adjustment.

HSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	5 DCLK	-
:	:	:	:	:	:	:	:	5 DCLK	-
0	0	0	0	0	1	0	1	5 DCLK	-
0	0	0	0	0	1	1	0	6 DCLK	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	0	16 DCLK	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255 DCLK	-

R08h: Timing for gate driver control.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	08h	1/0	-	-	OEW[5:0]					
			0	0	0	0	1	0	0	1

OEW[5:0]: Timing for gate driver control. tOEV is the high pulse width of OEV which is the time that all gate channels are off between two lines. tOEV=OEW[5:0] * 8, and it should be smaller than 0.5*Hactive.

OEW[5:0]						Function	Note
0	0	0	0	0	0	24 DCLK	-
:	:	:	:	:	:	24 DCLK	-
0	0	0	0	1	1	24 DCLK	-
:	:	:	:	:	:	:	-
0	0	1	0	0	1	72 DCLK	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	504 DCLK	-

R09h: Timing for gate driver control.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	09h	1/0	-	-	GEQW[5:0]					
			0	0	0	0	0	1	1	0

GEQW[5:0]: Timing for gate driver control. tGEQ is the time from the falling edge of CPV to the rising edge of OEV.
tGEQ=GEQW[5:0] * 4.

GEQW[5:0]						Function	Note
0	0	0	0	0	0	0 DCLK	-
:	:	:	:	:	:	:	-
0	0	0	1	1	0	24 DCLK	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	252 DCLK	-

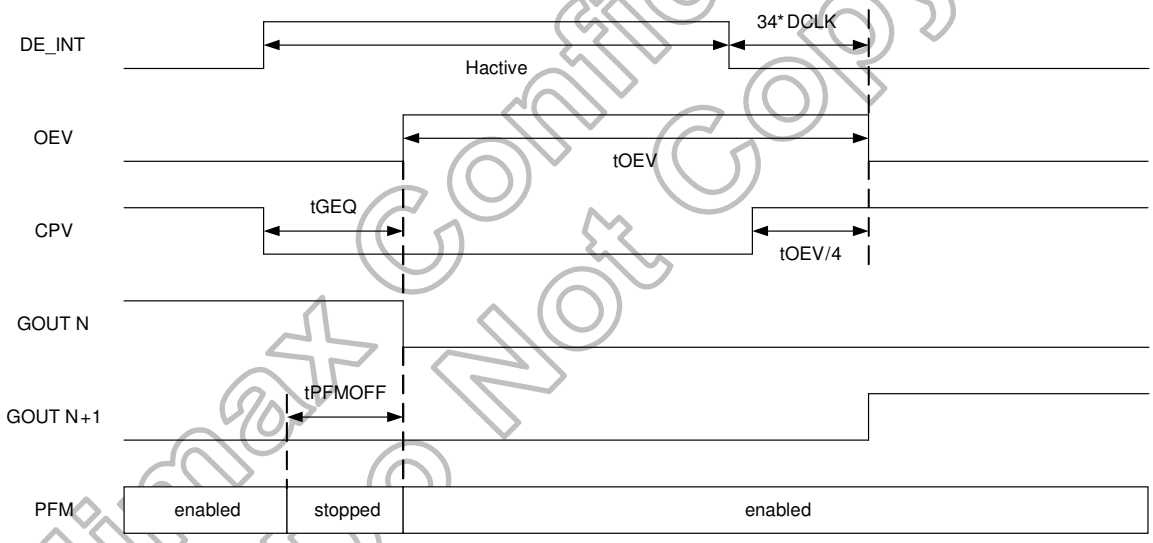


Figure 9.1: Gate control signals output and PFM timing

R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Ah	1/0	PCR[1:0]		EQW[5:0]					
			1	1	0	0	0	1	1	0

PCR[1:0]: Timing for source driver control. Source output are separated to four groups **(group 0h~3h)**, and tSWD is the time that output of each group driving each line is delayed.

PCR[1:0]		Function	Note
0	0	0	-
0	1	4 DCLK	-
1	0	8 DCLK	-
1	1	16 DCLK	Default

EQW[5:0]: Timing for source driver control. Source outputs are pulled to ground between each line if polarity changes, and tEQ is the time pulling output to ground. tEQ=EQW[5:0] *4*DCLK. It is suggested to set tEQ to 10%~20% of one line.

EQ0W[5:0]						Function	Note
0	0	0	0	0	0	12 DCLK	-
0	0	0	0	1	1	12 DCLK	-
0	0	0	1	1	0	24 DCLK	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	252 DCLK	-

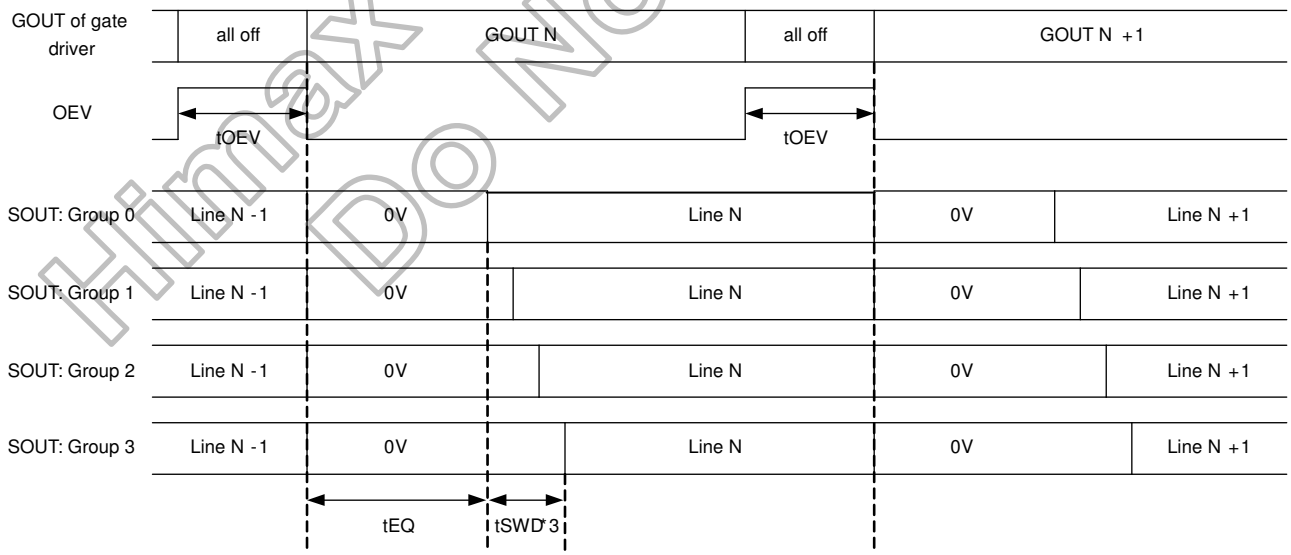


Figure 9.2: Source output timing

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Bh	1/0	ENDRV	BC[2:0]			POCSD[1:0]		POCGM[1:0]	
			0	0	1	1	0	0	0	0

ENDRV: Source driver capability selection.

ENDRV	Function	Note
0	100%	Default
1	200%	-

BC[2:0]: Source driver bias current selection.

BC[2:0]			Function	Note
0	0	0	40%	-
0	0	1	60%	-
0	1	0	80%	-
0	1	1	100%	Default
1	0	0	120%	-
1	0	1	140%	-
1	1	0	160%	-
1	1	1	180%	-

POCSD[1:0]: Source output offset cancelling selection.

POCSD[1:0]		Function	Note
0	0	Type 1: rotational	Default
0	1	Type 2: cancel by two lines	-
1	0	Type 3: cancel by lines	-
1	1	Type 4: no cancelling	-

POCGM[1:0]: Gamma offset cancelling selection.

POCGM[1:0]		Function	Note
0	0	Type 1: cancel by frame	Default
0	1	Type 2: cancel by two frames	-
1	0	Type 3: change with POCSD	-
1	1	Type 4: no cancelling	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Ch	1/0	TPOFFSET[7:0]							
			0	0	1	0	0	0	0	0

TPOFFSET [7:0]: TPSYNC timing adjustment, it is effective only when when TPSEL[1:0]=10.
DE_INT is an internal delayed version of DE, and its width is Hactive.
tTPD=DCLK * TPOFFSET[7:0], and tTPD should be smaller than Hactive.

TPOFFSET[7:0]								Function	Note
0	0	0	0	0	0	0	0	0*DCLK	-
:	:	:	:	:	:	:	:	:	-
0	0	1	0	0	0	0	0	32*DCLK	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255*DCLK	-

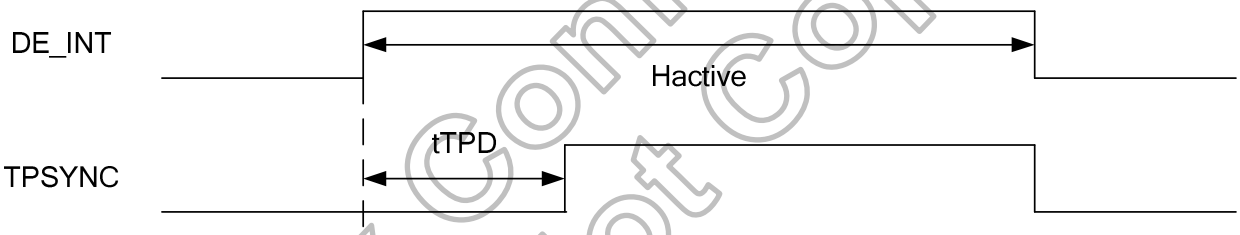


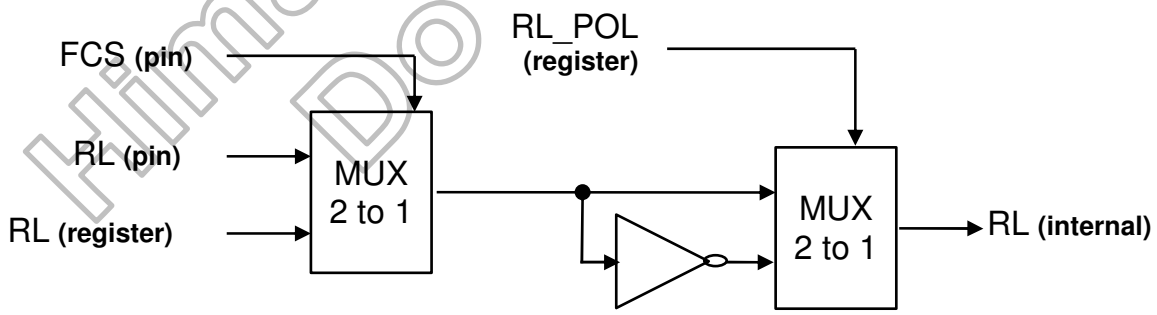
Figure 9.3: TPSYNC timing adjustment

R0Dh, R18h ~ R1Dh and R2Ah ~ R2Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Dh	1/0	RL_POL	TB_POL	DINT_POL	MODE_POL	PFMFS[1:0]		PFMOFF[1:0]	
			0	0	0	0	0	0	1	1
	18h		TON_PH[3:0]				TOFF_PH[3:0]			
			0	1	0	1	0	1	0	1
	19h		TON_NH[3:0]				TOFF_NH[3:0]			
			0	1	0	1	0	1	0	1
	1Ah		TON_PL[3:0]				TOFF_PL[3:0]			
			0	1	0	1	0	1	0	1
	1Bh		TON_NL[3:0]				TOFF_NL[3:0]			
			0	1	0	1	0	1	0	1
	1Ch		TON_PHS[3:0]				TOFF_PHS[3:0]			
			0	1	0	1	0	1	0	1
	1Dh		TON_NHS[3:0]				TOFF_NHS[3:0]			
			0	1	0	1	0	1	0	1
	2Ah		TON_PLS[3:0]				TOFF_PLS[3:0]			
			0	1	0	1	0	1	0	1
	2Bh		TON_NLS[3:0]				TOFF_NLS[3:0]			
			0	1	0	1	0	1	0	1

RL_POL: Select polarity of RL pin/register.

RL_POL	Function	Note
0	RL=1: SOUT1→SOUT2→SOUT2400 RL=0: SOUT2400→SOUT2399→SOUT1	Default
1	RL=1: SOUT2400→SOUT2399→SOUT1 RL=0: SOUT1→SOUT2→SOUT2400	-



TB_POL: Select polarity of TB pin/register.

TB_POL	Function	Note
0	TB=1: Top→Bottom TB=0: Bottom→Top	Default
1	TB=1: Bottom→Top TB=0: Top→Bottom	-

DINT_POL: Select polarity of DINT pin/register.

DINT_POL	Function	Note
0	DINT=1: 8-bit DINT=0: 6-bit	Default
1	DINT=1: 6-bit DINT=0: 8-bit	-

MODE_POL: Select polarity of MODE pin/register.

MODE_POL	Function	Note
0	MODE=1: Sync mode MODE=0: DE mode	Default
1	MODE=1: DE mode MODE=0: Sync mode	-

PFMFS [1:0]: PFM clock frequency selection.

PFMFS[1:0]		Function	Note
0	0	5.5MHz **(tPFM=181.8nsec)**	Default
0	1	11MHz **(tPFM=90.9nsec)**	-
1	0	22MHz **(tPFM=45.5nsec)**	-
1	1	22MHz **(tPFM=45.5nsec)**	-

PFMOFF [1:0]: Set period to stop PFM **(tPFMOFF)** for each line. Please refer to Figure 9.1: Gate control signals output and PFM timing.

PFMOFF[1:0]		Function	Note
0	0	Hactive/8	-
0	1	Hactive/4	-
1	0	0 **(PFM always enabled)**	-
1	1	0 **(PFM always enabled)**	Default

TON_PHS/PH/PLS/PL [3:0]: Pulse width of high state of DRVP **(tONP)** adjustment.

TON_PHS[3:0] TON_PH[3:0] TON_PLS[3:0] TON_PL[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

TOFF_PHS/PH/PLS/PL [3:0]: Pulse width of low state of DRVP **(tOFFP)** adjustment. Also note that low state will be larger than setting if AVDDP already reachs **(higher than)** the target.

TOFF_PHS[3:0] TOFF_PH[3:0] TOFF_PLS[3:0] TOFF_PL[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

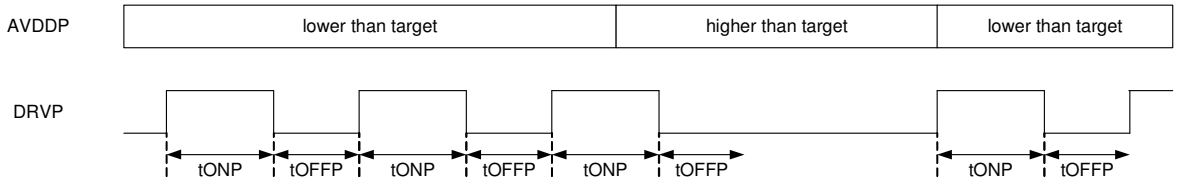


Figure 9.4: PFM settings for DRVP

TON_NHS/NH/NLS/NL [3:0]: Pulse width of low state of DRVN **(tONN)** adjustment.

TON_NHS[3:0] TON_NH[3:0] TON_NLS[3:0] TON_NL[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

TOFF_NHS/NH/NLS/NL [3:0]: Pulse width of high state of DRVN **(tOFFN)** adjustment. Also note that low state will be larger than setting if AVDDN already reachs **(lower than)** the target.

TOFF_NHS[3:0] TOFF_NH[3:0] TOFF_NLS[3:0] TOFF_NL[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

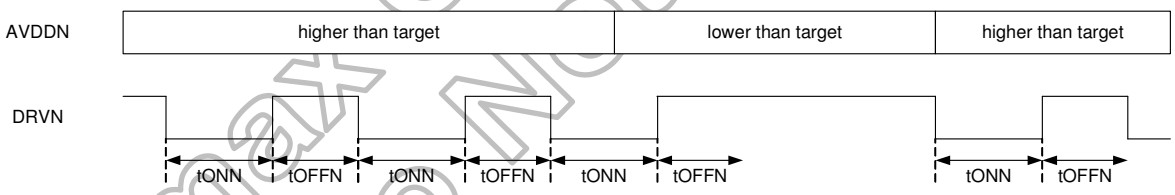


Figure 9.5: PFM settings for DRVN

R0Eh ~ R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Eh	1/0	RGC[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		GGC[7:0]							
			1	0	0	0	0	0	0	0
	10h		BGC[7:0]							
			1	0	0	0	0	0	0	0

RGC/GGC/BGC[7:0]: Gain **(contrast)** setting for red / green / blue color.
Gain=0.5+RGC/GGC/BGC[7:0]/256.

RGC[7:0] GGC[7:0] BGC[7:0]								Function	Note
0	0	0	0	0	0	0	0	128/256=0.500	-
0	0	0	0	0	0	0	1	129/256=0.504	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	256/256=1.000	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	383/256=1.496	-

R11h ~ R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	11h	1/0	-	-	ROB[5:0]					
			0	0	0	1	0	0	0	0
	12h		-	-	GOB[5:0]					
			0	0	0	1	0	0	0	0
	13h		-	-	BOB[5:0]					
			0	0	0	1	0	0	0	0

ROB/GOB/BOB[5:0]: Offset **(brightness)** setting for red/green/blue color.
Offset= -16+ROB/GOB/BOB[5:0].

ROB[5:0] GOB[5:0] BOB[5:0]						Function	Note
0	0	0	0	0	0	-16	-
0	0	0	0	0	1	-15	-
:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	Default
:	:	:	:	:	:	:	-

R14h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	14h	1/0	-	-	AVDDPEN	AVDDNEN	DRVPS[1:0]		DRVNS[1:0]	
			0	0	1	1	1	0	1	0

No.	R/W	Address								Default setting value							
R14	R/W	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	1/0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	0

AVDDPEN: AVDDP PFM enable, If AVDDPEN or AVDDNEN disable, the other one will disable too.

AVDDPEN	Function	Note
0	Disable	-
1	Enable	Default

AVDDNEN: AVDDN PFM enable.

AVDDNEN	Function	Note
0	Disable	-
1	Enable	Default

DRVPS[1:0]: DRVP capability selection.

DRVPS[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

DRVNS[1:0]: DRVN capability selection.

DRVNS[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	15h	1/0	AVDDPS[3:0]				AVDDNS[3:0]			
			1	1	0	1	1	1	0	1

AVDDPS[3:0]: AVDDP level selection.
AVDDP = 5.0+0.1*AVDDPS[3:0], max 6.3V.

AVDDPS[3:0]				Function	Note
0	0	0	0	5.0V	-
:	:	:	:	:	-
1	1	0	0	6.2V	-
1	1	0	1	6.3V	Default
:	:	:	:	:	-
1	1	1	1	6.3V	-

AVDDNS[3:0]: AVDDN level selection.
AVDDN = -5.0-0.1*AVDDNS[3:0], min -6.3V.

AVDDNS[3:0]				Function	Note
0	0	0	0	-5.0V	-
:	:	:	:	:	-
1	1	0	0	:	-
1	1	0	1	-6.3V	Default
:	:	:	:	:	-
1	1	1	1	-6.3V	-

R16h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	16h	1/0	VGHEN	VGHS[2:0]			VGLEN	VGLS[2:0]		
			1	1	0	0	1	0	1	1

VGHEN: VGH charge pump enable.

VGHEN	Function	Note
0	Disable	-
1	Enable	Default

VGHS[2:0]: VGH level selection.

VGHS[2:0]			Function	Note
0	0	0	12V	-
0	0	1	13V	-
0	1	0	14V	-
0	1	1	15V	-
1	0	0	16V	Default
1	0	1	17V	-
1	1	0	18V	-
1	1	1	19V	-

VGLEN: VGL charge pump enable.

VGLEN	Function	Note
0	Disable	-
1	Enable	Default

VGLS[2:0]: VGL level selection.

VGLS[2:0]			Function	Note
0	0	0	-7V	-
0	0	1	-8V	-
0	1	0	-9V	-
0	1	1	-10V	Default
1	0	0	-11V	-
1	0	1	-12V	-
1	1	0	-13V	-
1	1	1	-14V	-

Note: (1) VGH- VGL should be lower than 32V.

R17h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	17h	1/0	VSDPS[3:0]				VSDNS[3:0]			
			1	1	1	0	1	1	1	0

VSDPS[3:0]: VSDP level selection.
VSDP = 6.1 - 0.1 * (15-VSDPS[3:0])V, min = 5V.

VSDPS[3:0]				Function	Note
0	0	0	0	5.0V	-
:	:	:	:	:	-
0	1	0	0	5.0V	-
:	:	:	:	:	-
1	1	1	0	6.0V	Default
1	1	1	1	6.1V	-

VSDNS[3:0]: VSDN level selection.
VSDN = -6.1 + 0.1 * (15-VSDNS[3:0])V, max = -5V.

VSDNS[3:0]				Function	Note
0	0	0	0	-5.0V	-
:	:	:	:	:	-
0	1	0	0	-5.0V	-
:	:	:	:	:	-
1	1	1	0	-6.0V	Default
1	1	1	1	-6.1V	-

Note: (1) Must keep |AVDDP/N|-0.2 >= |VSDP/N|.

R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Eh	1/0	VDDTEN	VDDTS[1:0]		VCOMEN	-	-	VCOMD[1:0]	
			1	0	0	1	0	0	0	1

VDDTEN: VDD level detection enable.

VDDTEN	Function	Note
0	Disable	-
1	Enable	Default

VDDTS[1:0]: VDD detection threshold voltage selection.

VDDTS[1:0]		Function	Note
0	0	3.1V	Default
0	1	3.2V	-
1	0	3.3V	-
1	1	3.4V	-

VCOMEN: VCOM regulator enable.

VCOMEN	Function	Note
0	Disable	-
1	Enable	Default

VCOMD[1:0]: VCOM regulator capability selection.

VCOMD[1:0]		Function	Note
0	0	50%	-
0	1	100%	Default
1	0	150%	-
1	1	200%	-

R1Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Fh	1/0	-	-	-	-	VGHXS	VGLXS	FCP[1:0]	
			0	0	0	0	1	1	1	1

VGHXS: VGH boosting mode selection.

VGHXS	Function	Note
0	3X	-
1	4X	Default

VGLXS: VGL boosting mode selection.

VGLXS	Function	Note
0	2X	-
1	3X	Default

FCP[1:0]: VGH and VGL charge pump frequency selection.

FCP[1:0]		Function	Note
0	0	0.5 x Fline	-
0	1	1 x Fline	-
1	0	2 x Fline	-
1	1	4 x Fline	Default

R20h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	20h	1/0	VCOMS[7:0]							
			1	0	0	0	0	0	0	0

VCOMS [7:0]: VCOM level selection.
VCOM = -0.192+VCOMS[7:0]* (-0.012)V, min = -3V.

VCOMS[7:0]								Function	Note
0	0	0	0	0	0	0	0	-0.192V	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	-1.728V	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	-3.0V	-

R21h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	21h	0	-	-	-	VCOM_FLAG[4:0]				
			0	0	0	0	0	0	0	0

VCOM_FLAG[4:0]: OTP flag of VCOMS register. VCOMS[7:0] can be programmed to OTP for five times, this bit indicates how many times it has been programmed.

VCOM_FLAG[4:0]					Function	Note
0	0	0	0	0	Not programmed	Default
0	0	0	0	1	Programmed 1 time	-
0	0	0	1	1	Programmed 2 time	-
0	0	1	1	1	Programmed 3 time	-
0	1	1	1	1	Programmed 4 time	-
1	1	1	1	1	Programmed 5 time	

R22h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	22h	1/0	-	-	VGMREFEN	VGMPHS[4:0]				
			0	0	1	1	0	0	1	0

VGMREFEN: VGMPH/M/LO, VGMNH/M/LO regulators enable.

VGMREFEN	Function	Note
0	Disable	-
1	Enable	Default

VGMPHS[4:0]: VGMPHO level selection.
VGMPHO = 4 + 0.1* VGMPHS[4:0], max 5.9V.

VGMPHS[4:0]					Function	Note
0	0	0	0	0	4V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	Default
:	:	:	:	:	:	-
1	0	0	1	1	5.9V	-
1	1	1	1	1	5.9V	-

Note: (1) Must keep |VSDP/N|-0.2 >= |VGMPH/VGMNH|.

R23h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	23h	1/0	-	-	-	-	VGMPLS[3:0]			
			0	0	0	0	0	0	0	0

VGMPLS[3:0]: VGMPLO level selection.
VGMPLO = 0.2 + 0.1* VGMPLS[3:0].

VGMPLS[3:0]				Function	Note
0	0	0	0	0.2V	Default
:	:	:	:	:	-
1	0	0	1	1.1V	-
:	:	:	:	:	-
1	1	1	1	1.7V	-

R24h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	24h	1/0	-	-	-	VGMNHS[4:0]				
			0	0	0	1	0	0	1	0

VGMNHS [4:0]: VGMNHO level selection.
VGMNHO = -4 - 0.1* VGMNHS[4:0], min -5.9V.

VGMNHS[4:0]					Function	Note
0	0	0	0	0	-4.0V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	Default
:	:	:	:	:	:	-
1	0	0	1	1	-5.9V	-
1	1	1	1	1	-5.9V	-

R25h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	25h	1/0	-	-	-	-	VGMNLS[3:0]			
			0	0	0	0	0	0	0	0

VGMNLS [3:0]: VGMNLO level selection.
VGMNLO = -0.2 - 0.1* VGMNLS[3:0]

VGMNLS[3:0]				Function	Note
0	0	0	0	-0.2V	Default
:	:	:	:	:	-
1	0	0	1	-1.1V	-
:	:	:	:	:	-
1	1	1	1	-1.7V	-

R26h and R27h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	26h	1/0	GATEPASS[3:0]				-	-	GATENUM[9:8]	
			1	0	1	0	0	0	0	0
	27h		GATENUM[7:0]							
			0	0	0	0	0	0	0	0

GATEPASS[3:0]: Password to enable manual vertical resolution selection.

GATEPASS[3:0]				Function	Note
0	0	0	0	Disable	-
:	:	:	:	Disable	-
0	1	0	1	Enable	-
:	:	:	:	Disable	-
1	0	1	0	Disable	Default
:	:	:	:	Disable	-
1	1	1	1	Disable	-

GATENUM[9:0]: Manual vertical resolution selection. It is effective only if GATEPASS[3:0] is set to 0101b. When manual vertical resolution selection is enabled, vertical resolution Vactive is set to GATENUM[9:0]*2, where GATENUM[9:0]=50~1000 **(Vactive=100~2000)**.

GATENUM[9:0]										Function	Note
0	0	0	0	0	0	0	0	0	0	Not support	Default
0	0	0	0	0	0	0	0	0	1	Not support	-
:	:	:	:	:	:	:	:	:	:	Not support	-
0	0	0	0	1	1	0	0	0	1	Not support	-
0	0	0	0	1	1	0	0	1	0	100	-
:	:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	0	2000	-
1	1	1	1	1	0	1	0	0	1	Not support	
:	:	:	:	:	:	:	:	:	:	Not support	
1	1	1	1	1	1	1	1	1	1	Not support	

Note: (1) Vtotal should be smaller than 2046.

R28h & R29: Reserved

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	28h	1/0	HSETPASS[3:0]				-	HSETNUM[10:8]		
			1	0	1	0	0	0	0	0
	29h		HSETNUM[7:0]							
			0	0	0	0	0	0	0	0

HSETPASS[3:0]: Password to enable manual horizontal resolution selection.

HSETPASS[3:0]				Function	Note
0	0	0	0	Disable	-
:	:	:	:	Disable	-
0	1	0	1	Enable	-
:	:	:	:	Disable	-
1	0	1	0	Disable	Default
:	:	:	:	Disable	-
1	1	1	1	Disable	-

HSETNUM[10:0]: Manual horizontal resolution selection. It is effective only if HSETPASS[3:0] is set to 0101b. When manual horizontal resolution selection is enabled, Horizontal resolution Hactive is set to HSETNUM [10:0], where HSETNUM [10:0] should be an even number between 240~1600 **(HSETNUM[0] is always 0)**.

HSETNUM[10:0]											Function	Note
0	0	0	0	0	0	0	0	0	0	0	Not support	Default
:	:	:	:	:	:	:	:	:		:	Not support	-
0	0	0	1	1	1	0	1	1	1	1	Not support	-
0	0	0	1	1	1	1	0	0	0	0	240	-
:	:	:	:	:	:	:	:	:		:	:	-
1	1	0	0	1	0	0	0	0	0	0	1600	-
1	1	0	0	1	0	0	0	0	0	1	Not support	-
:	:	:	:	:	:	:	:	:		:	Not support	-
1	1	1	1	1	1	1	1	1	1	1	Not support	-

R2Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	2Ch	0	CHIPID[3:0]				REVID[3:0]			
			0	0	0	0	0	0	0	0

CHIPID[3:0]: Chip ID.

CHIPID[3:0]				Function	Note
0	0	0	0	-	Default
0	0	0	1	-	-
:	:	:	:	-	-
1	1	1	1	-	-

REVID[3:0]: Version ID.

REVID[3:0]				Function	Note
0	0	0	0	Version 1	-
0	0	0	1	Version 2	-
:	:	:	:	:	-
1	1	1	1	Version 16	-

9.3 Page 8: LVDS setting

R00h: Register page selection

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
8	00h	1/0	PAGE[7:0]							
			0	0	0	0	0	0	0	0

PAGE: Register page selection. Register R00h is defined as PAGE[7:0] for all pages. Only page 0~4 and 8~9 can be used, page 10 are reserved for testing.

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
8	01h	1/0	-	-	LVDS_AGIG	LVDS_FMT	RX_VB[1:0]		LVDS_VBDLL[1:0]	
			0	0	0	0	1	0	0	1

LVDS_AGING: LVDS power saving enable. When enabled, data lanes are turned off in BIST and self protection mode.

LVDS_AGING	Function	Note
0	Enabled	Default
1	Disabled	-

LVDS_FMT: LVDS data format selection.

LVDS_FMT	Function	Note
0	NS **(VESA)** format	Default
1	Thine **(JEIDA)** format	-

RX_VB[1:0]: LVDS receiver bias current adjustment.

RX_VB[1:0]		Function	Note
0	0	75%	
0	1	100%	
1	0	125%	Default
1	1	100%	

LVDS_VBDLL[1:0]: LVDS DLL bias current adjustment.

LVDS_VBDLL[1:0]		Function	Note
0	0	82%	
0	1	100%	Default
1	0	137%	
1	1	160%	

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
8	02h	1/0	-	-	LVDS_BW[1:0]		-	LVDS_CPB[2:0]		
			0	0	0	0	0	0	0	1

LVDS_BW[1:0]: LVDS DLL bandwidth selection.

LVDS_BW[1:0]		Function	Note
0	0		Default
0	1		-
1	0		-
1	1		-

LVDS_CPB[2:0]: LVDS DLL charge pump current selection.

LVDS_CPB[2:0]		Function	Note
0	0	0	
0	0	1	
:	:	:	
1	1	1	

R03h~R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
8	03h	1/0	-	LVDS_TC[2:0]			-	LVDS_TD0[2:0]		
			0	0	0	0	0	0	0	0
	04h		-	LVDS_TD1[2:0]			-	LVDS_TD2[2:0]		
			0	0	0	0	0	0	0	0
	05h		-	-	-	-	-	LVDS_TD3[2:0]		
			0	0	0	0	0	0	0	0

LVDS_TC[2:0]: LVDS clock lane skew adjustment.
LVDS_TD0[2:0]: LVDS data lane 0 **(LV0P/N and LV0P/NR)** skew adjustment.
LVDS_TD1[2:0]: LVDS data lane 1 **(LV1P/N and LV1P/NR)** skew adjustment.
LVDS_TD2[2:0]: LVDS data lane 2 **(LV2P/N and LV2P/NR)** skew adjustment.
LVDS_TD3[2:0]: LVDS data lane 3 **(LV3P/N and LV3P/NR)** skew adjustment.

LVDS_TC[2:0] LVDS_TD0[2:0] LVDS_TD1[2:0] LVDS_TD2[2:0] LVDS_TD3[2:0]			Function	Note
0	0	0	Delay 0*Td	Default
:	:	:		-
1	1	1	Delay 7*Td	-

9.4 Page 9: OTP control

R00h: Register page selection.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
9	00h	1/0	PAGE[7:0]							
			0	0	0	0	0	0	0	0

PAGE: Register page selection. Register R00h is defined as PAGE[7:0] for all pages. Only page 0~4 and 8~9 can be used, page 10 are reserved for testing.

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
9	01h	1/0	-	-	-	OTP_GROUP[4:0]				
			0	0	0	0	0	0	0	0

OTP_GROUP[4:0]: OTP program is in unit of OTP_Group. Each OTP_Group include several registers, detail refer to chaper 6.9 and 9.1.

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
9	02h	1/0	WOTP[7:0]							
			0	0	0	0	0	0	0	0

WOTP[7:0]: OTP program command enable/disable. Only when WOTP[7:0]=66h , OTP program enable , the other will disable.

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
9	03h	1/0	-	-	-	-	-	-	-	OTP_WR
			0	0	0	0	0	0	0	0

OTP_WR: Write OTP table enable/disable. Only when OTP_WR=1, write OTP is effective.

R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
9	09h	1/0	-	OTP_PROGRAM2	PTM[1]	-	-	-	-	-
			0	0	0	0	0	0	0	0

OTP_PROGRAM2: OTP table2 program selection.

OTP_PROGRAM2	Function	Note
0	OTP program first time **(OTP table1)**	Default
1	OTP program secind time **(OTP table2)**	-

PTM: for OTP marginal read, detail refer to 6.9.2.

PTM	Function	Note
0	Disabled	Default
1	Enabled	-

10. AC/DC Characteristics

10.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Main and I/O power supply	VDD1	-0.3	-	4.0	V
Power supply for internal reference	VDD2	-0.3	-	3.96	V
Power supply for source driver	AVDDP	-0.3	-	6.5	V
Power supply for source driver	AVDDN	-6.5	-	0.3	V
Programming voltage **(under 60sec)**	VDDOTP	-0.3	-	7.75	V
Storage temperature	T_{ST}	-55	-	+125	℃
Operating temperature	T_{OP}	-20	-	+85	℃
Junction temperature	Tjc	-	-	+125	℃
Digital I/O input signals: Input interface pins Input control pins,group1 Input control pins,group2 Serial interface pins Cascade and gate driver control pins	V_{IO}	-0.3		VDD1 + 0.3	V

Note: (1) Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) If VGH and VGL are given by external power supplies, they are not necessary to connect to HX8249-A01. But if they are connected, VGH- VGL should be lower than 32V.

10.2 Electrical characteristics

10.2.1 TTL interface

(VDD1=VDD2=2.7 to 3.6V, VSS1=VSS2=VSSA=0V, T_{OP}=25℃)

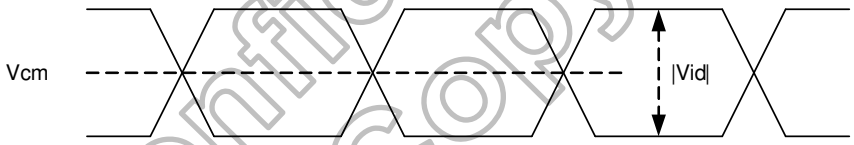
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Operating frequency, TTL mode	F_{TTL}	-	5.25	-	60	MHz
Operating frequency, LVDS mode	F_{LVDS}	-	10	-	85	MHz
Supply voltage for main power and digital I/O	VDD1 VDD2	-	2.7	-	3.6	V
Low level input voltage	Vil	-	VSS1-0.3	-	0.3*VDD1	V
High level input voltage	Vih	-	0.7*VDD1	-	VDD1+0.3	V
High level output voltage	V_{OH}	-	VDD1-0.4	-	-	V
Low level output voltage	V_{OL}	-	VSS1	-	VSS1+0.4	V
Pull low / high resistor	R_I	For digital input pins	200	350	850	KΩ
Low level input leakage current	I_{LKGL}	For digital input pins with pull high resistor	-18	-	2	μA
		For digital input pins without pull high resistor	-2	0	2	μA
High level input leakage current	I_{LKGH}	For digital input pins with pull low resistor	-2	-	18	μA
		For digital input pins without pull low resistor	-2	0	2	μA

10.2.2 LVDS interface

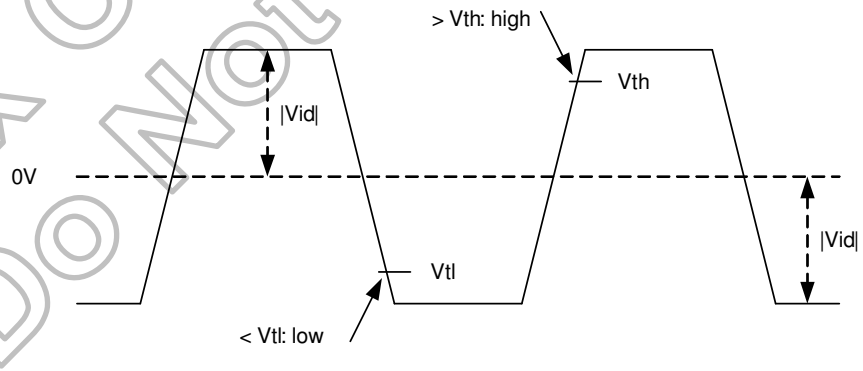
(VDD1=VDD2=2.7 to 3.6V, VSS1=VSS2=VSSA=0V, T_{OP} =25℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Differential input high Threshold voltage	Vth	Vcm=1.2V	-	-	+0.1	V
Differential input low threshold voltage	Vtl		-0.1	-	-	V
Differential input common Mode voltage	Vcm	-	1	1.2	1.8-|V_{id}|/2	V
LVDS input voltage	V_{INLV}		0.7		1.8	V
Differential input voltage	|Vid|	-	0.2	-	0.6	V
Differential input leakage Current	Ilvleak	-	-10	-	+10	μA
Termination Resistor	Zid	-	80	100	120	Ω

Single-ended:
LVCLKP (R),
LVCLKN (R),
LVD [3:0]P(R),
LVD [3:0]N(R)



Differential:
LVCLKP (R)-LVCLKN (R),
LVD [3:0]P(R)-
LVD [3:0]N(R)



10.2.3 Analog circuit

(VDD1=VDD2=2.7 to 3.6V, VSS1=VSS2=VSSA=0V, T_A=25℃)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Analog positive supply voltage	AVDDP	AVDDP is generated by PFM, AVDDPS[3:0]=Dh, with proper settings and components.	6.15	6.3	6.45	V
Analog negative supply voltage	AVDDN	AVDDN is generated by PFM, AVDDNS[3:0]=Dh, with propoer settings and components.	-6.45	-6.3	-6.15	V
Source driver positive supply voltage	VSDP	AVDDP=6.3V, VSDPS[3:0]=Fh, loading current=0	5.95	6.1	6.25	V
Source driver negative supply voltage	VSDN	AVDDN= -6.3V, VSDNS[3:0]=Fh, loading current=0	-6.25	-6.1	-5.95	V
Output for positive gamma reference high voltage	VGMPHO	VSDP≧6V, VGMPHS[4:0]=12h, connected to VGMPHI.	5.75	5.9	6.05	V
Output for positive gamma reference low voltage	VGMPLO	VGMPLS[3:0]=0h, connected to VGMPLI.	0.15	0.2	0.25	V
Output for negative gamma reference high voltage	VGMNHO	VSDN≦-6V, VGMNHS[4:0]=12h, connected to VGMNHI.	-6.05	-5.9	-5.75	V
Output for negative gamma reference low voltage	VGMNLO	VGMNLS[3:0]=0h, connected to VGMNLI.	-0.25	-0.2	-0.15	V
VCOM voltage	VCOM	VCOMS[7:0]=80h	-1.768	-1.728	-1.688	V
OTP programming voltage	VDDOTP	OTP program sequence < 60sec.	7.4	7.5	7.7	V
Internal digital operating voltage	DVDD	-	1.4	1.5	1.6	V
Internal regulator output for negative level shifter	VCL	-	-2.65	-2.5	-2.35	V
Source output voltage, positive polarity	V_{SDOP}	-	0.2	-	VSDP-0.2	V
Source output voltage, negative polarity	V_{SDON}	-	VSDN+0.2	-	-0.2	V
Output for gate driver positive power supply	VGH	VGH is generated by charge pump, VGHS[2:0]= 4h, loading current=0.	14.5	16	17.5	V
Output for gate driver negative power supply	VGL	VGL is generated by charge pump, VGLS[2:0]=3h, loading current=0.	-11	-10	-9	V

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Source output voltage deviation	V_{OD}	VSO=0.2 to 1V VSO= -1 to -0.2V	-	-	15	mV
		VSO=1V to (VSDP – 1V) VSO=(VSDN+ 1V) to -1V			10	mV
		VSO=(VSDP - 1V) to (VSDP - 0.2V) VSO=(VSDN + 0.2V) to (VSDN + 1V)	-	-	15	mV
Standby current **(VDD1 + VDD2)**	I_{STBVDD}	STBYB=0, stop all input signal and all input signals match internal pull high/low	-	-	150	μA
Standby current **(AVDDP)**	$I_{STBAVDDP}$	-	-	-	20	μA
Standby current **(AVDDN)**	$I_{STBAVDDN}$	-	-80	-	-	μA

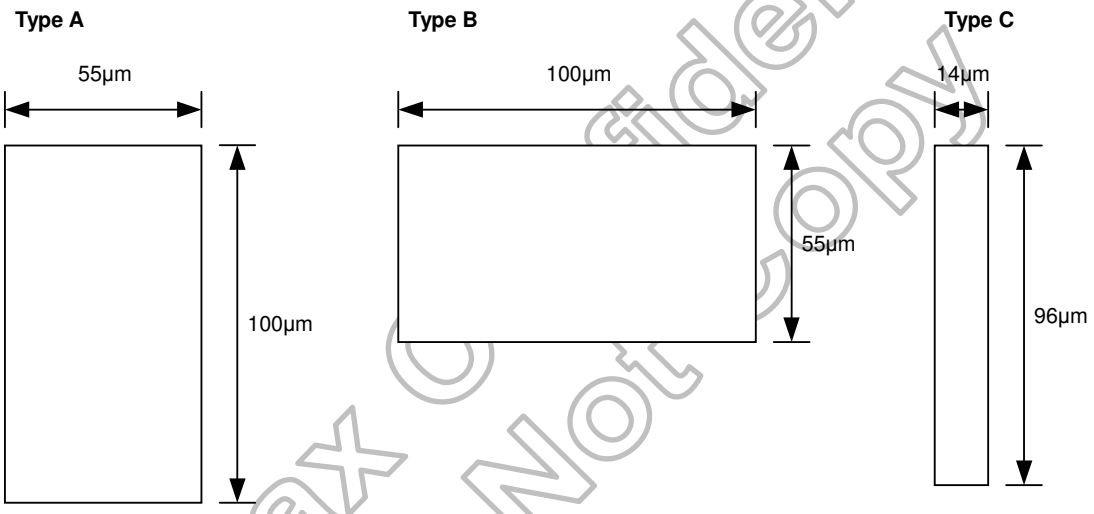
11. Chip Information

11.1 Chip size

Parameter	Size		Unit
	X	Y	
Chip size	27320	980	μm
Chip size **(include scribe line)**	27400	1060	

Table 11.1: Chip Information

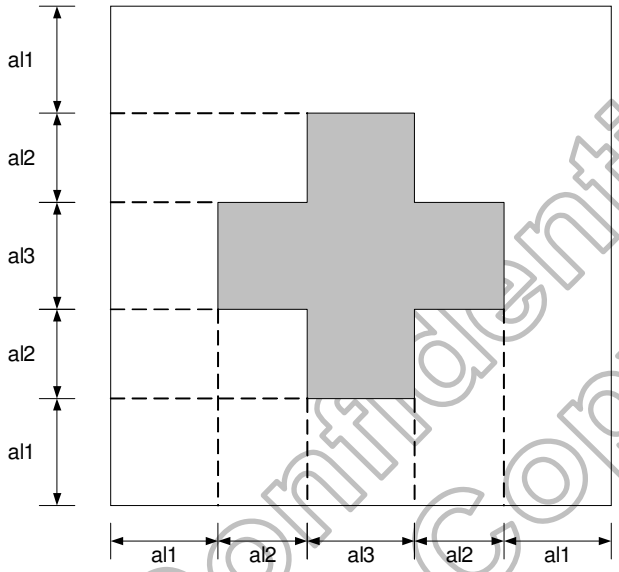
11.2 Bump information



Bump height: 12±3.0μm
Bump height Co-planarity within Die: < 2μm
Hardness: 75±20Hv
Shear stress: > 4.5 g/mil^2

11.3 Alignment mark

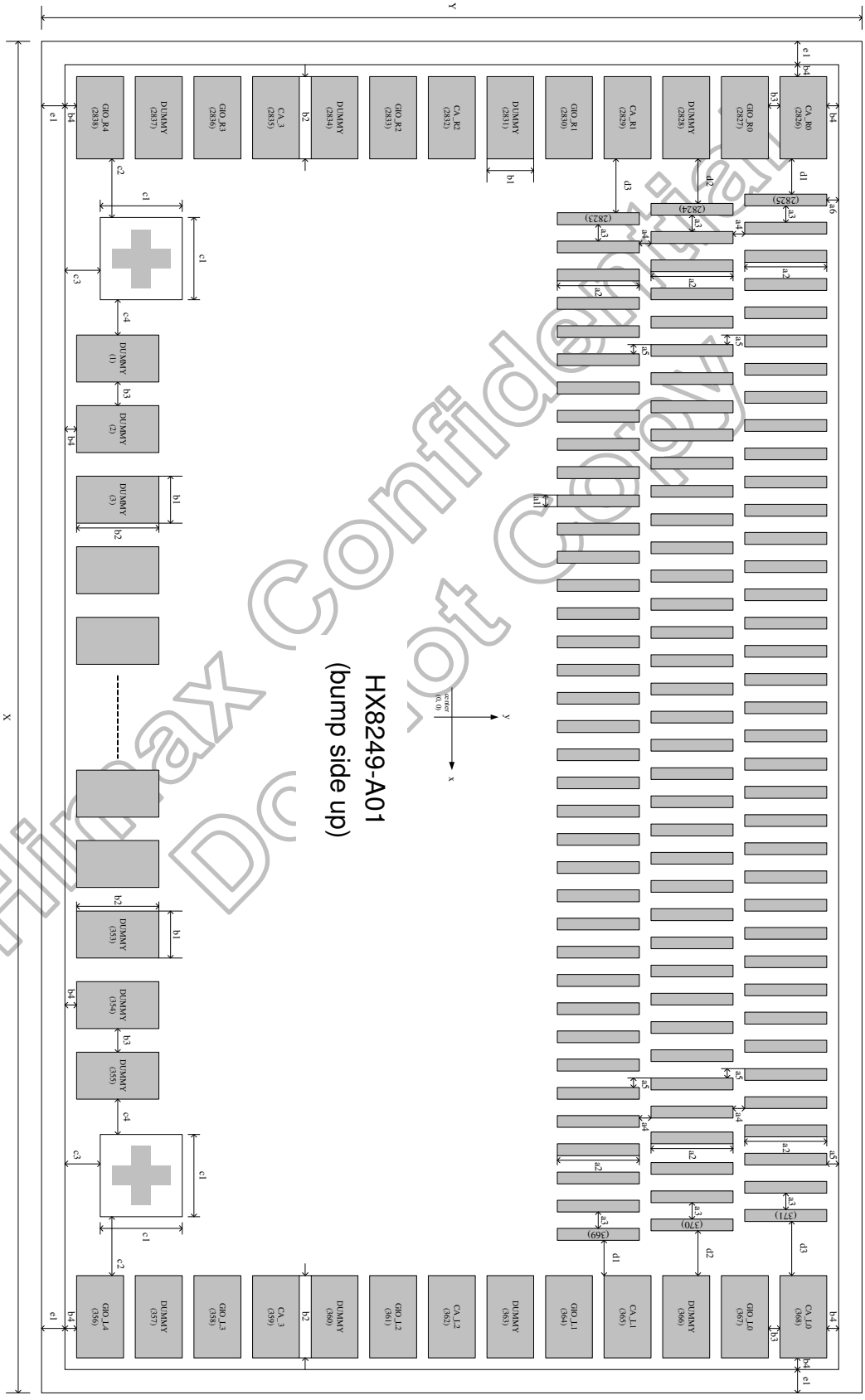
Two Alignment marks are center located at (-13400, -380) and (13400, -380). The cross pattern is top metal layer.



Symbol	Dimension (μm)
al1	29.75
al2	25.5
al3	29.5

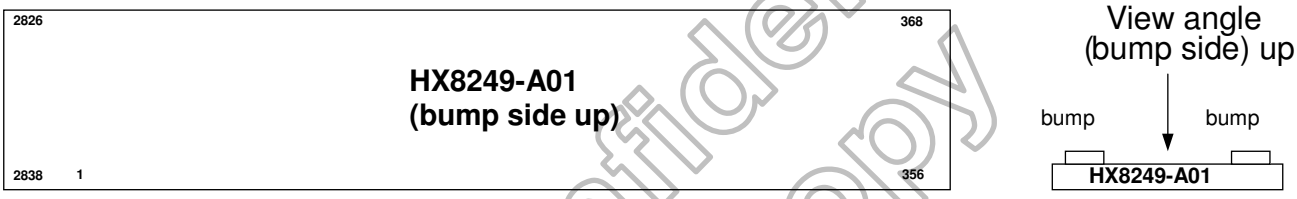
Table 11.2: Alignment mark dimension

11.4 Chip outline



Symbol	Dimension (μm)	Symbol	Dimension (μm)
a1	14	c1	140
a2	96	c2	77.5
a3	19	c3	40
a4	30	c4	27.5
a5	11	d1	32.5
a6	12.5	d2	43.5
b1	55	d3	54.5
b2	100	e1	40
b3	20	-	-
b4	12.5	-	-

Table 11.3: Chip outline dimension



12. Pad Coordinates

No.	Name	X	Y	Bump size (μm)	No.	Name	X	Y	Bump size (μm)
1	DUMMY	-13275	-427.5	55x100	51	CH1N	-9525	-427.5	55x100
2	DUMMY	-13200	-427.5	55x100	52	CH1N	-9450	-427.5	55x100
3	DUMMY	-13125	-427.5	55x100	53	VSS1P	-9375	-427.5	55x100
4	DUMMY	-13050	-427.5	55x100	54	VSS1P	-9300	-427.5	55x100
5	DUMMY	-12975	-427.5	55x100	55	VSS1P	-9225	-427.5	55x100
6	DUMMY	-12900	-427.5	55x100	56	VSS1P	-9150	-427.5	55x100
7	DUMMY	-12825	-427.5	55x100	57	VCL	-9075	-427.5	55x100
8	DUMMY	-12750	-427.5	55x100	58	VCL	-9000	-427.5	55x100
9	DUMMY	-12675	-427.5	55x100	59	VCL	-8925	-427.5	55x100
10	VCOM_R	-12600	-427.5	55x100	60	VCL	-8850	-427.5	55x100
11	VCOM_R	-12525	-427.5	55x100	61	AVDDN	-8775	-427.5	55x100
12	VCOM_R	-12450	-427.5	55x100	62	AVDDN	-8700	-427.5	55x100
13	THROUGH_1	-12375	-427.5	55x100	63	AVDDN	-8625	-427.5	55x100
14	THROUGH_1	-12300	-427.5	55x100	64	AVDDN	-8550	-427.5	55x100
15	CL2N	-12225	-427.5	55x100	65	AVDDN	-8475	-427.5	55x100
16	CL2N	-12150	-427.5	55x100	66	AVDDN	-8400	-427.5	55x100
17	CL2N	-12075	-427.5	55x100	67	AVDDN	-8325	-427.5	55x100
18	CL2P	-12000	-427.5	55x100	68	DRVN	-8250	-427.5	55x100
19	CL2P	-11925	-427.5	55x100	69	DRVN	-8175	-427.5	55x100
20	CL2P	-11850	-427.5	55x100	70	VDD1P	-8100	-427.5	55x100
21	CL1P	-11775	-427.5	55x100	71	VDD1P	-8025	-427.5	55x100
22	CL1P	-11700	-427.5	55x100	72	VDD1P	-7950	-427.5	55x100
23	CL1P	-11625	-427.5	55x100	73	VDD1P	-7875	-427.5	55x100
24	CL1N	-11550	-427.5	55x100	74	VSDN	-7800	-427.5	55x100
25	CL1N	-11475	-427.5	55x100	75	VSDN	-7725	-427.5	55x100
26	CL1N	-11400	-427.5	55x100	76	VSDN	-7650	-427.5	55x100
27	VGL	-11325	-427.5	55x100	77	VSDN	-7575	-427.5	55x100
28	VGL	-11250	-427.5	55x100	78	VSDN	-7500	-427.5	55x100
29	VGL	-11175	-427.5	55x100	79	VSDN	-7425	-427.5	55x100
30	VGL	-11100	-427.5	55x100	80	VSSA	-7350	-427.5	55x100
31	DUMMY	-11025	-427.5	55x100	81	VSSA	-7275	-427.5	55x100
32	VGH	-10950	-427.5	55x100	82	VSSA	-7200	-427.5	55x100
33	VGH	-10875	-427.5	55x100	83	VSSA	-7125	-427.5	55x100
34	VGH	-10800	-427.5	55x100	84	VSSA	-7050	-427.5	55x100
35	CH3P	-10725	-427.5	55x100	85	VSSA	-6975	-427.5	55x100
36	CH3P	-10650	-427.5	55x100	86	VSDP	-6900	-427.5	55x100
37	CH3P	-10575	-427.5	55x100	87	VSDP	-6825	-427.5	55x100
38	CH3N	-10500	-427.5	55x100	88	VSDP	-6750	-427.5	55x100
39	CH3N	-10425	-427.5	55x100	89	VSDP	-6675	-427.5	55x100
40	CH3N	-10350	-427.5	55x100	90	VSDP	-6600	-427.5	55x100
41	CH2P	-10275	-427.5	55x100	91	VSDP	-6525	-427.5	55x100
42	CH2P	-10200	-427.5	55x100	92	DRVP	-6450	-427.5	55x100
43	CH2P	-10125	-427.5	55x100	93	DRVP	-6375	-427.5	55x100
44	CH2N	-10050	-427.5	55x100	94	AVDDP	-6300	-427.5	55x100
45	CH2N	-9975	-427.5	55x100	95	AVDDP	-6225	-427.5	55x100
46	CH2N	-9900	-427.5	55x100	96	AVDDP	-6150	-427.5	55x100
47	CH1P	-9825	-427.5	55x100	97	AVDDP	-6075	-427.5	55x100
48	CH1P	-9750	-427.5	55x100	98	AVDDP	-6000	-427.5	55x100
49	CH1P	-9675	-427.5	55x100	99	AVDDP	-5925	-427.5	55x100
50	CH1N	-9600	-427.5	55x100	100	AVDDP	-5850	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
101	VSS1	-5775	-427.5	55x100
102	VSS1	-5700	-427.5	55x100
103	TEST0	-5625	-427.5	55x100
104	TEST0	-5550	-427.5	55x100
105	TEST1	-5475	-427.5	55x100
106	TEST1	-5400	-427.5	55x100
107	TEST2	-5325	-427.5	55x100
108	TEST2	-5250	-427.5	55x100
109	TEST3	-5175	-427.5	55x100
110	TEST3	-5100	-427.5	55x100
111	VDD1	-5025	-427.5	55x100
112	VDD1	-4950	-427.5	55x100
113	TEST4	-4875	-427.5	55x100
114	TEST4	-4800	-427.5	55x100
115	TEST5	-4725	-427.5	55x100
116	TEST5	-4650	-427.5	55x100
117	TEST6	-4575	-427.5	55x100
118	TEST6	-4500	-427.5	55x100
119	TEST7	-4425	-427.5	55x100
120	TEST7	-4350	-427.5	55x100
121	VSS1	-4275	-427.5	55x100
122	CSB	-4200	-427.5	55x100
123	SCL	-4125	-427.5	55x100
124	SDA	-4050	-427.5	55x100
125	SDA	-3975	-427.5	55x100
126	SDA	-3900	-427.5	55x100
127	VSS1	-3825	-427.5	55x100
128	VSS1	-3750	-427.5	55x100
129	VSS1	-3675	-427.5	55x100
130	VSS1	-3600	-427.5	55x100
131	TPSYNC	-3525	-427.5	55x100
132	TPSYNC	-3450	-427.5	55x100
133	ATREN	-3375	-427.5	55x100
134	INTL	-3300	-427.5	55x100
135	INV1	-3225	-427.5	55x100
136	INV0	-3150	-427.5	55x100
137	DUMMY	-3075	-427.5	55x100
138	DUMMY	-3000	-427.5	55x100
139	DUMMY	-2925	-427.5	55x100
140	DUMMY	-2850	-427.5	55x100
141	VSS1	-2775	-427.5	55x100
142	VSS1	-2700	-427.5	55x100
143	TB	-2625	-427.5	55x100
144	RL	-2550	-427.5	55x100
145	NB	-2475	-427.5	55x100
146	MODE	-2400	-427.5	55x100
147	DINT	-2325	-427.5	55x100
148	FCS	-2250	-427.5	55x100
149	GSQ	-2175	-427.5	55x100
150	TR	-2100	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
151	SIDEN	-2025	-427.5	55x100
152	SID	-1950	-427.5	55x100
153	BISTEN	-1875	-427.5	55x100
154	VSS1	-1800	-427.5	55x100
155	STBYB	-1725	-427.5	55x100
156	RESETB	-1650	-427.5	55x100
157	VSS1	-1575	-427.5	55x100
158	LVD0N	-1500	-427.5	55x100
159	LVD0NR	-1425	-427.5	55x100
160	LVD0P	-1350	-427.5	55x100
161	LVD0PR	-1275	-427.5	55x100
162	LVD1N	-1200	-427.5	55x100
163	LVD1NR	-1125	-427.5	55x100
164	LVD1P	-1050	-427.5	55x100
165	LVD1PR	-975	-427.5	55x100
166	LVCLKN	-900	-427.5	55x100
167	LVCLKNR	-825	-427.5	55x100
168	LVCLKP	-750	-427.5	55x100
169	LVCLKPR	-675	-427.5	55x100
170	LVD2N	-600	-427.5	55x100
171	LVD2NR	-525	-427.5	55x100
172	LVD2P	-450	-427.5	55x100
173	LVD2PR	-375	-427.5	55x100
174	LVD3N	-300	-427.5	55x100
175	LVD3NR	-225	-427.5	55x100
176	LVD3P	-150	-427.5	55x100
177	LVD3PR	-75	-427.5	55x100
178	VSS1	0	-427.5	55x100
179	VSS1	75	-427.5	55x100
180	DE	150	-427.5	55x100
181	VS	225	-427.5	55x100
182	HS	300	-427.5	55x100
183	DCLK	375	-427.5	55x100
184	VSS1	450	-427.5	55x100
185	DR7	525	-427.5	55x100
186	DR6	600	-427.5	55x100
187	DR5	675	-427.5	55x100
188	DR4	750	-427.5	55x100
189	DR3	825	-427.5	55x100
190	DR2	900	-427.5	55x100
191	DR1	975	-427.5	55x100
192	DR0	1050	-427.5	55x100
193	VSS1	1125	-427.5	55x100
194	DG7	1200	-427.5	55x100
195	DG6	1275	-427.5	55x100
196	DG5	1350	-427.5	55x100
197	DG4	1425	-427.5	55x100
198	DG3	1500	-427.5	55x100
199	DG2	1575	-427.5	55x100
200	DG1	1650	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
201	DG0	1725	-427.5	55x100
202	VSS1	1800	-427.5	55x100
203	DB7	1875	-427.5	55x100
204	DB6	1950	-427.5	55x100
205	DB5	2025	-427.5	55x100
206	DB4	2100	-427.5	55x100
207	DB3	2175	-427.5	55x100
208	DB2	2250	-427.5	55x100
209	DB1	2325	-427.5	55x100
210	DB0	2400	-427.5	55x100
211	VSS1	2475	-427.5	55x100
212	VGMPHI	2550	-427.5	55x100
213	VGMPHI	2625	-427.5	55x100
214	VGMPHI	2700	-427.5	55x100
215	VGMPHI	2775	-427.5	55x100
216	VGMPMI	2850	-427.5	55x100
217	VGMPMI	2925	-427.5	55x100
218	VGMPMI	3000	-427.5	55x100
219	VGMPMI	3075	-427.5	55x100
220	VGMPLI	3150	-427.5	55x100
221	VGMPLI	3225	-427.5	55x100
222	VGMPLI	3300	-427.5	55x100
223	VGMPLI	3375	-427.5	55x100
224	VGMNHI	3450	-427.5	55x100
225	VGMNHI	3525	-427.5	55x100
226	VGMNHI	3600	-427.5	55x100
227	VGMNHI	3675	-427.5	55x100
228	VGMNMI	3750	-427.5	55x100
229	VGMNMI	3825	-427.5	55x100
230	VGMNMI	3900	-427.5	55x100
231	VGMNMI	3975	-427.5	55x100
232	VGMNLI	4050	-427.5	55x100
233	VGMNLI	4125	-427.5	55x100
234	VGMNLI	4200	-427.5	55x100
235	VGMNLI	4275	-427.5	55x100
236	DVDD	4350	-427.5	55x100
237	DVDD	4425	-427.5	55x100
238	DVDD	4500	-427.5	55x100
239	DVDD	4575	-427.5	55x100
240	VDDLV	4650	-427.5	55x100
241	VDDLV	4725	-427.5	55x100
242	VDDLV	4800	-427.5	55x100
243	VDDLV	4875	-427.5	55x100
244	VDDLV	4950	-427.5	55x100
245	VSS1	5025	-427.5	55x100
246	VSS1	5100	-427.5	55x100
247	VSS1	5175	-427.5	55x100
248	RTERMEN	5250	-427.5	55x100
249	GPOS1	5325	-427.5	55x100
250	GPOS0	5400	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
251	RS3	5475	-427.5	55x100
252	RS2	5550	-427.5	55x100
253	RS1	5625	-427.5	55x100
254	RS0	5700	-427.5	55x100
255	VSS1	5775	-427.5	55x100
256	VSS1	5850	-427.5	55x100
257	VGMPHO	5925	-427.5	55x100
258	VGMPHO	6000	-427.5	55x100
259	VGMPHO	6075	-427.5	55x100
260	VGMPHO	6150	-427.5	55x100
261	VGMPMO	6225	-427.5	55x100
262	VGMPMO	6300	-427.5	55x100
263	VGMPMO	6375	-427.5	55x100
264	VGMPMO	6450	-427.5	55x100
265	VGMPLO	6525	-427.5	55x100
266	VGMPLO	6600	-427.5	55x100
267	VGMPLO	6675	-427.5	55x100
268	VGMPLO	6750	-427.5	55x100
269	VGMNHO	6825	-427.5	55x100
270	VGMNHO	6900	-427.5	55x100
271	VGMNHO	6975	-427.5	55x100
272	VGMNHO	7050	-427.5	55x100
273	VGMNMO	7125	-427.5	55x100
274	VGMNMO	7200	-427.5	55x100
275	VGMNMO	7275	-427.5	55x100
276	VGMNMO	7350	-427.5	55x100
277	VGMNLO	7425	-427.5	55x100
278	VGMNLO	7500	-427.5	55x100
279	VGMNLO	7575	-427.5	55x100
280	VGMNLO	7650	-427.5	55x100
281	VSDN	7725	-427.5	55x100
282	VSDN	7800	-427.5	55x100
283	VSDN	7875	-427.5	55x100
284	VSDN	7950	-427.5	55x100
285	VSDN	8025	-427.5	55x100
286	VSDN	8100	-427.5	55x100
287	VSSA	8175	-427.5	55x100
288	VSSA	8250	-427.5	55x100
289	VSSA	8325	-427.5	55x100
290	VSSA	8400	-427.5	55x100
291	VSSA	8475	-427.5	55x100
292	VSSA	8550	-427.5	55x100
293	VSDP	8625	-427.5	55x100
294	VSDP	8700	-427.5	55x100
295	VSDP	8775	-427.5	55x100
296	VSDP	8850	-427.5	55x100
297	VSDP	8925	-427.5	55x100
298	VSDP	9000	-427.5	55x100
299	VDD1	9075	-427.5	55x100
300	VDD1	9150	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
301	VDD1	9225	-427.5	55x100
302	VDD1	9300	-427.5	55x100
303	VDD2	9375	-427.5	55x100
304	VDD2	9450	-427.5	55x100
305	VDD2	9525	-427.5	55x100
306	VDD2	9600	-427.5	55x100
307	VSS1	9675	-427.5	55x100
308	VSS1	9750	-427.5	55x100
309	VSS1	9825	-427.5	55x100
310	VSS1	9900	-427.5	55x100
311	VSS2	9975	-427.5	55x100
312	VSS2	10050	-427.5	55x100
313	VSS2	10125	-427.5	55x100
314	VSS2	10200	-427.5	55x100
315	TO0	10275	-427.5	55x100
316	TO0	10350	-427.5	55x100
317	TO1	10425	-427.5	55x100
318	TO1	10500	-427.5	55x100
319	TO2	10575	-427.5	55x100
320	TO2	10650	-427.5	55x100
321	TO3	10725	-427.5	55x100
322	TO3	10800	-427.5	55x100
323	VSS1	10875	-427.5	55x100
324	VSS1	10950	-427.5	55x100
325	VSS1	11025	-427.5	55x100
326	VSS1	11100	-427.5	55x100
327	VSS1	11175	-427.5	55x100
328	VSS1	11250	-427.5	55x100
329	VSS1	11325	-427.5	55x100
330	VSS1	11400	-427.5	55x100
331	VSS1	11475	-427.5	55x100
332	VSS1	11550	-427.5	55x100
333	VSS1	11625	-427.5	55x100
334	VDDOTP	11700	-427.5	55x100
335	VDDOTP	11775	-427.5	55x100
336	VDDOTP	11850	-427.5	55x100
337	VDDOTP	11925	-427.5	55x100
338	THROUGH_2	12000	-427.5	55x100
339	THROUGH_2	12075	-427.5	55x100
340	VCOM	12150	-427.5	55x100
341	VCOM	12225	-427.5	55x100
342	VCOM	12300	-427.5	55x100
343	VCOM_L	12375	-427.5	55x100
344	VCOM_L	12450	-427.5	55x100
345	VCOM_L	12525	-427.5	55x100
346	DUMMY	12600	-427.5	55x100
347	DUMMY	12675	-427.5	55x100
348	DUMMY	12750	-427.5	55x100
349	DUMMY	12825	-427.5	55x100
350	DUMMY	12900	-427.5	55x100

No.	Name	X	Y	Bump size (μm)
351	DUMMY	12975	-427.5	55x100
352	DUMMY	13050	-427.5	55x100
353	DUMMY	13125	-427.5	55x100
354	DUMMY	13200	-427.5	55x100
355	DUMMY	13275	-427.5	55x100
356	GIO_L4	13597.5	-450	100x55
357	DUMMY	13597.5	-375	100x55
358	GIO_L3	13597.5	-300	100x55
359	CA_3	13597.5	-225	100x55
360	DUMMY	13597.5	-150	100x55
361	GIO_L2	13597.5	-75	100x55
362	CA_L2	13597.5	0	100x55
363	DUMMY	13597.5	75	100x55
364	GIO_L1	13597.5	150	100x55
365	CA_L1	13597.5	225	100x55
366	DUMMY	13597.5	300	100x55
367	GIO_L0	13597.5	375	100x55
368	CA_L0	13597.5	450	100x55
369	VSSA	13508	177.5	14x96
370	VSSA	13497	303.5	14x96
371	VSSA	13486	429.5	14x96
372	VCOM_L	13475	177.5	14x96
373	VCOM_L	13464	303.5	14x96
374	VCOM_L	13453	429.5	14x96
375	VCOM_L	13442	177.5	14x96
376	VCOM_L	13431	303.5	14x96
377	VCOM_L	13420	429.5	14x96
378	VSSA	13409	177.5	14x96
379	VSSA	13398	303.5	14x96
380	VSSA	13387	429.5	14x96
381	S1	13376	177.5	14x96
382	S2	13365	303.5	14x96
383	S3	13354	429.5	14x96
384	S4	13343	177.5	14x96
385	S5	13332	303.5	14x96
386	S6	13321	429.5	14x96
387	S7	13310	177.5	14x96
388	S8	13299	303.5	14x96
389	S9	13288	429.5	14x96
390	S10	13277	177.5	14x96
391	S11	13266	303.5	14x96
392	S12	13255	429.5	14x96
393	S13	13244	177.5	14x96
394	S14	13233	303.5	14x96
395	S15	13222	429.5	14x96
396	S16	13211	177.5	14x96
397	S17	13200	303.5	14x96
398	S18	13189	429.5	14x96
399	S19	13178	177.5	14x96
400	S20	13167	303.5	14x96

No.	Name	X	Y	Bump size (μm)
401	S21	13156	429.5	14x96
402	S22	13145	177.5	14x96
403	S23	13134	303.5	14x96
404	S24	13123	429.5	14x96
405	S25	13112	177.5	14x96
406	S26	13101	303.5	14x96
407	S27	13090	429.5	14x96
408	S28	13079	177.5	14x96
409	S29	13068	303.5	14x96
410	S30	13057	429.5	14x96
411	S31	13046	177.5	14x96
412	S32	13035	303.5	14x96
413	S33	13024	429.5	14x96
414	S34	13013	177.5	14x96
415	S35	13002	303.5	14x96
416	S36	12991	429.5	14x96
417	S37	12980	177.5	14x96
418	S38	12969	303.5	14x96
419	S39	12958	429.5	14x96
420	S40	12947	177.5	14x96
421	S41	12936	303.5	14x96
422	S42	12925	429.5	14x96
423	S43	12914	177.5	14x96
424	S44	12903	303.5	14x96
425	S45	12892	429.5	14x96
426	S46	12881	177.5	14x96
427	S47	12870	303.5	14x96
428	S48	12859	429.5	14x96
429	S49	12848	177.5	14x96
430	S50	12837	303.5	14x96
431	S51	12826	429.5	14x96
432	S52	12815	177.5	14x96
433	S53	12804	303.5	14x96
434	S54	12793	429.5	14x96
435	S55	12782	177.5	14x96
436	S56	12771	303.5	14x96
437	S57	12760	429.5	14x96
438	S58	12749	177.5	14x96
439	S59	12738	303.5	14x96
440	S60	12727	429.5	14x96
441	S61	12716	177.5	14x96
442	S62	12705	303.5	14x96
443	S63	12694	429.5	14x96
444	S64	12683	177.5	14x96
445	S65	12672	303.5	14x96
446	S66	12661	429.5	14x96
447	S67	12650	177.5	14x96
448	S68	12639	303.5	14x96
449	S69	12628	429.5	14x96
450	S70	12617	177.5	14x96

No.	Name	X	Y	Bump size (μm)
451	S71	12606	303.5	14x96
452	S72	12595	429.5	14x96
453	S73	12584	177.5	14x96
454	S74	12573	303.5	14x96
455	S75	12562	429.5	14x96
456	S76	12551	177.5	14x96
457	S77	12540	303.5	14x96
458	S78	12529	429.5	14x96
459	S79	12518	177.5	14x96
460	S80	12507	303.5	14x96
461	S81	12496	429.5	14x96
462	S82	12485	177.5	14x96
463	S83	12474	303.5	14x96
464	S84	12463	429.5	14x96
465	S85	12452	177.5	14x96
466	S86	12441	303.5	14x96
467	S87	12430	429.5	14x96
468	S88	12419	177.5	14x96
469	S89	12408	303.5	14x96
470	S90	12397	429.5	14x96
471	S91	12386	177.5	14x96
472	S92	12375	303.5	14x96
473	S93	12364	429.5	14x96
474	S94	12353	177.5	14x96
475	S95	12342	303.5	14x96
476	S96	12331	429.5	14x96
477	S97	12320	177.5	14x96
478	S98	12309	303.5	14x96
479	S99	12298	429.5	14x96
480	S100	12287	177.5	14x96
481	S101	12276	303.5	14x96
482	S102	12265	429.5	14x96
483	S103	12254	177.5	14x96
484	S104	12243	303.5	14x96
485	S105	12232	429.5	14x96
486	S106	12221	177.5	14x96
487	S107	12210	303.5	14x96
488	S108	12199	429.5	14x96
489	S109	12188	177.5	14x96
490	S110	12177	303.5	14x96
491	S111	12166	429.5	14x96
492	S112	12155	177.5	14x96
493	S113	12144	303.5	14x96
494	S114	12133	429.5	14x96
495	S115	12122	177.5	14x96
496	S116	12111	303.5	14x96
497	S117	12100	429.5	14x96
498	S118	12089	177.5	14x96
499	S119	12078	303.5	14x96
500	S120	12067	429.5	14x96

No.	Name	X	Y	Bump size (μm)
501	S121	12056	177.5	14x96
502	S122	12045	303.5	14x96
503	S123	12034	429.5	14x96
504	S124	12023	177.5	14x96
505	S125	12012	303.5	14x96
506	S126	12001	429.5	14x96
507	S127	11990	177.5	14x96
508	S128	11979	303.5	14x96
509	S129	11968	429.5	14x96
510	S130	11957	177.5	14x96
511	S131	11946	303.5	14x96
512	S132	11935	429.5	14x96
513	S133	11924	177.5	14x96
514	S134	11913	303.5	14x96
515	S135	11902	429.5	14x96
516	S136	11891	177.5	14x96
517	S137	11880	303.5	14x96
518	S138	11869	429.5	14x96
519	S139	11858	177.5	14x96
520	S140	11847	303.5	14x96
521	S141	11836	429.5	14x96
522	S142	11825	177.5	14x96
523	S143	11814	303.5	14x96
524	S144	11803	429.5	14x96
525	S145	11792	177.5	14x96
526	S146	11781	303.5	14x96
527	S147	11770	429.5	14x96
528	S148	11759	177.5	14x96
529	S149	11748	303.5	14x96
530	S150	11737	429.5	14x96
531	S151	11726	177.5	14x96
532	S152	11715	303.5	14x96
533	S153	11704	429.5	14x96
534	S154	11693	177.5	14x96
535	S155	11682	303.5	14x96
536	S156	11671	429.5	14x96
537	S157	11660	177.5	14x96
538	S158	11649	303.5	14x96
539	S159	11638	429.5	14x96
540	S160	11627	177.5	14x96
541	S161	11616	303.5	14x96
542	S162	11605	429.5	14x96
543	S163	11594	177.5	14x96
544	S164	11583	303.5	14x96
545	S165	11572	429.5	14x96
546	S166	11561	177.5	14x96
547	S167	11550	303.5	14x96
548	S168	11539	429.5	14x96
549	S169	11528	177.5	14x96
550	S170	11517	303.5	14x96

No.	Name	X	Y	Bump size (μm)
551	S171	11506	429.5	14x96
552	S172	11495	177.5	14x96
553	S173	11484	303.5	14x96
554	S174	11473	429.5	14x96
555	S175	11462	177.5	14x96
556	S176	11451	303.5	14x96
557	S177	11440	429.5	14x96
558	S178	11429	177.5	14x96
559	S179	11418	303.5	14x96
560	S180	11407	429.5	14x96
561	S181	11396	177.5	14x96
562	S182	11385	303.5	14x96
563	S183	11374	429.5	14x96
564	S184	11363	177.5	14x96
565	S185	11352	303.5	14x96
566	S186	11341	429.5	14x96
567	S187	11330	177.5	14x96
568	S188	11319	303.5	14x96
569	S189	11308	429.5	14x96
570	S190	11297	177.5	14x96
571	S191	11286	303.5	14x96
572	S192	11275	429.5	14x96
573	S193	11264	177.5	14x96
574	S194	11253	303.5	14x96
575	S195	11242	429.5	14x96
576	S196	11231	177.5	14x96
577	S197	11220	303.5	14x96
578	S198	11209	429.5	14x96
579	S199	11198	177.5	14x96
580	S200	11187	303.5	14x96
581	S201	11176	429.5	14x96
582	S202	11165	177.5	14x96
583	S203	11154	303.5	14x96
584	S204	11143	429.5	14x96
585	S205	11132	177.5	14x96
586	S206	11121	303.5	14x96
587	S207	11110	429.5	14x96
588	S208	11099	177.5	14x96
589	S209	11088	303.5	14x96
590	S210	11077	429.5	14x96
591	S211	11066	177.5	14x96
592	S212	11055	303.5	14x96
593	S213	11044	429.5	14x96
594	S214	11033	177.5	14x96
595	S215	11022	303.5	14x96
596	S216	11011	429.5	14x96
597	S217	11000	177.5	14x96
598	S218	10989	303.5	14x96
599	S219	10978	429.5	14x96
600	S220	10967	177.5	14x96

No.	Name	X	Y	Bump size (μm)
601	S221	10956	303.5	14x96
602	S222	10945	429.5	14x96
603	S223	10934	177.5	14x96
604	S224	10923	303.5	14x96
605	S225	10912	429.5	14x96
606	S226	10901	177.5	14x96
607	S227	10890	303.5	14x96
608	S228	10879	429.5	14x96
609	S229	10868	177.5	14x96
610	S230	10857	303.5	14x96
611	S231	10846	429.5	14x96
612	S232	10835	177.5	14x96
613	S233	10824	303.5	14x96
614	S234	10813	429.5	14x96
615	S235	10802	177.5	14x96
616	S236	10791	303.5	14x96
617	S237	10780	429.5	14x96
618	S238	10769	177.5	14x96
619	S239	10758	303.5	14x96
620	S240	10747	429.5	14x96
621	S241	10736	177.5	14x96
622	S242	10725	303.5	14x96
623	S243	10714	429.5	14x96
624	S244	10703	177.5	14x96
625	S245	10692	303.5	14x96
626	S246	10681	429.5	14x96
627	S247	10670	177.5	14x96
628	S248	10659	303.5	14x96
629	S249	10648	429.5	14x96
630	S250	10637	177.5	14x96
631	S251	10626	303.5	14x96
632	S252	10615	429.5	14x96
633	S253	10604	177.5	14x96
634	S254	10593	303.5	14x96
635	S255	10582	429.5	14x96
636	S256	10571	177.5	14x96
637	S257	10560	303.5	14x96
638	S258	10549	429.5	14x96
639	S259	10538	177.5	14x96
640	S260	10527	303.5	14x96
641	S261	10516	429.5	14x96
642	S262	10505	177.5	14x96
643	S263	10494	303.5	14x96
644	S264	10483	429.5	14x96
645	S265	10472	177.5	14x96
646	S266	10461	303.5	14x96
647	S267	10450	429.5	14x96
648	S268	10439	177.5	14x96
649	S269	10428	303.5	14x96
650	S270	10417	429.5	14x96

No.	Name	X	Y	Bump size (μm)
651	S271	10406	177.5	14x96
652	S272	10395	303.5	14x96
653	S273	10384	429.5	14x96
654	S274	10373	177.5	14x96
655	S275	10362	303.5	14x96
656	S276	10351	429.5	14x96
657	S277	10340	177.5	14x96
658	S278	10329	303.5	14x96
659	S279	10318	429.5	14x96
660	S280	10307	177.5	14x96
661	S281	10296	303.5	14x96
662	S282	10285	429.5	14x96
663	S283	10274	177.5	14x96
664	S284	10263	303.5	14x96
665	S285	10252	429.5	14x96
666	S286	10241	177.5	14x96
667	S287	10230	303.5	14x96
668	S288	10219	429.5	14x96
669	S289	10208	177.5	14x96
670	S290	10197	303.5	14x96
671	S291	10186	429.5	14x96
672	S292	10175	177.5	14x96
673	S293	10164	303.5	14x96
674	S294	10153	429.5	14x96
675	S295	10142	177.5	14x96
676	S296	10131	303.5	14x96
677	S297	10120	429.5	14x96
678	S298	10109	177.5	14x96
679	S299	10098	303.5	14x96
680	S300	10087	429.5	14x96
681	S301	10076	177.5	14x96
682	S302	10065	303.5	14x96
683	S303	10054	429.5	14x96
684	S304	10043	177.5	14x96
685	S305	10032	303.5	14x96
686	S306	10021	429.5	14x96
687	S307	10010	177.5	14x96
688	S308	9999	303.5	14x96
689	S309	9988	429.5	14x96
690	S310	9977	177.5	14x96
691	S311	9966	303.5	14x96
692	S312	9955	429.5	14x96
693	S313	9944	177.5	14x96
694	S314	9933	303.5	14x96
695	S315	9922	429.5	14x96
696	S316	9911	177.5	14x96
697	S317	9900	303.5	14x96
698	S318	9889	429.5	14x96
699	S319	9878	177.5	14x96
700	S320	9867	303.5	14x96

No.	Name	X	Y	Bump size (μm)
701	S321	9856	429.5	14x96
702	S322	9845	177.5	14x96
703	S323	9834	303.5	14x96
704	S324	9823	429.5	14x96
705	S325	9812	177.5	14x96
706	S326	9801	303.5	14x96
707	S327	9790	429.5	14x96
708	S328	9779	177.5	14x96
709	S329	9768	303.5	14x96
710	S330	9757	429.5	14x96
711	S331	9746	177.5	14x96
712	S332	9735	303.5	14x96
713	S333	9724	429.5	14x96
714	S334	9713	177.5	14x96
715	S335	9702	303.5	14x96
716	S336	9691	429.5	14x96
717	S337	9680	177.5	14x96
718	S338	9669	303.5	14x96
719	S339	9658	429.5	14x96
720	S340	9647	177.5	14x96
721	S341	9636	303.5	14x96
722	S342	9625	429.5	14x96
723	S343	9614	177.5	14x96
724	S344	9603	303.5	14x96
725	S345	9592	429.5	14x96
726	S346	9581	177.5	14x96
727	S347	9570	303.5	14x96
728	S348	9559	429.5	14x96
729	S349	9548	177.5	14x96
730	S350	9537	303.5	14x96
731	S351	9526	429.5	14x96
732	S352	9515	177.5	14x96
733	S353	9504	303.5	14x96
734	S354	9493	429.5	14x96
735	S355	9482	177.5	14x96
736	S356	9471	303.5	14x96
737	S357	9460	429.5	14x96
738	S358	9449	177.5	14x96
739	S359	9438	303.5	14x96
740	S360	9427	429.5	14x96
741	S361	9416	177.5	14x96
742	S362	9405	303.5	14x96
743	S363	9394	429.5	14x96
744	S364	9383	177.5	14x96
745	S365	9372	303.5	14x96
746	S366	9361	429.5	14x96
747	S367	9350	177.5	14x96
748	S368	9339	303.5	14x96
749	S369	9328	429.5	14x96
750	S370	9317	177.5	14x96

No.	Name	X	Y	Bump size (μm)
751	S371	9306	303.5	14x96
752	S372	9295	429.5	14x96
753	S373	9284	177.5	14x96
754	S374	9273	303.5	14x96
755	S375	9262	429.5	14x96
756	S376	9251	177.5	14x96
757	S377	9240	303.5	14x96
758	S378	9229	429.5	14x96
759	S379	9218	177.5	14x96
760	S380	9207	303.5	14x96
761	S381	9196	429.5	14x96
762	S382	9185	177.5	14x96
763	S383	9174	303.5	14x96
764	S384	9163	429.5	14x96
765	S385	9152	177.5	14x96
766	S386	9141	303.5	14x96
767	S387	9130	429.5	14x96
768	S388	9119	177.5	14x96
769	S389	9108	303.5	14x96
770	S390	9097	429.5	14x96
771	S391	9086	177.5	14x96
772	S392	9075	303.5	14x96
773	S393	9064	429.5	14x96
774	S394	9053	177.5	14x96
775	S395	9042	303.5	14x96
776	S396	9031	429.5	14x96
777	S397	9020	177.5	14x96
778	S398	9009	303.5	14x96
779	S399	8998	429.5	14x96
780	S400	8987	177.5	14x96
781	S401	8976	303.5	14x96
782	S402	8965	429.5	14x96
783	S403	8954	177.5	14x96
784	S404	8943	303.5	14x96
785	S405	8932	429.5	14x96
786	S406	8921	177.5	14x96
787	S407	8910	303.5	14x96
788	S408	8899	429.5	14x96
789	S409	8888	177.5	14x96
790	S410	8877	303.5	14x96
791	S411	8866	429.5	14x96
792	S412	8855	177.5	14x96
793	S413	8844	303.5	14x96
794	S414	8833	429.5	14x96
795	S415	8822	177.5	14x96
796	S416	8811	303.5	14x96
797	S417	8800	429.5	14x96
798	S418	8789	177.5	14x96
799	S419	8778	303.5	14x96
800	S420	8767	429.5	14x96

No.	Name	X	Y	Bump size (μm)
801	S421	8756	177.5	14x96
802	S422	8745	303.5	14x96
803	S423	8734	429.5	14x96
804	S424	8723	177.5	14x96
805	S425	8712	303.5	14x96
806	S426	8701	429.5	14x96
807	S427	8690	177.5	14x96
808	S428	8679	303.5	14x96
809	S429	8668	429.5	14x96
810	S430	8657	177.5	14x96
811	S431	8646	303.5	14x96
812	S432	8635	429.5	14x96
813	S433	8624	177.5	14x96
814	S434	8613	303.5	14x96
815	S435	8602	429.5	14x96
816	S436	8591	177.5	14x96
817	S437	8580	303.5	14x96
818	S438	8569	429.5	14x96
819	S439	8558	177.5	14x96
820	S440	8547	303.5	14x96
821	S441	8536	429.5	14x96
822	S442	8525	177.5	14x96
823	S443	8514	303.5	14x96
824	S444	8503	429.5	14x96
825	S445	8492	177.5	14x96
826	S446	8481	303.5	14x96
827	S447	8470	429.5	14x96
828	S448	8459	177.5	14x96
829	S449	8448	303.5	14x96
830	S450	8437	429.5	14x96
831	S451	8426	177.5	14x96
832	S452	8415	303.5	14x96
833	S453	8404	429.5	14x96
834	S454	8393	177.5	14x96
835	S455	8382	303.5	14x96
836	S456	8371	429.5	14x96
837	S457	8360	177.5	14x96
838	S458	8349	303.5	14x96
839	S459	8338	429.5	14x96
840	S460	8327	177.5	14x96
841	S461	8316	303.5	14x96
842	S462	8305	429.5	14x96
843	S463	8294	177.5	14x96
844	S464	8283	303.5	14x96
845	S465	8272	429.5	14x96
846	S466	8261	177.5	14x96
847	S467	8250	303.5	14x96
848	S468	8239	429.5	14x96
849	S469	8228	177.5	14x96
850	S470	8217	303.5	14x96

No.	Name	X	Y	Bump size (μm)
851	S471	8206	429.5	14x96
852	S472	8195	177.5	14x96
853	S473	8184	303.5	14x96
854	S474	8173	429.5	14x96
855	S475	8162	177.5	14x96
856	S476	8151	303.5	14x96
857	S477	8140	429.5	14x96
858	S478	8129	177.5	14x96
859	S479	8118	303.5	14x96
860	S480	8107	429.5	14x96
861	S481	8096	177.5	14x96
862	S482	8085	303.5	14x96
863	S483	8074	429.5	14x96
864	S484	8063	177.5	14x96
865	S485	8052	303.5	14x96
866	S486	8041	429.5	14x96
867	S487	8030	177.5	14x96
868	S488	8019	303.5	14x96
869	S489	8008	429.5	14x96
870	S490	7997	177.5	14x96
871	S491	7986	303.5	14x96
872	S492	7975	429.5	14x96
873	S493	7964	177.5	14x96
874	S494	7953	303.5	14x96
875	S495	7942	429.5	14x96
876	S496	7931	177.5	14x96
877	S497	7920	303.5	14x96
878	S498	7909	429.5	14x96
879	S499	7898	177.5	14x96
880	S500	7887	303.5	14x96
881	S501	7876	429.5	14x96
882	S502	7865	177.5	14x96
883	S503	7854	303.5	14x96
884	S504	7843	429.5	14x96
885	S505	7832	177.5	14x96
886	S506	7821	303.5	14x96
887	S507	7810	429.5	14x96
888	S508	7799	177.5	14x96
889	S509	7788	303.5	14x96
890	S510	7777	429.5	14x96
891	S511	7766	177.5	14x96
892	S512	7755	303.5	14x96
893	S513	7744	429.5	14x96
894	S514	7733	177.5	14x96
895	S515	7722	303.5	14x96
896	S516	7711	429.5	14x96
897	S517	7700	177.5	14x96
898	S518	7689	303.5	14x96
899	S519	7678	429.5	14x96
900	S520	7667	177.5	14x96

No.	Name	X	Y	Bump size (μm)
901	S521	7656	303.5	14x96
902	S522	7645	429.5	14x96
903	S523	7634	177.5	14x96
904	S524	7623	303.5	14x96
905	S525	7612	429.5	14x96
906	S526	7601	177.5	14x96
907	S527	7590	303.5	14x96
908	S528	7579	429.5	14x96
909	S529	7568	177.5	14x96
910	S530	7557	303.5	14x96
911	S531	7546	429.5	14x96
912	S532	7535	177.5	14x96
913	S533	7524	303.5	14x96
914	S534	7513	429.5	14x96
915	S535	7502	177.5	14x96
916	S536	7491	303.5	14x96
917	S537	7480	429.5	14x96
918	S538	7469	177.5	14x96
919	S539	7458	303.5	14x96
920	S540	7447	429.5	14x96
921	S541	7436	177.5	14x96
922	S542	7425	303.5	14x96
923	S543	7414	429.5	14x96
924	S544	7403	177.5	14x96
925	S545	7392	303.5	14x96
926	S546	7381	429.5	14x96
927	S547	7370	177.5	14x96
928	S548	7359	303.5	14x96
929	S549	7348	429.5	14x96
930	S550	7337	177.5	14x96
931	S551	7326	303.5	14x96
932	S552	7315	429.5	14x96
933	S553	7304	177.5	14x96
934	S554	7293	303.5	14x96
935	S555	7282	429.5	14x96
936	S556	7271	177.5	14x96
937	S557	7260	303.5	14x96
938	S558	7249	429.5	14x96
939	S559	7238	177.5	14x96
940	S560	7227	303.5	14x96
941	S561	7216	429.5	14x96
942	S562	7205	177.5	14x96
943	S563	7194	303.5	14x96
944	S564	7183	429.5	14x96
945	S565	7172	177.5	14x96
946	S566	7161	303.5	14x96
947	S567	7150	429.5	14x96
948	S568	7139	177.5	14x96
949	S569	7128	303.5	14x96
950	S570	7117	429.5	14x96

No.	Name	X	Y	Bump size (μm)
951	S571	7106	177.5	14x96
952	S572	7095	303.5	14x96
953	S573	7084	429.5	14x96
954	S574	7073	177.5	14x96
955	S575	7062	303.5	14x96
956	S576	7051	429.5	14x96
957	S577	7040	177.5	14x96
958	S578	7029	303.5	14x96
959	S579	7018	429.5	14x96
960	S580	7007	177.5	14x96
961	S581	6996	303.5	14x96
962	S582	6985	429.5	14x96
963	S583	6974	177.5	14x96
964	S584	6963	303.5	14x96
965	S585	6952	429.5	14x96
966	S586	6941	177.5	14x96
967	S587	6930	303.5	14x96
968	S588	6919	429.5	14x96
969	S589	6908	177.5	14x96
970	S590	6897	303.5	14x96
971	S591	6886	429.5	14x96
972	S592	6875	177.5	14x96
973	S593	6864	303.5	14x96
974	S594	6853	429.5	14x96
975	S595	6842	177.5	14x96
976	S596	6831	303.5	14x96
977	S597	6820	429.5	14x96
978	S598	6809	177.5	14x96
979	S599	6798	303.5	14x96
980	S600	6787	429.5	14x96
981	S601	6776	177.5	14x96
982	S602	6765	303.5	14x96
983	S603	6754	429.5	14x96
984	S604	6743	177.5	14x96
985	S605	6732	303.5	14x96
986	S606	6721	429.5	14x96
987	S607	6710	177.5	14x96
988	S608	6699	303.5	14x96
989	S609	6688	429.5	14x96
990	S610	6677	177.5	14x96
991	S611	6666	303.5	14x96
992	S612	6655	429.5	14x96
993	S613	6644	177.5	14x96
994	S614	6633	303.5	14x96
995	S615	6622	429.5	14x96
996	S616	6611	177.5	14x96
997	S617	6600	303.5	14x96
998	S618	6589	429.5	14x96
999	S619	6578	177.5	14x96
1000	S620	6567	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1001	S621	6556	429.5	14x96
1002	S622	6545	177.5	14x96
1003	S623	6534	303.5	14x96
1004	S624	6523	429.5	14x96
1005	S625	6512	177.5	14x96
1006	S626	6501	303.5	14x96
1007	S627	6490	429.5	14x96
1008	S628	6479	177.5	14x96
1009	S629	6468	303.5	14x96
1010	S630	6457	429.5	14x96
1011	S631	6446	177.5	14x96
1012	S632	6435	303.5	14x96
1013	S633	6424	429.5	14x96
1014	S634	6413	177.5	14x96
1015	S635	6402	303.5	14x96
1016	S636	6391	429.5	14x96
1017	S637	6380	177.5	14x96
1018	S638	6369	303.5	14x96
1019	S639	6358	429.5	14x96
1020	S640	6347	177.5	14x96
1021	S641	6336	303.5	14x96
1022	S642	6325	429.5	14x96
1023	S643	6314	177.5	14x96
1024	S644	6303	303.5	14x96
1025	S645	6292	429.5	14x96
1026	S646	6281	177.5	14x96
1027	S647	6270	303.5	14x96
1028	S648	6259	429.5	14x96
1029	S649	6248	177.5	14x96
1030	S650	6237	303.5	14x96
1031	S651	6226	429.5	14x96
1032	S652	6215	177.5	14x96
1033	S653	6204	303.5	14x96
1034	S654	6193	429.5	14x96
1035	S655	6182	177.5	14x96
1036	S656	6171	303.5	14x96
1037	S657	6160	429.5	14x96
1038	S658	6149	177.5	14x96
1039	S659	6138	303.5	14x96
1040	S660	6127	429.5	14x96
1041	S661	6116	177.5	14x96
1042	S662	6105	303.5	14x96
1043	S663	6094	429.5	14x96
1044	S664	6083	177.5	14x96
1045	S665	6072	303.5	14x96
1046	S666	6061	429.5	14x96
1047	S667	6050	177.5	14x96
1048	S668	6039	303.5	14x96
1049	S669	6028	429.5	14x96
1050	S670	6017	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1051	S671	6006	303.5	14x96
1052	S672	5995	429.5	14x96
1053	S673	5984	177.5	14x96
1054	S674	5973	303.5	14x96
1055	S675	5962	429.5	14x96
1056	S676	5951	177.5	14x96
1057	S677	5940	303.5	14x96
1058	S678	5929	429.5	14x96
1059	S679	5918	177.5	14x96
1060	S680	5907	303.5	14x96
1061	S681	5896	429.5	14x96
1062	S682	5885	177.5	14x96
1063	S683	5874	303.5	14x96
1064	S684	5863	429.5	14x96
1065	S685	5852	177.5	14x96
1066	S686	5841	303.5	14x96
1067	S687	5830	429.5	14x96
1068	S688	5819	177.5	14x96
1069	S689	5808	303.5	14x96
1070	S690	5797	429.5	14x96
1071	S691	5786	177.5	14x96
1072	S692	5775	303.5	14x96
1073	S693	5764	429.5	14x96
1074	S694	5753	177.5	14x96
1075	S695	5742	303.5	14x96
1076	S696	5731	429.5	14x96
1077	S697	5720	177.5	14x96
1078	S698	5709	303.5	14x96
1079	S699	5698	429.5	14x96
1080	S700	5687	177.5	14x96
1081	S701	5676	303.5	14x96
1082	S702	5665	429.5	14x96
1083	S703	5654	177.5	14x96
1084	S704	5643	303.5	14x96
1085	S705	5632	429.5	14x96
1086	S706	5621	177.5	14x96
1087	S707	5610	303.5	14x96
1088	S708	5599	429.5	14x96
1089	S709	5588	177.5	14x96
1090	S710	5577	303.5	14x96
1091	S711	5566	429.5	14x96
1092	S712	5555	177.5	14x96
1093	S713	5544	303.5	14x96
1094	S714	5533	429.5	14x96
1095	S715	5522	177.5	14x96
1096	S716	5511	303.5	14x96
1097	S717	5500	429.5	14x96
1098	S718	5489	177.5	14x96
1099	S719	5478	303.5	14x96
1100	S720	5467	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1101	S721	5456	177.5	14x96
1102	S722	5445	303.5	14x96
1103	S723	5434	429.5	14x96
1104	S724	5423	177.5	14x96
1105	S725	5412	303.5	14x96
1106	S726	5401	429.5	14x96
1107	S727	5390	177.5	14x96
1108	S728	5379	303.5	14x96
1109	S729	5368	429.5	14x96
1110	S730	5357	177.5	14x96
1111	S731	5346	303.5	14x96
1112	S732	5335	429.5	14x96
1113	S733	5324	177.5	14x96
1114	S734	5313	303.5	14x96
1115	S735	5302	429.5	14x96
1116	S736	5291	177.5	14x96
1117	S737	5280	303.5	14x96
1118	S738	5269	429.5	14x96
1119	S739	5258	177.5	14x96
1120	S740	5247	303.5	14x96
1121	S741	5236	429.5	14x96
1122	S742	5225	177.5	14x96
1123	S743	5214	303.5	14x96
1124	S744	5203	429.5	14x96
1125	S745	5192	177.5	14x96
1126	S746	5181	303.5	14x96
1127	S747	5170	429.5	14x96
1128	S748	5159	177.5	14x96
1129	S749	5148	303.5	14x96
1130	S750	5137	429.5	14x96
1131	S751	5126	177.5	14x96
1132	S752	5115	303.5	14x96
1133	S753	5104	429.5	14x96
1134	S754	5093	177.5	14x96
1135	S755	5082	303.5	14x96
1136	S756	5071	429.5	14x96
1137	S757	5060	177.5	14x96
1138	S758	5049	303.5	14x96
1139	S759	5038	429.5	14x96
1140	S760	5027	177.5	14x96
1141	S761	5016	303.5	14x96
1142	S762	5005	429.5	14x96
1143	S763	4994	177.5	14x96
1144	S764	4983	303.5	14x96
1145	S765	4972	429.5	14x96
1146	S766	4961	177.5	14x96
1147	S767	4950	303.5	14x96
1148	S768	4939	429.5	14x96
1149	S769	4928	177.5	14x96
1150	S770	4917	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1151	S771	4906	429.5	14x96
1152	S772	4895	177.5	14x96
1153	S773	4884	303.5	14x96
1154	S774	4873	429.5	14x96
1155	S775	4862	177.5	14x96
1156	S776	4851	303.5	14x96
1157	S777	4840	429.5	14x96
1158	S778	4829	177.5	14x96
1159	S779	4818	303.5	14x96
1160	S780	4807	429.5	14x96
1161	S781	4796	177.5	14x96
1162	S782	4785	303.5	14x96
1163	S783	4774	429.5	14x96
1164	S784	4763	177.5	14x96
1165	S785	4752	303.5	14x96
1166	S786	4741	429.5	14x96
1167	S787	4730	177.5	14x96
1168	S788	4719	303.5	14x96
1169	S789	4708	429.5	14x96
1170	S790	4697	177.5	14x96
1171	S791	4686	303.5	14x96
1172	S792	4675	429.5	14x96
1173	S793	4664	177.5	14x96
1174	S794	4653	303.5	14x96
1175	S795	4642	429.5	14x96
1176	S796	4631	177.5	14x96
1177	S797	4620	303.5	14x96
1178	S798	4609	429.5	14x96
1179	S799	4598	177.5	14x96
1180	S800	4587	303.5	14x96
1181	S801	4576	429.5	14x96
1182	S802	4565	177.5	14x96
1183	S803	4554	303.5	14x96
1184	S804	4543	429.5	14x96
1185	S805	4532	177.5	14x96
1186	S806	4521	303.5	14x96
1187	S807	4510	429.5	14x96
1188	S808	4499	177.5	14x96
1189	S809	4488	303.5	14x96
1190	S810	4477	429.5	14x96
1191	S811	4466	177.5	14x96
1192	S812	4455	303.5	14x96
1193	S813	4444	429.5	14x96
1194	S814	4433	177.5	14x96
1195	S815	4422	303.5	14x96
1196	S816	4411	429.5	14x96
1197	S817	4400	177.5	14x96
1198	S818	4389	303.5	14x96
1199	S819	4378	429.5	14x96
1200	S820	4367	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1201	S821	4356	303.5	14x96
1202	S822	4345	429.5	14x96
1203	S823	4334	177.5	14x96
1204	S824	4323	303.5	14x96
1205	S825	4312	429.5	14x96
1206	S826	4301	177.5	14x96
1207	S827	4290	303.5	14x96
1208	S828	4279	429.5	14x96
1209	S829	4268	177.5	14x96
1210	S830	4257	303.5	14x96
1211	S831	4246	429.5	14x96
1212	S832	4235	177.5	14x96
1213	S833	4224	303.5	14x96
1214	S834	4213	429.5	14x96
1215	S835	4202	177.5	14x96
1216	S836	4191	303.5	14x96
1217	S837	4180	429.5	14x96
1218	S838	4169	177.5	14x96
1219	S839	4158	303.5	14x96
1220	S840	4147	429.5	14x96
1221	S841	4136	177.5	14x96
1222	S842	4125	303.5	14x96
1223	S843	4114	429.5	14x96
1224	S844	4103	177.5	14x96
1225	S845	4092	303.5	14x96
1226	S846	4081	429.5	14x96
1227	S847	4070	177.5	14x96
1228	S848	4059	303.5	14x96
1229	S849	4048	429.5	14x96
1230	S850	4037	177.5	14x96
1231	S851	4026	303.5	14x96
1232	S852	4015	429.5	14x96
1233	S853	4004	177.5	14x96
1234	S854	3993	303.5	14x96
1235	S855	3982	429.5	14x96
1236	S856	3971	177.5	14x96
1237	S857	3960	303.5	14x96
1238	S858	3949	429.5	14x96
1239	S859	3938	177.5	14x96
1240	S860	3927	303.5	14x96
1241	S861	3916	429.5	14x96
1242	S862	3905	177.5	14x96
1243	S863	3894	303.5	14x96
1244	S864	3883	429.5	14x96
1245	S865	3872	177.5	14x96
1246	S866	3861	303.5	14x96
1247	S867	3850	429.5	14x96
1248	S868	3839	177.5	14x96
1249	S869	3828	303.5	14x96
1250	S870	3817	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1251	S871	3806	177.5	14x96
1252	S872	3795	303.5	14x96
1253	S873	3784	429.5	14x96
1254	S874	3773	177.5	14x96
1255	S875	3762	303.5	14x96
1256	S876	3751	429.5	14x96
1257	S877	3740	177.5	14x96
1258	S878	3729	303.5	14x96
1259	S879	3718	429.5	14x96
1260	S880	3707	177.5	14x96
1261	S881	3696	303.5	14x96
1262	S882	3685	429.5	14x96
1263	S883	3674	177.5	14x96
1264	S884	3663	303.5	14x96
1265	S885	3652	429.5	14x96
1266	S886	3641	177.5	14x96
1267	S887	3630	303.5	14x96
1268	S888	3619	429.5	14x96
1269	S889	3608	177.5	14x96
1270	S890	3597	303.5	14x96
1271	S891	3586	429.5	14x96
1272	S892	3575	177.5	14x96
1273	S893	3564	303.5	14x96
1274	S894	3553	429.5	14x96
1275	S895	3542	177.5	14x96
1276	S896	3531	303.5	14x96
1277	S897	3520	429.5	14x96
1278	S898	3509	177.5	14x96
1279	S899	3498	303.5	14x96
1280	S900	3487	429.5	14x96
1281	S901	3476	177.5	14x96
1282	S902	3465	303.5	14x96
1283	S903	3454	429.5	14x96
1284	S904	3443	177.5	14x96
1285	S905	3432	303.5	14x96
1286	S906	3421	429.5	14x96
1287	S907	3410	177.5	14x96
1288	S908	3399	303.5	14x96
1289	S909	3388	429.5	14x96
1290	S910	3377	177.5	14x96
1291	S911	3366	303.5	14x96
1292	S912	3355	429.5	14x96
1293	S913	3344	177.5	14x96
1294	S914	3333	303.5	14x96
1295	S915	3322	429.5	14x96
1296	S916	3311	177.5	14x96
1297	S917	3300	303.5	14x96
1298	S918	3289	429.5	14x96
1299	S919	3278	177.5	14x96
1300	S920	3267	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1301	S921	3256	429.5	14x96
1302	S922	3245	177.5	14x96
1303	S923	3234	303.5	14x96
1304	S924	3223	429.5	14x96
1305	S925	3212	177.5	14x96
1306	S926	3201	303.5	14x96
1307	S927	3190	429.5	14x96
1308	S928	3179	177.5	14x96
1309	S929	3168	303.5	14x96
1310	S930	3157	429.5	14x96
1311	S931	3146	177.5	14x96
1312	S932	3135	303.5	14x96
1313	S933	3124	429.5	14x96
1314	S934	3113	177.5	14x96
1315	S935	3102	303.5	14x96
1316	S936	3091	429.5	14x96
1317	S937	3080	177.5	14x96
1318	S938	3069	303.5	14x96
1319	S939	3058	429.5	14x96
1320	S940	3047	177.5	14x96
1321	S941	3036	303.5	14x96
1322	S942	3025	429.5	14x96
1323	S943	3014	177.5	14x96
1324	S944	3003	303.5	14x96
1325	S945	2992	429.5	14x96
1326	S946	2981	177.5	14x96
1327	S947	2970	303.5	14x96
1328	S948	2959	429.5	14x96
1329	S949	2948	177.5	14x96
1330	S950	2937	303.5	14x96
1331	S951	2926	429.5	14x96
1332	S952	2915	177.5	14x96
1333	S953	2904	303.5	14x96
1334	S954	2893	429.5	14x96
1335	S955	2882	177.5	14x96
1336	S956	2871	303.5	14x96
1337	S957	2860	429.5	14x96
1338	S958	2849	177.5	14x96
1339	S959	2838	303.5	14x96
1340	S960	2827	429.5	14x96
1341	S961	2816	177.5	14x96
1342	S962	2805	303.5	14x96
1343	S963	2794	429.5	14x96
1344	S964	2783	177.5	14x96
1345	S965	2772	303.5	14x96
1346	S966	2761	429.5	14x96
1347	S967	2750	177.5	14x96
1348	S968	2739	303.5	14x96
1349	S969	2728	429.5	14x96
1350	S970	2717	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1351	S971	2706	303.5	14x96
1352	S972	2695	429.5	14x96
1353	S973	2684	177.5	14x96
1354	S974	2673	303.5	14x96
1355	S975	2662	429.5	14x96
1356	S976	2651	177.5	14x96
1357	S977	2640	303.5	14x96
1358	S978	2629	429.5	14x96
1359	S979	2618	177.5	14x96
1360	S980	2607	303.5	14x96
1361	S981	2596	429.5	14x96
1362	S982	2585	177.5	14x96
1363	S983	2574	303.5	14x96
1364	S984	2563	429.5	14x96
1365	S985	2552	177.5	14x96
1366	S986	2541	303.5	14x96
1367	S987	2530	429.5	14x96
1368	S988	2519	177.5	14x96
1369	S989	2508	303.5	14x96
1370	S990	2497	429.5	14x96
1371	S991	2486	177.5	14x96
1372	S992	2475	303.5	14x96
1373	S993	2464	429.5	14x96
1374	S994	2453	177.5	14x96
1375	S995	2442	303.5	14x96
1376	S996	2431	429.5	14x96
1377	S997	2420	177.5	14x96
1378	S998	2409	303.5	14x96
1379	S999	2398	429.5	14x96
1380	S1000	2387	177.5	14x96
1381	S1001	2376	303.5	14x96
1382	S1002	2365	429.5	14x96
1383	S1003	2354	177.5	14x96
1384	S1004	2343	303.5	14x96
1385	S1005	2332	429.5	14x96
1386	S1006	2321	177.5	14x96
1387	S1007	2310	303.5	14x96
1388	S1008	2299	429.5	14x96
1389	S1009	2288	177.5	14x96
1390	S1010	2277	303.5	14x96
1391	S1011	2266	429.5	14x96
1392	S1012	2255	177.5	14x96
1393	S1013	2244	303.5	14x96
1394	S1014	2233	429.5	14x96
1395	S1015	2222	177.5	14x96
1396	S1016	2211	303.5	14x96
1397	S1017	2200	429.5	14x96
1398	S1018	2189	177.5	14x96
1399	S1019	2178	303.5	14x96
1400	S1020	2167	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1401	S1021	2156	177.5	14x96
1402	S1022	2145	303.5	14x96
1403	S1023	2134	429.5	14x96
1404	S1024	2123	177.5	14x96
1405	S1025	2112	303.5	14x96
1406	S1026	2101	429.5	14x96
1407	S1027	2090	177.5	14x96
1408	S1028	2079	303.5	14x96
1409	S1029	2068	429.5	14x96
1410	S1030	2057	177.5	14x96
1411	S1031	2046	303.5	14x96
1412	S1032	2035	429.5	14x96
1413	S1033	2024	177.5	14x96
1414	S1034	2013	303.5	14x96
1415	S1035	2002	429.5	14x96
1416	S1036	1991	177.5	14x96
1417	S1037	1980	303.5	14x96
1418	S1038	1969	429.5	14x96
1419	S1039	1958	177.5	14x96
1420	S1040	1947	303.5	14x96
1421	S1041	1936	429.5	14x96
1422	S1042	1925	177.5	14x96
1423	S1043	1914	303.5	14x96
1424	S1044	1903	429.5	14x96
1425	S1045	1892	177.5	14x96
1426	S1046	1881	303.5	14x96
1427	S1047	1870	429.5	14x96
1428	S1048	1859	177.5	14x96
1429	S1049	1848	303.5	14x96
1430	S1050	1837	429.5	14x96
1431	S1051	1826	177.5	14x96
1432	S1052	1815	303.5	14x96
1433	S1053	1804	429.5	14x96
1434	S1054	1793	177.5	14x96
1435	S1055	1782	303.5	14x96
1436	S1056	1771	429.5	14x96
1437	S1057	1760	177.5	14x96
1438	S1058	1749	303.5	14x96
1439	S1059	1738	429.5	14x96
1440	S1060	1727	177.5	14x96
1441	S1061	1716	303.5	14x96
1442	S1062	1705	429.5	14x96
1443	S1063	1694	177.5	14x96
1444	S1064	1683	303.5	14x96
1445	S1065	1672	429.5	14x96
1446	S1066	1661	177.5	14x96
1447	S1067	1650	303.5	14x96
1448	S1068	1639	429.5	14x96
1449	S1069	1628	177.5	14x96
1450	S1070	1617	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1451	S1071	1606	429.5	14x96
1452	S1072	1595	177.5	14x96
1453	S1073	1584	303.5	14x96
1454	S1074	1573	429.5	14x96
1455	S1075	1562	177.5	14x96
1456	S1076	1551	303.5	14x96
1457	S1077	1540	429.5	14x96
1458	S1078	1529	177.5	14x96
1459	S1079	1518	303.5	14x96
1460	S1080	1507	429.5	14x96
1461	S1081	1496	177.5	14x96
1462	S1082	1485	303.5	14x96
1463	S1083	1474	429.5	14x96
1464	S1084	1463	177.5	14x96
1465	S1085	1452	303.5	14x96
1466	S1086	1441	429.5	14x96
1467	S1087	1430	177.5	14x96
1468	S1088	1419	303.5	14x96
1469	S1089	1408	429.5	14x96
1470	S1090	1397	177.5	14x96
1471	S1091	1386	303.5	14x96
1472	S1092	1375	429.5	14x96
1473	S1093	1364	177.5	14x96
1474	S1094	1353	303.5	14x96
1475	S1095	1342	429.5	14x96
1476	S1096	1331	177.5	14x96
1477	S1097	1320	303.5	14x96
1478	S1098	1309	429.5	14x96
1479	S1099	1298	177.5	14x96
1480	S1100	1287	303.5	14x96
1481	S1101	1276	429.5	14x96
1482	S1102	1265	177.5	14x96
1483	S1103	1254	303.5	14x96
1484	S1104	1243	429.5	14x96
1485	S1105	1232	177.5	14x96
1486	S1106	1221	303.5	14x96
1487	S1107	1210	429.5	14x96
1488	S1108	1199	177.5	14x96
1489	S1109	1188	303.5	14x96
1490	S1110	1177	429.5	14x96
1491	S1111	1166	177.5	14x96
1492	S1112	1155	303.5	14x96
1493	S1113	1144	429.5	14x96
1494	S1114	1133	177.5	14x96
1495	S1115	1122	303.5	14x96
1496	S1116	1111	429.5	14x96
1497	S1117	1100	177.5	14x96
1498	S1118	1089	303.5	14x96
1499	S1119	1078	429.5	14x96
1500	S1120	1067	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1501	S1121	1056	303.5	14x96
1502	S1122	1045	429.5	14x96
1503	S1123	1034	177.5	14x96
1504	S1124	1023	303.5	14x96
1505	S1125	1012	429.5	14x96
1506	S1126	1001	177.5	14x96
1507	S1127	990	303.5	14x96
1508	S1128	979	429.5	14x96
1509	S1129	968	177.5	14x96
1510	S1130	957	303.5	14x96
1511	S1131	946	429.5	14x96
1512	S1132	935	177.5	14x96
1513	S1133	924	303.5	14x96
1514	S1134	913	429.5	14x96
1515	S1135	902	177.5	14x96
1516	S1136	891	303.5	14x96
1517	S1137	880	429.5	14x96
1518	S1138	869	177.5	14x96
1519	S1139	858	303.5	14x96
1520	S1140	847	429.5	14x96
1521	S1141	836	177.5	14x96
1522	S1142	825	303.5	14x96
1523	S1143	814	429.5	14x96
1524	S1144	803	177.5	14x96
1525	S1145	792	303.5	14x96
1526	S1146	781	429.5	14x96
1527	S1147	770	177.5	14x96
1528	S1148	759	303.5	14x96
1529	S1149	748	429.5	14x96
1530	S1150	737	177.5	14x96
1531	S1151	726	303.5	14x96
1532	S1152	715	429.5	14x96
1533	S1153	704	177.5	14x96
1534	S1154	693	303.5	14x96
1535	S1155	682	429.5	14x96
1536	S1156	671	177.5	14x96
1537	S1157	660	303.5	14x96
1538	S1158	649	429.5	14x96
1539	S1159	638	177.5	14x96
1540	S1160	627	303.5	14x96
1541	S1161	616	429.5	14x96
1542	S1162	605	177.5	14x96
1543	S1163	594	303.5	14x96
1544	S1164	583	429.5	14x96
1545	S1165	572	177.5	14x96
1546	S1166	561	303.5	14x96
1547	S1167	550	429.5	14x96
1548	S1168	539	177.5	14x96
1549	S1169	528	303.5	14x96
1550	S1170	517	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1551	S1171	506	177.5	14x96
1552	S1172	495	303.5	14x96
1553	S1173	484	429.5	14x96
1554	S1174	473	177.5	14x96
1555	S1175	462	303.5	14x96
1556	S1176	451	429.5	14x96
1557	S1177	440	177.5	14x96
1558	S1178	429	303.5	14x96
1559	S1179	418	429.5	14x96
1560	S1180	407	177.5	14x96
1561	S1181	396	303.5	14x96
1562	S1182	385	429.5	14x96
1563	S1183	374	177.5	14x96
1564	S1184	363	303.5	14x96
1565	S1185	352	429.5	14x96
1566	S1186	341	177.5	14x96
1567	S1187	330	303.5	14x96
1568	S1188	319	429.5	14x96
1569	S1189	308	177.5	14x96
1570	S1190	297	303.5	14x96
1571	S1191	286	429.5	14x96
1572	S1192	275	177.5	14x96
1573	S1193	264	303.5	14x96
1574	S1194	253	429.5	14x96
1575	S1195	242	177.5	14x96
1576	S1196	231	303.5	14x96
1577	S1197	220	429.5	14x96
1578	S1198	209	177.5	14x96
1579	S1199	198	303.5	14x96
1580	S1200	187	429.5	14x96
1581	VSSA	176	177.5	14x96
1582	VSSA	165	303.5	14x96
1583	VSSA	154	429.5	14x96
1584	VSSA	143	177.5	14x96
1585	VSSA	132	303.5	14x96
1586	VSSA	121	429.5	14x96
1587	VSSA	110	177.5	14x96
1588	VSSA	99	303.5	14x96
1589	VSSA	88	429.5	14x96
1590	VSSA	77	177.5	14x96
1591	VSSA	66	303.5	14x96
1592	VSSA	55	429.5	14x96
1593	VSSA	44	177.5	14x96
1594	VSSA	33	303.5	14x96
1595	VSSA	22	429.5	14x96
1596	VSSA	11	177.5	14x96
1597	VSSA	0	303.5	14x96
1598	VSSA	-11	429.5	14x96
1599	VSSA	-22	177.5	14x96
1600	VSSA	-33	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1601	VSSA	-44	429.5	14x96
1602	VSSA	-55	177.5	14x96
1603	VSSA	-66	303.5	14x96
1604	VSSA	-77	429.5	14x96
1605	VSSA	-88	177.5	14x96
1606	VSSA	-99	303.5	14x96
1607	VSSA	-110	429.5	14x96
1608	VSSA	-121	177.5	14x96
1609	VSSA	-132	303.5	14x96
1610	VSSA	-143	429.5	14x96
1611	VSSA	-154	177.5	14x96
1612	VSSA	-165	303.5	14x96
1613	VSSA	-176	429.5	14x96
1614	S1201	-187	177.5	14x96
1615	S1202	-198	303.5	14x96
1616	S1203	-209	429.5	14x96
1617	S1204	-220	177.5	14x96
1618	S1205	-231	303.5	14x96
1619	S1206	-242	429.5	14x96
1620	S1207	-253	177.5	14x96
1621	S1208	-264	303.5	14x96
1622	S1209	-275	429.5	14x96
1623	S1210	-286	177.5	14x96
1624	S1211	-297	303.5	14x96
1625	S1212	-308	429.5	14x96
1626	S1213	-319	177.5	14x96
1627	S1214	-330	303.5	14x96
1628	S1215	-341	429.5	14x96
1629	S1216	-352	177.5	14x96
1630	S1217	-363	303.5	14x96
1631	S1218	-374	429.5	14x96
1632	S1219	-385	177.5	14x96
1633	S1220	-396	303.5	14x96
1634	S1221	-407	429.5	14x96
1635	S1222	-418	177.5	14x96
1636	S1223	-429	303.5	14x96
1637	S1224	-440	429.5	14x96
1638	S1225	-451	177.5	14x96
1639	S1226	-462	303.5	14x96
1640	S1227	-473	429.5	14x96
1641	S1228	-484	177.5	14x96
1642	S1229	-495	303.5	14x96
1643	S1230	-506	429.5	14x96
1644	S1231	-517	177.5	14x96
1645	S1232	-528	303.5	14x96
1646	S1233	-539	429.5	14x96
1647	S1234	-550	177.5	14x96
1648	S1235	-561	303.5	14x96
1649	S1236	-572	429.5	14x96
1650	S1237	-583	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1651	S1238	-594	303.5	14x96
1652	S1239	-605	429.5	14x96
1653	S1240	-616	177.5	14x96
1654	S1241	-627	303.5	14x96
1655	S1242	-638	429.5	14x96
1656	S1243	-649	177.5	14x96
1657	S1244	-660	303.5	14x96
1658	S1245	-671	429.5	14x96
1659	S1246	-682	177.5	14x96
1660	S1247	-693	303.5	14x96
1661	S1248	-704	429.5	14x96
1662	S1249	-715	177.5	14x96
1663	S1250	-726	303.5	14x96
1664	S1251	-737	429.5	14x96
1665	S1252	-748	177.5	14x96
1666	S1253	-759	303.5	14x96
1667	S1254	-770	429.5	14x96
1668	S1255	-781	177.5	14x96
1669	S1256	-792	303.5	14x96
1670	S1257	-803	429.5	14x96
1671	S1258	-814	177.5	14x96
1672	S1259	-825	303.5	14x96
1673	S1260	-836	429.5	14x96
1674	S1261	-847	177.5	14x96
1675	S1262	-858	303.5	14x96
1676	S1263	-869	429.5	14x96
1677	S1264	-880	177.5	14x96
1678	S1265	-891	303.5	14x96
1679	S1266	-902	429.5	14x96
1680	S1267	-913	177.5	14x96
1681	S1268	-924	303.5	14x96
1682	S1269	-935	429.5	14x96
1683	S1270	-946	177.5	14x96
1684	S1271	-957	303.5	14x96
1685	S1272	-968	429.5	14x96
1686	S1273	-979	177.5	14x96
1687	S1274	-990	303.5	14x96
1688	S1275	-1001	429.5	14x96
1689	S1276	-1012	177.5	14x96
1690	S1277	-1023	303.5	14x96
1691	S1278	-1034	429.5	14x96
1692	S1279	-1045	177.5	14x96
1693	S1280	-1056	303.5	14x96
1694	S1281	-1067	429.5	14x96
1695	S1282	-1078	177.5	14x96
1696	S1283	-1089	303.5	14x96
1697	S1284	-1100	429.5	14x96
1698	S1285	-1111	177.5	14x96
1699	S1286	-1122	303.5	14x96
1700	S1287	-1133	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1701	S1288	-1144	177.5	14x96
1702	S1289	-1155	303.5	14x96
1703	S1290	-1166	429.5	14x96
1704	S1291	-1177	177.5	14x96
1705	S1292	-1188	303.5	14x96
1706	S1293	-1199	429.5	14x96
1707	S1294	-1210	177.5	14x96
1708	S1295	-1221	303.5	14x96
1709	S1296	-1232	429.5	14x96
1710	S1297	-1243	177.5	14x96
1711	S1298	-1254	303.5	14x96
1712	S1299	-1265	429.5	14x96
1713	S1300	-1276	177.5	14x96
1714	S1301	-1287	303.5	14x96
1715	S1302	-1298	429.5	14x96
1716	S1303	-1309	177.5	14x96
1717	S1304	-1320	303.5	14x96
1718	S1305	-1331	429.5	14x96
1719	S1306	-1342	177.5	14x96
1720	S1307	-1353	303.5	14x96
1721	S1308	-1364	429.5	14x96
1722	S1309	-1375	177.5	14x96
1723	S1310	-1386	303.5	14x96
1724	S1311	-1397	429.5	14x96
1725	S1312	-1408	177.5	14x96
1726	S1313	-1419	303.5	14x96
1727	S1314	-1430	429.5	14x96
1728	S1315	-1441	177.5	14x96
1729	S1316	-1452	303.5	14x96
1730	S1317	-1463	429.5	14x96
1731	S1318	-1474	177.5	14x96
1732	S1319	-1485	303.5	14x96
1733	S1320	-1496	429.5	14x96
1734	S1321	-1507	177.5	14x96
1735	S1322	-1518	303.5	14x96
1736	S1323	-1529	429.5	14x96
1737	S1324	-1540	177.5	14x96
1738	S1325	-1551	303.5	14x96
1739	S1326	-1562	429.5	14x96
1740	S1327	-1573	177.5	14x96
1741	S1328	-1584	303.5	14x96
1742	S1329	-1595	429.5	14x96
1743	S1330	-1606	177.5	14x96
1744	S1331	-1617	303.5	14x96
1745	S1332	-1628	429.5	14x96
1746	S1333	-1639	177.5	14x96
1747	S1334	-1650	303.5	14x96
1748	S1335	-1661	429.5	14x96
1749	S1336	-1672	177.5	14x96
1750	S1337	-1683	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1751	S1338	-1694	429.5	14x96
1752	S1339	-1705	177.5	14x96
1753	S1340	-1716	303.5	14x96
1754	S1341	-1727	429.5	14x96
1755	S1342	-1738	177.5	14x96
1756	S1343	-1749	303.5	14x96
1757	S1344	-1760	429.5	14x96
1758	S1345	-1771	177.5	14x96
1759	S1346	-1782	303.5	14x96
1760	S1347	-1793	429.5	14x96
1761	S1348	-1804	177.5	14x96
1762	S1349	-1815	303.5	14x96
1763	S1350	-1826	429.5	14x96
1764	S1351	-1837	177.5	14x96
1765	S1352	-1848	303.5	14x96
1766	S1353	-1859	429.5	14x96
1767	S1354	-1870	177.5	14x96
1768	S1355	-1881	303.5	14x96
1769	S1356	-1892	429.5	14x96
1770	S1357	-1903	177.5	14x96
1771	S1358	-1914	303.5	14x96
1772	S1359	-1925	429.5	14x96
1773	S1360	-1936	177.5	14x96
1774	S1361	-1947	303.5	14x96
1775	S1362	-1958	429.5	14x96
1776	S1363	-1969	177.5	14x96
1777	S1364	-1980	303.5	14x96
1778	S1365	-1991	429.5	14x96
1779	S1366	-2002	177.5	14x96
1780	S1367	-2013	303.5	14x96
1781	S1368	-2024	429.5	14x96
1782	S1369	-2035	177.5	14x96
1783	S1370	-2046	303.5	14x96
1784	S1371	-2057	429.5	14x96
1785	S1372	-2068	177.5	14x96
1786	S1373	-2079	303.5	14x96
1787	S1374	-2090	429.5	14x96
1788	S1375	-2101	177.5	14x96
1789	S1376	-2112	303.5	14x96
1790	S1377	-2123	429.5	14x96
1791	S1378	-2134	177.5	14x96
1792	S1379	-2145	303.5	14x96
1793	S1380	-2156	429.5	14x96
1794	S1381	-2167	177.5	14x96
1795	S1382	-2178	303.5	14x96
1796	S1383	-2189	429.5	14x96
1797	S1384	-2200	177.5	14x96
1798	S1385	-2211	303.5	14x96
1799	S1386	-2222	429.5	14x96
1800	S1387	-2233	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1801	S1388	-2244	303.5	14x96
1802	S1389	-2255	429.5	14x96
1803	S1390	-2266	177.5	14x96
1804	S1391	-2277	303.5	14x96
1805	S1392	-2288	429.5	14x96
1806	S1393	-2299	177.5	14x96
1807	S1394	-2310	303.5	14x96
1808	S1395	-2321	429.5	14x96
1809	S1396	-2332	177.5	14x96
1810	S1397	-2343	303.5	14x96
1811	S1398	-2354	429.5	14x96
1812	S1399	-2365	177.5	14x96
1813	S1400	-2376	303.5	14x96
1814	S1401	-2387	429.5	14x96
1815	S1402	-2398	177.5	14x96
1816	S1403	-2409	303.5	14x96
1817	S1404	-2420	429.5	14x96
1818	S1405	-2431	177.5	14x96
1819	S1406	-2442	303.5	14x96
1820	S1407	-2453	429.5	14x96
1821	S1408	-2464	177.5	14x96
1822	S1409	-2475	303.5	14x96
1823	S1410	-2486	429.5	14x96
1824	S1411	-2497	177.5	14x96
1825	S1412	-2508	303.5	14x96
1826	S1413	-2519	429.5	14x96
1827	S1414	-2530	177.5	14x96
1828	S1415	-2541	303.5	14x96
1829	S1416	-2552	429.5	14x96
1830	S1417	-2563	177.5	14x96
1831	S1418	-2574	303.5	14x96
1832	S1419	-2585	429.5	14x96
1833	S1420	-2596	177.5	14x96
1834	S1421	-2607	303.5	14x96
1835	S1422	-2618	429.5	14x96
1836	S1423	-2629	177.5	14x96
1837	S1424	-2640	303.5	14x96
1838	S1425	-2651	429.5	14x96
1839	S1426	-2662	177.5	14x96
1840	S1427	-2673	303.5	14x96
1841	S1428	-2684	429.5	14x96
1842	S1429	-2695	177.5	14x96
1843	S1430	-2706	303.5	14x96
1844	S1431	-2717	429.5	14x96
1845	S1432	-2728	177.5	14x96
1846	S1433	-2739	303.5	14x96
1847	S1434	-2750	429.5	14x96
1848	S1435	-2761	177.5	14x96
1849	S1436	-2772	303.5	14x96
1850	S1437	-2783	429.5	14x96

No.	Name	X	Y	Bump size (μm)
1851	S1438	-2794	177.5	14x96
1852	S1439	-2805	303.5	14x96
1853	S1440	-2816	429.5	14x96
1854	S1441	-2827	177.5	14x96
1855	S1442	-2838	303.5	14x96
1856	S1443	-2849	429.5	14x96
1857	S1444	-2860	177.5	14x96
1858	S1445	-2871	303.5	14x96
1859	S1446	-2882	429.5	14x96
1860	S1447	-2893	177.5	14x96
1861	S1448	-2904	303.5	14x96
1862	S1449	-2915	429.5	14x96
1863	S1450	-2926	177.5	14x96
1864	S1451	-2937	303.5	14x96
1865	S1452	-2948	429.5	14x96
1866	S1453	-2959	177.5	14x96
1867	S1454	-2970	303.5	14x96
1868	S1455	-2981	429.5	14x96
1869	S1456	-2992	177.5	14x96
1870	S1457	-3003	303.5	14x96
1871	S1458	-3014	429.5	14x96
1872	S1459	-3025	177.5	14x96
1873	S1460	-3036	303.5	14x96
1874	S1461	-3047	429.5	14x96
1875	S1462	-3058	177.5	14x96
1876	S1463	-3069	303.5	14x96
1877	S1464	-3080	429.5	14x96
1878	S1465	-3091	177.5	14x96
1879	S1466	-3102	303.5	14x96
1880	S1467	-3113	429.5	14x96
1881	S1468	-3124	177.5	14x96
1882	S1469	-3135	303.5	14x96
1883	S1470	-3146	429.5	14x96
1884	S1471	-3157	177.5	14x96
1885	S1472	-3168	303.5	14x96
1886	S1473	-3179	429.5	14x96
1887	S1474	-3190	177.5	14x96
1888	S1475	-3201	303.5	14x96
1889	S1476	-3212	429.5	14x96
1890	S1477	-3223	177.5	14x96
1891	S1478	-3234	303.5	14x96
1892	S1479	-3245	429.5	14x96
1893	S1480	-3256	177.5	14x96
1894	S1481	-3267	303.5	14x96
1895	S1482	-3278	429.5	14x96
1896	S1483	-3289	177.5	14x96
1897	S1484	-3300	303.5	14x96
1898	S1485	-3311	429.5	14x96
1899	S1486	-3322	177.5	14x96
1900	S1487	-3333	303.5	14x96

No.	Name	X	Y	Bump size (μm)
1901	S1488	-3344	429.5	14x96
1902	S1489	-3355	177.5	14x96
1903	S1490	-3366	303.5	14x96
1904	S1491	-3377	429.5	14x96
1905	S1492	-3388	177.5	14x96
1906	S1493	-3399	303.5	14x96
1907	S1494	-3410	429.5	14x96
1908	S1495	-3421	177.5	14x96
1909	S1496	-3432	303.5	14x96
1910	S1497	-3443	429.5	14x96
1911	S1498	-3454	177.5	14x96
1912	S1499	-3465	303.5	14x96
1913	S1500	-3476	429.5	14x96
1914	S1501	-3487	177.5	14x96
1915	S1502	-3498	303.5	14x96
1916	S1503	-3509	429.5	14x96
1917	S1504	-3520	177.5	14x96
1918	S1505	-3531	303.5	14x96
1919	S1506	-3542	429.5	14x96
1920	S1507	-3553	177.5	14x96
1921	S1508	-3564	303.5	14x96
1922	S1509	-3575	429.5	14x96
1923	S1510	-3586	177.5	14x96
1924	S1511	-3597	303.5	14x96
1925	S1512	-3608	429.5	14x96
1926	S1513	-3619	177.5	14x96
1927	S1514	-3630	303.5	14x96
1928	S1515	-3641	429.5	14x96
1929	S1516	-3652	177.5	14x96
1930	S1517	-3663	303.5	14x96
1931	S1518	-3674	429.5	14x96
1932	S1519	-3685	177.5	14x96
1933	S1520	-3696	303.5	14x96
1934	S1521	-3707	429.5	14x96
1935	S1522	-3718	177.5	14x96
1936	S1523	-3729	303.5	14x96
1937	S1524	-3740	429.5	14x96
1938	S1525	-3751	177.5	14x96
1939	S1526	-3762	303.5	14x96
1940	S1527	-3773	429.5	14x96
1941	S1528	-3784	177.5	14x96
1942	S1529	-3795	303.5	14x96
1943	S1530	-3806	429.5	14x96
1944	S1531	-3817	177.5	14x96
1945	S1532	-3828	303.5	14x96
1946	S1533	-3839	429.5	14x96
1947	S1534	-3850	177.5	14x96
1948	S1535	-3861	303.5	14x96
1949	S1536	-3872	429.5	14x96
1950	S1537	-3883	177.5	14x96

No.	Name	X	Y	Bump size (μm)
1951	S1538	-3894	303.5	14x96
1952	S1539	-3905	429.5	14x96
1953	S1540	-3916	177.5	14x96
1954	S1541	-3927	303.5	14x96
1955	S1542	-3938	429.5	14x96
1956	S1543	-3949	177.5	14x96
1957	S1544	-3960	303.5	14x96
1958	S1545	-3971	429.5	14x96
1959	S1546	-3982	177.5	14x96
1960	S1547	-3993	303.5	14x96
1961	S1548	-4004	429.5	14x96
1962	S1549	-4015	177.5	14x96
1963	S1550	-4026	303.5	14x96
1964	S1551	-4037	429.5	14x96
1965	S1552	-4048	177.5	14x96
1966	S1553	-4059	303.5	14x96
1967	S1554	-4070	429.5	14x96
1968	S1555	-4081	177.5	14x96
1969	S1556	-4092	303.5	14x96
1970	S1557	-4103	429.5	14x96
1971	S1558	-4114	177.5	14x96
1972	S1559	-4125	303.5	14x96
1973	S1560	-4136	429.5	14x96
1974	S1561	-4147	177.5	14x96
1975	S1562	-4158	303.5	14x96
1976	S1563	-4169	429.5	14x96
1977	S1564	-4180	177.5	14x96
1978	S1565	-4191	303.5	14x96
1979	S1566	-4202	429.5	14x96
1980	S1567	-4213	177.5	14x96
1981	S1568	-4224	303.5	14x96
1982	S1569	-4235	429.5	14x96
1983	S1570	-4246	177.5	14x96
1984	S1571	-4257	303.5	14x96
1985	S1572	-4268	429.5	14x96
1986	S1573	-4279	177.5	14x96
1987	S1574	-4290	303.5	14x96
1988	S1575	-4301	429.5	14x96
1989	S1576	-4312	177.5	14x96
1990	S1577	-4323	303.5	14x96
1991	S1578	-4334	429.5	14x96
1992	S1579	-4345	177.5	14x96
1993	S1580	-4356	303.5	14x96
1994	S1581	-4367	429.5	14x96
1995	S1582	-4378	177.5	14x96
1996	S1583	-4389	303.5	14x96
1997	S1584	-4400	429.5	14x96
1998	S1585	-4411	177.5	14x96
1999	S1586	-4422	303.5	14x96
2000	S1587	-4433	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2001	S1588	-4444	177.5	14x96
2002	S1589	-4455	303.5	14x96
2003	S1590	-4466	429.5	14x96
2004	S1591	-4477	177.5	14x96
2005	S1592	-4488	303.5	14x96
2006	S1593	-4499	429.5	14x96
2007	S1594	-4510	177.5	14x96
2008	S1595	-4521	303.5	14x96
2009	S1596	-4532	429.5	14x96
2010	S1597	-4543	177.5	14x96
2011	S1598	-4554	303.5	14x96
2012	S1599	-4565	429.5	14x96
2013	S1600	-4576	177.5	14x96
2014	S1601	-4587	303.5	14x96
2015	S1602	-4598	429.5	14x96
2016	S1603	-4609	177.5	14x96
2017	S1604	-4620	303.5	14x96
2018	S1605	-4631	429.5	14x96
2019	S1606	-4642	177.5	14x96
2020	S1607	-4653	303.5	14x96
2021	S1608	-4664	429.5	14x96
2022	S1609	-4675	177.5	14x96
2023	S1610	-4686	303.5	14x96
2024	S1611	-4697	429.5	14x96
2025	S1612	-4708	177.5	14x96
2026	S1613	-4719	303.5	14x96
2027	S1614	-4730	429.5	14x96
2028	S1615	-4741	177.5	14x96
2029	S1616	-4752	303.5	14x96
2030	S1617	-4763	429.5	14x96
2031	S1618	-4774	177.5	14x96
2032	S1619	-4785	303.5	14x96
2033	S1620	-4796	429.5	14x96
2034	S1621	-4807	177.5	14x96
2035	S1622	-4818	303.5	14x96
2036	S1623	-4829	429.5	14x96
2037	S1624	-4840	177.5	14x96
2038	S1625	-4851	303.5	14x96
2039	S1626	-4862	429.5	14x96
2040	S1627	-4873	177.5	14x96
2041	S1628	-4884	303.5	14x96
2042	S1629	-4895	429.5	14x96
2043	S1630	-4906	177.5	14x96
2044	S1631	-4917	303.5	14x96
2045	S1632	-4928	429.5	14x96
2046	S1633	-4939	177.5	14x96
2047	S1634	-4950	303.5	14x96
2048	S1635	-4961	429.5	14x96
2049	S1636	-4972	177.5	14x96
2050	S1637	-4983	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2051	S1638	-4994	429.5	14x96
2052	S1639	-5005	177.5	14x96
2053	S1640	-5016	303.5	14x96
2054	S1641	-5027	429.5	14x96
2055	S1642	-5038	177.5	14x96
2056	S1643	-5049	303.5	14x96
2057	S1644	-5060	429.5	14x96
2058	S1645	-5071	177.5	14x96
2059	S1646	-5082	303.5	14x96
2060	S1647	-5093	429.5	14x96
2061	S1648	-5104	177.5	14x96
2062	S1649	-5115	303.5	14x96
2063	S1650	-5126	429.5	14x96
2064	S1651	-5137	177.5	14x96
2065	S1652	-5148	303.5	14x96
2066	S1653	-5159	429.5	14x96
2067	S1654	-5170	177.5	14x96
2068	S1655	-5181	303.5	14x96
2069	S1656	-5192	429.5	14x96
2070	S1657	-5203	177.5	14x96
2071	S1658	-5214	303.5	14x96
2072	S1659	-5225	429.5	14x96
2073	S1660	-5236	177.5	14x96
2074	S1661	-5247	303.5	14x96
2075	S1662	-5258	429.5	14x96
2076	S1663	-5269	177.5	14x96
2077	S1664	-5280	303.5	14x96
2078	S1665	-5291	429.5	14x96
2079	S1666	-5302	177.5	14x96
2080	S1667	-5313	303.5	14x96
2081	S1668	-5324	429.5	14x96
2082	S1669	-5335	177.5	14x96
2083	S1670	-5346	303.5	14x96
2084	S1671	-5357	429.5	14x96
2085	S1672	-5368	177.5	14x96
2086	S1673	-5379	303.5	14x96
2087	S1674	-5390	429.5	14x96
2088	S1675	-5401	177.5	14x96
2089	S1676	-5412	303.5	14x96
2090	S1677	-5423	429.5	14x96
2091	S1678	-5434	177.5	14x96
2092	S1679	-5445	303.5	14x96
2093	S1680	-5456	429.5	14x96
2094	S1681	-5467	177.5	14x96
2095	S1682	-5478	303.5	14x96
2096	S1683	-5489	429.5	14x96
2097	S1684	-5500	177.5	14x96
2098	S1685	-5511	303.5	14x96
2099	S1686	-5522	429.5	14x96
2100	S1687	-5533	177.5	14x96

No.	Name	X	Y	Bump size (μm)
2101	S1688	-5544	303.5	14x96
2102	S1689	-5555	429.5	14x96
2103	S1690	-5566	177.5	14x96
2104	S1691	-5577	303.5	14x96
2105	S1692	-5588	429.5	14x96
2106	S1693	-5599	177.5	14x96
2107	S1694	-5610	303.5	14x96
2108	S1695	-5621	429.5	14x96
2109	S1696	-5632	177.5	14x96
2110	S1697	-5643	303.5	14x96
2111	S1698	-5654	429.5	14x96
2112	S1699	-5665	177.5	14x96
2113	S1700	-5676	303.5	14x96
2114	S1701	-5687	429.5	14x96
2115	S1702	-5698	177.5	14x96
2116	S1703	-5709	303.5	14x96
2117	S1704	-5720	429.5	14x96
2118	S1705	-5731	177.5	14x96
2119	S1706	-5742	303.5	14x96
2120	S1707	-5753	429.5	14x96
2121	S1708	-5764	177.5	14x96
2122	S1709	-5775	303.5	14x96
2123	S1710	-5786	429.5	14x96
2124	S1711	-5797	177.5	14x96
2125	S1712	-5808	303.5	14x96
2126	S1713	-5819	429.5	14x96
2127	S1714	-5830	177.5	14x96
2128	S1715	-5841	303.5	14x96
2129	S1716	-5852	429.5	14x96
2130	S1717	-5863	177.5	14x96
2131	S1718	-5874	303.5	14x96
2132	S1719	-5885	429.5	14x96
2133	S1720	-5896	177.5	14x96
2134	S1721	-5907	303.5	14x96
2135	S1722	-5918	429.5	14x96
2136	S1723	-5929	177.5	14x96
2137	S1724	-5940	303.5	14x96
2138	S1725	-5951	429.5	14x96
2139	S1726	-5962	177.5	14x96
2140	S1727	-5973	303.5	14x96
2141	S1728	-5984	429.5	14x96
2142	S1729	-5995	177.5	14x96
2143	S1730	-6006	303.5	14x96
2144	S1731	-6017	429.5	14x96
2145	S1732	-6028	177.5	14x96
2146	S1733	-6039	303.5	14x96
2147	S1734	-6050	429.5	14x96
2148	S1735	-6061	177.5	14x96
2149	S1736	-6072	303.5	14x96
2150	S1737	-6083	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2151	S1738	-6094	177.5	14x96
2152	S1739	-6105	303.5	14x96
2153	S1740	-6116	429.5	14x96
2154	S1741	-6127	177.5	14x96
2155	S1742	-6138	303.5	14x96
2156	S1743	-6149	429.5	14x96
2157	S1744	-6160	177.5	14x96
2158	S1745	-6171	303.5	14x96
2159	S1746	-6182	429.5	14x96
2160	S1747	-6193	177.5	14x96
2161	S1748	-6204	303.5	14x96
2162	S1749	-6215	429.5	14x96
2163	S1750	-6226	177.5	14x96
2164	S1751	-6237	303.5	14x96
2165	S1752	-6248	429.5	14x96
2166	S1753	-6259	177.5	14x96
2167	S1754	-6270	303.5	14x96
2168	S1755	-6281	429.5	14x96
2169	S1756	-6292	177.5	14x96
2170	S1757	-6303	303.5	14x96
2171	S1758	-6314	429.5	14x96
2172	S1759	-6325	177.5	14x96
2173	S1760	-6336	303.5	14x96
2174	S1761	-6347	429.5	14x96
2175	S1762	-6358	177.5	14x96
2176	S1763	-6369	303.5	14x96
2177	S1764	-6380	429.5	14x96
2178	S1765	-6391	177.5	14x96
2179	S1766	-6402	303.5	14x96
2180	S1767	-6413	429.5	14x96
2181	S1768	-6424	177.5	14x96
2182	S1769	-6435	303.5	14x96
2183	S1770	-6446	429.5	14x96
2184	S1771	-6457	177.5	14x96
2185	S1772	-6468	303.5	14x96
2186	S1773	-6479	429.5	14x96
2187	S1774	-6490	177.5	14x96
2188	S1775	-6501	303.5	14x96
2189	S1776	-6512	429.5	14x96
2190	S1777	-6523	177.5	14x96
2191	S1778	-6534	303.5	14x96
2192	S1779	-6545	429.5	14x96
2193	S1780	-6556	177.5	14x96
2194	S1781	-6567	303.5	14x96
2195	S1782	-6578	429.5	14x96
2196	S1783	-6589	177.5	14x96
2197	S1784	-6600	303.5	14x96
2198	S1785	-6611	429.5	14x96
2199	S1786	-6622	177.5	14x96
2200	S1787	-6633	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2201	S1788	-6644	429.5	14x96
2202	S1789	-6655	177.5	14x96
2203	S1790	-6666	303.5	14x96
2204	S1791	-6677	429.5	14x96
2205	S1792	-6688	177.5	14x96
2206	S1793	-6699	303.5	14x96
2207	S1794	-6710	429.5	14x96
2208	S1795	-6721	177.5	14x96
2209	S1796	-6732	303.5	14x96
2210	S1797	-6743	429.5	14x96
2211	S1798	-6754	177.5	14x96
2212	S1799	-6765	303.5	14x96
2213	S1800	-6776	429.5	14x96
2214	S1801	-6787	177.5	14x96
2215	S1802	-6798	303.5	14x96
2216	S1803	-6809	429.5	14x96
2217	S1804	-6820	177.5	14x96
2218	S1805	-6831	303.5	14x96
2219	S1806	-6842	429.5	14x96
2220	S1807	-6853	177.5	14x96
2221	S1808	-6864	303.5	14x96
2222	S1809	-6875	429.5	14x96
2223	S1810	-6886	177.5	14x96
2224	S1811	-6897	303.5	14x96
2225	S1812	-6908	429.5	14x96
2226	S1813	-6919	177.5	14x96
2227	S1814	-6930	303.5	14x96
2228	S1815	-6941	429.5	14x96
2229	S1816	-6952	177.5	14x96
2230	S1817	-6963	303.5	14x96
2231	S1818	-6974	429.5	14x96
2232	S1819	-6985	177.5	14x96
2233	S1820	-6996	303.5	14x96
2234	S1821	-7007	429.5	14x96
2235	S1822	-7018	177.5	14x96
2236	S1823	-7029	303.5	14x96
2237	S1824	-7040	429.5	14x96
2238	S1825	-7051	177.5	14x96
2239	S1826	-7062	303.5	14x96
2240	S1827	-7073	429.5	14x96
2241	S1828	-7084	177.5	14x96
2242	S1829	-7095	303.5	14x96
2243	S1830	-7106	429.5	14x96
2244	S1831	-7117	177.5	14x96
2245	S1832	-7128	303.5	14x96
2246	S1833	-7139	429.5	14x96
2247	S1834	-7150	177.5	14x96
2248	S1835	-7161	303.5	14x96
2249	S1836	-7172	429.5	14x96
2250	S1837	-7183	177.5	14x96

No.	Name	X	Y	Bump size (μm)
2251	S1838	-7194	303.5	14x96
2252	S1839	-7205	429.5	14x96
2253	S1840	-7216	177.5	14x96
2254	S1841	-7227	303.5	14x96
2255	S1842	-7238	429.5	14x96
2256	S1843	-7249	177.5	14x96
2257	S1844	-7260	303.5	14x96
2258	S1845	-7271	429.5	14x96
2259	S1846	-7282	177.5	14x96
2260	S1847	-7293	303.5	14x96
2261	S1848	-7304	429.5	14x96
2262	S1849	-7315	177.5	14x96
2263	S1850	-7326	303.5	14x96
2264	S1851	-7337	429.5	14x96
2265	S1852	-7348	177.5	14x96
2266	S1853	-7359	303.5	14x96
2267	S1854	-7370	429.5	14x96
2268	S1855	-7381	177.5	14x96
2269	S1856	-7392	303.5	14x96
2270	S1857	-7403	429.5	14x96
2271	S1858	-7414	177.5	14x96
2272	S1859	-7425	303.5	14x96
2273	S1860	-7436	429.5	14x96
2274	S1861	-7447	177.5	14x96
2275	S1862	-7458	303.5	14x96
2276	S1863	-7469	429.5	14x96
2277	S1864	-7480	177.5	14x96
2278	S1865	-7491	303.5	14x96
2279	S1866	-7502	429.5	14x96
2280	S1867	-7513	177.5	14x96
2281	S1868	-7524	303.5	14x96
2282	S1869	-7535	429.5	14x96
2283	S1870	-7546	177.5	14x96
2284	S1871	-7557	303.5	14x96
2285	S1872	-7568	429.5	14x96
2286	S1873	-7579	177.5	14x96
2287	S1874	-7590	303.5	14x96
2288	S1875	-7601	429.5	14x96
2289	S1876	-7612	177.5	14x96
2290	S1877	-7623	303.5	14x96
2291	S1878	-7634	429.5	14x96
2292	S1879	-7645	177.5	14x96
2293	S1880	-7656	303.5	14x96
2294	S1881	-7667	429.5	14x96
2295	S1882	-7678	177.5	14x96
2296	S1883	-7689	303.5	14x96
2297	S1884	-7700	429.5	14x96
2298	S1885	-7711	177.5	14x96
2299	S1886	-7722	303.5	14x96
2300	S1887	-7733	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2301	S1888	-7744	177.5	14x96
2302	S1889	-7755	303.5	14x96
2303	S1890	-7766	429.5	14x96
2304	S1891	-7777	177.5	14x96
2305	S1892	-7788	303.5	14x96
2306	S1893	-7799	429.5	14x96
2307	S1894	-7810	177.5	14x96
2308	S1895	-7821	303.5	14x96
2309	S1896	-7832	429.5	14x96
2310	S1897	-7843	177.5	14x96
2311	S1898	-7854	303.5	14x96
2312	S1899	-7865	429.5	14x96
2313	S1900	-7876	177.5	14x96
2314	S1901	-7887	303.5	14x96
2315	S1902	-7898	429.5	14x96
2316	S1903	-7909	177.5	14x96
2317	S1904	-7920	303.5	14x96
2318	S1905	-7931	429.5	14x96
2319	S1906	-7942	177.5	14x96
2320	S1907	-7953	303.5	14x96
2321	S1908	-7964	429.5	14x96
2322	S1909	-7975	177.5	14x96
2323	S1910	-7986	303.5	14x96
2324	S1911	-7997	429.5	14x96
2325	S1912	-8008	177.5	14x96
2326	S1913	-8019	303.5	14x96
2327	S1914	-8030	429.5	14x96
2328	S1915	-8041	177.5	14x96
2329	S1916	-8052	303.5	14x96
2330	S1917	-8063	429.5	14x96
2331	S1918	-8074	177.5	14x96
2332	S1919	-8085	303.5	14x96
2333	S1920	-8096	429.5	14x96
2334	S1921	-8107	177.5	14x96
2335	S1922	-8118	303.5	14x96
2336	S1923	-8129	429.5	14x96
2337	S1924	-8140	177.5	14x96
2338	S1925	-8151	303.5	14x96
2339	S1926	-8162	429.5	14x96
2340	S1927	-8173	177.5	14x96
2341	S1928	-8184	303.5	14x96
2342	S1929	-8195	429.5	14x96
2343	S1930	-8206	177.5	14x96
2344	S1931	-8217	303.5	14x96
2345	S1932	-8228	429.5	14x96
2346	S1933	-8239	177.5	14x96
2347	S1934	-8250	303.5	14x96
2348	S1935	-8261	429.5	14x96
2349	S1936	-8272	177.5	14x96
2350	S1937	-8283	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2351	S1938	-8294	429.5	14x96
2352	S1939	-8305	177.5	14x96
2353	S1940	-8316	303.5	14x96
2354	S1941	-8327	429.5	14x96
2355	S1942	-8338	177.5	14x96
2356	S1943	-8349	303.5	14x96
2357	S1944	-8360	429.5	14x96
2358	S1945	-8371	177.5	14x96
2359	S1946	-8382	303.5	14x96
2360	S1947	-8393	429.5	14x96
2361	S1948	-8404	177.5	14x96
2362	S1949	-8415	303.5	14x96
2363	S1950	-8426	429.5	14x96
2364	S1951	-8437	177.5	14x96
2365	S1952	-8448	303.5	14x96
2366	S1953	-8459	429.5	14x96
2367	S1954	-8470	177.5	14x96
2368	S1955	-8481	303.5	14x96
2369	S1956	-8492	429.5	14x96
2370	S1957	-8503	177.5	14x96
2371	S1958	-8514	303.5	14x96
2372	S1959	-8525	429.5	14x96
2373	S1960	-8536	177.5	14x96
2374	S1961	-8547	303.5	14x96
2375	S1962	-8558	429.5	14x96
2376	S1963	-8569	177.5	14x96
2377	S1964	-8580	303.5	14x96
2378	S1965	-8591	429.5	14x96
2379	S1966	-8602	177.5	14x96
2380	S1967	-8613	303.5	14x96
2381	S1968	-8624	429.5	14x96
2382	S1969	-8635	177.5	14x96
2383	S1970	-8646	303.5	14x96
2384	S1971	-8657	429.5	14x96
2385	S1972	-8668	177.5	14x96
2386	S1973	-8679	303.5	14x96
2387	S1974	-8690	429.5	14x96
2388	S1975	-8701	177.5	14x96
2389	S1976	-8712	303.5	14x96
2390	S1977	-8723	429.5	14x96
2391	S1978	-8734	177.5	14x96
2392	S1979	-8745	303.5	14x96
2393	S1980	-8756	429.5	14x96
2394	S1981	-8767	177.5	14x96
2395	S1982	-8778	303.5	14x96
2396	S1983	-8789	429.5	14x96
2397	S1984	-8800	177.5	14x96
2398	S1985	-8811	303.5	14x96
2399	S1986	-8822	429.5	14x96
2400	S1987	-8833	177.5	14x96

No.	Name	X	Y	Bump size (μm)
2401	S1988	-8844	303.5	14x96
2402	S1989	-8855	429.5	14x96
2403	S1990	-8866	177.5	14x96
2404	S1991	-8877	303.5	14x96
2405	S1992	-8888	429.5	14x96
2406	S1993	-8899	177.5	14x96
2407	S1994	-8910	303.5	14x96
2408	S1995	-8921	429.5	14x96
2409	S1996	-8932	177.5	14x96
2410	S1997	-8943	303.5	14x96
2411	S1998	-8954	429.5	14x96
2412	S1999	-8965	177.5	14x96
2413	S2000	-8976	303.5	14x96
2414	S2001	-8987	429.5	14x96
2415	S2002	-8998	177.5	14x96
2416	S2003	-9009	303.5	14x96
2417	S2004	-9020	429.5	14x96
2418	S2005	-9031	177.5	14x96
2419	S2006	-9042	303.5	14x96
2420	S2007	-9053	429.5	14x96
2421	S2008	-9064	177.5	14x96
2422	S2009	-9075	303.5	14x96
2423	S2010	-9086	429.5	14x96
2424	S2011	-9097	177.5	14x96
2425	S2012	-9108	303.5	14x96
2426	S2013	-9119	429.5	14x96
2427	S2014	-9130	177.5	14x96
2428	S2015	-9141	303.5	14x96
2429	S2016	-9152	429.5	14x96
2430	S2017	-9163	177.5	14x96
2431	S2018	-9174	303.5	14x96
2432	S2019	-9185	429.5	14x96
2433	S2020	-9196	177.5	14x96
2434	S2021	-9207	303.5	14x96
2435	S2022	-9218	429.5	14x96
2436	S2023	-9229	177.5	14x96
2437	S2024	-9240	303.5	14x96
2438	S2025	-9251	429.5	14x96
2439	S2026	-9262	177.5	14x96
2440	S2027	-9273	303.5	14x96
2441	S2028	-9284	429.5	14x96
2442	S2029	-9295	177.5	14x96
2443	S2030	-9306	303.5	14x96
2444	S2031	-9317	429.5	14x96
2445	S2032	-9328	177.5	14x96
2446	S2033	-9339	303.5	14x96
2447	S2034	-9350	429.5	14x96
2448	S2035	-9361	177.5	14x96
2449	S2036	-9372	303.5	14x96
2450	S2037	-9383	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2451	S2038	-9394	177.5	14x96
2452	S2039	-9405	303.5	14x96
2453	S2040	-9416	429.5	14x96
2454	S2041	-9427	177.5	14x96
2455	S2042	-9438	303.5	14x96
2456	S2043	-9449	429.5	14x96
2457	S2044	-9460	177.5	14x96
2458	S2045	-9471	303.5	14x96
2459	S2046	-9482	429.5	14x96
2460	S2047	-9493	177.5	14x96
2461	S2048	-9504	303.5	14x96
2462	S2049	-9515	429.5	14x96
2463	S2050	-9526	177.5	14x96
2464	S2051	-9537	303.5	14x96
2465	S2052	-9548	429.5	14x96
2466	S2053	-9559	177.5	14x96
2467	S2054	-9570	303.5	14x96
2468	S2055	-9581	429.5	14x96
2469	S2056	-9592	177.5	14x96
2470	S2057	-9603	303.5	14x96
2471	S2058	-9614	429.5	14x96
2472	S2059	-9625	177.5	14x96
2473	S2060	-9636	303.5	14x96
2474	S2061	-9647	429.5	14x96
2475	S2062	-9658	177.5	14x96
2476	S2063	-9669	303.5	14x96
2477	S2064	-9680	429.5	14x96
2478	S2065	-9691	177.5	14x96
2479	S2066	-9702	303.5	14x96
2480	S2067	-9713	429.5	14x96
2481	S2068	-9724	177.5	14x96
2482	S2069	-9735	303.5	14x96
2483	S2070	-9746	429.5	14x96
2484	S2071	-9757	177.5	14x96
2485	S2072	-9768	303.5	14x96
2486	S2073	-9779	429.5	14x96
2487	S2074	-9790	177.5	14x96
2488	S2075	-9801	303.5	14x96
2489	S2076	-9812	429.5	14x96
2490	S2077	-9823	177.5	14x96
2491	S2078	-9834	303.5	14x96
2492	S2079	-9845	429.5	14x96
2493	S2080	-9856	177.5	14x96
2494	S2081	-9867	303.5	14x96
2495	S2082	-9878	429.5	14x96
2496	S2083	-9889	177.5	14x96
2497	S2084	-9900	303.5	14x96
2498	S2085	-9911	429.5	14x96
2499	S2086	-9922	177.5	14x96
2500	S2087	-9933	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2501	S2088	-9944	429.5	14x96
2502	S2089	-9955	177.5	14x96
2503	S2090	-9966	303.5	14x96
2504	S2091	-9977	429.5	14x96
2505	S2092	-9988	177.5	14x96
2506	S2093	-9999	303.5	14x96
2507	S2094	-10010	429.5	14x96
2508	S2095	-10021	177.5	14x96
2509	S2096	-10032	303.5	14x96
2510	S2097	-10043	429.5	14x96
2511	S2098	-10054	177.5	14x96
2512	S2099	-10065	303.5	14x96
2513	S2100	-10076	429.5	14x96
2514	S2101	-10087	177.5	14x96
2515	S2102	-10098	303.5	14x96
2516	S2103	-10109	429.5	14x96
2517	S2104	-10120	177.5	14x96
2518	S2105	-10131	303.5	14x96
2519	S2106	-10142	429.5	14x96
2520	S2107	-10153	177.5	14x96
2521	S2108	-10164	303.5	14x96
2522	S2109	-10175	429.5	14x96
2523	S2110	-10186	177.5	14x96
2524	S2111	-10197	303.5	14x96
2525	S2112	-10208	429.5	14x96
2526	S2113	-10219	177.5	14x96
2527	S2114	-10230	303.5	14x96
2528	S2115	-10241	429.5	14x96
2529	S2116	-10252	177.5	14x96
2530	S2117	-10263	303.5	14x96
2531	S2118	-10274	429.5	14x96
2532	S2119	-10285	177.5	14x96
2533	S2120	-10296	303.5	14x96
2534	S2121	-10307	429.5	14x96
2535	S2122	-10318	177.5	14x96
2536	S2123	-10329	303.5	14x96
2537	S2124	-10340	429.5	14x96
2538	S2125	-10351	177.5	14x96
2539	S2126	-10362	303.5	14x96
2540	S2127	-10373	429.5	14x96
2541	S2128	-10384	177.5	14x96
2542	S2129	-10395	303.5	14x96
2543	S2130	-10406	429.5	14x96
2544	S2131	-10417	177.5	14x96
2545	S2132	-10428	303.5	14x96
2546	S2133	-10439	429.5	14x96
2547	S2134	-10450	177.5	14x96
2548	S2135	-10461	303.5	14x96
2549	S2136	-10472	429.5	14x96
2550	S2137	-10483	177.5	14x96

No.	Name	X	Y	Bump size (μm)
2551	S2138	-10494	303.5	14x96
2552	S2139	-10505	429.5	14x96
2553	S2140	-10516	177.5	14x96
2554	S2141	-10527	303.5	14x96
2555	S2142	-10538	429.5	14x96
2556	S2143	-10549	177.5	14x96
2557	S2144	-10560	303.5	14x96
2558	S2145	-10571	429.5	14x96
2559	S2146	-10582	177.5	14x96
2560	S2147	-10593	303.5	14x96
2561	S2148	-10604	429.5	14x96
2562	S2149	-10615	177.5	14x96
2563	S2150	-10626	303.5	14x96
2564	S2151	-10637	429.5	14x96
2565	S2152	-10648	177.5	14x96
2566	S2153	-10659	303.5	14x96
2567	S2154	-10670	429.5	14x96
2568	S2155	-10681	177.5	14x96
2569	S2156	-10692	303.5	14x96
2570	S2157	-10703	429.5	14x96
2571	S2158	-10714	177.5	14x96
2572	S2159	-10725	303.5	14x96
2573	S2160	-10736	429.5	14x96
2574	S2161	-10747	177.5	14x96
2575	S2162	-10758	303.5	14x96
2576	S2163	-10769	429.5	14x96
2577	S2164	-10780	177.5	14x96
2578	S2165	-10791	303.5	14x96
2579	S2166	-10802	429.5	14x96
2580	S2167	-10813	177.5	14x96
2581	S2168	-10824	303.5	14x96
2582	S2169	-10835	429.5	14x96
2583	S2170	-10846	177.5	14x96
2584	S2171	-10857	303.5	14x96
2585	S2172	-10868	429.5	14x96
2586	S2173	-10879	177.5	14x96
2587	S2174	-10890	303.5	14x96
2588	S2175	-10901	429.5	14x96
2589	S2176	-10912	177.5	14x96
2590	S2177	-10923	303.5	14x96
2591	S2178	-10934	429.5	14x96
2592	S2179	-10945	177.5	14x96
2593	S2180	-10956	303.5	14x96
2594	S2181	-10967	429.5	14x96
2595	S2182	-10978	177.5	14x96
2596	S2183	-10989	303.5	14x96
2597	S2184	-11000	429.5	14x96
2598	S2185	-11011	177.5	14x96
2599	S2186	-11022	303.5	14x96
2600	S2187	-11033	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2601	S2188	-11044	177.5	14x96
2602	S2189	-11055	303.5	14x96
2603	S2190	-11066	429.5	14x96
2604	S2191	-11077	177.5	14x96
2605	S2192	-11088	303.5	14x96
2606	S2193	-11099	429.5	14x96
2607	S2194	-11110	177.5	14x96
2608	S2195	-11121	303.5	14x96
2609	S2196	-11132	429.5	14x96
2610	S2197	-11143	177.5	14x96
2611	S2198	-11154	303.5	14x96
2612	S2199	-11165	429.5	14x96
2613	S2200	-11176	177.5	14x96
2614	S2201	-11187	303.5	14x96
2615	S2202	-11198	429.5	14x96
2616	S2203	-11209	177.5	14x96
2617	S2204	-11220	303.5	14x96
2618	S2205	-11231	429.5	14x96
2619	S2206	-11242	177.5	14x96
2620	S2207	-11253	303.5	14x96
2621	S2208	-11264	429.5	14x96
2622	S2209	-11275	177.5	14x96
2623	S2210	-11286	303.5	14x96
2624	S2211	-11297	429.5	14x96
2625	S2212	-11308	177.5	14x96
2626	S2213	-11319	303.5	14x96
2627	S2214	-11330	429.5	14x96
2628	S2215	-11341	177.5	14x96
2629	S2216	-11352	303.5	14x96
2630	S2217	-11363	429.5	14x96
2631	S2218	-11374	177.5	14x96
2632	S2219	-11385	303.5	14x96
2633	S2220	-11396	429.5	14x96
2634	S2221	-11407	177.5	14x96
2635	S2222	-11418	303.5	14x96
2636	S2223	-11429	429.5	14x96
2637	S2224	-11440	177.5	14x96
2638	S2225	-11451	303.5	14x96
2639	S2226	-11462	429.5	14x96
2640	S2227	-11473	177.5	14x96
2641	S2228	-11484	303.5	14x96
2642	S2229	-11495	429.5	14x96
2643	S2230	-11506	177.5	14x96
2644	S2231	-11517	303.5	14x96
2645	S2232	-11528	429.5	14x96
2646	S2233	-11539	177.5	14x96
2647	S2234	-11550	303.5	14x96
2648	S2235	-11561	429.5	14x96
2649	S2236	-11572	177.5	14x96
2650	S2237	-11583	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2651	S2238	-11594	429.5	14x96
2652	S2239	-11605	177.5	14x96
2653	S2240	-11616	303.5	14x96
2654	S2241	-11627	429.5	14x96
2655	S2242	-11638	177.5	14x96
2656	S2243	-11649	303.5	14x96
2657	S2244	-11660	429.5	14x96
2658	S2245	-11671	177.5	14x96
2659	S2246	-11682	303.5	14x96
2660	S2247	-11693	429.5	14x96
2661	S2248	-11704	177.5	14x96
2662	S2249	-11715	303.5	14x96
2663	S2250	-11726	429.5	14x96
2664	S2251	-11737	177.5	14x96
2665	S2252	-11748	303.5	14x96
2666	S2253	-11759	429.5	14x96
2667	S2254	-11770	177.5	14x96
2668	S2255	-11781	303.5	14x96
2669	S2256	-11792	429.5	14x96
2670	S2257	-11803	177.5	14x96
2671	S2258	-11814	303.5	14x96
2672	S2259	-11825	429.5	14x96
2673	S2260	-11836	177.5	14x96
2674	S2261	-11847	303.5	14x96
2675	S2262	-11858	429.5	14x96
2676	S2263	-11869	177.5	14x96
2677	S2264	-11880	303.5	14x96
2678	S2265	-11891	429.5	14x96
2679	S2266	-11902	177.5	14x96
2680	S2267	-11913	303.5	14x96
2681	S2268	-11924	429.5	14x96
2682	S2269	-11935	177.5	14x96
2683	S2270	-11946	303.5	14x96
2684	S2271	-11957	429.5	14x96
2685	S2272	-11968	177.5	14x96
2686	S2273	-11979	303.5	14x96
2687	S2274	-11990	429.5	14x96
2688	S2275	-12001	177.5	14x96
2689	S2276	-12012	303.5	14x96
2690	S2277	-12023	429.5	14x96
2691	S2278	-12034	177.5	14x96
2692	S2279	-12045	303.5	14x96
2693	S2280	-12056	429.5	14x96
2694	S2281	-12067	177.5	14x96
2695	S2282	-12078	303.5	14x96
2696	S2283	-12089	429.5	14x96
2697	S2284	-12100	177.5	14x96
2698	S2285	-12111	303.5	14x96
2699	S2286	-12122	429.5	14x96
2700	S2287	-12133	177.5	14x96

No.	Name	X	Y	Bump size (μm)
2701	S2288	-12144	303.5	14x96
2702	S2289	-12155	429.5	14x96
2703	S2290	-12166	177.5	14x96
2704	S2291	-12177	303.5	14x96
2705	S2292	-12188	429.5	14x96
2706	S2293	-12199	177.5	14x96
2707	S2294	-12210	303.5	14x96
2708	S2295	-12221	429.5	14x96
2709	S2296	-12232	177.5	14x96
2710	S2297	-12243	303.5	14x96
2711	S2298	-12254	429.5	14x96
2712	S2299	-12265	177.5	14x96
2713	S2300	-12276	303.5	14x96
2714	S2301	-12287	429.5	14x96
2715	S2302	-12298	177.5	14x96
2716	S2303	-12309	303.5	14x96
2717	S2304	-12320	429.5	14x96
2718	S2305	-12331	177.5	14x96
2719	S2306	-12342	303.5	14x96
2720	S2307	-12353	429.5	14x96
2721	S2308	-12364	177.5	14x96
2722	S2309	-12375	303.5	14x96
2723	S2310	-12386	429.5	14x96
2724	S2311	-12397	177.5	14x96
2725	S2312	-12408	303.5	14x96
2726	S2313	-12419	429.5	14x96
2727	S2314	-12430	177.5	14x96
2728	S2315	-12441	303.5	14x96
2729	S2316	-12452	429.5	14x96
2730	S2317	-12463	177.5	14x96
2731	S2318	-12474	303.5	14x96
2732	S2319	-12485	429.5	14x96
2733	S2320	-12496	177.5	14x96
2734	S2321	-12507	303.5	14x96
2735	S2322	-12518	429.5	14x96
2736	S2323	-12529	177.5	14x96
2737	S2324	-12540	303.5	14x96
2738	S2325	-12551	429.5	14x96
2739	S2326	-12562	177.5	14x96
2740	S2327	-12573	303.5	14x96
2741	S2328	-12584	429.5	14x96
2742	S2329	-12595	177.5	14x96
2743	S2330	-12606	303.5	14x96
2744	S2331	-12617	429.5	14x96
2745	S2332	-12628	177.5	14x96
2746	S2333	-12639	303.5	14x96
2747	S2334	-12650	429.5	14x96
2748	S2335	-12661	177.5	14x96
2749	S2336	-12672	303.5	14x96
2750	S2337	-12683	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2751	S2338	-12694	177.5	14x96
2752	S2339	-12705	303.5	14x96
2753	S2340	-12716	429.5	14x96
2754	S2341	-12727	177.5	14x96
2755	S2342	-12738	303.5	14x96
2756	S2343	-12749	429.5	14x96
2757	S2344	-12760	177.5	14x96
2758	S2345	-12771	303.5	14x96
2759	S2346	-12782	429.5	14x96
2760	S2347	-12793	177.5	14x96
2761	S2348	-12804	303.5	14x96
2762	S2349	-12815	429.5	14x96
2763	S2350	-12826	177.5	14x96
2764	S2351	-12837	303.5	14x96
2765	S2352	-12848	429.5	14x96
2766	S2353	-12859	177.5	14x96
2767	S2354	-12870	303.5	14x96
2768	S2355	-12881	429.5	14x96
2769	S2356	-12892	177.5	14x96
2770	S2357	-12903	303.5	14x96
2771	S2358	-12914	429.5	14x96
2772	S2359	-12925	177.5	14x96
2773	S2360	-12936	303.5	14x96
2774	S2361	-12947	429.5	14x96
2775	S2362	-12958	177.5	14x96
2776	S2363	-12969	303.5	14x96
2777	S2364	-12980	429.5	14x96
2778	S2365	-12991	177.5	14x96
2779	S2366	-13002	303.5	14x96
2780	S2367	-13013	429.5	14x96
2781	S2368	-13024	177.5	14x96
2782	S2369	-13035	303.5	14x96
2783	S2370	-13046	429.5	14x96
2784	S2371	-13057	177.5	14x96
2785	S2372	-13068	303.5	14x96
2786	S2373	-13079	429.5	14x96
2787	S2374	-13090	177.5	14x96
2788	S2375	-13101	303.5	14x96
2789	S2376	-13112	429.5	14x96
2790	S2377	-13123	177.5	14x96
2791	S2378	-13134	303.5	14x96
2792	S2379	-13145	429.5	14x96
2793	S2380	-13156	177.5	14x96
2794	S2381	-13167	303.5	14x96
2795	S2382	-13178	429.5	14x96
2796	S2383	-13189	177.5	14x96
2797	S2384	-13200	303.5	14x96
2798	S2385	-13211	429.5	14x96
2799	S2386	-13222	177.5	14x96
2800	S2387	-13233	303.5	14x96

No.	Name	X	Y	Bump size (μm)
2801	S2388	-13244	429.5	14x96
2802	S2389	-13255	177.5	14x96
2803	S2390	-13266	303.5	14x96
2804	S2391	-13277	429.5	14x96
2805	S2392	-13288	177.5	14x96
2806	S2393	-13299	303.5	14x96
2807	S2394	-13310	429.5	14x96
2808	S2395	-13321	177.5	14x96
2809	S2396	-13332	303.5	14x96
2810	S2397	-13343	429.5	14x96
2811	S2398	-13354	177.5	14x96
2812	S2399	-13365	303.5	14x96
2813	S2400	-13376	429.5	14x96
2814	VSSA	-13387	177.5	14x96
2815	VSSA	-13398	303.5	14x96
2816	VSSA	-13409	429.5	14x96
2817	VCOM_R	-13420	177.5	14x96
2818	VCOM_R	-13431	303.5	14x96
2819	VCOM_R	-13442	429.5	14x96

No.	Name	X	Y	Bump size (μm)
2820	VCOM_R	-13453	177.5	14x96
2821	VCOM_R	-13464	303.5	14x96
2822	VCOM_R	-13475	429.5	14x96
2823	VSSA	-13486	177.5	14x96
2824	VSSA	-13497	303.5	14x96
2825	VSSA	-13508	429.5	14x96
2826	CA_R0	-13597.5	450	100x55
2827	GIO_R0	-13597.5	375	100x55
2828	DUMMY	-13597.5	300	100x55
2829	CA_R1	-13597.5	225	100x55
2830	GIO_R1	-13597.5	150	100x55
2831	DUMMY	-13597.5	75	100x55
2832	CA_R2	-13597.5	0	100x55
2833	GIO_R2	-13597.5	-75	100x55
2834	DUMMY	-13597.5	-150	100x55
2835	CA_3	-13597.5	-225	100x55
2836	GIO_R3	-13597.5	-300	100x55
2837	DUMMY	-13597.5	-375	100x55
2838	GIO_R4	-13597.5	-450	100x55

13. Ordering Information

Part no.	Package
HX8249-A01XPDxxx	X: mean fab code PD: mean COG xxx: mean chip thickness **(μm)**