DATA SHEET

(DOC No. HX8250-A-DS)

HX8250-A

960CH TFT LCD Source Driver
with TCON

Preliminary version 04 February, 2007

Himax Technologies, Inc.
http://www.himax.com.tw

1. General Description

HX8250-A is a 960-channel outputs source driver with TCON, OSD mixer, and 3-wire Serial Port Interface. It also supports 2-chip cascade mode to extend source channel to be 1920 channels.

The interface follows digital 8-bit serial/24-bit parallel RGB, CCIR601 and CCIR656 input format. The TCON generates the 960x240, 1920x240, and 1920x480 resolution and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales.

The source driver receives 6-bit by 3 dots of digital display data per clock from TCON and generates corresponding 64-level gray scale voltage output. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation. Therefore, a high quality display with less crosstalk can be achieved.

2. Features

TCON

- Support display resolution 960x240, 1920x240, and 1920x480
- Support digital 8-bit serial RGB, CCIR601, and CCIR656 input mode
- Support digital 24-bit parallel RGB input mode
- Internal dithering 8-bit data to 6-bit data for Source Driver Circuit
- Only support stripe types of panel group
- Operation frequency: 40 MHz max
- Support NTSC/PAL TV system
- OSD overlay supported in CCIR601and CCIR656 input mode
- Provide source and gate drivers control timing
- Provide flip and mirror scan control
- Operation Voltage Level 2.7V to 3.6V

Source Driver

- 960 channels output source driver for TFT LCD panel
- Dynamic output range: 0.1 to VDD-0.1V
- Voltage deviation of outputs: ±20mV
- Dot inversion driving scheme
- Right and left shift capability
- LCD power: 6.5 to 13.5V

Others

- COG package

3. Block Diagram

3.1 Whole chip block diagram

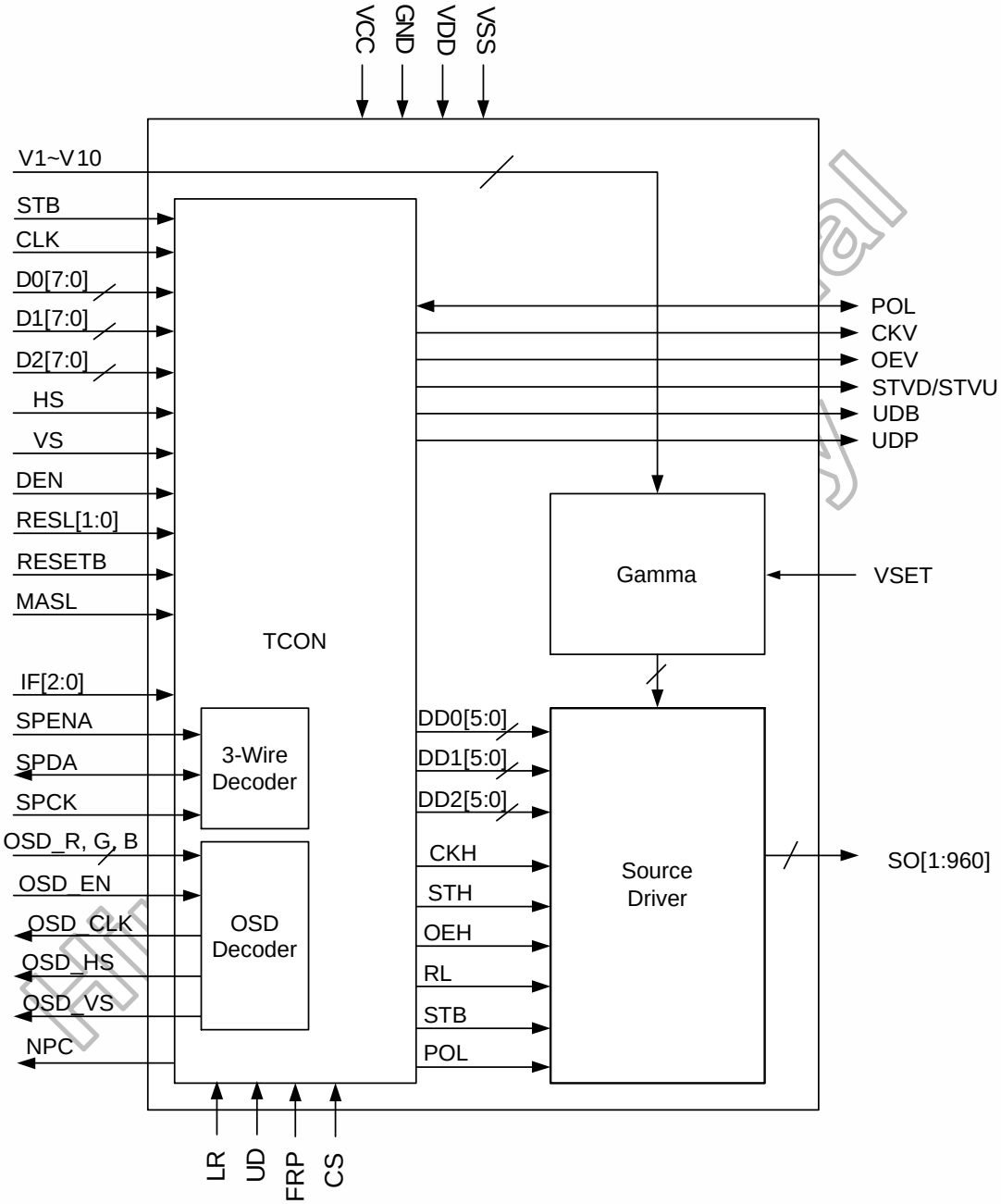


Figure 3. 1 HX8250-A block diagram

3.2 Source driver block diagram

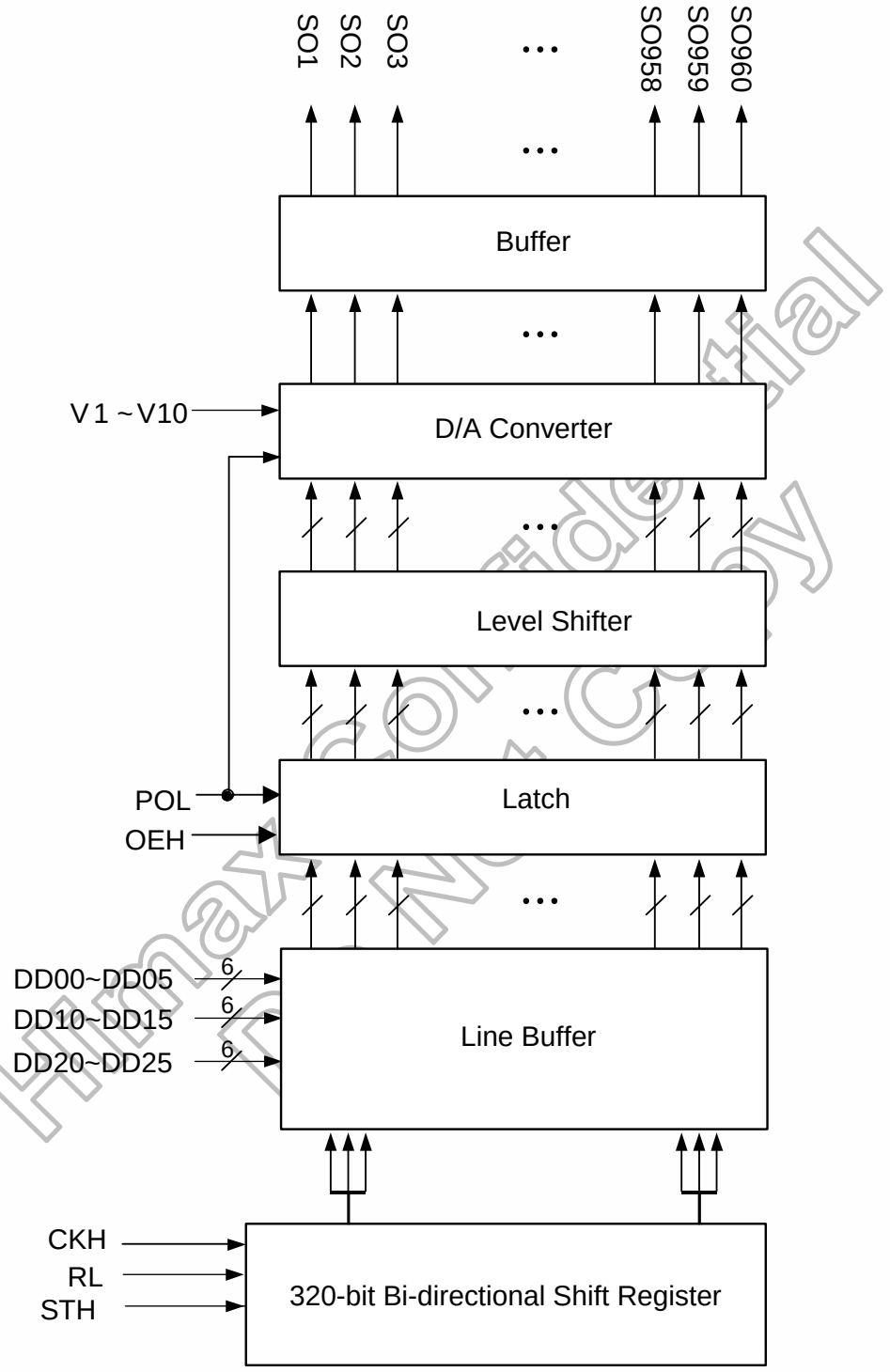


Figure 3. 2 Source driver block diagram

4. Pin description

Pin name	I/O	Description
CLK	I	Clock signal. Latching data at the rising edge.
D07~D00 D17~D10 D27~D20	I	Digital data input. DX0 is LSB and DX7 is MSB. 1. If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G, and B data in turn. 2. If serial RGB or CCIR601 or CCIR656 input mode is selected, only D07~D00 are used, and others short to GND. When disable dithering function, please use DX07~DX02 as 6-bit input.
HS	I	Horizontal sync input in digital RGB and CCIR601 mode. (Short to GND if not used)
VS	I	Vertical sync input in digital RGB and CCIR601 mode. (Short to GND if not used)
DEN	I	Input data enable control. When DE mode, active High to enable data input. Default pull low.
NPC	O	NTSC or PAL mode auto detection result. When NPC=H, NTSC mode is selected. When NPC=L, PAL mode is selected.
RESETB	I	Hardware global reset. Low active. Default pull high.
MASL	I	Master and slave mode selection. Default pull high. Only used in cascade mode. MASL = “H”, for Master mode. MASL = “L”, for Slave mode.
POL_I	I	Sync control input signal in cascade mode. Default pull low. When used as slave chip in cascade mode, receive the sync control signal from master chip. Please keep open when no use.
POL_O	O	Sync control output signal in cascade mode. When used as master chip in cascade mode, output sync control signal to next slave chip. POL_O will keep Hi-Z when no use.
LR	I	The shift direction of device internal shift register is controlled by this pin as shown below: LR=H: STH à SO1 à • • • à SO960 à STHO LR=L: STH à SO960 à • • • à SO1 à STHO
UD	I	Up/down scan setting. When UD=H, reverse scan. When UD=L, normal scan.
IF[2:0]	I	Control the input data format. IF[2:0] / Input data format 000 / 8-bit Serial RGB 001 (default) / 24-bit Parallel RGB 010 / CCIR601 mode A 24.54MHz 011 / CCIR601 mode B 24.54MHz 100 / CCIR601 mode A 27MHz 101 / CCIR601 mode B 27MHz 110 / CCIR656 mode A 27MHz 111 / CCIR656 mode B 27MHz
RESL[1:0]	I	Control the resolution selection. RESL[1:0] / Resolution 00 / 960x240 01 / 1920x240 10 (default) / 1920x480 (parallel RGB only) 11 / reserved

FRP	I	Select normally white or normally black panel. Default pull low. FRP=L, pass the input data for normally white panel. FRP=H, inverse the input data for normally black panel.
CS	I	Charge share function control. Default pull high. CS=L, disable charge share function. CS=H, enable charge share function.
STB	I	Standby mode control. Default pull high. When STB=L, TCON and source driver are off. When STB=H, all the functions are on.
VSET	I	Gamma correction voltage can be set to input 4 voltage levels or 10 voltage levels externally. Default pull low. VSET=L, only externally input V1, V5, V6 and V10 reference voltage, others reference voltage are generated by internal resistors. VSET=H, externally input V1~V10 reference voltage. No matter what setting, it doesn't need OPA buffer to the reference inputs.
V1~V10	I	Used as reference voltage input pins. Hold the reference voltage fixed during the period of LCD drive output. To ensure the correct analog voltage is output from D/A converter, the V1~V10 must be stable before D/A conversion. VDD>V1>V2>V3>V4>V5>V6>V7>V8>V9>V10>VSS.
SPCK	I	Serial port Clock. Default pull high.
SPDA	I/O	Serial port Data input/output. Default pull high.
SPENA	I	Serial port Data Enable Signal. Default pull high.
CKV	O	Gate driver clock.
OEV	O	Enable output control of gate driver.
STVD	O	Start pulse for gate driver. When UD=L, STVD is output. When UD=H, STVD is Hi-Z.
STVU	O	Start pulse for gate driver. When UD=L, STVU is Hi-Z. When UD=H, STVU is output.
UDB	O	Reverse of UD.
UDP	O	Internal link to UD.
OSD_HS	O	OSD Hsync output.
OSD_VS	O	OSD Vsync output.
OSD_CLK	O	OSD clock output.
OSD_R	I	OSD red data input. Default pull low.
OSD_G	I	OSD green data input. Default pull low.
OSD_B	I	OSD blue data input. Default pull low.
OSD_EN	I	OSD enable input. Default pull low. OSD_EN=H : OSD enable. OSD_EN=L : OSD disable.
SO1~SO960	O	Output driver signal.
TEST1	I	Test pins. Default pull low.
TEST2	I	Test pins. Default pull low.
TP[7:0]	O	Test pins. They must be open.
TESTO	O	Test pin. It must be open.
TESTG[3:0]	I	Test pins. Default pull low.
TESTGO	O	Test pin. It must be open.
VDD	I	Analog power. 6.5V to 13.5V.
VSS	I	Analog ground.
VCC	I	Digital power. 2.7V to 3.6V.
GND	I	Digital ground.

PASSR1 PASSR2	-	Link together internally. Please use as signal path, not power path.
PASSL1 PASSL2	-	Link together internally. Please use as signal path, not power path.
PASS1 PASS2	-	Link together internally. Please use as signal path, not power path.

Note: (1) Please power on following the sequence VCC **à** logic input **à** VDD and V1 ~ V10. Reverse the sequence to shut down.

(2) To stabilize the supply voltages, please be sure to insert a 0.1uF bypass capacitor between VCC-GND and VDD-VSS. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01uF is also advised between the gamma-corrected power supply terminals (V1, V2, …, V10) and VSS.

(3) Please keep V1~V10 not cross to the toggle signals as possible to avoid the AC coupling on the DC V1~V10 voltage. When used as cascade mode, please keep the coupled amount of V1~V10 are the same between the two chip.

(4) The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommended as below.

Pin Name	Wiring resistance value(Ω)
VCC(3.3V)	< 30
GND(0V)	< 30
VDD(8.4V)	< 5
VSS(0V)	< 5
V1 ~ V10	< 100
CLK	< 100
Dx7 ~ Dx0	< 200
HS	< 200
VS	< 200
DE	< 200
POL_O to POL_I (cascade mode)	< 200
OSD_R, OSD_G, OSD_B OSD_HS, OSD_VS, OSD_CLK	< 200
Others	< 1000

5. Operation description

5.1 Relationship between input data and output channels

I Source Driver

LR	First					→				Last
H	Out1	Out2	Out3	•••	•••	•••	•••	Out958	Out959	Out960

LR	Last					←				First
L	Out960	Out959	Out958	•••	•••	•••	•••	Out3	Out2	Out1

Table 5. 1 Relationship between input data and output channels

5.2 HX8250-A chip locations with LR and UD control

HX8250-A can be controlled Left/Right shift and Up/Down scan by LR and UD pins. The setting depends on HX8250-A and Gate Driver positions with panel. Please reference to below diagram to set the LR and UD.

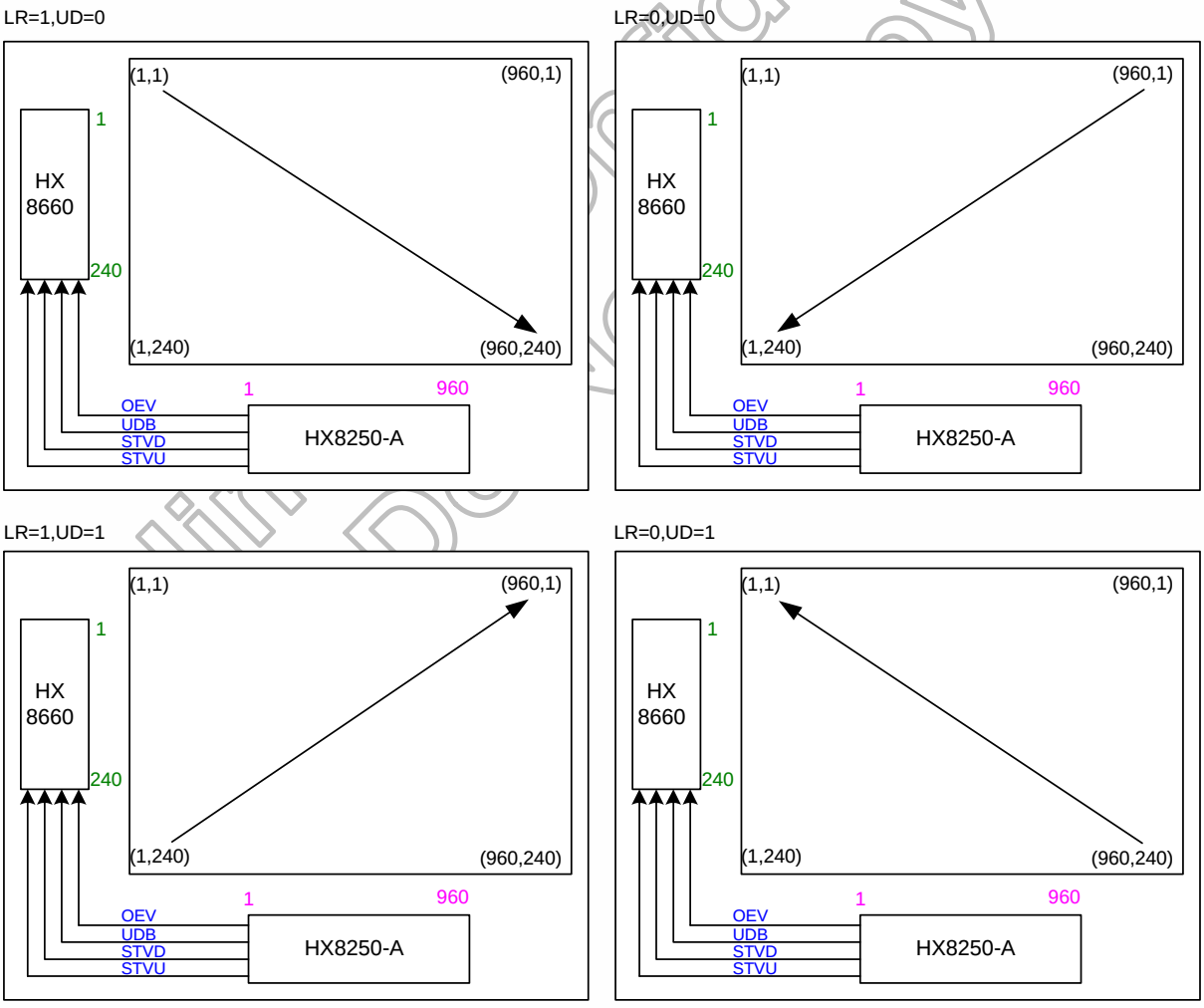


Figure 5. 1 HX8250-A chip location put down side and Gate Driver put left side.

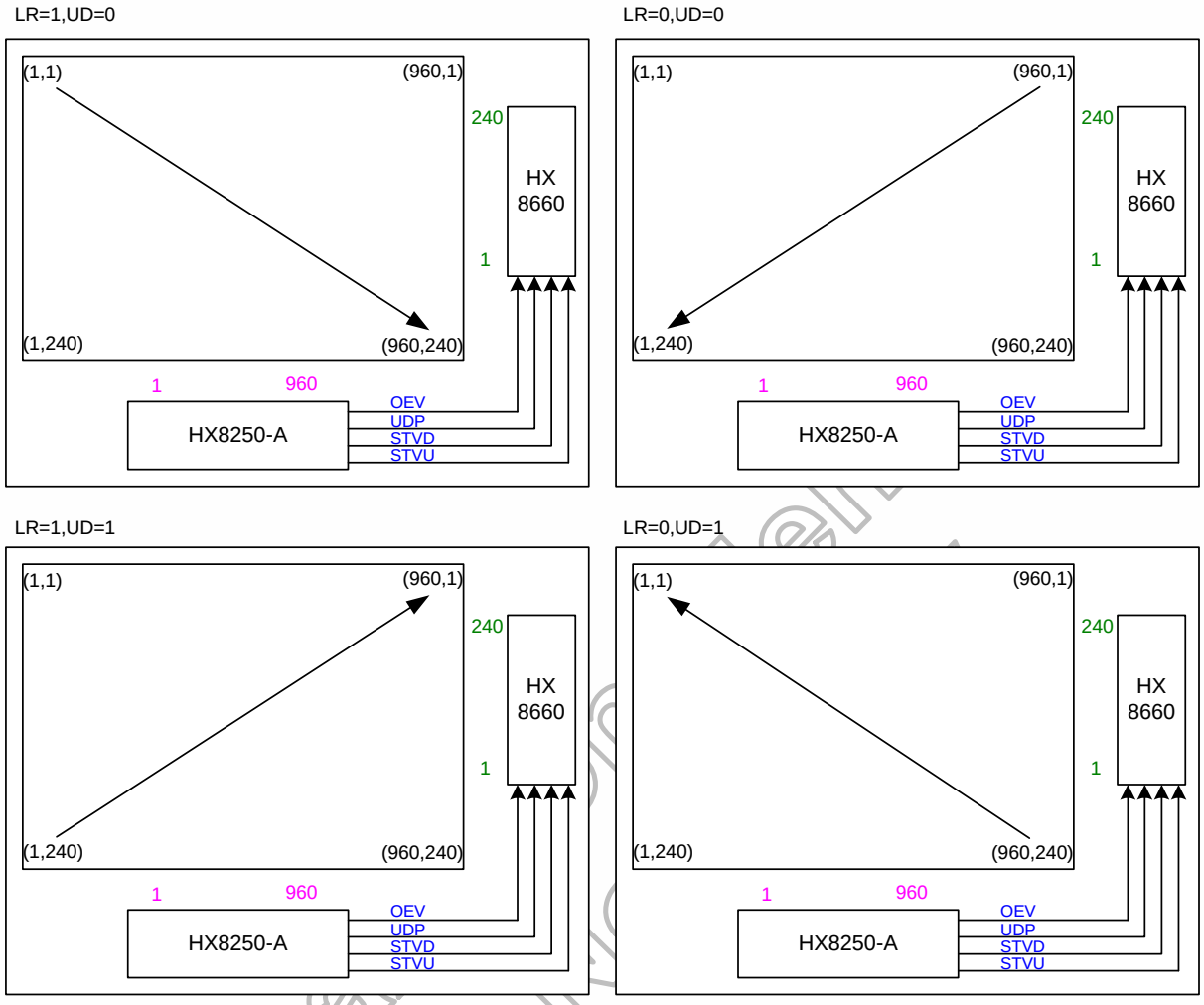


Figure 5. 2 HX8250-A chip put down side and Gate Driver put right side.

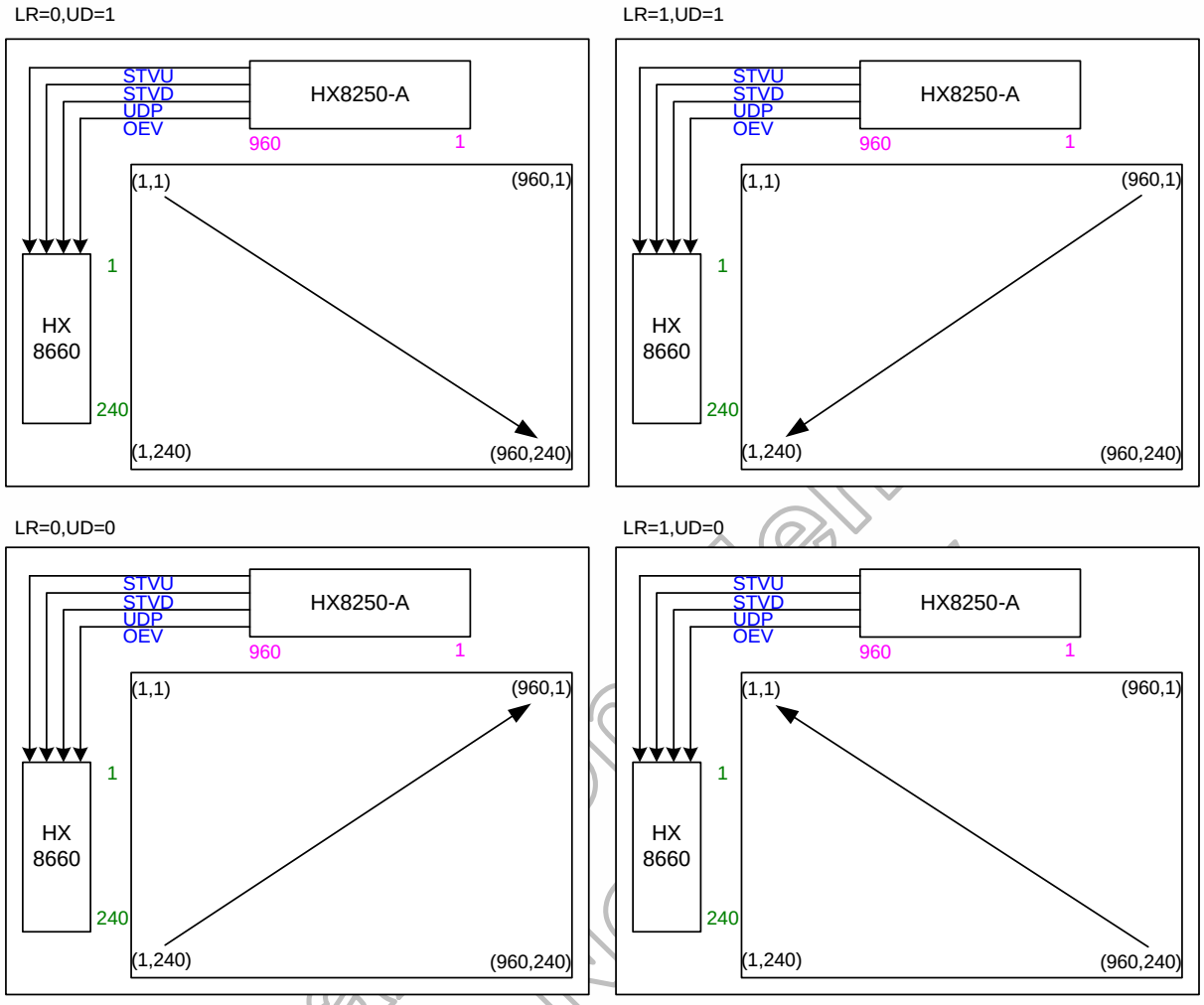


Figure 5. 3 HX8250-A chip put up side and Gate Driver put left side.

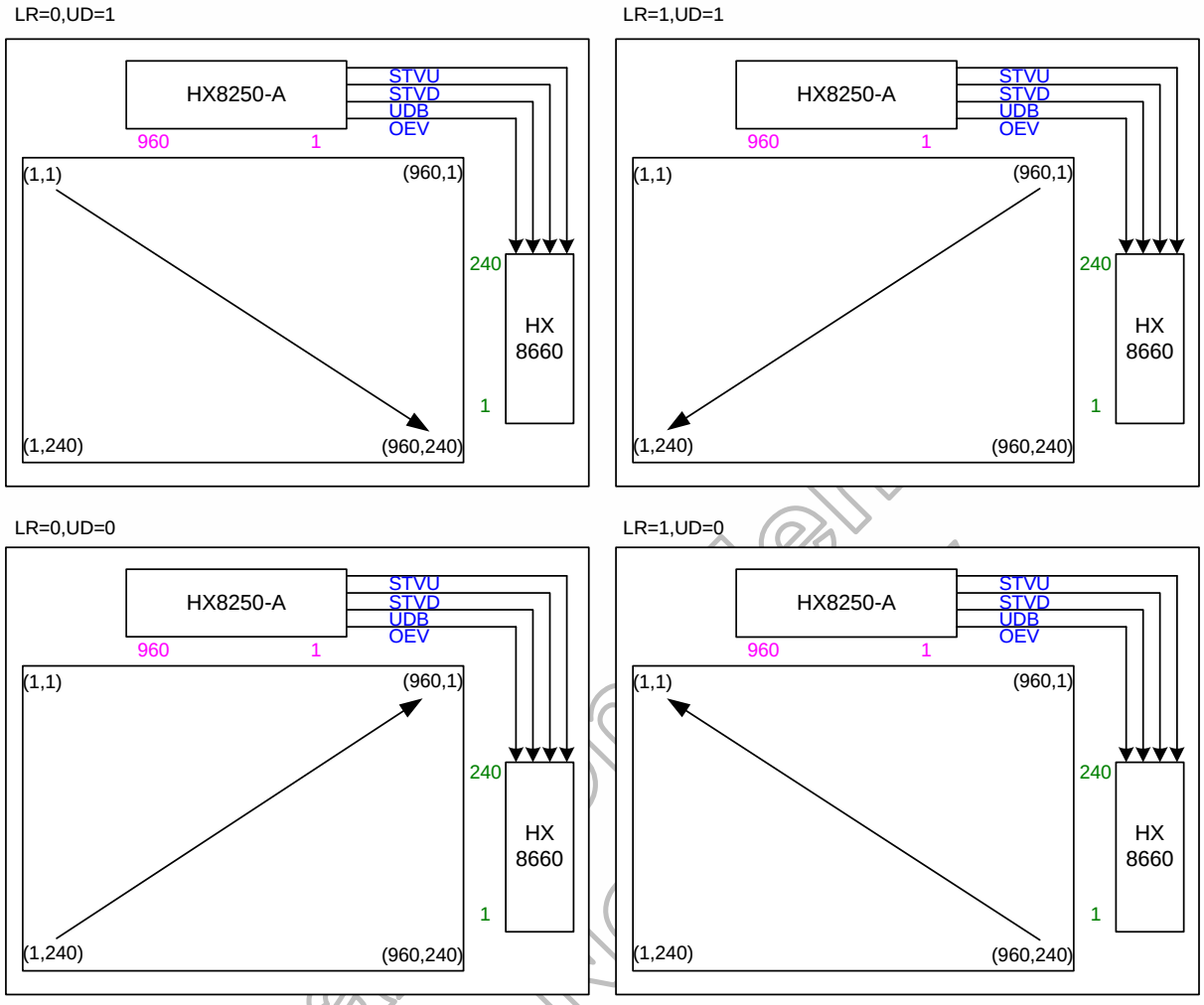


Figure 5. 4 HX8250-A chip put up side and Gate Driver put Left side.

5.3 Digital RGB data input format

For digital RGB input data format, both SYNC mode and DE mode are supported. HX8250-A will auto detect which mode is used. If DEN signal is fixed low, SYNC mode is used. Otherwise, DE mode is used. The OSD function is not supported in digital serial/parallel RGB mode.

5.4 NTSC/PAL mode auto detection

For NTSC/PAL mode setting, the auto-detection function is implemented. You don't have to define this setting and can use NPC pin to monitor detection result.

5.5 Cascade mode for 1920x240, 1920x480 resolutions

HX8250-A supports 1920x240 and 1920x480 resolutions by cascade 2 chips. When connect to cascade mode, user need to set MASL pin to define which chip is master mode or slave mode. Master chip and slave chip are decided by the fixed position. Always master chip's SO960 is neighbor to slave chip's SO1.

It needs to receive the polarity signal from the master chip for the polarity synchronized. Please always connect POL_O of Master chip to POL_I of Slave chip. POL_I of Master chip and POL_O of Slave chip could keep NC. Please reference to the following diagrams.

Signals to gate driver could be provided by master chip or slave chip. Each side of master chip or slave chip could provide the gate signals, and user can chooses the closer side to connect with gate driver.

Please minimize the parasitic R of the POL path. The parasitic R should be smaller than 200 ohm.

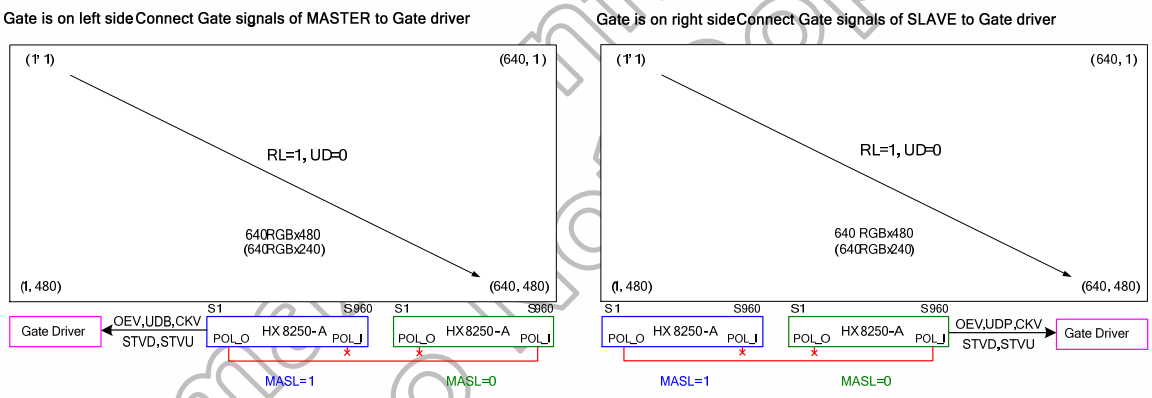


Figure 5. 5 2-chip cascade for 1920x480

5.6 Relationship between gamma correction and output voltage

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V10 gamma correction reference voltage inputs.

Gamma correction characteristic curve:

Figure 5. 6 Gamma correction characteristic curve

Gamma correction resistor ratio: (1 unit = 125ohm)

V1, V10 →

Name	Resistor	Name	Resistor
R0	6.4	R32	0.8
R1	6	R33	0.8
R2	5.6	R34	0.8
R3	5.2	R35	0.8
R4	4.8	R36	0.8
R5	4.4	R37	0.8
R6	4.4	R38	0.8
R7	4	R39	0.8
R8	4	R40	0.8
R9	3.2	R41	0.8
R10	3.2	R42	0.8
R11	2.8	R43	0.8
R12	2.8	R44	0.8
R13	2.8	R45	0.8
R14	2.4	R46	0.8
R15	2.4	R47	0.8
R16	2.4	R48	0.8
R17	2	R49	0.8
R18	2	R50	0.8
R19	2	R51	0.8
R20	1.6	R52	0.8
R21	1.6	R53	1.2
R22	1.6	R54	1.2
R23	1.2	R55	1.2
R24	1.2	R56	1.6
R25	1.2	R57	1.6
R26	1.2	R58	2
R27	0.8	R59	2
R28	0.8	R60	2.4
R29	0.8	R61	4
R30	0.8	R62	6.4
R31	0.8		

V2, V9 →

← V4, V7

← V5, V6

V3, V8 →

Output Voltages vs. Source Input Data when VSET=H:
Please input V1~V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V2 + (V1 – V2)X 58 / 64.4	V10 + (V9 – V10)X 6.4 / 64.4
02H	V2 + (V1 – V2)X 52 / 64.4	V10 + (V9 – V10)X 12.4 / 64.4
03H	V2 + (V1 – V2)X 46.4 / 64.4	V10 + (V9 – V10)X 18 / 64.4
04H	V2 + (V1 – V2)X 41.2 / 64.4	V10 + (V9 – V10)X 23.2 / 64.4
05H	V2 + (V1 – V2)X 36.4 / 64.4	V10 + (V9 – V10)X 28 / 64.4
06H	V2 + (V1 – V2)X 32 / 64.4	V10 + (V9 – V10)X 32.4 / 64.4
07H	V2 + (V1 – V2)X 27.6 / 64.4	V10 + (V9 – V10)X 36.8 / 64.4
08H	V2 + (V1 – V2)X 23.6 / 64.4	V10 + (V9 – V10)X 40.8 / 64.4
09H	V2 + (V1 – V2)X 19.6 / 64.4	V10 + (V9 – V10)X 44.8 / 64.4
0AH	V2 + (V1 – V2)X 16.4 / 64.4	V10 + (V9 – V10)X 48 / 64.4
0BH	V2 + (V1 – V2)X 13.2 / 64.4	V10 + (V9 – V10)X 51.2 / 64.4
0CH	V2 + (V1 – V2)X 10.4 / 64.4	V10 + (V9 – V10)X 54 / 64.4
0DH	V2 + (V1 – V2)X 7.6 / 64.4	V10 + (V9 – V10)X 56.8 / 64.4
0EH	V2 + (V1 – V2)X 4.8 / 64.4	V10 + (V9 – V10)X 59.6 / 64.4
0FH	V2 + (V1 – V2)X 2.4 / 64.4	V10 + (V9 – V10)X 62 / 64.4
10H	V2	V9
11H	V3 + (V2 – V3) X 19.6 / 22	V9 + (V8 – V9)X 2.4 / 22
12H	V3 + (V2 – V3) X 17.6 / 22	V9 + (V8 – V9)X 4.4 / 22
13H	V3 + (V2 – V3) X 15.6 / 22	V9 + (V8 – V9)X 6.4 / 22
14H	V3 + (V2 – V3) X 13.6 / 22	V9 + (V8 – V9)X 8.4 / 22
15H	V3 + (V2 – V3) X 12 / 22	V9 + (V8 – V9)X 10 / 22
16H	V3 + (V2 – V3) X 10.4 / 22	V9 + (V8 – V9)X 11.6 / 22
17H	V3 + (V2 – V3) X 8.8 / 22	V9 + (V8 – V9)X 13.2 / 22
18H	V3 + (V2 – V3) X 7.6 / 22	V9 + (V8 – V9)X 14.4 / 22
19H	V3 + (V2 – V3) X 6.4 / 22	V9 + (V8 – V9)X 15.6 / 22
1AH	V3 + (V2 – V3) X 5.2 / 22	V9 + (V8 – V9)X 16.8 / 22
1BH	V3 + (V2 – V3) X 4 / 22	V9 + (V8 – V9)X 18 / 22
1CH	V3 + (V2 – V3) X 3.2 / 22	V9 + (V8 – V9)X 18.8 / 22
1DH	V3 + (V2 – V3) X 2.4 / 22	V9 + (V8 – V9)X 19.6 / 22
1EH	V3 + (V2 – V3) X 1.6 / 22	V9 + (V8 – V9)X 20.4 / 22
1FH	V3 + (V2 – V3) X 0.8 / 22	V9 + (V8 – V9)X 21.2 / 22

Output Voltages vs. Source Input Data when VSET=H (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V3	V8
21H	V4 + (V3 – V4) X 12 / 12.8	V8 + (V7 – V8) X 0.8 / 12.8
22H	V4 + (V3 – V4) X 11.2 / 12.8	V8 + (V7 – V8) X 1.6 / 12.8
23H	V4 + (V3 – V4) X 10.4 / 12.8	V8 + (V7 – V8) X 2.4 / 12.8
24H	V4 + (V3 – V4) X 9.6 / 12.8	V8 + (V7 – V8) X 3.2 / 12.8
25H	V4 + (V3 – V4) X 8.8 / 12.8	V8 + (V7 – V8) X 4 / 12.8
26H	V4 + (V3 – V4) X 8 / 12.8	V8 + (V7 – V8) X 4.8 / 12.8
27H	V4 + (V3 – V4) X 7.2 / 12.8	V8 + (V7 – V8) X 5.6 / 12.8
28H	V4 + (V3 – V4) X 6.4 / 12.8	V8 + (V7 – V8) X 6.4 / 12.8
29H	V4 + (V3 – V4) X 5.6 / 12.8	V8 + (V7 – V8) X 7.2 / 12.8
2AH	V4 + (V3 – V4) X 4.8 / 12.8	V8 + (V7 – V8) X 8 / 12.8
2BH	V4 + (V3 – V4) X 4 / 12.8	V8 + (V7 – V8) X 8.8 / 12.8
2CH	V4 + (V3 – V4) X 3.2 / 12.8	V8 + (V7 – V8) X 9.6 / 12.8
2DH	V4 + (V3 – V4) X 2.4 / 12.8	V8 + (V7 – V8) X 10.4 / 12.8
2EH	V4 + (V3 – V4) X 1.6 / 12.8	V8 + (V7 – V8) X 11.2 / 12.8
2FH	V4 + (V3 – V4) X 0.8 / 12.8	V8 + (V7 – V8) X 12 / 12.8
30H	V4	V7
31H	V5 + (V4 – V5) X 26.8 / 27.6	V7 + (V6 – V7) X 0.8 / 27.6
32H	V5 + (V4 – V5) X 26 / 27.6	V7 + (V6 – V7) X 1.6 / 27.6
33H	V5 + (V4 – V5) X 25.2 / 27.6	V7 + (V6 – V7) X 2.4 / 27.6
34H	V5 + (V4 – V5) X 24.4 / 27.6	V7 + (V6 – V7) X 3.2 / 27.6
35H	V5 + (V4 – V5) X 23.6 / 27.6	V7 + (V6 – V7) X 4 / 27.6
36H	V5 + (V4 – V5) X 22.4 / 27.6	V7 + (V6 – V7) X 5.2 / 27.6
37H	V5 + (V4 – V5) X 21.2 / 27.6	V7 + (V6 – V7) X 6.4 / 27.6
38H	V5 + (V4 – V5) X 20 / 27.6	V7 + (V6 – V7) X 7.6 / 27.6
39H	V5 + (V4 – V5) X 18.4 / 27.6	V7 + (V6 – V7) X 9.2 / 27.6
3AH	V5 + (V4 – V5) X 16.8 / 27.6	V7 + (V6 – V7) X 10.8 / 27.6
3BH	V5 + (V4 – V5) X 14.8 / 27.6	V7 + (V6 – V7) X 12.8 / 27.6
3CH	V5 + (V4 – V5) X 12.8 / 27.6	V7 + (V6 – V7) X 14.8 / 27.6
3DH	V5 + (V4 – V5) X 10.4 / 27.6	V7 + (V6 – V7) X 17.2 / 27.6
3EH	V5 + (V4 – V5) X 6.4 / 27.6	V7 + (V6 – V7) X 21.2 / 27.6
3FH	V5	V6

Output Voltages vs. Source Input Data when VSET=L:
Please input V1, V5 and V6, V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V5 + (V1 – V5)X 120.4 / 126.8	V10 + (V6 – V10)X 6.4 / 126.8
02H	V5 + (V1 – V5)X 114.4 / 126.8	V10 + (V6 – V10)X 12.4 / 126.8
03H	V5 + (V1 – V5)X 108.8 / 126.8	V10 + (V6 – V10)X 18 / 126.8
04H	V5 + (V1 – V5)X 103.6 / 126.8	V10 + (V6 – V10)X 23.2 / 126.8
05H	V5 + (V1 – V5)X 98.8 / 126.8	V10 + (V6 – V10)X 28 / 126.8
06H	V5 + (V1 – V5)X 94.4 / 126.8	V10 + (V6 – V10)X 32.4 / 126.8
07H	V5 + (V1 – V5)X 90 / 126.8	V10 + (V6 – V10)X 36.8 / 126.8
08H	V5 + (V1 – V5)X 86 / 126.8	V10 + (V6 – V10)X 40.8 / 126.8
09H	V5 + (V1 – V5)X 82 / 126.8	V10 + (V6 – V10)X 44.8 / 126.8
0AH	V5 + (V1 – V5)X 78.8 / 126.8	V10 + (V6 – V10)X 48 / 126.8
0BH	V5 + (V1 – V5)X 75.6 / 126.8	V10 + (V6 – V10)X 51.2 / 126.8
0CH	V5 + (V1 – V5)X 72.8 / 126.8	V10 + (V6 – V10)X 54 / 126.8
0DH	V5 + (V1 – V5)X 70 / 126.8	V10 + (V6 – V10)X 56.8 / 126.8
0EH	V5 + (V1 – V5)X 67.2 / 126.8	V10 + (V6 – V10)X 59.6 / 126.8
0FH	V5 + (V1 – V5)X 64.8 / 126.8	V10 + (V6 – V10)X 62 / 126.8
10H	V5 + (V1 – V5)X 62.4 / 126.8	V10 + (V6 – V10)X 64.4 / 126.8
11H	V5 + (V1 – V5)X 60 / 126.8	V10 + (V6 – V10)X 66.8 / 126.8
12H	V5 + (V1 – V5)X 58 / 126.8	V10 + (V6 – V10)X 68.8 / 126.8
13H	V5 + (V1 – V5)X 56 / 126.8	V10 + (V6 – V10)X 70.8 / 126.8
14H	V5 + (V1 – V5)X 54 / 126.8	V10 + (V6 – V10)X 72.8 / 126.8
15H	V5 + (V1 – V5)X 52.4 / 126.8	V10 + (V6 – V10)X 74.4 / 126.8
16H	V5 + (V1 – V5)X 50.8 / 126.8	V10 + (V6 – V10)X 76 / 126.8
17H	V5 + (V1 – V5)X 49.2 / 126.8	V10 + (V6 – V10)X 77.6 / 126.8
18H	V5 + (V1 – V5)X 48 / 126.8	V10 + (V6 – V10)X 78.8 / 126.8
19H	V5 + (V1 – V5)X 46.8 / 126.8	V10 + (V6 – V10)X 80 / 126.8
1AH	V5 + (V1 – V5)X 45.6 / 126.8	V10 + (V6 – V10)X 81.2 / 126.8
1BH	V5 + (V1 – V5)X 44.4 / 126.8	V10 + (V6 – V10)X 82.4 / 126.8
1CH	V5 + (V1 – V5)X 43.6 / 126.8	V10 + (V6 – V10)X 83.2 / 126.8
1DH	V5 + (V1 – V5)X 42.8 / 126.8	V10 + (V6 – V10)X 84 / 126.8
1EH	V5 + (V1 – V5)X 42 / 126.8	V10 + (V6 – V10)X 84.8 / 126.8
1FH	V5 + (V1 – V5)X 41.2 / 126.8	V10 + (V6 – V10)X 85.6 / 126.8

Output Voltages vs. Source Input Data when VSET=L (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V5 + (V1 – V5)X 40.4 / 126.8	V10 + (V6 – V10)X 86.4 / 126.8
21H	V5 + (V1 – V5)X 39.6 / 126.8	V10 + (V6 – V10)X 87.2 / 126.8
22H	V5 + (V1 – V5)X 38.8 / 126.8	V10 + (V6 – V10)X 88 / 126.8
23H	V5 + (V1 – V5)X 38 / 126.8	V10 + (V6 – V10)X 88.8 / 126.8
24H	V5 + (V1 – V5)X 37.2 / 126.8	V10 + (V6 – V10)X 89.6 / 126.8
25H	V5 + (V1 – V5)X 36.4 / 126.8	V10 + (V6 – V10)X 90.4 / 126.8
26H	V5 + (V1 – V5)X 35.6 / 126.8	V10 + (V6 – V10)X 91.2 / 126.8
27H	V5 + (V1 – V5)X 34.8 / 126.8	V10 + (V6 – V10)X 92 / 126.8
28H	V5 + (V1 – V5)X 34 / 126.8	V10 + (V6 – V10)X 92.8 / 126.8
29H	V5 + (V1 – V5)X 33.2 / 126.8	V10 + (V6 – V10)X 93.6 / 126.8
2AH	V5 + (V1 – V5)X 32.4 / 126.8	V10 + (V6 – V10)X 94.4 / 126.8
2BH	V5 + (V1 – V5)X 31.6 / 126.8	V10 + (V6 – V10)X 95.2 / 126.8
2CH	V5 + (V1 – V5)X 30.8 / 126.8	V10 + (V6 – V10)X 96 / 126.8
2DH	V5 + (V1 – V5)X 30 / 126.8	V10 + (V6 – V10)X 96.8 / 126.8
2EH	V5 + (V1 – V5)X 29.2 / 126.8	V10 + (V6 – V10)X 97.6 / 126.8
2FH	V5 + (V1 – V5)X 28.4/ 126.8	V10 + (V6 – V10)X 98.4 / 126.8
30H	V5 + (V1 – V5)X 27.6 / 126.8	V10 + (V6 – V10)X 99.2 / 126.8
31H	V5 + (V1 – V5)X 26.8 / 126.8	V10 + (V6 – V10)X 100 / 126.8
32H	V5 + (V1 – V5)X 26 / 126.8	V10 + (V6 – V10)X 100.8 / 126.8
33H	V5 + (V1 – V5)X 25.2 / 126.8	V10 + (V6 – V10)X 101.6 / 126.8
34H	V5 + (V1 – V5)X 24.4 / 126.8	V10 + (V6 – V10)X 102.4 / 126.8
35H	V5 + (V1 – V5)X 23.6 / 126.8	V10 + (V6 – V10)X 103.2 / 126.8
36H	V5 + (V1 – V5)X 22.4 / 126.8	V10 + (V6 – V10)X 104.4 / 126.8
37H	V5 + (V1 – V5)X 21.2 / 126.8	V10 + (V6 – V10)X 105.6 / 126.8
38H	V5 + (V1 – V5)X 20 / 126.8	V10 + (V6 – V10)X 106.8 / 126.8
39H	V5 + (V1 – V5)X 18.4 / 126.8	V10 + (V6 – V10)X 108.4 / 126.8
3AH	V5 + (V1 – V5)X 16.8 / 126.8	V10 + (V6 – V10)X 110 / 126.8
3BH	V5 + (V1 – V5)X 14.8 / 126.8	V10 + (V6 – V10)X 112 / 126.8
3CH	V5 + (V1 – V5)X 12.8 / 126.8	V10 + (V6 – V10)X 114 / 126.8
3DH	V5 + (V1 – V5)X 10.4 / 126.8	V10 + (V6 – V10)X 116.4 / 126.8
3EH	V5 + (V1 – V5)X 6.4 / 126.8	V10 + (V6 – V10)X 120.4 / 126.8
3FH	V5	V6

5.7 SPI Register Description

Register Name	Test RW	Address A3	A2	A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	□	□	□	□	□	PSC	STB	RESETB
						□	□	□	□	□	0	0	1
R1	0	0	0	0	1	□	□	□	RESL1	RESL0	IF2	IF1	IF0
						□	□	□	1	0	0	0	1
R2	0	0	0	1	0	□	□	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
						□	□	0	0	0	0	0	0
R3	0	0	0	1	1	□	□	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
						□	□	0	0	0	0	0	0
R4	0	0	1	0	0	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
						1	0	1	1	0	0	0	1
R5	0	0	1	0	1	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	□
						1	0	0	1	0	1	0	□

□ RW must always keep low.
□ "□ "= don`t care.

l Register R0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	PSC	STB	RESETB
Default	-	-	-	-	-	0	0	1

Table 5. 2 Register R0 setting

PSC: Operating mode setting by input pin or SPI register.
PSC="L", set STB, FRP, CS, IF[2:0], RESL[1:0] by input pin.
PSC="H", set STB, FRP, CS, IF[2:0], RESL[1:0] by SPI register.

STB: Standby mode setting.
STB="L", TCON and source driver are off.
STB="H", all the functions are on.

RESETB: Global reset.
RESETB="L", global reset the whole chip.
RESETB="H", Normal operation.

l Register R1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	RESL1	RESL0	IF2	IF1	IF0
Default	—	—	—	1	0	0	0	1

Table 5. 3 Register R1 setting

RESL [1:0]: Display resolution selection.

RESL1	RESL0	Resolution
0	0	960x240
0	1	1920x240
1	0	1920x480 (parallel RGB only)
1	1	reserved

Table 5. 4 Display resolution selection.

IF [2:0]: Data input mode selection.

IF2	IF1	IF0	Data input format	Operating freq
0	0	0	8-bit serial RGB	38.4MHz (Max)
0	0	1	24-bit parallel RGB	25.175MHz (Max)
0	1	0	CCIR601 (YUV mode A)	24.54MHz
0	1	1	CCIR601 (YUV mode B)	24.54MHz
1	0	0	CCIR601 (YUV mode A)	27MHz
1	0	1	CCIR601 (YUV mode B)	27MHz
1	1	0	CCIR656 (YUV mode A)	27MHz
1	1	1	CCIR656 (YUV mode B)	27MHz

Table 5. 5 Data input mode selection.

l Register R2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	—	—	0	0	0	0	0	0

Table 5. 6 Register R2 setting

STHD [5:0]: adjust start pulse position by dot

STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position adjust	Unit
0	0	0	0	0	0	0	T_{CPH}
0	0	0	0	0	1	+1	T_{CPH}
0	0	0	0	1	0	+2	T_{CPH}
0	0	0	0	1	1	+3	T_{CPH}
0	0	0	1	0	0	+4	T_{CPH}
0	0	0	1	0	1	+5	T_{CPH}
0	0	0	1	1	0	+6	T_{CPH}
0	0	0	1	1	1	+7	T_{CPH}
				⋮			
0	1	1	0	0	0	+24	T_{CPH}
0	1	1	0	0	1	+25	T_{CPH}
0	1	1	0	1	0	+26	T_{CPH}
0	1	1	0	1	1	+27	T_{CPH}
0	1	1	1	0	0	+28	T_{CPH}
0	1	1	1	0	1	+29	T_{CPH}
0	1	1	1	1	0	+30	T_{CPH}
0	1	1	1	1	1	+31	T_{CPH}
1	0	0	0	0	0	-1	T_{CPH}
1	0	0	0	0	1	-2	T_{CPH}
1	0	0	0	1	0	-3	T_{CPH}
1	0	0	0	1	1	-4	T_{CPH}
1	0	0	1	0	0	-5	T_{CPH}
1	0	0	1	0	1	-6	T_{CPH}
1	0	0	1	1	0	-7	T_{CPH}
1	0	0	1	1	1	-8	T_{CPH}
				⋮			
1	1	1	0	0	0	-25	T_{CPH}
1	1	1	0	0	1	-26	T_{CPH}
1	1	1	0	1	0	-27	T_{CPH}
1	1	1	0	1	1	-28	T_{CPH}
1	1	1	1	0	0	-29	T_{CPH}
1	1	1	1	0	1	-30	T_{CPH}
1	1	1	1	1	0	-31	T_{CPH}
1	1	1	1	1	1	-32	T_{CPH}

Table 5. 7 Adjust start pulse position by dot

l Register R3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
Default	–	–	0	0	0	0	0	0

Table 5. 8 Register R3 setting

STVP [3:0]: adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STV position adjust	Unit
0	0	0	0	0	T_H
0	0	0	1	+1	T_H
0	0	1	0	+2	T_H
0	0	1	1	+3	T_H
0	1	0	0	+4	T_H
0	1	0	1	+5	T_H
0	1	1	0	+6	T_H
0	1	1	1	+7	T_H
1	0	0	0	-1	T_H
1	0	0	1	-2	T_H
1	0	1	0	-3	T_H
1	0	1	1	-4	T_H
1	1	0	0	-5	T_H
1	1	0	1	-6	T_H
1	1	1	0	-7	T_H
1	1	1	1	-8	T_H

Table 5. 9 Adjust first line position by line

FRAD [1:0]: Odd frame or Even frame advance control.

FRAD1	FRAD0	Advance Frame	Notes
0	0	Default	Odd/Even frame Tstv are the same
0	1	Odd frame	Even frame Tstv = STVP setting + 1H
1	0	Even frame	Odd frame Tstv = STVP setting + 1H
1	1	Reserve	Reserve

Note: Please set the FRAD[1:0]=01 when CCIR601 NTSC/PAL、CCIR656 PAL mode；set the PRAD[1:0]=00 when CCIR656 NTSC mode for video decoder SAA7114。(Please refer the input timing of the “8.1.3 Data input format for CCIR601 Mode”)

Table 5. 10 Odd frame or Even frame advance control

l Register R4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
Default	1	0	1	1	0	0	0	1

Table 5. 11 Register R4 setting

CS: Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function.

FRP: Select normally white or normally black panel.
FRP=L, pass the input data for normally white panel.
FRP=H, inverse the input data for normally black panel.

FRC: Dithering ON/OFF control.
FRC=L, Dithering function disable.
FRC=H, Dithering function enable

LPF: Low pass filter function enable/disable in CCIR656/CCIR601 mode
LPF=”L”, Low pass filer function disable
LPF=”H”, Low pass filer function enable

VS_POL: VS polarity setting.
VS_POL=L, negative polarity.
VS_POL=H, positive polarity.

Note: Please set the VS_POL=H when CCIR601 mode for video decoder SAA7114.
(Please refer the input timing of the “8.1.3 Data input format for CCIR601 Mode”)

HS_POL: HS polarity setting.
HS_POL=L, negative polarity.
HS_POL=H, positive polarity.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.
NPC_SET=L, auto detection.
NPC_SET=H, define by NPC_IN.

NPC_IN: Define the NTSC/PAL mode by SPI.
NPC_IN=L, PAL.
NPC_IN=H, NTSC.

l Register R5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	reserved
Default	1	0	0	1	0	1	0	–

Table 5. 12 Register R5 setting

AUTO_DP: When power on, select blank image display time decided by A_TIME (bit 5, 4) or DISP_ON (bit 6).
AUTO_DP =”L”, Blank image display time decided by DISP_ON (bit 6).
AUTO_DP =”H”, Blank image display time decided by A_TIME(bit 5, 4).

DISP_ON: When AUTO_DP (bit 7) = ”L”, and DISP_ON = ”H”, blank image display off, then display normal image.

A_TIME [1:0]: When AUTO_DP(bit 7) = ”H”, the blank image display time is decided by A_TIME
00: blank image display time is 8 VS time.
01: blank image display time is 16 VS time.
10: blank image display time is 32 VS time.
11: blank image display time is 64 VS time.

B_TIME [2:0]: When into STB mode, the blank image display time is decided by B_TIME.
000: blank image display time is 3 VS time.
001: blank image display time is 4 VS time.
010: blank image display time is 5 VS time.
011: blank image display time is 6 VS time.
100: blank image display time is 7 VS time.
101: blank image display time is 8 VS time.
110: blank image display time is 9 VS time.
111: blank image display time is 10 VS time.

5.8 Power ON/OFF sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC, GND **à** VDD, VSS **à** V1 to V10
Power OFF: V1 to V10 **à** VDD, VSS **à** VCC, GND

5.9 Power ON Control

HX8250-A has a power ON sequence control function. There are two kinds of the mode. One is auto mode, and another is manual mode.

Auto Mode: When power is ON, blank data is outputted for 16-frames (default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TIME1(bit 5) and A_TIME0(bit 4) when AUTO_DP(bit 7) = ”H”

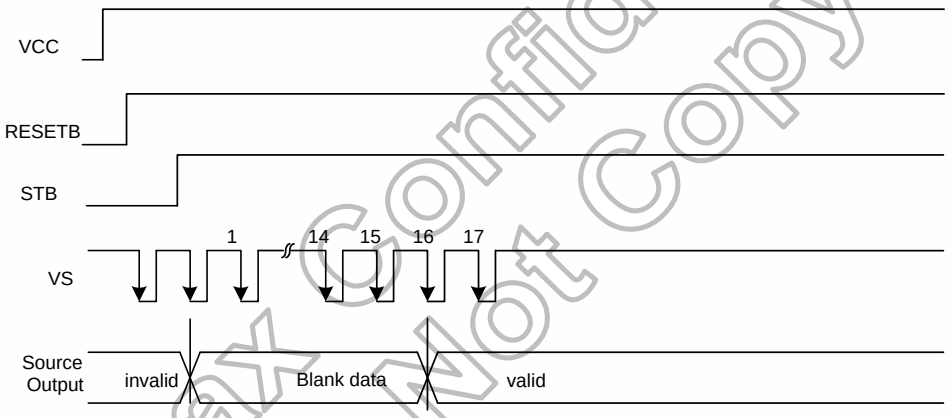


Figure 5. 7 Power on control for Auto Mode

Manual Mode: When power is ON, you should set the register R5 AUTO_DP(bit 7) = ”L” to stay at the manual mode. Blank data is outputted until the DISP_ON(bit 6) = H then display the normal image.

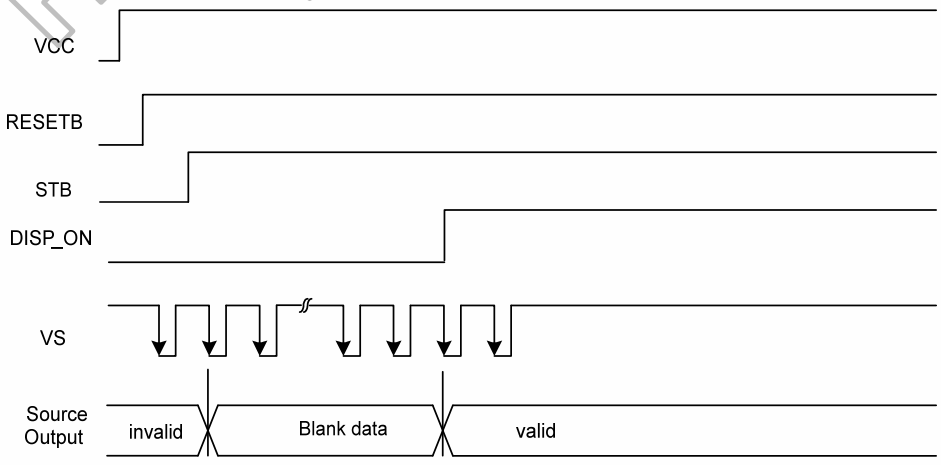


Figure 5. 8 Power on control for Manual Mode

5.10 Standby ON/OFF Control

HX8250-A has a standby ON/OFF sequence control function. When STB pin is “L”, blank data is outputted for 5-frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel. It can be defined in register R5 B_TIME[2:0] to adjust the frame number of the blank data.

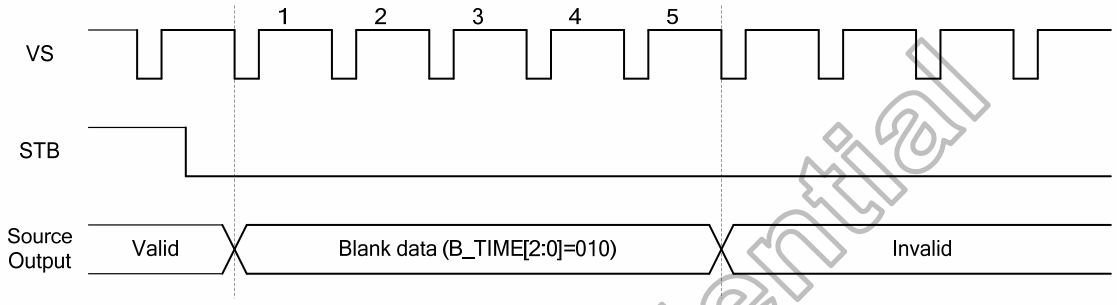


Figure 5. 9 Standby ON/OFF Control

5.11 Reset when power on

HX8250-A is internally initialized by the global reset signal, RESETB. The reset input must be held for at least 1ms after power is stable.

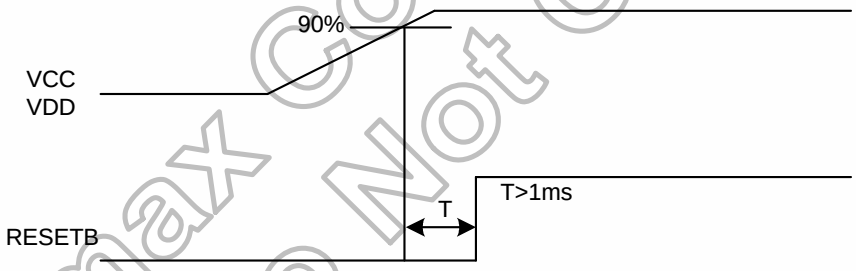


Figure 5. 10 RESETB control after power stable

6. DC Characteristics

6.1 Absolute Maximum Rating (GND=VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VCC	-0.3	-	+7.0	V
Power supply voltage 2	VDD	-0.3	-	+13.5	V
Logic Output Voltage	V_{OUT}	-0.3	-	+7.0	V
Input voltage	Vin	-0.3	-	VDD+0.3	V
Operation temperature	T_{OPR}	-40	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: (1)All of the voltages listed above are with respective to GND=VSS=0V.
(2)Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6.2 DC Electrical Characteristics (GND=VSS=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	2.7	3.3	3.6	V	-
Power supply voltage	VDD	6.5	8.4	13.5	V	-
Low level input voltage	V_{IL}	0	-	0.3VCC	V	-
High level input voltage	V_{IH}	0.7VCC	-	VCC	V	-
Output low voltage	V_{OL}	0	-	0.2VCC	V	I_{OL}=400μA
Output high voltage	V_{OH}	0.8VCC	-	VCC	V	I_{OH}=-400μA
Input leakage current	I_{IN}	-1	-	+1	μA	No pull up or pull down.
Output voltage deviation	V_{VD}	-	±20	-	mV	SO1~SO960, V_{IN}=0.1~13.4V,
DC offset	V_{OS}	-	-	±20	mV	SO1~SO960, V_{IN}=0.1~13.4V,
Output leakage current	I_O	-1	-	+1	μA	SO1~SO960 at high impedance
Pull high resistance	R_H	600	900	1200	kΩ	RESETB,STB, MASL, CS, SPCK, SPENA, SPDA, RESL1, IF0
Pull low resistance	R_L	600	900	1200	kΩ	DEN,IF[2:1],RESL0, FRP, Dx[7:0], VSET, OSD_EN, OSD_R,OSD_G, OSD_B, TEST1, TEST2
Output current	I_{OH}	40	60	-	μA	SO1~SO960, V_O =9.9V vs. 9V, VDD=10V
Output current	I_{OL}	40	60	-	μA	SO1~SO960, Vo=0.1V vs. 1.0V, VDD=10V
Analog operating current	I_{DD}	-	6	-	mA	F_{cph} =19.2MHz, serial RGB, f_{HS}=15.7KHz, black pattern, VDD=8.4V, RL=2K, CL=60pF
Digital operating current	I_{CC}	-	2.5	-	mA	F_{cph} =19.2MHz, serial RGB, f_{HS}=15.7KHz, black pattern, VCC=3.3V
Analog standby current	I_{VDD}	-	-	10	μA	All LCD outputs are High-Z.
Digital standby current	I_{VCC}	-	-	10	μA	All inputs are stopped and outputs are High-Z.

7. AC Characteristics

7.1 Input signal characteristics

7.1.1 AC Electrical Characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
HS setup time	T_{hst}	10	-	-	ns
HS hold time	T_{hhd}	10	-	-	ns
VS setup time	T_{vst}	10	-	-	ns
VS hold time	T_{vhd}	10	-	-	ns
Data setup time	T_{dsu}	10	-	-	ns
Data hold time	T_{dhd}	10	-	-	ns
DEN setup time	T_{esu}	10	-	-	ns
VS falling to HS falling time on odd field @ RGB mode	T_{HV_O}	-4	0	+4	T_{CPH}
VS falling to HS falling time on even field @ RGB mode	T_{HV_E}	0.4	0.5	0.6	T_H
Source output settling time	T_{ST}	-	12	20	µs
Source output loading R	R_{SL}	-	2	-	K ohm
Source output loading C	C_{SL}	-	60	-	pF
POL output delay time	T_{DP}	-	-	40	ns

7.1.2 Digital Serial RGB interface (960x240 resolution)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	19.28	-	MHz
CLK period		T_{CPH}	-	51.87	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	1224	-	T_{CPH}
HS pulse width		T_{WH}	5	90	-	T_{CPH}
HS-first horizontal data time		T_{HS}	172	204	235	T_{CPH}
DEN pulse width		T_{EP}	-	960	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 204th CLK after HS falling (when STHD[5:0]=000000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	72	-	T_{CPH}
HS-CKV time	T_1	-	48	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	81	-	T_{CPH}
STV setup time	T_{SUV}	-	42	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

7.1.3 Digital Serial RGB interface (1920x240 resolution)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	38.56	-	MHz
CLK period		T_{CPH}	-	25.94	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	2448	-	T_{CPH}
HS pulse width		T_{WH}	5	180	-	T_{CPH}
HS-first horizontal data time		T_{HS}	376	408	439	T_{CPH}
DEN pulse width		T_{EP}	-	1920	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 408th CLK after HS falling (when STHD[5:0]=00000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	208	-	T_{CPH}
CKV pulse width	T_{CKV}	-	144	-	T_{CPH}
HS-CKV time	T_1	-	96	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	162	-	T_{CPH}
STV setup time	T_{SUV}	-	90	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

7.1.4 Digital Parallel RGB interface (960x240 resolution)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	6.43	-	MHz
CLK period		T_{CPH}	-	155.62	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	408	-	T_{CPH}
HS pulse width		T_{WH}	5	30	-	T_{CPH}
HS-first horizontal data time		T_{HS}	36	68	99	T_{CPH}
DEN pulse width		T_{EP}	-	320	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 68th CLK after HS falling (when STHD[5:0]=00000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	26	-	T_{CPH}
CKV pulse width	T_{CKV}	-	24	-	T_{CPH}
HS-CKV time	T_1	-	16	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	25	-	T_{CPH}
STV setup time	T_{SUV}	-	10	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

7.1.5 Digital Parallel RGB interface (1920x240 resolution)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	12.85	-	MHz
CLK period		T_{CPH}	-	77.81	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	816	-	T_{CPH}
HS pulse width		T_{WH}	5	60	-	T_{CPH}
HS-first horizontal data time		T_{HS}	104	136	167	T_{CPH}
DEN pulse width		T_{EP}	-	640	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 136th CLK after HS falling (when STHD[5:0]=00000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	64	-	T_{CPH}
CKV pulse width	T_{CKV}	-	48	-	T_{CPH}
HS-CKV time	T_1	-	32	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	54	-	T_{CPH}
STV setup time	T_{SUV}	-	26	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

7.1.6 Digital Parallel RGB interface (1920x480 resolution)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	25.175	-	MHz
CLK period	T_{CPH}	-	39.7	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	800	-	T_{CPH}
HS pulse width	T_{WH}	5	30	-	T_{CPH}
HS-first horizontal data time	T_{HS}	112	144	175	T_{CPH}
DEN pulse width	T_{EP}	-	640	-	T_{CPH}
VS pulse width	T_{WV}	1	3	5	T_H
VS-DEN time	T_{STV}	-	35	-	T_H
VS period	T_V	-	525	-	T_H

Note: When SYNC mode is used, 1st data start from 144th CLK after HS falling (when STHD[5:0]=00000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

7.1.7 CCIR601 interface

(For 24.54MHz, NTSC mode)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	24.54	-	MHz
CLK period	T_{CPH}	-	40.7	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1560	-	T_{CPH}
Horizontal active data area	T_{HA}	-	1280	-	T_{CPH}
VS pulse width	T_{WV}		1.5		T_H
VS-1st Data input time	T_{STV}	-	17	-	T_H
VS period	T_V	-	262.5	-	T_H

(For 27MHz)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{cph}	-	27	-	MHz
CLK period		T_{cph}	-	37	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VS pulse width		T_{WV}		1.5		T_H
VS-1st Data input time	NTSC	T_{STV}	-	17	-	T_H
	PAL	T_{STV}	-	24	-	T_H
VS period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

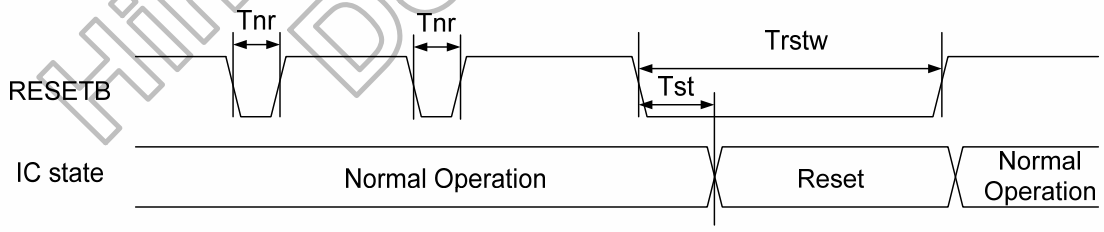
7.1.8 CCIR656 interface

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	27	-	MHz
CLK period		T_{CPH}	-	37	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VS-1st Data input time	NTSC	T_{STV}	-	22	-	T_H
	PAL	T_{STV}	-	28	-	T_H
VS period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse width	T_{STV}	-	1	-	T_H

7.1.9 Hardware reset timing

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
RESETB low pulse width	T_{rstw}	10	-	-	µs
Negative noise pulse width	T_{nr}		-	2	µs
Reset start time	T_{st}	2	-		µs



8. Waveform

8.1 Timing Controller Timing Chart

8.1.1 Clock and Data input waveforms

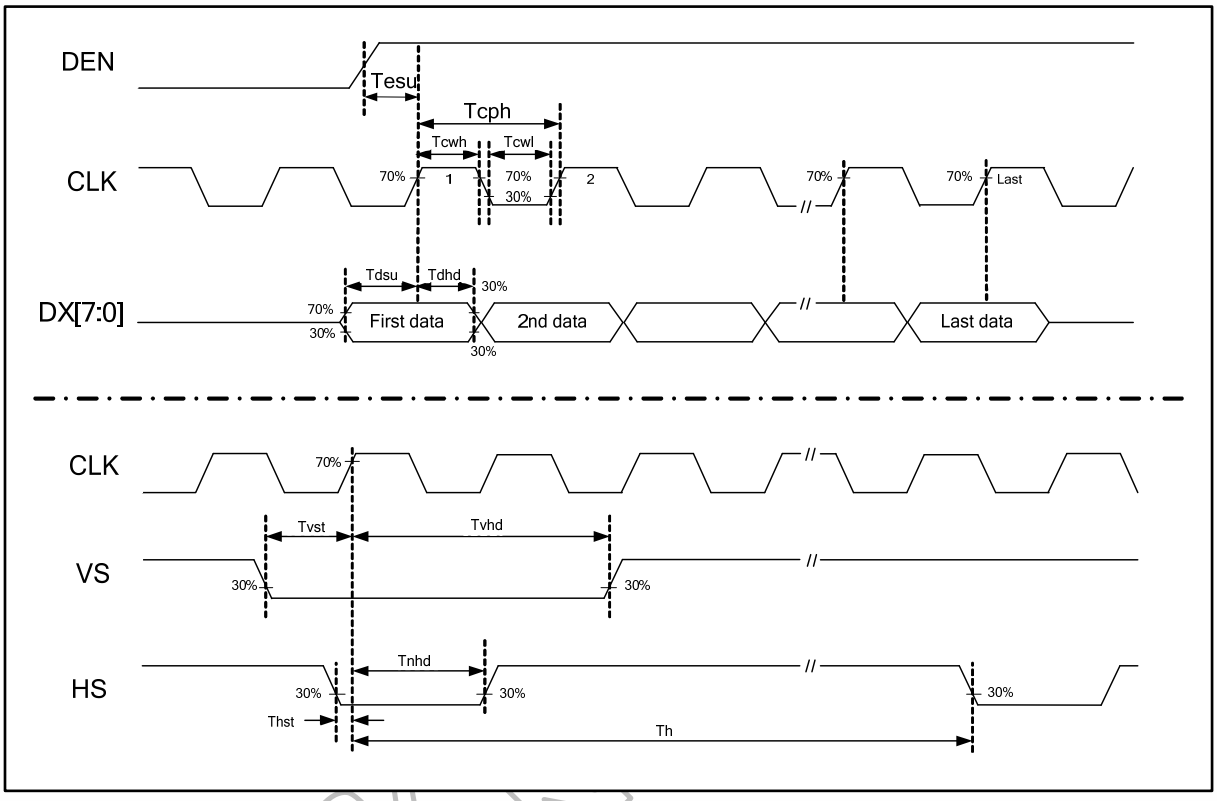


Figure 8. 1 Clock and Data input waveforms.

8.1.2 Data input format for RGB Mode

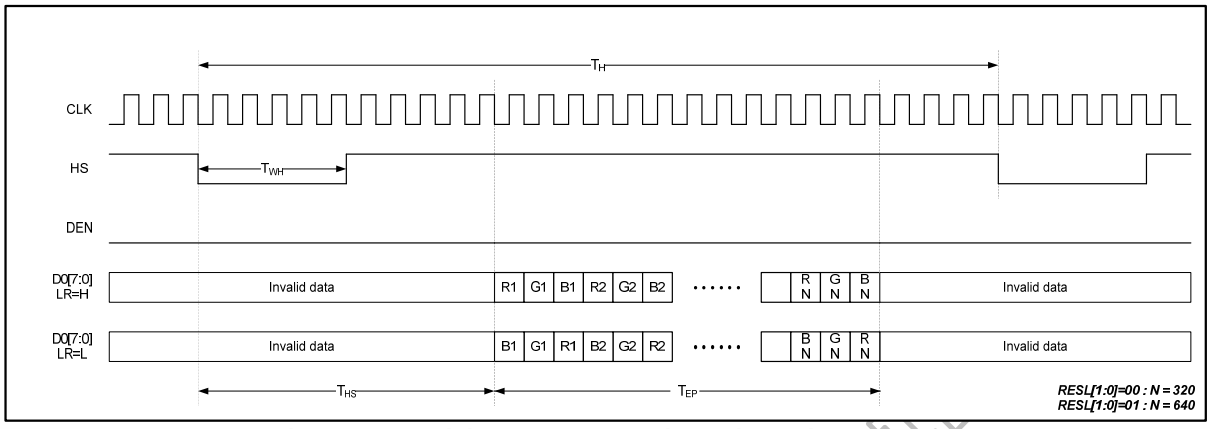


Figure 8. 2 Serial RGB SYNC Mode Horizontal Data Format

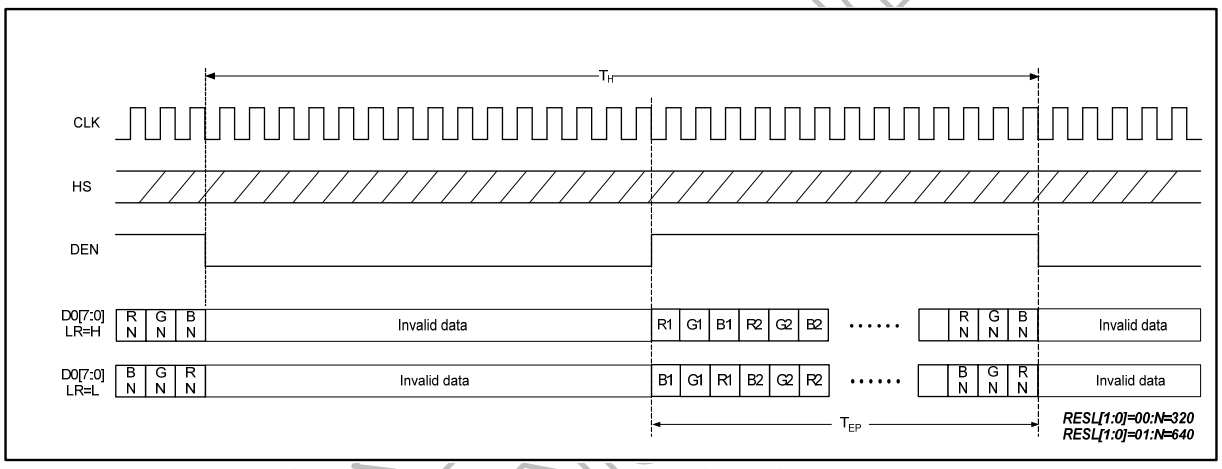


Figure 8. 3 Serial RGB DE Mode Horizontal Data Format

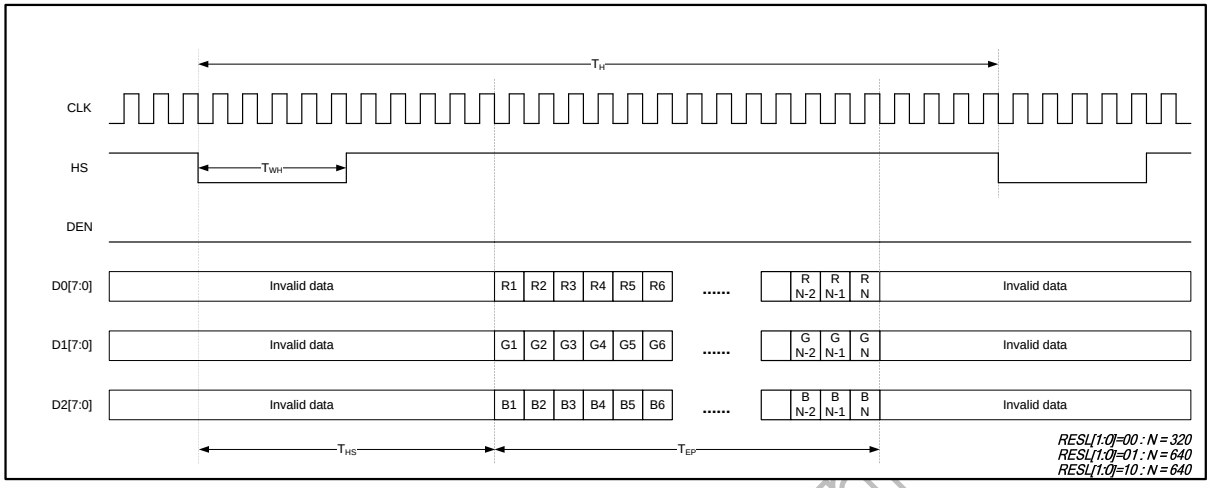


Figure 8. 4 Parallel RGB SYNC Mode Horizontal Data Format

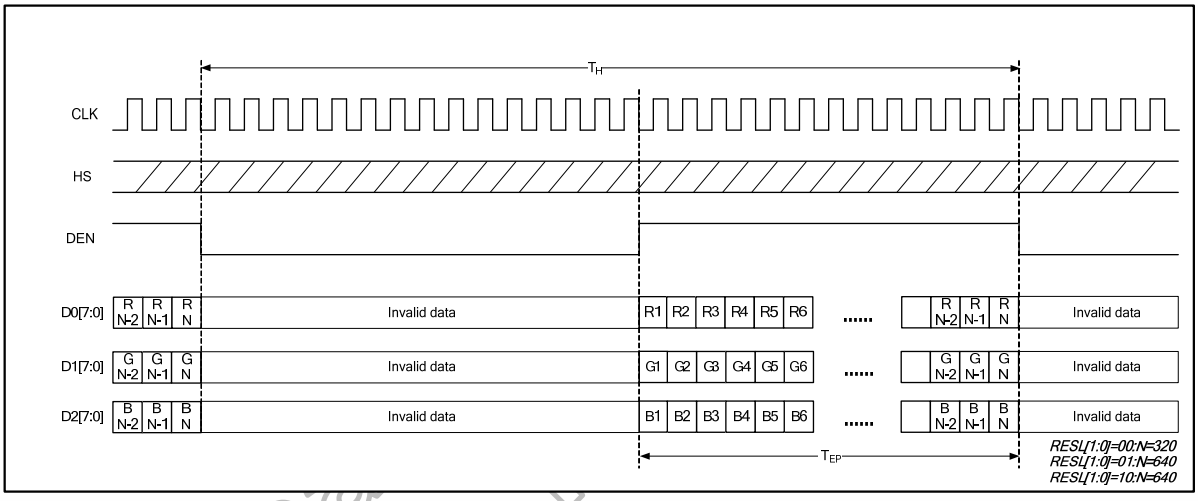


Figure 8. 5 Parallel RGB DE Mode Horizontal Data Format

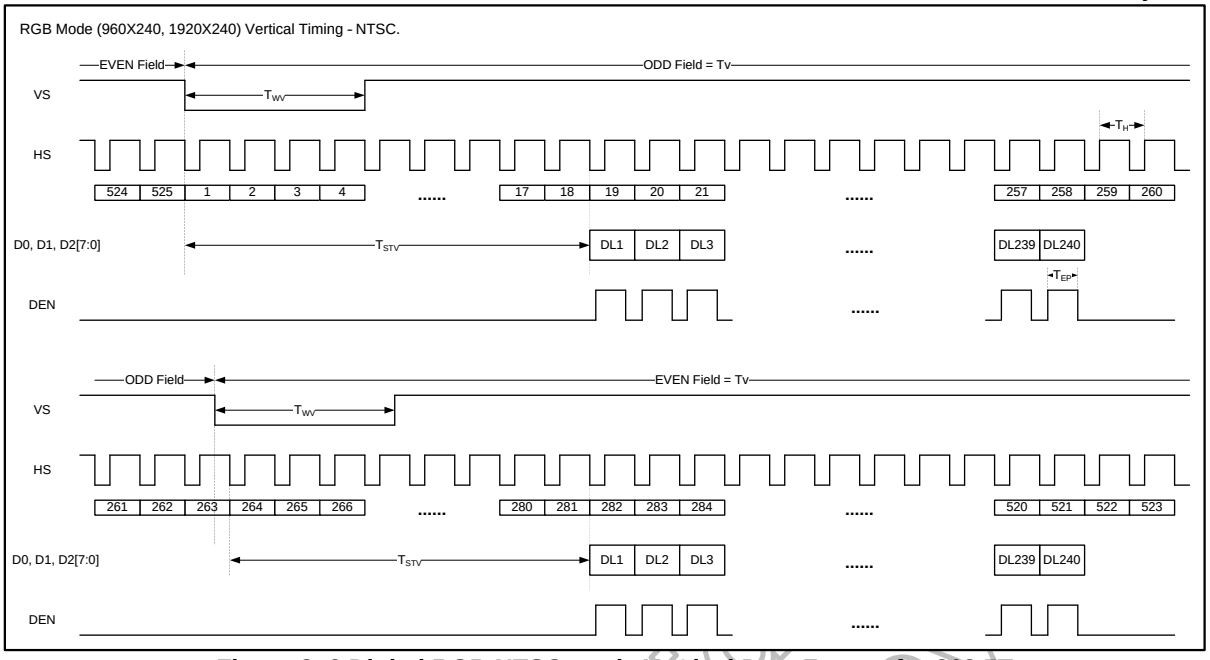


Figure 8. 6 Digital RGB NTSC mode Vertical Data Format for 262.5T_H

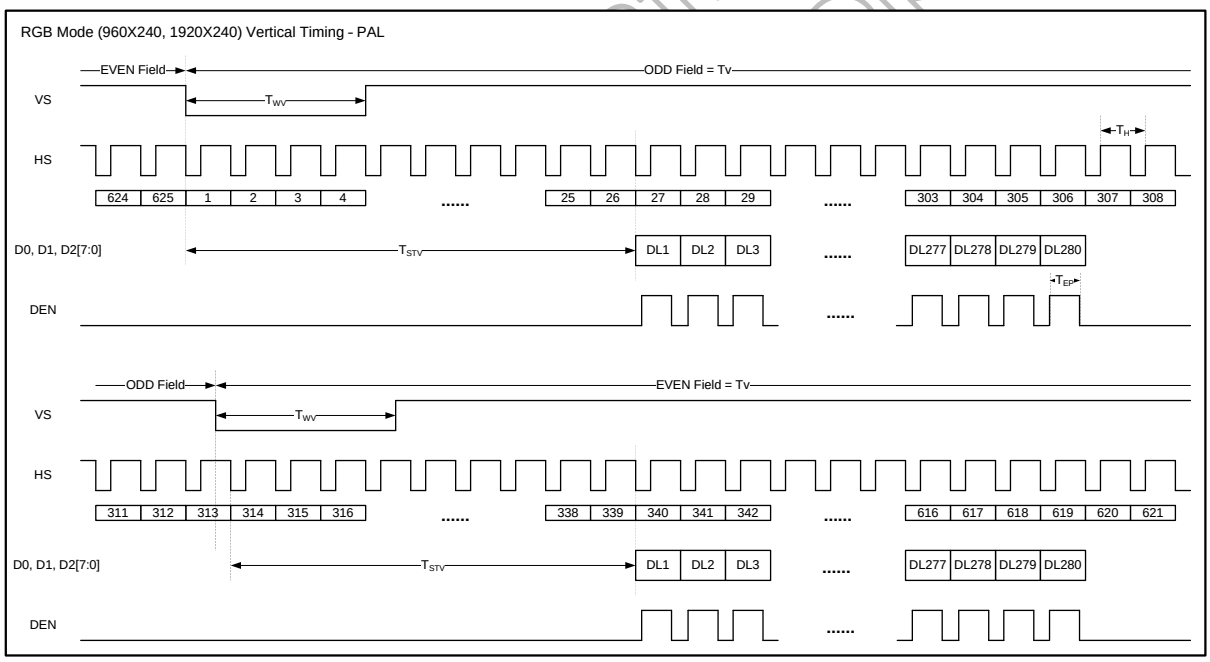


Figure 8. 7 Digital RGB PAL mode Vertical Data Format for 312.5T_H

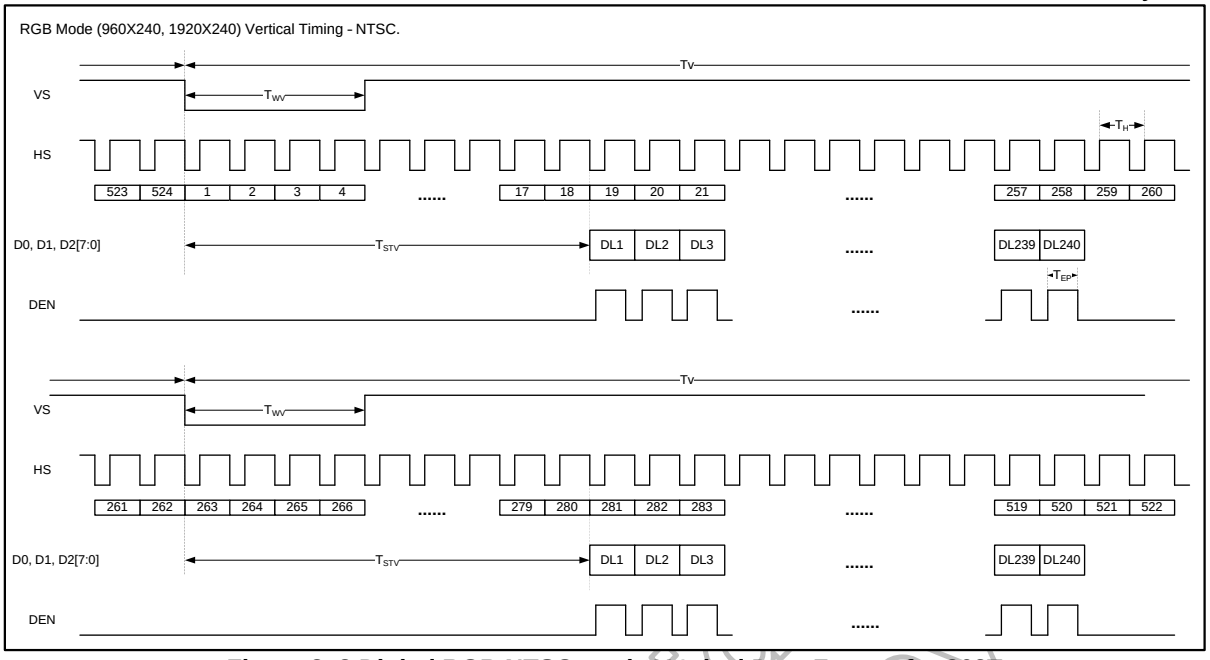


Figure 8. 8 Digital RGB NTSC mode Vertical Data Format for $262T_H$

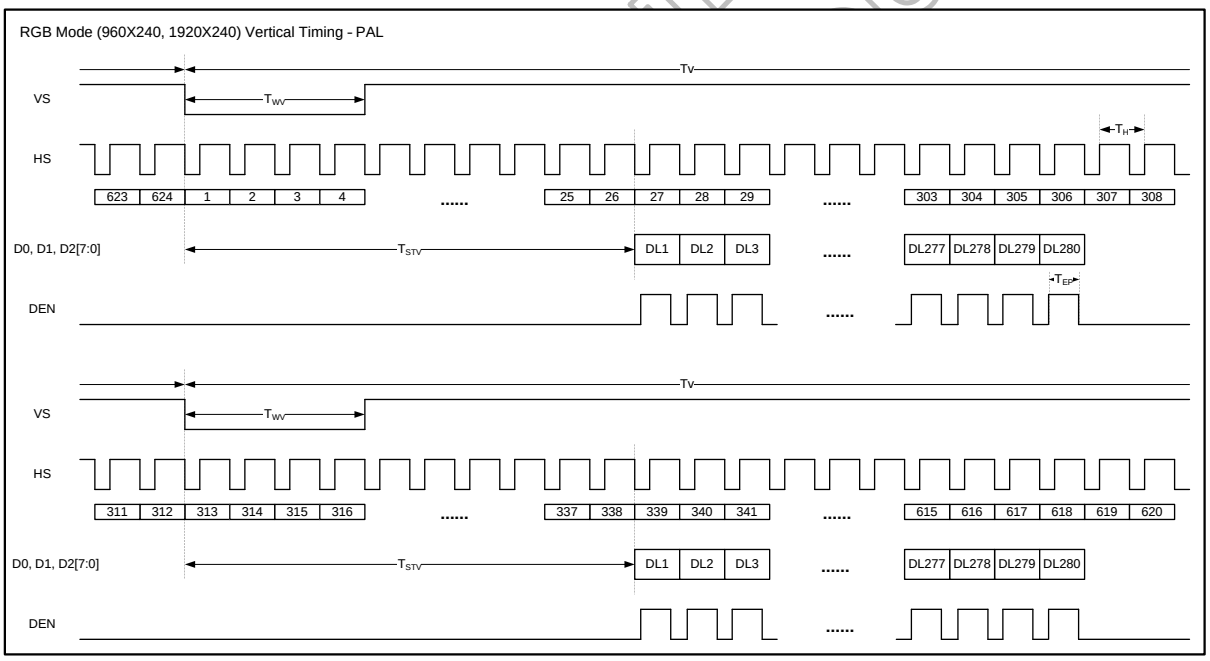


Figure 8. 9 Digital RGB PAL mode Vertical Data Format for $312T_H$

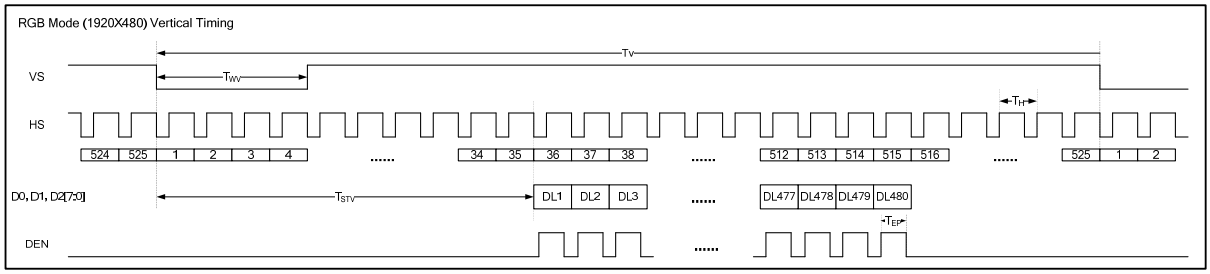


Figure 8. 10 Digital RGB mode Horizontal timing for RESL[1:0]=10

8.1.3 Data input format for CCIR601 Mode

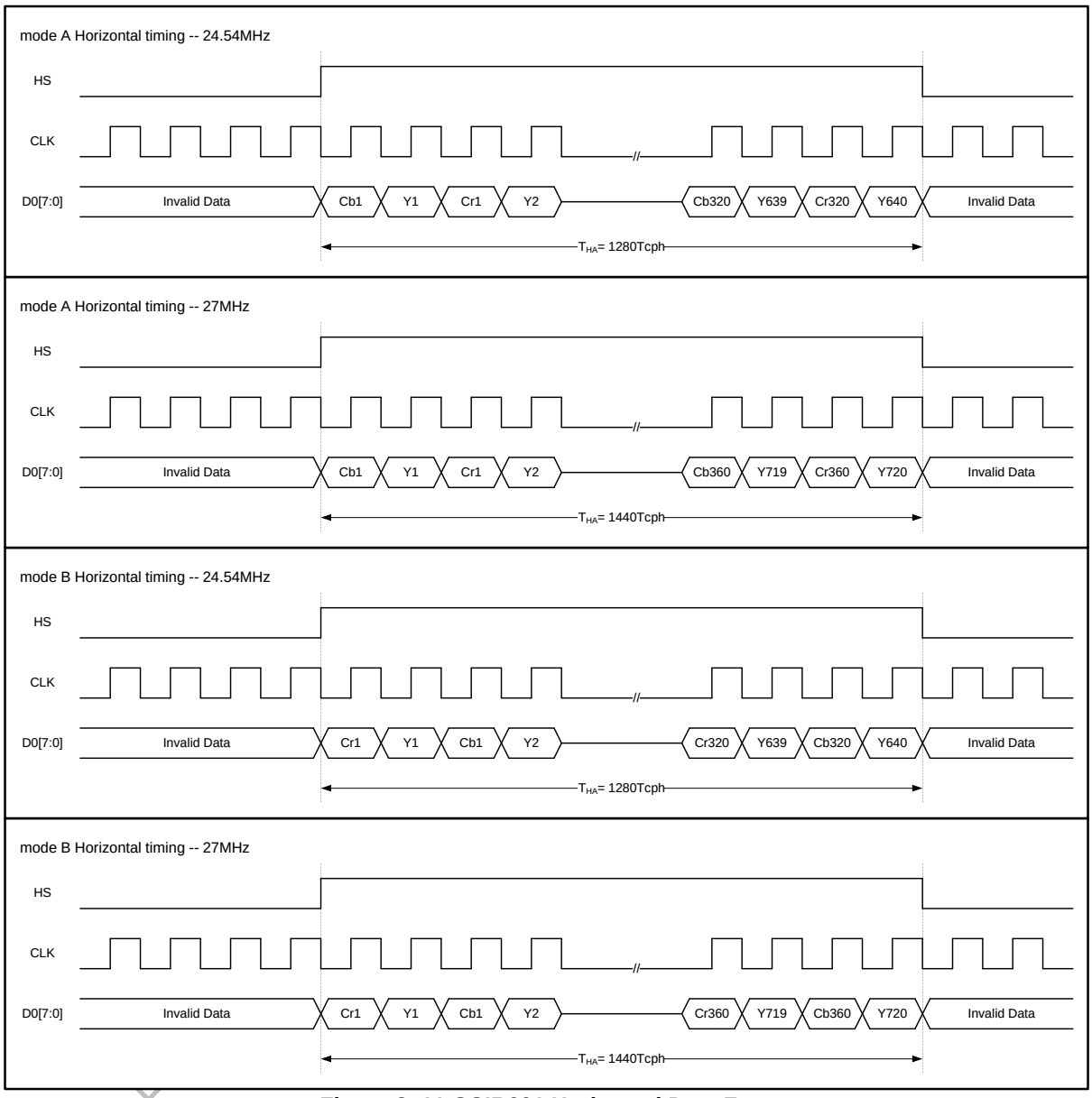


Figure 8. 11 CCIR601 Horizontal Data Format

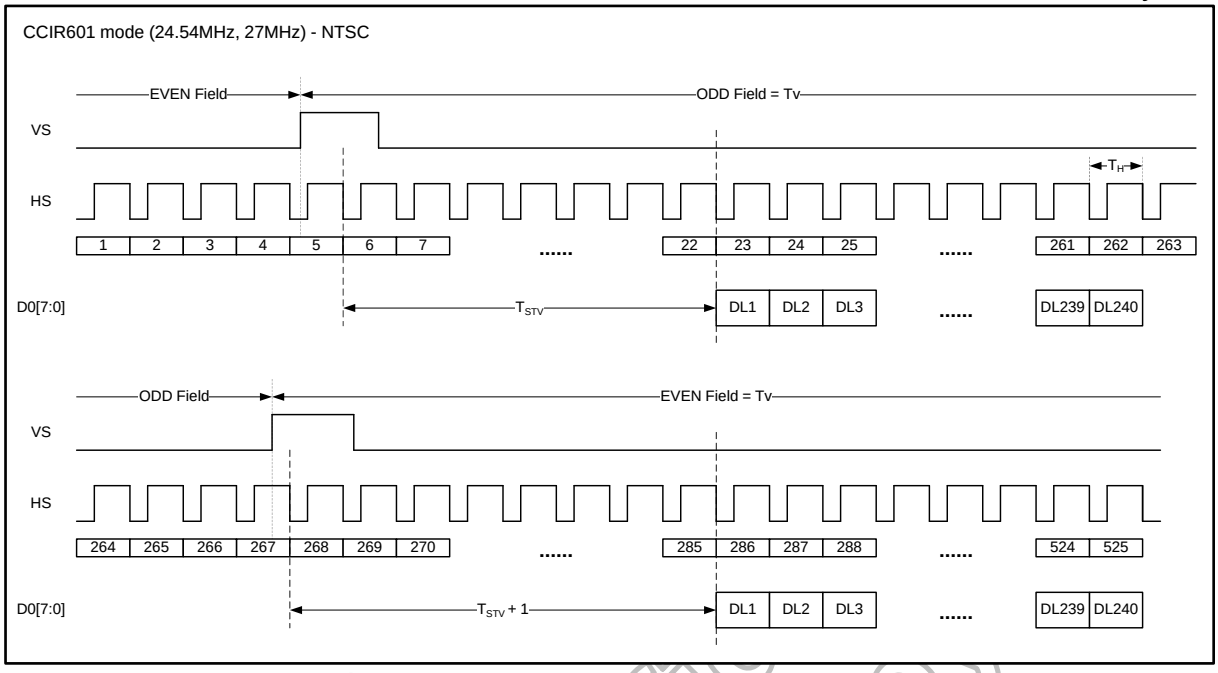


Figure 8. 12 CCIR601 Vertical Data Format-NTSC

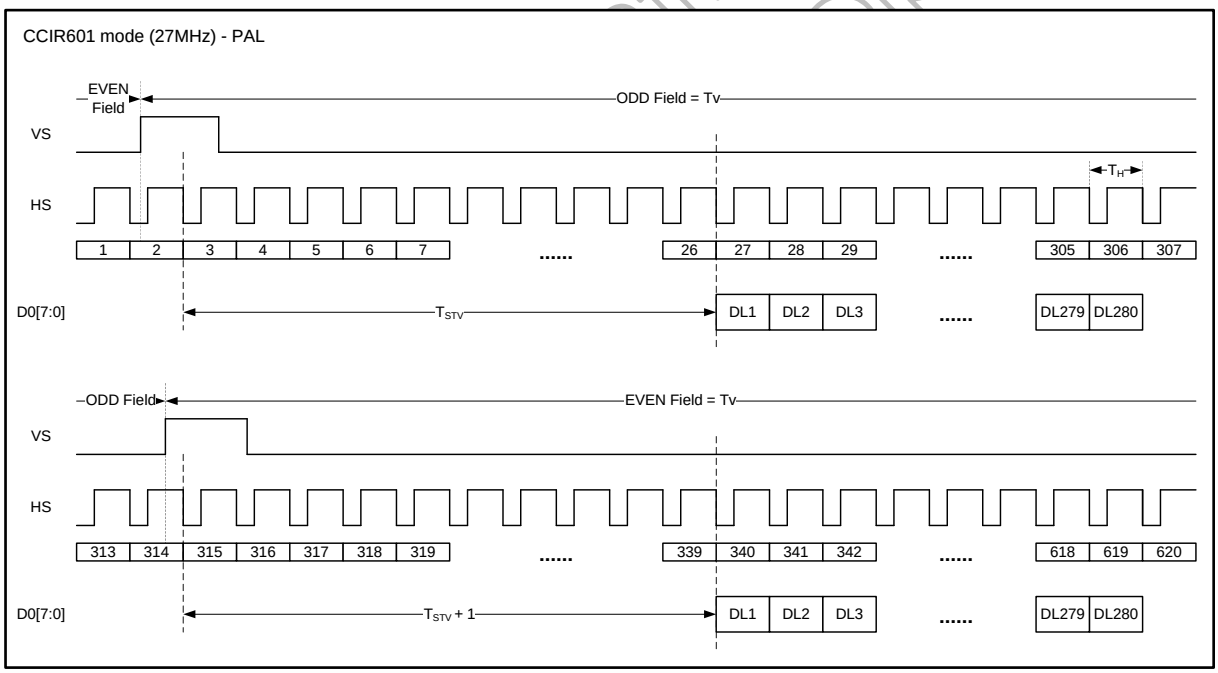


Figure 8. 13 CCIR601 Vertical Data Format - PAL

8.1.4 Data input format for CCIR656 Mode

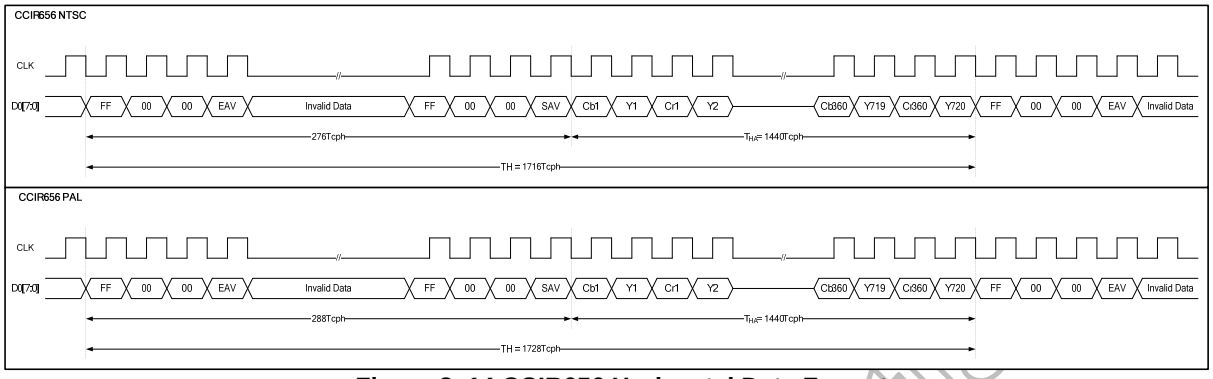


Figure 8. 14 CCIR656 Horizontal Data Format

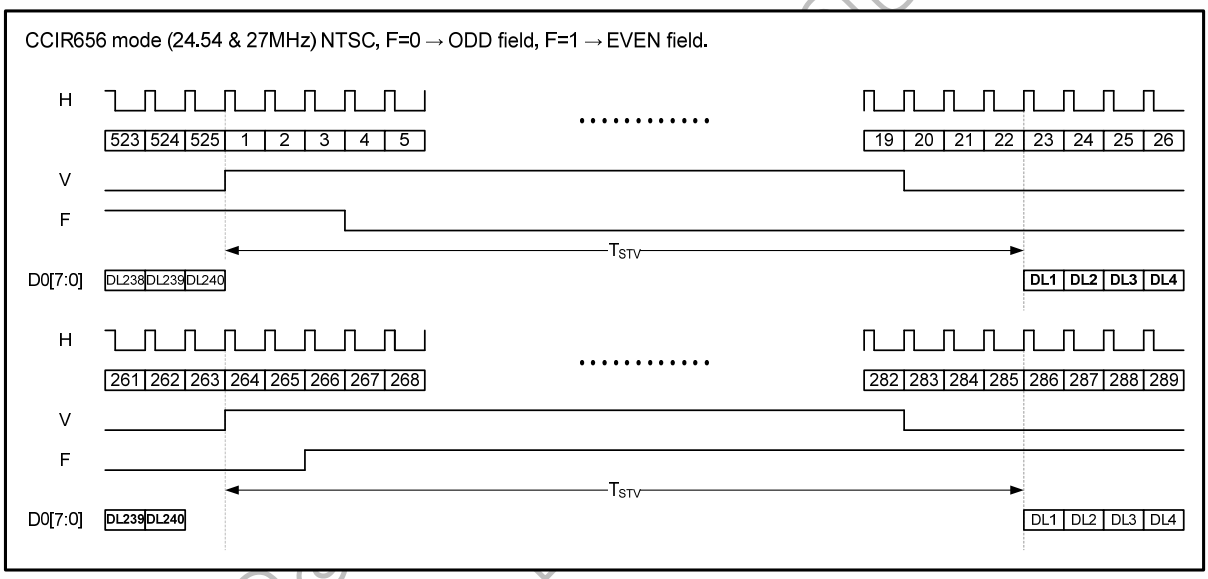


Figure 8. 15 CCIR656 NTSC Vertical Data Format - NTSC

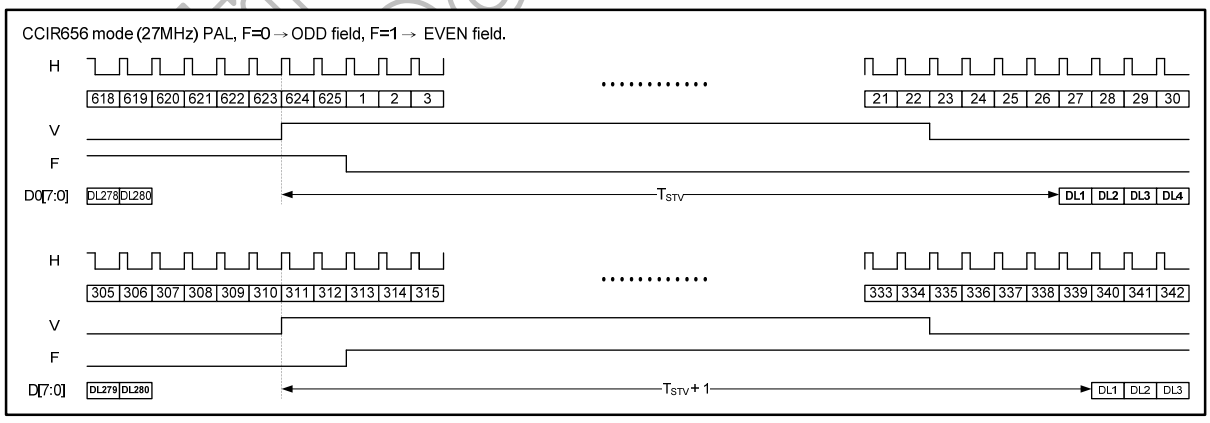


Figure 8. 16 CCIR656 NTSC Vertical Data Format - PAL

8.1.5 The HS & VS timing of the ODD/EVEN field.

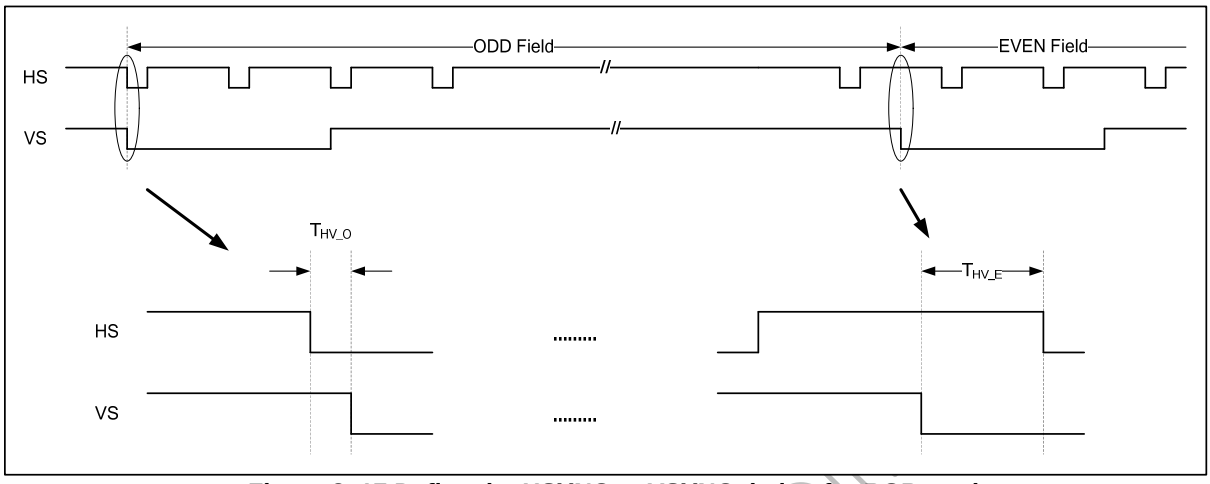


Figure 8. 17 Define the HSYNC to VSYNC timing for RGB mode

8.1.6 Digital Output timing waveforms

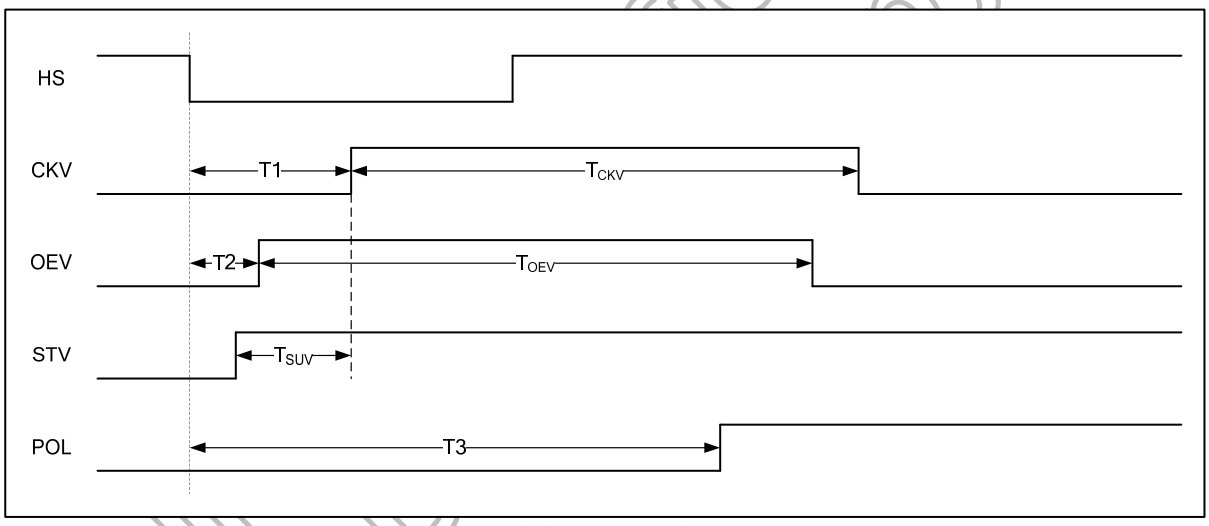


Figure 8. 18 Digital output timing waveforms

8.1.7 The PAL mode Skipped Line Location

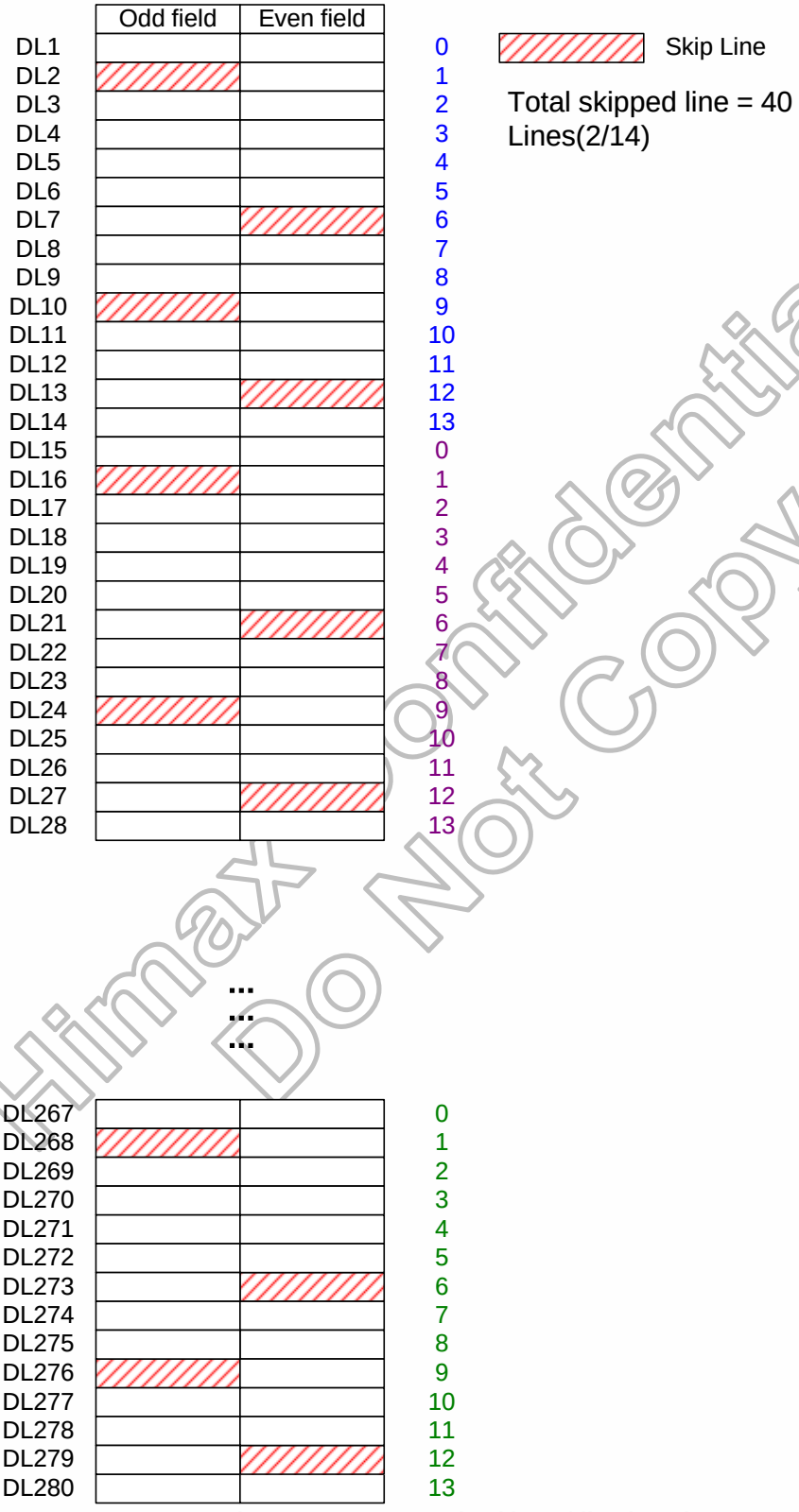


Figure 8. 19 PAL mode skipped line location

8.1.8 OSD output timing

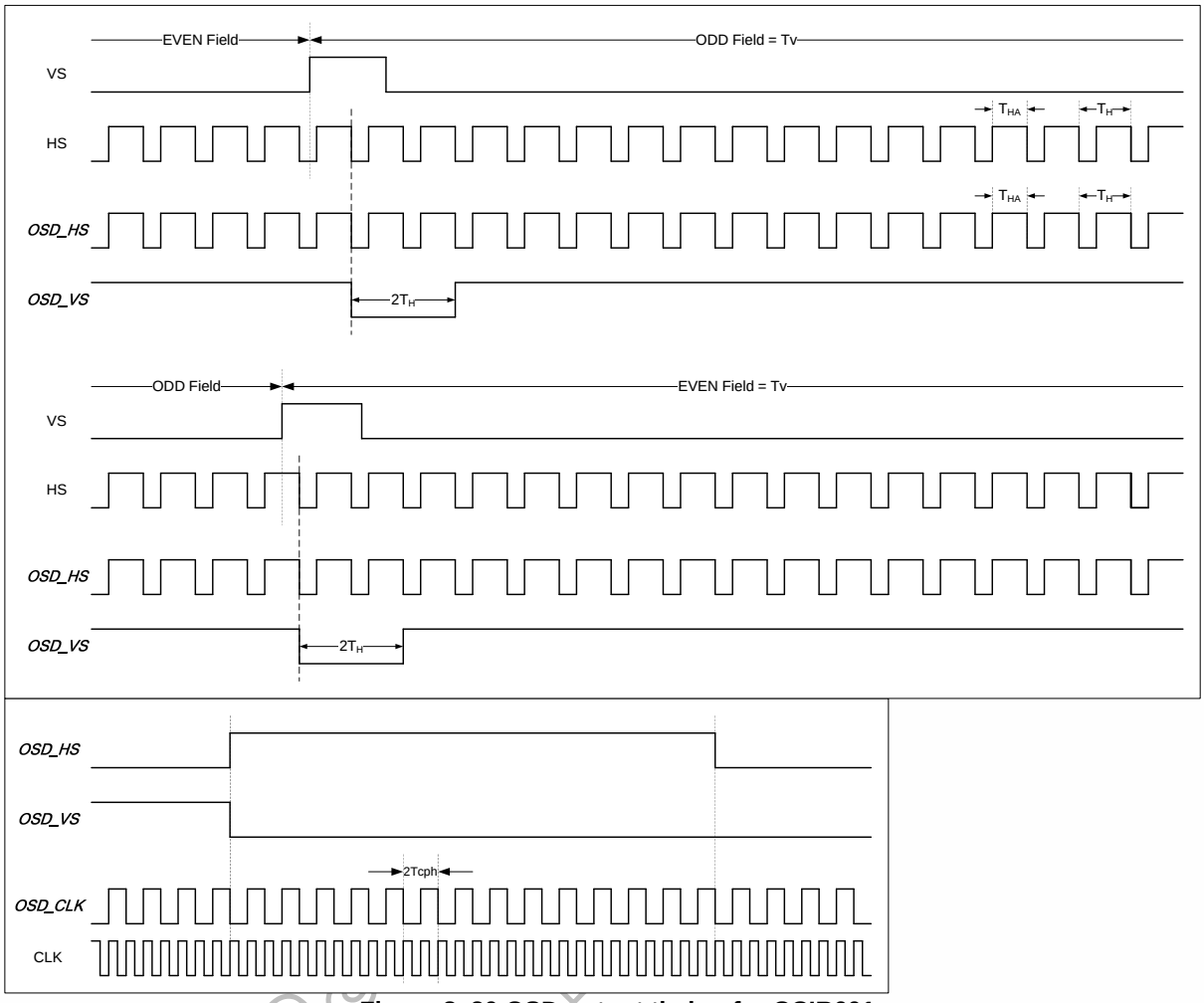


Figure 8. 20 OSD output timing for CCIR601

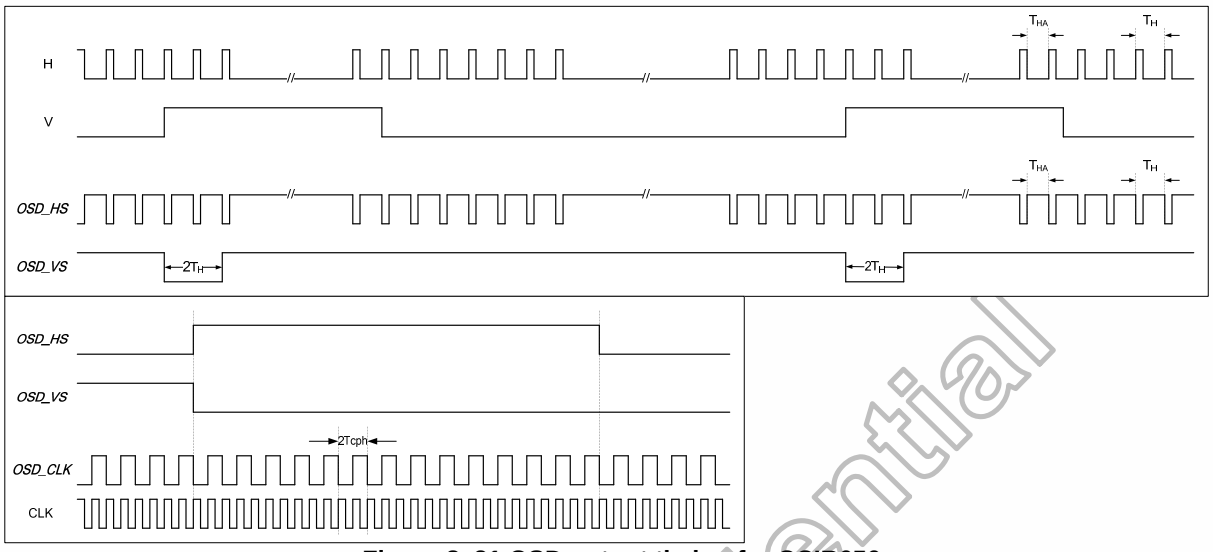


Figure 8. 21 OSD output timing for CCIR656

8.2 Output Timing Chart

8.2.1 Source Driver output timing waveforms

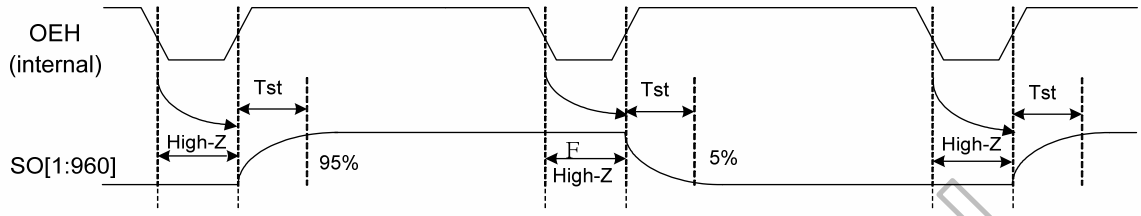
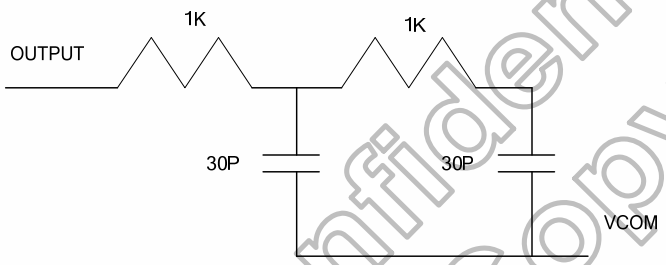


Figure 8. 22 OEH and Source Data Output timing waveforms

Source Output load condition:



9. SPI timing characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

I SPI timing

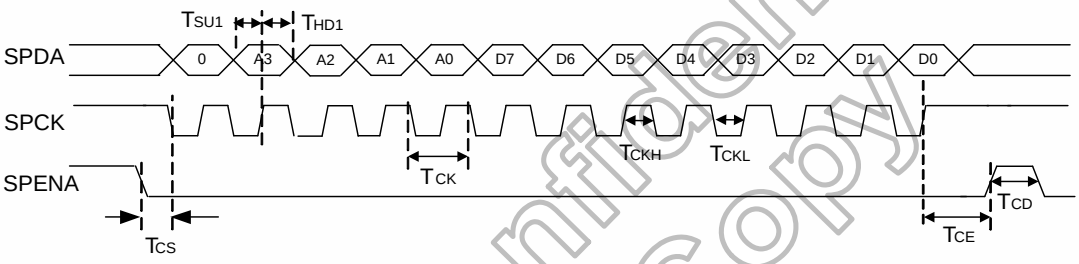
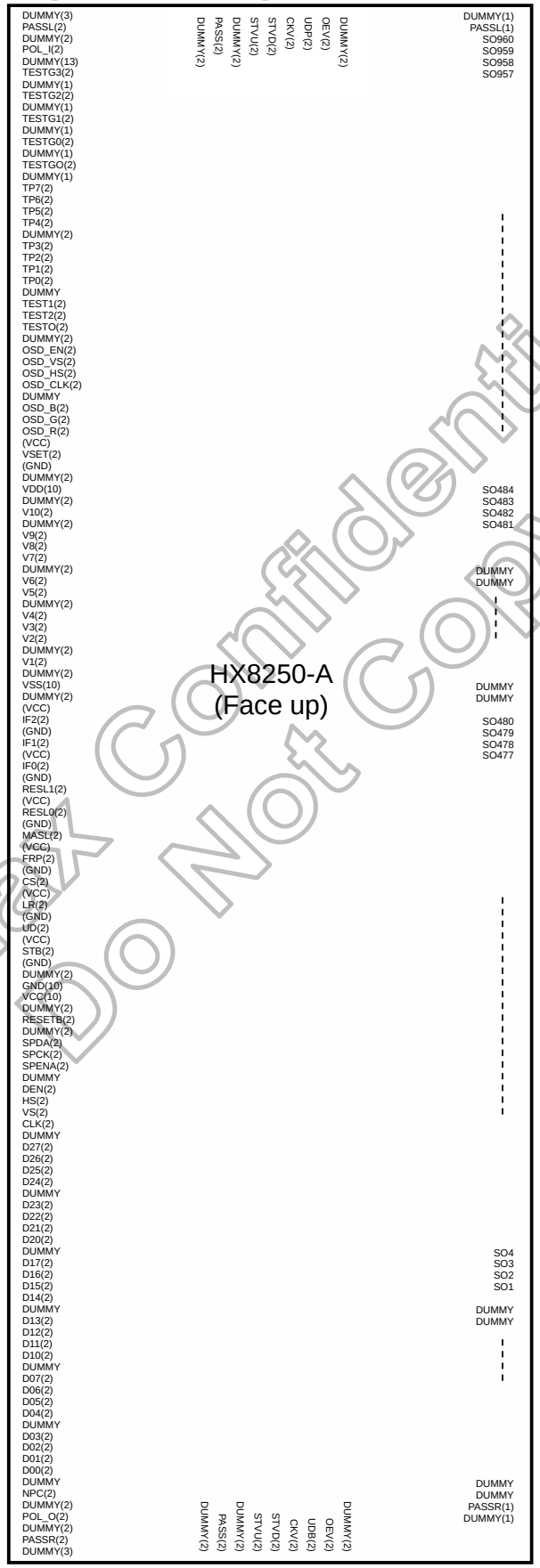
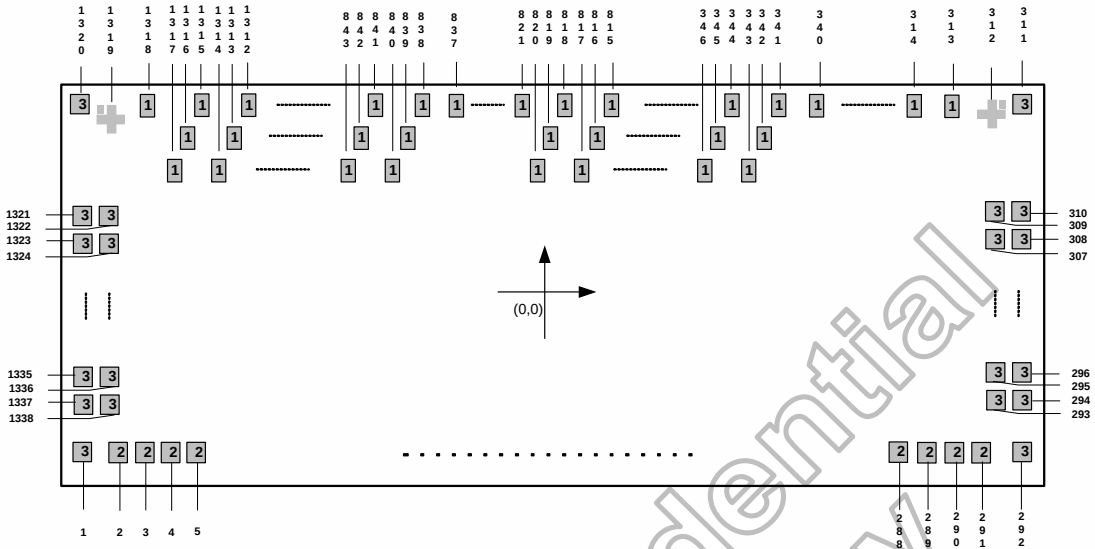


Figure 10. 1 SPI timing

10. Pin Assignment (IC face view)



11. Package Outline



11.1 Pad Diagram

NO.	NAME	X	Y
1	SIDE_DUMMY	-10612	-495
2	DUMMY	-10531	-475
3	DUMMY	-10461	-475
4	PASSL	-10391	-475
5	PASSL	-10321	-475
6	DUMMY	-10251	-475
7	DUMMY	-10181	-475
8	POL_I	-10111	-475
9	POL_I	-10041	-475
10	DUMMY	-9951	-475
11	DUMMY	-9881	-475
12	DUMMY	-9811	-475
13	DUMMY	-9741	-475
14	DUMMY	-9671	-475
15	DUMMY	-9601	-475
16	DUMMY	-9531	-475
17	DUMMY	-9461	-475
18	DUMMY	-9391	-475
19	DUMMY	-9321	-475
20	DUMMY	-9251	-475
21	DUMMY	-9181	-475
22	DUMMY	-9111	-475
23	TESTG3	-9041	-475
24	TESTG3	-8971	-475
25	DUMMY	-8901	-475
26	TESTG2	-8831	-475
27	TESTG2	-8761	-475
28	DUMMY	-8691	-475
29	TESTG1	-8621	-475
30	TESTG1	-8551	-475
31	DUMMY	-8481	-475
32	TESTG0	-8411	-475
33	TESTG0	-8341	-475
34	DUMMY	-8271	-475
35	TESTGO	-8201	-475
36	TESTGO	-8131	-475
37	DUMMY	-8061	-475
38	TP7	-7991	-475
39	TP7	-7921	-475
40	DUMMY	-7846	-475
41	TP6	-7776	-475
42	TP6	-7706	-475
43	DUMMY	-7631	-475
44	TP5	-7561	-475
45	TP5	-7491	-475
46	DUMMY	-7416	-475
47	TP4	-7346	-475
48	TP4	-7276	-475
49	DUMMY	-7201	-475
50	TP3	-7131	-475

NO.	NAME	X	Y
51	TP3	-7061	-475
52	DUMMY	-6986	-475
53	TP2	-6916	-475
54	TP2	-6846	-475
55	DUMMY	-6771	-475
56	TP1	-6701	-475
57	TP1	-6631	-475
58	DUMMY	-6556	-475
59	TESTO0	-6486	-475
60	TESTO0	-6416	-475
61	DUMMY	-6341	-475
62	TEST1	-6271	-475
63	TEST1	-6201	-475
64	TEST2	-6111	-475
65	TEST2	-6041	-475
66	DUMMY	-5971	-475
67	TESTO	-5901	-475
68	TESTO	-5831	-475
69	DUMMY	-5756	-475
70	DUMMY	-5686	-475
71	OSD_EN	-5596	-475
72	OSD_EN	-5526	-475
73	DUMMY	-5456	-475
74	OSD_VS	-5386	-475
75	OSD_VS	-5316	-475
76	DUMMY	-5241	-475
77	OSD_HS	-5171	-475
78	OSD_HS	-5101	-475
79	DUMMY	-5026	-475
80	OSD_CLK	-4956	-475
81	OSD_CLK	-4886	-475
82	DUMMY	-4811	-475
83	OSD_B	-4741	-475
84	OSD_B	-4671	-475
85	OSD_G	-4581	-475
86	OSD_G	-4511	-475
87	OSD_R	-4441	-475
88	OSD_R	-4371	-475
89	VCC	-4281	-475
90	VSET	-4211	-475
91	VSET	-4141	-475
92	GND	-4051	-475
93	DUMMY	-3981	-475
94	DUMMY	-3911	-475
95	VDD	-3841	-475
96	VDD	-3771	-475
97	VDD	-3701	-475
98	VDD	-3631	-475
99	VDD	-3561	-475
100	VDD	-3491	-475

NO.	NAME	X	Y	NO.	NAME	X	Y
101	VDD	-3421	-475	151	IF2	99	-475
102	VDD	-3351	-475	152	GND	169	-475
103	VDD	-3281	-475	153	IF1	239	-475
104	VDD	-3211	-475	154	IF1	309	-475
105	DUMMY	-3141	-475	155	VCC	399	-475
106	DUMMY	-3071	-475	156	IF0	489	-475
107	V10	-3001	-475	157	IF0	559	-475
108	V10	-2931	-475	158	GND	629	-475
109	DUMMY	-2861	-475	159	RESL1	699	-475
110	DUMMY	-2791	-475	160	RESL1	769	-475
111	V9	-2721	-475	161	VCC	859	-475
112	V9	-2651	-475	162	RESL0	949	-475
113	V8	-2581	-475	163	RESL0	1019	-475
114	V8	-2511	-475	164	GND	1089	-475
115	V7	-2441	-475	165	MASL	1159	-475
116	V7	-2371	-475	166	MASL	1229	-475
117	DUMMY	-2301	-475	167	VCC	1319	-475
118	DUMMY	-2231	-475	168	FRP	1409	-475
119	V6	-2161	-475	169	FRP	1479	-475
120	V6	-2091	-475	170	GND	1549	-475
121	V5	-2021	-475	171	CS	1619	-475
122	V5	-1951	-475	172	CS	1689	-475
123	DUMMY	-1881	-475	173	VCC	1779	-475
124	DUMMY	-1811	-475	174	LR	1869	-475
125	V4	-1741	-475	175	LR	1939	-475
126	V4	-1671	-475	176	GND	2009	-475
127	V3	-1601	-475	177	UD	2079	-475
128	V3	-1531	-475	178	UD	2149	-475
129	V2	-1461	-475	179	VCC	2239	-475
130	V2	-1391	-475	180	STB	2329	-475
131	DUMMY	-1321	-475	181	STB	2399	-475
132	DUMMY	-1251	-475	182	GND	2469	-475
133	V1	-1181	-475	183	DUMMY	2539	-475
134	V1	-1111	-475	184	DUMMY	2609	-475
135	DUMMY	-1041	-475	185	GND	2679	-475
136	DUMMY	-971	-475	186	GND	2749	-475
137	VSS	-901	-475	187	GND	2819	-475
138	VSS	-831	-475	188	GND	2889	-475
139	VSS	-761	-475	189	GND	2959	-475
140	VSS	-691	-475	190	GND	3029	-475
141	VSS	-621	-475	191	GND	3099	-475
142	VSS	-551	-475	192	GND	3169	-475
143	VSS	-481	-475	193	GND	3239	-475
144	VSS	-411	-475	194	GND	3309	-475
145	VSS	-341	-475	195	VCC	3379	-475
146	VSS	-271	-475	196	VCC	3449	-475
147	DUMMY	-201	-475	197	VCC	3519	-475
148	DUMMY	-131	-475	198	VCC	3589	-475
149	VCC	-61	-475	199	VCC	3659	-475
150	IF2	29	-475	200	VCC	3729	-475

NO.	NAME	X	Y	NO.	NAME	X	Y
201	VCC	3799	-475	251	D14	7544	-475
202	VCC	3869	-475	252	D14	7614	-475
203	VCC	3939	-475	253	D13	7684	-475
204	VCC	4009	-475	254	D13	7754	-475
205	DUMMY	4079	-475	255	D12	7844	-475
206	DUMMY	4149	-475	256	D12	7914	-475
207	RESETB	4219	-475	257	D11	7984	-475
208	RESETB	4289	-475	258	D11	8054	-475
209	DUMMY	4389	-475	259	D10	8144	-475
210	SPDA	4459	-475	260	D10	8214	-475
211	SPDA	4529	-475	261	DUMMY	8284	-475
212	DUMMY	4634	-475	262	D07	8354	-475
213	DUMMY	4704	-475	263	D07	8424	-475
214	SPCK	4774	-475	264	D06	8514	-475
215	SPCK	4844	-475	265	D06	8584	-475
216	SPENA	4934	-475	266	D05	8654	-475
217	SPENA	5004	-475	267	D05	8724	-475
218	DUMMY	5074	-475	268	D04	8814	-475
219	DEN	5144	-475	269	D04	8884	-475
220	DEN	5214	-475	270	D03	8954	-475
221	HS	5304	-475	271	D03	9024	-475
222	HS	5374	-475	272	D02	9114	-475
223	VS	5444	-475	273	D02	9184	-475
224	VS	5514	-475	274	D01	9254	-475
225	CLK	5604	-475	275	D01	9324	-475
226	CLK	5674	-475	276	D00	9414	-475
227	DUMMY	5744	-475	277	D00	9484	-475
228	D27	5814	-475	278	DUMMY	9554	-475
229	D27	5884	-475	279	NPC	9624	-475
230	D26	5974	-475	280	NPC	9694	-475
231	D26	6044	-475	281	DUMMY	9768	-475
232	D25	6114	-475	282	DUMMY	9838	-475
233	D25	6184	-475	283	DUMMY	9908	-475
234	D24	6274	-475	284	POL_O	9978	-475
235	D24	6344	-475	285	POL_O	10048	-475
236	D23	6414	-475	286	DUMMY	10122	-475
237	D23	6484	-475	287	DUMMY	10192	-475
238	D22	6574	-475	288	PASSR	10275	-475
239	D22	6644	-475	289	PASSR	10345	-475
240	D21	6714	-475	290	DUMMY	10415	-475
241	D21	6784	-475	291	DUMMY	10485	-475
242	D20	6874	-475	292	SIDE_DUMMY	10612	-495
243	D20	6944	-475	293	DUMMY	10542	-312
244	DUMMY	7014	-475	294	DUMMY	10612	-312
245	D17	7084	-475	295	PASS	10542	-234
246	D17	7154	-475	296	PASS	10612	-234
247	D16	7244	-475	297	DUMMY	10542	-156
248	D16	7314	-475	298	DUMMY	10612	-156
249	D15	7384	-475	299	STVU	10542	-78
250	D15	7454	-475	300	STVU	10612	-78

NO.	NAME	X	Y
301	STVD	10542	0
302	STVD	10612	0
303	CKV	10542	78
304	CKV	10612	78
305	UDB	10542	156
306	UDB	10612	156
307	OEV	10542	234
308	OEV	10612	234
309	DUMMY	10542	312
310	DUMMY	10612	312
311	SIDE_DUMMY	10612	495
312	MARK_R	10504.5	457.5
313	PASSR	10389.5	470
314	DUMMY	10332.5	470
315	DUMMY	10275.5	470
316	DUMMY	10218.5	470
317	DUMMY	10161.5	470
318	DUMMY	10104.5	470
319	DUMMY	10047.5	470
320	DUMMY	9990.5	470
321	DUMMY	9933.5	470
322	DUMMY	9876.5	470
323	DUMMY	9819.5	470
324	DUMMY	9762.5	470
325	DUMMY	9705.5	470
326	DUMMY	9648.5	470
327	DUMMY	9591.5	470
328	DUMMY	9534.5	470
329	DUMMY	9477.5	470
330	DUMMY	9420.5	470
331	DUMMY	9363.5	470
332	DUMMY	9306.5	470
333	DUMMY	9249.5	470
334	DUMMY	9192.5	470
335	DUMMY	9135.5	470
336	DUMMY	9078.5	470
337	DUMMY	9021.5	470
338	DUMMY	8964.5	470
339	DUMMY	8907.5	470
340	DUMMY	8850.5	470
341	OUT1	8793.5	470
342	OUT2	8774.5	340
343	OUT3	8755.5	210
344	OUT4	8736.5	470
345	OUT5	8717.5	340
346	OUT6	8698.5	210
347	OUT7	8679.5	470
348	OUT8	8660.5	340
349	OUT9	8641.5	210
350	OUT10	8622.5	470

NO.	NAME	X	Y
351	OUT11	8603.5	340
352	OUT12	8584.5	210
353	OUT13	8565.5	470
354	OUT14	8546.5	340
355	OUT15	8527.5	210
356	OUT16	8508.5	470
357	OUT17	8489.5	340
358	OUT18	8470.5	210
359	OUT19	8451.5	470
360	OUT20	8432.5	340
361	OUT21	8413.5	210
362	OUT22	8394.5	470
363	OUT23	8375.5	340
364	OUT24	8356.5	210
365	OUT25	8337.5	470
366	OUT26	8318.5	340
367	OUT27	8299.5	210
368	OUT28	8280.5	470
369	OUT29	8261.5	340
370	OUT30	8242.5	210
371	OUT31	8223.5	470
372	OUT32	8204.5	340
373	OUT33	8185.5	210
374	OUT34	8166.5	470
375	OUT35	8147.5	340
376	OUT36	8128.5	210
377	OUT37	8109.5	470
378	OUT38	8090.5	340
379	OUT39	8071.5	210
380	OUT40	8052.5	470
381	OUT41	8033.5	340
382	OUT42	8014.5	210
383	OUT43	7995.5	470
384	OUT44	7976.5	340
385	OUT45	7957.5	210
386	OUT46	7938.5	470
387	OUT47	7919.5	340
388	OUT48	7900.5	210
389	OUT49	7881.5	470
390	OUT50	7862.5	340
391	OUT51	7843.5	210
392	OUT52	7824.5	470
393	OUT53	7805.5	340
394	OUT54	7786.5	210
395	OUT55	7767.5	470
396	OUT56	7748.5	340
397	OUT57	7729.5	210
398	OUT58	7710.5	470
399	OUT59	7691.5	340
400	OUT60	7672.5	210

NO.	NAME	X	Y	NO.	NAME	X	Y
401	OUT61	7653.5	470	451	OUT111	6703.5	210
402	OUT62	7634.5	340	452	OUT112	6684.5	470
403	OUT63	7615.5	210	453	OUT113	6665.5	340
404	OUT64	7596.5	470	454	OUT114	6646.5	210
405	OUT65	7577.5	340	455	OUT115	6627.5	470
406	OUT66	7558.5	210	456	OUT116	6608.5	340
407	OUT67	7539.5	470	457	OUT117	6589.5	210
408	OUT68	7520.5	340	458	OUT118	6570.5	470
409	OUT69	7501.5	210	459	OUT119	6551.5	340
410	OUT70	7482.5	470	460	OUT120	6532.5	210
411	OUT71	7463.5	340	461	OUT121	6513.5	470
412	OUT72	7444.5	210	462	OUT122	6494.5	340
413	OUT73	7425.5	470	463	OUT123	6475.5	210
414	OUT74	7406.5	340	464	OUT124	6456.5	470
415	OUT75	7387.5	210	465	OUT125	6437.5	340
416	OUT76	7368.5	470	466	OUT126	6418.5	210
417	OUT77	7349.5	340	467	OUT127	6399.5	470
418	OUT78	7330.5	210	468	OUT128	6380.5	340
419	OUT79	7311.5	470	469	OUT129	6361.5	210
420	OUT80	7292.5	340	470	OUT130	6342.5	470
421	OUT81	7273.5	210	471	OUT131	6323.5	340
422	OUT82	7254.5	470	472	OUT132	6304.5	210
423	OUT83	7235.5	340	473	OUT133	6285.5	470
424	OUT84	7216.5	210	474	OUT134	6266.5	340
425	OUT85	7197.5	470	475	OUT135	6247.5	210
426	OUT86	7178.5	340	476	OUT136	6228.5	470
427	OUT87	7159.5	210	477	OUT137	6209.5	340
428	OUT88	7140.5	470	478	OUT138	6190.5	210
429	OUT89	7121.5	340	479	OUT139	6171.5	470
430	OUT90	7102.5	210	480	OUT140	6152.5	340
431	OUT91	7083.5	470	481	OUT141	6133.5	210
432	OUT92	7064.5	340	482	OUT142	6114.5	470
433	OUT93	7045.5	210	483	OUT143	6095.5	340
434	OUT94	7026.5	470	484	OUT144	6076.5	210
435	OUT95	7007.5	340	485	OUT145	6057.5	470
436	OUT96	6988.5	210	486	OUT146	6038.5	340
437	OUT97	6969.5	470	487	OUT147	6019.5	210
438	OUT98	6950.5	340	488	OUT148	6000.5	470
439	OUT99	6931.5	210	489	OUT149	5981.5	340
440	OUT100	6912.5	470	490	OUT150	5962.5	210
441	OUT101	6893.5	340	491	OUT151	5943.5	470
442	OUT102	6874.5	210	492	OUT152	5924.5	340
443	OUT103	6855.5	470	493	OUT153	5905.5	210
444	OUT104	6836.5	340	494	OUT154	5886.5	470
445	OUT105	6817.5	210	495	OUT155	5867.5	340
446	OUT106	6798.5	470	496	OUT156	5848.5	210
447	OUT107	6779.5	340	497	OUT157	5829.5	470
448	OUT108	6760.5	210	498	OUT158	5810.5	340
449	OUT109	6741.5	470	499	OUT159	5791.5	210
450	OUT110	6722.5	340	500	OUT160	5772.5	470

NO.	NAME	X	Y	NO.	NAME	X	Y
501	OUT161	5753.5	340	551	OUT211	4803.5	470
502	OUT162	5734.5	210	552	OUT212	4784.5	340
503	OUT163	5715.5	470	553	OUT213	4765.5	210
504	OUT164	5696.5	340	554	OUT214	4746.5	470
505	OUT165	5677.5	210	555	OUT215	4727.5	340
506	OUT166	5658.5	470	556	OUT216	4708.5	210
507	OUT167	5639.5	340	557	OUT217	4689.5	470
508	OUT168	5620.5	210	558	OUT218	4670.5	340
509	OUT169	5601.5	470	559	OUT219	4651.5	210
510	OUT170	5582.5	340	560	OUT220	4632.5	470
511	OUT171	5563.5	210	561	OUT221	4613.5	340
512	OUT172	5544.5	470	562	OUT222	4594.5	210
513	OUT173	5525.5	340	563	OUT223	4575.5	470
514	OUT174	5506.5	210	564	OUT224	4556.5	340
515	OUT175	5487.5	470	565	OUT225	4537.5	210
516	OUT176	5468.5	340	566	OUT226	4518.5	470
517	OUT177	5449.5	210	567	OUT227	4499.5	340
518	OUT178	5430.5	470	568	OUT228	4480.5	210
519	OUT179	5411.5	340	569	OUT229	4461.5	470
520	OUT180	5392.5	210	570	OUT230	4442.5	340
521	OUT181	5373.5	470	571	OUT231	4423.5	210
522	OUT182	5354.5	340	572	OUT232	4404.5	470
523	OUT183	5335.5	210	573	OUT233	4385.5	340
524	OUT184	5316.5	470	574	OUT234	4366.5	210
525	OUT185	5297.5	340	575	OUT235	4347.5	470
526	OUT186	5278.5	210	576	OUT236	4328.5	340
527	OUT187	5259.5	470	577	OUT237	4309.5	210
528	OUT188	5240.5	340	578	OUT238	4290.5	470
529	OUT189	5221.5	210	579	OUT239	4271.5	340
530	OUT190	5202.5	470	580	OUT240	4252.5	210
531	OUT191	5183.5	340	581	OUT241	4233.5	470
532	OUT192	5164.5	210	582	OUT242	4214.5	340
533	OUT193	5145.5	470	583	OUT243	4195.5	210
534	OUT194	5126.5	340	584	OUT244	4176.5	470
535	OUT195	5107.5	210	585	OUT245	4157.5	340
536	OUT196	5088.5	470	586	OUT246	4138.5	210
537	OUT197	5069.5	340	587	OUT247	4119.5	470
538	OUT198	5050.5	210	588	OUT248	4100.5	340
539	OUT199	5031.5	470	589	OUT249	4081.5	210
540	OUT200	5012.5	340	590	OUT250	4062.5	470
541	OUT201	4993.5	210	591	OUT251	4043.5	340
542	OUT202	4974.5	470	592	OUT252	4024.5	210
543	OUT203	4955.5	340	593	OUT253	4005.5	470
544	OUT204	4936.5	210	594	OUT254	3986.5	340
545	OUT205	4917.5	470	595	OUT255	3967.5	210
546	OUT206	4898.5	340	596	OUT256	3948.5	470
547	OUT207	4879.5	210	597	OUT257	3929.5	340
548	OUT208	4860.5	470	598	OUT258	3910.5	210
549	OUT209	4841.5	340	599	OUT259	3891.5	470
550	OUT210	4822.5	210	600	OUT260	3872.5	340

NO.	NAME	X	Y	NO.	NAME	X	Y
601	OUT261	3853.5	210	651	OUT311	2903.5	340
602	OUT262	3834.5	470	652	OUT312	2884.5	210
603	OUT263	3815.5	340	653	OUT313	2865.5	470
604	OUT264	3796.5	210	654	OUT314	2846.5	340
605	OUT265	3777.5	470	655	OUT315	2827.5	210
606	OUT266	3758.5	340	656	OUT316	2808.5	470
607	OUT267	3739.5	210	657	OUT317	2789.5	340
608	OUT268	3720.5	470	658	OUT318	2770.5	210
609	OUT269	3701.5	340	659	OUT319	2751.5	470
610	OUT270	3682.5	210	660	OUT320	2732.5	340
611	OUT271	3663.5	470	661	OUT321	2713.5	210
612	OUT272	3644.5	340	662	OUT322	2694.5	470
613	OUT273	3625.5	210	663	OUT323	2675.5	340
614	OUT274	3606.5	470	664	OUT324	2656.5	210
615	OUT275	3587.5	340	665	OUT325	2637.5	470
616	OUT276	3568.5	210	666	OUT326	2618.5	340
617	OUT277	3549.5	470	667	OUT327	2599.5	210
618	OUT278	3530.5	340	668	OUT328	2580.5	470
619	OUT279	3511.5	210	669	OUT329	2561.5	340
620	OUT280	3492.5	470	670	OUT330	2542.5	210
621	OUT281	3473.5	340	671	OUT331	2523.5	470
622	OUT282	3454.5	210	672	OUT332	2504.5	340
623	OUT283	3435.5	470	673	OUT333	2485.5	210
624	OUT284	3416.5	340	674	OUT334	2466.5	470
625	OUT285	3397.5	210	675	OUT335	2447.5	340
626	OUT286	3378.5	470	676	OUT336	2428.5	210
627	OUT287	3359.5	340	677	OUT337	2409.5	470
628	OUT288	3340.5	210	678	OUT338	2390.5	340
629	OUT289	3321.5	470	679	OUT339	2371.5	210
630	OUT290	3302.5	340	680	OUT340	2352.5	470
631	OUT291	3283.5	210	681	OUT341	2333.5	340
632	OUT292	3264.5	470	682	OUT342	2314.5	210
633	OUT293	3245.5	340	683	OUT343	2295.5	470
634	OUT294	3226.5	210	684	OUT344	2276.5	340
635	OUT295	3207.5	470	685	OUT345	2257.5	210
636	OUT296	3188.5	340	686	OUT346	2238.5	470
637	OUT297	3169.5	210	687	OUT347	2219.5	340
638	OUT298	3150.5	470	688	OUT348	2200.5	210
639	OUT299	3131.5	340	689	OUT349	2181.5	470
640	OUT300	3112.5	210	690	OUT350	2162.5	340
641	OUT301	3093.5	470	691	OUT351	2143.5	210
642	OUT302	3074.5	340	692	OUT352	2124.5	470
643	OUT303	3055.5	210	693	OUT353	2105.5	340
644	OUT304	3036.5	470	694	OUT354	2086.5	210
645	OUT305	3017.5	340	695	OUT355	2067.5	470
646	OUT306	2998.5	210	696	OUT356	2048.5	340
647	OUT307	2979.5	470	697	OUT357	2029.5	210
648	OUT308	2960.5	340	698	OUT358	2010.5	470
649	OUT309	2941.5	210	699	OUT359	1991.5	340
650	OUT310	2922.5	470	700	OUT360	1972.5	210

NO.	NAME	X	Y
701	OUT361	1953.5	470
702	OUT362	1934.5	340
703	OUT363	1915.5	210
704	OUT364	1896.5	470
705	OUT365	1877.5	340
706	OUT366	1858.5	210
707	OUT367	1839.5	470
708	OUT368	1820.5	340
709	OUT369	1801.5	210
710	OUT370	1782.5	470
711	OUT371	1763.5	340
712	OUT372	1744.5	210
713	OUT373	1725.5	470
714	OUT374	1706.5	340
715	OUT375	1687.5	210
716	OUT376	1668.5	470
717	OUT377	1649.5	340
718	OUT378	1630.5	210
719	OUT379	1611.5	470
720	OUT380	1592.5	340
721	OUT381	1573.5	210
722	OUT382	1554.5	470
723	OUT383	1535.5	340
724	OUT384	1516.5	210
725	OUT385	1497.5	470
726	OUT386	1478.5	340
727	OUT387	1459.5	210
728	OUT388	1440.5	470
729	OUT389	1421.5	340
730	OUT390	1402.5	210
731	OUT391	1383.5	470
732	OUT392	1364.5	340
733	OUT393	1345.5	210
734	OUT394	1326.5	470
735	OUT395	1307.5	340
736	OUT396	1288.5	210
737	OUT397	1269.5	470
738	OUT398	1250.5	340
739	OUT399	1231.5	210
740	OUT400	1212.5	470
741	OUT401	1193.5	340
742	OUT402	1174.5	210
743	OUT403	1155.5	470
744	OUT404	1136.5	340
745	OUT405	1117.5	210
746	OUT406	1098.5	470
747	OUT407	1079.5	340
748	OUT408	1060.5	210
749	OUT409	1041.5	470
750	OUT410	1022.5	340

NO.	NAME	X	Y
751	OUT411	1003.5	210
752	OUT412	984.5	470
753	OUT413	965.5	340
754	OUT414	946.5	210
755	OUT415	927.5	470
756	OUT416	908.5	340
757	OUT417	889.5	210
758	OUT418	870.5	470
759	OUT419	851.5	340
760	OUT420	832.5	210
761	OUT421	813.5	470
762	OUT422	794.5	340
763	OUT423	775.5	210
764	OUT424	756.5	470
765	OUT425	737.5	340
766	OUT426	718.5	210
767	OUT427	699.5	470
768	OUT428	680.5	340
769	OUT429	661.5	210
770	OUT430	642.5	470
771	OUT431	623.5	340
772	OUT432	604.5	210
773	OUT433	585.5	470
774	OUT434	566.5	340
775	OUT435	547.5	210
776	OUT436	528.5	470
777	OUT437	509.5	340
778	OUT438	490.5	210
779	OUT439	471.5	470
780	OUT440	452.5	340
781	OUT441	433.5	210
782	OUT442	414.5	470
783	OUT443	395.5	340
784	OUT444	376.5	210
785	OUT445	357.5	470
786	OUT446	338.5	340
787	OUT447	319.5	210
788	OUT448	300.5	470
789	OUT449	281.5	340
790	OUT450	262.5	210
791	OUT451	243.5	470
792	OUT452	224.5	340
793	OUT453	205.5	210
794	OUT454	186.5	470
795	OUT455	167.5	340
796	OUT456	148.5	210
797	OUT457	129.5	470
798	OUT458	110.5	340
799	OUT459	91.5	210
800	OUT460	72.5	470

NO.	NAME	X	Y	NO.	NAME	X	Y
801	OUT461	53.5	340	851	OUT494	-1540.5	340
802	OUT462	34.5	210	852	OUT495	-1559.5	210
803	OUT463	15.5	470	853	OUT496	-1578.5	470
804	OUT464	-3.5	340	854	OUT497	-1597.5	340
805	OUT465	-22.5	210	855	OUT498	-1616.5	210
806	OUT466	-41.5	470	856	OUT499	-1635.5	470
807	OUT467	-60.5	340	857	OUT500	-1654.5	340
808	OUT468	-79.5	210	858	OUT501	-1673.5	210
809	OUT469	-98.5	470	859	OUT502	-1692.5	470
810	OUT470	-117.5	340	860	OUT503	-1711.5	340
811	OUT471	-136.5	210	861	OUT504	-1730.5	210
812	OUT472	-155.5	470	862	OUT505	-1749.5	470
813	OUT473	-174.5	340	863	OUT506	-1768.5	340
814	OUT474	-193.5	210	864	OUT507	-1787.5	210
815	OUT475	-212.5	470	865	OUT508	-1806.5	470
816	OUT476	-231.5	340	866	OUT509	-1825.5	340
817	OUT477	-250.5	210	867	OUT510	-1844.5	210
818	OUT478	-269.5	470	868	OUT511	-1863.5	470
819	OUT479	-288.5	340	869	OUT512	-1882.5	340
820	OUT480	-307.5	210	870	OUT513	-1901.5	210
821	DUMMY	-325.5	470	871	OUT514	-1920.5	470
822	DUMMY	-382.5	470	872	OUT515	-1939.5	340
823	DUMMY	-439.5	470	873	OUT516	-1958.5	210
824	DUMMY	-496.5	470	874	OUT517	-1977.5	470
825	DUMMY	-553.5	470	875	OUT518	-1996.5	340
826	DUMMY	-610.5	470	876	OUT519	-2015.5	210
827	DUMMY	-667.5	470	877	OUT520	-2034.5	470
828	DUMMY	-724.5	470	878	OUT521	-2053.5	340
829	DUMMY	-781.5	470	879	OUT522	-2072.5	210
830	DUMMY	-838.5	470	880	OUT523	-2091.5	470
831	DUMMY	-895.5	470	881	OUT524	-2110.5	340
832	DUMMY	-952.5	470	882	OUT525	-2129.5	210
833	DUMMY	-1009.5	470	883	OUT526	-2148.5	470
834	DUMMY	-1066.5	470	884	OUT527	-2167.5	340
835	DUMMY	-1123.5	470	885	OUT528	-2186.5	210
836	DUMMY	-1180.5	470	886	OUT529	-2205.5	470
837	DUMMY	-1237.5	470	887	OUT530	-2224.5	340
838	OUT481	-1293.5	470	888	OUT531	-2243.5	210
839	OUT482	-1312.5	340	889	OUT532	-2262.5	470
840	OUT483	-1331.5	210	890	OUT533	-2281.5	340
841	OUT484	-1350.5	470	891	OUT534	-2300.5	210
842	OUT485	-1369.5	340	892	OUT535	-2319.5	470
843	OUT486	-1388.5	210	893	OUT536	-2338.5	340
844	OUT487	-1407.5	470	894	OUT537	-2357.5	210
845	OUT488	-1426.5	340	895	OUT538	-2376.5	470
846	OUT489	-1445.5	210	896	OUT539	-2395.5	340
847	OUT490	-1464.5	470	897	OUT540	-2414.5	210
848	OUT491	-1483.5	340	898	OUT541	-2433.5	470
849	OUT492	-1502.5	210	899	OUT542	-2452.5	340
850	OUT493	-1521.5	470	900	OUT543	-2471.5	210

NO.	NAME	X	Y	NO.	NAME	X	Y
901	OUT544	-2490.5	470	951	OUT594	-3440.5	210
902	OUT545	-2509.5	340	952	OUT595	-3459.5	470
903	OUT546	-2528.5	210	953	OUT596	-3478.5	340
904	OUT547	-2547.5	470	954	OUT597	-3497.5	210
905	OUT548	-2566.5	340	955	OUT598	-3516.5	470
906	OUT549	-2585.5	210	956	OUT599	-3535.5	340
907	OUT550	-2604.5	470	957	OUT600	-3554.5	210
908	OUT551	-2623.5	340	958	OUT601	-3573.5	470
909	OUT552	-2642.5	210	959	OUT602	-3592.5	340
910	OUT553	-2661.5	470	960	OUT603	-3611.5	210
911	OUT554	-2680.5	340	961	OUT604	-3630.5	470
912	OUT555	-2699.5	210	962	OUT605	-3649.5	340
913	OUT556	-2718.5	470	963	OUT606	-3668.5	210
914	OUT557	-2737.5	340	964	OUT607	-3687.5	470
915	OUT558	-2756.5	210	965	OUT608	-3706.5	340
916	OUT559	-2775.5	470	966	OUT609	-3725.5	210
917	OUT560	-2794.5	340	967	OUT610	-3744.5	470
918	OUT561	-2813.5	210	968	OUT611	-3763.5	340
919	OUT562	-2832.5	470	969	OUT612	-3782.5	210
920	OUT563	-2851.5	340	970	OUT613	-3801.5	470
921	OUT564	-2870.5	210	971	OUT614	-3820.5	340
922	OUT565	-2889.5	470	972	OUT615	-3839.5	210
923	OUT566	-2908.5	340	973	OUT616	-3858.5	470
924	OUT567	-2927.5	210	974	OUT617	-3877.5	340
925	OUT568	-2946.5	470	975	OUT618	-3896.5	210
926	OUT569	-2965.5	340	976	OUT619	-3915.5	470
927	OUT570	-2984.5	210	977	OUT620	-3934.5	340
928	OUT571	-3003.5	470	978	OUT621	-3953.5	210
929	OUT572	-3022.5	340	979	OUT622	-3972.5	470
930	OUT573	-3041.5	210	980	OUT623	-3991.5	340
931	OUT574	-3060.5	470	981	OUT624	-4010.5	210
932	OUT575	-3079.5	340	982	OUT625	-4029.5	470
933	OUT576	-3098.5	210	983	OUT626	-4048.5	340
934	OUT577	-3117.5	470	984	OUT627	-4067.5	210
935	OUT578	-3136.5	340	985	OUT628	-4086.5	470
936	OUT579	-3155.5	210	986	OUT629	-4105.5	340
937	OUT580	-3174.5	470	987	OUT630	-4124.5	210
938	OUT581	-3193.5	340	988	OUT631	-4143.5	470
939	OUT582	-3212.5	210	989	OUT632	-4162.5	340
940	OUT583	-3231.5	470	990	OUT633	-4181.5	210
941	OUT584	-3250.5	340	991	OUT634	-4200.5	470
942	OUT585	-3269.5	210	992	OUT635	-4219.5	340
943	OUT586	-3288.5	470	993	OUT636	-4238.5	210
944	OUT587	-3307.5	340	994	OUT637	-4257.5	470
945	OUT588	-3326.5	210	995	OUT638	-4276.5	340
946	OUT589	-3345.5	470	996	OUT639	-4295.5	210
947	OUT590	-3364.5	340	997	OUT640	-4314.5	470
948	OUT591	-3383.5	210	998	OUT641	-4333.5	340
949	OUT592	-3402.5	470	999	OUT642	-4352.5	210
950	OUT593	-3421.5	340	1000	OUT643	-4371.5	470

NO.	NAME	X	Y
1001	OUT644	-4390.5	340
1002	OUT645	-4409.5	210
1003	OUT646	-4428.5	470
1004	OUT647	-4447.5	340
1005	OUT648	-4466.5	210
1006	OUT649	-4485.5	470
1007	OUT650	-4504.5	340
1008	OUT651	-4523.5	210
1009	OUT652	-4542.5	470
1010	OUT653	-4561.5	340
1011	OUT654	-4580.5	210
1012	OUT655	-4599.5	470
1013	OUT656	-4618.5	340
1014	OUT657	-4637.5	210
1015	OUT658	-4656.5	470
1016	OUT659	-4675.5	340
1017	OUT660	-4694.5	210
1018	OUT661	-4713.5	470
1019	OUT662	-4732.5	340
1020	OUT663	-4751.5	210
1021	OUT664	-4770.5	470
1022	OUT665	-4789.5	340
1023	OUT666	-4808.5	210
1024	OUT667	-4827.5	470
1025	OUT668	-4846.5	340
1026	OUT669	-4865.5	210
1027	OUT670	-4884.5	470
1028	OUT671	-4903.5	340
1029	OUT672	-4922.5	210
1030	OUT673	-4941.5	470
1031	OUT674	-4960.5	340
1032	OUT675	-4979.5	210
1033	OUT676	-4998.5	470
1034	OUT677	-5017.5	340
1035	OUT678	-5036.5	210
1036	OUT679	-5055.5	470
1037	OUT680	-5074.5	340
1038	OUT681	-5093.5	210
1039	OUT682	-5112.5	470
1040	OUT683	-5131.5	340
1041	OUT684	-5150.5	210
1042	OUT685	-5169.5	470
1043	OUT686	-5188.5	340
1044	OUT687	-5207.5	210
1045	OUT688	-5226.5	470
1046	OUT689	-5245.5	340
1047	OUT690	-5264.5	210
1048	OUT691	-5283.5	470
1049	OUT692	-5302.5	340
1050	OUT693	-5321.5	210

NO.	NAME	X	Y
1051	OUT694	-5340.5	470
1052	OUT695	-5359.5	340
1053	OUT696	-5378.5	210
1054	OUT697	-5397.5	470
1055	OUT698	-5416.5	340
1056	OUT699	-5435.5	210
1057	OUT700	-5454.5	470
1058	OUT701	-5473.5	340
1059	OUT702	-5492.5	210
1060	OUT703	-5511.5	470
1061	OUT704	-5530.5	340
1062	OUT705	-5549.5	210
1063	OUT706	-5568.5	470
1064	OUT707	-5587.5	340
1065	OUT708	-5606.5	210
1066	OUT709	-5625.5	470
1067	OUT710	-5644.5	340
1068	OUT711	-5663.5	210
1069	OUT712	-5682.5	470
1070	OUT713	-5701.5	340
1071	OUT714	-5720.5	210
1072	OUT715	-5739.5	470
1073	OUT716	-5758.5	340
1074	OUT717	-5777.5	210
1075	OUT718	-5796.5	470
1076	OUT719	-5815.5	340
1077	OUT720	-5834.5	210
1078	OUT721	-5853.5	470
1079	OUT722	-5872.5	340
1080	OUT723	-5891.5	210
1081	OUT724	-5910.5	470
1082	OUT725	-5929.5	340
1083	OUT726	-5948.5	210
1084	OUT727	-5967.5	470
1085	OUT728	-5986.5	340
1086	OUT729	-6005.5	210
1087	OUT730	-6024.5	470
1088	OUT731	-6043.5	340
1089	OUT732	-6062.5	210
1090	OUT733	-6081.5	470
1091	OUT734	-6100.5	340
1092	OUT735	-6119.5	210
1093	OUT736	-6138.5	470
1094	OUT737	-6157.5	340
1095	OUT738	-6176.5	210
1096	OUT739	-6195.5	470
1097	OUT740	-6214.5	340
1098	OUT741	-6233.5	210
1099	OUT742	-6252.5	470
1100	OUT743	-6271.5	340

NO.	NAME	X	Y
1101	OUT744	-6290.5	210
1102	OUT745	-6309.5	470
1103	OUT746	-6328.5	340
1104	OUT747	-6347.5	210
1105	OUT748	-6366.5	470
1106	OUT749	-6385.5	340
1107	OUT750	-6404.5	210
1108	OUT751	-6423.5	470
1109	OUT752	-6442.5	340
1110	OUT753	-6461.5	210
1111	OUT754	-6480.5	470
1112	OUT755	-6499.5	340
1113	OUT756	-6518.5	210
1114	OUT757	-6537.5	470
1115	OUT758	-6556.5	340
1116	OUT759	-6575.5	210
1117	OUT760	-6594.5	470
1118	OUT761	-6613.5	340
1119	OUT762	-6632.5	210
1120	OUT763	-6651.5	470
1121	OUT764	-6670.5	340
1122	OUT765	-6689.5	210
1123	OUT766	-6708.5	470
1124	OUT767	-6727.5	340
1125	OUT768	-6746.5	210
1126	OUT769	-6765.5	470
1127	OUT770	-6784.5	340
1128	OUT771	-6803.5	210
1129	OUT772	-6822.5	470
1130	OUT773	-6841.5	340
1131	OUT774	-6860.5	210
1132	OUT775	-6879.5	470
1133	OUT776	-6898.5	340
1134	OUT777	-6917.5	210
1135	OUT778	-6936.5	470
1136	OUT779	-6955.5	340
1137	OUT780	-6974.5	210
1138	OUT781	-6993.5	470
1139	OUT782	-7012.5	340
1140	OUT783	-7031.5	210
1141	OUT784	-7050.5	470
1142	OUT785	-7069.5	340
1143	OUT786	-7088.5	210
1144	OUT787	-7107.5	470
1145	OUT788	-7126.5	340
1146	OUT789	-7145.5	210
1147	OUT790	-7164.5	470
1148	OUT791	-7183.5	340
1149	OUT792	-7202.5	210
1150	OUT793	-7221.5	470

NO.	NAME	X	Y
1151	OUT794	-7240.5	340
1152	OUT795	-7259.5	210
1153	OUT796	-7278.5	470
1154	OUT797	-7297.5	340
1155	OUT798	-7316.5	210
1156	OUT799	-7335.5	470
1157	OUT800	-7354.5	340
1158	OUT801	-7373.5	210
1159	OUT802	-7392.5	470
1160	OUT803	-7411.5	340
1161	OUT804	-7430.5	210
1162	OUT805	-7449.5	470
1163	OUT806	-7468.5	340
1164	OUT807	-7487.5	210
1165	OUT808	-7506.5	470
1166	OUT809	-7525.5	340
1167	OUT810	-7544.5	210
1168	OUT811	-7563.5	470
1169	OUT812	-7582.5	340
1170	OUT813	-7601.5	210
1171	OUT814	-7620.5	470
1172	OUT815	-7639.5	340
1173	OUT816	-7658.5	210
1174	OUT817	-7677.5	470
1175	OUT818	-7696.5	340
1176	OUT819	-7715.5	210
1177	OUT820	-7734.5	470
1178	OUT821	-7753.5	340
1179	OUT822	-7772.5	210
1180	OUT823	-7791.5	470
1181	OUT824	-7810.5	340
1182	OUT825	-7829.5	210
1183	OUT826	-7848.5	470
1184	OUT827	-7867.5	340
1185	OUT828	-7886.5	210
1186	OUT829	-7905.5	470
1187	OUT830	-7924.5	340
1188	OUT831	-7943.5	210
1189	OUT832	-7962.5	470
1190	OUT833	-7981.5	340
1191	OUT834	-8000.5	210
1192	OUT835	-8019.5	470
1193	OUT836	-8038.5	340
1194	OUT837	-8057.5	210
1195	OUT838	-8076.5	470
1196	OUT839	-8095.5	340
1197	OUT840	-8114.5	210
1198	OUT841	-8133.5	470
1199	OUT842	-8152.5	340
1200	OUT843	-8171.5	210

NO.	NAME	X	Y
1201	OUT844	-8190.5	470
1202	OUT845	-8209.5	340
1203	OUT846	-8228.5	210
1204	OUT847	-8247.5	470
1205	OUT848	-8266.5	340
1206	OUT849	-8285.5	210
1207	OUT850	-8304.5	470
1208	OUT851	-8323.5	340
1209	OUT852	-8342.5	210
1210	OUT853	-8361.5	470
1211	OUT854	-8380.5	340
1212	OUT855	-8399.5	210
1213	OUT856	-8418.5	470
1214	OUT857	-8437.5	340
1215	OUT858	-8456.5	210
1216	OUT859	-8475.5	470
1217	OUT860	-8494.5	340
1218	OUT861	-8513.5	210
1219	OUT862	-8532.5	470
1220	OUT863	-8551.5	340
1221	OUT864	-8570.5	210
1222	OUT865	-8589.5	470
1223	OUT866	-8608.5	340
1224	OUT867	-8627.5	210
1225	OUT868	-8646.5	470
1226	OUT869	-8665.5	340
1227	OUT870	-8684.5	210
1228	OUT871	-8703.5	470
1229	OUT872	-8722.5	340
1230	OUT873	-8741.5	210
1231	OUT874	-8760.5	470
1232	OUT875	-8779.5	340
1233	OUT876	-8798.5	210
1234	OUT877	-8817.5	470
1235	OUT878	-8836.5	340
1236	OUT879	-8855.5	210
1237	OUT880	-8874.5	470
1238	OUT881	-8893.5	340
1239	OUT882	-8912.5	210
1240	OUT883	-8931.5	470
1241	OUT884	-8950.5	340
1242	OUT885	-8969.5	210
1243	OUT886	-8988.5	470
1244	OUT887	-9007.5	340
1245	OUT888	-9026.5	210
1246	OUT889	-9045.5	470
1247	OUT890	-9064.5	340
1248	OUT891	-9083.5	210
1249	OUT892	-9102.5	470
1250	OUT893	-9121.5	340

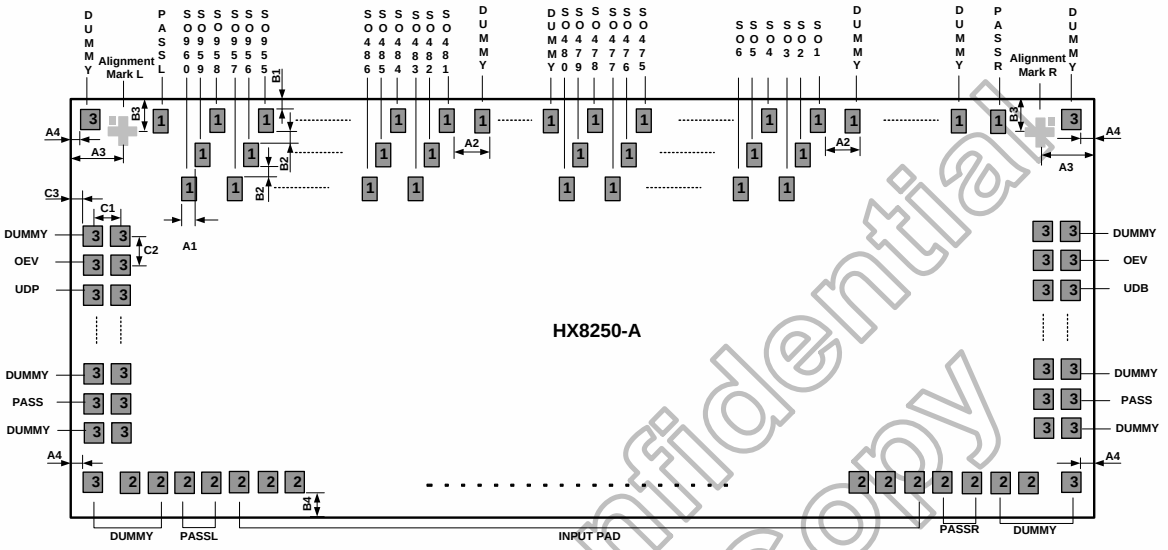
NO.	NAME	X	Y
1251	OUT894	-9140.5	210
1252	OUT895	-9159.5	470
1253	OUT896	-9178.5	340
1254	OUT897	-9197.5	210
1255	OUT898	-9216.5	470
1256	OUT899	-9235.5	340
1257	OUT900	-9254.5	210
1258	OUT901	-9273.5	470
1259	OUT902	-9292.5	340
1260	OUT903	-9311.5	210
1261	OUT904	-9330.5	470
1262	OUT905	-9349.5	340
1263	OUT906	-9368.5	210
1264	OUT907	-9387.5	470
1265	OUT908	-9406.5	340
1266	OUT909	-9425.5	210
1267	OUT910	-9444.5	470
1268	OUT911	-9463.5	340
1269	OUT912	-9482.5	210
1270	OUT913	-9501.5	470
1271	OUT914	-9520.5	340
1272	OUT915	-9539.5	210
1273	OUT916	-9558.5	470
1274	OUT917	-9577.5	340
1275	OUT918	-9596.5	210
1276	OUT919	-9615.5	470
1277	OUT920	-9634.5	340
1278	OUT921	-9653.5	210
1279	OUT922	-9672.5	470
1280	OUT923	-9691.5	340
1281	OUT924	-9710.5	210
1282	OUT925	-9729.5	470
1283	OUT926	-9748.5	340
1284	OUT927	-9767.5	210
1285	OUT928	-9786.5	470
1286	OUT929	-9805.5	340
1287	OUT930	-9824.5	210
1288	OUT931	-9843.5	470
1289	OUT932	-9862.5	340
1290	OUT933	-9881.5	210
1291	OUT934	-9900.5	470
1292	OUT935	-9919.5	340
1293	OUT936	-9938.5	210
1294	OUT937	-9957.5	470
1295	OUT938	-9976.5	340
1296	OUT939	-9995.5	210
1297	OUT940	-10014.5	470
1298	OUT941	-10033.5	340
1299	OUT942	-10052.5	210
1300	OUT943	-10071.5	470

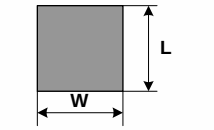
NO.	NAME	X	Y
1301	OUT944	-10090.5	340
1302	OUT945	-10109.5	210
1303	OUT946	-10128.5	470
1304	OUT947	-10147.5	340
1305	OUT948	-10166.5	210
1306	OUT949	-10185.5	470
1307	OUT950	-10204.5	340
1308	OUT951	-10223.5	210
1309	OUT952	-10242.5	470
1310	OUT953	-10261.5	340
1311	OUT954	-10280.5	210
1312	OUT955	-10299.5	470
1313	OUT956	-10318.5	340
1314	OUT957	-10337.5	210
1315	OUT958	-10356.5	470
1316	OUT959	-10375.5	340
1317	OUT960	-10394.5	210
1318	PASSL	-10413.5	470
1319	MARK_L	-10504.5	457.5
1320	SIDE_DUMMY	-10612	495

NO.	NAME	X	Y
1321	DUMMY	-10612	312
1322	DUMMY	-10542	312
1323	OEV	-10612	234
1324	OEV	-10542	234
1325	UDP	-10612	156
1326	UDP	-10542	156
1327	CKV	-10612	78
1328	CKV	-10542	78
1329	STVD	-10612	0
1330	STVD	-10542	0
1331	STVU	-10612	-78
1332	STVU	-10542	-78
1333	DUMMY	-10612	-156
1334	DUMMY	-10542	-156
1335	PASS	-10612	-234
1336	PASS	-10542	-234
1337	DUMMY	-10612	-312
1338	DUMMY	-10542	-312

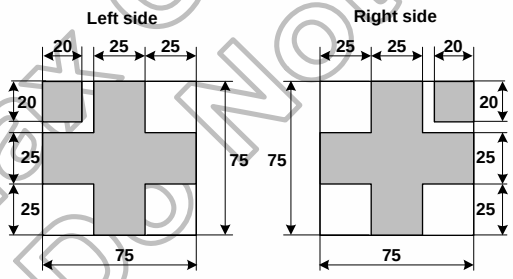
12. Bump Mask information

- Chip size: 21405 μm x 1170 μm
- Bump height: 15 μm ± 3 μm
- Bump hardness: 60 H_V ± 15 H_V

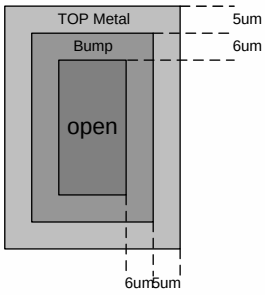




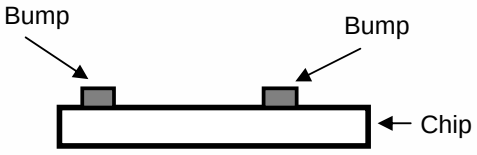
Alignment mark dimension unit:um



1 : WxL = 17umx100um
2 : WxL = 50umx90um
3 : WxL = 50umx50um



Symbol	Dimension (μm)
A1	19
A2	57
A3	198
A4	65.5
B1	65
B2	30
B3	127.5
B4	65
C1	70
C2	78
C3	65.5



The figure of "View Angle"

13. Ordering Information

PART NO.	PACKAGE TYPE
HX8250-A000PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400μm)

14. Revision History

Version	Date	Description of Changes
00	2006/08/11	New setup
	2006/08/24	1. Add FRP register. 2. Change 1920x240 interface to Serial RGB, Parallel RGB, CCIR601, CCIR656 mode.
	2006/09/01	1. Add CSH register. 2. Add FRP, CSH pin. 3. Change IF[2:0] default=001, RESL[1:0]=10.
	2006/09/06	1. Modify Figure5.2 Cascade diagram error.
	2006/09/15	1. Add 10. Pin Assignment 2. Modify P21 T_{HV_O}, T_{HV_E} definition.
	2006/09/25	1. Modify the AC timing of the 1920x240. (page25) 2. Modify the AC timing of the 1920x480. (page26) 3. Modify the data format figures. (page30~38) 4. Add the PAL mode skipped line location. (page39)
	2006/10/03	1. Add the OSD output timing. (page40、41)
	2006/10/04	1. Modify 10. Pin Assignment. (page44) 2. Remove POL pin, add POL_I, POL_O, PASS1, PASS2 pins. (Page5、6)
01	2006/10/13	1. Add Cascade mode POL signal layout notice. (Page11) 2. Modify type error of FRAD note. (Page15) 3. Change 5.11 to reset when power on. (Page19) 4. Modify type error of 6.2 DC EL Characteristics. (Page20) 5. Add Pin outline. (Page45~59) 6. Add Bump information. (Page60) 7. Add Chip size. (Page60)
02	2006/10/30	1. Add description to OSD_EN pin. (Page 6) 2. Add description to PASS, PASSL, PASSR pins. (Page7) 3. Add recommend input resistance. (Page7) 4. Add 5.2 LR and UD control. (Page 8~11) 5. Add Gamma table when VSET=L. (Page16~17) 6. Modify Figure 5.2 UDP/UDB setting. (Page 18) 7. Modify Figure 5.6 Set RESETB when VCC/VDD stable. (Page 26) 8. Modify Pin assignment. (Page 51) 9. Modify Pin outline & pad location. (Page 52~66) 10. Modify Alignment mark dimension. (Page 67) 11. Modify A3, A4, B3, C3 dimension. (Page 67)

03	2007/01/29	1. Change Pins V1~V14 to V1~V10. (Remove original V2, V6, V9, V13 and rename V3~V5 to V2~V4, V7~V8 to V5~V6, V10~V12 to V7~V9, V14 to V10) (Page 3, 4, 6) 2. Add Caution 3 for V1~V10 input notice. (Page 7) 3. Modify Gamma table for changing V1~V14 to V1~V10. (Page 12~17) 4. Add TESTG[3:0] and TESTGO, TESTO Pins. (Page 6) 5. Modify 11.1 Pad diagram TESTO[7:0] -> TP[7:0], VDDA -> VDD, VSSA-> VSS, VSS -> GND, 1318 PASSR -> PASSL, 1326 UDB -> UDP, V1~V14 -> V1~V10, Dummy -> TESTG[3:0], Dummy -> TESTGO (Page 52~54, 66) 6. Modify Pin assignment. (Page 51) 7. Modify Cascade mode description. (Page 12) 8. Change Operation description 5.4~5.6 to 5.3~5.5. (Page 11, 12) 9. Change Gamma table from 5.3 to 5.6. (Page 13~16) 10. “normally” pull high/low rename “default” pull high/low(Page 5~6) 11. Rename from “HS-DEN time” to “HS-first horizontal data time”. (Page 29~33) 12. Seperate RGB Horizontal data format diagram into individual SYNC and DE mode diagrams. (Page 37) 13. Modify 6.2 DC characteristic : IDD=6mA, ICC=2.5mA. (Page 27) 14. Rename “A_TIME” to “A_TIME[1:0]”, “B_TIME” to “B_TIME[2:0]” (Page 24)
04	2007/05/04	1. Modify pin V1~V14 to V1~V10. (Page 50) 2. Modify Cascade mode description. (Page 12) 3. Modify DC characteristic pull high pin : RESL1, IF0 (Page 27)