DATA SHEET

(DOC No. HX8258-A-DS)

HX8258-A

1200/1026 CH TFT LCD Source Driver with TCON

Version 04 April, 2009

Himax Technologies, Inc.
http://www.himax.com.tw

1. General Description

HX8258-A is a 1200/1026 channel outputs source driver with TCON, and 3-wire Serial Port Interface. It also supports 3-chip cascade mode to extend source channel to be 3072-channel outputs (resolution: 1024RGB x 768).

The interface follows digital 24-bit parallel RGB input format. The TCON generates the 400x240, 800x480, 800x600, 1024x600 and 1024x768 resolutions and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales.

The source driver receives 6-bit by 3 dots of digital display data per clock from TCON and generates corresponding 64-level gray scale voltage output. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation. Therefore, a high quality display with less crosstalk can be achieved.

2. Features

TCON

- Support display resolution 400x240, 800x480, 800x600, 1024x600 and 1024x768
- Support digital 24-bit parallel RGB input mode
- Internal dithering 8-bit data to 6-bit data for Source Driver Circuit
- Only support stripe types of panel group
- Operation frequency: 70 MHz max
- Provide source and gate drivers control timing
- Provide flip and mirror scan control
- Operation Voltage Level 2.7V to 3.6V

Source Driver

- 1200 channels output source driver for TFT LCD panel
- Dynamic output range: 0.1 to VDDA-0.1V
- Voltage deviation of outputs: ±20mV
- Dot inversion driving scheme
- Right and left shift capability
- LCD power: 6.5 to 13.5V

Others

- COG package

3. Block Diagram

3.1 Whole chip block diagram

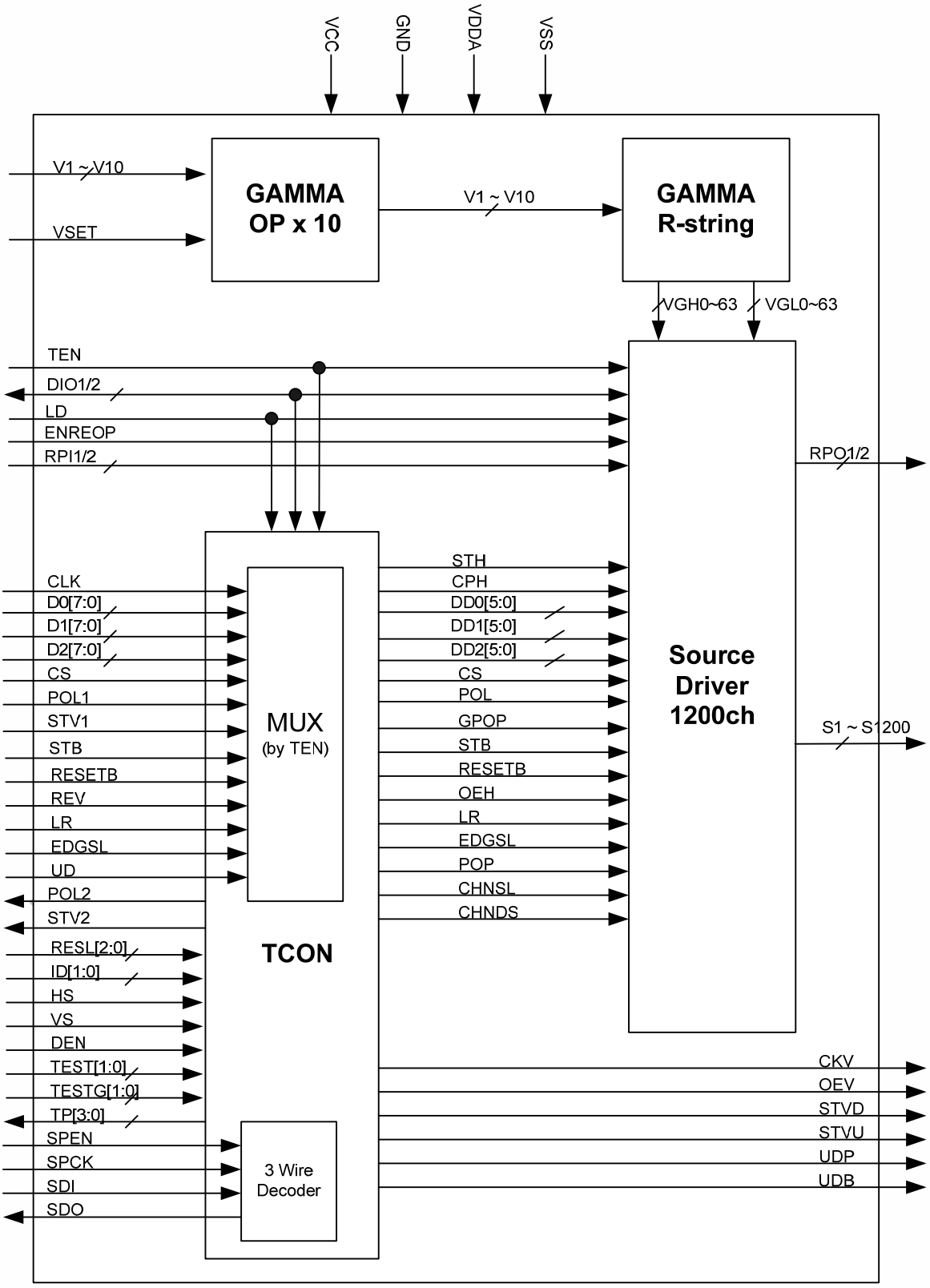


Figure 3. 1 HX8258-A block diagram

3.2 Source driver block diagram

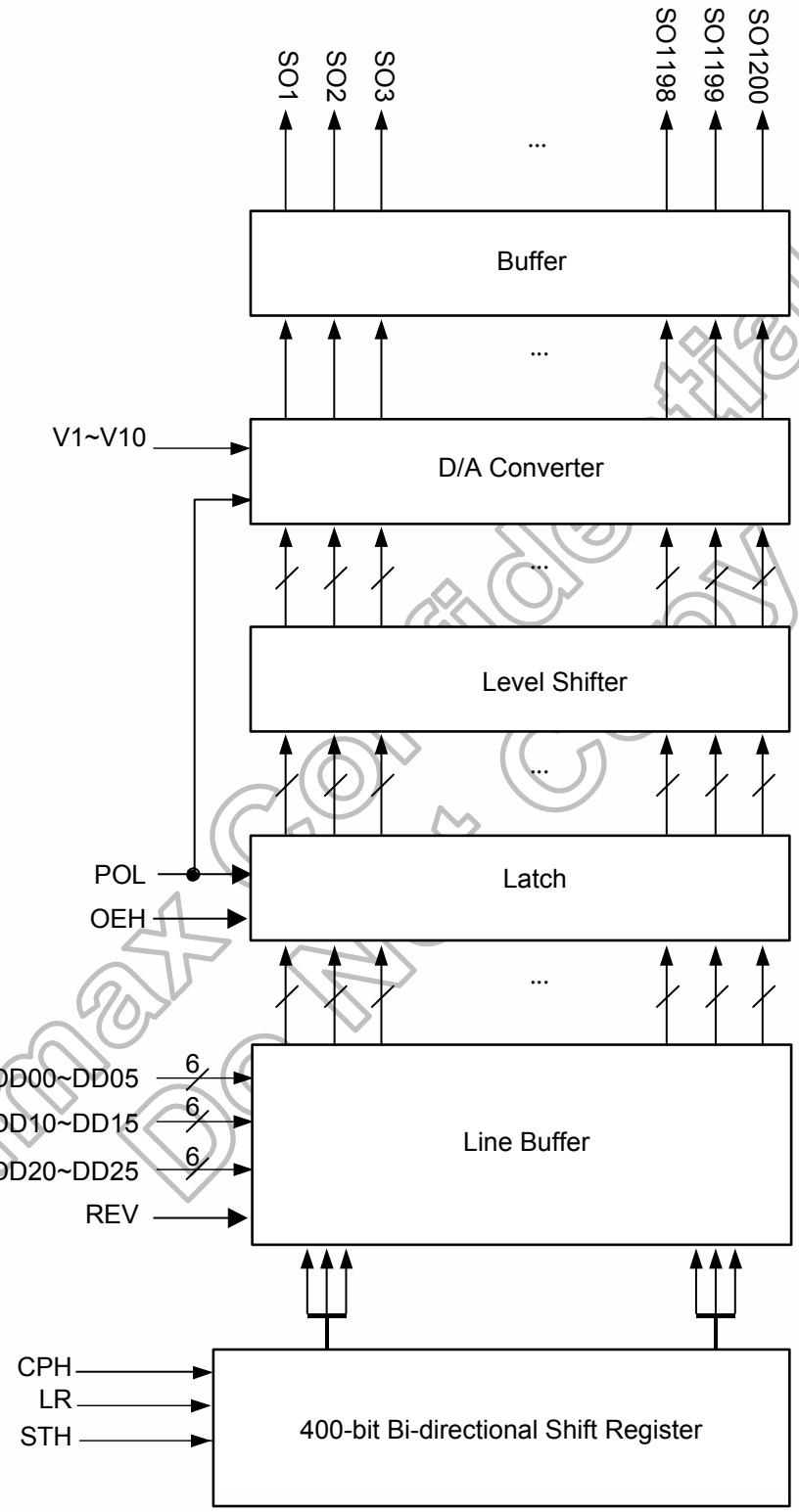


Figure 3. 2 Source driver block diagram

4. Pin description

Pin name	I/O	TEN Setting	Description
CLK	I	H	Clock signal. User can input different polarity CLK by EDGSL setting.
		L	Clock signal. User can select CLK rising or dual edge to latch data by EDGSL setting.
D07~D00 D17~D10 D27~D20	I	H	Digital data input. Dx0 is LSB and Dx7 is MSB. (Default pull low). D0x, D1x, and D2x indicate R, G, and B data in turn. When disable dithering function, please use Dx7~Dx2 as 6-bit input.
		L	Dx7 ~ Dx2 are HX8258-A Source Driver 6-bit data input, short Dx1 and Dx0 to GND.
HS	I	H	Horizontal sync input in digital parallel RGB.
		L	Short HS to GND
VS	I	H	Vertical sync input in digital parallel RGB.
		L	Short VS to GND
DEN	I	H	Input data enable control. When DE mode, active High to enable data input. (Default pull low).
		L	Short DEN to GND
RESETB	I	H/L	Hardware global reset. Low active. (Default pull high).
DIO1	I/O	H	Short DIO1 to GND
		L	When LR = H, DIO1 is used for start pulse input. When LR = L, DIO1 is used for start pulse output. ***Don't input redundancy DIO in blanking period.**
DIO2	I/O	H	Short DIO2 to GND
		L	When LR = H, DIO2 is used for start pulse output. When LR = L, DIO2 is used for start pulse input. ***Don't input redundancy DIO in blanking period.**
LD	I	H	Short LD to GND.
		L	The contents of the data register are transferred to the latch circuit at the rising edge of LD. Then the gray scale voltage is output from the device at the falling edge of LD. For normal operation, it is required to input one LD per horizontal display line.
TEN	I	H	TCON enable control. HX8258-A internal TCON enable (Default pull high).
		L	HX8258-A internal TCON disable.
POL1	I	H	Polarity signal of cascade source drivers. Detail setting refer to 5.3 cascade mode setting.
		L	POL1=L, use V1 to V5 for OUT_{2n-1} & V6 to V10 for OUT_{2n}. POL1=H, use V6 to V10 for OUT_{2n-1} & V1 to V5 for OUT_{2n}.
POL2	O	H	Polarity signal of cascade source drivers. Detail setting refer to 5.3 cascade mode setting.
		L	Floating POL2
REV	I	H	REV=H, normally black panel. REV=L, normally white panel. (default pull low)
		L	The REV signal controls data inversion internally to Source Driver. REV=H, display data is inverted. REV=L, display data is not inverted.

<table>
<tr><th>Pin name</th><th>I/O</th><th>TEN Setting</th><th>Description</th></tr>
<tr><td>LR</td><td>I</td><td>H/L</td><td>Shift direction of HX8258-A Source Driver internal shift register is controlled by this pin as shown below:
LR=H: DIO1→SO1→• • •→SO1200→DIO2 (default pull high)
LR=L: DIO2→SO1200→• • •→SO1→DIO1</td></tr>
<tr><td rowspan="2">UD</td><td rowspan="2">I</td><td>H</td><td>Gate Driver Up/down scan setting.
When UD=H, reverse scan.
When UD=L, normal scan. (Default pull low).</td></tr>
<tr><td>L</td><td>Short UD to GND</td></tr>
<tr><td>CS</td><td>I</td><td>H/L</td><td>Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function. (Default pull high).</td></tr>
<tr><td>STB</td><td>I</td><td>H/L</td><td>Standby mode control.
When STB=L, TCON and source driver are off.
When STB=H, all the functions are on. (Default pull high).</td></tr>
<tr><td>RESL[2:0]</td><td>I</td><td>H/L</td><td>Control the resolution selection.
<table>
<tr><th>RESL[2:0]</th><th>Resolution</th></tr>
<tr><td>000</td><td>800x480 (Default)</td></tr>
<tr><td>001</td><td>800x600</td></tr>
<tr><td>010</td><td>1024x600</td></tr>
<tr><td>011</td><td>1024x768</td></tr>
<tr><td>100</td><td>NA</td></tr>
<tr><td>101</td><td>NA</td></tr>
<tr><td>110</td><td>NA</td></tr>
<tr><td>111</td><td>400x240</td></tr>
</table></td></tr>
<tr><td>VSET</td><td>I</td><td>H/L</td><td>Gamma correction voltage can be set to input 4 voltage levels or 10 voltage levels externally.
VSET=L, only externally input V1, V5, V6 and V10 reference voltage, others reference voltage are generated by internal resistors.
VSET=H, externally input V1~V10 reference voltage.
No matter what setting, it doesn’t need OPA buffer to the reference inputs. (default pull high)</td></tr>
<tr><td rowspan="2">STV1</td><td rowspan="2">I</td><td>H</td><td>Short STV1 to GND</td></tr>
<tr><td>L</td><td>Offset cancel signal of cascade HX8258-A Source Drivers.
Detail setting refer to 5.3 cascade mode setting</td></tr>
<tr><td rowspan="2">STV2</td><td rowspan="2">O</td><td>H</td><td>Floating STV2</td></tr>
<tr><td>L</td><td>Offset cancel signal of cascade HX8258-A Source Drivers.
Detail setting refer to 5.3 cascade mode setting</td></tr>
<tr><td rowspan="2">EDGSL</td><td rowspan="2">I</td><td>H</td><td>Define input clock polarity
When EDGSL=L, latch data by rising edge of CLK. (default pull low)
When EDGSL=H, CLK polarity is inverted, latch data by falling edge of CLK.</td></tr>
<tr><td>L</td><td>Define clock edge select input.
When EDGSL = L, Latch data by rising edge of CLK. (Default pull low).
When EDGSL = H, Latch data by rising and falling edges of CLK.</td></tr>
<tr><td>ENREOP</td><td>I</td><td>H/L</td><td>Enable repair line OP RPI1/2, RPO1/2
ENREOP = H, Enable repair line OP RPI1/2, RPO1/2
ENREOP = L, Disable repair line OP RPI1/2, RPO1/2 (Default pull low).</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>TEN Setting</th><th>Description</th></tr>
<tr><td>RPI1/2</td><td>I</td><td>H/L</td><td>Repair OP input.</td></tr>
<tr><td>RPO1/2</td><td>O</td><td>H/L</td><td>Repair OP output.</td></tr>
<tr><td>V1~V10</td><td>I</td><td>H/L</td><td>Used as reference voltage input pins.
Hold the reference voltage fixed during the period of LCD drive output. To ensure the correct analog voltage is output from D/A converter, the V1~V10 must be stable before D/A conversion.
VDDA>V1>V2>V3>V4>V5>V6>V7>V8>V9>V10>VSS.</td></tr>
<tr><td>ID[1:0]</td><td>I</td><td>H/L</td><td>Work with RESL[2:0], LR
<table>
<tr><th rowspan="2">RESL[2:0]</th><th rowspan="2">ID[1:0]</th><th colspan="2">Sample cycle</th><th rowspan="2">Channel Number</th></tr>
<tr><th>LR = H</th><th>LR = L</th></tr>
<tr><td rowspan="4">000/001 (800X480/ 800X600)</td><td>00</td><td>1 ~ 400</td><td>401 ~ 800</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>01</td><td>401 ~ 800</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>10</td><td colspan="3">NA</td></tr>
<tr><td>11</td></tr>
<tr><td rowspan="4">010/011 (1024X600/ 1024X768)</td><td>00</td><td>1 ~ 342</td><td>683 ~ 1024</td><td>1026CH (S1 ~ S513/S688 ~ S1200)</td></tr>
<tr><td>01</td><td>343 ~ 684</td><td>341 ~ 682</td><td>1026CH (S1 ~ S513/S688 ~ S1200)</td></tr>
<tr><td>10</td><td>685 ~ 1024</td><td>1 ~ 340</td><td>1020CH (S1 ~ S513/S688 ~ S1194)</td></tr>
<tr><td>11</td><td colspan="3">NA</td></tr>
<tr><td rowspan="4">111 (400x240)</td><td>00</td><td>1 ~ 400</td><td>1 ~ 400</td><td>1200CH (S1 ~ S1200)</td></tr>
<tr><td>01</td><td colspan="3" rowspan="3">NA</td></tr>
<tr><td>10</td></tr>
<tr><td>11</td></tr>
</table></td></tr>
<tr><td rowspan="2">SPCK</td><td rowspan="2">I</td><td>H</td><td>Serial port Clock. (Default pull high).</td></tr>
<tr><td>L</td><td>Short SPCK to GND</td></tr>
<tr><td rowspan="2">SDI</td><td rowspan="2">I</td><td>H</td><td>Serial port Data input. (Default pull high).</td></tr>
<tr><td>L</td><td>Short SDI to GND</td></tr>
<tr><td rowspan="2">SPEN</td><td rowspan="2">I</td><td>H</td><td>Serial port Data Enable Signal. (Default pull high).</td></tr>
<tr><td>L</td><td>Short SPEN to GND</td></tr>
<tr><td rowspan="2">SDO</td><td rowspan="2">O</td><td>H</td><td>3-Wire serial bus data output</td></tr>
<tr><td>L</td><td>Floating SDO</td></tr>
<tr><td rowspan="2">CKV</td><td rowspan="2">O</td><td>H</td><td>Gate driver clock.</td></tr>
<tr><td>L</td><td>Floating CKV</td></tr>
<tr><td rowspan="2">OEV</td><td rowspan="2">O</td><td>H</td><td>Enable output control of gate driver.</td></tr>
<tr><td>L</td><td>Floating OEV</td></tr>
<tr><td rowspan="2">STVD</td><td rowspan="2">O</td><td>H</td><td>Start pulse for gate driver.
When UD=L, STVD is output.
When UD=H, STVD is Hi-Z.</td></tr>
<tr><td>L</td><td>Floating STVD</td></tr>
<tr><td rowspan="2">STVU</td><td rowspan="2">O</td><td>H</td><td>Start pulse for gate driver.
When UD=L, STVU is Hi-Z.
When UD=H, STVU is output.</td></tr>
<tr><td>L</td><td>Floating STVU</td></tr>
<tr><td rowspan="2">UDB</td><td rowspan="2">O</td><td>H</td><td>Reverse of UD.</td></tr>
<tr><td>L</td><td>Floating UDB</td></tr>
<tr><td rowspan="2">UDP</td><td rowspan="2">O</td><td>H</td><td>Internal link to UD.</td></tr>
<tr><td>L</td><td>Floating UDP</td></tr>
<tr><td>SO1~SO1200</td><td>O</td><td>H/L</td><td>Output driver signal.</td></tr>
<tr><td>TEST[1:0]</td><td>I</td><td>H/L</td><td>Test pins. (Default pull low).</td></tr>
<tr><td>TESTG[1:0]</td><td>I</td><td>H/L</td><td>Test pin. (Default pull low).</td></tr>
<tr><td>TP[3:0]</td><td>O</td><td>H/L</td><td>Test pins. They must be open.</td></tr>
<tr><td>VDDA</td><td>I</td><td>H/L</td><td>Analog power. 6.5V to 13.5V.</td></tr>
</table>

Pin name	I/O	TEN Setting	Description
VSS	I	H/L	Analog ground.
VCC	I	H/L	Digital power. 2.7V to 3.6V.
GND	I	H/L	Digital ground.
PASS1 PASS2	-	H/L	Link together internally. Please use as signal path, not power path.

Note: (1) Please power on following the sequence VCC → logic input → VDDA and V1 ~ V10. Reverse the sequence to shut down.

(2) To stabilize the supply voltages, please be sure to insert a 0.1uF bypass capacitor between VCC-GND and VDDA-VSS. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01uF is also advised between the gamma-corrected power supply terminals (V1, V2, …, V10) and VSS.

(3) Please keep V1~V10 not cross to the toggle signals as possible to avoid the AC coupling on the DC V1~V10 voltage. When used as cascade mode, please keep the coupled amount of V1~V10 are the same between the two chips.

(4) The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommended as below.

Pin Name	Wiring resistance value(Ω)
VCC(3.3V)	< 30
GND(0V)	< 30
VDDA(8.4V)	< 5
VSS(0V)	< 5
V1 ~ V10	< 100
CLK	< 100
Dx7 ~ Dx0	< 200
HS	< 200
VS	< 200
DEN	< 200
POL1 to POL2	< 200
STV1 to STV2	< 200
DIO1 to DIO2	< 200
Others	< 1000

5. Operation description

5.1 Relationship between input data and output channels

- **Source Driver**

LR	First					→		Last		
H	Out1	Out2	Out3	•••	•••	•••	•••	Out1198	Out1199	Out1200

LR	Last					←		First		
L	Out1200	Out1199	Out1198	•••	•••	•••	•••	Out3	Out2	Out1

Table 5. 1 Relationship between input data and output channels

5.2 HX8258-A chip Driver configuration with LR, ID0, ID1, RESL0, RESL1, RESL2

HX8258-A supports timing controller for five resolutions. Since HX8258-A has 1200 channels, for example, two pieces of HX8258-A source drivers are cascaded for extended 2400 channels for 800RGB. The configuration examples of the HX8258-A are illustrated as figure 5.1 ~ 5.20.

RESL[2:0] 111 400x240

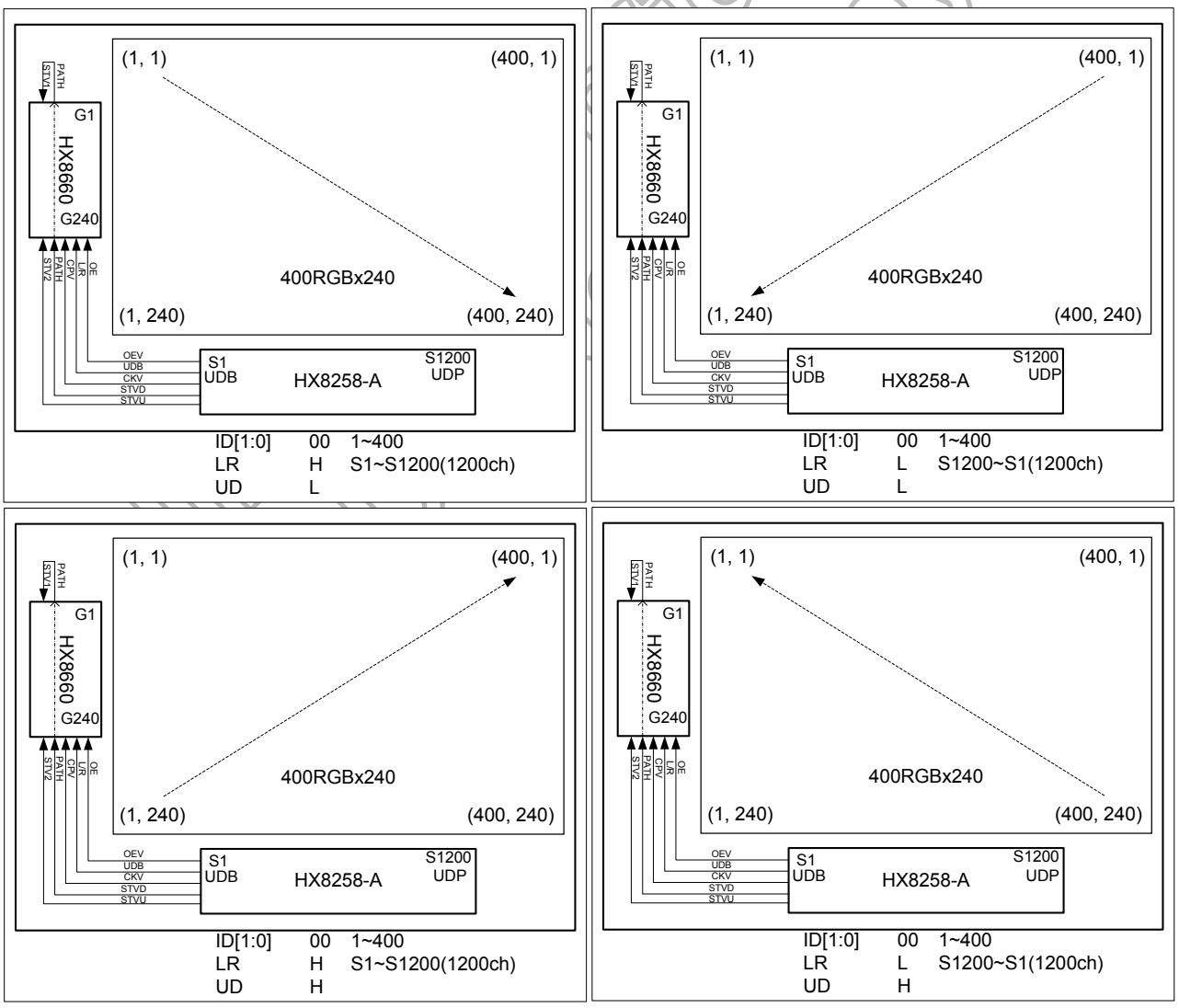


Figure 5. 1 HX8258-A put down side and HX8660 put left side for 400RGB X 240

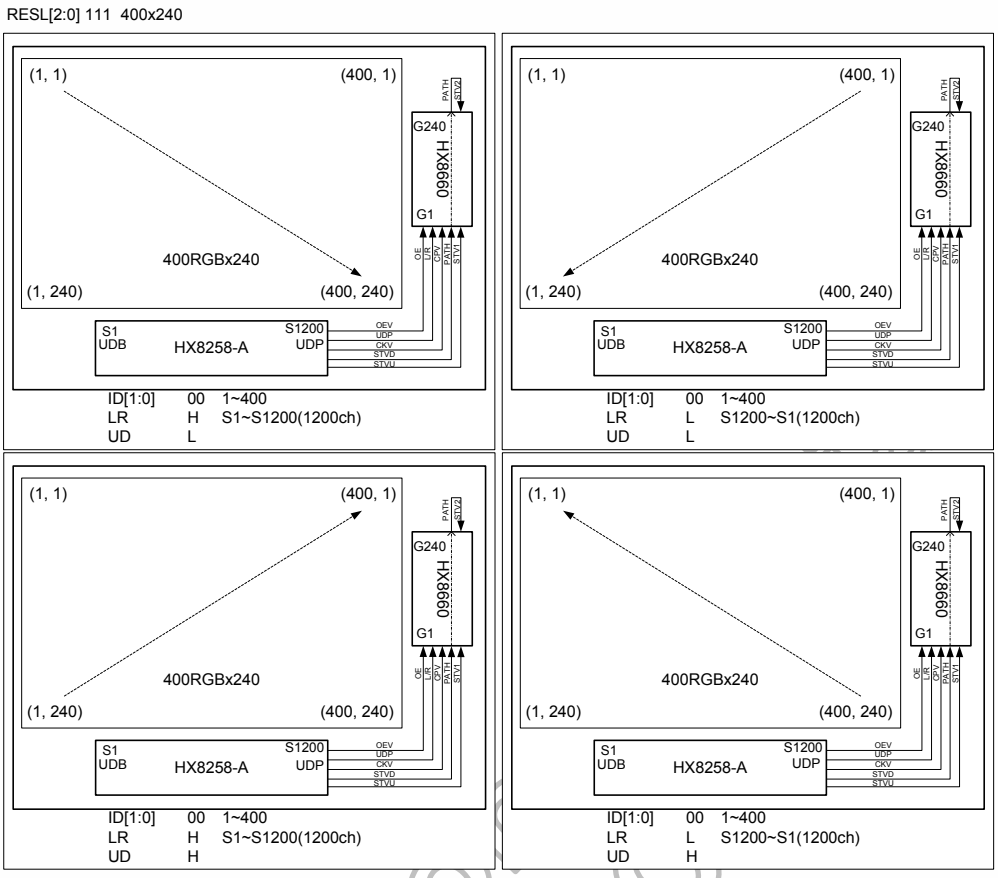


Figure 5. 2 HX8258-A put down side and HX8660 put right side for 400RGB X 240

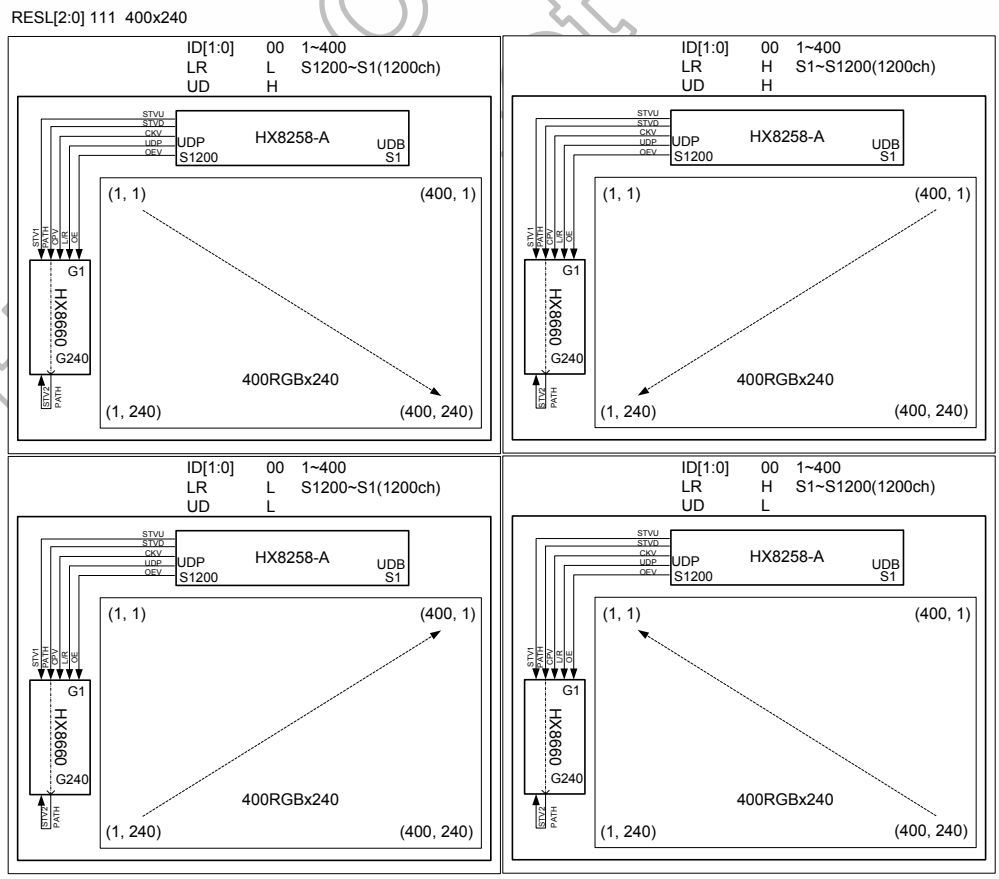


Figure 5. 3 HX8258-A put up side and HX8660 put left side for 400RGB X 240

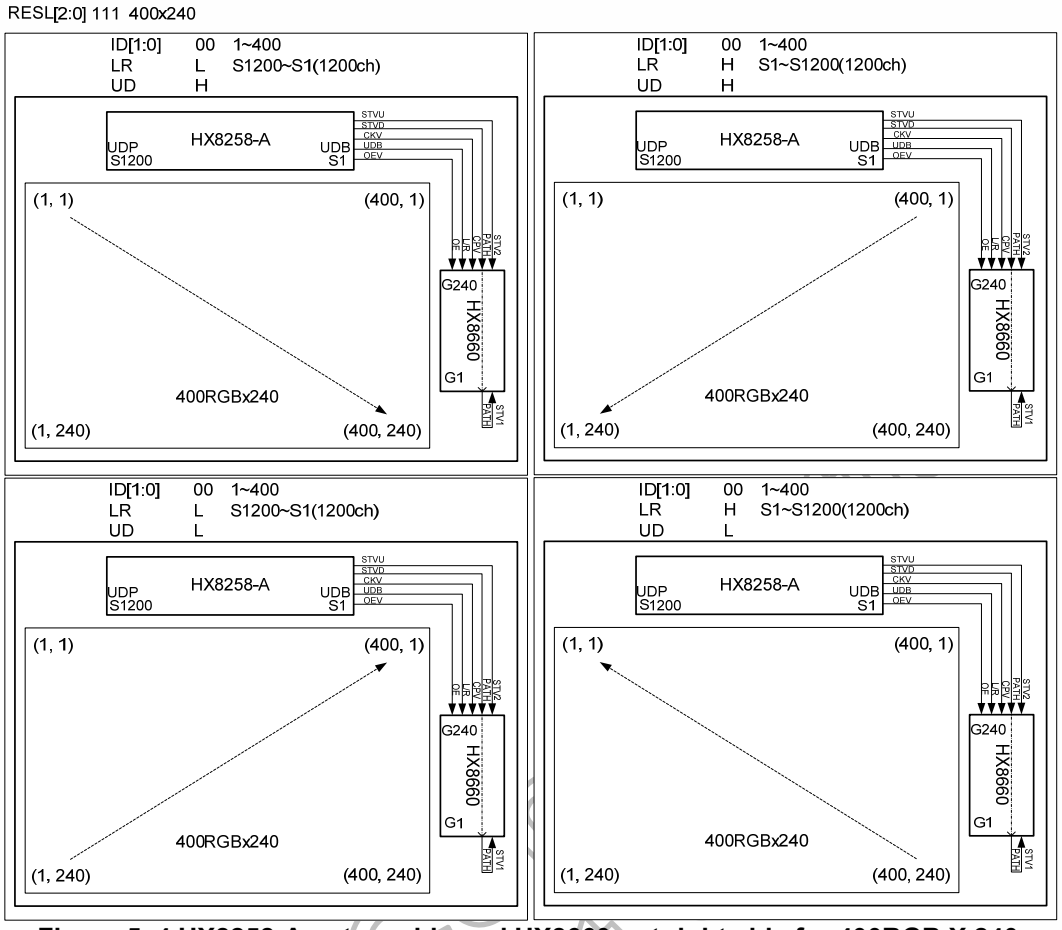


Figure 5. 4 HX8258-A put up side and HX8660 put right side for 400RGB X 240

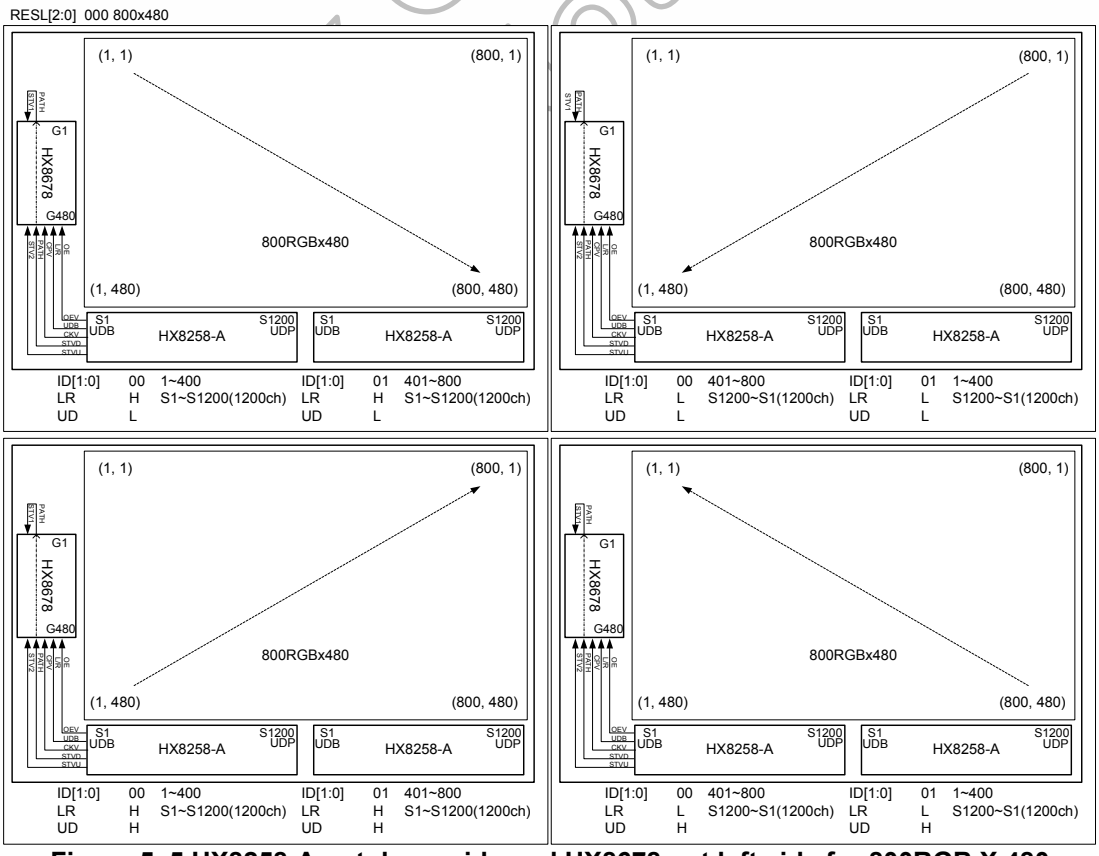


Figure 5. 5 HX8258-A put down side and HX8678 put left side for 800RGB X 480

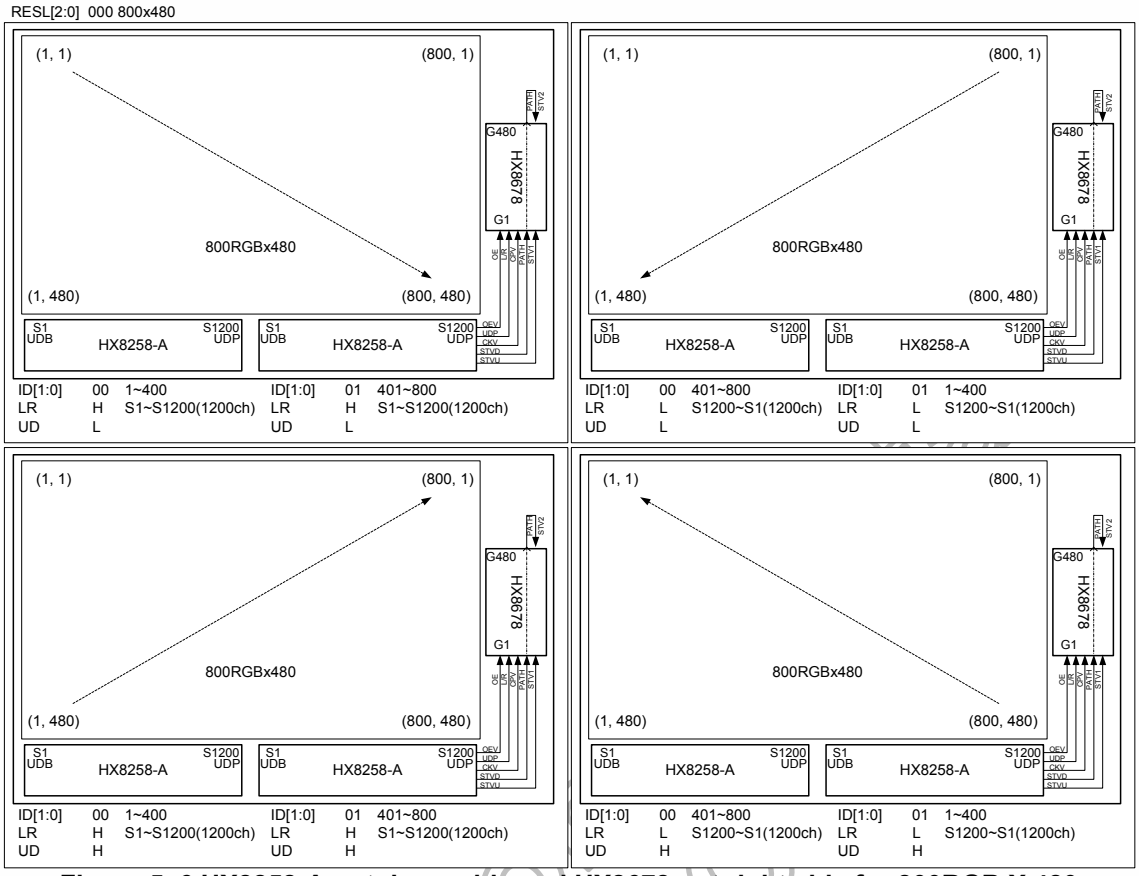


Figure 5. 6 HX8258-A put down side and HX8678 put right side for 800RGB X 480

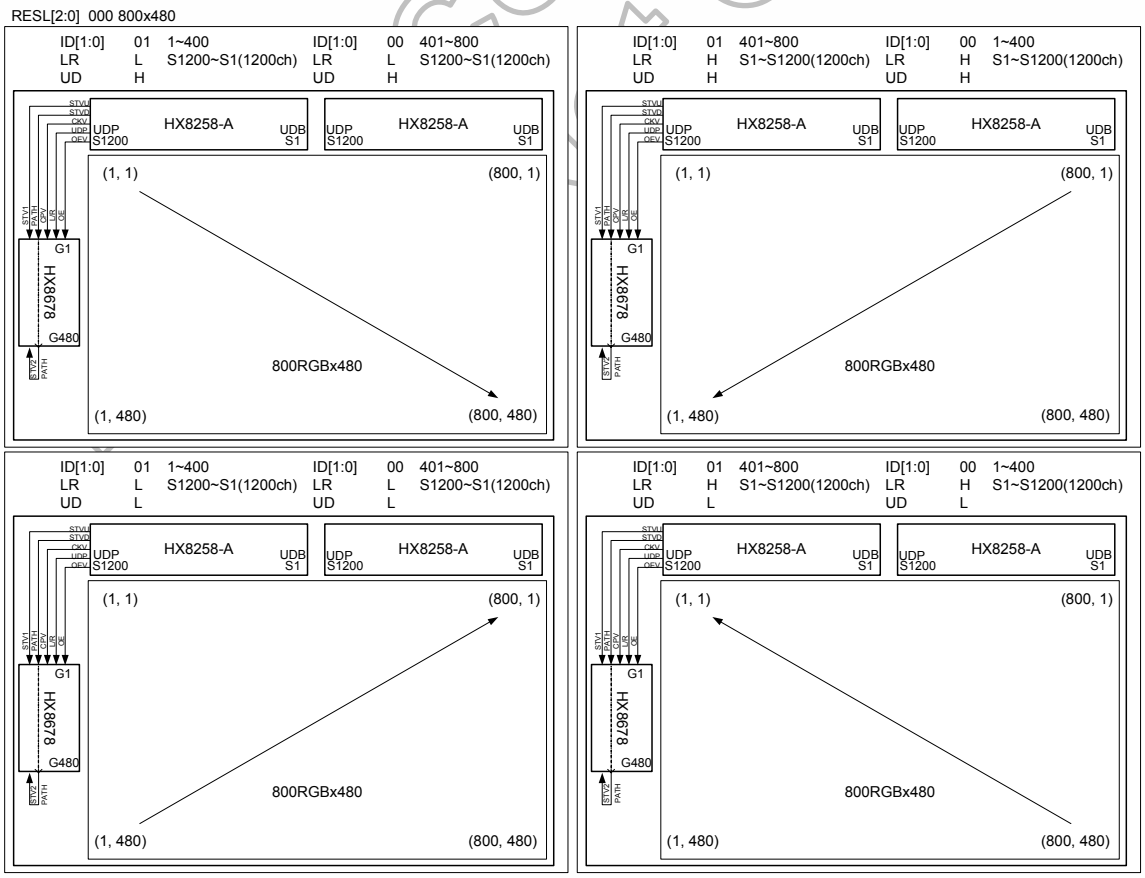


Figure 5. 7 HX8258-A put up side and HX8678 put left side for 800RGB X 480

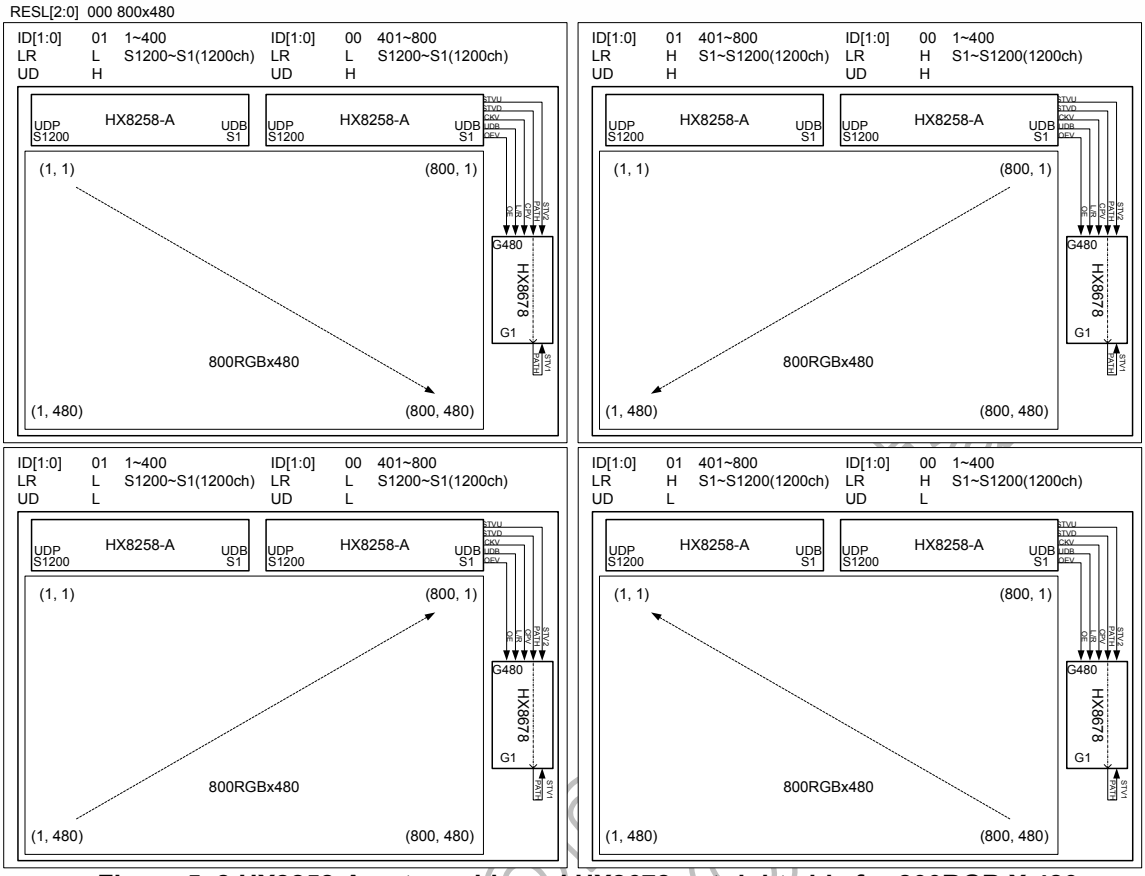


Figure 5. 8 HX8258-A put up side and HX8678 put right side for 800RGB X 480

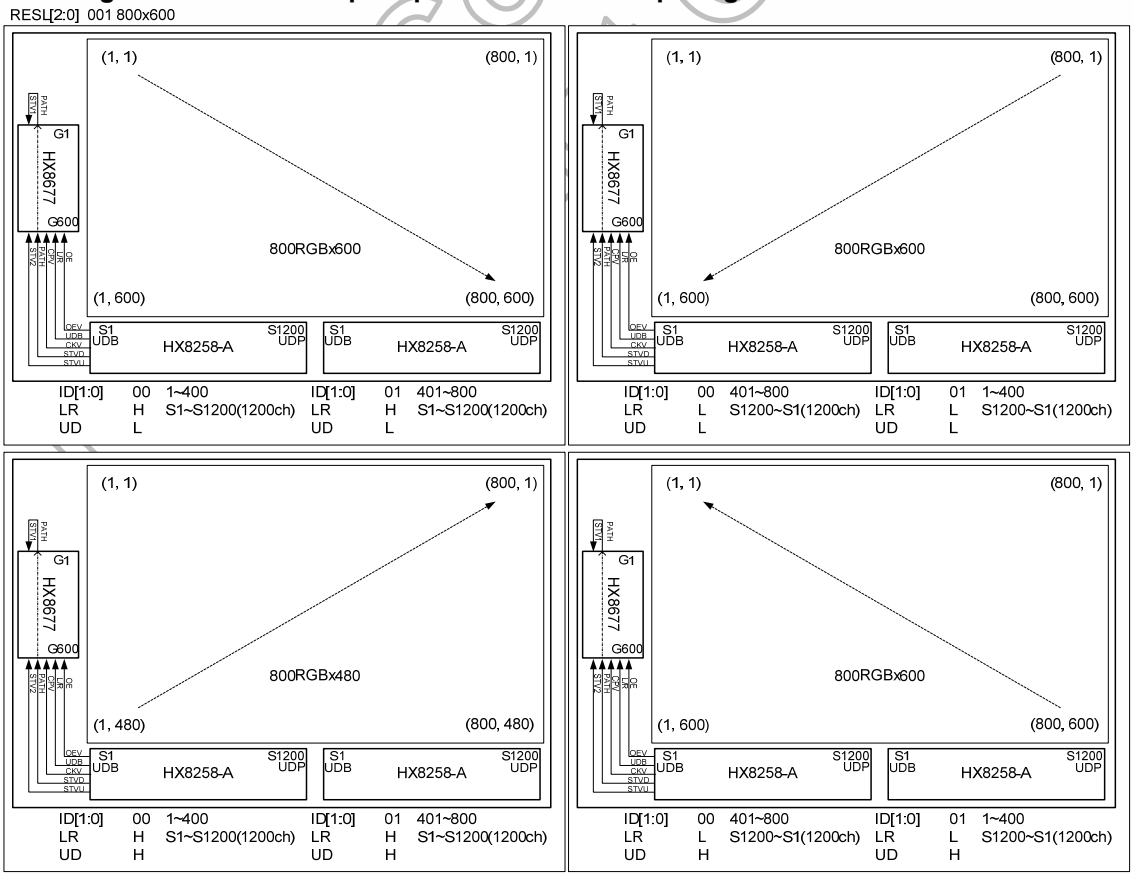


Figure 5. 9 HX8258-A put down side and HX8677 put left side for 800RGB X 600

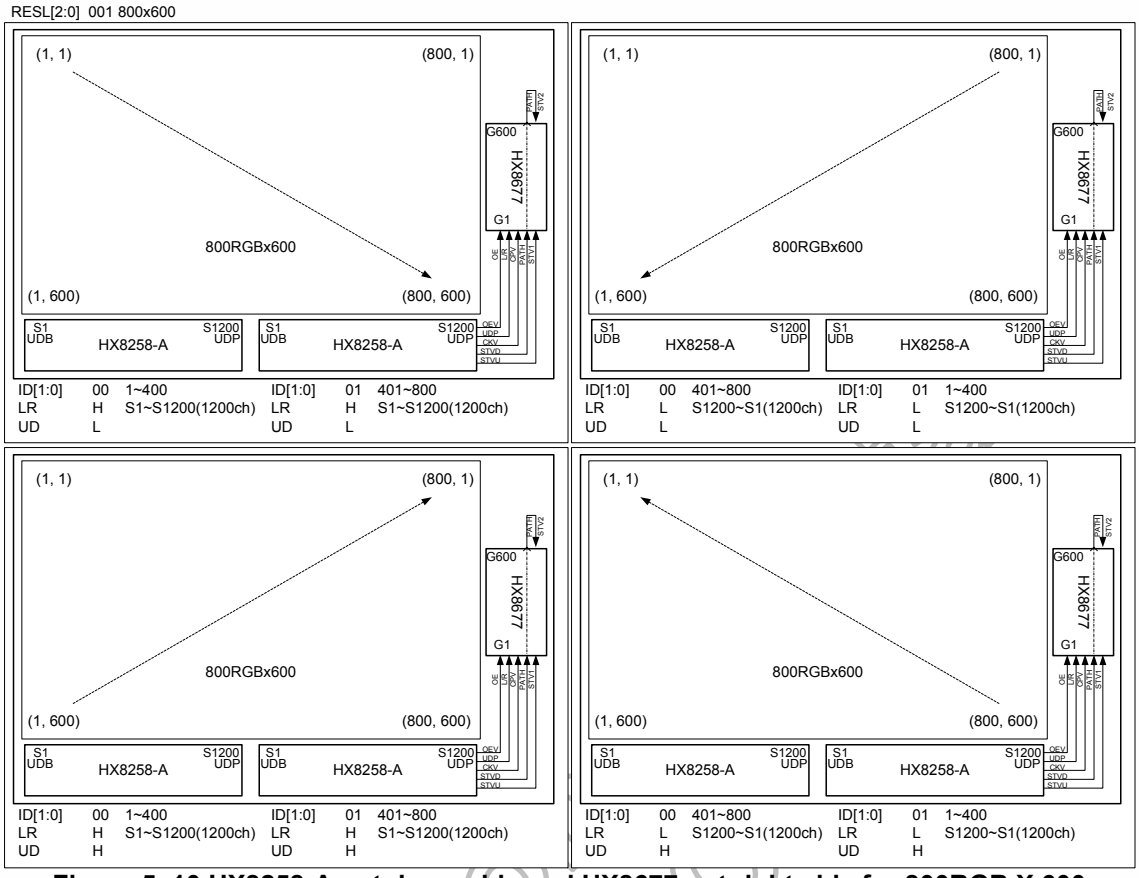


Figure 5. 10 HX8258-A put down side and HX8677 put right side for 800RGB X 600

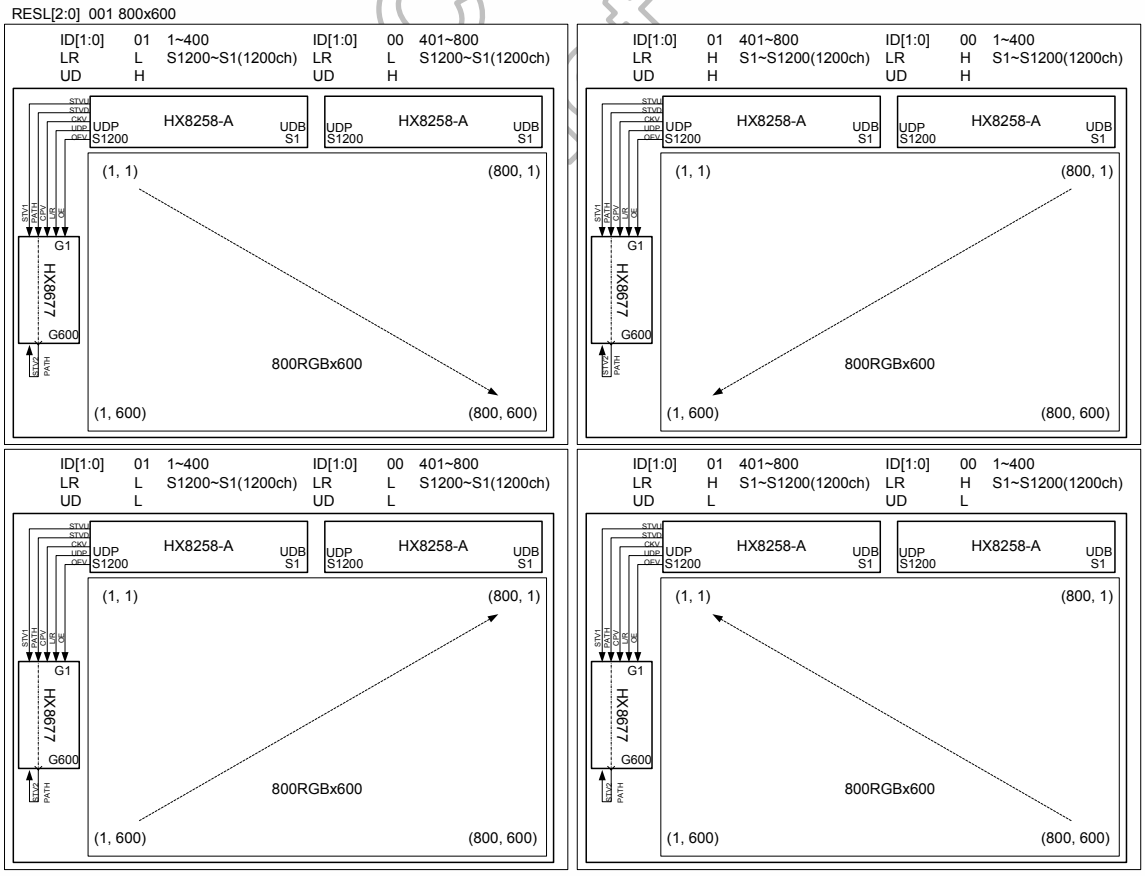


Figure 5. 11 HX8258-A put up side and HX8677 put left side for 800RGB X 600

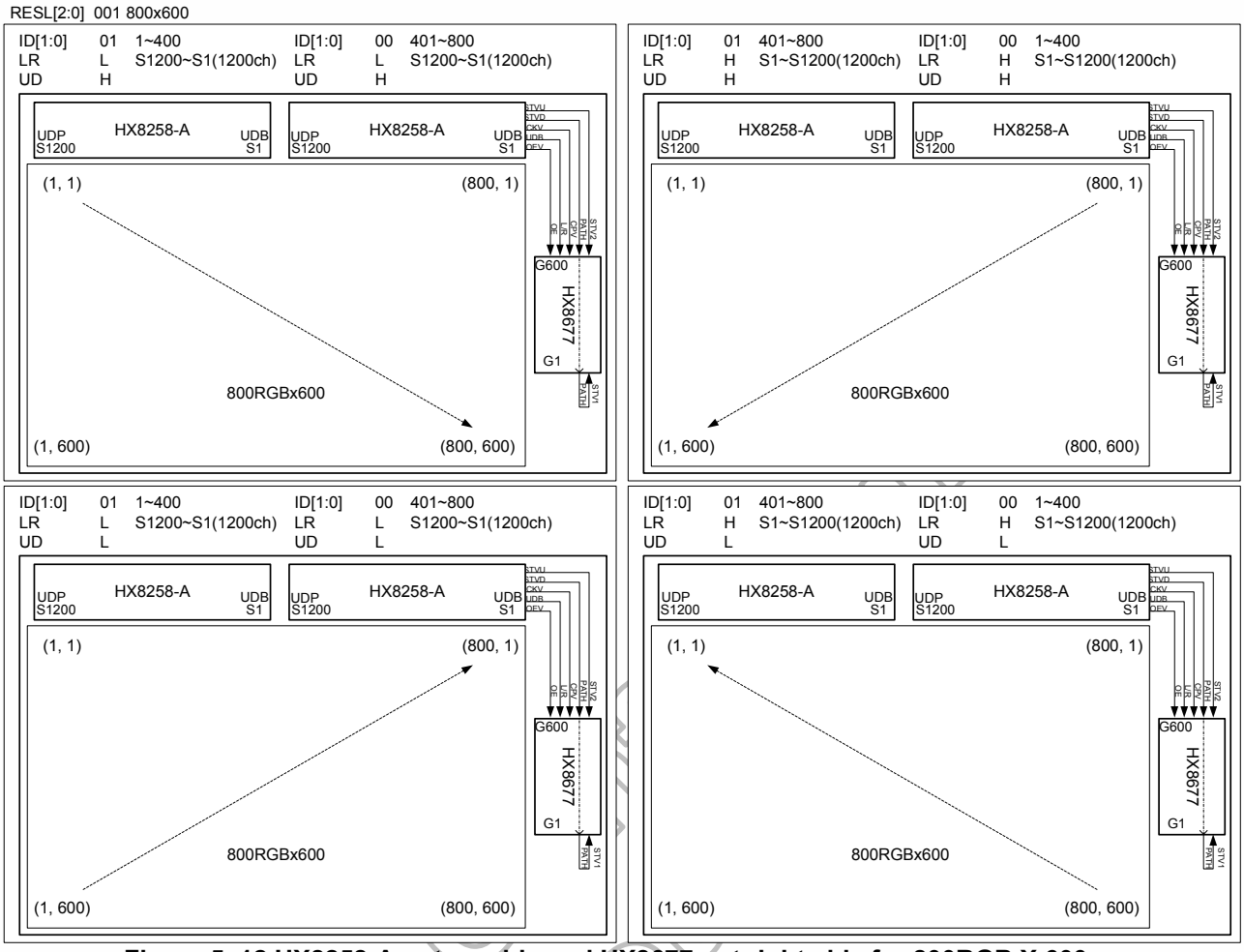


Figure 5. 12 HX8258-A put up side and HX8677 put right side for 800RGB X 600

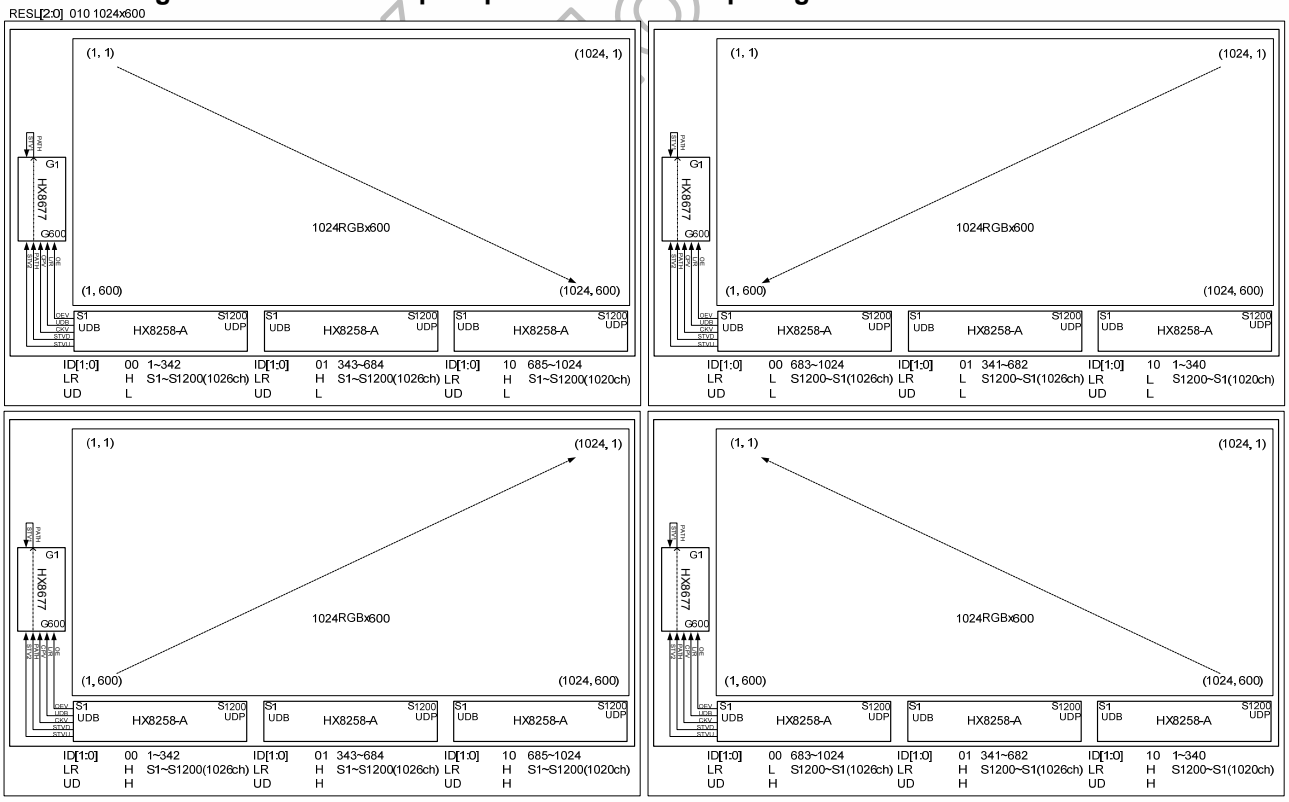


Figure 5. 13 HX8258-A put down side and HX8677 put left side for 1024RGB X 600

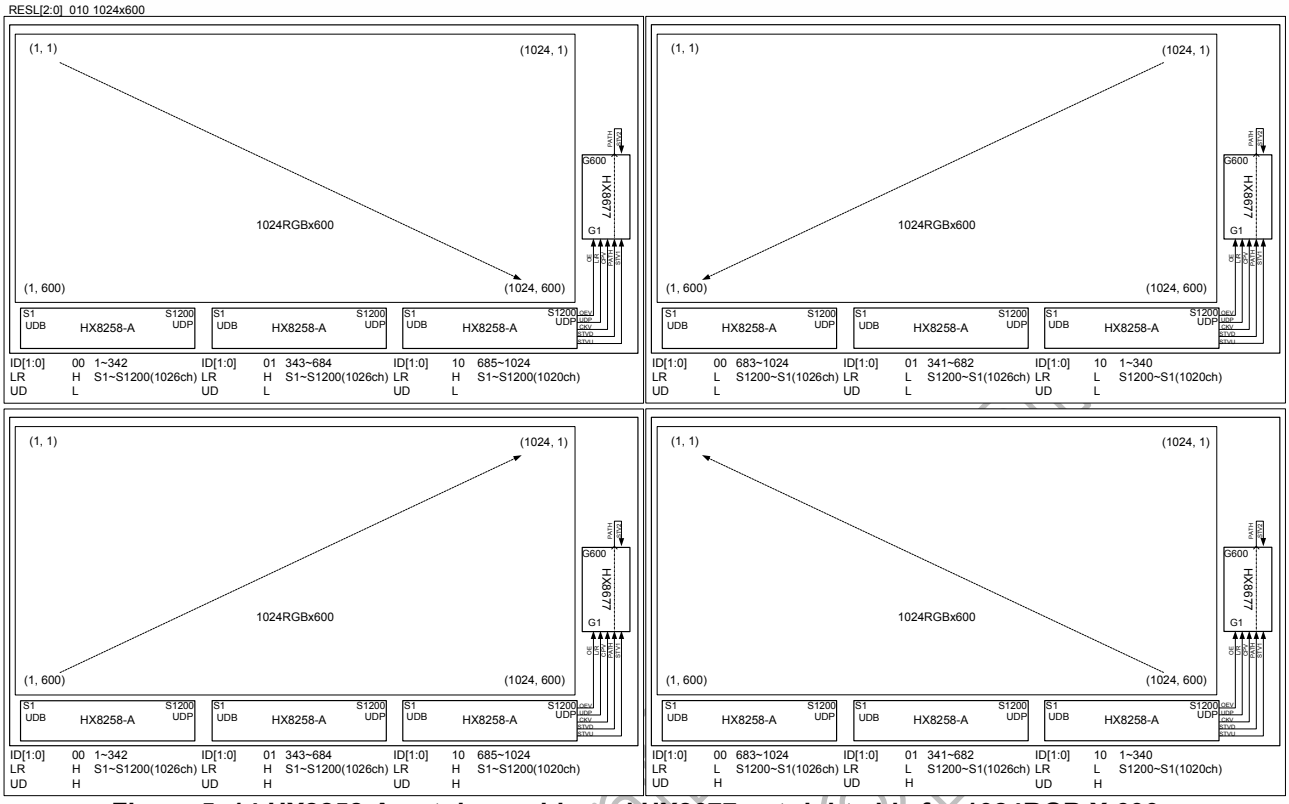


Figure 5. 14 HX8258-A put down side and HX8677 put right side for 1024RGB X 600

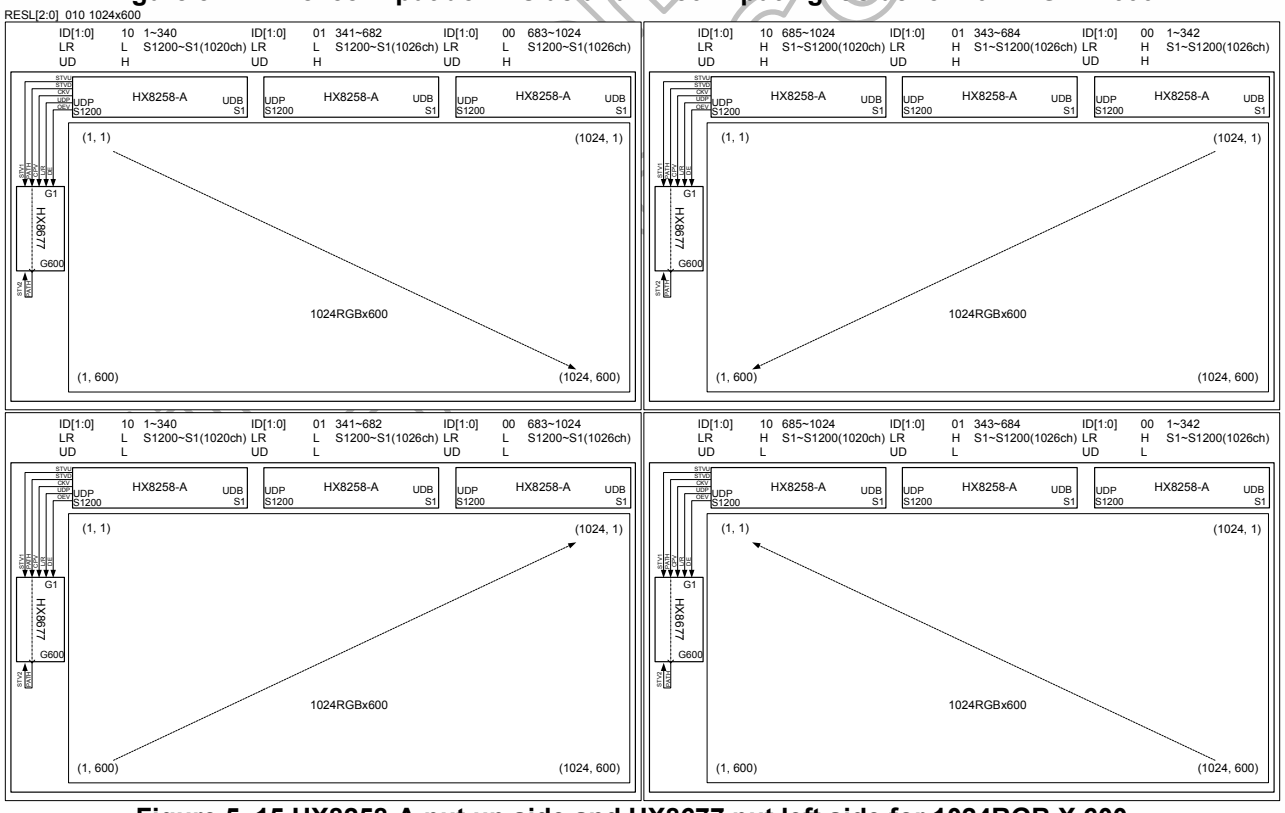


Figure 5. 15 HX8258-A put up side and HX8677 put left side for 1024RGB X 600

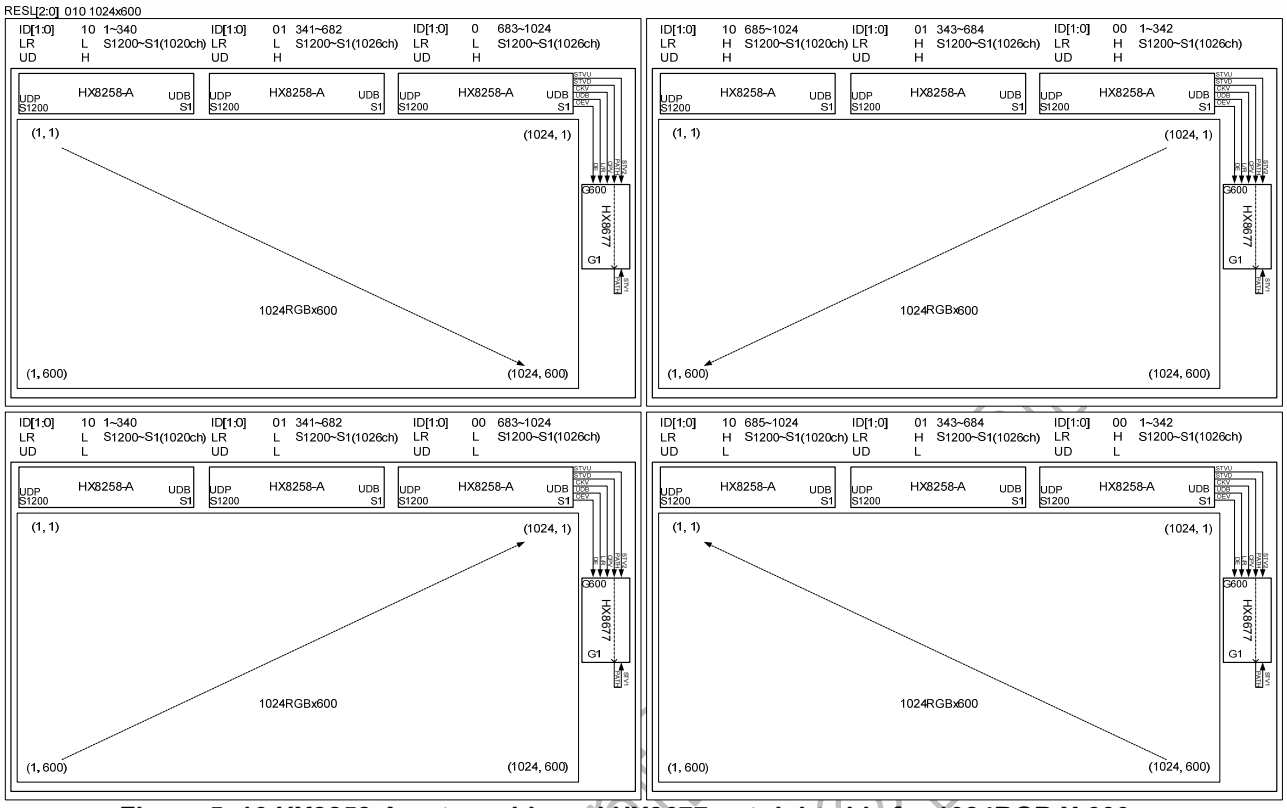


Figure 5. 16 HX8258-A put up side and HX8677 put right side for 1024RGB X 600

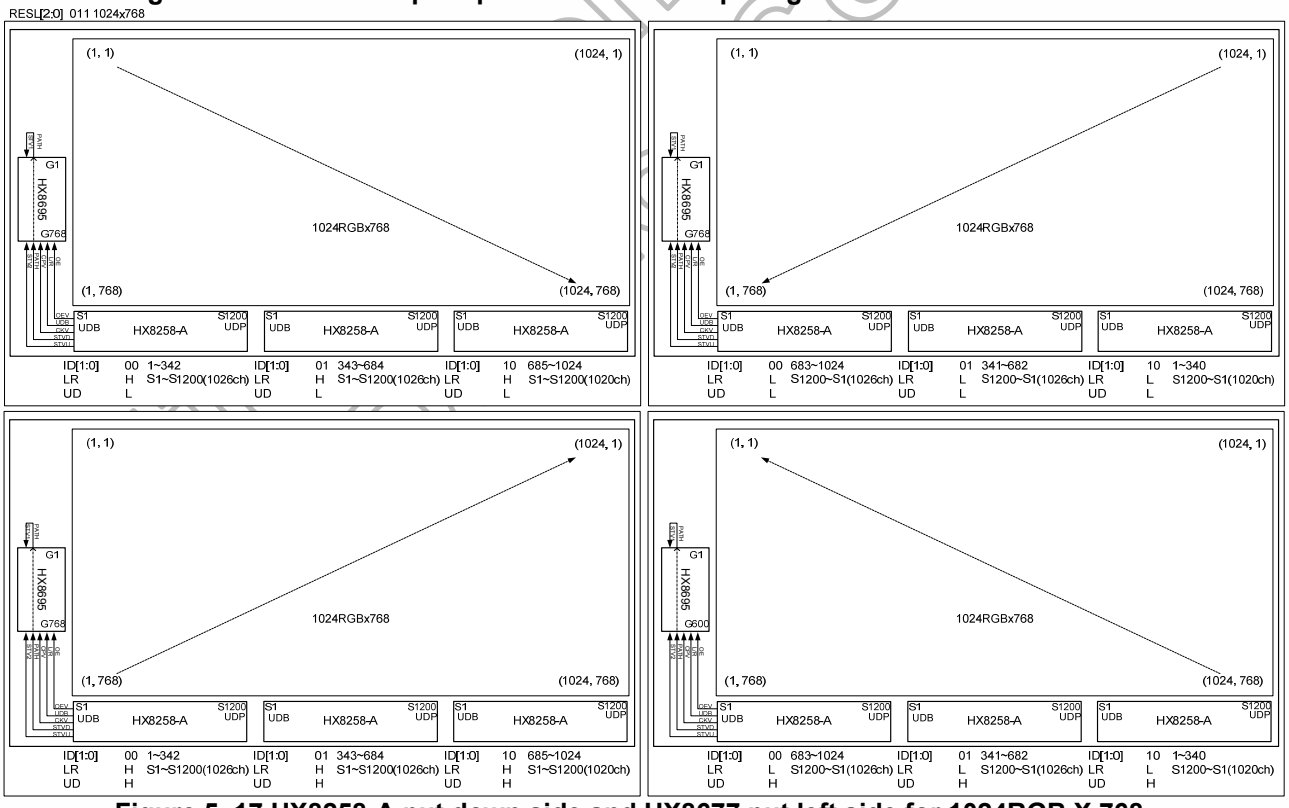


Figure 5. 17 HX8258-A put down side and HX8677 put left side for 1024RGB X 768

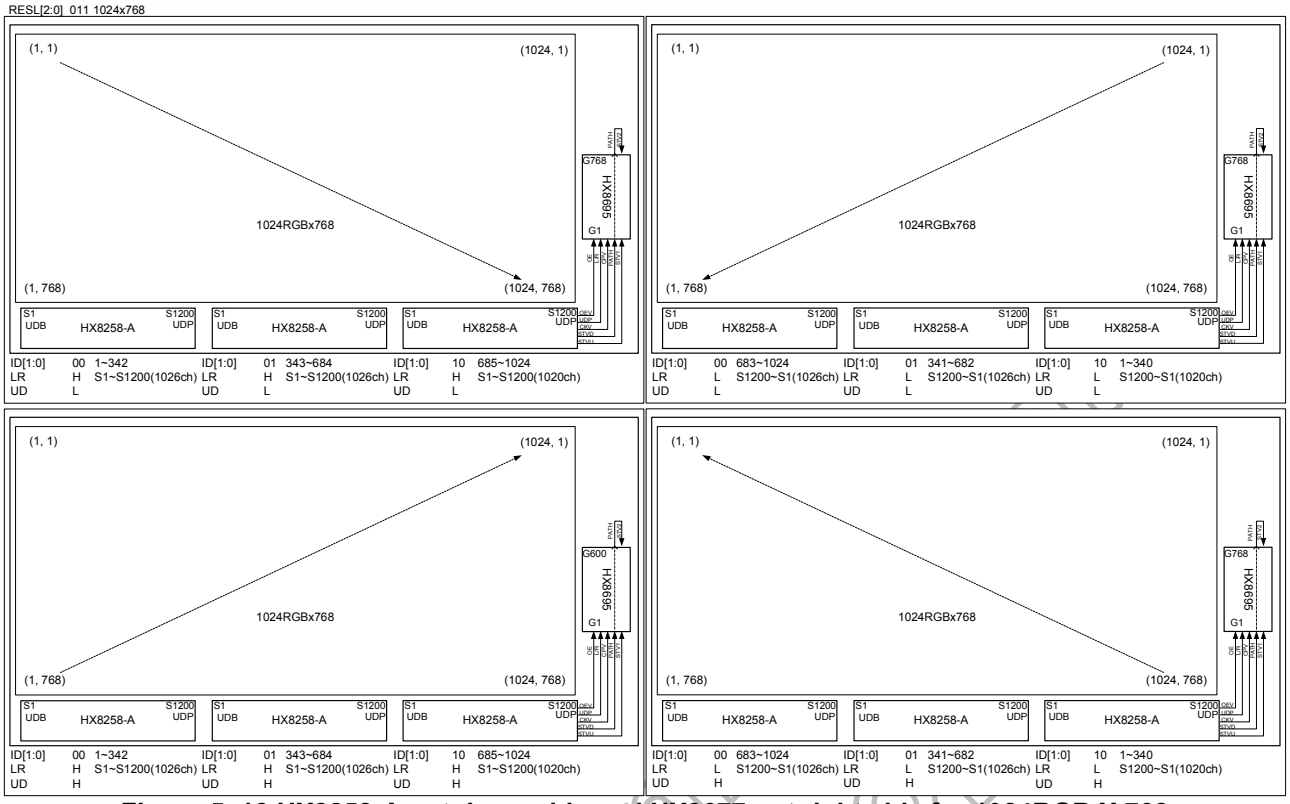


Figure 5. 18 HX8258-A put down side and HX8677 put right side for 1024RGB X 768

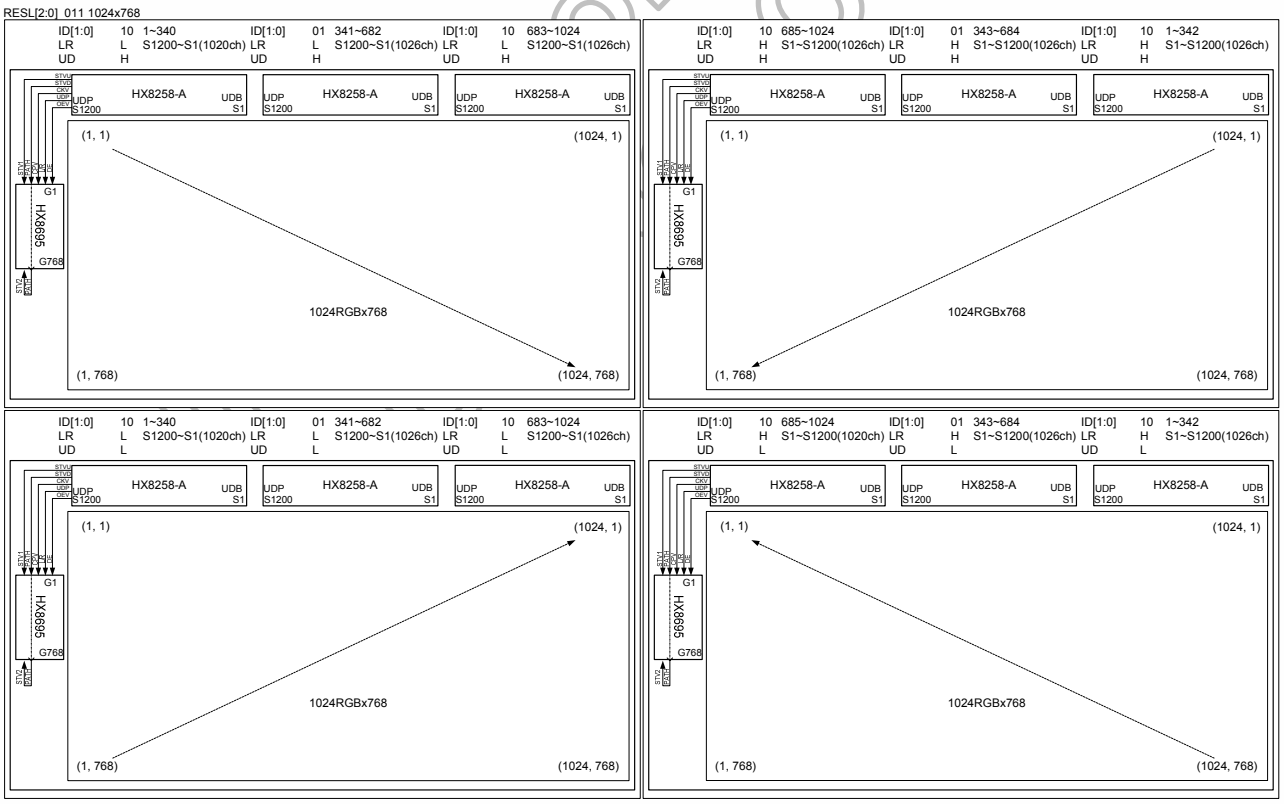


Figure 5. 19 HX8258-A put up side and HX8677 put left side for 1024RGB X 768

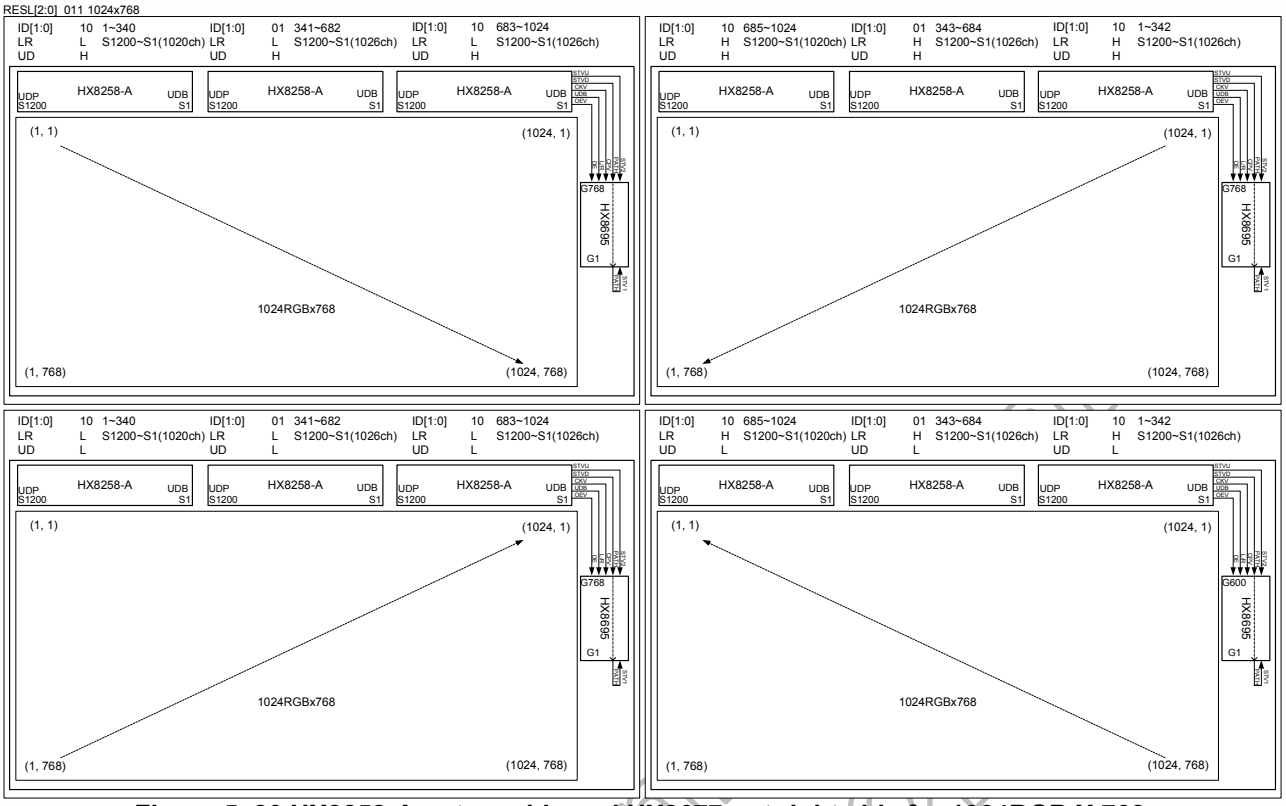


Figure 5. 20 HX8258-A put up side and HX8677 put right side for 1024RGB X 768

HX8258-A has several modes of timing control circuit, according to the setting (ID0 & ID1) and shift direction (LR) of the driver. These modes are decided by ID0, ID1 and LR settings as table 5.1. For example, when resolution is 800RGBx480, LR=H and HX8258-A {ID1, ID0} is set as the 00, it latches the display data from the 1st to the 400th clock at DE active regions. When HX8258-A is set as the second ({ID1, ID0} = 01), it starts latching data from the 401st to the 800th clock at DE active region.

RESL[2:0]	{ID1,ID0}	Sample cycle		Channel number
		LR=H	LR=L	
800X480 WVGA1(LLL)	00	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
	01	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
	10	NA		
	11			
800X600 SVGA(LLH)	00	1 ~ 400	401 ~ 800	1200CH (S1 ~ S1200)
	01	401 ~ 800	1 ~ 400	1200CH (S1 ~ S1200)
	10	NA		
	11			
1024X600 (LHL)	00	1 ~ 342	683 ~ 1024	1026CH (S1 ~ S513/S688 ~ S1200)
	01	343 ~ 684	341 ~ 682	1026CH (S1 ~ S513/S688 ~ S1200)
	10	685 ~ 1024	1 ~ 340	1020CH (S1 ~ S513/S688 ~ S1194)
	11	NA		
1024X768 XGA(LHH)	00	1 ~ 342	683 ~ 1024	1026CH (S1 ~ S513/S688 ~ S1200)
	01	343 ~ 684	341 ~ 682	1026CH (S1 ~ S513/S688 ~ S1200)
	10	685 ~ 1024	1 ~ 340	1020CH (S1 ~ S513/S688 ~ S1194)
	11	NA		
400X240 (HHH)	00	1 ~ 400	1 ~ 400	1200CH (S1 ~ S1200)
	01	NA		
	10			
	11			

Table 5. 2 Several modes of timing control

In HX8258-A, 24-bit data are transferred into HX8258-A each cycle when DE is activated. Meanwhile, if LR="H" (right shift), D07 to D00 is displayed for output channel S3n-2, D17 to D10 are displayed for channel S3n-1, and D27 to D20 are displayed for channel S3n, where n=1, 2, … to 400 sequentially. The relationship between display data and source output is shown in the following figure.
If LR="L" (left shift), D07 to D00, D17 to D10, and D27 to D20 are still displayed for channel S3n-2, S3n-1, and S3n, respectively, but n=400 to 1 sequentially.

Driver latch data are according to LR pin setting.

Input data format	24-bit RGB, 3 dots (sub-pixels) per clock
Input data width	24 bits with Dx7 is MSB and Dx0 is LSB, x=0,1,2

The following diagram shows the relationship of input data and output source channel for HX8258-A in different configurations (1024 RGB resolution).

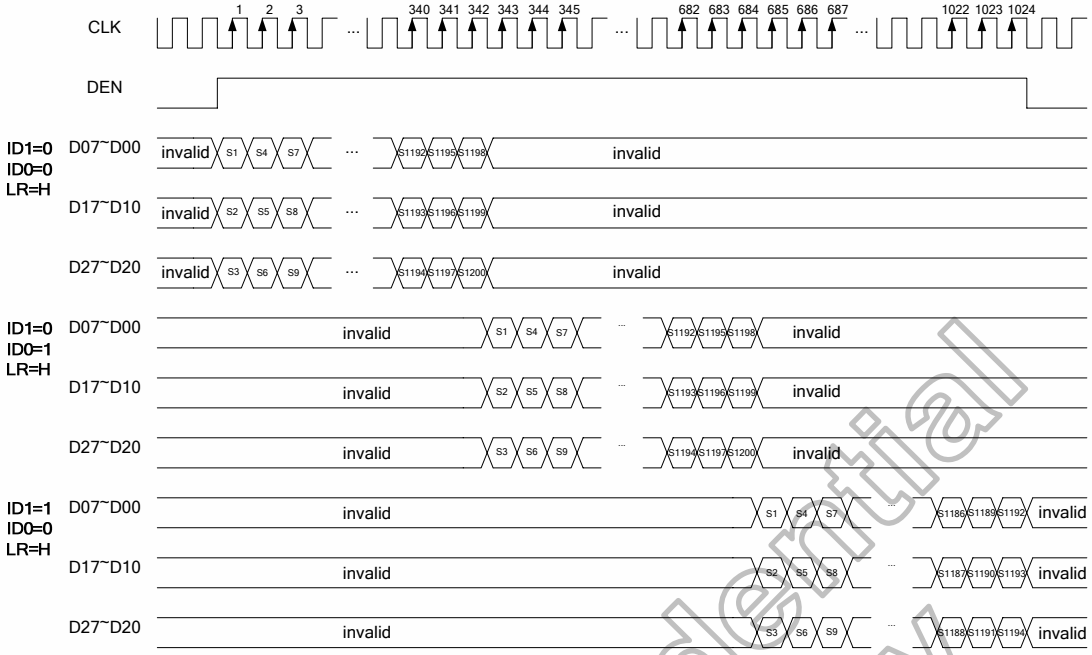
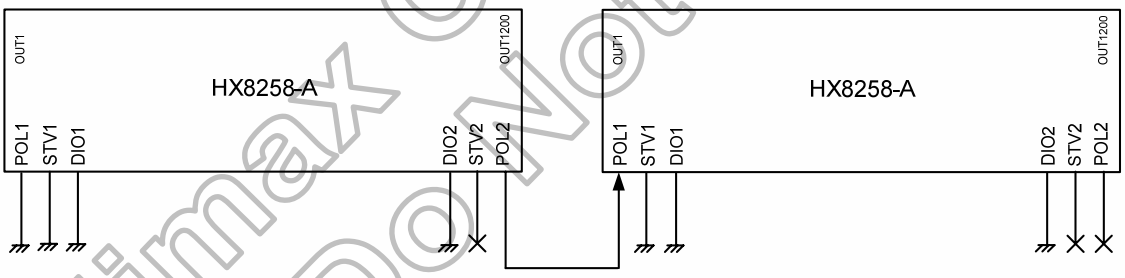


Figure 5. 21 Input output relationship when TCON enable (TEN=H)

5.3 Connect circuits for cascade mode

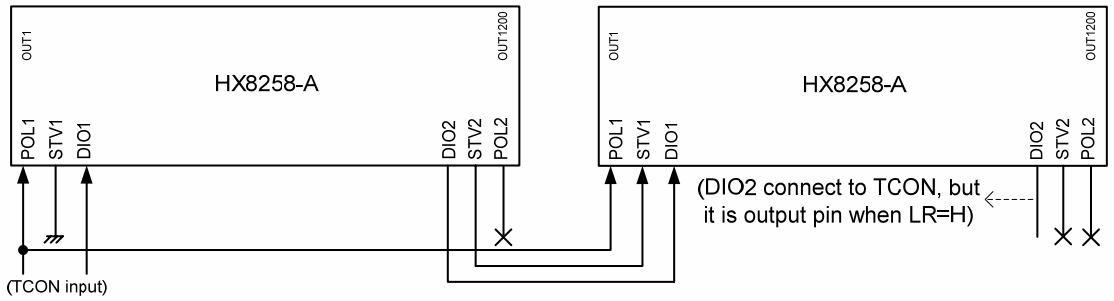
HX8258-A supports 800x480 and 800x600 resolutions by cascade 2 chips, and 1024x600 and 1024x768 resolutions by cascade 3 chips. In cascade mode, user need to set ID[1:0] pins to define chip's ID, detail connect circuits are shown in Figure 5.22 ~5.25. The connect circuits depend on amount of chips and TEN.



TEN = H
RESL[2:0] = 000/001
ID[1:0] = 00
LR = H/L

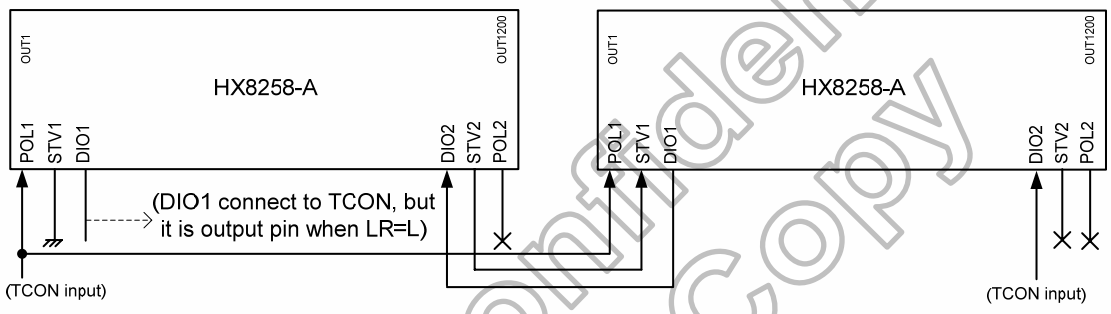
TEN = H
RESL[2:0] = 000/001
ID[1:0] = 01
LR = H/L

Figure 5. 22 the connect circuit for cascading two HX8258-A chips when TEN=H



TEN = L
RESL[2:0] = 000/001
ID[1:0] = 00
LR = H

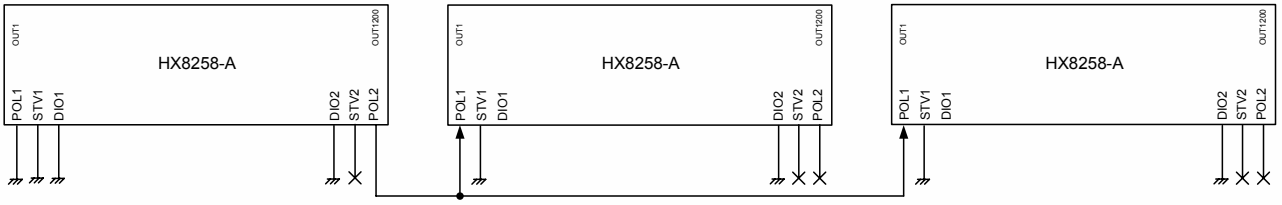
TEN = L
RESL[2:0] = 000/001
ID[1:0] = 01
LR = H



TEN = L
RESL[2:0] = 000/001
ID[1:0] = 00
LR = L

TEN = L
RESL[2:0] = 000/001
ID[1:0] = 01
LR = L

Figure 5. 23 the connect circuit for cascading two HX8258-A chips when TEN=L

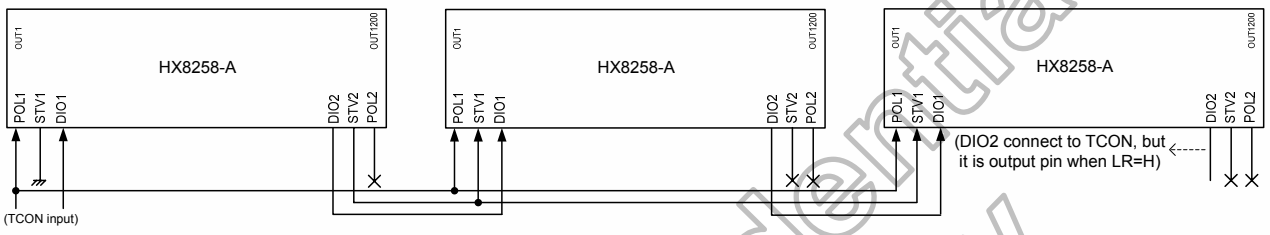


TEN = H
RESL[2:0] = 010/011
ID[1:0] = 00
LR = H/L

TEN = H
RESL[2:0] = 010/011
ID[1:0] = 01
LR = H/L

TEN = H
RESL[2:0] = 010/011
ID[1:0] = 10
LR = H/L

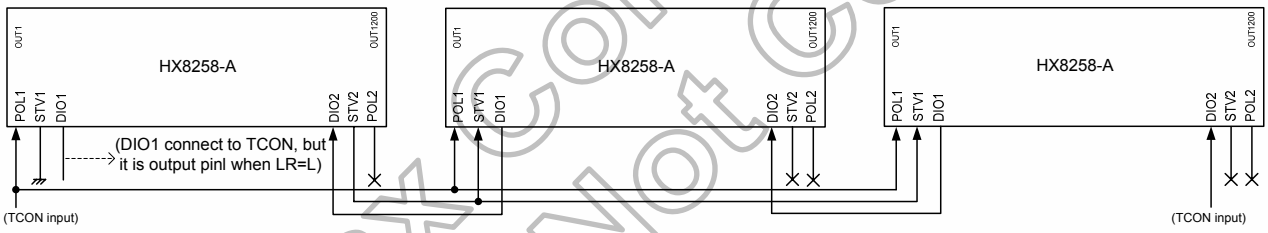
Figure 5. 24 the connect circuit for cascading three HX8258-A chips when TEN=H



TEN = L
RESL[2:0] = 010/011
ID[1:0] = 00
LR = H

TEN = L
RESL[2:0] = 010/011
ID[1:0] = 01
LR = H

TEN = L
RESL[2:0] = 010/011
ID[1:0] = 10
LR = H



TEN = L
RESL[2:0] = 010/011
ID[1:0] = 00
LR = L

TEN = L
RESL[2:0] = 010/011
ID[1:0] = 01
LR = L

TEN = L
RESL[2:0] = 010/011
ID[1:0] = 10
LR = L

Figure 5. 25 the connect circuit for cascading three HX8258-A chips when TEN=L

5.4 Relationship between gamma correction and output voltage

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V10 gamma correction reference voltage inputs.

Gamma correction characteristic curve:

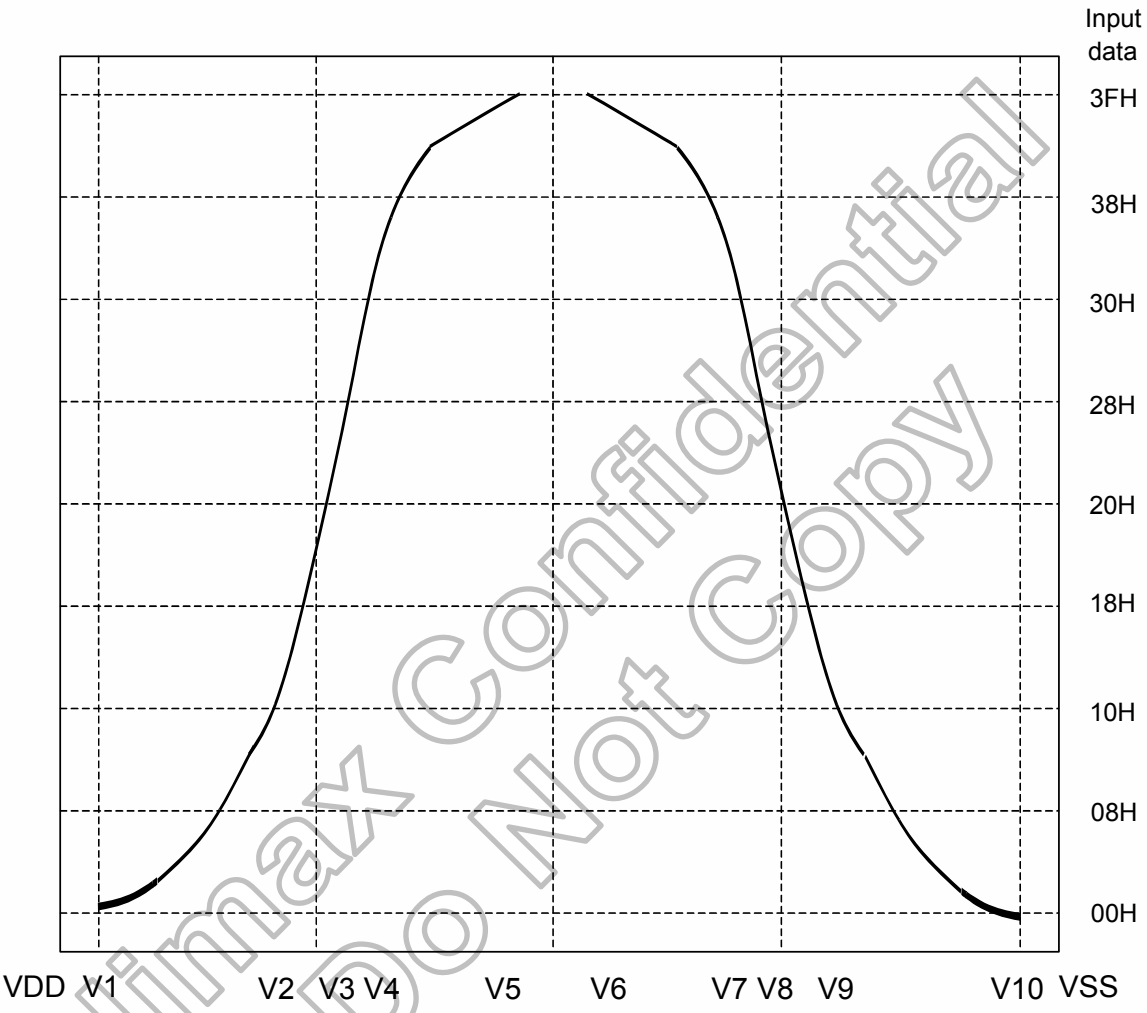


Figure 5. 26 Gamma correction characteristic curve

Gamma correction resistor ratio: (1 unit = 125ohm)

V1, V10 →

Name	Resistor	Name	Resistor
R0	6.4	R32	0.8
R1	6	R33	0.8
R2	5.6	R34	0.8
R3	5.2	R35	0.8
R4	4.8	R36	0.8
R5	4.4	R37	0.8
R6	4.4	R38	0.8
R7	4	R39	0.8
R8	4	R40	0.8
R9	3.2	R41	0.8
R10	3.2	R42	0.8
R11	2.8	R43	0.8
R12	2.8	R44	0.8
R13	2.8	R45	0.8
R14	2.4	R46	0.8
R15	2.4	R47	0.8
R16	2.4	R48	0.8
R17	2	R49	0.8
R18	2	R50	0.8
R19	2	R51	0.8
R20	1.6	R52	0.8
R21	1.6	R53	1.2
R22	1.6	R54	1.2
R23	1.2	R55	1.2
R24	1.2	R56	1.6
R25	1.2	R57	1.6
R26	1.2	R58	2
R27	0.8	R59	2
R28	0.8	R60	2.4
R29	0.8	R61	4
R30	0.8	R62	6.4
R31	0.8		

V2, V9 →

← V4, V7

← V5, V6

V3, V8 →

Output Voltages vs. Source Input Data when VSET=H:
Please input V1~V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V2 + (V1 – V2)X 58 / 64.4	V10 + (V9 – V10)X 6.4 / 64.4
02H	V2 + (V1 – V2)X 52 / 64.4	V10 + (V9 – V10)X 12.4 / 64.4
03H	V2 + (V1 – V2)X 46.4 / 64.4	V10 + (V9 – V10)X 18 / 64.4
04H	V2 + (V1 – V2)X 41.2 / 64.4	V10 + (V9 – V10)X 23.2 / 64.4
05H	V2 + (V1 – V2)X 36.4 / 64.4	V10 + (V9 – V10)X 28 / 64.4
06H	V2 + (V1 – V2)X 32 / 64.4	V10 + (V9 – V10)X 32.4 / 64.4
07H	V2 + (V1 – V2)X 27.6 / 64.4	V10 + (V9 – V10)X 36.8 / 64.4
08H	V2 + (V1 – V2)X 23.6 / 64.4	V10 + (V9 – V10)X 40.8 / 64.4
09H	V2 + (V1 – V2)X 19.6 / 64.4	V10 + (V9 – V10)X 44.8 / 64.4
0AH	V2 + (V1 – V2)X 16.4 / 64.4	V10 + (V9 – V10)X 48 / 64.4
0BH	V2 + (V1 – V2)X 13.2 / 64.4	V10 + (V9 – V10)X 51.2 / 64.4
0CH	V2 + (V1 – V2)X 10.4 / 64.4	V10 + (V9 – V10)X 54 / 64.4
0DH	V2 + (V1 – V2)X 7.6 / 64.4	V10 + (V9 – V10)X 56.8 / 64.4
0EH	V2 + (V1 – V2)X 4.8 / 64.4	V10 + (V9 – V10)X 59.6 / 64.4
0FH	V2 + (V1 – V2)X 2.4 / 64.4	V10 + (V9 – V10)X 62 / 64.4
10H	V2	V9
11H	V3 + (V2 – V3) X 19.6 / 22	V9 + (V8 – V9)X 2.4 / 22
12H	V3 + (V2 – V3) X 17.6 / 22	V9 + (V8 – V9)X 4.4 / 22
13H	V3 + (V2 – V3) X 15.6 / 22	V9 + (V8 – V9)X 6.4 / 22
14H	V3 + (V2 – V3) X 13.6 / 22	V9 + (V8 – V9)X 8.4 / 22
15H	V3 + (V2 – V3) X 12 / 22	V9 + (V8 – V9)X 10 / 22
16H	V3 + (V2 – V3) X 10.4 / 22	V9 + (V8 – V9)X 11.6 / 22
17H	V3 + (V2 – V3) X 8.8 / 22	V9 + (V8 – V9)X 13.2 / 22
18H	V3 + (V2 – V3) X 7.6 / 22	V9 + (V8 – V9)X 14.4 / 22
19H	V3 + (V2 – V3) X 6.4 / 22	V9 + (V8 – V9)X 15.6 / 22
1AH	V3 + (V2 – V3) X 5.2 / 22	V9 + (V8 – V9)X 16.8 / 22
1BH	V3 + (V2 – V3) X 4 / 22	V9 + (V8 – V9)X 18 / 22
1CH	V3 + (V2 – V3) X 3.2 / 22	V9 + (V8 – V9)X 18.8 / 22
1DH	V3 + (V2 – V3) X 2.4 / 22	V9 + (V8 – V9)X 19.6 / 22
1EH	V3 + (V2 – V3) X 1.6 / 22	V9 + (V8 – V9)X 20.4 / 22
1FH	V3 + (V2 – V3) X 0.8 / 22	V9 + (V8 – V9)X 21.2 / 22

Output Voltages vs. Source Input Data when VSET=H (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V3	V8
21H	V4 + (V3 – V4) X 12 / 12.8	V8 + (V7 – V8) X 0.8 / 12.8
22H	V4 + (V3 – V4) X 11.2 / 12.8	V8 + (V7 – V8) X 1.6 / 12.8
23H	V4 + (V3 – V4) X 10.4 / 12.8	V8 + (V7 – V8) X 2.4 / 12.8
24H	V4 + (V3 – V4) X 9.6 / 12.8	V8 + (V7 – V8) X 3.2 / 12.8
25H	V4 + (V3 – V4) X 8.8 / 12.8	V8 + (V7 – V8) X 4 / 12.8
26H	V4 + (V3 – V4) X 8 / 12.8	V8 + (V7 – V8) X 4.8 / 12.8
27H	V4 + (V3 – V4) X 7.2 / 12.8	V8 + (V7 – V8) X 5.6 / 12.8
28H	V4 + (V3 – V4) X 6.4 / 12.8	V8 + (V7 – V8) X 6.4 / 12.8
29H	V4 + (V3 – V4) X 5.6 / 12.8	V8 + (V7 – V8) X 7.2 / 12.8
2AH	V4 + (V3 – V4) X 4.8 / 12.8	V8 + (V7 – V8) X 8 / 12.8
2BH	V4 + (V3 – V4) X 4 / 12.8	V8 + (V7 – V8) X 8.8 / 12.8
2CH	V4 + (V3 – V4) X 3.2 / 12.8	V8 + (V7 – V8) X 9.6 / 12.8
2DH	V4 + (V3 – V4) X 2.4 / 12.8	V8 + (V7 – V8) X 10.4 / 12.8
2EH	V4 + (V3 – V4) X 1.6 / 12.8	V8 + (V7 – V8) X 11.2 / 12.8
2FH	V4 + (V3 – V4) X 0.8 / 12.8	V8 + (V7 – V8) X 12 / 12.8
30H	V4	V7
31H	V5 + (V4 – V5) X 26.8 / 27.6	V7 + (V6 – V7) X 0.8 / 27.6
32H	V5 + (V4 – V5) X 26 / 27.6	V7 + (V6 – V7) X 1.6 / 27.6
33H	V5 + (V4 – V5) X 25.2 / 27.6	V7 + (V6 – V7) X 2.4 / 27.6
34H	V5 + (V4 – V5) X 24.4 / 27.6	V7 + (V6 – V7) X 3.2 / 27.6
35H	V5 + (V4 – V5) X 23.6 / 27.6	V7 + (V6 – V7) X 4 / 27.6
36H	V5 + (V4 – V5) X 22.4 / 27.6	V7 + (V6 – V7) X 5.2 / 27.6
37H	V5 + (V4 – V5) X 21.2 / 27.6	V7 + (V6 – V7) X 6.4 / 27.6
38H	V5 + (V4 – V5) X 20 / 27.6	V7 + (V6 – V7) X 7.6 / 27.6
39H	V5 + (V4 – V5) X 18.4 / 27.6	V7 + (V6 – V7) X 9.2 / 27.6
3AH	V5 + (V4 – V5) X 16.8 / 27.6	V7 + (V6 – V7) X 10.8 / 27.6
3BH	V5 + (V4 – V5) X 14.8 / 27.6	V7 + (V6 – V7) X 12.8 / 27.6
3CH	V5 + (V4 – V5) X 12.8 / 27.6	V7 + (V6 – V7) X 14.8 / 27.6
3DH	V5 + (V4 – V5) X 10.4 / 27.6	V7 + (V6 – V7) X 17.2 / 27.6
3EH	V5 + (V4 – V5) X 6.4 / 27.6	V7 + (V6 – V7) X 21.2 / 27.6
3FH	V5	V6

Output Voltages vs. Source Input Data when VSET=L:
Please input V1, V5 and V6, V10 Gamma voltage.

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V10
01H	V5 + (V1 – V5)X 120.4 / 126.8	V10 + (V6 – V10)X 6.4 / 126.8
02H	V5 + (V1 – V5)X 114.4 / 126.8	V10 + (V6 – V10)X 12.4 / 126.8
03H	V5 + (V1 – V5)X 108.8 / 126.8	V10 + (V6 – V10)X 18 / 126.8
04H	V5 + (V1 – V5)X 103.6 / 126.8	V10 + (V6 – V10)X 23.2 / 126.8
05H	V5 + (V1 – V5)X 98.8 / 126.8	V10 + (V6 – V10)X 28 / 126.8
06H	V5 + (V1 – V5)X 94.4 / 126.8	V10 + (V6 – V10)X 32.4 / 126.8
07H	V5 + (V1 – V5)X 90 / 126.8	V10 + (V6 – V10)X 36.8 / 126.8
08H	V5 + (V1 – V5)X 86 / 126.8	V10 + (V6 – V10)X 40.8 / 126.8
09H	V5 + (V1 – V5)X 82 / 126.8	V10 + (V6 – V10)X 44.8 / 126.8
0AH	V5 + (V1 – V5)X 78.8 / 126.8	V10 + (V6 – V10)X 48 / 126.8
0BH	V5 + (V1 – V5)X 75.6 / 126.8	V10 + (V6 – V10)X 51.2 / 126.8
0CH	V5 + (V1 – V5)X 72.8 / 126.8	V10 + (V6 – V10)X 54 / 126.8
0DH	V5 + (V1 – V5)X 70 / 126.8	V10 + (V6 – V10)X 56.8 / 126.8
0EH	V5 + (V1 – V5)X 67.2 / 126.8	V10 + (V6 – V10)X 59.6 / 126.8
0FH	V5 + (V1 – V5)X 64.8 / 126.8	V10 + (V6 – V10)X 62 / 126.8
10H	V5 + (V1 – V5)X 62.4 / 126.8	V10 + (V6 – V10)X 64.4 / 126.8
11H	V5 + (V1 – V5)X 60 / 126.8	V10 + (V6 – V10)X 66.8 / 126.8
12H	V5 + (V1 – V5)X 58 / 126.8	V10 + (V6 – V10)X 68.8 / 126.8
13H	V5 + (V1 – V5)X 56 / 126.8	V10 + (V6 – V10)X 70.8 / 126.8
14H	V5 + (V1 – V5)X 54 / 126.8	V10 + (V6 – V10)X 72.8 / 126.8
15H	V5 + (V1 – V5)X 52.4 / 126.8	V10 + (V6 – V10)X 74.4 / 126.8
16H	V5 + (V1 – V5)X 50.8 / 126.8	V10 + (V6 – V10)X 76 / 126.8
17H	V5 + (V1 – V5)X 49.2 / 126.8	V10 + (V6 – V10)X 77.6 / 126.8
18H	V5 + (V1 – V5)X 48 / 126.8	V10 + (V6 – V10)X 78.8 / 126.8
19H	V5 + (V1 – V5)X 46.8 / 126.8	V10 + (V6 – V10)X 80 / 126.8
1AH	V5 + (V1 – V5)X 45.6 / 126.8	V10 + (V6 – V10)X 81.2 / 126.8
1BH	V5 + (V1 – V5)X 44.4 / 126.8	V10 + (V6 – V10)X 82.4 / 126.8
1CH	V5 + (V1 – V5)X 43.6 / 126.8	V10 + (V6 – V10)X 83.2 / 126.8
1DH	V5 + (V1 – V5)X 42.8 / 126.8	V10 + (V6 – V10)X 84 / 126.8
1EH	V5 + (V1 – V5)X 42 / 126.8	V10 + (V6 – V10)X 84.8 / 126.8
1FH	V5 + (V1 – V5)X 41.2 / 126.8	V10 + (V6 – V10)X 85.6 / 126.8

Output Voltages vs. Source Input Data when VSET=L (continued):

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V5 + (V1 – V5)X 40.4 / 126.8	V10 + (V6 – V10)X 86.4 / 126.8
21H	V5 + (V1 – V5)X 39.6 / 126.8	V10 + (V6 – V10)X 87.2 / 126.8
22H	V5 + (V1 – V5)X 38.8 / 126.8	V10 + (V6 – V10)X 88 / 126.8
23H	V5 + (V1 – V5)X 38 / 126.8	V10 + (V6 – V10)X 88.8 / 126.8
24H	V5 + (V1 – V5)X 37.2 / 126.8	V10 + (V6 – V10)X 89.6 / 126.8
25H	V5 + (V1 – V5)X 36.4 / 126.8	V10 + (V6 – V10)X 90.4 / 126.8
26H	V5 + (V1 – V5)X 35.6 / 126.8	V10 + (V6 – V10)X 91.2 / 126.8
27H	V5 + (V1 – V5)X 34.8 / 126.8	V10 + (V6 – V10)X 92 / 126.8
28H	V5 + (V1 – V5)X 34 / 126.8	V10 + (V6 – V10)X 92.8 / 126.8
29H	V5 + (V1 – V5)X 33.2 / 126.8	V10 + (V6 – V10)X 93.6 / 126.8
2AH	V5 + (V1 – V5)X 32.4 / 126.8	V10 + (V6 – V10)X 94.4 / 126.8
2BH	V5 + (V1 – V5)X 31.6 / 126.8	V10 + (V6 – V10)X 95.2 / 126.8
2CH	V5 + (V1 – V5)X 30.8 / 126.8	V10 + (V6 – V10)X 96 / 126.8
2DH	V5 + (V1 – V5)X 30 / 126.8	V10 + (V6 – V10)X 96.8 / 126.8
2EH	V5 + (V1 – V5)X 29.2 / 126.8	V10 + (V6 – V10)X 97.6 / 126.8
2FH	V5 + (V1 – V5)X 28.4/ 126.8	V10 + (V6 – V10)X 98.4 / 126.8
30H	V5 + (V1 – V5)X 27.6 / 126.8	V10 + (V6 – V10)X 99.2 / 126.8
31H	V5 + (V1 – V5)X 26.8 / 126.8	V10 + (V6 – V10)X 100 / 126.8
32H	V5 + (V1 – V5)X 26 / 126.8	V10 + (V6 – V10)X 100.8 / 126.8
33H	V5 + (V1 – V5)X 25.2 / 126.8	V10 + (V6 – V10)X 101.6 / 126.8
34H	V5 + (V1 – V5)X 24.4 / 126.8	V10 + (V6 – V10)X 102.4 / 126.8
35H	V5 + (V1 – V5)X 23.6 / 126.8	V10 + (V6 – V10)X 103.2 / 126.8
36H	V5 + (V1 – V5)X 22.4 / 126.8	V10 + (V6 – V10)X 104.4 / 126.8
37H	V5 + (V1 – V5)X 21.2 / 126.8	V10 + (V6 – V10)X 105.6 / 126.8
38H	V5 + (V1 – V5)X 20 / 126.8	V10 + (V6 – V10)X 106.8 / 126.8
39H	V5 + (V1 – V5)X 18.4 / 126.8	V10 + (V6 – V10)X 108.4 / 126.8
3AH	V5 + (V1 – V5)X 16.8 / 126.8	V10 + (V6 – V10)X 110 / 126.8
3BH	V5 + (V1 – V5)X 14.8 / 126.8	V10 + (V6 – V10)X 112 / 126.8
3CH	V5 + (V1 – V5)X 12.8 / 126.8	V10 + (V6 – V10)X 114 / 126.8
3DH	V5 + (V1 – V5)X 10.4 / 126.8	V10 + (V6 – V10)X 116.4 / 126.8
3EH	V5 + (V1 – V5)X 6.4 / 126.8	V10 + (V6 – V10)X 120.4 / 126.8
3FH	V5	V6

5.5 SPI Register Description

Register Name	Test RW	Address A3	A2	A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	–	–	–	–	–	PSC	STB	RESETB
						–	–	–	–	–	0	0	1
R1	0	0	0	0	1	–	–	–	–	–	RESL2	RESL1	RESL0
						–	–	–	–	–	0	0	0
R2	0	0	0	1	0	STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
						1	0	0	0	0	0	0	0
R3	0	0	0	1	1	–	STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0
						–	0	0	1	1	0	1	1
R4	0	0	1	0	0	–	EDGSL	LR	UD	CS	FRC	VS_POL	HS_POL
						–	0	1	0	1	1	0	0
R5	0	0	1	0	1	–	–	–	A_TIME1	A_TIME0	–	–	–
						–	–	–	0	0	1	0	0

※ RW must always keep low.
※ "–" = don`t care.

- **Register R0**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	PSC	STB	RESETB
Default	-	-	-	-	-	0	0	1

Table 5. 3 Register R0 setting

PSC: Operating mode setting by input pin or SPI register.
PSC="L", set STB, CS, RESL[2:0], EDGSL, LR, UD by input pin.
PSC="H", set STB, CS, RESL[2:0], EDGSL, LR, UD by SPI register.

STB: Standby mode setting.
STB="L", TCON and source driver are off.
STB="H", all the functions are on.

RESETB: Global reset.
RESETB="L", global reset the whole chip.
RESETB="H", Normal operation.

- **Register R1**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	RESL2	RESL1	RESL0
Default	–	–	–	–	–	0	0	0

Table 5. 4 Register R1 setting

RESL [2:0]: Display resolution selection.

RESL2	RESL1	RESL0	Resolution
0	0	0	800x480
0	0	1	800x600
0	1	0	1024x600
0	1	1	1024x768
1	0	0	NA
1	0	1	NA
1	1	0	NA
1	1	1	400x240

Table 5. 5 Display resolution selection

Register R2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	1	0	0	0	0	0	0	0

Table 5. 6 Register R2 setting

STHD [7:0]: adjust first dot data position,

T_{HS}= STHD [7:0]+ N (N depend on resolution)

STHD7	STHD6	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position adjust	Unit
0	0	0	0	0	0	0	0	0	T_{CPH}
0	0	0	0	0	0	0	1	1	T_{CPH}
0	0	0	0	0	0	1	0	2	T_{CPH}
0	0	0	0	0	0	1	1	3	T_{CPH}
0	0	0	0	0	1	0	0	4	T_{CPH}
0	0	0	0	0	1	0	1	5	T_{CPH}
0	0	0	0	0	1	1	0	6	T_{CPH}
0	0	0	0	0	1	1	1	7	T_{CPH}
0	1	0	1	1	0	0	0	88	T_{CPH}
0	1	0	1	1	0	0	1	89	T_{CPH}
0	1	0	1	1	0	1	0	90	T_{CPH}
0	1	1	1	1	1	1	0	126	T_{CPH}
0	1	1	1	1	1	1	1	127	T_{CPH}
1	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***128***	***T_{CPH}***
1	1	1	1	1	0	0	0	248	T_{CPH}
1	1	1	1	1	0	0	1	249	T_{CPH}
1	1	1	1	1	0	1	0	250	T_{CPH}
1	1	1	1	1	0	1	1	251	T_{CPH}
1	1	1	1	1	1	0	0	252	T_{CPH}
1	1	1	1	1	1	0	1	253	T_{CPH}
1	1	1	1	1	1	1	0	254	T_{CPH}
1	1	1	1	1	1	1	1	255	T_{CPH}

Table 5. 7 Adjust start pulse position by dot

- **Register R3**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0
Default	–	0	0	1	1	0	1	1

Table 5. 8 Register R3 setting

STVD [6:0]: adjust first line position, ***T_{VS}= STVD [6:0] + N (N depend on resolution)***.

STVD6	STVD5	STVD4	STVD3	STVD2	STVD1	STVD0	STV position adjust	Unit
0	0	0	0	0	0	0	0	T_H
0	0	0	0	0	0	1	1	T_H
0	0	0	0	0	1	0	2	T_H
0	0	0	0	0	1	1	3	T_H
0	0	0	0	1	0	0	4	T_H
0	0	0	0	1	0	1	5	T_H
0	0	0	0	1	1	0	6	T_H
0	0	0	0	1	1	1	7	T_H
				⋮				
0	0	1	1	0	0	0	24	T_H
0	0	1	1	0	0	1	25	T_H
0	0	1	1	0	1	0	26	T_H
0	***0***	***1***	***1***	***0***	***1***	***1***	***27***	***T_H***
0	0	1	1	1	0	0	28	T_H
0	0	1	1	1	0	1	29	T_H
0	0	1	1	1	1	0	30	T_H
0	0	1	1	1	1	1	31	T_H
				⋮				
1	1	1	1	0	0	0	120	T_H
1	1	1	1	0	0	1	121	T_H
1	1	1	1	0	1	0	122	T_H
1	1	1	1	0	1	1	123	T_H
1	1	1	1	1	0	0	124	T_H
1	1	1	1	1	0	1	125	T_H
1	1	1	1	1	1	0	126	T_H
1	1	1	1	1	1	1	127	T_H

Table 5. 9 Adjust first line position by line

- **Register R4**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	EDGSL	LR	UD	CS	FRC	VS_POL	HS_POL
Default	–	0	1	0	1	1	0	0

Table 5. 10 Register R4 setting

EDGSL: Define input clock polarity.
EDGSL="L", CLK polarity is not inverted, latch data at CLK rising edge.
EDGSL="H", CLK polarity is inverted, latch data at CLK falling edge.

LR: Shift direction control.
LR=H: DIO1->SO1->• • • • • •->SO1200->DIO2
LR=L: DIO2->SO1200->• • • • • •->SO1->DIO1

UD: Gate Driver Up/down scan setting.
UD=H, reverse scan.
UD=L, normal scan.

CS: Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function.

FRC: Dithering ON/OFF control.
FRC=L, Dithering function disable.
FRC=H, Dithering function enable

VS_POL: VS polarity setting.
VS_POL=L, negative polarity.
VS_POL=H, positive polarity.

HS_POL: HS polarity setting.
HS_POL=L, negative polarity.
HS_POL=H, positive polarity.

- **Register R5**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	A_TIME1	A_TIME0	reserved	reserved	reserved
Default	–	–	–	0	0	1	0	0

Table 5. 11 Register R5 setting

A_TIME [1:0]: The blank image display time is decided by A_TIME

00: blank image display time is 4 VS time.

01: blank image display time is 8 VS time.

10: blank image display time is 16 VS time.

11: blank image display time is 32 VS time.

5.6 Power on/off sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC, GND → VDDA, VSS → V1 to V10
Power OFF: V1 to V10 → VDDA, VSS → VCC, GND

5.7 Power on control

HX8258-A has a power ON sequence control function. When power is ON, blank data is outputted for 4-frames (default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TIME[1:0].

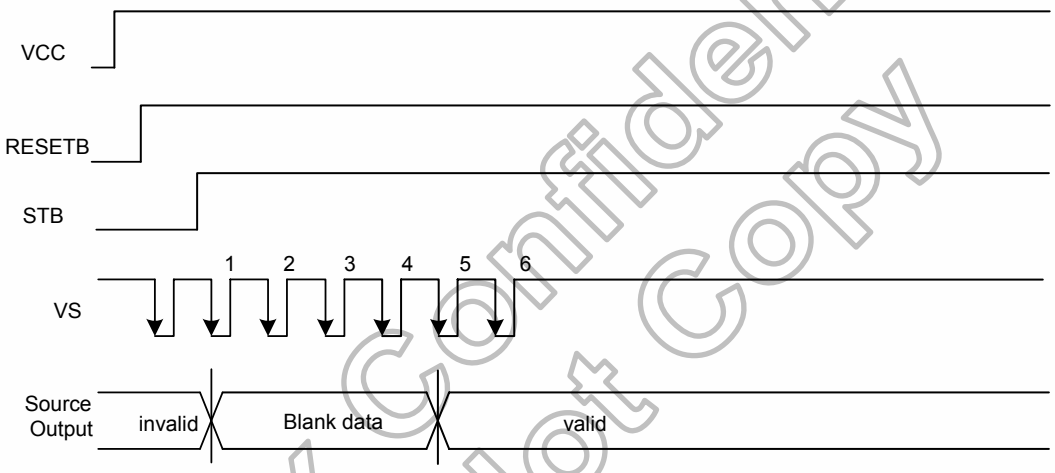


Figure 5. 27 Power on control for Auto Mode

5.8 Standby on/off control

HX8258-A has a standby ON/OFF sequence control function. When STB pin is “L”, blank data is outputted for 11-frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel.

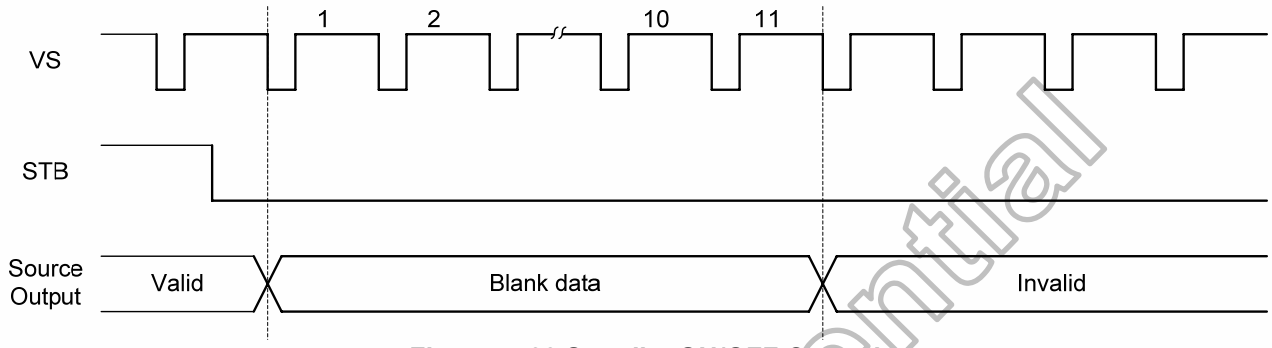


Figure 5. 28 Standby ON/OFF Control

5.9 Reset when power on

HX8258-A is internally initialized by the global reset signal, RESETB. The reset input must be held for at least 1ms after power is stable. Write SPI commend must after RESET rising more than 10 us.

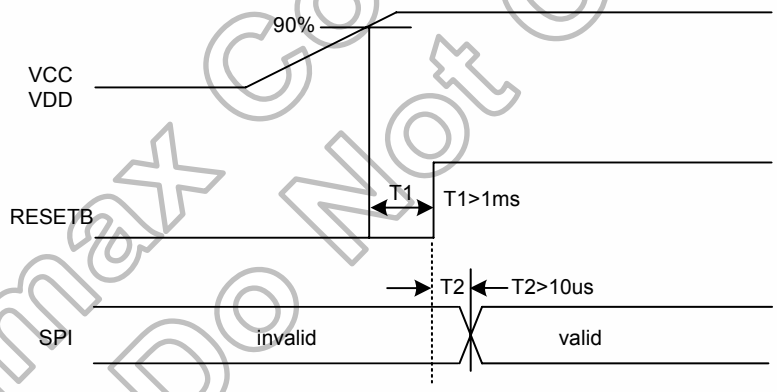


Figure 5. 29 RESETB control after power stable

6. DC Characteristics

6.1 Absolute Maximum Rating (GND=VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VCC	-0.3	-	+7.0	V
Power supply voltage 2	VDDA	-0.3	-	+13.5	V
Logic Output Voltage	V_{OUT}	-0.3	-	+7.0	V
Input voltage	Vin	-0.3	-	VDDA+0.3	V
Operation temperature	T_{OPR}	-40	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: (1) All of the voltages listed above are with respective to GND=VSS=0V.
(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6.2 DC Electrical Characteristics (GND=VSS=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	2.7	3.3	3.6	V	-
Power supply voltage	VDDA	6.5	8.4	13.5	V	-
Low level input voltage	V_{IL}	0	-	0.3*VCC	V	-
High level input voltage	V_{IH}	0.7*VCC	-	VCC	V	-
Output low voltage	V_{OL}	0	-	0.2*VCC	V	I_{OL}=400μA
Output high voltage	V_{OH}	0.8*VCC	-	VCC	V	I_{OH}=-400μA
Input level V1~V4, V6	Vref1	0.35*VDDA		VDDA-0.1	V	Gamma correction voltage input, VDDA=8.4V
Input level V7~V10, V5	Vref2	VSSA+0.1		0.65*VDDA	V	Gamma correction voltage input, VDDA=8.4V
Input leakage current	I_{IN}	-1	-	+1	V	No pull up or pull down.
Output voltage deviation	V_{VD}	-	±20	-	mV	SO1~SO1200
DC offset	V_{OS}	-	-	±20	mV	SO1~SO1200, V_{IN}=0.1~13.4V,
Output leakage current	I_O	-1	-	+1	μA	SO1~SO1200 at high impedance
Pull high resistance	R_H	250	500	750	kΩ	RESETB,STB, TEN, CS, SPCK, SPEN, SDI, LR, VSET
Pull low resistance	R_L	250	500	750	kΩ	Dx[7:0] (x=2,1,0), DEN,RESL[2:0], REV, EDGSL, ENREOP, UD, TEST[1:0], TESTG[1:0]
Output current	I_{OH}	40	60	-	μA	SO1~SO1200, V_O =9.9V vs. 9V, VDDA=10V
Output current	I_{OL}	40	60	-	μA	SO1~SO1200, Vo=0.1V vs. 1.0V, VDDA=10V
Analog operating current	I_{DD}	-	10	-	mA	Fcph=33.3MHz, Parallel RGB, Fhs=32kHz, Black pattern, VDDA=8.4V, Vcc=3.3V, RL=2k, CL=60pF
Digital operating current	I_{CC}	-	4.4	-	mA	Fcph=33.3MHz, Parallel RGB, Fhs=32kHz, Black pattern, VDDA=8.4V, Vcc=3.3V, RL=2k, CL=60pF
Analog standby current	I_{VDDA}	-	-	200	μA	All LCD outputs are High-Z.
Digital standby current	I_{VCC}	-	-	800	μA	All inputs are stopped and outputs are High-Z.

7. AC Characteristics

7.1 Input signal characteristics

7.1.1 AC Electrical Characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
HS setup time	T_{hst}	6	-	-	ns
HS hold time	T_{hhd}	6	-	-	ns
VS setup time	T_{vst}	6	-	-	ns
VS hold time	T_{vhd}	6	-	-	ns
Data setup time	T_{dsu}	6	-	-	ns
Data hold time	T_{dhd}	6	-	-	ns
DEN setup time	T_{esu}	6	-	-	ns
Source output settling time	T_{ST}	-	-	15	µs
Source output loading R	R_{SL}	-	2	-	kΩ
Source output loading C	C_{SL}	-	60	-	pF
Repair OP output loading C	C_{RL}	-	150	-	pF
Repair OP output settling time	T_{RT}	-	-	15	µs
POL output delay time	T_{DP}	-	-	40	ns

7.1.2 Resolution：800x480

- **sync mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	29.93	33.26	36.59	MHz
CLK period	T_{CPH}	27.32	30.06	33.41	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	950	1056	1600	T_{CPH}
HS pulse width	T_{WH}	1	128	T_{HS} -2	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+88(1)			T_{CPH}
HS Active Time	T_{HA}	-	800	-	T_{CPH}
VS period	T_V	490	525	625	T_H
VS pulse width	T_{WV}	1	2	T_{VS}	T_H
VS-DEN time	T_{VS}	STVD[6:0]+8			T_H
VS Active Time	T_{VA}	-	480	-	T_H

Note: (1) $T_{HS}+T_{HA}<T_H$

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	29.93	33.26	36.59	MHz
CLK period	T_{CPH}	-	30.06	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1000	1056	1200	T_{CPH}
DE pulse width	T_{DEH}	-	800	-	T_{CPH}
DE frame blanking(2)	T_{DEB}	10	45	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{DE}	-	480	-	$T_{DEH}+T_{DEL}$

Note: (2) DE frame blanking (T_{DEB}) must be the integer of DE period ($T_{DEH}+T_{DEL}$).

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	150	-	T_{CPH}
CKV pulse width	T_{CKV}	-	133	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	40	-	T_{CPH}
DE(internal)-OEV time	T_3	-	23	-	T_{CPH}
DE(internal)-POL time	T_4	-	157	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

7.1.3 Resolution：800x600

- **sync mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	35.81	39.79	43.77	MHz
CLK period	T_{CPH}	22.85	25.13	27.92	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	950	1056	1600	T_{CPH}
HS pulse width	T_{WH}	1	128	T_{HS-2}	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+88(1)			T_{CPH}
HS Active Time	T_{HA}	-	800	-	T_{CPH}
VS period	T_V	610	628	720	T_H
VS pulse width	T_{WV}	1	4	T_{VS}	T_H
VS-DEN time	T_{VS}	STVD[6:0]+0			T_H
VS Active Time	T_{VA}	-	600	-	T_H

Note: (1) $T_{HS}+T_{HA}<T_H$

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	39.79	-	MHz
CLK period	T_{CPH}	-	25.13	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1000	1056	1200	T_{CPH}
DE pulse width	T_{DEH}	-	800	-	T_{CPH}
DE frame blanking(2)	T_{DEB}	10	28	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{DE}	-	600	-	$T_{DEH}+T_{DEL}$

Note: (2) DE frame blanking (T_{DEB}) must be the integer of DE period ($T_{DEH}+T_{DEL}$).

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	150	-	T_{CPH}
CKV pulse width	T_{CKV}	-	133	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	40	-	T_{CPH}
DE(internal)-OEV time	T_3	-	23	-	T_{CPH}
DE(internal)-POL time	T_4	-	157	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

7.1.4 Resolution：1024x600

- **sync mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	50.64	-	MHz
CLK period	T_{CPH}	-	19.75	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1344	-	T_{CPH}
HS pulse width	T_{WH}	1	136	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+168(1)			T_{CPH}
HS Active Time	T_{HA}	-	1024	-	T_{CPH}
VS period	T_V	-	628	-	T_H
VS pulse width	T_{WV}	1	4	-	T_H
VS-DEN time	T_{VS}	STVD[6:0]+0			T_H
VS Active Time	T_{VA}	-	600	-	T_H

Note: (1) $T_{HS}+T_{HA}<T_H$

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	50.64	-	MHz
CLK period	T_{CPH}	-	19.75	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1300	1344	1500	T_{CPH}
DE pulse width	T_{DEH}	-	1024	-	T_{CPH}
DE frame blanking(2)	T_{DEB}	10	28	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{DE}	-	600	-	$T_{DEH}+T_{DEL}$

Note: (2) DE frame blanking (T_{DEB}) must be the integer of DE period ($T_{DEH}+T_{DEL}$).

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	229	-	T_{CPH}
CKV pulse width	T_{CKV}	-	203	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	61	-	T_{CPH}
DE(internal)-OEV time	T_3	-	35	-	T_{CPH}
DE(internal)-POL time	T_4	-	238	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

7.1.5 Resolution：1024x768

- **sync mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	65.00	-	MHz
CLK period	T_{CPH}	-	15.39	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1344	-	T_{CPH}
HS pulse width	T_{WH}	1	136	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]+168(1)			T_{CPH}
HS Active Time	T_{HA}	-	1024	-	T_{CPH}
VS period	T_V	-	806	-	T_H
VS pulse width	T_{WV}	1	6	-	T_H
VS-DEN time	T_{VS}	STVD[6:0]+8			T_H
VS Active Time	T_{VA}	-	768	-	T_H

Note: (1) $T_{HS}+T_{HA}<T_H$

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	65.00	-	MHz
CLK period	T_{CPH}	-	15.39	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	1300	1344	1500	T_{CPH}
DE pulse width	T_{DEH}	-	1024	-	T_{CPH}
DE frame blanking(2)	T_{DEB}	10	38	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{DE}	-	768	-	$T_{DEH}+T_{DEL}$

Note: (2) DE frame blanking (T_{DEB}) must be the integer of DE period ($T_{DEH}+T_{DEL}$).

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	292	-	T_{CPH}
CKV pulse width	T_{CKV}	-	260	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	78	-	T_{CPH}
DE(internal)-OEV time	T_3	-	46	-	T_{CPH}
DE(internal)-POL time	T_4	-	305	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

7.1.6 Resolution：400x240

- **Sync mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	8.3	-	MHz
CLK period	T_{CPH}	-	120.47	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	528	-	T_{CPH}
HS pulse width	T_{WH}	1	46	-	T_{CPH}
HS-first horizontal data time	T_{HS}	STHD[7:0]-26(1) (2)			T_{CPH}
HS Active Time	T_{HA}	-	400	-	T_{CPH}
VS period	T_V	-	262	-	T_H
VS pulse width	T_{WV}	1	2	-	T_H
VS-DEN time	T_{VS}	STVD[6:0]-9(3)			T_H
VS Active Time	T_{VA}	-	240	-	T_H

Note: (1) $T_{HS}+T_{HA}<T_H$
(2) T_{HS} must be greater than 8 → STHD[7:0] must be greater than 34
(3) T_{VS} must be greater than 0 → STVD[6:0] must be greater than 9

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	8.3	-	MHz
CLK period	T_{CPH}	-	120.47	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
DE period	$T_{DEH}+T_{DEL}$	500	528	600	T_{CPH}
DE pulse width	T_{DEH}	-	400	-	T_{CPH}
DE frame blanking(2)	T_{DEB}	10	22	110	$T_{DEH}+T_{DEL}$
DE frame width	T_{DE}	-	240	-	$T_{DEH}+T_{DEL}$

Note: (2) DE frame blanking (T_{DEB}) must be the integer of DE period ($T_{DEH}+T_{DEL}$).

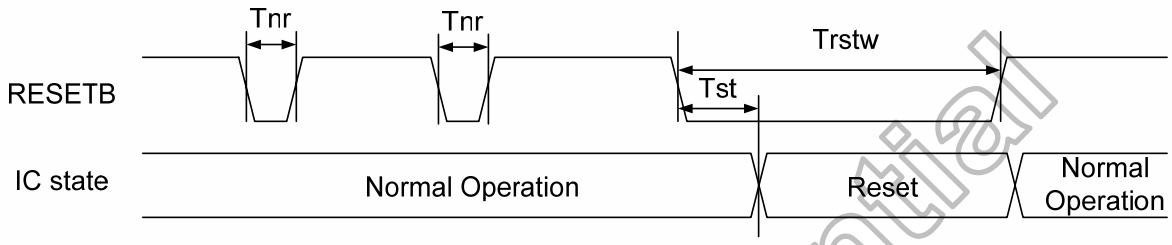
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	43	-	T_{CPH}
CKV pulse width	T_{CKV}	-	39	-	T_{CPH}
DE(internal)-STV time	T_1	-	4	-	T_{CPH}
DE(internal)-CKV time	T_2	-	14	-	T_{CPH}
DE(internal)-OEV time	T_3	-	10	-	T_{CPH}
DE(internal)-POL time	T_4	-	45	-	T_{CPH}
STV pulse width	-	-	1	-	T_H

7.1.7 AC Electrical Characteristics without timing controller

Parameter	Symbol	Spec.			Unit	Conditions
		Min.	Typ.	Max.		
CLK frequency	Fclk	-	65	70	MHz	-
CLK pulse width	Tcw	6	-	-	ns	-
Data set-up time	Tsu	4	-	-	ns	Dx0~Dx5 (x=0,1,2), REV and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	Dx0~Dx5 (x=0,1,2), REV and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=20pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	-
Pulse width of LD	Twld	2	-	-	Tcph	-
Time that LD to DIO1/2	Tlds	5	-	-	Tcph	-
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	15	μs	10% or 90% target voltage, CL=60pF, R=2kΩ

7.1.8 Hardware reset timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
RESETB low pulse width	T_{rstw}	10	-	-	µs
Negative noise pulse width	T_{nr}		-	2	µs
Reset start time	T_{st}	2	-		µs



8. Waveform

8.1 Timing Controller Timing Chart

8.1.1 Clock and Data input waveforms

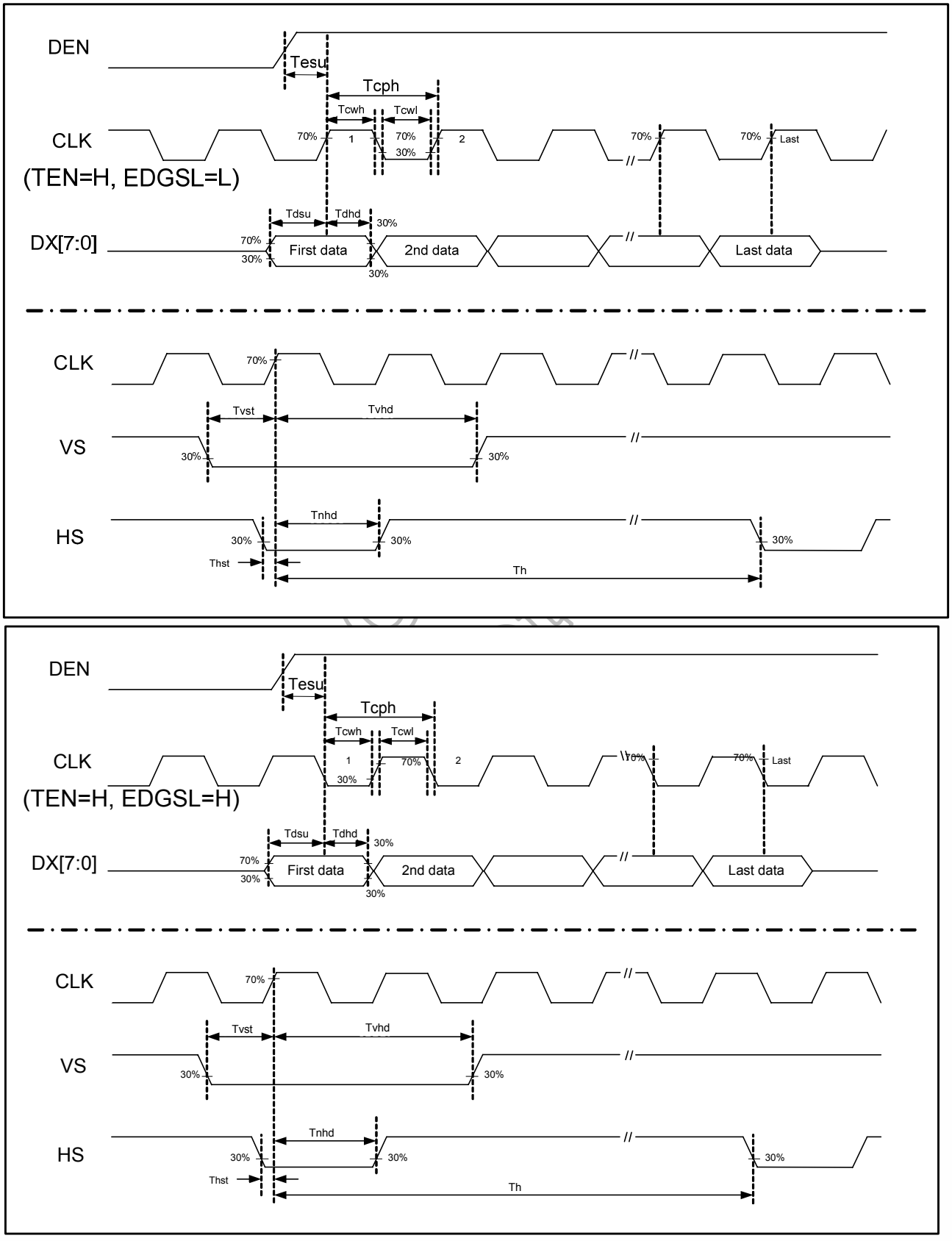


Figure 8. 1 Clock and Data input waveforms

8.1.2 Data input format

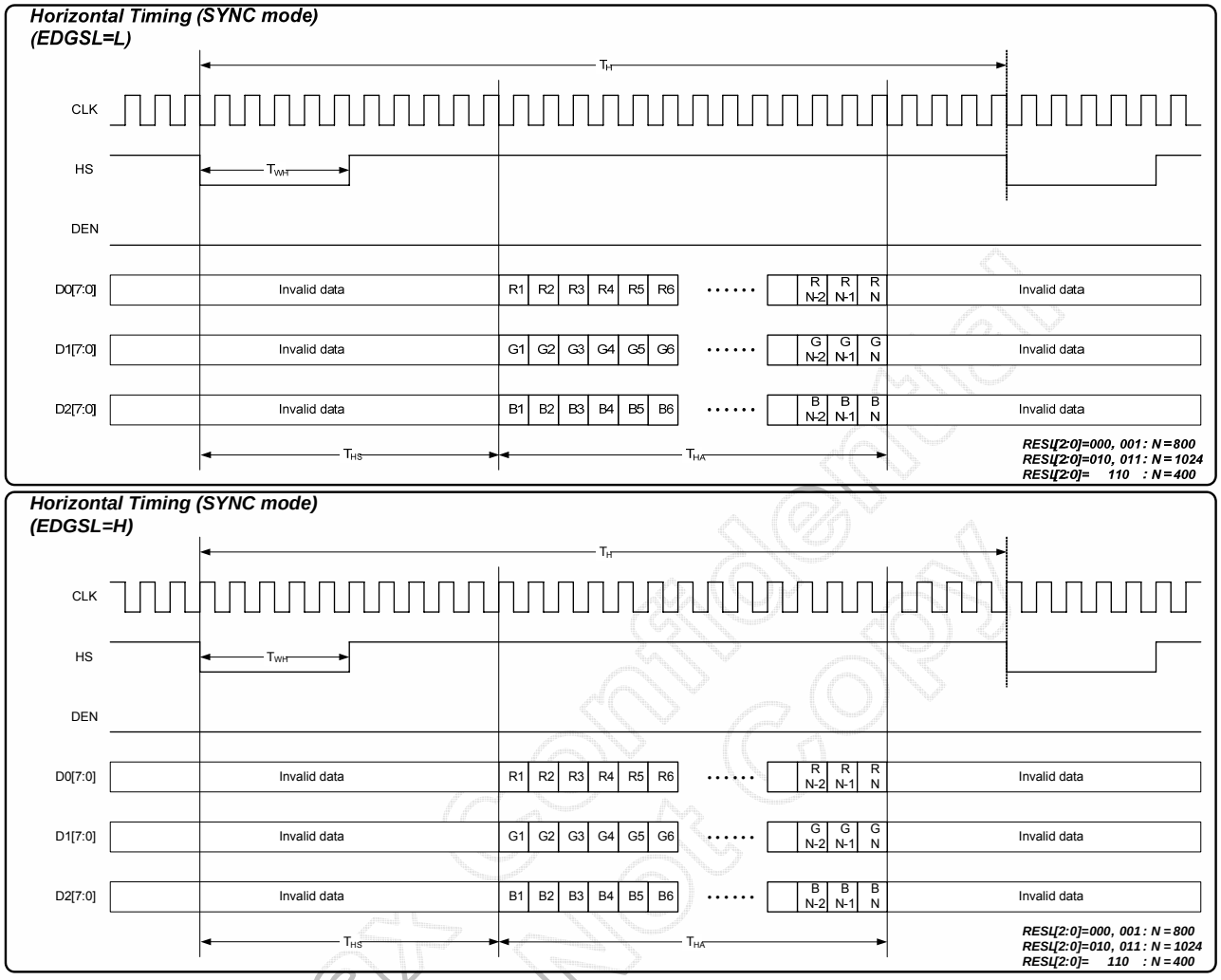


Figure 8. 2 SYNC Mode Horizontal Data Format

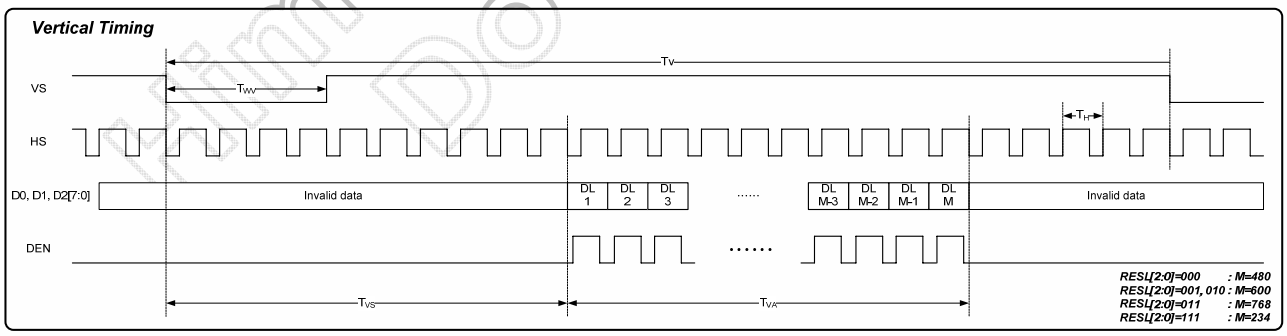


Figure 8. 3 SYNC Mode Vertical Data Format

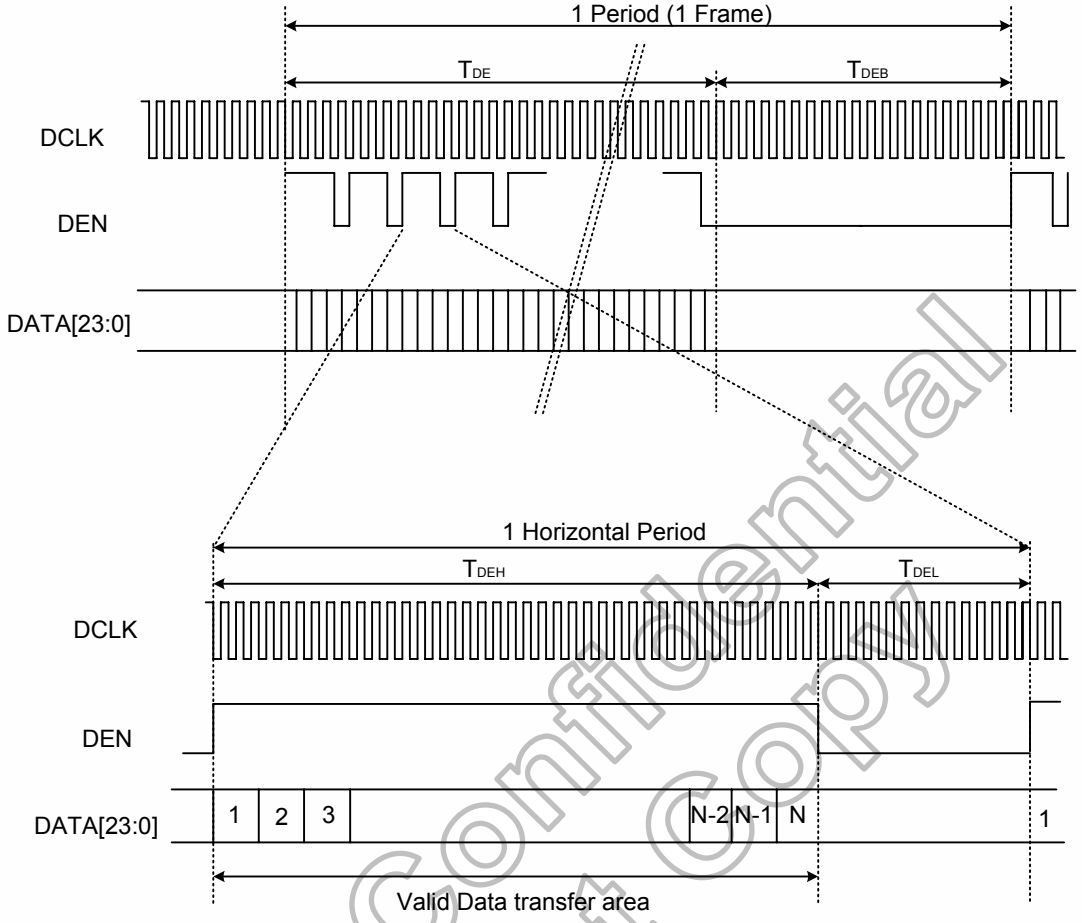


Figure 8. 4 DE Mode Data Format

8.1.3 Digital Output timing waveforms

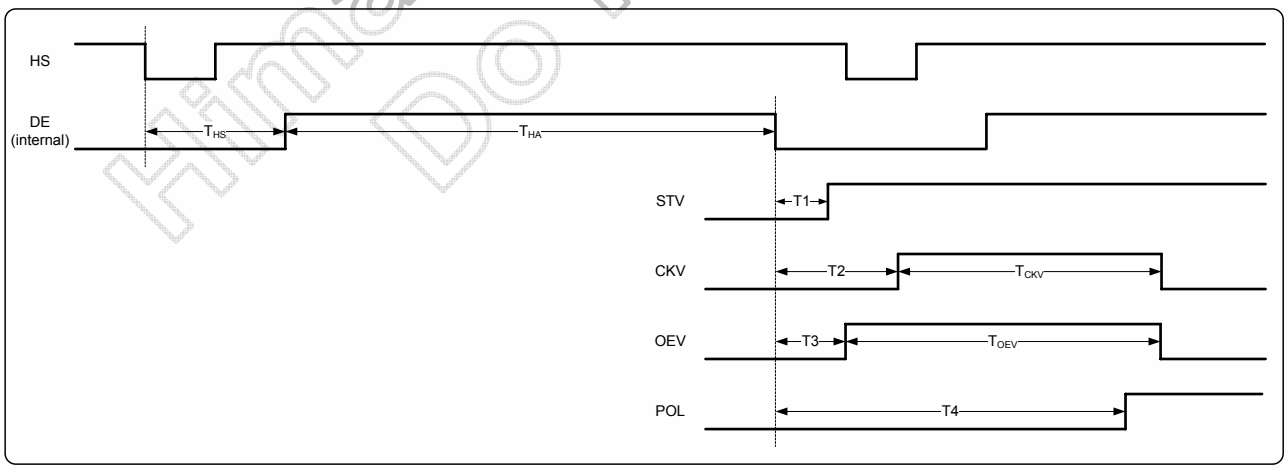


Figure 8. 5 Digital output timing waveforms

8.2 Timing Chart without Timing controller

Without timing controller, HX8258-A supports two configure modes (EDGSL=L or H). Two configuration examples for 1200 channels are illustrated as figure 8.6 & 8.7. And examples for 1026 channels and 1020 channels as figure 8.8 and 8.9 under EDGSL =H.

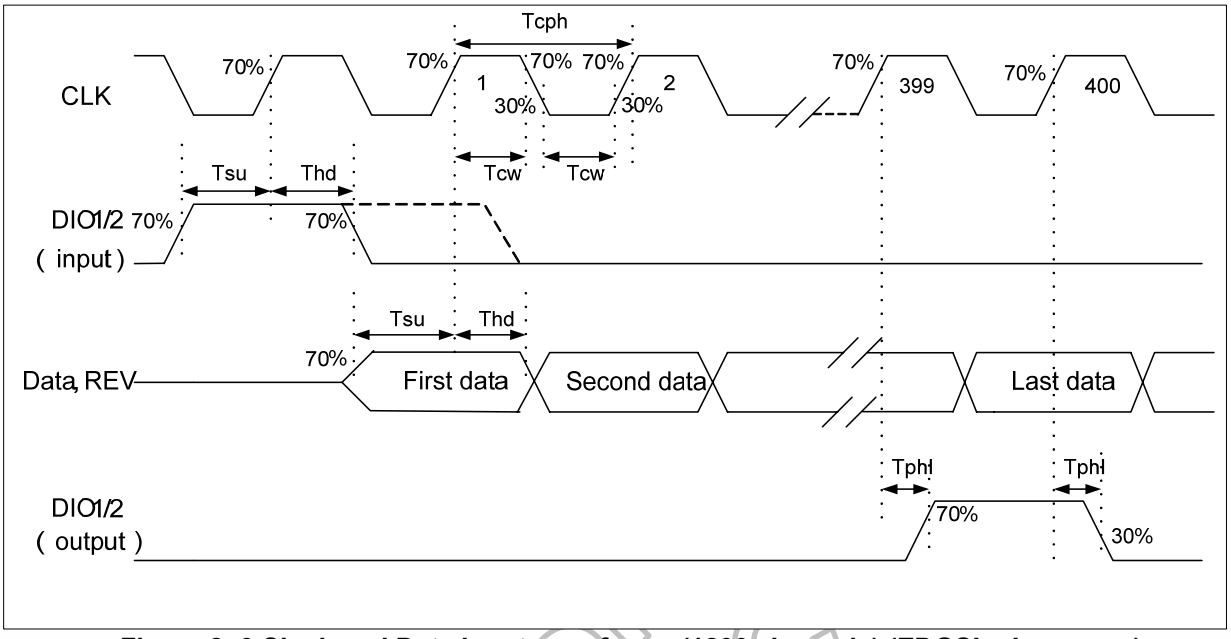


Figure 8. 6 Clock and Data input waveforms (1200 channels) (EDGSL =L or open)

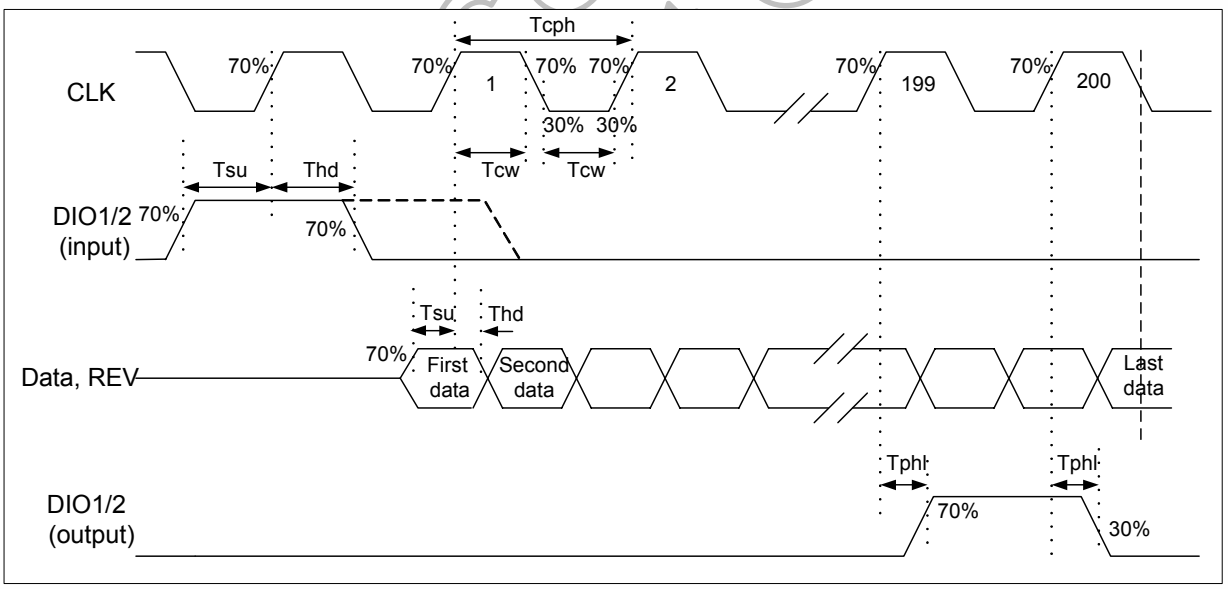


Figure 8. 7 Clock and Data input waveforms (1200 channels) (EDGSL =H)

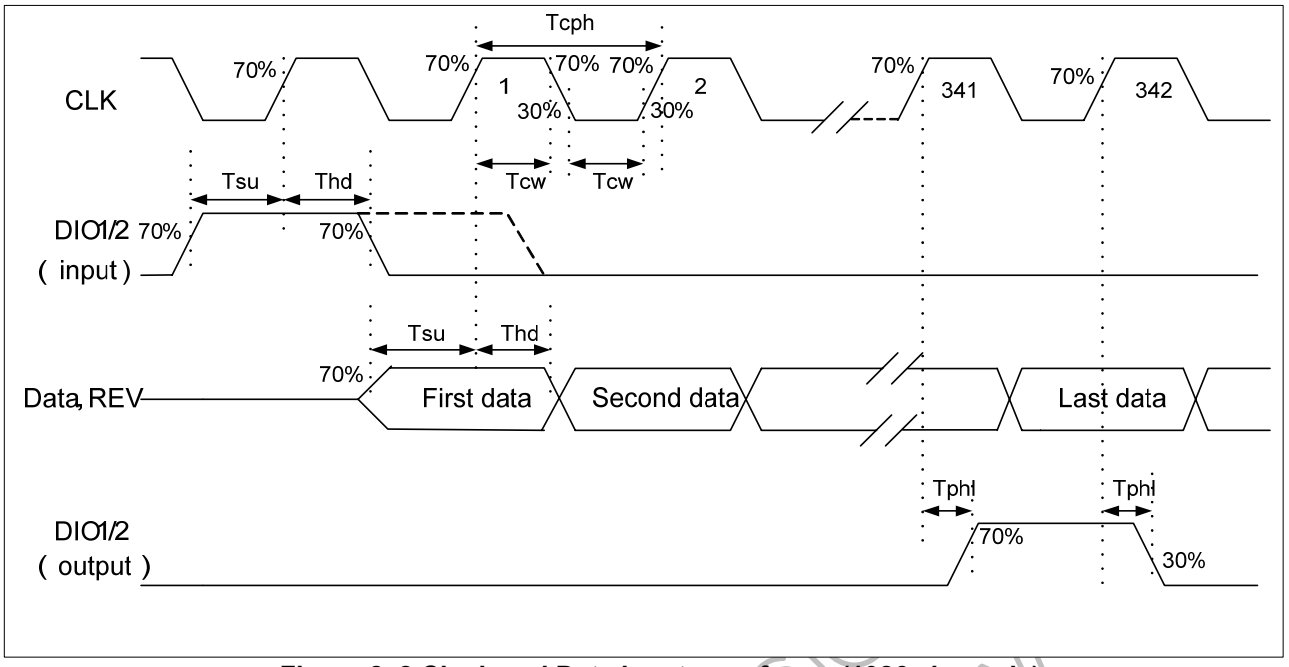


Figure 8. 8 Clock and Data input waveforms (1026 channels)

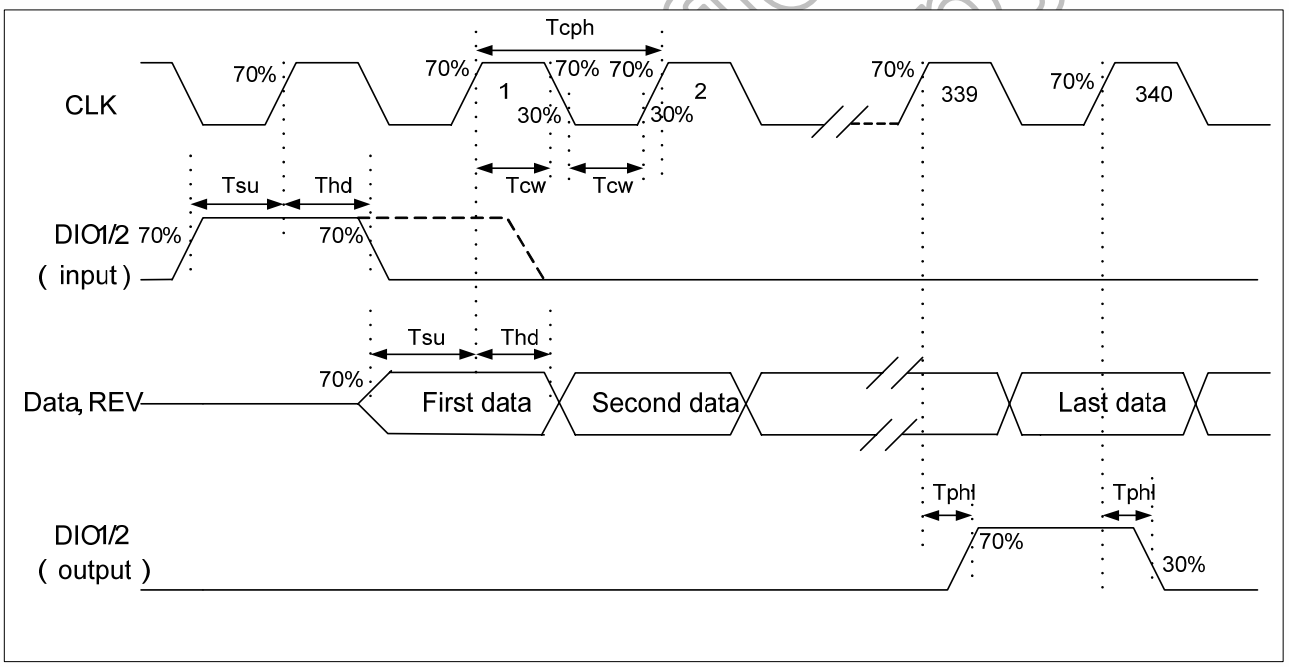


Figure 8. 9 Clock and Data input waveforms (1020 channels)

8.3 Output Timing Chart

8.3.1 Source Driver output timing waveforms

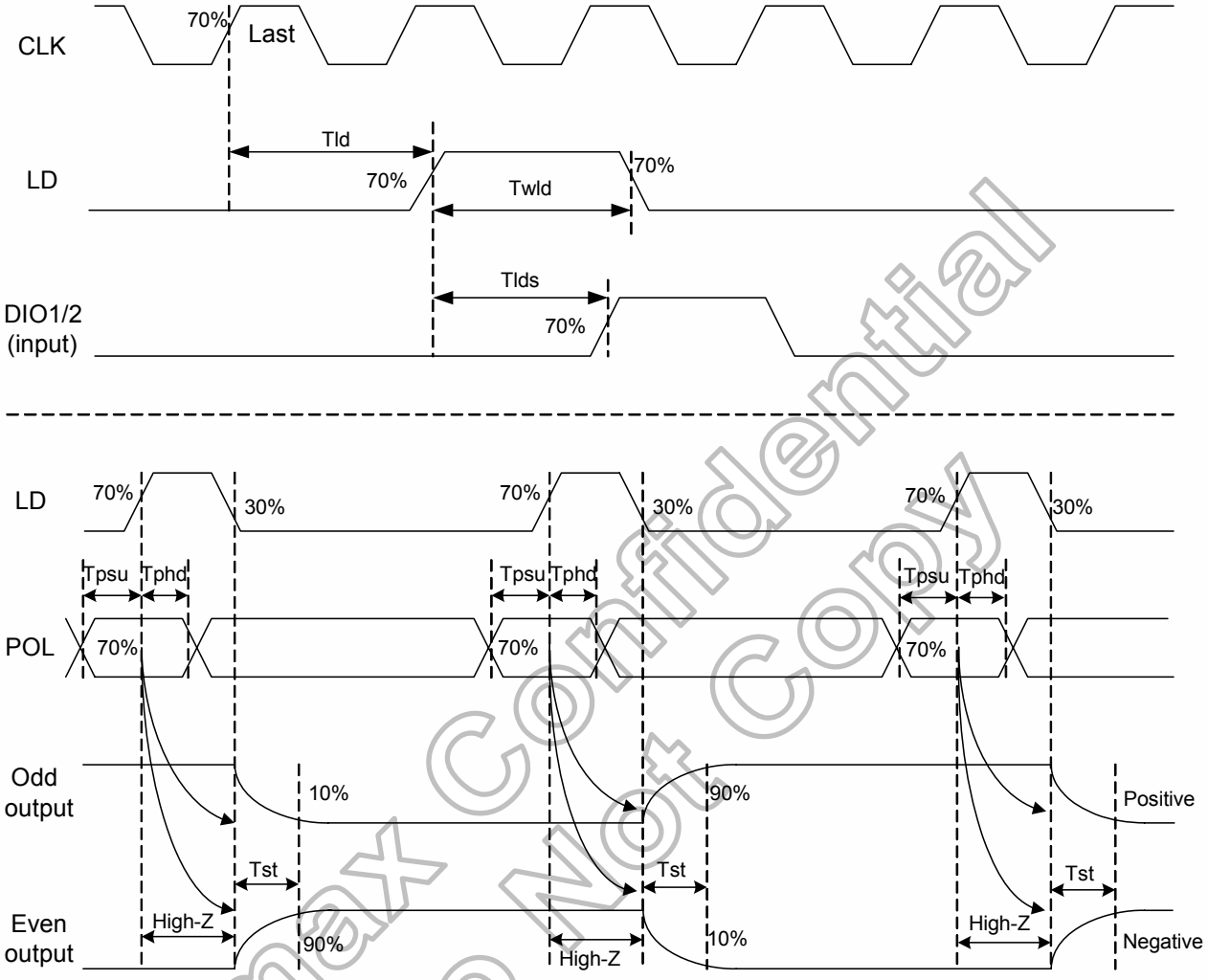
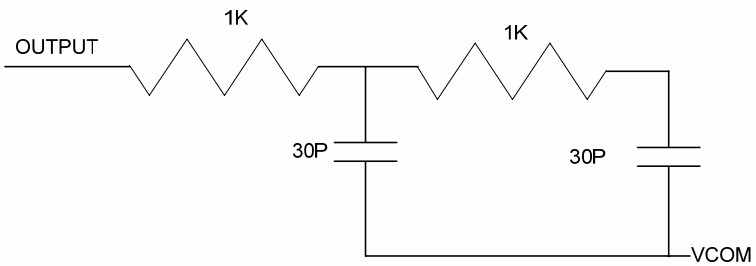


Figure 8. 10 LD and Source Data Output timing waveforms

Source Output load condition



9. SPI timing characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

- **SPI timing**

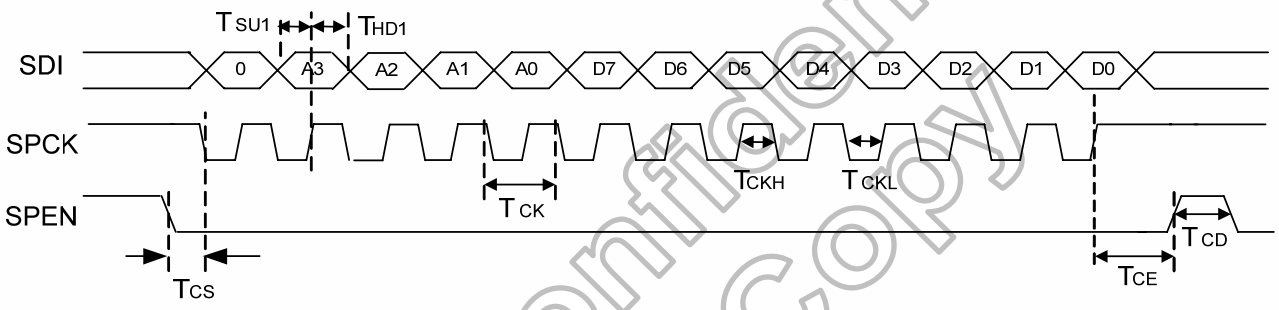
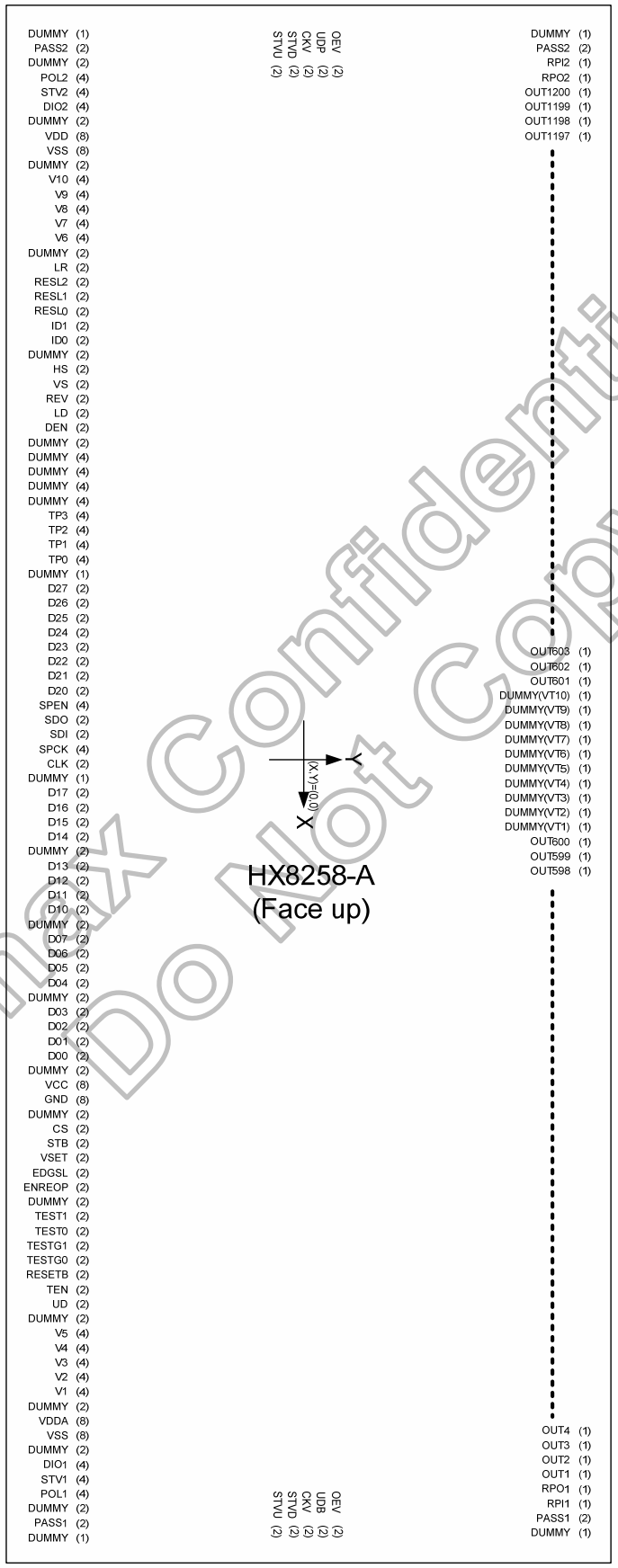


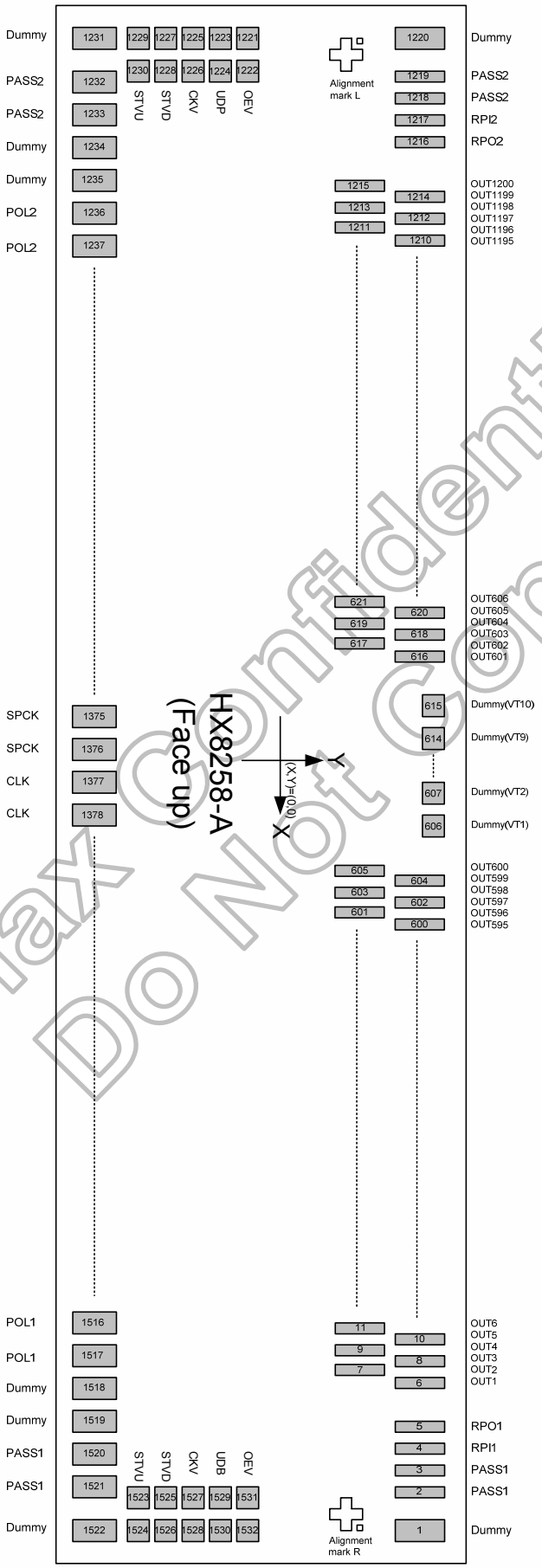
Figure 9. 1 SPI timing (write data)

- SPEN must keep low more than 13 clocks after SDI starting to write data.
- Write SPI commend must after RESET rising more than 10 us.

10. Pin Assignment (IC face view)



11. Package Outline



11.1 Pad Diagram

No.	Name	X	Y
1	DUMMY	10370	460
2	PASS1	10321	460
3	PASS1	10290	460
4	RPI1	10259	460
5	RPO1	10228	460
6	OUT1	10167	460
7	OUT2	10151.5	340
8	OUT3	10136	460
9	OUT4	10120.5	340
10	OUT5	10105	460
11	OUT6	10089.5	340
12	OUT7	10074	460
13	OUT8	10058.5	340
14	OUT9	10043	460
15	OUT10	10027.5	340
16	OUT11	10012	460
17	OUT12	9996.5	340
18	OUT13	9981	460
19	OUT14	9965.5	340
20	OUT15	9950	460
21	OUT16	9934.5	340
22	OUT17	9919	460
23	OUT18	9903.5	340
24	OUT19	9888	460
25	OUT20	9872.5	340
26	OUT21	9857	460
27	OUT22	9841.5	340
28	OUT23	9826	460
29	OUT24	9810.5	340
30	OUT25	9795	460
31	OUT26	9779.5	340
32	OUT27	9764	460
33	OUT28	9748.5	340
34	OUT29	9733	460
35	OUT30	9717.5	340
36	OUT31	9702	460
37	OUT32	9686.5	340
38	OUT33	9671	460
39	OUT34	9655.5	340
40	OUT35	9640	460
41	OUT36	9624.5	340
42	OUT37	9609	460
43	OUT38	9593.5	340
44	OUT39	9578	460
45	OUT40	9562.5	340
46	OUT41	9547	460
47	OUT42	9531.5	340
48	OUT43	9516	460
49	OUT44	9500.5	340
50	OUT45	9485	460

No.	Name	X	Y
51	OUT46	9469.5	340
52	OUT47	9454	460
53	OUT48	9438.5	340
54	OUT49	9423	460
55	OUT50	9407.5	340
56	OUT51	9392	460
57	OUT52	9376.5	340
58	OUT53	9361	460
59	OUT54	9345.5	340
60	OUT55	9330	460
61	OUT56	9314.5	340
62	OUT57	9299	460
63	OUT58	9283.5	340
64	OUT59	9268	460
65	OUT60	9252.5	340
66	OUT61	9237	460
67	OUT62	9221.5	340
68	OUT63	9206	460
69	OUT64	9190.5	340
70	OUT65	9175	460
71	OUT66	9159.5	340
72	OUT67	9144	460
73	OUT68	9128.5	340
74	OUT69	9113	460
75	OUT70	9097.5	340
76	OUT71	9082	460
77	OUT72	9066.5	340
78	OUT73	9051	460
79	OUT74	9035.5	340
80	OUT75	9020	460
81	OUT76	9004.5	340
82	OUT77	8989	460
83	OUT78	8973.5	340
84	OUT79	8958	460
85	OUT80	8942.5	340
86	OUT81	8927	460
87	OUT82	8911.5	340
88	OUT83	8896	460
89	OUT84	8880.5	340
90	OUT85	8865	460
91	OUT86	8849.5	340
92	OUT87	8834	460
93	OUT88	8818.5	340
94	OUT89	8803	460
95	OUT90	8787.5	340
96	OUT91	8772	460
97	OUT92	8756.5	340
98	OUT93	8741	460
99	OUT94	8725.5	340
100	OUT95	8710	460

No.	Name	X	Y
101	OUT96	8694.5	340
102	OUT97	8679	460
103	OUT98	8663.5	340
104	OUT99	8648	460
105	OUT100	8632.5	340
106	OUT101	8617	460
107	OUT102	8601.5	340
108	OUT103	8586	460
109	OUT104	8570.5	340
110	OUT105	8555	460
111	OUT106	8539.5	340
112	OUT107	8524	460
113	OUT108	8508.5	340
114	OUT109	8493	460
115	OUT110	8477.5	340
116	OUT111	8462	460
117	OUT112	8446.5	340
118	OUT113	8431	460
119	OUT114	8415.5	340
120	OUT115	8400	460
121	OUT116	8384.5	340
122	OUT117	8369	460
123	OUT118	8353.5	340
124	OUT119	8338	460
125	OUT120	8322.5	340
126	OUT121	8307	460
127	OUT122	8291.5	340
128	OUT123	8276	460
129	OUT124	8260.5	340
130	OUT125	8245	460
131	OUT126	8229.5	340
132	OUT127	8214	460
133	OUT128	8198.5	340
134	OUT129	8183	460
135	OUT130	8167.5	340
136	OUT131	8152	460
137	OUT132	8136.5	340
138	OUT133	8121	460
139	OUT134	8105.5	340
140	OUT135	8090	460
141	OUT136	8074.5	340
142	OUT137	8059	460
143	OUT138	8043.5	340
144	OUT139	8028	460
145	OUT140	8012.5	340
146	OUT141	7997	460
147	OUT142	7981.5	340
148	OUT143	7966	460
149	OUT144	7950.5	340
150	OUT145	7935	460

No.	Name	X	Y
151	OUT146	7919.5	340
152	OUT147	7904	460
153	OUT148	7888.5	340
154	OUT149	7873	460
155	OUT150	7857.5	340
156	OUT151	7842	460
157	OUT152	7826.5	340
158	OUT153	7811	460
159	OUT154	7795.5	340
160	OUT155	7780	460
161	OUT156	7764.5	340
162	OUT157	7749	460
163	OUT158	7733.5	340
164	OUT159	7718	460
165	OUT160	7702.5	340
166	OUT161	7687	460
167	OUT162	7671.5	340
168	OUT163	7656	460
169	OUT164	7640.5	340
170	OUT165	7625	460
171	OUT166	7609.5	340
172	OUT167	7594	460
173	OUT168	7578.5	340
174	OUT169	7563	460
175	OUT170	7547.5	340
176	OUT171	7532	460
177	OUT172	7516.5	340
178	OUT173	7501	460
179	OUT174	7485.5	340
180	OUT175	7470	460
181	OUT176	7454.5	340
182	OUT177	7439	460
183	OUT178	7423.5	340
184	OUT179	7408	460
185	OUT180	7392.5	340
186	OUT181	7377	460
187	OUT182	7361.5	340
188	OUT183	7346	460
189	OUT184	7330.5	340
190	OUT185	7315	460
191	OUT186	7299.5	340
192	OUT187	7284	460
193	OUT188	7268.5	340
194	OUT189	7253	460
195	OUT190	7237.5	340
196	OUT191	7222	460
197	OUT192	7206.5	340
198	OUT193	7191	460
199	OUT194	7175.5	340
200	OUT195	7160	460

No.	Name	X	Y
201	OUT196	7144.5	340
202	OUT197	7129	460
203	OUT198	7113.5	340
204	OUT199	7098	460
205	OUT200	7082.5	340
206	OUT201	7067	460
207	OUT202	7051.5	340
208	OUT203	7036	460
209	OUT204	7020.5	340
210	OUT205	7005	460
211	OUT206	6989.5	340
212	OUT207	6974	460
213	OUT208	6958.5	340
214	OUT209	6943	460
215	OUT210	6927.5	340
216	OUT211	6912	460
217	OUT212	6896.5	340
218	OUT213	6881	460
219	OUT214	6865.5	340
220	OUT215	6850	460
221	OUT216	6834.5	340
222	OUT217	6819	460
223	OUT218	6803.5	340
224	OUT219	6788	460
225	OUT220	6772.5	340
226	OUT221	6757	460
227	OUT222	6741.5	340
228	OUT223	6726	460
229	OUT224	6710.5	340
230	OUT225	6695	460
231	OUT226	6679.5	340
232	OUT227	6664	460
233	OUT228	6648.5	340
234	OUT229	6633	460
235	OUT230	6617.5	340
236	OUT231	6602	460
237	OUT232	6586.5	340
238	OUT233	6571	460
239	OUT234	6555.5	340
240	OUT235	6540	460
241	OUT236	6524.5	340
242	OUT237	6509	460
243	OUT238	6493.5	340
244	OUT239	6478	460
245	OUT240	6462.5	340
246	OUT241	6447	460
247	OUT242	6431.5	340
248	OUT243	6416	460
249	OUT244	6400.5	340
250	OUT245	6385	460

No.	Name	X	Y
251	OUT246	6369.5	340
252	OUT247	6354	460
253	OUT248	6338.5	340
254	OUT249	6323	460
255	OUT250	6307.5	340
256	OUT251	6292	460
257	OUT252	6276.5	340
258	OUT253	6261	460
259	OUT254	6245.5	340
260	OUT255	6230	460
261	OUT256	6214.5	340
262	OUT257	6199	460
263	OUT258	6183.5	340
264	OUT259	6168	460
265	OUT260	6152.5	340
266	OUT261	6137	460
267	OUT262	6121.5	340
268	OUT263	6106	460
269	OUT264	6090.5	340
270	OUT265	6075	460
271	OUT266	6059.5	340
272	OUT267	6044	460
273	OUT268	6028.5	340
274	OUT269	6013	460
275	OUT270	5997.5	340
276	OUT271	5982	460
277	OUT272	5966.5	340
278	OUT273	5951	460
279	OUT274	5935.5	340
280	OUT275	5920	460
281	OUT276	5904.5	340
282	OUT277	5889	460
283	OUT278	5873.5	340
284	OUT279	5858	460
285	OUT280	5842.5	340
286	OUT281	5827	460
287	OUT282	5811.5	340
288	OUT283	5796	460
289	OUT284	5780.5	340
290	OUT285	5765	460
291	OUT286	5749.5	340
292	OUT287	5734	460
293	OUT288	5718.5	340
294	OUT289	5703	460
295	OUT290	5687.5	340
296	OUT291	5672	460
297	OUT292	5656.5	340
298	OUT293	5641	460
299	OUT294	5625.5	340
300	OUT295	5610	460

No.	Name	X	Y
301	OUT296	5594.5	340
302	OUT297	5579	460
303	OUT298	5563.5	340
304	OUT299	5548	460
305	OUT300	5532.5	340
306	OUT301	5517	460
307	OUT302	5501.5	340
308	OUT303	5486	460
309	OUT304	5470.5	340
310	OUT305	5455	460
311	OUT306	5439.5	340
312	OUT307	5424	460
313	OUT308	5408.5	340
314	OUT309	5393	460
315	OUT310	5377.5	340
316	OUT311	5362	460
317	OUT312	5346.5	340
318	OUT313	5331	460
319	OUT314	5315.5	340
320	OUT315	5300	460
321	OUT316	5284.5	340
322	OUT317	5269	460
323	OUT318	5253.5	340
324	OUT319	5238	460
325	OUT320	5222.5	340
326	OUT321	5207	460
327	OUT322	5191.5	340
328	OUT323	5176	460
329	OUT324	5160.5	340
330	OUT325	5145	460
331	OUT326	5129.5	340
332	OUT327	5114	460
333	OUT328	5098.5	340
334	OUT329	5083	460
335	OUT330	5067.5	340
336	OUT331	5052	460
337	OUT332	5036.5	340
338	OUT333	5021	460
339	OUT334	5005.5	340
340	OUT335	4990	460
341	OUT336	4974.5	340
342	OUT337	4959	460
343	OUT338	4943.5	340
344	OUT339	4928	460
345	OUT340	4912.5	340
346	OUT341	4897	460
347	OUT342	4881.5	340
348	OUT343	4866	460
349	OUT344	4850.5	340
350	OUT345	4835	460

No.	Name	X	Y
351	OUT346	4819.5	340
352	OUT347	4804	460
353	OUT348	4788.5	340
354	OUT349	4773	460
355	OUT350	4757.5	340
356	OUT351	4742	460
357	OUT352	4726.5	340
358	OUT353	4711	460
359	OUT354	4695.5	340
360	OUT355	4680	460
361	OUT356	4664.5	340
362	OUT357	4649	460
363	OUT358	4633.5	340
364	OUT359	4618	460
365	OUT360	4602.5	340
366	OUT361	4587	460
367	OUT362	4571.5	340
368	OUT363	4556	460
369	OUT364	4540.5	340
370	OUT365	4525	460
371	OUT366	4509.5	340
372	OUT367	4494	460
373	OUT368	4478.5	340
374	OUT369	4463	460
375	OUT370	4447.5	340
376	OUT371	4432	460
377	OUT372	4416.5	340
378	OUT373	4401	460
379	OUT374	4385.5	340
380	OUT375	4370	460
381	OUT376	4354.5	340
382	OUT377	4339	460
383	OUT378	4323.5	340
384	OUT379	4308	460
385	OUT380	4292.5	340
386	OUT381	4277	460
387	OUT382	4261.5	340
388	OUT383	4246	460
389	OUT384	4230.5	340
390	OUT385	4215	460
391	OUT386	4199.5	340
392	OUT387	4184	460
393	OUT388	4168.5	340
394	OUT389	4153	460
395	OUT390	4137.5	340
396	OUT391	4122	460
397	OUT392	4106.5	340
398	OUT393	4091	460
399	OUT394	4075.5	340
400	OUT395	4060	460

No.	Name	X	Y
401	OUT396	4044.5	340
402	OUT397	4029	460
403	OUT398	4013.5	340
404	OUT399	3998	460
405	OUT400	3982.5	340
406	OUT401	3967	460
407	OUT402	3951.5	340
408	OUT403	3936	460
409	OUT404	3920.5	340
410	OUT405	3905	460
411	OUT406	3889.5	340
412	OUT407	3874	460
413	OUT408	3858.5	340
414	OUT409	3843	460
415	OUT410	3827.5	340
416	OUT411	3812	460
417	OUT412	3796.5	340
418	OUT413	3781	460
419	OUT414	3765.5	340
420	OUT415	3750	460
421	OUT416	3734.5	340
422	OUT417	3719	460
423	OUT418	3703.5	340
424	OUT419	3688	460
425	OUT420	3672.5	340
426	OUT421	3657	460
427	OUT422	3641.5	340
428	OUT423	3626	460
429	OUT424	3610.5	340
430	OUT425	3595	460
431	OUT426	3579.5	340
432	OUT427	3564	460
433	OUT428	3548.5	340
434	OUT429	3533	460
435	OUT430	3517.5	340
436	OUT431	3502	460
437	OUT432	3486.5	340
438	OUT433	3471	460
439	OUT434	3455.5	340
440	OUT435	3440	460
441	OUT436	3424.5	340
442	OUT437	3409	460
443	OUT438	3393.5	340
444	OUT439	3378	460
445	OUT440	3362.5	340
446	OUT441	3347	460
447	OUT442	3331.5	340
448	OUT443	3316	460
449	OUT444	3300.5	340
450	OUT445	3285	460

No.	Name	X	Y
451	OUT446	3269.5	340
452	OUT447	3254	460
453	OUT448	3238.5	340
454	OUT449	3223	460
455	OUT450	3207.5	340
456	OUT451	3192	460
457	OUT452	3176.5	340
458	OUT453	3161	460
459	OUT454	3145.5	340
460	OUT455	3130	460
461	OUT456	3114.5	340
462	OUT457	3099	460
463	OUT458	3083.5	340
464	OUT459	3068	460
465	OUT460	3052.5	340
466	OUT461	3037	460
467	OUT462	3021.5	340
468	OUT463	3006	460
469	OUT464	2990.5	340
470	OUT465	2975	460
471	OUT466	2959.5	340
472	OUT467	2944	460
473	OUT468	2928.5	340
474	OUT469	2913	460
475	OUT470	2897.5	340
476	OUT471	2882	460
477	OUT472	2866.5	340
478	OUT473	2851	460
479	OUT474	2835.5	340
480	OUT475	2820	460
481	OUT476	2804.5	340
482	OUT477	2789	460
483	OUT478	2773.5	340
484	OUT479	2758	460
485	OUT480	2742.5	340
486	OUT481	2727	460
487	OUT482	2711.5	340
488	OUT483	2696	460
489	OUT484	2680.5	340
490	OUT485	2665	460
491	OUT486	2649.5	340
492	OUT487	2634	460
493	OUT488	2618.5	340
494	OUT489	2603	460
495	OUT490	2587.5	340
496	OUT491	2572	460
497	OUT492	2556.5	340
498	OUT493	2541	460
499	OUT494	2525.5	340
500	OUT495	2510	460

No.	Name	X	Y
501	OUT496	2494.5	340
502	OUT497	2479	460
503	OUT498	2463.5	340
504	OUT499	2448	460
505	OUT500	2432.5	340
506	OUT501	2417	460
507	OUT502	2401.5	340
508	OUT503	2386	460
509	OUT504	2370.5	340
510	OUT505	2355	460
511	OUT506	2339.5	340
512	OUT507	2324	460
513	OUT508	2308.5	340
514	OUT509	2293	460
515	OUT510	2277.5	340
516	OUT511	2262	460
517	OUT512	2246.5	340
518	OUT513	2231	460
519	OUT514	2215.5	340
520	OUT515	2200	460
521	OUT516	2184.5	340
522	OUT517	2169	460
523	OUT518	2153.5	340
524	OUT519	2138	460
525	OUT520	2122.5	340
526	OUT521	2107	460
527	OUT522	2091.5	340
528	OUT523	2076	460
529	OUT524	2060.5	340
530	OUT525	2045	460
531	OUT526	2029.5	340
532	OUT527	2014	460
533	OUT528	1998.5	340
534	OUT529	1983	460
535	OUT530	1967.5	340
536	OUT531	1952	460
537	OUT532	1936.5	340
538	OUT533	1921	460
539	OUT534	1905.5	340
540	OUT535	1890	460
541	OUT536	1874.5	340
542	OUT537	1859	460
543	OUT538	1843.5	340
544	OUT539	1828	460
545	OUT540	1812.5	340
546	OUT541	1797	460
547	OUT542	1781.5	340
548	OUT543	1766	460
549	OUT544	1750.5	340
550	OUT545	1735	460

No.	Name	X	Y
551	OUT546	1719.5	340
552	OUT547	1704	460
553	OUT548	1688.5	340
554	OUT549	1673	460
555	OUT550	1657.5	340
556	OUT551	1642	460
557	OUT552	1626.5	340
558	OUT553	1611	460
559	OUT554	1595.5	340
560	OUT555	1580	460
561	OUT556	1564.5	340
562	OUT557	1549	460
563	OUT558	1533.5	340
564	OUT559	1518	460
565	OUT560	1502.5	340
566	OUT561	1487	460
567	OUT562	1471.5	340
568	OUT563	1456	460
569	OUT564	1440.5	340
570	OUT565	1425	460
571	OUT566	1409.5	340
572	OUT567	1394	460
573	OUT568	1378.5	340
574	OUT569	1363	460
575	OUT570	1347.5	340
576	OUT571	1332	460
577	OUT572	1316.5	340
578	OUT573	1301	460
579	OUT574	1285.5	340
580	OUT575	1270	460
581	OUT576	1254.5	340
582	OUT577	1239	460
583	OUT578	1223.5	340
584	OUT579	1208	460
585	OUT580	1192.5	340
586	OUT581	1177	460
587	OUT582	1161.5	340
588	OUT583	1146	460
589	OUT584	1130.5	340
590	OUT585	1115	460
591	OUT586	1099.5	340
592	OUT587	1084	460
593	OUT588	1068.5	340
594	OUT589	1053	460
595	OUT590	1037.5	340
596	OUT591	1022	460
597	OUT592	1006.5	340
598	OUT593	991	460
599	OUT594	975.5	340
600	OUT595	960	460

No.	Name	X	Y
601	OUT596	944.5	340
602	OUT597	929	460
603	OUT598	913.5	340
604	OUT599	898	460
605	OUT600	882.5	340
606	Dummy(VT1)	630	485
607	Dummy(VT2)	490	485
608	Dummy(VT3)	350	485
609	Dummy(VT4)	210	485
610	Dummy(VT5)	70	485
611	Dummy(VT6)	-70	485
612	Dummy(VT7)	-210	485
613	Dummy(VT8)	-350	485
614	Dummy(VT9)	-490	485
615	Dummy(VT10)	-630	485
616	OUT601	-882.5	460
617	OUT602	-898	340
618	OUT603	-913.5	460
619	OUT604	-929	340
620	OUT605	-944.5	460
621	OUT606	-960	340
622	OUT607	-975.5	460
623	OUT608	-991	340
624	OUT609	-1006.5	460
625	OUT610	-1022	340
626	OUT611	-1037.5	460
627	OUT612	-1053	340
628	OUT613	-1068.5	460
629	OUT614	-1084	340
630	OUT615	-1099.5	460
631	OUT616	-1115	340
632	OUT617	-1130.5	460
633	OUT618	-1146	340
634	OUT619	-1161.5	460
635	OUT620	-1177	340
636	OUT621	-1192.5	460
637	OUT622	-1208	340
638	OUT623	-1223.5	460
639	OUT624	-1239	340
640	OUT625	-1254.5	460
641	OUT626	-1270	340
642	OUT627	-1285.5	460
643	OUT628	-1301	340
644	OUT629	-1316.5	460
645	OUT630	-1332	340
646	OUT631	-1347.5	460
647	OUT632	-1363	340
648	OUT633	-1378.5	460
649	OUT634	-1394	340
650	OUT635	-1409.5	460

No.	Name	X	Y
651	OUT636	-1425	340
652	OUT637	-1440.5	460
653	OUT638	-1456	340
654	OUT639	-1471.5	460
655	OUT640	-1487	340
656	OUT641	-1502.5	460
657	OUT642	-1518	340
658	OUT643	-1533.5	460
659	OUT644	-1549	340
660	OUT645	-1564.5	460
661	OUT646	-1580	340
662	OUT647	-1595.5	460
663	OUT648	-1611	340
664	OUT649	-1626.5	460
665	OUT650	-1642	340
666	OUT651	-1657.5	460
667	OUT652	-1673	340
668	OUT653	-1688.5	460
669	OUT654	-1704	340
670	OUT655	-1719.5	460
671	OUT656	-1735	340
672	OUT657	-1750.5	460
673	OUT658	-1766	340
674	OUT659	-1781.5	460
675	OUT660	-1797	340
676	OUT661	-1812.5	460
677	OUT662	-1828	340
678	OUT663	-1843.5	460
679	OUT664	-1859	340
680	OUT665	-1874.5	460
681	OUT666	-1890	340
682	OUT667	-1905.5	460
683	OUT668	-1921	340
684	OUT669	-1936.5	460
685	OUT670	-1952	340
686	OUT671	-1967.5	460
687	OUT672	-1983	340
688	OUT673	-1998.5	460
689	OUT674	-2014	340
690	OUT675	-2029.5	460
691	OUT676	-2045	340
692	OUT677	-2060.5	460
693	OUT678	-2076	340
694	OUT679	-2091.5	460
695	OUT680	-2107	340
696	OUT681	-2122.5	460
697	OUT682	-2138	340
698	OUT683	-2153.5	460
699	OUT684	-2169	340
700	OUT685	-2184.5	460

No.	Name	X	Y
701	OUT686	-2200	340
702	OUT687	-2215.5	460
703	OUT688	-2231	340
704	OUT689	-2246.5	460
705	OUT690	-2262	340
706	OUT691	-2277.5	460
707	OUT692	-2293	340
708	OUT693	-2308.5	460
709	OUT694	-2324	340
710	OUT695	-2339.5	460
711	OUT696	-2355	340
712	OUT697	-2370.5	460
713	OUT698	-2386	340
714	OUT699	-2401.5	460
715	OUT700	-2417	340
716	OUT701	-2432.5	460
717	OUT702	-2448	340
718	OUT703	-2463.5	460
719	OUT704	-2479	340
720	OUT705	-2494.5	460
721	OUT706	-2510	340
722	OUT707	-2525.5	460
723	OUT708	-2541	340
724	OUT709	-2556.5	460
725	OUT710	-2572	340
726	OUT711	-2587.5	460
727	OUT712	-2603	340
728	OUT713	-2618.5	460
729	OUT714	-2634	340
730	OUT715	-2649.5	460
731	OUT716	-2665	340
732	OUT717	-2680.5	460
733	OUT718	-2696	340
734	OUT719	-2711.5	460
735	OUT720	-2727	340
736	OUT721	-2742.5	460
737	OUT722	-2758	340
738	OUT723	-2773.5	460
739	OUT724	-2789	340
740	OUT725	-2804.5	460
741	OUT726	-2820	340
742	OUT727	-2835.5	460
743	OUT728	-2851	340
744	OUT729	-2866.5	460
745	OUT730	-2882	340
746	OUT731	-2897.5	460
747	OUT732	-2913	340
748	OUT733	-2928.5	460
749	OUT734	-2944	340
750	OUT735	-2959.5	460

No.	Name	X	Y
751	OUT736	-2975	340
752	OUT737	-2990.5	460
753	OUT738	-3006	340
754	OUT739	-3021.5	460
755	OUT740	-3037	340
756	OUT741	-3052.5	460
757	OUT742	-3068	340
758	OUT743	-3083.5	460
759	OUT744	-3099	340
760	OUT745	-3114.5	460
761	OUT746	-3130	340
762	OUT747	-3145.5	460
763	OUT748	-3161	340
764	OUT749	-3176.5	460
765	OUT750	-3192	340
766	OUT751	-3207.5	460
767	OUT752	-3223	340
768	OUT753	-3238.5	460
769	OUT754	-3254	340
770	OUT755	-3269.5	460
771	OUT756	-3285	340
772	OUT757	-3300.5	460
773	OUT758	-3316	340
774	OUT759	-3331.5	460
775	OUT760	-3347	340
776	OUT761	-3362.5	460
777	OUT762	-3378	340
778	OUT763	-3393.5	460
779	OUT764	-3409	340
780	OUT765	-3424.5	460
781	OUT766	-3440	340
782	OUT767	-3455.5	460
783	OUT768	-3471	340
784	OUT769	-3486.5	460
785	OUT770	-3502	340
786	OUT771	-3517.5	460
787	OUT772	-3533	340
788	OUT773	-3548.5	460
789	OUT774	-3564	340
790	OUT775	-3579.5	460
791	OUT776	-3595	340
792	OUT777	-3610.5	460
793	OUT778	-3626	340
794	OUT779	-3641.5	460
795	OUT780	-3657	340
796	OUT781	-3672.5	460
797	OUT782	-3688	340
798	OUT783	-3703.5	460
799	OUT784	-3719	340
800	OUT785	-3734.5	460

No.	Name	X	Y
801	OUT786	-3750	340
802	OUT787	-3765.5	460
803	OUT788	-3781	340
804	OUT789	-3796.5	460
805	OUT790	-3812	340
806	OUT791	-3827.5	460
807	OUT792	-3843	340
808	OUT793	-3858.5	460
809	OUT794	-3874	340
810	OUT795	-3889.5	460
811	OUT796	-3905	340
812	OUT797	-3920.5	460
813	OUT798	-3936	340
814	OUT799	-3951.5	460
815	OUT800	-3967	340
816	OUT801	-3982.5	460
817	OUT802	-3998	340
818	OUT803	-4013.5	460
819	OUT804	-4029	340
820	OUT805	-4044.5	460
821	OUT806	-4060	340
822	OUT807	-4075.5	460
823	OUT808	-4091	340
824	OUT809	-4106.5	460
825	OUT810	-4122	340
826	OUT811	-4137.5	460
827	OUT812	-4153	340
828	OUT813	-4168.5	460
829	OUT814	-4184	340
830	OUT815	-4199.5	460
831	OUT816	-4215	340
832	OUT817	-4230.5	460
833	OUT818	-4246	340
834	OUT819	-4261.5	460
835	OUT820	-4277	340
836	OUT821	-4292.5	460
837	OUT822	-4308	340
838	OUT823	-4323.5	460
839	OUT824	-4339	340
840	OUT825	-4354.5	460
841	OUT826	-4370	340
842	OUT827	-4385.5	460
843	OUT828	-4401	340
844	OUT829	-4416.5	460
845	OUT830	-4432	340
846	OUT831	-4447.5	460
847	OUT832	-4463	340
848	OUT833	-4478.5	460
849	OUT834	-4494	340
850	OUT835	-4509.5	460

No.	Name	X	Y
851	OUT836	-4525	340
852	OUT837	-4540.5	460
853	OUT838	-4556	340
854	OUT839	-4571.5	460
855	OUT840	-4587	340
856	OUT841	-4602.5	460
857	OUT842	-4618	340
858	OUT843	-4633.5	460
859	OUT844	-4649	340
860	OUT845	-4664.5	460
861	OUT846	-4680	340
862	OUT847	-4695.5	460
863	OUT848	-4711	340
864	OUT849	-4726.5	460
865	OUT850	-4742	340
866	OUT851	-4757.5	460
867	OUT852	-4773	340
868	OUT853	-4788.5	460
869	OUT854	-4804	340
870	OUT855	-4819.5	460
871	OUT856	-4835	340
872	OUT857	-4850.5	460
873	OUT858	-4866	340
874	OUT859	-4881.5	460
875	OUT860	-4897	340
876	OUT861	-4912.5	460
877	OUT862	-4928	340
878	OUT863	-4943.5	460
879	OUT864	-4959	340
880	OUT865	-4974.5	460
881	OUT866	-4990	340
882	OUT867	-5005.5	460
883	OUT868	-5021	340
884	OUT869	-5036.5	460
885	OUT870	-5052	340
886	OUT871	-5067.5	460
887	OUT872	-5083	340
888	OUT873	-5098.5	460
889	OUT874	-5114	340
890	OUT875	-5129.5	460
891	OUT876	-5145	340
892	OUT877	-5160.5	460
893	OUT878	-5176	340
894	OUT879	-5191.5	460
895	OUT880	-5207	340
896	OUT881	-5222.5	460
897	OUT882	-5238	340
898	OUT883	-5253.5	460
899	OUT884	-5269	340
900	OUT885	-5284.5	460

No.	Name	X	Y
901	OUT886	-5300	340
902	OUT887	-5315.5	460
903	OUT888	-5331	340
904	OUT889	-5346.5	460
905	OUT890	-5362	340
906	OUT891	-5377.5	460
907	OUT892	-5393	340
908	OUT893	-5408.5	460
909	OUT894	-5424	340
910	OUT895	-5439.5	460
911	OUT896	-5455	340
912	OUT897	-5470.5	460
913	OUT898	-5486	340
914	OUT899	-5501.5	460
915	OUT900	-5517	340
916	OUT901	-5532.5	460
917	OUT902	-5548	340
918	OUT903	-5563.5	460
919	OUT904	-5579	340
920	OUT905	-5594.5	460
921	OUT906	-5610	340
922	OUT907	-5625.5	460
923	OUT908	-5641	340
924	OUT909	-5656.5	460
925	OUT910	-5672	340
926	OUT911	-5687.5	460
927	OUT912	-5703	340
928	OUT913	-5718.5	460
929	OUT914	-5734	340
930	OUT915	-5749.5	460
931	OUT916	-5765	340
932	OUT917	-5780.5	460
933	OUT918	-5796	340
934	OUT919	-5811.5	460
935	OUT920	-5827	340
936	OUT921	-5842.5	460
937	OUT922	-5858	340
938	OUT923	-5873.5	460
939	OUT924	-5889	340
940	OUT925	-5904.5	460
941	OUT926	-5920	340
942	OUT927	-5935.5	460
943	OUT928	-5951	340
944	OUT929	-5966.5	460
945	OUT930	-5982	340
946	OUT931	-5997.5	460
947	OUT932	-6013	340
948	OUT933	-6028.5	460
949	OUT934	-6044	340
950	OUT935	-6059.5	460

No.	Name	X	Y
951	OUT936	-6075	340
952	OUT937	-6090.5	460
953	OUT938	-6106	340
954	OUT939	-6121.5	460
955	OUT940	-6137	340
956	OUT941	-6152.5	460
957	OUT942	-6168	340
958	OUT943	-6183.5	460
959	OUT944	-6199	340
960	OUT945	-6214.5	460
961	OUT946	-6230	340
962	OUT947	-6245.5	460
963	OUT948	-6261	340
964	OUT949	-6276.5	460
965	OUT950	-6292	340
966	OUT951	-6307.5	460
967	OUT952	-6323	340
968	OUT953	-6338.5	460
969	OUT954	-6354	340
970	OUT955	-6369.5	460
971	OUT956	-6385	340
972	OUT957	-6400.5	460
973	OUT958	-6416	340
974	OUT959	-6431.5	460
975	OUT960	-6447	340
976	OUT961	-6462.5	460
977	OUT962	-6478	340
978	OUT963	-6493.5	460
979	OUT964	-6509	340
980	OUT965	-6524.5	460
981	OUT966	-6540	340
982	OUT967	-6555.5	460
983	OUT968	-6571	340
984	OUT969	-6586.5	460
985	OUT970	-6602	340
986	OUT971	-6617.5	460
987	OUT972	-6633	340
988	OUT973	-6648.5	460
989	OUT974	-6664	340
990	OUT975	-6679.5	460
991	OUT976	-6695	340
992	OUT977	-6710.5	460
993	OUT978	-6726	340
994	OUT979	-6741.5	460
995	OUT980	-6757	340
996	OUT981	-6772.5	460
997	OUT982	-6788	340
998	OUT983	-6803.5	460
999	OUT984	-6819	340
1000	OUT985	-6834.5	460

No.	Name	X	Y
1001	OUT986	-6850	340
1002	OUT987	-6865.5	460
1003	OUT988	-6881	340
1004	OUT989	-6896.5	460
1005	OUT990	-6912	340
1006	OUT991	-6927.5	460
1007	OUT992	-6943	340
1008	OUT993	-6958.5	460
1009	OUT994	-6974	340
1010	OUT995	-6989.5	460
1011	OUT996	-7005	340
1012	OUT997	-7020.5	460
1013	OUT998	-7036	340
1014	OUT999	-7051.5	460
1015	OUT1000	-7067	340
1016	OUT1001	-7082.5	460
1017	OUT1002	-7098	340
1018	OUT1003	-7113.5	460
1019	OUT1004	-7129	340
1020	OUT1005	-7144.5	460
1021	OUT1006	-7160	340
1022	OUT1007	-7175.5	460
1023	OUT1008	-7191	340
1024	OUT1009	-7206.5	460
1025	OUT1010	-7222	340
1026	OUT1011	-7237.5	460
1027	OUT1012	-7253	340
1028	OUT1013	-7268.5	460
1029	OUT1014	-7284	340
1030	OUT1015	-7299.5	460
1031	OUT1016	-7315	340
1032	OUT1017	-7330.5	460
1033	OUT1018	-7346	340
1034	OUT1019	-7361.5	460
1035	OUT1020	-7377	340
1036	OUT1021	-7392.5	460
1037	OUT1022	-7408	340
1038	OUT1023	-7423.5	460
1039	OUT1024	-7439	340
1040	OUT1025	-7454.5	460
1041	OUT1026	-7470	340
1042	OUT1027	-7485.5	460
1043	OUT1028	-7501	340
1044	OUT1029	-7516.5	460
1045	OUT1030	-7532	340
1046	OUT1031	-7547.5	460
1047	OUT1032	-7563	340
1048	OUT1033	-7578.5	460
1049	OUT1034	-7594	340
1050	OUT1035	-7609.5	460

No.	Name	X	Y
1051	OUT1036	-7625	340
1052	OUT1037	-7640.5	460
1053	OUT1038	-7656	340
1054	OUT1039	-7671.5	460
1055	OUT1040	-7687	340
1056	OUT1041	-7702.5	460
1057	OUT1042	-7718	340
1058	OUT1043	-7733.5	460
1059	OUT1044	-7749	340
1060	OUT1045	-7764.5	460
1061	OUT1046	-7780	340
1062	OUT1047	-7795.5	460
1063	OUT1048	-7811	340
1064	OUT1049	-7826.5	460
1065	OUT1050	-7842	340
1066	OUT1051	-7857.5	460
1067	OUT1052	-7873	340
1068	OUT1053	-7888.5	460
1069	OUT1054	-7904	340
1070	OUT1055	-7919.5	460
1071	OUT1056	-7935	340
1072	OUT1057	-7950.5	460
1073	OUT1058	-7966	340
1074	OUT1059	-7981.5	460
1075	OUT1060	-7997	340
1076	OUT1061	-8012.5	460
1077	OUT1062	-8028	340
1078	OUT1063	-8043.5	460
1079	OUT1064	-8059	340
1080	OUT1065	-8074.5	460
1081	OUT1066	-8090	340
1082	OUT1067	-8105.5	460
1083	OUT1068	-8121	340
1084	OUT1069	-8136.5	460
1085	OUT1070	-8152	340
1086	OUT1071	-8167.5	460
1087	OUT1072	-8183	340
1088	OUT1073	-8198.5	460
1089	OUT1074	-8214	340
1090	OUT1075	-8229.5	460
1091	OUT1076	-8245	340
1092	OUT1077	-8260.5	460
1093	OUT1078	-8276	340
1094	OUT1079	-8291.5	460
1095	OUT1080	-8307	340
1096	OUT1081	-8322.5	460
1097	OUT1082	-8338	340
1098	OUT1083	-8353.5	460
1099	OUT1084	-8369	340
1100	OUT1085	-8384.5	460

No.	Name	X	Y
1101	OUT1086	-8400	340
1102	OUT1087	-8415.5	460
1103	OUT1088	-8431	340
1104	OUT1089	-8446.5	460
1105	OUT1090	-8462	340
1106	OUT1091	-8477.5	460
1107	OUT1092	-8493	340
1108	OUT1093	-8508.5	460
1109	OUT1094	-8524	340
1110	OUT1095	-8539.5	460
1111	OUT1096	-8555	340
1112	OUT1097	-8570.5	460
1113	OUT1098	-8586	340
1114	OUT1099	-8601.5	460
1115	OUT1100	-8617	340
1116	OUT1101	-8632.5	460
1117	OUT1102	-8648	340
1118	OUT1103	-8663.5	460
1119	OUT1104	-8679	340
1120	OUT1105	-8694.5	460
1121	OUT1106	-8710	340
1122	OUT1107	-8725.5	460
1123	OUT1108	-8741	340
1124	OUT1109	-8756.5	460
1125	OUT1110	-8772	340
1126	OUT1111	-8787.5	460
1127	OUT1112	-8803	340
1128	OUT1113	-8818.5	460
1129	OUT1114	-8834	340
1130	OUT1115	-8849.5	460
1131	OUT1116	-8865	340
1132	OUT1117	-8880.5	460
1133	OUT1118	-8896	340
1134	OUT1119	-8911.5	460
1135	OUT1120	-8927	340
1136	OUT1121	-8942.5	460
1137	OUT1122	-8958	340
1138	OUT1123	-8973.5	460
1139	OUT1124	-8989	340
1140	OUT1125	-9004.5	460
1141	OUT1126	-9020	340
1142	OUT1127	-9035.5	460
1143	OUT1128	-9051	340
1144	OUT1129	-9066.5	460
1145	OUT1130	-9082	340
1146	OUT1131	-9097.5	460
1147	OUT1132	-9113	340
1148	OUT1133	-9128.5	460
1149	OUT1134	-9144	340
1150	OUT1135	-9159.5	460

No.	Name	X	Y
1151	OUT1136	-9175	340
1152	OUT1137	-9190.5	460
1153	OUT1138	-9206	340
1154	OUT1139	-9221.5	460
1155	OUT1140	-9237	340
1156	OUT1141	-9252.5	460
1157	OUT1142	-9268	340
1158	OUT1143	-9283.5	460
1159	OUT1144	-9299	340
1160	OUT1145	-9314.5	460
1161	OUT1146	-9330	340
1162	OUT1147	-9345.5	460
1163	OUT1148	-9361	340
1164	OUT1149	-9376.5	460
1165	OUT1150	-9392	340
1166	OUT1151	-9407.5	460
1167	OUT1152	-9423	340
1168	OUT1153	-9438.5	460
1169	OUT1154	-9454	340
1170	OUT1155	-9469.5	460
1171	OUT1156	-9485	340
1172	OUT1157	-9500.5	460
1173	OUT1158	-9516	340
1174	OUT1159	-9531.5	460
1175	OUT1160	-9547	340
1176	OUT1161	-9562.5	460
1177	OUT1162	-9578	340
1178	OUT1163	-9593.5	460
1179	OUT1164	-9609	340
1180	OUT1165	-9624.5	460
1181	OUT1166	-9640	340
1182	OUT1167	-9655.5	460
1183	OUT1168	-9671	340
1184	OUT1169	-9686.5	460
1185	OUT1170	-9702	340
1186	OUT1171	-9717.5	460
1187	OUT1172	-9733	340
1188	OUT1173	-9748.5	460
1189	OUT1174	-9764	340
1190	OUT1175	-9779.5	460
1191	OUT1176	-9795	340
1192	OUT1177	-9810.5	460
1193	OUT1178	-9826	340
1194	OUT1179	-9841.5	460
1195	OUT1180	-9857	340
1196	OUT1181	-9872.5	460
1197	OUT1182	-9888	340
1198	OUT1183	-9903.5	460
1199	OUT1184	-9919	340
1200	OUT1185	-9934.5	460

No.	Name	X	Y
1201	OUT1186	-9950	340
1202	OUT1187	-9965.5	460
1203	OUT1188	-9981	340
1204	OUT1189	-9996.5	460
1205	OUT1190	-10012	340
1206	OUT1191	-10027.5	460
1207	OUT1192	-10043	340
1208	OUT1193	-10058.5	460
1209	OUT1194	-10074	340
1210	OUT1195	-10089.5	460
1211	OUT1196	-10105	340
1212	OUT1197	-10120.5	460
1213	OUT1198	-10136	340
1214	OUT1199	-10151.5	460
1215	OUT1200	-10167	340
1216	RPO2	-10228	460
1217	RPI2	-10259	460
1218	PASS2	-10290	460
1219	PASS2	-10321	460
1220	DUMMY	-10370	460
1221	OEV	-10370	-15
1222	OEV	-10300	-15
1223	UDP	-10370	-85
1224	UDP	-10300	-85
1225	CKV	-10370	-155
1226	CKV	-10300	-155
1227	STVD	-10370	-225
1228	STVD	-10300	-225
1229	STVU	-10370	-295
1230	STVU	-10300	-295
1231	DUMMY	-10370	-465
1232	PASS2	-10115	-465
1233	PASS2	-10045	-465
1234	DUMMY	-9975	-465
1235	DUMMY	-9905	-465
1236	POL2	-9835	-465
1237	POL2	-9765	-465
1238	POL2	-9695	-465
1239	POL2	-9625	-465
1240	STV2	-9555	-465
1241	STV2	-9485	-465
1242	STV2	-9415	-465
1243	STV2	-9345	-465
1244	DIO2	-9275	-465
1245	DIO2	-9205	-465
1246	DIO2	-9135	-465
1247	DIO2	-9065	-465
1248	DUMMY	-8995	-465
1249	DUMMY	-8925	-465
1250	VDDA	-8855	-465

No.	Name	X	Y
1251	VDDA	-8785	-465
1252	VDDA	-8715	-465
1253	VDDA	-8645	-465
1254	VDDA	-8575	-465
1255	VDDA	-8505	-465
1256	VDDA	-8435	-465
1257	VDDA	-8365	-465
1258	VSS	-8295	-465
1259	VSS	-8225	-465
1260	VSS	-8155	-465
1261	VSS	-8085	-465
1262	VSS	-8015	-465
1263	VSS	-7945	-465
1264	VSS	-7875	-465
1265	VSS	-7805	-465
1266	DUMMY	-7735	-465
1267	DUMMY	-7665	-465
1268	V10	-7595	-465
1269	V10	-7525	-465
1270	V10	-7455	-465
1271	V10	-7385	-465
1272	V9	-7315	-465
1273	V9	-7245	-465
1274	V9	-7175	-465
1275	V9	-7105	-465
1276	V8	-7035	-465
1277	V8	-6965	-465
1278	V8	-6895	-465
1279	V8	-6825	-465
1280	V7	-6755	-465
1281	V7	-6685	-465
1282	V7	-6615	-465
1283	V7	-6545	-465
1284	V6	-6475	-465
1285	V6	-6405	-465
1286	V6	-6335	-465
1287	V6	-6265	-465
1288	DUMMY	-6195	-465
1289	DUMMY	-6125	-465
1290	LR	-6055	-465
1291	LR	-5985	-465
1292	RESL2	-5915	-465
1293	RESL2	-5845	-465
1294	RESL1	-5775	-465
1295	RESL1	-5705	-465
1296	RESL0	-5635	-465
1297	RESL0	-5565	-465
1298	ID1	-5495	-465
1299	ID1	-5425	-465
1300	ID0	-5355	-465

No.	Name	X	Y
1301	ID0	-5285	-465
1302	DUMMY	-5215	-465
1303	DUMMY	-5145	-465
1304	HS	-5075	-465
1305	HS	-5005	-465
1306	VS	-4935	-465
1307	VS	-4865	-465
1308	REV	-4795	-465
1309	REV	-4725	-465
1310	LD	-4655	-465
1311	LD	-4585	-465
1312	DEN	-4515	-465
1313	DEN	-4445	-465
1314	DUMMY	-4375	-465
1315	DUMMY	-4305	-465
1316	DUMMY	-4235	-465
1317	DUMMY	-4165	-465
1318	DUMMY	-4095	-465
1319	DUMMY	-4025	-465
1320	DUMMY	-3955	-465
1321	DUMMY	-3885	-465
1322	DUMMY	-3815	-465
1323	DUMMY	-3745	-465
1324	DUMMY	-3675	-465
1325	DUMMY	-3605	-465
1326	DUMMY	-3535	-465
1327	DUMMY	-3465	-465
1328	DUMMY	-3395	-465
1329	DUMMY	-3325	-465
1330	DUMMY	-3255	-465
1331	DUMMY	-3185	-465
1332	TP3	-3115	-465
1333	TP3	-3045	-465
1334	TP3	-2975	-465
1335	TP3	-2905	-465
1336	TP2	-2835	-465
1337	TP2	-2765	-465
1338	TP2	-2695	-465
1339	TP2	-2625	-465
1340	TP1	-2555	-465
1341	TP1	-2485	-465
1342	TP1	-2415	-465
1343	TP1	-2345	-465
1344	TP0	-2275	-465
1345	TP0	-2205	-465
1346	TP0	-2135	-465
1347	TP0	-2065	-465
1348	DUMMY	-1995	-465
1349	D27	-1925	-465
1350	D27	-1855	-465

No.	Name	X	Y
1351	D26	-1785	-465
1352	D26	-1715	-465
1353	D25	-1645	-465
1354	D25	-1575	-465
1355	D24	-1505	-465
1356	D24	-1435	-465
1357	D23	-1365	-465
1358	D23	-1295	-465
1359	D22	-1225	-465
1360	D22	-1155	-465
1361	D21	-1085	-465
1362	D21	-1015	-465
1363	D20	-945	-465
1364	D20	-875	-465
1365	SPEN	-805	-465
1366	SPEN	-735	-465
1367	SPEN	-665	-465
1368	SPEN	-595	-465
1369	SDO	-525	-465
1370	SDO	-455	-465
1371	SDI	-385	-465
1372	SDI	-315	-465
1373	SPCK	-245	-465
1374	SPCK	-175	-465
1375	SPCK	-105	-465
1376	SPCK	-35	-465
1377	CLK	35	-465
1378	CLK	105	-465
1379	DUMMY	175	-465
1380	D17	245	-465
1381	D17	315	-465
1382	D16	385	-465
1383	D16	455	-465
1384	D15	525	-465
1385	D15	595	-465
1386	D14	665	-465
1387	D14	735	-465
1388	DUMMY	805	-465
1389	DUMMY	875	-465
1390	D13	945	-465
1391	D13	1015	-465
1392	D12	1085	-465
1393	D12	1155	-465
1394	D11	1225	-465
1395	D11	1295	-465
1396	D10	1365	-465
1397	D10	1435	-465
1398	DUMMY	1505	-465
1399	DUMMY	1575	-465
1400	D07	1645	-465

No.	Name	X	Y
1401	D07	1715	-465
1402	D06	1785	-465
1403	D06	1855	-465
1404	D05	1925	-465
1405	D05	1995	-465
1406	D04	2065	-465
1407	D04	2135	-465
1408	DUMMY	2205	-465
1409	DUMMY	2275	-465
1410	D03	2345	-465
1411	D03	2415	-465
1412	D02	2485	-465
1413	D02	2555	-465
1414	D01	2625	-465
1415	D01	2695	-465
1416	D00	2765	-465
1417	D00	2835	-465
1418	DUMMY	2905	-465
1419	DUMMY	2975	-465
1420	VCC	3045	-465
1421	VCC	3115	-465
1422	VCC	3185	-465
1423	VCC	3255	-465
1424	VCC	3325	-465
1425	VCC	3395	-465
1426	VCC	3465	-465
1427	VCC	3535	-465
1428	GND	3605	-465
1429	GND	3675	-465
1430	GND	3745	-465
1431	GND	3815	-465
1432	GND	3885	-465
1433	GND	3955	-465
1434	GND	4025	-465
1435	GND	4095	-465
1436	DUMMY	4165	-465
1437	DUMMY	4235	-465
1438	CS	4305	-465
1439	CS	4375	-465
1440	STB	4445	-465
1441	STB	4515	-465
1442	VSET	4585	-465
1443	VSET	4655	-465
1444	EDGSL	4725	-465
1445	EDGSL	4795	-465
1446	ENREOP	4865	-465
1447	ENREOP	4935	-465
1448	DUMMY	5005	-465
1449	DUMMY	5075	-465
1450	TEST1	5145	-465

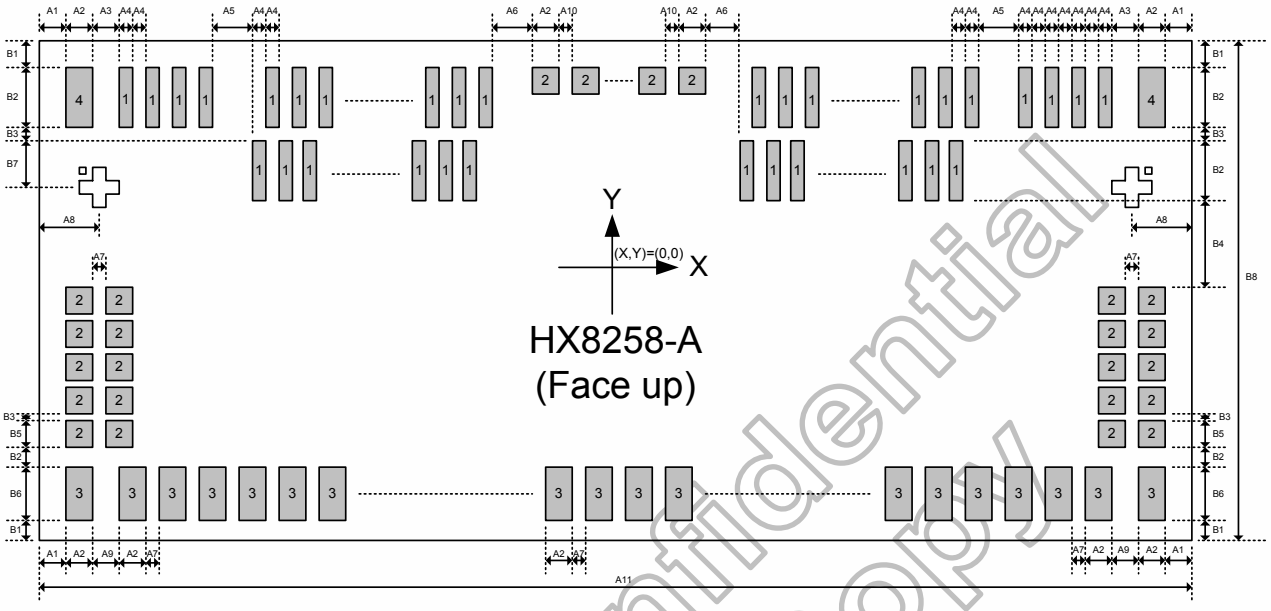
No.	Name	X	Y
1451	TEST1	5215	-465
1452	TEST0	5285	-465
1453	TEST0	5355	-465
1454	TESTG1	5425	-465
1455	TESTG1	5495	-465
1456	TESTG0	5565	-465
1457	TESTG0	5635	-465
1458	RESETB	5705	-465
1459	RESETB	5775	-465
1460	TEN	5845	-465
1461	TEN	5915	-465
1462	UD	5985	-465
1463	UD	6055	-465
1464	DUMMY	6125	-465
1465	DUMMY	6195	-465
1466	V5	6265	-465
1467	V5	6335	-465
1468	V5	6405	-465
1469	V5	6475	-465
1470	V4	6545	-465
1471	V4	6615	-465
1472	V4	6685	-465
1473	V4	6755	-465
1474	V3	6825	-465
1475	V3	6895	-465
1476	V3	6965	-465
1477	V3	7035	-465
1478	V2	7105	-465
1479	V2	7175	-465
1480	V2	7245	-465
1481	V2	7315	-465
1482	V1	7385	-465
1483	V1	7455	-465
1484	V1	7525	-465
1485	V1	7595	-465
1486	DUMMY	7665	-465
1487	DUMMY	7735	-465
1488	VDDA	7805	-465
1489	VDDA	7875	-465
1490	VDDA	7945	-465
1491	VDDA	8015	-465
1492	VDDA	8085	-465
1493	VDDA	8155	-465
1494	VDDA	8225	-465
1495	VDDA	8295	-465
1496	VSS	8365	-465
1497	VSS	8435	-465
1498	VSS	8505	-465
1499	VSS	8575	-465
1500	VSS	8645	-465

No.	Name	X	Y
1501	VSS	8715	-465
1502	VSS	8785	-465
1503	VSS	8855	-465
1504	DUMMY	8925	-465
1505	DUMMY	8995	-465
1506	DIO1	9065	-465
1507	DIO1	9135	-465
1508	DIO1	9205	-465
1509	DIO1	9275	-465
1510	STV1	9345	-465
1511	STV1	9415	-465
1512	STV1	9485	-465
1513	STV1	9555	-465
1514	POL1	9625	-465
1515	POL1	9695	-465
1516	POL1	9765	-465
1517	POL1	9835	-465
1518	DUMMY	9905	-465
1519	DUMMY	9975	-465
1520	PASS1	10045	-465
1521	PASS1	10115	-465
1522	DUMMY	10370	-465
1523	STVU	10300	-295
1524	STVU	10370	-295
1525	STVD	10300	-225
1526	STVD	10370	-225
1527	CKV	10300	-155
1528	CKV	10370	-155
1529	UDB	10300	-85
1530	UDB	10370	-85
1531	OEV	10300	-15
1532	OEV	10370	-15

Name	X	Y
Alignment_Mark_R	10342.5	280.5
Alignment_Mark_L	-10342.5	280.5

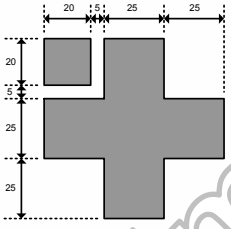
12. Bump Mask information

- Chip size : 20920 um x 1150 um (include scribe line)
- Bump height : 15 um ± 3 um
- Bump hardness : 65 Hv ± 15 Hv

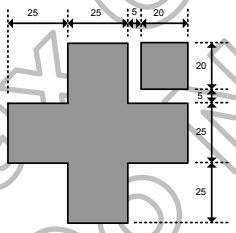


Alignment mark
(unit : um)

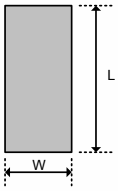
Left side



Right side



Bump PAD size



1 W x L = 15.5um x 100um
2 W x L = 50um x 50um
3 W x L = 50um x 90um
4 W x L = 50um x 100um

Symbol	Dimension (um)
A1	65
A2	50
A3	16.25
A4	15.5
A5	45.5
A6	219.75
A7	20
A8	117.5
A9	205
A10	90
A11	20920

Symbol	Dimension (um)
B1	65
B2	100
B3	20
B4	280
B5	50
B6	90
B7	109.5
B8	1150

13. Ordering Information

PART NO.	PACKAGE TYPE
HX8258-A000PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400μm)

14. Revision History

Version	Date	Description of Changes
01	2007/12/13	New Setup
02	2008/01/14	Page 37 Add the limit value for Gamma correction voltage input.
	2008/03/07	Page 38 Add repair OP electrical characteristics.
03	2008/07/03	Page 37 Modify pull high and pull low resistance value.
	2008/07/16	Page 71 Modify Bump hardness.
04	2009/04/14	Page 39 ~ Page 43 Add notes for DE frame blanking (T_{DEB}).