



DATA SHEET

(DOC No. HX8278-A-LT-DS)

HX8278-A-LT

TFT LCD Single Chip Digital
Driver

Preliminary version 00 March, 2017

HX8278-A-LT

TFT LCD Single Chip Digital Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

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HX8278-A-LT

480x840 TFT LCD Single Chip Digital Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

Preliminary Version 00

March, 2017

1. General Description

HX8278-A-LT is a highly integrated single chip driver with built-in timing controller for color TFT LCD panels. This driver supports adjustable display resolutions, with functions of 480-channel 8-bit dot-inversion source driver, 840-channel gate driver, timing controller, power circuits, I2C interface (I2C) or serial peripheral interface (SPI). This driver is for industrial or automotive products.

2. Features

General:

- COG (Chip on glass) package
- Support normally black and normally white panels
- 8-bit per color true resolution (16.7 million colors)
- Closed loop for IC bonding resistance measurement
- On-chip OTP (one-time-programming) memory for all registers
- External EEPROM for all registers
- GAS function (Gate all select) to prevent image sticking when abnormal power off
- CRC check function
- Touch panel synchronization signal TPSYNC
- Failure detection signal FFLAG
- AEC-Q100 compliant for automotive applications

Timing controller:

- Panel resolution: 480RGBx272, 400RGBx240, 360RGBx240, 320RGBx240, or adjustable resolutions
- Support 24/18/16-bit parallel TTL, 8-bit serial TTL, 4/3/2-lane LVDS input
- Support Sync mode and DE mode
- 4-wire SPI, 3-wire SPI or I2C command setting
- Digital gamma processing and contrast with color shift / brightness control on RGB data
- Internal pattern generator with basic patterns in built-in self testing (BIST) mode
- Self protection function for missing CLK, HS, VS or DE input
- Dynamic VCOM/VGH/VGL/VGMPH/VGMPL/VGMNH/VGMNL and digital gamma settings controlled by external temperature sensor

Source driver:

- Maximum 480-channel source output for 120RGB to 480RGB resolutions
- Source driver output with 8-bit DAC (256 levels) and 2-bit dithering
- Dot / 3 dot / 6 dot and column inversion of triple gate driving
- Maximum $\pm 6.7V$ output swing
- Right and left shift capability
- 2 layer staggered pad with 14 μm pitch

Gate driver:

- Maximum 840-channel gate output for 120 to 280 display lines.
- Six scan types
- Forward and reversed shift capability

Power:

- Main power supply VDD=3.0V to 3.6V
- Built-in charge pumps for source / gamma power supplies AVDDP and AVDDN
- Built-in charge pumps for gate driver operation voltages VGH and VGL
- Built-in regulators for gamma reference and TCON power supplies
- Built-in driving circuit for VCOM

Others:

- Built-in oscillator for BIST and Self protection function operation

3. Block Diagram and DC/DC Construction

3.1 Block diagram

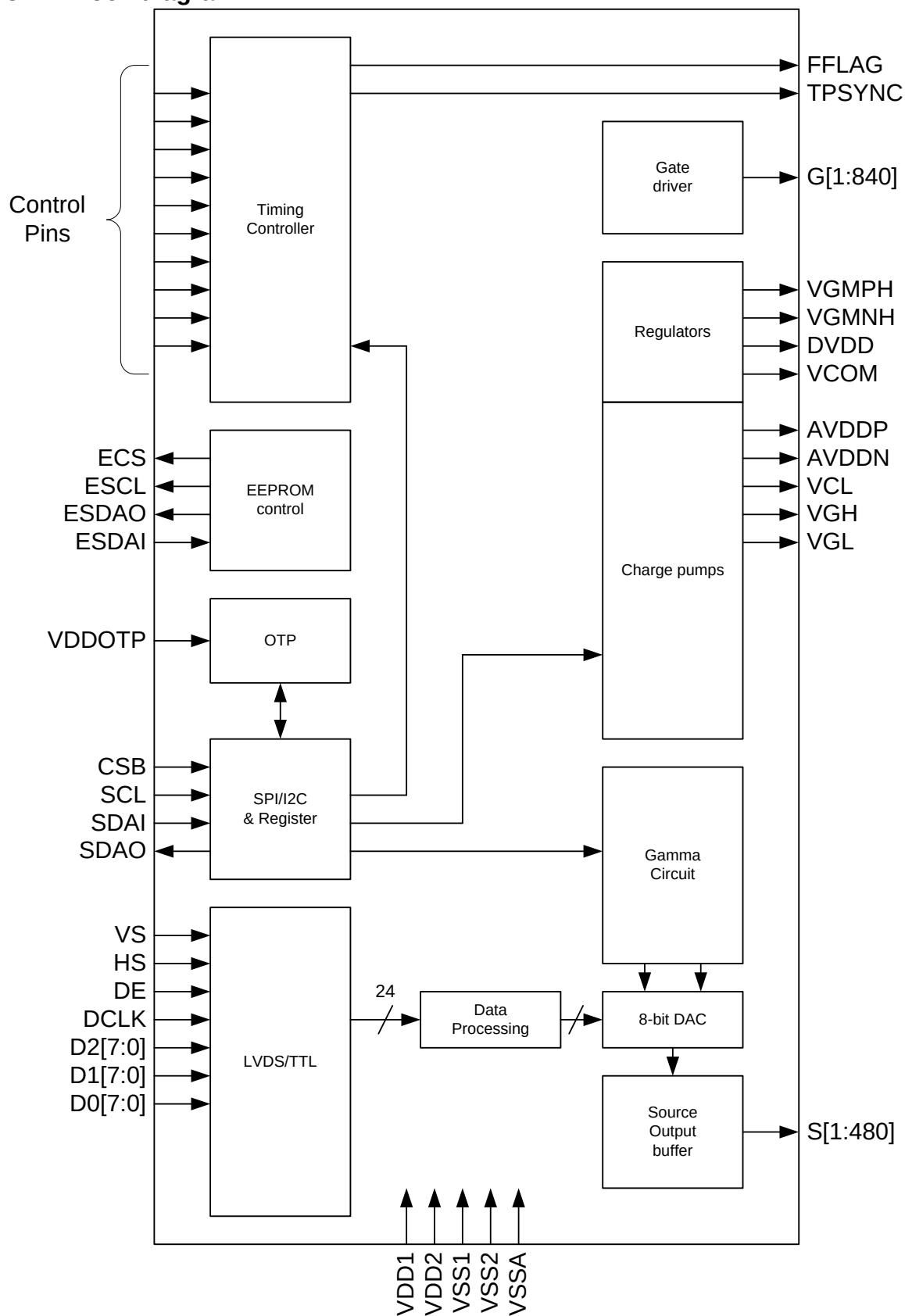


Figure 3.1: Block diagram

3.2 DC/DC voltage construction

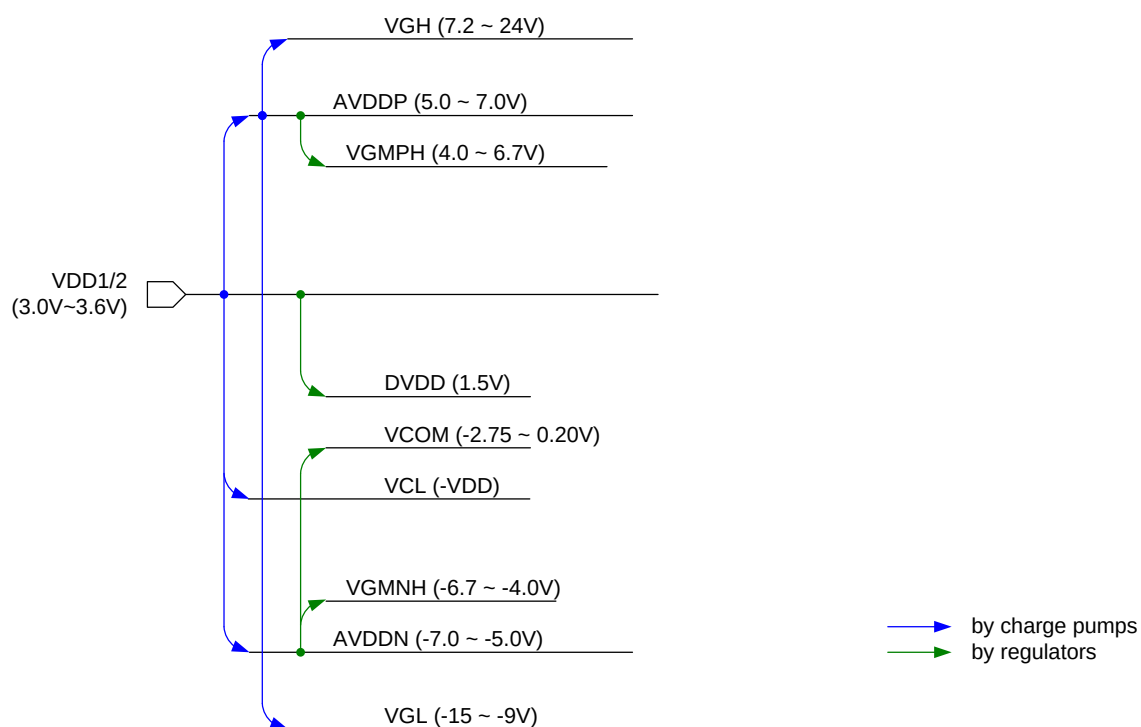


Figure 3.2: DC/DC voltage construction

3.3 Circuit for external components

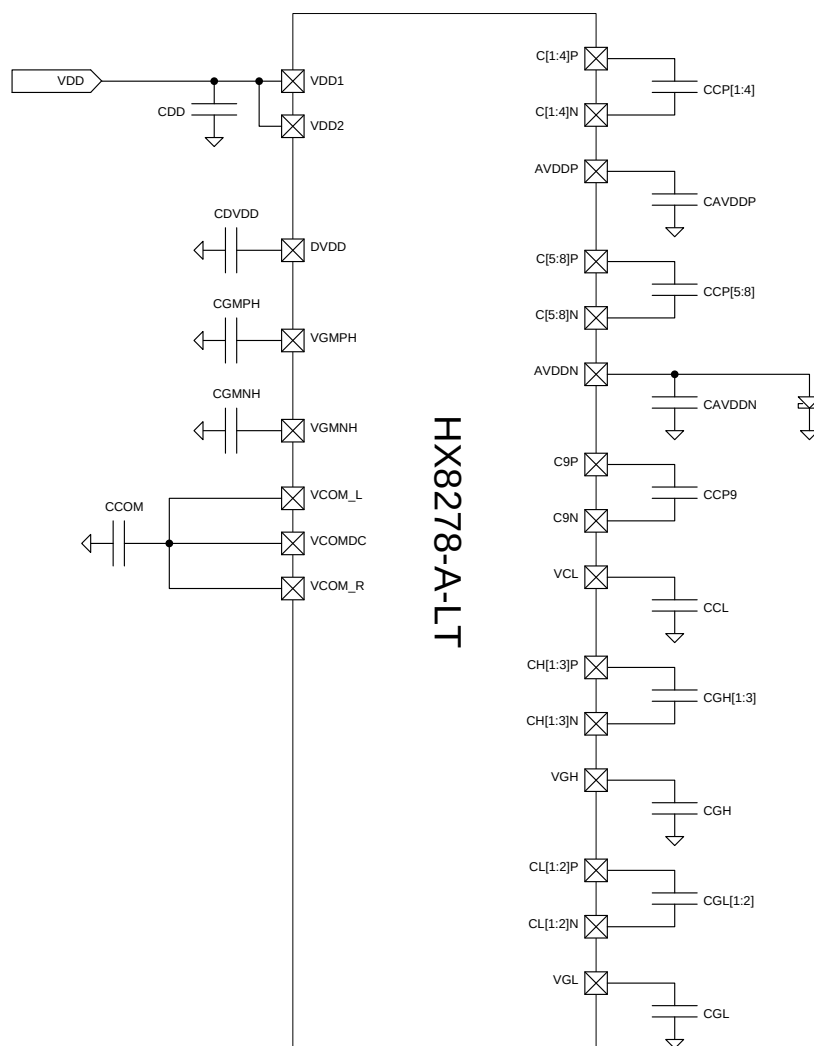


Figure 3.3: External components

Pin name	Capacitor name	Voltage(v)	Capacitance (μF)	
			Min	Max
VDD1/2	CDD	6.3	4.7	-
C[1:4]P/N	CCP[1:4]	6.3	1	2.2
AVDDP	CAVDDP	10	2.2	4.7
C[5:8]P/N	CCP[5:8]	6.3	1	2.2
AVDDN	CAVDDN	10	2.2	4.7
C9P/N	CCP9	6.3	1	2.2
VCL	CCL	6.3	2.2	4.7
CH[1:3]P/N	CGH[1:3]	10	1	2.2
VGH	CGH	25	1	2.2
CL[1:2]P/N	CGL[1:2]	10	1	2.2
VGL	CGL	16	1	2.2
VGMPH	CGMPH	10	1	2.2
VGMNH	CGMNH	10	1	2.2
DVDD	CDVDD	6.3	2.2	4.7
VCOMDC	CCOM	6.3	2.2	4.7

Table 3.1: Values of external capacitors

4. Pin Description

4.1 Pin description

Input interface pins (VDD1/VSS1 level)

Pin name	Type	Pulled internally	Description
D[0:2][0:7]	I	-	Data input pins for TTL and LVDS interface.
DCLK	I	-	Clock input pin for TTL interface
HS	I	-	Horizontal sync signal for TTL interface
VS	I	-	Vertical sync signal for TTL interface
DE	I	-	Data enable signal for TTL interface
RP[0:4] RN[0:4]	C	-	On-chip termination resistor connection

Note: (1) Refer to "Input pins for LVDS / TTL interface"

Table 4.1: Input interface pins

Input control pins, group 1 (Function controlled by hardware only) (VDD1/VSS1 level)

Pad name	Type	Pulled internally	Description		
RESETB	I	H	Reset pin. If RESETB=0, the chip is in reset state.		
FCS	I	H	Function control by Hardware/Software selection. (RL, TB function is the hardware setting “XOR” register setting when FCS=L.)		
			FCS	Function control	Note
			1	Hardware pin (group 2)	Default
			0	Software register	-
ATREN	I	H	Enable auto reload OTP/EEPROM every 60 frames		
			ATREN	Function	Note
			1	Enable auto reload OTP/EEPROM	Default
			0	Disable auto reload OTP/EEPROM	-
			Note: (1) When EEPEN=H (enable EEPROM reload setting) the register table will auto-reload from EEPROM. (2) When EEPEN=L(disable EEPROM reload setting) the register table will auto-reload from OTP		
IFSEL	I	L	Interface select		
			IFSEL	Function	Note
			1	I2C	-
			0	SPI	Default
EEPEN	I	L	EEPROM enable		
			EEPEN	Function	Note
			1	Enable	-
			0	Disable	Default

Table 4.2: Input control pins, group 1 (Function control by hardware only)

**Input control pins, group 2 (Function controlled by hardware and/or software setting)
(VDD1/VSS1 level)**

Pad name	Type	Pulled internally	Description												
STBYB	I	H	Standby mode setting pin. If STBYB=0, the chip is in standby mode.												
TR	I	L	Interface selection. <table><tr><th>TR</th><th>Function</th><th>Note</th></tr><tr><td>0</td><td>TTL</td><td>Default</td></tr><tr><td>1</td><td>LVDS</td><td>-</td></tr></table>	TR	Function	Note	0	TTL	Default	1	LVDS	-			
TR	Function	Note													
0	TTL	Default													
1	LVDS	-													
MODE[1:0]	I	H	Input timing mode selection. Effective when FCS=1. <table><tr><th>MODE[1:0]</th><th>Function</th><th>Note</th></tr><tr><td>00</td><td>DE mode</td><td>-</td></tr><tr><td>01</td><td>SYNC mode</td><td>Default</td></tr><tr><td>1x</td><td>Reserved</td><td>-</td></tr></table>	MODE[1:0]	Function	Note	00	DE mode	-	01	SYNC mode	Default	1x	Reserved	-
MODE[1:0]	Function	Note													
00	DE mode	-													
01	SYNC mode	Default													
1x	Reserved	-													
RL	I	H	Horizontal shift direction selection. (RL function is the hardware setting “XOR” register setting when FCS=L.) <table><tr><th>RL</th><th>Source output sequence and data order</th><th>Note</th></tr><tr><td>1</td><td>Forward (Left to right, S1 to S480)</td><td>Default</td></tr><tr><td>0</td><td>Reverse (Right to left, S480 to S1)</td><td>-</td></tr></table>	RL	Source output sequence and data order	Note	1	Forward (Left to right, S1 to S480)	Default	0	Reverse (Right to left, S480 to S1)	-			
RL	Source output sequence and data order	Note													
1	Forward (Left to right, S1 to S480)	Default													
0	Reverse (Right to left, S480 to S1)	-													
TB	I	H	Vertical shift direction selection. (TB function is the hardware setting “XOR” register setting when FCS=L.) <table><tr><th>TB</th><th>Function</th><th>Note</th></tr><tr><td>1</td><td>Forward (Top to bottom, G1 to G840)</td><td>Default</td></tr><tr><td>0</td><td>Reverse (Bottom to top, G840 to G1)</td><td>-</td></tr></table>	TB	Function	Note	1	Forward (Top to bottom, G1 to G840)	Default	0	Reverse (Bottom to top, G840 to G1)	-			
TB	Function	Note													
1	Forward (Top to bottom, G1 to G840)	Default													
0	Reverse (Bottom to top, G840 to G1)	-													
BISTEN	I	L	Enable bolt-in self test (BIST) function. Effective when FCS=1. <table><tr><th>BISTEN</th><th>Function</th><th>Note</th></tr><tr><td>1</td><td>BIST mode</td><td>-</td></tr><tr><td>0</td><td>Normal mode</td><td>Default</td></tr></table>	BISTEN	Function	Note	1	BIST mode	-	0	Normal mode	Default			
BISTEN	Function	Note													
1	BIST mode	-													
0	Normal mode	Default													
INTL	I	L	Interlaced / normal input selection. Effective when FCS=1. <table><tr><th>INTL</th><th>Function</th><th>Note</th></tr><tr><td>1</td><td>Interlaced input</td><td>-</td></tr><tr><td>0</td><td>Normal input</td><td>Default</td></tr></table>	INTL	Function	Note	1	Interlaced input	-	0	Normal input	Default			
INTL	Function	Note													
1	Interlaced input	-													
0	Normal input	Default													

Table 4.3: Input control pins, group 1 (Function control by hardware or software setting)

Serial interface pins (VDD1/VSS1 level)

Pin name	Type	Pulled internally	Description
CSB	I	H	Serial Interface chip enable signal for SPI interface.
SCL	I	H	Serial interface clock input for SPI / I2C interface.
SDAI	I	L	Serial interface address and data input for SPI / I2C interface.
SDAO	O	-	Serial interface data output for SPI / I2C interface. (I2C interface need external pull high resistor.)

Table 4.4: Serial interface pins

EEPROM interface pins (VDD1/VSS1 level)

Pin name	Type	Pulled internally	Description
TESTO5 (ECS)	O	-	Chip select enable signal for EEPROM ECS=0: Not accessing EEPROM

			ECS=1: Accessing EEPROM
TESTO6 (ESCL)	O	-	Clock signal for EEPROM
ESDAI	I	L	Serial data input from EEPROM
TESTO7 (ESDAO)	O	-	Serial data (address) output for EEPROM

Table 4.5: EEPROM interface pins
Source and gate output pins

Pin name	Type	Description
S[1:480]	O	Source driver output pins.
G[1:840]	O	Gate driver output pins.

Table 4.6: Source and gate output pins
Power supply pins: Connected to power supply

Pin name	Type	Description
VDD1	P	Power input for main and I/O power (3.0V to 3.6V).
VDD1P	P	Power input for charge pumps. Internally shorted to VDD1, but must be connected when charge pumps are used.
VSS1	P	Ground pin for logic circuit and I/O (0V).
VSS1P	P	Ground pin for charge pumps. Internally shorted to VSS1, but must be connected when charge pumps are used.
VDD2	P	Power pin for internal references (3.0V to 3.6V).
VSS2	P	Internal reference circuit ground (0V).
VSSA	P	Analog circuit ground (0V).
VDDOTP	P	Power input for OTP programming (8.6V). Leave this pin open or connect it to VDD1 when not programming OTP.

Table 4.7: Power supply pins
Charge pump pins: Connect to capacitors

Pin name	Type	Description
AVDDP	O	Charge pump output for source / gamma.
AVDDN	O	Charge pump output for source / gamma.
VCL	O	Charge pump output for level shifter.
VGH	O	Charge pump output for gate driver.
VGL	O	Charge pump output for gate driver.
C[1:4]P/N	C	Capacitor connection pin for AVDDP charge pump.
C[5:8]P/N	C	Capacitor connection pin for AVDDN charge pump.
C9P/N	C	Capacitor connection pin for VCL charge pump.
CH[1:3]P/N	C	Capacitor connection pin for VGH charge pump.
CL[1:2]P/N	C	Capacitor connection pin for VGL charge pump.

Table 4.8: Charge pump pins
Regulator output pins: Connect to capacitors

Pin name	Type	Description
VGMPH	O	Internal regulator output for positive gamma reference voltage.
VGMNH	O	Internal regulator output for negative gamma reference voltage.
DVDD	O	Internal regulator output for logic power supply (1.5V).
VCOMDC	O	Internal driving circuit for VCOM (-2.75V to -0.2V).

Table 4.9: Regulator output pins

Special function pins

Pin name	Type	Description
TPSYNC	O	Synchronization signal for touch panel.
TESTO0 (FFLAG)	O	Result of failure detection.

Table 4.10: Special function pins

Test pins, through pins and dummy pins

Pin name	Type	Description
TESTO[4:1]	O	Logic test pins, leave these pins open.
TESTI	I	Logic test pins, leave this pin open.
TESTA[5:0]	O	Internal reference voltage test pin, leave these pins open.
THROUGH [1:2]	-	These sets of pins can be used for resistance measurement.
VCOM_R VCOM_L	-	These sets of pins can be used for VCOM connection to the panel.
DUMMY	-	These pins are open and separated to each other.

Table 4.11: Test pins, through pins and dummy pins

4.2 Group 2 input pins vs. registers

The following settings can be controlled by hardware input pin and/or values in register page 0.

Pin name	Register (Page.0)
STBYB	R01h[7:0]
TR	R02h[6]
MODE[1:0]	R02h[2:1]
RL	R03h[7]
TB	R03h[6]
INTL	R03h[3]
BISTEN	R05h[4]

Table 4.12: Hardware input pins vs. relating registers

Standby operation is controlled by hardware input pin STBYB and register STBYB_CMD (R01h in page 0).

Hardware pin STBYB	Register STBYB_CMD (R01h)	Operation state
1	≠0x55	Normal
	0x55	Standby
0	X	Standby

Table 4.13: Operation state of STBYB

Scan directions are controlled by hardware input pins RL and TB, and values in register page 0. When FCS is set to 0, the chip is controlled by both with XOR operation. Otherwise, the chip is controlled by hardware pin.

FCS	Hardware pin	Register value	Operation state
1	1	X	1
	0		0
0	1	1	0
		0	1
	0	1	1
		0	0

Table 4.14: Operation state of RL and TB

The other group 2 input pins (TR, MODE[1:0], INTL, BISTEN) are selected by FCS. When FCS is set to 0, the chip is controlled by register values. Otherwise, the chip is controlled by hardware pin.

FCS	Hardware pin	Register value	Operation state
1	1	X	1
	0		0
0	X	1	1
		0	0

Table 4.15: Operation state of group 2 input pins except RL and TB

4.3 Input pins for LVDS / TTL interface

HX8278-A-LT supports TTL and LVDS interface in several formats. In TTL interface, unused data pins should be connected to ground. Unused pins in LVDS interfaces can be left floating.

Pin name	Pin type	TTL Parallel 24-bit (RGB 888)	TTL Parallel 18-bit (RGB 666)	TTL Parallel 16-bit (RGB 565)	TTL Serial 8-bit	LVDS 4-lane (8-bit)	LVDS 3-lane (6-bit)	LVDS 2-lane (8-bit)
D20	TTL/ Differential	DB0	VSS	VSS	VSS	-	-	-
D21		DB1	VSS	VSS	VSS	-	-	-
D22		DB2	DB2	VSS	VSS	-	-	-
D23		DB3	DB3	DB3	VSS	-	-	-
D24		DB4	DB4	DB4	VSS	-	-	-
D25		DB5	DB5	DB5	VSS	-	-	-
D26		DB6	DB6	DB6	VSS	-	-	-
D27		DB7	DB7	DB7	VSS	-	-	-
D10		DG0	VSS	VSS	VSS	-	-	-
D11		DG1	VSS	VSS	VSS	-	-	-
D12		DG2	DG2	DG2	VSS	-	-	-
D13		DG3	DG3	DG3	VSS	-	-	-
D14		DG4	DG4	DG4	VSS	-	-	-
D15		DG5	DG5	DG5	VSS	-	-	-
D16		DG6	DG6	DG6	VSS	LV3P	-	-
D17		DG7	DG7	DG7	VSS	LV3N	-	-
D00		DR0	VSS	VSS	D0	LVCLKP	LVCLKP	LVCLKP
D01		DR1	VSS	VSS	D1	LVCLKN	LVCLKN	LVCLKN
D02		DR2	DR2	VSS	D2	LV2P	LV2P	LV2P
D03		DR3	DR3	DR3	D3	LV2N	LV2N	LV2N
D04		DR4	DR4	DR4	D4	LV1P	LV1P	-
D05		DR5	DR5	DR5	D5	LV1N	LV1N	-
D06		DR6	DR6	DR6	D6	LV0P	LV0P	LV0P
D07		DR7	DR7	DR7	D7	LV0N	LV0N	LV0N
HS	TTL	HS				-		
VS		VS				-		
DE		DE				-		
DCLK		DCLK				-		

Table 4.16: Input pins for TTL / LVDS

4.3.1TTL interface

TTL interface is selected by setting TR to 0. Four modes are available.

TR	DINT[1]	DINT[0]	LVDS_FMT	Interface
0	0	0	X	TTL, Parallel 18-bit (RGB 666)
		1		TTL, Parallel 24-bit (RGB 888)
	1	0		TTL, Parallel 16-bit (RGB 565)
		1		TTL, Serial 8-bit

Table 4.17: TTL input modes

4.3.2 LVDS interface

LVDS interface is selected by setting TR to 1. Five modes are available.

TR	DINT[1]	DINT[0]	LVDS_FMT	Interface
1	0	0	X	LVDS, 3-lane (6-bit)
		1	0	LVDS, 4-lane (8-bit), JEIDA
			1	LVDS, 4-lane (8-bit), VESA
	1	X	0	LVDS, 2-lane (8-bit), JEIDA
			1	LVDS, 2-lane (8-bit), VESA

Table 4.18: LVDS input modes

4.3.2.1 LVDS, 3-lane (6-bit) mode

In this mode LV3P/N pins are not used, and only one format is supported.

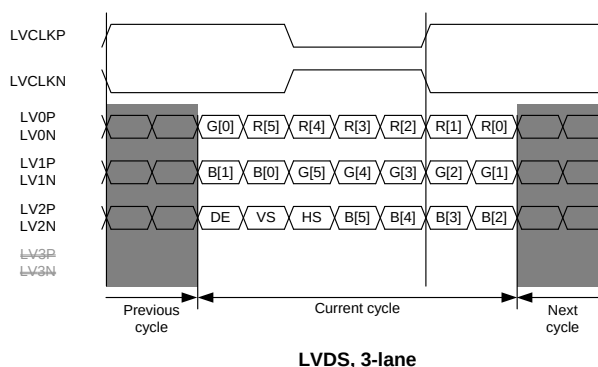


Figure 4.1: LVDS, 3-lane mode

4.3.2.2 LVDS, 4-lane (8-bit) mode

In this mode, two data formats (JEIDA and VESA) are selected by LVDS_FMT.

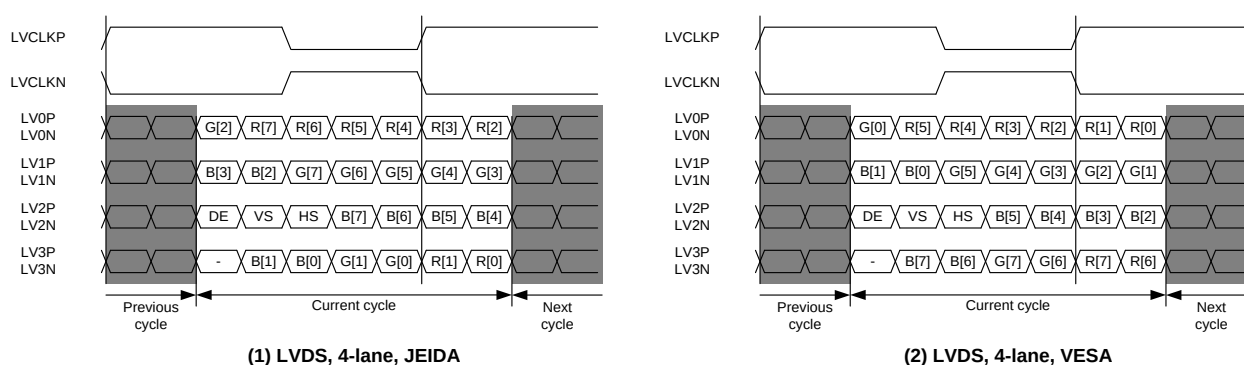
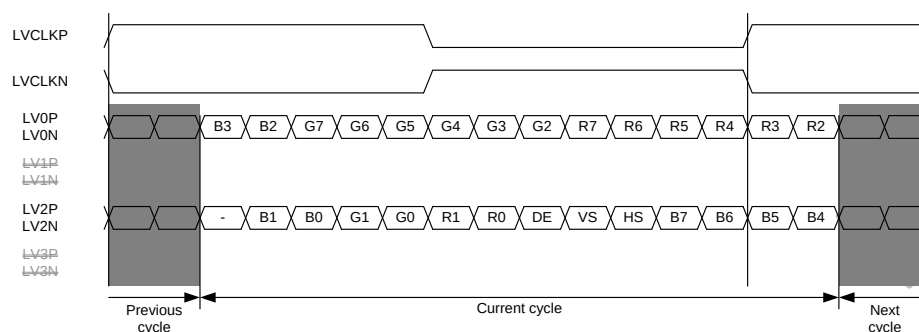


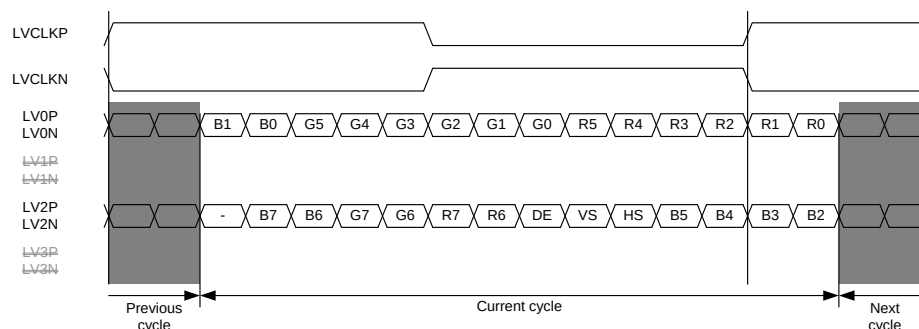
Figure 4.2: LVDS, 4-lane mode, two formats

4.3.2.3 LVDS, 2-lane (8-bit) mode

In this mode, LV1P/N and LV3P/N are not used. Two data formats (JEIDA and VESA) are selected by LVDS_FMT.



(1) LVDS, 2-lane, JEIDA

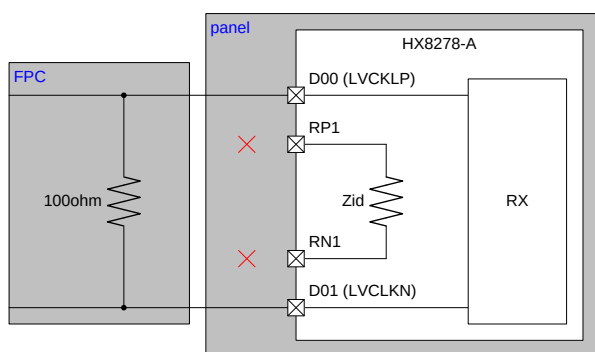


(2) LVDS, 2-lane, VESA

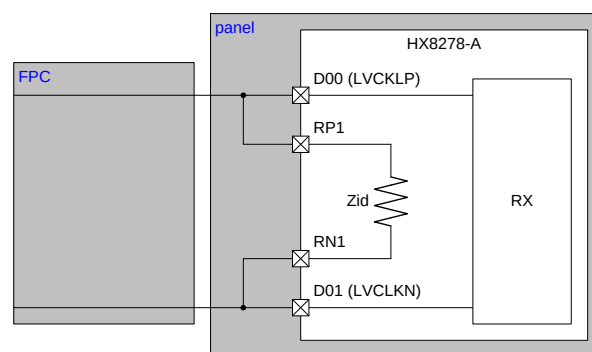
Figure 4.3: LVDS, 2-lane mode, two formats

4.3.2.4 On-chip LVDS termination resistors

There are five resistors between RP[0:4] and RN[0:4] input pins. They can be connected to LVDS input pins as termination resistors. Zid is typically 100ohm.



(1) connection when using external resistors



(2) connection when using on-chip resistors

Figure 4.4: Connection of termination resistors

Resistor pins	LVDS input pins
RP/N0	D16/D17 (LV3P/N)
RP/N1	D00/D01 (LVCLKP/N)
RP/N2	D02/D03 (LV2P/N)
RP/N3	D04/D05 (LV1P/N)
RP/N4	D06/D07 (LV0P/N)

Table 4.19: On-chip termination resistors vs. LVDS input pins

4.3.3 Data mapping

Data mapping for 6-bit mode is the same for both LVDS and TTL mode. 6-bit input data $DR/G/B[5:0]$ will be mapped to 8-bit data $D_{R/G/Bin}[7:0]$, where $D_{R/G/Bin}[7:2]=DI[5:0]$, and $D_{R/G/Bin}[1:0]=DR/G/B[5:4]$.

Mapped 8-bit data	Input Data	Mapped 8-bit data	Input Data	Mapped 8-bit data	Input Data
$D_{Rin}[0]$	DR6	$D_{Gin}[0]$	DG6	$D_{Bin}[0]$	DB6
$D_{Rin}[1]$	DR7	$D_{Gin}[1]$	DG7	$D_{Bin}[1]$	DB7
$D_{Rin}[2]$	DR2	$D_{Gin}[2]$	DG2	$D_{Bin}[2]$	DB2
$D_{Rin}[3]$	DR3	$D_{Gin}[3]$	DG3	$D_{Bin}[3]$	DB3
$D_{Rin}[4]$	DR4	$D_{Gin}[4]$	DG4	$D_{Bin}[4]$	DB4
$D_{Rin}[5]$	DR5	$D_{Gin}[5]$	DG5	$D_{Bin}[5]$	DB5
$D_{Rin}[6]$	DR6	$D_{Gin}[6]$	DG6	$D_{Bin}[6]$	DB6
$D_{Rin}[7]$	DR7	$D_{Gin}[7]$	DG7	$D_{Bin}[7]$	DB7

Table 4.20: Data mapping for 6-bit mode

4.4 IO pins for SPI / I2C

HX8278-A-LT supports SPI and I2C by setting IFSEL.

When IFSEL is set to 0, SPI mode is selected. SDAI and SDAO can be separated for 4-wire SPI mode, or connected together for 3-wire SPI mode. In the case of 3-wire SPI, it is suggested to connect SDAI and SDAO with a 1kohm resistor.

When IFSEL is set to 1, I2C mode is selected. CSB pin is not used and can be left floating. Note that a pull-high resistor is necessary on SDA.

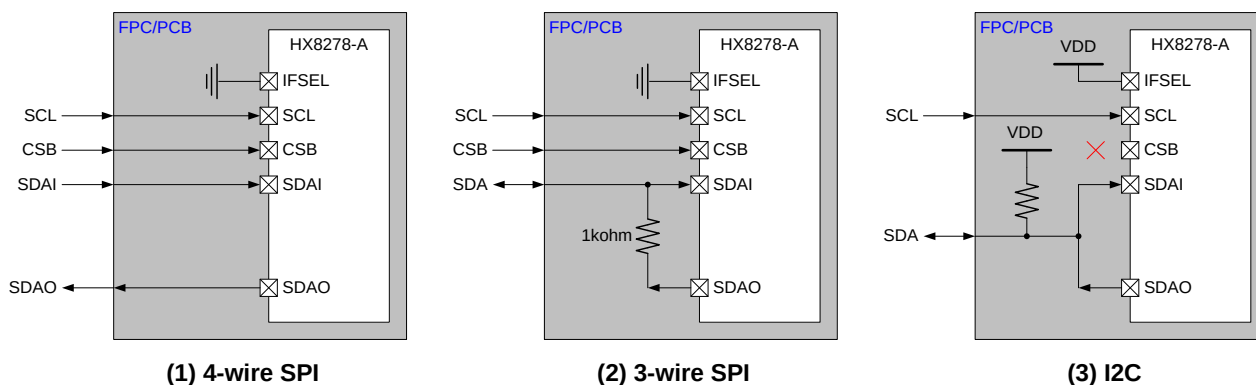


Figure 4.5: Connection of SPI/I2C I/O pins

4.5 Through pins for bonding resistance measurement

THROUGH_1 and THROUGH_2 pins are used for measuring bonding resistance. Note that THROUGH_1 pins are not connected to THROUGH_2 pins.

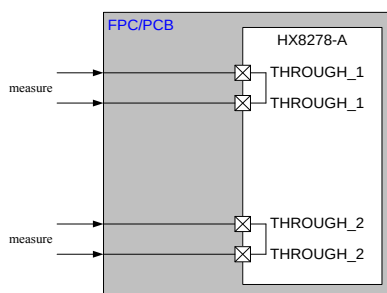


Figure 4.6: Connection for bonding resistance measurement

4.6 Recommended wiring resistance values

The recommended wiring resistance values are listed below as reference. Wiring resistance values affect the current capacity of the power supply, thus they are related to panel loading.

Pad type	Pad	Resistance	Pad type	Pad	Resistance
Power supply pins	VDD1	< 10Ω	Input interface and output pins	D0[7:0] D1[7:0] D2[7:0] DCLK	< 50Ω
	VDD1P				
	VSS1				
	VSS1P				
	VDD2				
	VSS2				
	VSSA				
	VDDOTP				
Regulator output pins	VGMPH	< 20Ω	Input control pins	TB	< 100Ω
	VGMNH	< 10Ω		RL	
	DVDD			MODE	
VCOMDC		RESETB			
SPI /I2C pins	CSB	< 100Ω		STBYB	
	SCL			ATREN	
	SDAI			TR	
	SDAO	< 20Ω		INTL	
Charge pump pins	AVDDP	< 10Ω		IFSEL	
	AVDDN	< 20Ω		BISTEN	
	VCL			FCS	
	VGH				
	VGL				
	C[1:8]P/N	< 10Ω			
	C9P/N	< 20Ω			
	CH[1:3]P/N				
	CL[1:3]P/N				
			EEPROM	ECS	< 20Ω
Through pins	THROUGH [1:2]	-		ESCL	
	VCOM_R	-		ESDAI	
	VCOM_L	-		ESDAO	
			Others	TPSYNC	< 20Ω

Table 4.21: Recommended wiring resistance values

5. Panel Architecture and Resolutions

5.1 Panel architecture

Panel architecture is shown as below. For the Nth display line, G[3N+1] controls the gate lines of red color, G[3N+2] controls the gate lines of green color, and G[3N+3] controls the gate lines of blue color.

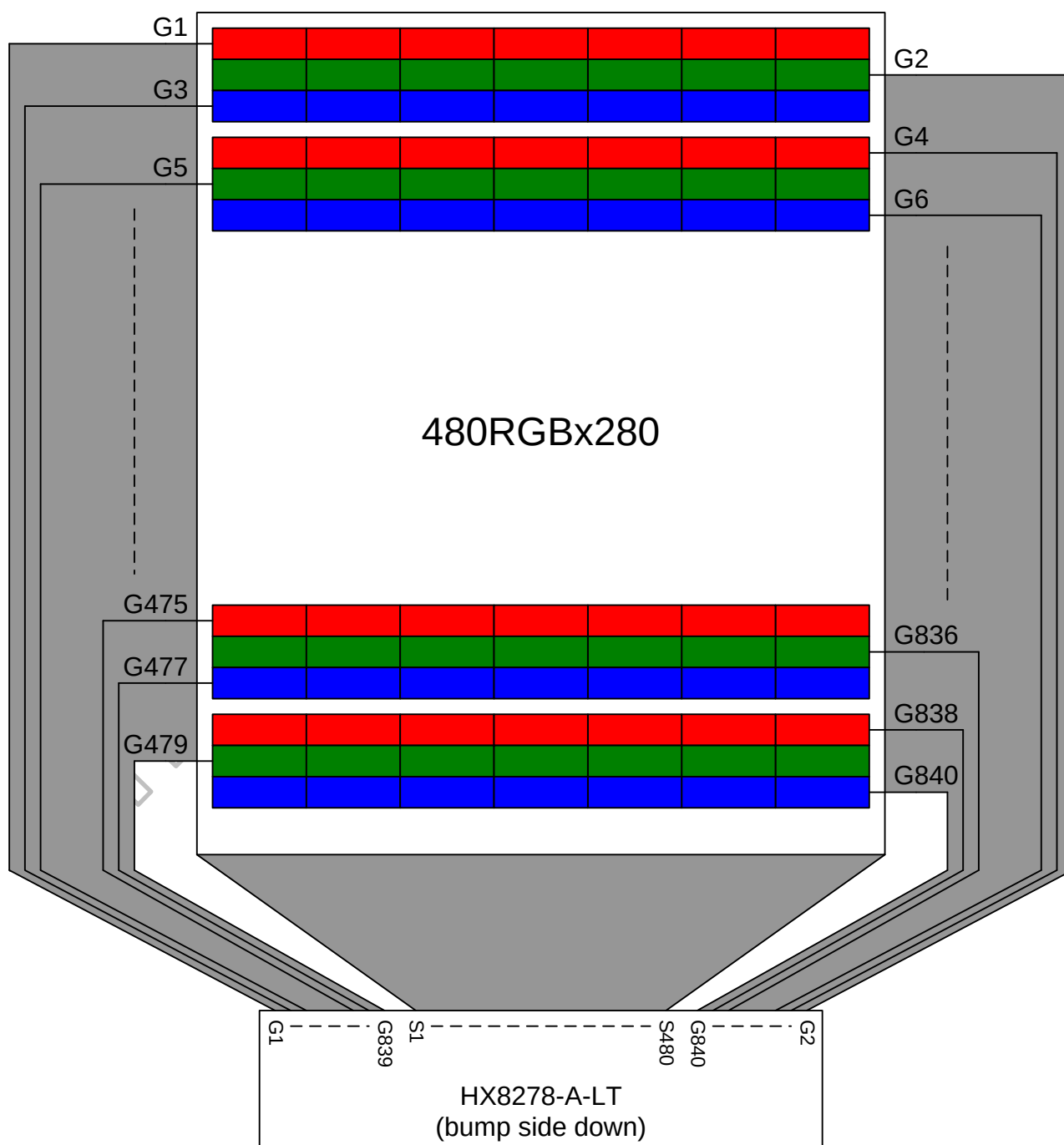


Figure 5.1: Panel architecture

5.2 Resolutions

5.2.1 Typical resolutions

Four typical resolutions are selected with RS[1:0].

Resolution		Setting
RGB (X)	Line (Y)	RS[1:0]
480	272	00
400	240	01
260	240	10
320	240	11

Table 5.1: Resolution table

5.2.2 Adjustable resolution:

Display resolution can be set as Hactive (RGB) x Vactive, where Hactive is a multiple of 4 ranging from 120 to 480 (that is, 120, 124, 128, ..., 476, 480), and Vactive is an even number ranging from 120 to 280. Hactive and Vactive can be selected with RS[1:0], or set with register HSETNUM[10:0] and GATENUM[9:0].

5.2.3 Valid source output

When horizontal resolution is set to Hactive RGB, S1 to S[Hactive/2], S[481-Hactive/2] to S480 will output sequentially.

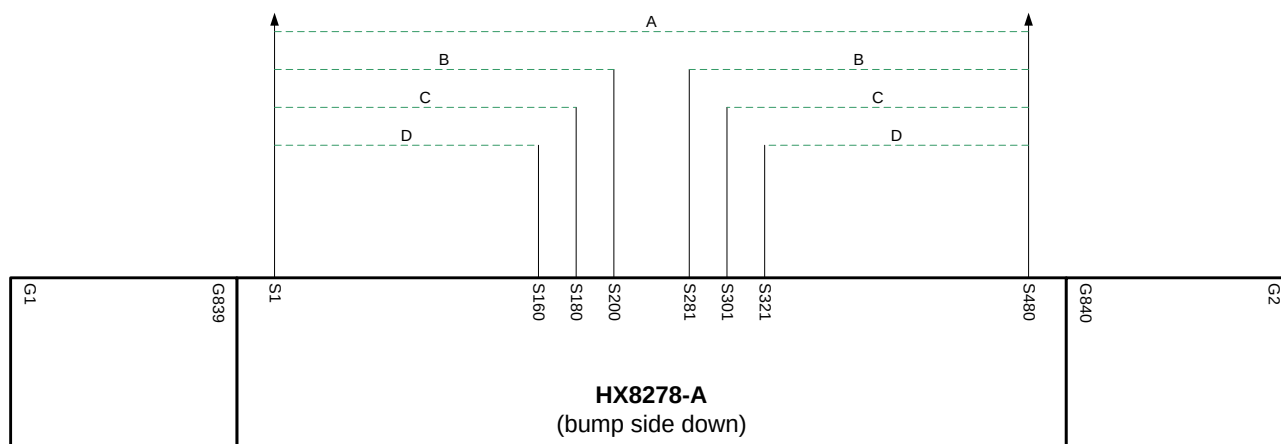


Figure 5.2: Valid source output

Channels		Valid source output
A	480	S1~S480
B	400	S1~S200, S281~S480
C	360	S1~S180, S301~S480
D	320	S1~S160, S321~S480
-	Hactive	S1~S[Hactive/2], S[481-Hactive/2]~S480

Note: Hactive is multiple of 4.

Table 5.2: Valid source output table

5.2.4 Valid gate output

When vertical resolution is set to Vactive lines, G1 to G[3*Vactive] will output sequentially in the direction controlled by TB.

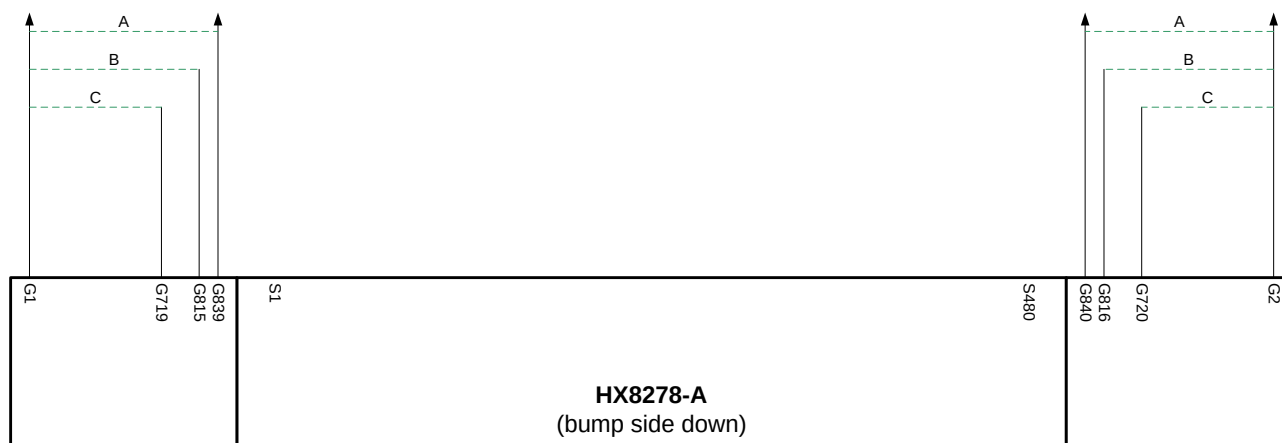


Figure 5.3: Valid gate output

Channels		Valid source output
A	280	G1~G840
B	272	G1~G816
C	240	G1~G720
-	Vactive	G1~G[3*Vactive]

Note: Vactive is even.

Table 5.3: Valid gate output table

5.3 Gate scan types

The gate driver supports six scan types, which are selected by GDSEQ[2:0].

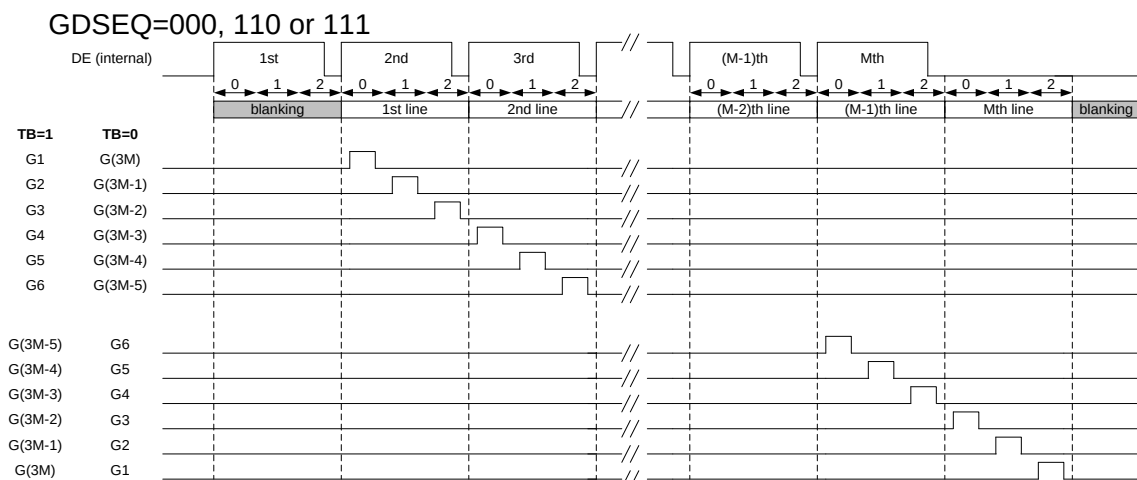


Figure 5.4: Gate scan type 0

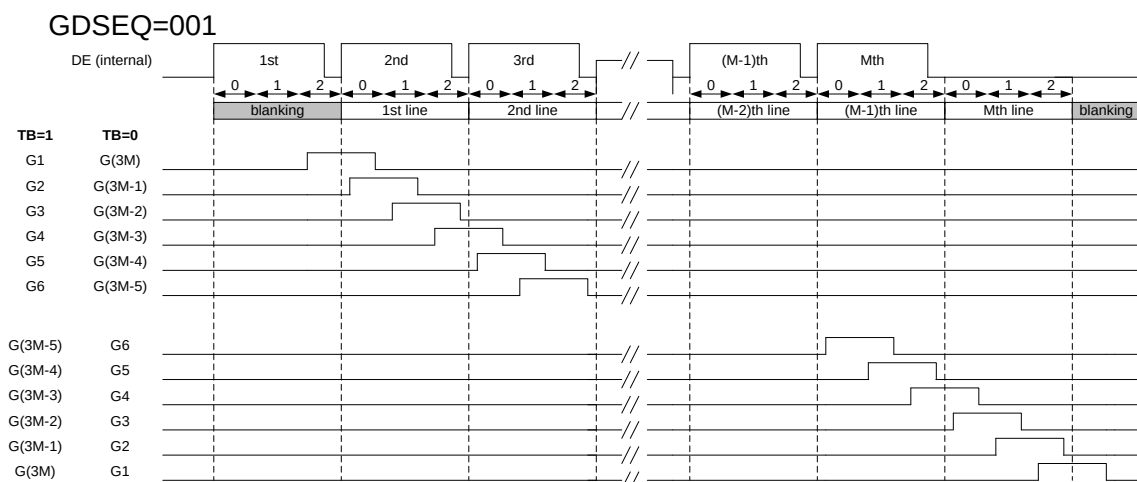


Figure 5.5: Gate scan type 1

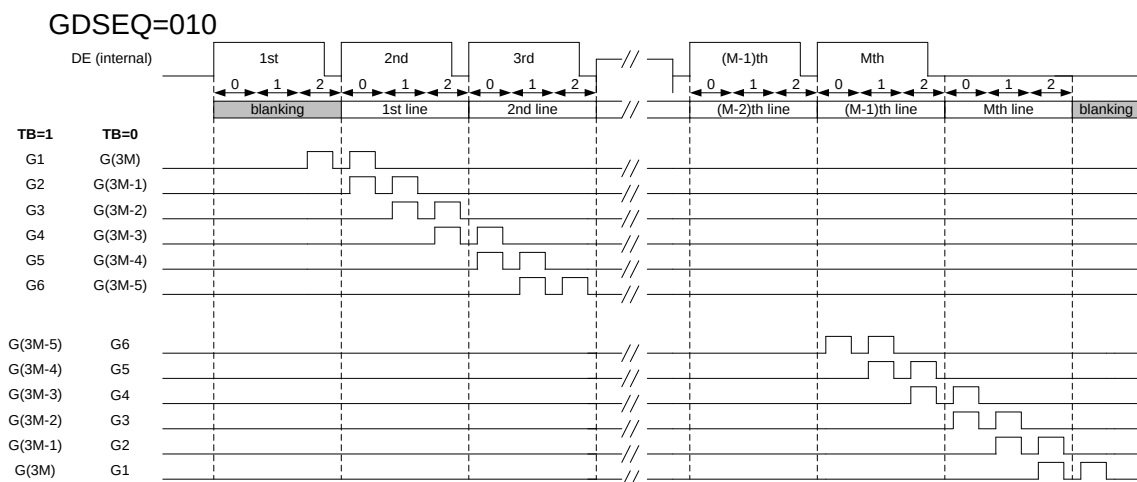


Figure 5.6: Gate scan type 2

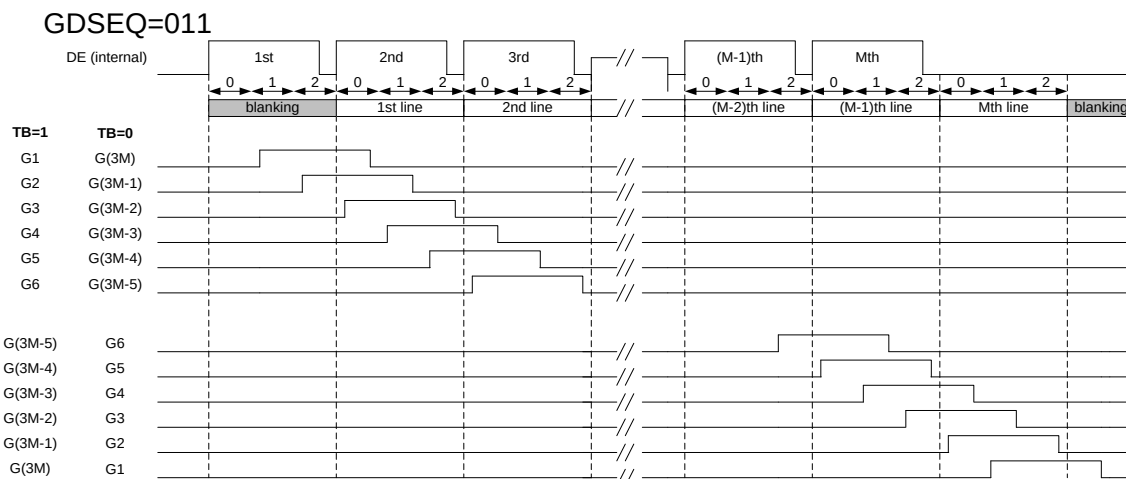


Figure 5.7: Gate scan type 3

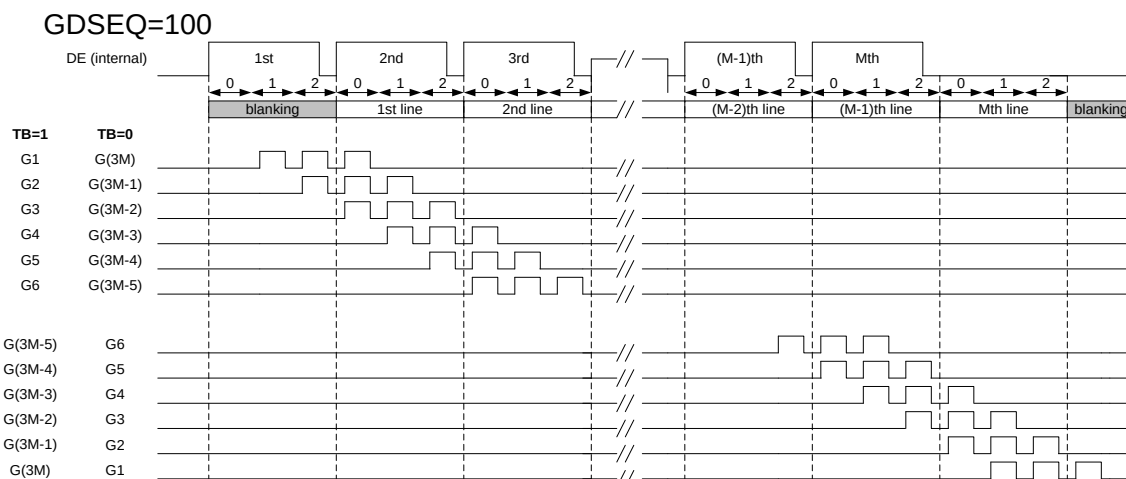


Figure 5.8: Gate scan type 4

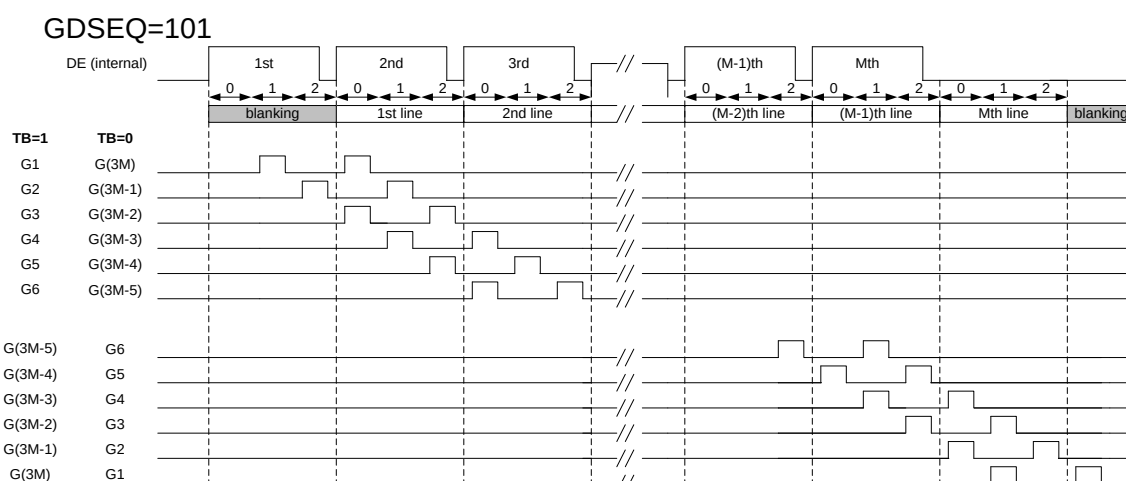


Figure 5.9: Gate scan type 5

6. Function Description

6.1 Power on/off sequence

6.1.1 Power on sequence

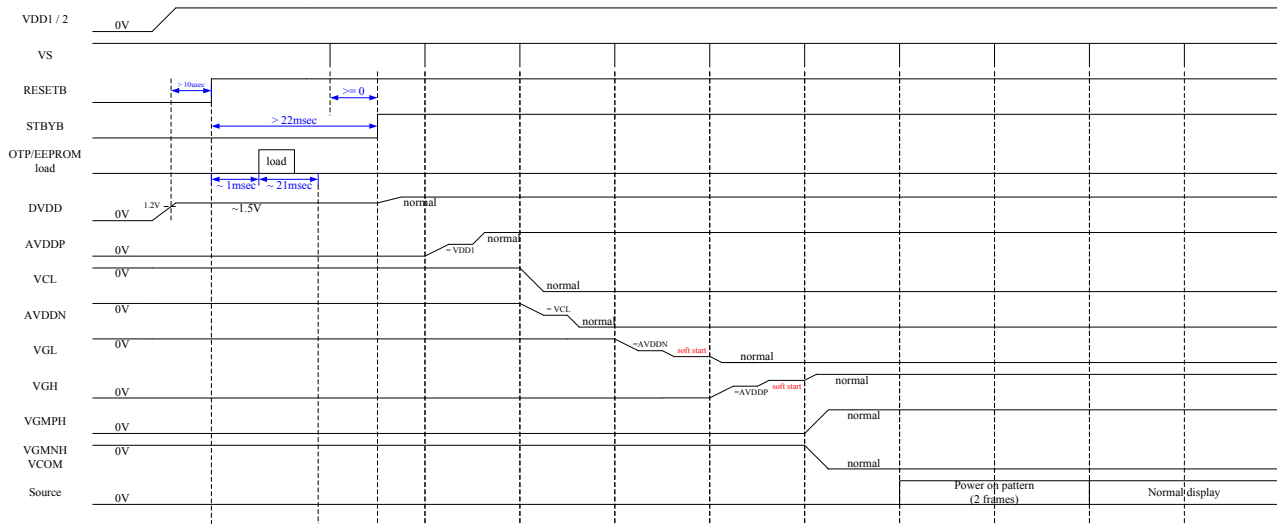


Figure 6.1: Power on sequence

6.1.2 Power off sequence

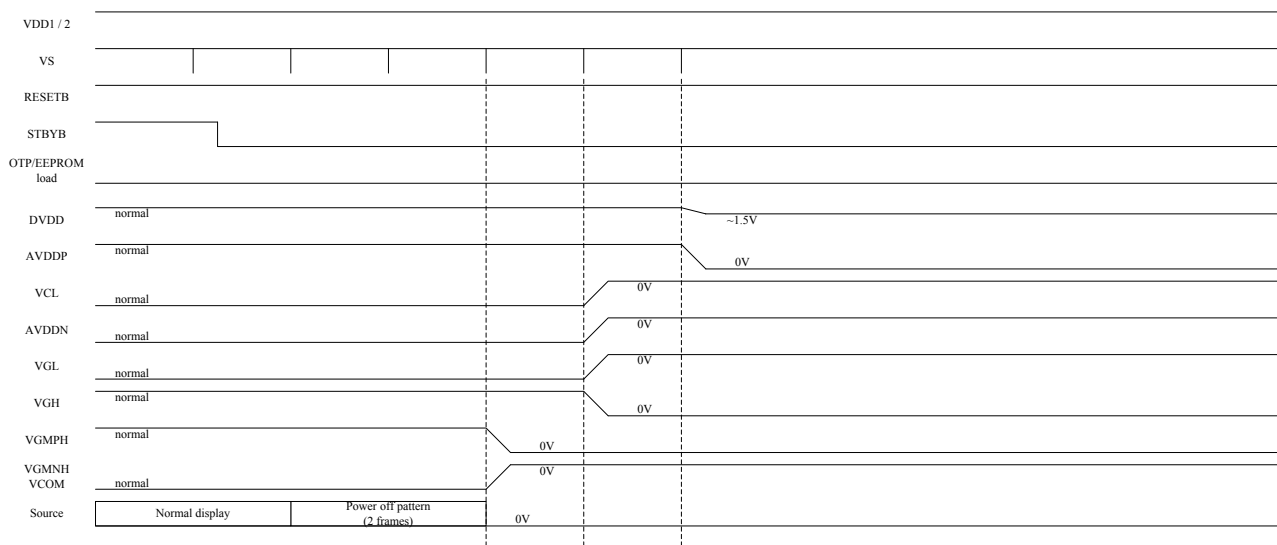
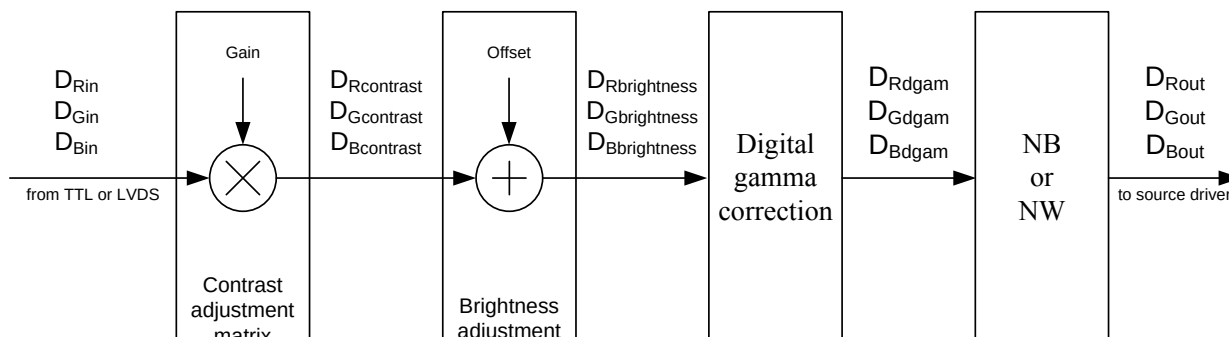


Figure 6.2: Power off sequence

6.2 Data processing circuit

Input 24-bit RGB data from TTL or LVDS interface is processed in the following order.



6.2.1 Contrast adjustment with color shift

Contrast adjustment is done on RGB data separately by multiplying a gain ranging from 0.5 to 1.496. The gain Rr_C , Gg_C , Bb_C for each color is set with 3 sets of 8-bit registers ($Rr_C[7:0]$, $Gg_C[7:0]$, $Bb_C[7:0]$) with default value 1.0.

Color shift is defined with mutual gain Rg_C , Rb_C , Gr_C , Gb_C , Bg_C , Bb_C between colors in the range of 0 to 0.123, and it is set with 6 sets of 6-bit registers ($Rg_C[5:0]$, $Rb_C[5:0]$, $Gr_C[5:0]$, $Gb_C[5:0]$, $Bg_C[5:0]$, $Bb_C[5:0]$) with default value 0.

If the resulting output data exceeds 255, it will be clamped to 255.

$$\begin{aligned} D_{Rcontrast} &= D_{Rin} * Rr_C + D_{Gin} * Rg_C + D_{Bin} * Rb_C \\ D_{Gcontrast} &= D_{Rin} * Gr_C + D_{Gin} * Gg_C + D_{Bin} * Gb_C \\ D_{Bcontrast} &= D_{Rin} * Br_C + D_{Gin} * Bg_C + D_{Bin} * Bb_C \end{aligned}$$

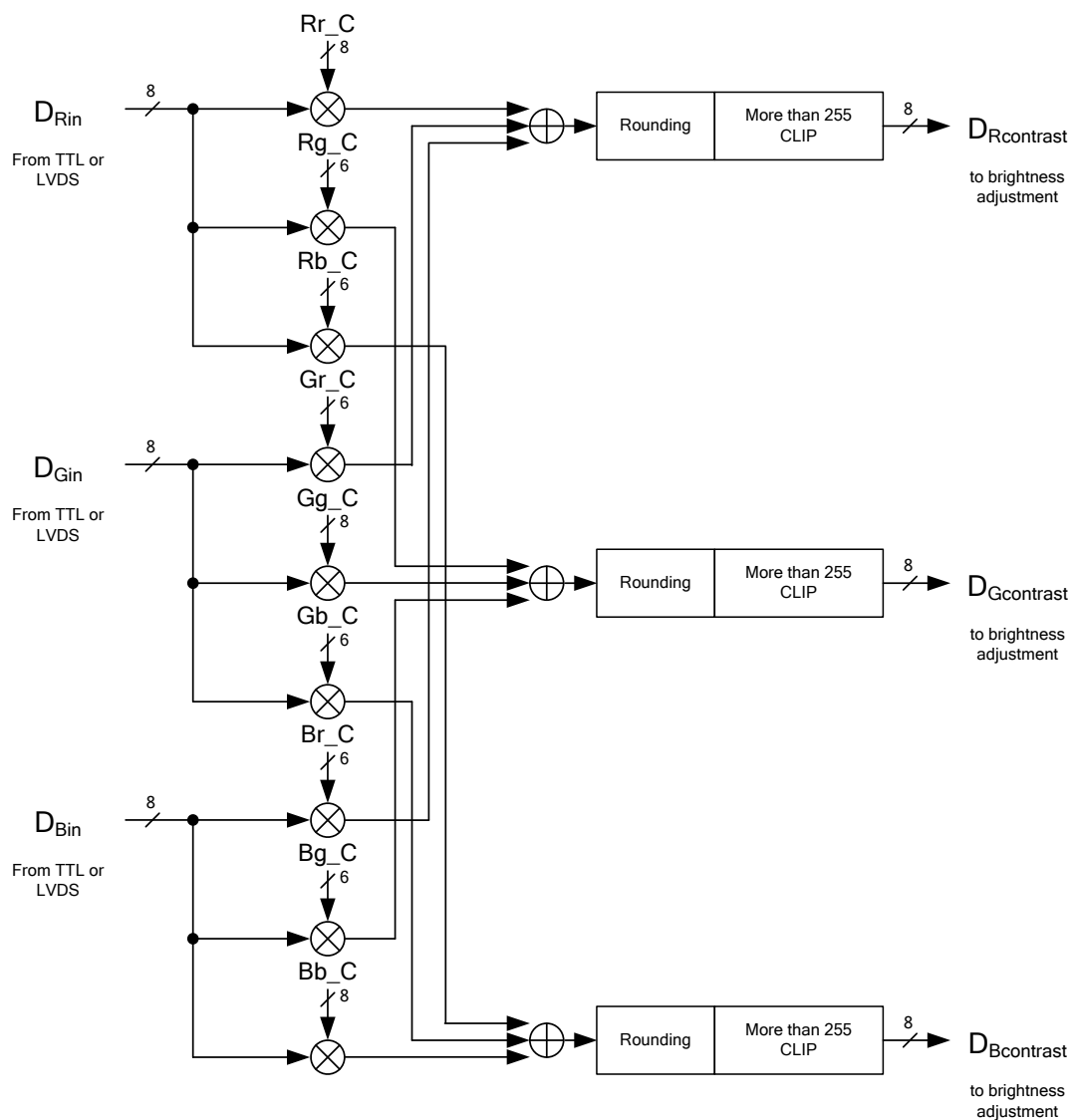


Figure 6.4: Contrast adjustment matrix

6.2.2 Brightness adjustment

Brightness adjustment is done on RGB data separately by adding an offset ranging from -16 to +47. The offset of each color is set with 3 sets of 6-bit registers (**ROB[5:0]**, **GOB[5:0]**, **BOB[5:0]**). If the resulting output data exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

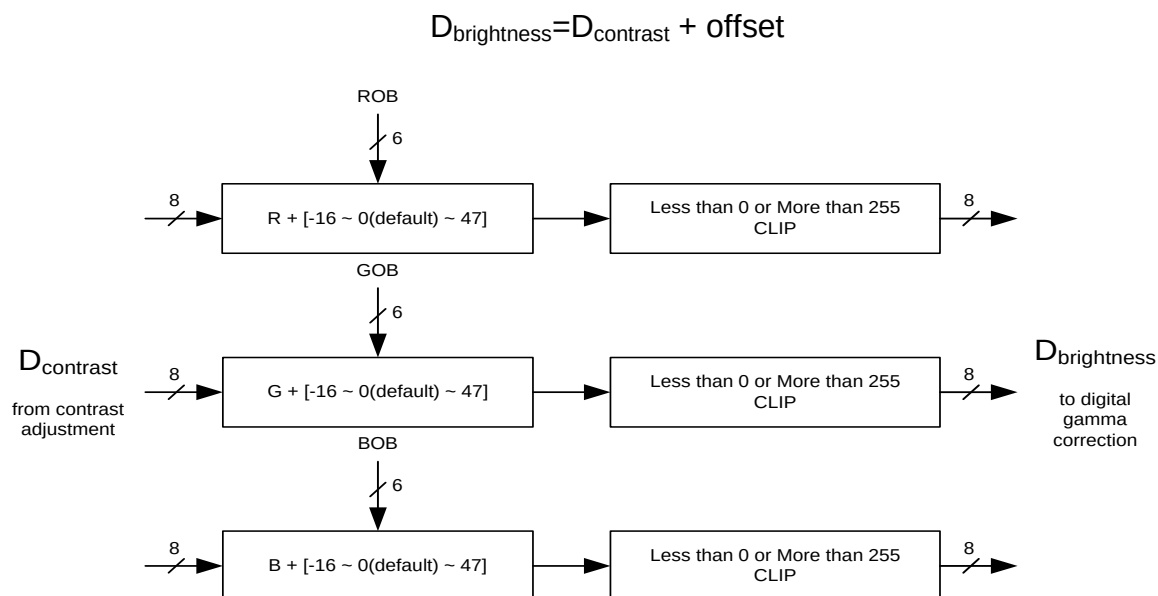


Figure 6.5: Brightness adjustment

6.2.3 Digital gamma correction

The digital gamma correction is done on RGB data separately with 33-segment piecewise linear interpolation, positive and negative polarities are also independent. The 32 segments are defined with 33 register values Y_1 to Y_{33} (in register page 2~7) for 33 reference points X_1 to $X_{33} = 0, 1, 2, 3, 5, 7, 9, 11, 13, 15, 23, 31, 47, 63, 79, 95, 127, 159, 175, 191, 207, 223, 231, 239, 241, 243, 245, 247, 249, 251, 253, 254$ and 255. Y on X between X_n and X_{n+1} is interpolated with the following equations.

$$Y = Y_n + (Y_{n+1} - Y_n) * (X - X_n) / (X_{n+1} - X_n)$$

The gamma correction output 10-bit data D_{dgam} is then fed to 8-bit DAC and voltage buffer to drive the source lines on the panel with dithering.

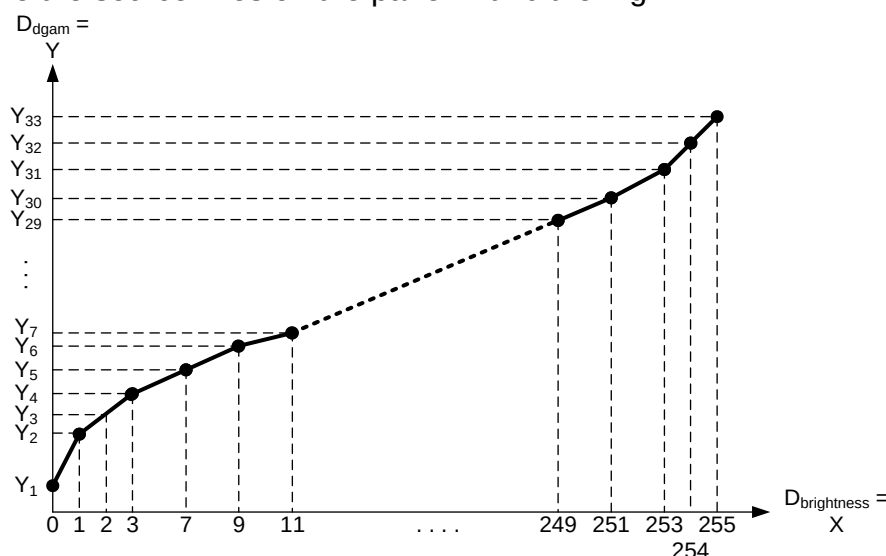


Figure 6.6: Digital gamma correction

6.2.4 NB/NW selection

The data after digital gamma processing D_{dgam} will go to NB/NW block. It will transfer D_{dgam} to corresponding data $D_{\text{Rout}}[9:0]$, $D_{\text{Gout}}[9:0]$ and $D_{\text{Bout}}[9:0]$ for the source driver. For the case of NB, D_{Rout} , D_{Gout} , D_{Bout} equal to D_{dgam} , while for the case of NW D_{Rout} , D_{Gout} , D_{Bout} are inverted D_{dgam} .

6.3 Gamma adjustment

In the source driver, 10-bit data $D_{Rout}[9:0]$, $D_{Gout}[9:0]$ and $D_{Bout}[9:0]$ are converted to analog grayscale voltages $VGSP[255:0]$ for positive polarity and $VGSN[255:0]$ for negative polarity with 8-bit DACs and 2-bit dithering.

Relation between data k ($D_{Rout}[9:2]$, $D_{Gout}[9:2]$ and $D_{Bout}[9:2]$) and $VGSP[255:0]$ and $VGSN[255:0]$ is:

$$VGSP[k] = VGMPL + (VGMPH - VGMPL) * (k+1)/256$$

$$VGSN[k] = VGMNL + (VGMNH - VGMNL) * (k+1)/256$$

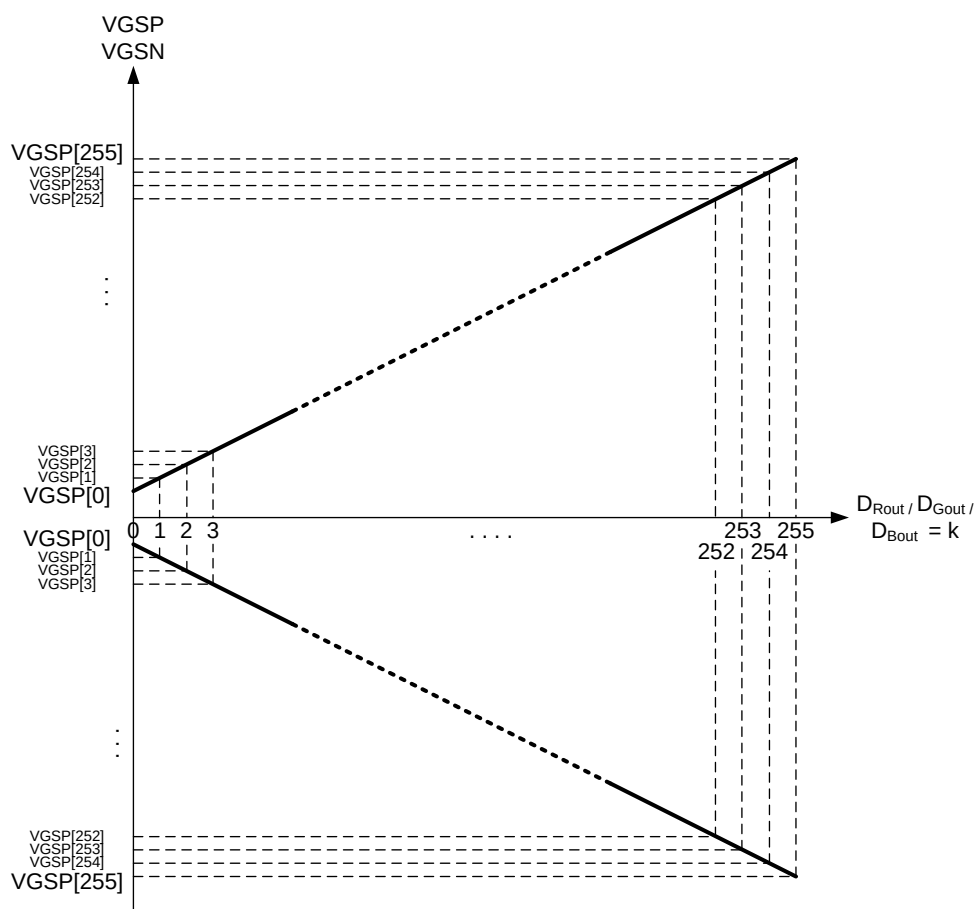


Figure 6.7: Analog grayscale voltages

6.4 BIST function

A pattern generator is embedded for BIST (Built-In Self Test) mode. When BISTEN is set to 1, built-in patterns will be displayed. These patterns can be selected by register PTSEL[3:0]. When PTSEL[3:0] is set to 1111, pattern 0 to 12 will be displayed sequentially and periodically.

Frame rate in BIST mode is 60Hz for the four typical resolutions. When adjustable resolution is enabled (by setting GATEPASS[3:0] or HSETPASS[3:0]), internal clock frequency, horizontal blanking and vertical blanking can be set with register BISTCLKS[1:0], BISTHBS[7:0] and BISTVBS[3:0].

Pattern 7 Checker board pattern is combination of the 16 pixels x 16 pixels black and white blocks. Pattern 9 VCOM trimming pattern depends on the inversion type.

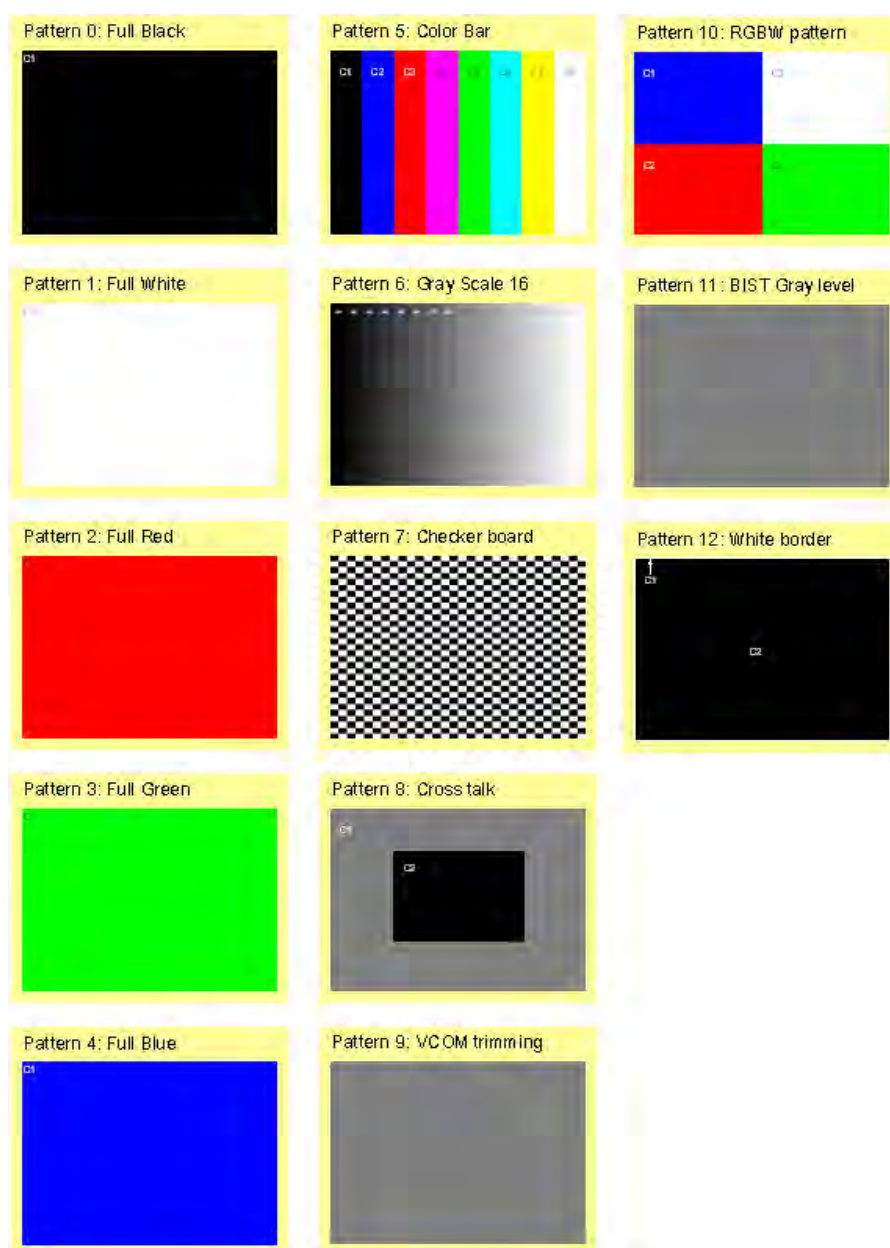
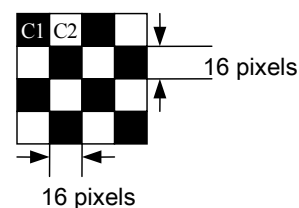
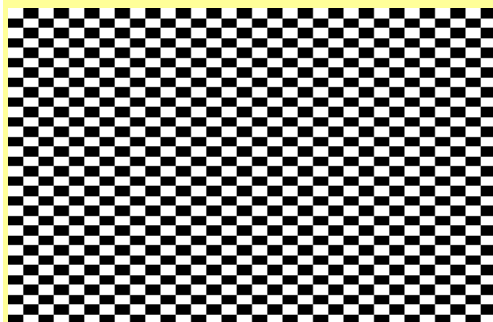
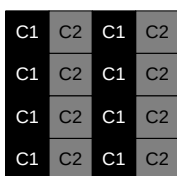


Figure 6.8: BIST patterns

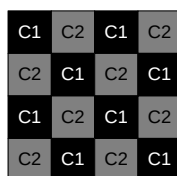
Pattern 7: Checker board



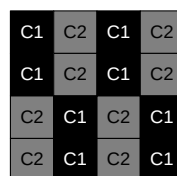
Column inversion



3 dot (line) inversion



6 dot (2 line) inversion



Dot inversion

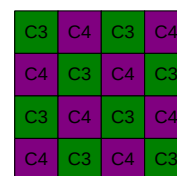


Figure 6.10: BIST pattern 9: flicker pattern

PTSEL[2:0]	Pattern name	Color	R	G	B
0	Black	C1	0	0	0
1	White	C1	255	255	255
2	Red	C1	255	0	0
3	Green	C1	0	255	0
4	Blue	C1	0	0	255
5	Color Bar	C1	0	0	0
		C2	0	0	255
		C3	255	0	0
		C4	255	0	255
		C5	0	255	0
		C6	0	255	255
		C7	255	255	0
		C8	255	255	255
6	16 Grayscale	C1	0	0	0
		C2	17	17	17
		C3	34	34	34
		C4	51	51	51
		C5	68	68	68
		C6	85	85	85
		C7	102	102	102
		C8	119	119	119
		C9	136	136	136
		C10	153	153	153
		C11	170	170	170
		C12	187	187	187
		C13	204	204	204
		C14	221	221	221
		C15	238	238	238
		C16	255	255	255
7	Checker board (16x16)	C1	0	0	0

		C2	255	255	255
8	Cross talk	C1	128	128	128
		C2	0	0	0
9	Flicker for VCOM trimming	C1	0	0	0
		C2	128	128	128
		C3	0	128	0
		C4	128	0	128
10	RGBW	C1	0	0	255
		C2	255	0	0
		C3	255	255	255
		C4	0	255	0
11	Gray selected by BIST_GRAY[7:0]	C1	BIST_GRAY[7:0]	BIST_GRAY[7:0]	BIST_GRAY[7:0]
12	White border	C1	0	0	0
		C2	255	255	255
13, 14	Black	C1	0	0	0
15	Auto loop from pattern 0 to pattern 12 (default)				

Table 6.1: BIST patterns

6.5 Protection function

6.5.1 GAS mode

When power is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS (gate all select) function can speed the process that image disappears.

HX8278-A-LT can detect abnormally low voltage and discharge LCD panel to prevent image sticking.

Any one of the following cases with duration larger than 10usec will trigger GAS function.

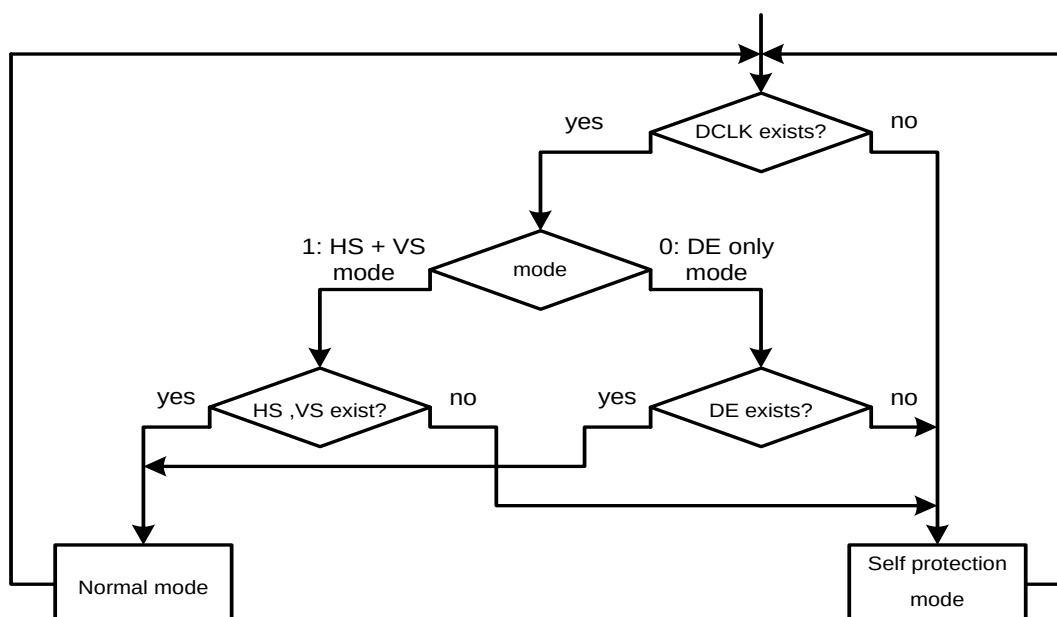
- A. VDD1/2 is lower than 2.4V
- B. AVDDP is lower than 4V
- C. AVDDN is higher than -4V

6.5.2 Self protection mode

HX8278-A-LT keeps detecting input signals DE, HS, VS, and DCLK. If any of these signals is missing, the chip will enter self protection mode and display black or white pattern set by register SPFSEL. For the four typical resolutions, frame rate in self protection mode is set to 60Hz. When adjustable resolution is enabled (by setting GATEPASS[3:0] or HSETPASS[3:0]), internal clock frequency, horizontal blanking and vertical blanking can be set in the same way to BIST mode.

Note that it is forbidden to power on with self protection mode. All input signals (clock, DE in DE mode, HS and VS in SYNC mode) should be supplied before STBYB is set to high.

Also note that TPSYNC can be used to indicate self protection mode (and GAS mode) by setting TPSYNC_FAIL_ENB to 0.



6.6 CRC

CRC (cyclic redundancy check) function is provided to check input RGB data. For each frame, RGB data is calculated with selected polynomial (CRC-24, CRC-16CCITT or CRC-8-ATM) and initial value. The order of RGB input data can be selected.

The calculated result CRC_SUMO[23:0] is then compared to predicted result CRC_SUMI[23:0]. If calculated result does not match the predicted result, an error flag will be set. Errors are counted and can be checked on CRC_ERRCNT[15:0] register. CRC_SUMO[23:0] can also be read out in selected order.

Note that calculated result of the Nth frame can be read in the (N+1)th frame, predicted result should also be given in the (N+1)th frame, and the error flag is available in the (N+2)th frame.

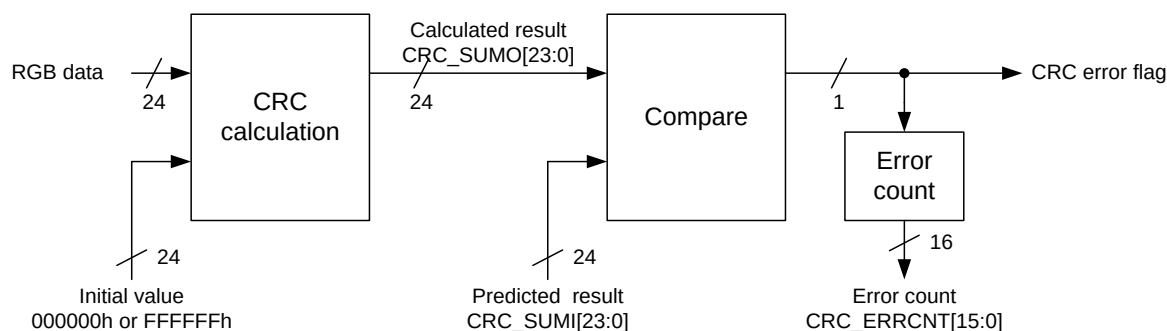
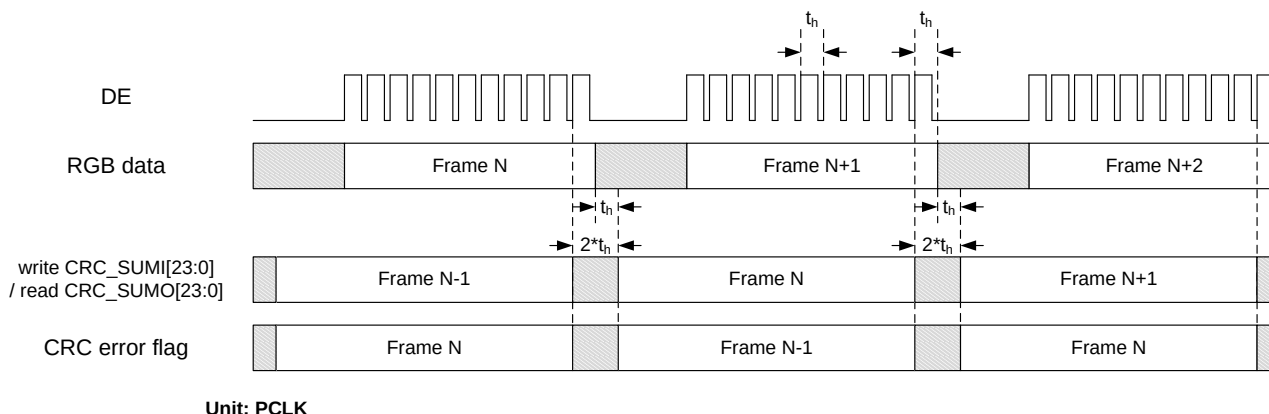


Figure 6.12: CRC

CRC type	CRC polynomial
24-bit (CRC-24)	$X^{24} + X^{23} + X^{18} + X^{17} + X^{14} + X^{11} + X^{10} + X^7 + X^6 + X^5 + X^4 + X^3 + X^1 + 1$
16-bit (CRC-16CCITT)	$X^{16} + X^{12} + X^5 + 1$
8-bit (CRC-8-ATM)	$X^8 + X^2 + X + 1$

Table 6.2: CRC types



Unit: PCLK

Figure 6.13: CRC timing

6.7 TPSYNC for touch panel synchronization

HX8278-A-LT provides an output pin TPSYNC for touch panel synchronization. It can be selected to be shifted (a delay version of) HS, shifted VDEN, shifted VS or TPS by page 0 register TPSYNCS[2:0]. Signals of failure detection FFLAG and GAS can also be selected.

TPS is an internal signal similar to source driving signals S_bank[0:2], with adjustable offset Ttpd. TPS can be stopped or kept toggling in vertical blanking period, depending on value of TPSVBEN.

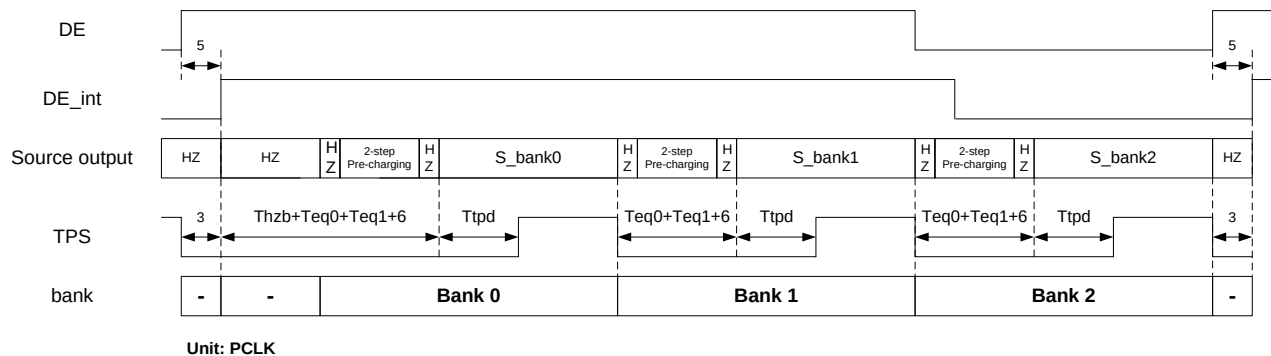


Figure 6.14: TPSYNC: TPS timing

Shifted VS refers to VS in sync mode, and refers to DE in DE mode.

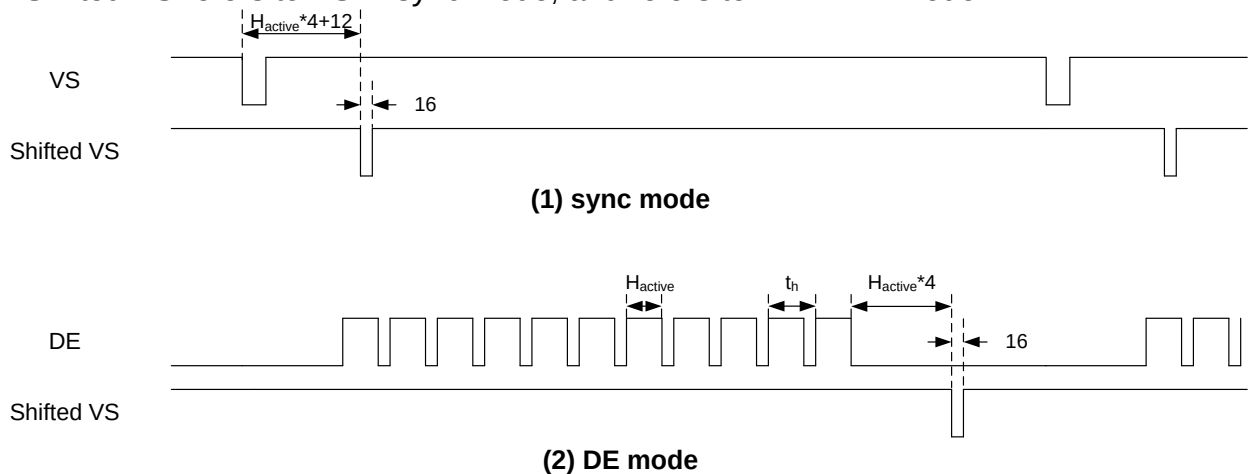


Figure 6.15: TPSYNC: shifted VS timing

Shifted HS refers to HS. Width of its low state is same to HS.

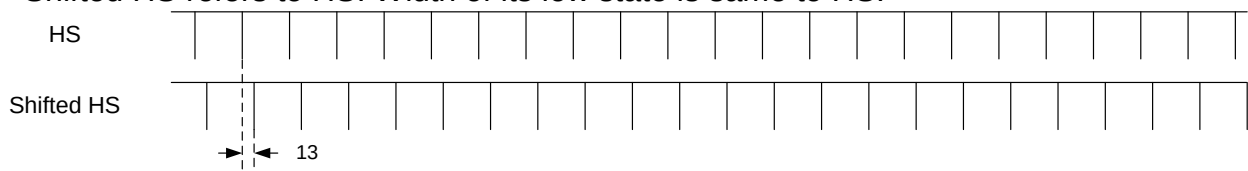


Figure 6.16: TPSYNC: shifted HS timing

VDEN refers to DE. In sync mode DE is calculated with HS and horizontal back porch (t_{hbp}).

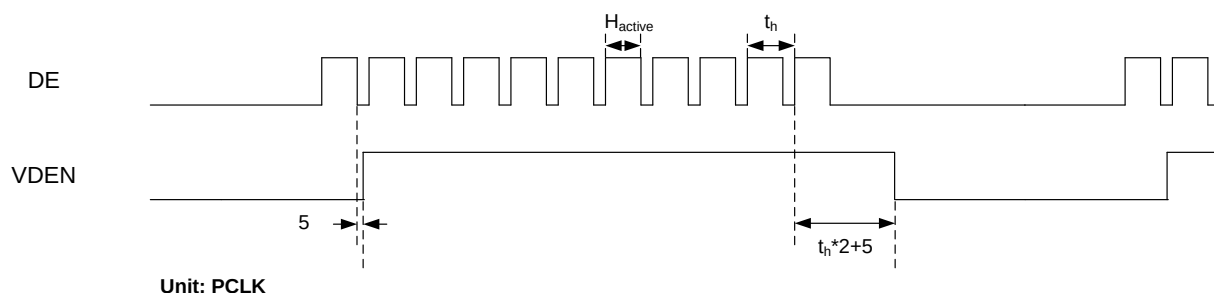


Figure 6.17: TPSYNC: VDEN timing

6.8 Failure detection

HX8278-A-LT is able to detect internal failure and provide detection results in several ways. Eight failure modes are detected, and eight error flags can be read out from read-only register R7Ah of page 0. The detection of each mode can be disabled by setting register R1Eh of page 0.

Error flag	Enable	Failure mode
FDEF[0]	FDENB[0]	LVDS unlock
FDEF[1]	FDENB[1]	VDD low
FDEF[2]	FDENB[2]	Source data latch fail
FDEF[3]	FDENB[3]	CRC error
FDEF[4]	FDENB[4]	Input signals from TTL/LVDS abnormal
FDEF[5]	FDENB[5]	EEPROM reload fail
FDEF[6]	FDENB[6]	OTP programming fail
FDEF[7]	FDENB[7]	OTP reload fail

Table 6.3: Eight failure modes

A signal FFLAG is also provided as an overall indication of failure. It is normally low, and any one of the eight failure modes will set FFLAG to high. FFLAG is able to output from output pin TPSYNC by setting TPSYNCS[2:0] = 100b, and / or output pin TESTO0 by setting FFLAGEN = 1. The polarity of FFLAG can be inversed by setting register FFLAGPOL.

6.9 Dynamic settings controlled by external temperature sensor

Voltages relating to panel display (including VGMPH/PL/NH/NL, VCOM, VGH/L) and digital gamma settings are able to change with temperature, depending on register values TS_SEL[1:0] coming from external temperature sensor.

When TS_VEN is set to 1, dynamic settings of voltages is enabled. Note that dynamic voltage settings are supported by OTP and EEPROM.

TS_VEN	TS_VGMEN	TS_SEL[1:0]		Effective settings	Note
0	X	X	X	VGMPHS/PLS/NHS/NLS[4:0]	Default
1	0	X	X		-
1	1	0	0		
		0	1	VGMPHS/PLS/NHS/NLS_LT[4:0]	
		1	X	VGMPHS/PLS/NHS/NLS_HT[4:0]	-

Table 6.4: Dynamic gamma reference settings

TS_VEN	TS_VCOMEN	TS_SEL[1:0]		Effective settings	Note
0	X	X	X	VCOMS[7:0]	Default
1	0	X	X		-
1	1	0	0		
		0	1	VCOMS_LT[7:0]	
		1	X	VCOMS_HT[7:0]	-

Table 6.5: Dynamic VCOM settings

TS_VEN	TS_VGHLEN	TS_SEL[1:0]		Effective settings	Note
0	X	X	X	VGHS[3:0], VGLS[2:0]	Default
1	0	X	X	VGHS[3:0], VGLS[2:0]	-
1	1	0	0	VGHS[3:0], VGLS[2:0]	
		0	1	VGHS_LT[3:0], VGLS_LT[2:0]	
		1	X	VGHS_HT[3:0], VGLS_HT[2:0]	-

Table 6.6: Dynamic VGH and VGL settings

When TS_DGMEN[1] is set to 1, dynamic settings of digital gamma is enabled. Two sets of digital gamma register values W1 and W2 should be stored in OTP, and the selected set will be loaded from OTP and be effective. Digital gamma settings can either selected by TS_SEL[1:0], or manually by a bit TS_DGM_MS. Note that dynamic digital gamma settings are not supported by EEPROM.

TS_DGMEN[1:0]		TS_SEL[1:0]		TS_DG_M_RT	TS_DG_M_MS	Effective settings	Note
0	X	X	X	X	X	If W2 is programmed, load W2. Else load W1.	Default
1	0	0	0	0	X	W2	-
		0	0	1	X	W1	-
		0	1	X	X	W1	
		1	X	X	X	W2	
1	1	X	X	X	0	W2	
					1	W1	

Table 6.7: Dynamic digital gamma settings

6.10 Multiple frame polarity control and INTL

Suppose a “P frame” is defined as the first source output starting with positive polarity, and an “N frame” is defined as starting with negative polarity. Normally frame polarity is changed by frame, that is odd frames are P frames and even frames are N frames.

P frame						N frame						P frame						N frame					
+	-	+	-	+	-	-	+	-	+	-	+	+	-	+	-	+	-	-	+	-	+	-	+
-	+	-	+	-	+	+	-	+	-	+	-	+	-	+	-	+	-	-	+	-	+	-	+
+	-	+	-	+	-	-	+	-	+	-	+	+	-	+	-	+	-	-	+	-	+	-	+
-	+	-	+	-	+	+	-	+	-	+	-	+	-	+	-	+	-	-	+	-	+	-	+
+	-	+	-	+	-	-	+	-	+	-	+	+	-	+	-	+	-	-	+	-	+	-	+
-	+	-	+	-	+	+	-	+	-	+	-	+	-	+	-	+	-	-	+	-	+	-	+

Example 1: dot inversion

Example 2: 3 dot inversion

Figure 6.18: Definition of frame polarity

It is able to be inversed periodically for 2^K frames by setting MFPCS[3:0] to K, maximum period is 4096 frames. In the first frame of each period, VCOM value VCOMS[7:0] is added an offset VCOMSOFS[7:0] ranging from -127 to +127.

(1) Normal: K=0

frame #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P/N frame	P	N	P	N	P	N	P	N	P	N	P	N	P	N	P	N
VCOM offset																

(2) K=1, period = 2 frames

frame #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P/N frame	P	N	N	P	P	N	N	P	P	N	N	P	P	N	N	P
VCOM offset	o		o		o		o		o		o		o		o	

(3) K=2, period = 4 frames

frame #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P/N frame	P	N	P	N	N	P	N	P	P	N	P	N	N	P	N	P
VCOM offset	o				o				o				o			

Figure 6.19: Multiple frame polarity control

INTL function for interlaced input is a simple special case that period is two frames, i.e. K=1. It can be enabled either by input pin INTL or register.

(1) Normal: INTL=0

frame #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P/N frame	P	N	P	N	P	N	P	N	P	N	P	N	P	N	P	N
VCOM offset																

(2) INTL=1: period = 2 frames, no VCOM offset

frame #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P/N frame	P	N	N	P	P	N	N	P	P	N	N	P	P	N	N	P
VCOM offset																

Figure 6.20: INTL function

6.11 SPI Interface

HX8278-A-LT supports 4-wire SPI (**serial peripheral interface**) to set internal registers. Setting one command needs 16 SCL clocks. Note that ATREN should be set to low when accessing SPI.

The first bit R/W selects read/write mode. Setting R/W to 0 selects write mode, and setting R/W to 1 selects read mode.

- A. A[6:0] specify the address of the register to be read or written.
- B. D[7:0] is the 8-bit data of each register.

The address and data are transferred from the MSB to LSB edge sequentially at SCL rising edge.

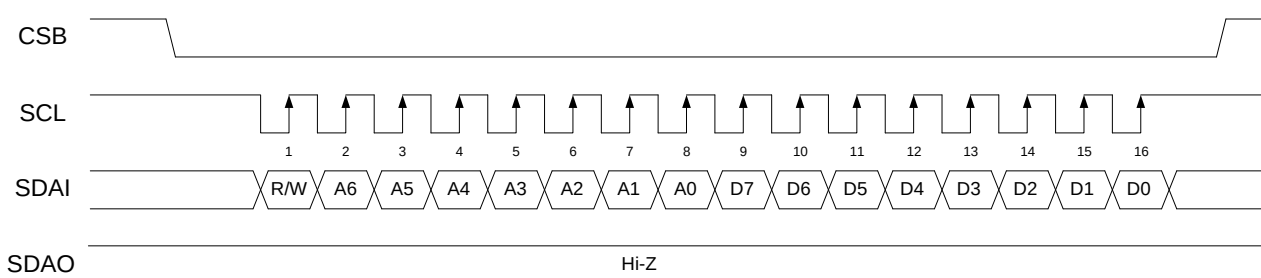


Figure 6.21: SPI signals, normal write mode

6.11.1 SPI normal read/write mode

In normal write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

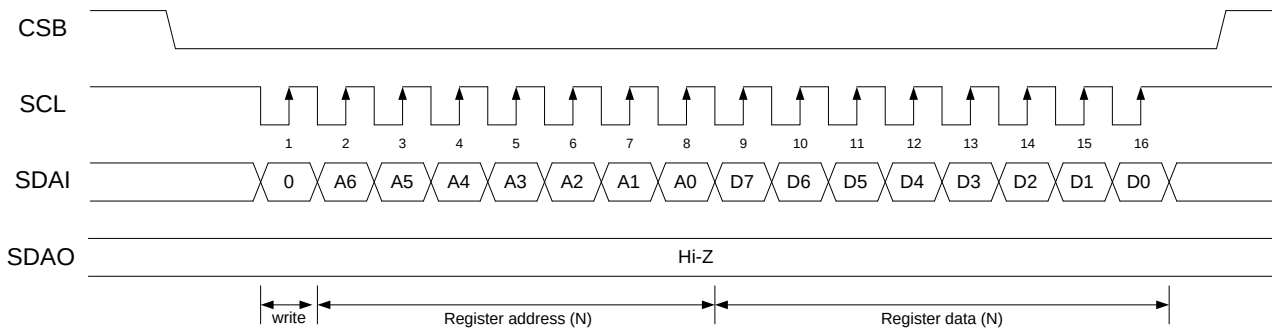


Figure 6.22: SPI signals, normal write mode

In normal read mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

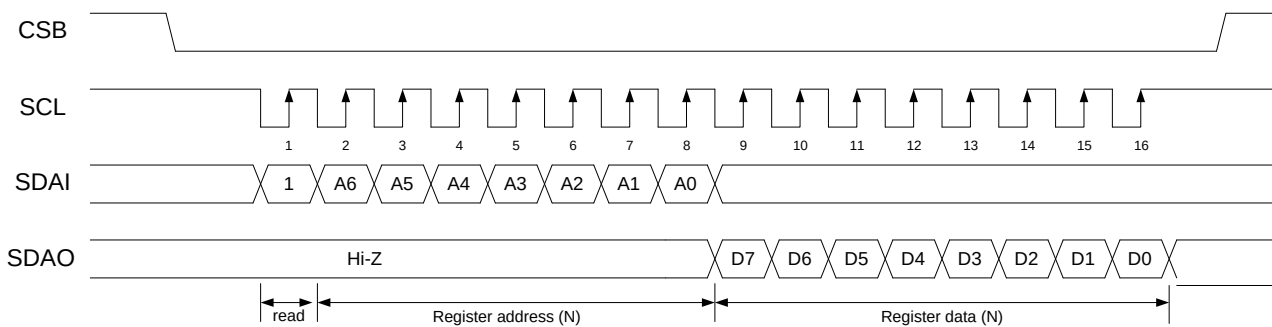


Figure 6.23: SPI signals, normal read mode

6.11.2 SPI burst write mode

HX8278-A-LT supports burst mode for writing all registers one time. After choose page want to write , Only the start address is needed, and repeats one set of 8 SCL pulses to access the following registers sequentially.

In burst write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

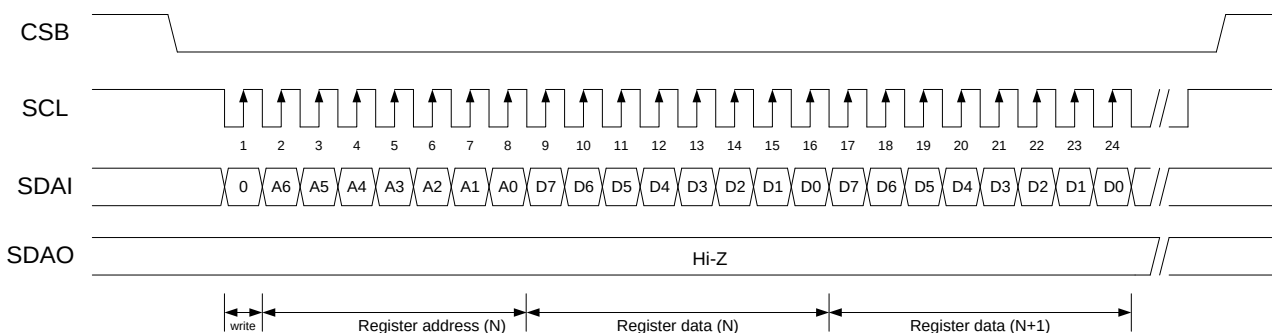


Figure 6.24: SPI signals, burst write mode

In burst write mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

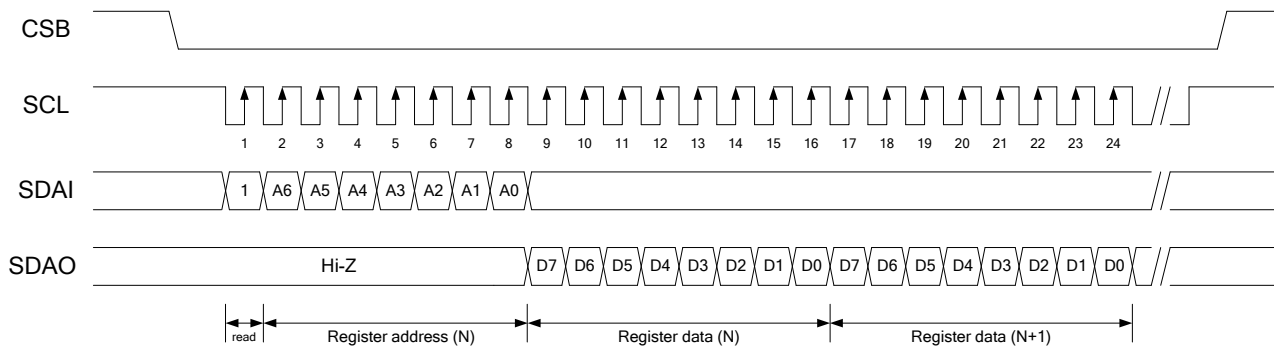
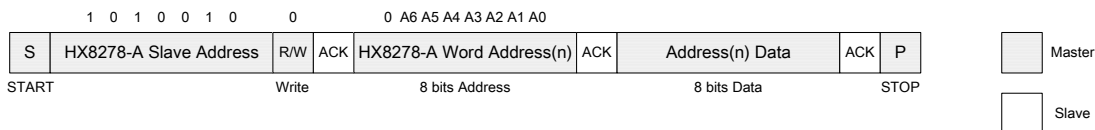


Figure 6.25: SPI signals, burst read mode

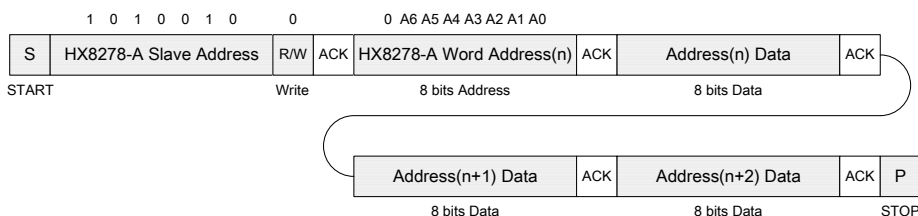
6.12 I2C Interface

HX8278-A-LT supports 2-wire serial interface (I2C) to set internal registers. HX8278-A-LT is a slave and the slave address is fixed 1010010. Note that ATREN should be set to low when accessing I2C.

Byte write



Burst write



Byte read



Burst read

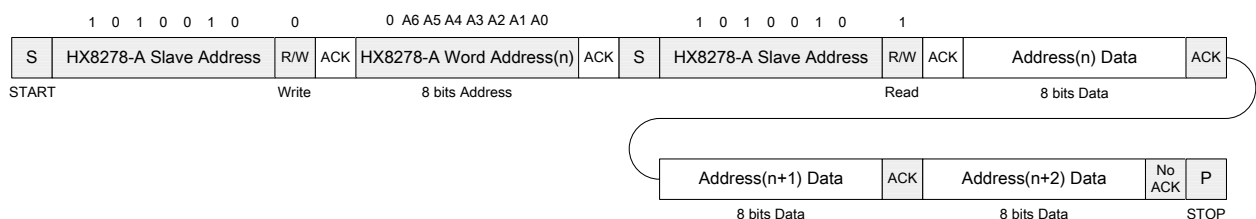


Figure 6.26: I2C format

6.13 OTP

Register values can be stored in OTP. Registers belong to OTP group 6 and 13 can be programmed for 10 times, and group 15~20 can be programmed for two times. The others groups can be programmed by three times.

OTP programming flow is shown as below. The failure detection function will detect OTP trimming status. Register FEDF[6] (page 0, R7Ah[6] or page 1, R0Fh[0]) indicates OTP programming error.

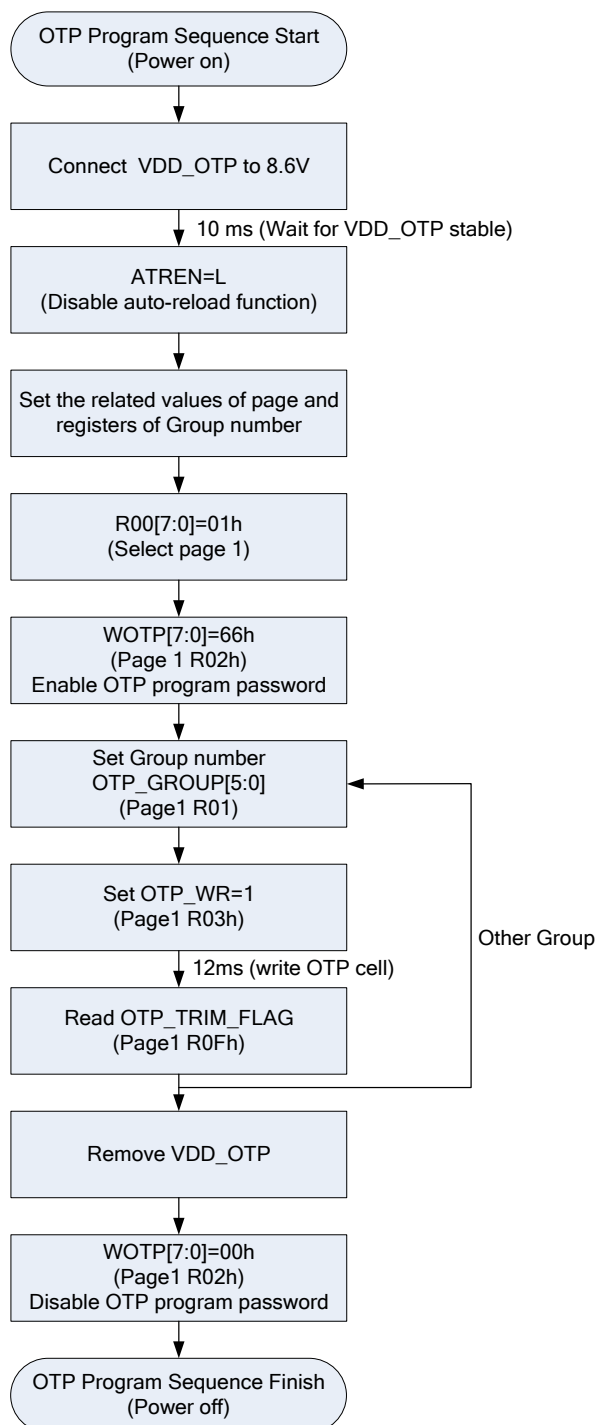


Figure 6.27: OTP program flow

7. Input / Output Timing

7.1 Display data input timing

7.1.1 Parallel RGB or LVDS in Sync mode

• Horizontal

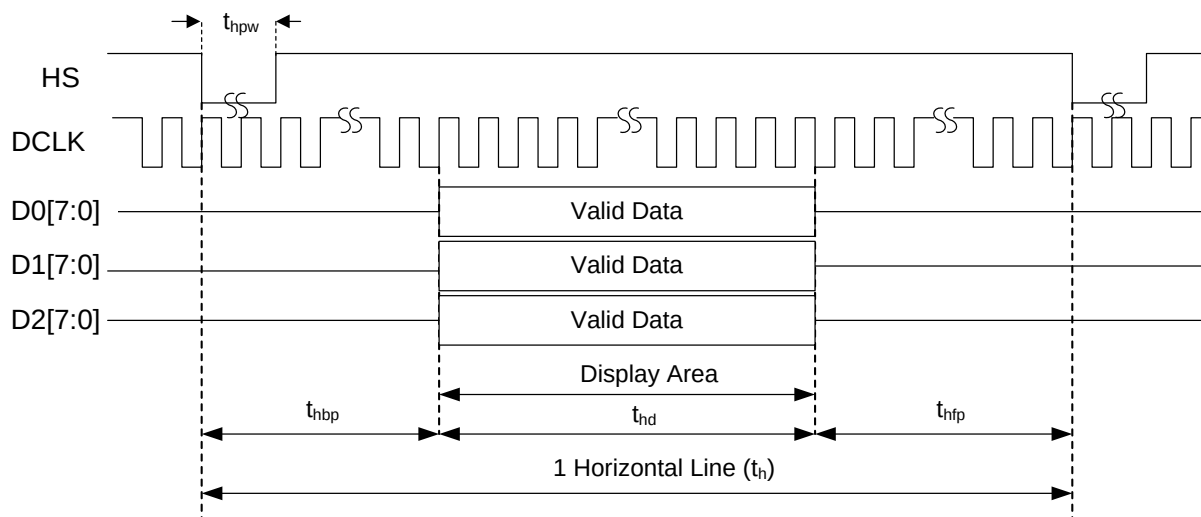


Figure 7.1: Horizontal input timing in Sync mode

• Vertical

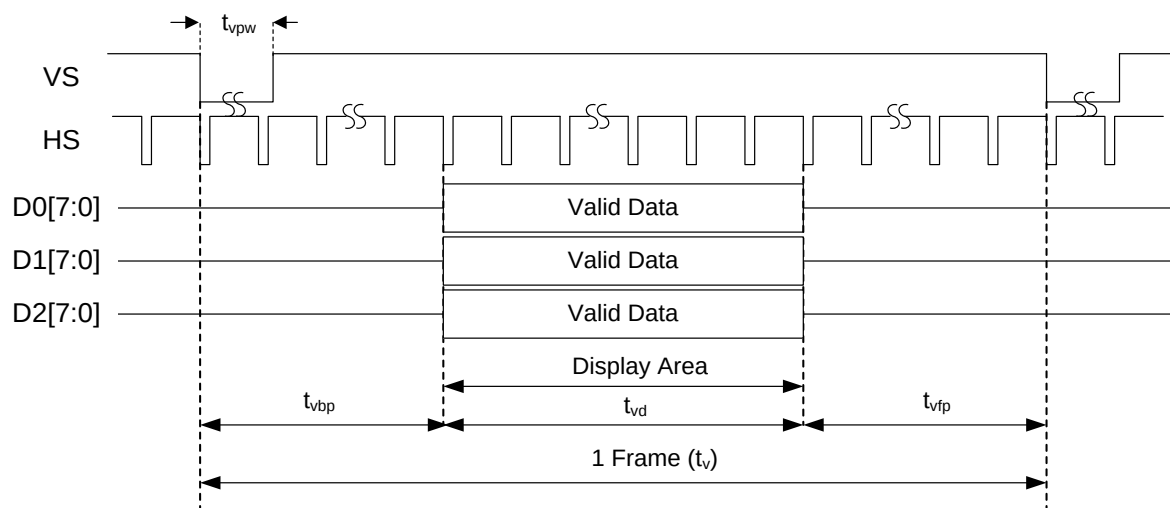


Figure 7.2: Vertical input timing in Sync mode

Parameter	Symbol	Panel Resolution									Unit
		480 RGBx280			480 RGBx272			400 RGBx240			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		9.31			9.05			6.82		MHz
Horizontal valid data	t _{hd}	480			480			400			DCLK
Hsync pulse Width	t _{hpw}	11	16	127	11	16	127	11	16	127	DCLK
Hsync back porch	t _{hbp}	6	16	127	6	16	127	6	16	127	DCLK
Hsync front porch	t _{hfp}	24	28	255	24	28	255	24	28	255	DCLK
1 horizontal line	t _h	510	524	862	510	524	862	430	444	782	DCLK
Vertical valid data	t _{vd}	280			272			240			H
Vsync pulse width	t _{vpw}	1	3	20	1	3	20	1	3	20	H
Vsync back porch	t _{vbp}	4	8	127	4	8	127	4	8	127	H
Vsync front porch	t _{vfp}	4	8	127	4	8	127	4	8	127	H
1 vertical field	t _v	288	296	534	280	288	526	248	256	494	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		360 RGBx240			320 RGBx240			Hactive RGBxVactive			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		6.21			5.59					MHz
Horizontal valid data	t _{hd}	360			320			Hactive			DCLK
Hsync pulse Width	t _{hpw}	11	16	127	11	16	127	11	16	127	DCLK
Hsync back porch	t _{hbp}	6	16	127	6	16	127	6	16	127	DCLK
Hsync front porch	t _{hfp}	24	28	255	24	28	255	24	28	255	DCLK
1 horizontal line	t _h	390	404	742	350	364	702	Hactive +30	Hactive +44	Hactive +382	DCLK
Vertical valid data	t _{vd}	240			240			Vactive			H
Vsync pulse width	t _{vpw}	1	3	20	1	3	20	1	3	20	H
Vsync back porch	t _{vbp}	4	8	127	4	8	127	4	8	127	H
Vsync front porch	t _{vfp}	4	8	127	4	8	127	4	8	127	H
1 vertical field	t _v	248	256	494	248	256	494	Vactive +8	Vactive +16	Vactive +254	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Note: (1) FR (Frame rate) = $F_{DCLK} / t_h / t_v$.

(2) Horizontal back-porch can be adjusted in Sync mode by register R07h of page 0.

(3) Vertical back-porch can be adjusted in Sync mode by register R06h of page 0.

(4) $t_h = t_{hbp} + t_{hfp} + t_{hd}$ and $t_v = t_{vbp} + t_{vfp} + t_{vd}$.

Table 7.1: Input timing of parallel RGB or LVDS in Sync mode

7.1.2 Serial RGB in Sync mode

Parameter	Symbol	Panel Resolution									Unit
		480 RGBx280			480 RGBx272			400 RGBx240			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		26.36			25.64			19.11		MHz
Horizontal valid data	t _{hd}	1440			1440			1200			DCLK
Hsync pulse Width	t _{hpw}	11	16	127	11	16	127	11	16	127	DCLK
Hsync back porch	t _{hbp}	6	16	127	6	16	127	6	16	127	DCLK
Hsync front porch	t _{hfp}	24	28	255	24	28	255	24	28	255	DCLK
1 horizontal line	t _h	1530	1484	1822	1530	1484	1822	1290	1244	1582	DCLK
Vertical valid data	t _{vd}	280			272			240			H
Vsync pulse width	t _{vpw}	1	3	20	1	3	20	1	3	20	H
Vsync back porch	t _{vbp}	4	8	127	4	8	127	4	8	127	H
Vsync front porch	t _{vfp}	4	8	127	4	8	127	4	8	127	H
1 vertical field	t _v	288	296	534	280	288	526	248	256	494	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		360 RGBx240			320 RGBx240			Hactive RGBxVactive			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		17.26			15.42					MHz
Horizontal valid data	t _{hd}	1080			960			Hactive*3			DCLK
Hsync pulse Width	t _{hpw}	11	16	127	11	16	127	11	16	127	DCLK
Hsync back porch	t _{hbp}	6	16	127	6	16	127	6	16	127	DCLK
Hsync front porch	t _{hfp}	24	28	255	24	28	255	24	74	255	DCLK
1 horizontal line	t _h	1170	1124	1462	1050	1004	1342	Hactive*3 +90	Hactive*3 +90	Hactive*3 +382	DCLK
Vertical valid data	t _{vd}	240			240			Vactive			H
Vsync pulse width	t _{vpw}	1	3	20	1	3	20	1	3	20	H
Vsync back porch	t _{vbp}	4	8	127	4	8	127	4	8	127	H
Vsync front porch	t _{vfp}	4	8	127	4	8	127	4	8	127	H
1 vertical field	t _v	248	256	494	248	256	494	Vactive +8	Vactive +16	Vactive +254	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Note: (1) FR (Frame rate) = $F_{DCLK} / t_h / t_v$.

(2) Horizontal back-porch can be adjusted in Sync mode by register R07h of page 0.

(3) Vertical back-porch can be adjusted in Sync mode by register R06h of page 0.

(4) $t_h = t_{hbp} + t_{hfp} + t_{hd}$ and $t_v = t_{vbp} + t_{vfp} + t_{vd}$.

Table 7.2: Input timing of serial RGB in Sync mode

7.1.3 Parallel RGB or LVDS in DE mode

In DE mode only DE signal is needed.

• Horizontal

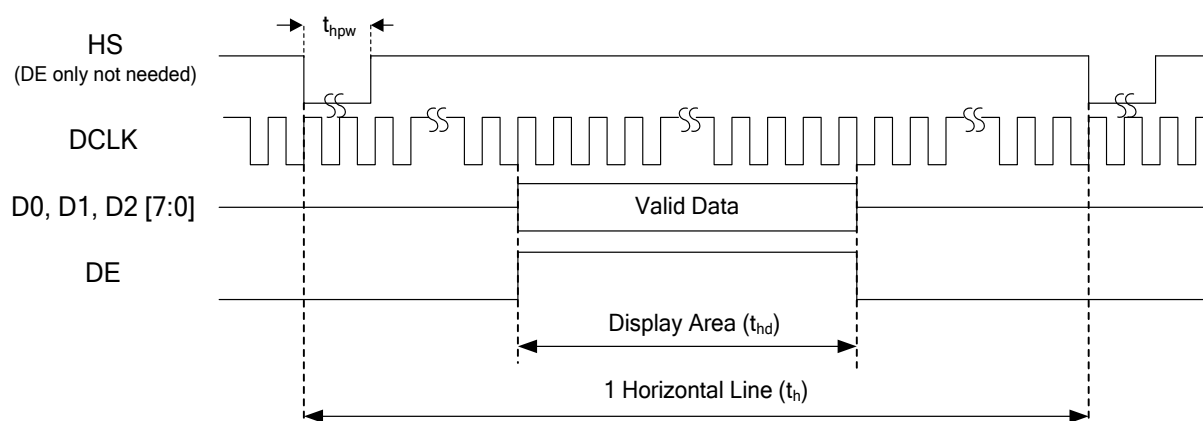


Figure 7.3: Horizontal input timing in DE mode

• Vertical

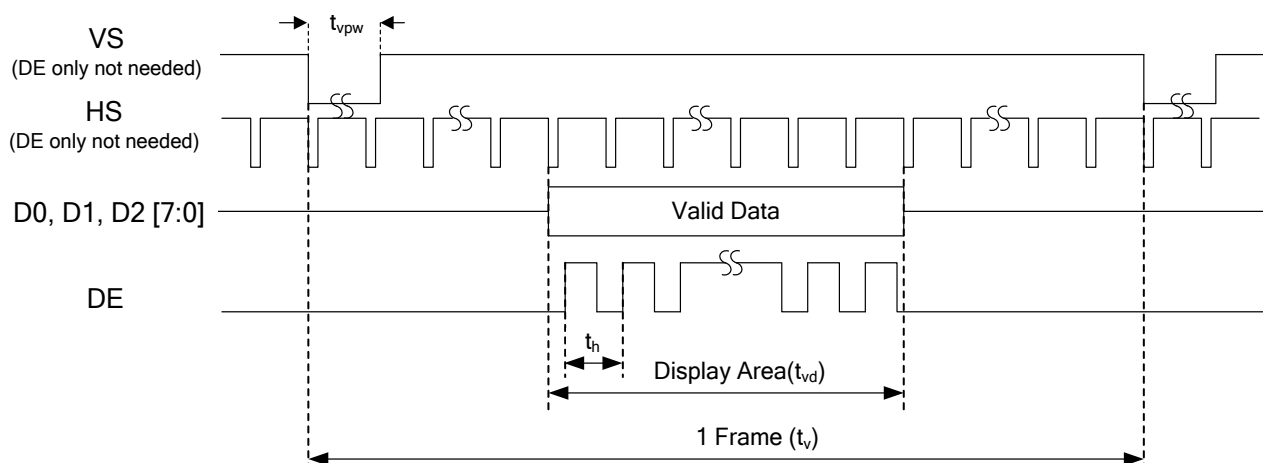


Figure 7.4: Vertical input timing in DE mode

Parameter	Symbol	Panel Resolution									Unit
		480 RGBx280			480 RGBx272			400 RGBx240			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		9.31			9.05			6.82		MHz
Horizontal valid data	t _{hd}	480			480			400			DCLK
1 horizontal line	t _h	510	524	862	510	524	862	430	444	782	DCLK
Vertical valid data	t _{vd}	280			272			240			H
1 vertical field	t _v	288	296	534	280	288	526	248	256	494	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		360 RGBx240			320 RGBx240			Hactive RGBxVactive			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		6.21			5.59					MHz
Horizontal valid data	t _{hd}	360			320			Hactive			DCLK
1 horizontal line	t _h	390	404	742	350	364	702	Hactive +30	Hactive +44	Hactive +382	DCLK
Vertical valid data	t _{vd}	240			240			Vactive			H
1 vertical field	t _v	248	256	494	248	256	494	Vactive +8	Vactive +16	Vactive +254	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Note:

(1) FR (Frame rate) = $F_{DCLK} / t_h / t_v$.

(2) Vertical blanking ($t_v - t_{vd}$, in unit of time) should be smaller than 4ms, or the chip will enter self protection mode.

Table 7.3: Input timing of parallel RGB or LVDS in DE mode

7.1.4 Serial RGB in DE mode

Parameter	Symbol	Panel Resolution									Unit
		480 RGBx280			480 RGBx272			400 RGBx240			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		26.36			25.64			19.11		MHz
Horizontal valid data	t _{hd}	1440			1440			1200			DCLK
1 horizontal line	t _h	1530	1484	1822	1530	1484	1822	1290	1244	1582	DCLK
Vertical valid data	t _{vd}	280			272			240			H
1 vertical field	t _v	288	296	534	280	288	526	248	256	494	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		360 RGBx240			320 RGBx240			Hactive RGBxVactive			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F _{DCLK}		17.26			15.42					MHz
Horizontal valid data	t _{hd}	1080			960			Hactive*3			DCLK
1 horizontal line	t _h	1170	1124	1462	1050	1004	1342	Hactive*3 +90	Hactive*3 +90	Hactive*3 +382	DCLK
Vertical valid data	t _{vd}	240			240			Vactive			H
1 vertical field	t _v	248	256	494	248	256	494	Vactive +8	Vactive +16	Vactive +254	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Note:

(1) FR (Frame rate) = $F_{DCLK} / t_h / t_v$.

(2) Vertical blanking ($t_v - t_{vd}$, in unit of time) should be smaller than 4ms, or the chip will enter self protection mode.

Table 7.4: Input timing of serial RGB in DE mode

7.2 Reset input timing

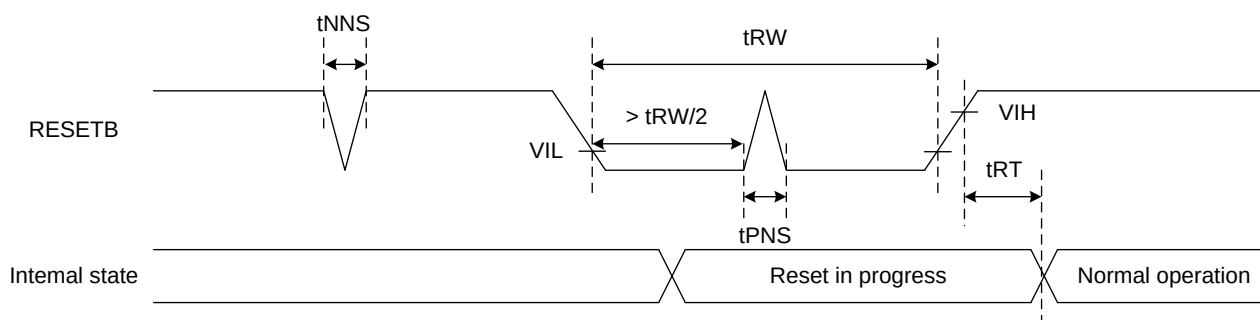


Figure 7.5: Reset input timing

(VDD1=VDD2=3.0 to 3.6V, GND=0V, $T_A=-40$ to $+105$ °C)

Signal	Parameter	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	t_{RW}	15	-	-	μs
	Reset complete time	t_{RT}	-	-	5	μs
	Positive spike noise width	t_{PNS}	-	-	TBD	ns
	Negative spike noise width	t_{NNS}	-	-	1	us

Table 7.5: Reset timing parameter

7.3 Output timing

HX8278-A-LT is a triple-gate driver. Output timing refers to the DE signal, coming from DE input pin or generated by HS signal.

Each display line is divided to three banks (bank 0 to bank 2) for three colors, by default $T_{bank0} = T_{bank1} = T_{bank2} = (H_{total} - 3 \cdot Th_{zb}) / 3$. Length of these banks can be adjusted by registers $BANK[1:0]OFS[5:0]$.

Gate and source output timing is shown below. Three banks of gate driving are controlled by adjusting $Toeb$ and $Toef$. Three banks of source driving is aligned to bank 0 to bank 2, and the pre-charging time $Teq0$ and $Teq1$ are adjustable.

Note: PCLK is pixel clock frequency, which equals to clock frequency (DCLK) in parallel RGB and LVDS modes, and is 1/3 of clock frequency in serial RGB mode.

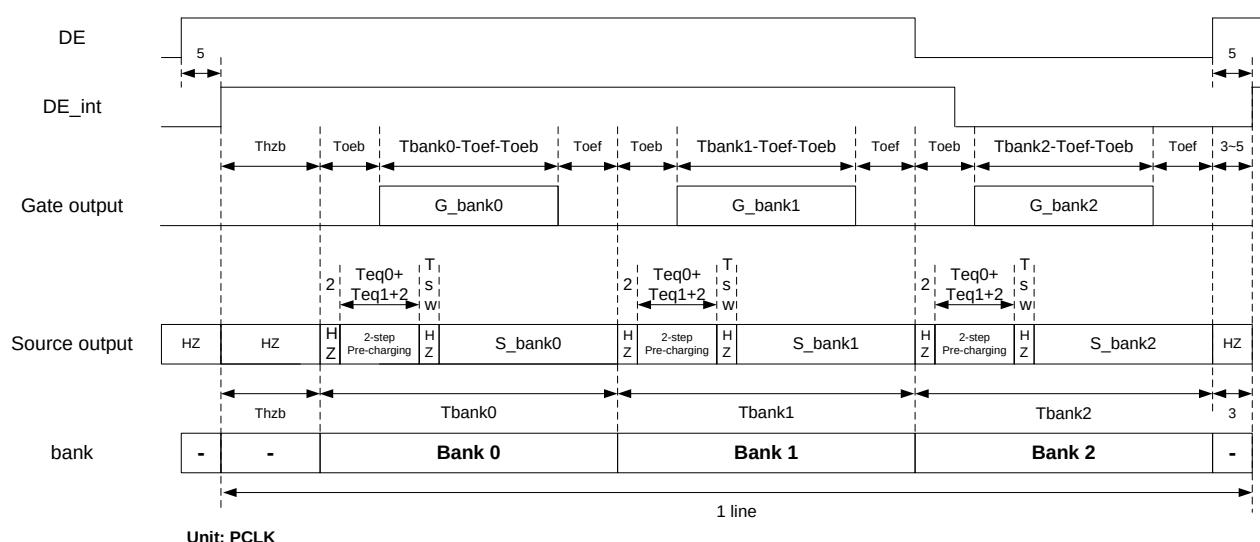


Figure 7.6: Gate and source output timing of one line

Source output timing of one bank is shown below. For each bank, if the polarity is different to the previous bank, source output is 2-step pre-charged to VSS and VDD/VCL. Source channels are separated to two groups that have different driving start time T_{sw} .

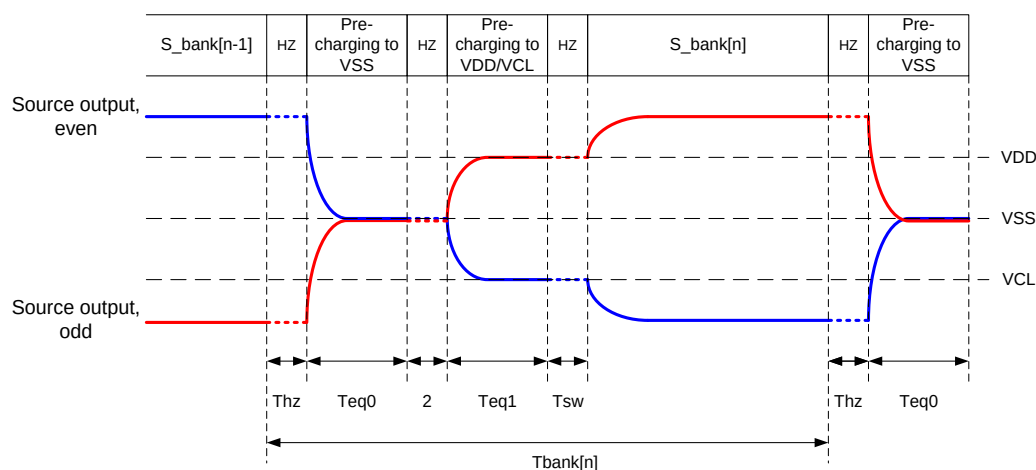


Figure 7.7: Source output timing of one bank

8. Register Description

8.1 Register Table

8.1.1 Register table: Page 0 (Normal function)

Address	Default	Read/Write	D[7:0]	Name	Description	OTP group
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 00h for page 0.	-
01h	00h	R/W	[7:0]	STANDBY	Standby control.	-
02h	11h	R/W	[6]	TR	Interface selection.	Group 2, 3 times
			[5:4]	DINT[1:0]	Input format selection for TTL / LVDS interface.	
			[3]	-	Reserved	
			[2:1]	MODE[1:0]	Input timing selection for TTL / LVDS interface.	
			[0]	NB	Panel type selection.	
03h	30h	R/W	[7]	RL	Horizontal shift direction.	
			[6]	TB	Vertical shift direction.	
			[5:4]	INV[1:0]	Inversion type selection.	
			[2]	INTL	Interlaced or normal input.	
			[1:0]	RS[1:0]	Typical resolution selection.	
04h	00h	R/W	[7]	RBEXC	Exchange R data and B data.	
			[6]	HSP	HS polarity for TTL / LVDS interface.	
			[5]	VSP	VS polarity for TTL / LVDS interface.	
			[4]	CLOCKP	Clock polarity for TTL interface.	
			[1]	PON	Power on pattern selection.	
05h	CFh	R/W	[0]	POFF	Power off pattern selection.	
			[7]	GASEN	GAS function enable.	
			[6]	SPFEN	Self protection function enable.	
			[5]	SPFSEL	White/Black pattern selection in Self protection mode.	
			[4]	BISTEN	BIST mode enable.	
06h	05h	R/W	[7:0]	VBPP[7:0]	Vertical back porch adjustment.	Group 3, 3 times
07h	10h	R/W	[7:0]	HBP[7:0]	Horizontal back porch adjustment.	
08h	00h	R/W	[7:5]	-	Reserved	
			[4]	THZBS	Output timing Thzb control.	
			[3:2]	SD_VBLAST[1:0]	Set source output in the last line of V-blanking.	
			[1:0]	SD_VB[1:0]	Set source output in the V-blanking except last line.	
09h	88h	R/W	[7:6]	PCR[1:0]	Source buffer driving timing control.	
			[5]	ENDRV	Source buffer driving ability selection.	
			[4:0]	EQ0W[4:0]	Source output timing control.	
0Ah	60h	R/W	[7:5]	BC[2:0]	Source buffer bias current selection.	
			[4:0]	EQ1W[4:0]	Source output timing control.	
0Bh	00h	R/W	[7:4]	MFPCS[3:0]	Period of multiple frame polarity control.	
			[3:2]	POCSD[1:0]	Source buffer offset cancellation control.	
			[1:0]	POCGM[1:0]	Gamma buffer offset cancellation control.	
0Ch	00h	R/W	[7:0]	BANK0OFS[5:0]	Bank timing control.	Group 4, 3 times
0Dh	00h	R/W	[7:0]	BANK1OFS[5:0]	Bank timing control.	
0Eh	08h	R/W	[7]	-	Reserved.	
			[6:0]	TOEB[6:0]	Gate output timing control.	
0Fh	08h	R/W	[7]	-	Reserved.	
			[6:0]	TOEF[6:0]	Gate output timing control.	
10h	00h	R/W	[7:3]	-	Reserved.	
			[2:0]	GDSEQ[2:0]	Gate scan type selection.	
11h	80h	R/W	[7:0]	-	Reserved	
12h	80h	R/W	[7:0]	-	Reserved	
13h	80h	R/W	[7:0]	-	Reserved	
14h	0Ah	R/W	[7:4]	-	Reserved	
			[3:0]	GATEPASS[3:0]	Password to enable manual vertical resolution selection.	
15h	8Ch	R/W	[7:0]	GATENUM[7:0]	Adjustable vertical resolution selection.	Group 4, 3 times

Address	Default	Read/Write	D[7:0]	Name	Description	OTP group
16h	0Ah	R/W	[7:4]	-	Reserved	
			[3:0]	HSETPASS[3:0]	Password to enable adjustable horizontal resolution selection.	
17h	78h	R/W	[6:0]	HSETNUM[6:0]	Adjustable horizontal resolution selection	
18h	00h	R/W	[7:0]	BISTHBS[7:0]	Horizontal blanking selection in BIST and self protection mode.	
19h	00h	R/W	[7:4]	BISTVBS[3:0]	Vertical blanking selection in BIST and self protection mode.	Group 5, 3 times
			[1:0]	BISTCLKS[1:0]	Internal clock frequency selection in BIST and self protection mode.	
1Ah	43h	R/W	[7]	FFLAGPOL	FFLAG polarity selection.	
			[6]	TPSYNC_FAIL_ENB	Set TPSYNC state in GAS or SP mode.	
			[5]	FFLAGEN	TEST00 output FFLAG enable.	
			[4]	TPSVBEN	TPS signal state in vertical blanking selection.	
			[3]	TPSYNCPOL	TPSYNC polarity selection.	
			[2:0]	TPSYNCS[2:0]	TPSYNC output selection.	
1Bh	20h	R/W	[7:0]	TPS_OFS[7:0]	TPS signal offset Ttpd setting.	
1Ch	0Fh	R/W	[7:4]	-	Reserved	
			[3:0]	PTSEL[3:0]	BIST pattern selection.	Group 6, 10 times
1Dh	80h	R/W	[7:0]	BIST_GRAY[7:0]	BIST pattern 11 grayscale selection.	
1Eh	88h	R/W	[7:0]	FDENB[7:0]	Failure detection enable.	
1Fh	80h	R/W	[7:0]	VCOMS[7:0]	VCOM level selection.	Group 7, 3 times
20h	00h	R/W	[7:0]	VCOMSOFS[7:0]	VCOMS[7:0] offset value for multiply frame polarity control.	
21h	7Fh	R/W	[4]	VCOMEN	VCOM regulator enable	
			[3]	VGHEN	VGH charge pump enable	
			[2]	VGLEN	VGL charge pump enable	
			[1]	AVDDNEN	AVDDN charge pump enable	
			[0]	AVDDPEN	AVDDP charge pump enable	
22h	0Dh	R/W	[4:0]	AVDDPS[4:0]	AVDDP level selection.	
23h	0Dh	R/W	[4:0]	AVDDPS[4:0]	AVDDN level selection.	
24h	73h	R/W	[7:4]	VGHS[3:0]	VGH level selection.	
			[3]	Reserved	-	Group 8, 3 times
			[2:0]	VGLS[2:0]	VGL level selection.	
25h	14h	R/W	[4:0]	VGMPHS[4:0]	VGMPH level selection.	
26h	14h	R/W	[4:0]	VGMNHS[4:0]	VGMNH level selection.	
27h	03h	R/W	[3:2]	AVDD_FCP[1:0]	AVDDP & AVDDN charge pump period selection.	
			[1]	AVDDNX3	AVDDN boosting mode selection.	
			[0]	AVDDPX3	AVDDPboosting mode selection.	
28h	0Fh	R/W	[7]	VGHL_LIMIT	VGH-VGL voltage limiter enable.	
			[5:4]	VGHL_FCP[1:0]	VGH & VGL charge pump period selection.	
			[2]	VGLXS	VGL boosting mode selection.	
			[1:0]	VGHXS[1:0]	VGHboosting mode selection.	Group 9, 3 times
29h	F1h	R/W	[7]	VGMNHEN	VGMNH regulator enable.	
			[6]	VGMPHEN	VGMPH regulator enable.	
			[5]	Reserved	-	
			[1:0]	VCOMD[1:0]	VCOM driving capability selection.	
2Ah	00h	R/W	[4:0]	VGMPHS[4:0]	VGMPH level selection	
2Bh	00h	R/W	[4:0]	VGMNLS[4:0]	VGMNL level selection	
2Ch	AAh	R/W	[1]	GASLOADEN	Reload OTP/EEPROM or not when recovering from GAS mode.	
			[0]	COM_OTP	VCOMS[7:0] loaded from OTP or EEPROM	
2Dh	AAh				Reserved	
2Eh	FFh				Reserved	
2Fh	00h				Reserved	Group 9, 3 times
30h	00h				Reserved	
31h	00h	R/W	[7:0]	-	Reserved	
32h	00h	R/W	[7:0]	-	Reserved	
33h	00h	R/W	[7:0]	-	Reserved	
34h	00h	R/W	[7:0]	-	Reserved	
35h	00h	R/W	[7:0]	-	Reserved	

Address	Default	Read/Write	D[7:0]	Name	Description	OTP group	
36h	AAh	R/W	[7:0]	-	Reserved	Group 10, 3 times	
37h	FFh	R/W	[7:0]	-	Reserved		
38h	05h	R/W	[6]	DLL_BANK	LVDS frequency selection.		
			[5]	AGING	LVDS data lane enable in SP mode.		
			[4]	LVDS_FMT	LVDS data format selection.		
			[3:2]	LVDS_RXB[1:0]	LVDS receiver bias current selection.		
			[1:0]	LVDS_VB[1:0]	LVDS DLL bias current selection.		
39h	22h	R/W	[5:4]	LVDS_BW[1:0]	LVDS DLL bandwidth selection.		
		[3:0]	LVDS_CPB[3:0]	LVDS charge pump current selection.			
3Ah	00h	R/W	[2:0]	LVDS_TUNE_C[2:0]	Set delay of LVDS clock lane.		
3Bh	00h	R/W	[6:4]	LVDS_TUNE_D0[2:0]	Set delay of LVDS data lanes 0.		
			[3:0]	LVDS_TUNE_D1[2:0]	Set delay of LVDS data lanes 1.		
3Ch	00h	R/W	[6:4]	LVDS_TUNE_D2[2:0]	Set delay of LVDS data lanes 2.		
			[3:0]	LVDS_TUNE_D3[2:0]	Set delay of LVDS data lanes 3.		
3Dh	55h	R/W	[7:0]	-	Reserved		
3Eh	AAh	R/W	[7:0]	-	Reserved		
3Fh	00h	R/W	[2]	TS_VEN		Group 11, 3 times	
			[1:0]	TS_SEL1[0]			
40h	00h	R/W	[6:5]	TS_DGMEN[1:0]			
			[4]	TS_DGM_MS			
			[3]	TS_DGM_RT			
			[2]	TS_VGMEN			
			[1]	TS_VCOMEN			
			[0]	TS_VGHLEN			
41h	80h	R/W	[7:0]	VCOMS_HT[7:0]	VCOM level selection for HT.		Group 11, 3 times
42h	80h	R/W	[7:0]	VCOMS_LT[7:0]	VCOM level selection for LT.		
43h	73h	R/W	[7:4]	VGHS_HT[3:0]	VGH level selection for HT.		
			[2:0]	VGLS_HT[2:0]	VGL level selection for HT.		
44h	73h	R/W	[7:4]	VGHS_LT[3:0]	VGH level selection for LT.		
			[2:0]	VGLS_LT[2:0]	VGL level selection for LT.		
45h	34h	R/W	[4:0]	VGMPHS_HT[4:0]	VGMPH level selection for HT.		
46h	B4h	R/W	[2:0]	VGMNHS_HT[4:0]	VGMNH level selection for HT.		
47h	74h	R/W	[2:0]	VGMPHS_LT[4:0]	VGMPH level selection for LT.		
48h	74h	R/W	[2:0]	VGMNHS_LT[4:0]	VGMNH level selection for LT.		
49h	00h	R/W	[3]	VGMPLS_HT[4]	VGMPH level selection for HT, MSB.		
			[2]	VGMNLS_HT[4]	VGMNL level selection for HT, MSB.		
			[1]	VGMPLS_LT[4]	VGMPH level selection for LT, MSB.		
			[0]	VGMNLS_LT[4]	VGMNL level selection for LT, MSB.		
4Ah	00h	R/W	[7:4]	VGMPLS_HT[3:0]	VGMPH level selection for HT, LSB.		
			[3:0]	VGMNLS_HT[3:0]	VGMNL level selection for HT, LSB.		
4Bh	00h	R/W	[7:4]	VGMPLS_LT[3:0]	VGMPH level selection for LT, LSB.		
			[3:0]	VGMNLS_LT[3:0]	VGMNL level selection for LT, LSB.		
4Ch	00h	R/W	[6]	CRC_OUT_SWAP	CRC calculated data output order selection.	Group 12, 3 times	
			[5:4]	CRC_TYPE[1:0]	CRC type selection.		
			[3:2]	CRC_IN_SWAP[1:0]	CRC input RGB data order selection.		
			[1]	CRC_INI_SEL	CRC initial value selection.		
			[0]	CRC_EN	CRC function enable.		
4Dh	00h	R/W	[7:0]	CRC_SUMI[23:16]	Predicted CRC result input from the system.		
4Eh	00h	R/W	[7:0]	CRC_SUMI[15:8]			
4Fh	00h	R/W	[7:0]	CRC_SUMI[7:0]			
50h	10h	R/W	[7:0]	-	Reserved.	Group 13, 10 times	
51h	01h	R/W	[7:4]	CHIP_ID[3:0]	Chip ID.		
			[3:0]	VER_ID[3:0]	Version ID.		
52h	10h	R/W	[7:6]	-	Reserved.	Group 14, 3 times	
	10h	R/W	[5:0]	ROB[5:0]	Offset (Brightness) setting for red color.		
			[7:6]	-	Reserved.		
53h	10h	R/W	[5:0]	GOB[5:0]	Offset (Brightness) setting for green color.		
			[7:6]	-	Reserved.		
54h	10h	R/W	[5:0]	BOB[5:0]	Offset (Brightness) setting for blue color.		
			[7:0]	Rr_C[7:0]	Gain (contrast) of red		
56h	80h	R/W	[7:0]	Gg_C[7:0]	Gain (contrast) of green		

Address	Default	Read/Write	D[7:0]	Name	Description	OTP group
57h	80h	R/W	[7:0]	Bb_C[7:0]	Gain (contrast) of blue	
58h	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Rg_C[5:0]	G Gain of red	
59h	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Rb_C[5:0]	B Gain of red	
5Ah	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Gr_C[5:0]	R Gain of Green	
5Bh	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Gb_C[5:0]	B Gain of Green	
5Ch	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Br_C[5:0]	R Gain of blue	
5Dh	00h	R/W	[7:6]	-	Reserved.	
			[5:0]	Bg_C[5:0]	G Gain of blue	
5Eh	00h	R/W	[7:0]	-	Reserved	
71h	-	R	[7:0]	-	Reserved	
72h	-	R	[7:0]	-	Reserved	
73h	-	R	[7:0]	CRC_SUMO[23:16]	CRC calculated result output.	
74h	-	R	[7:0]	CRC_SUMO[15:8]	CRC calculated result output.	
75h	-	R	[7:0]	CRC_SUMO[7:0]	CRC calculated result output.	
76h	-	R	[7:0]	CRC_ERR_CNT[15:8]	CRC error count.	
77h	-	R	[7:0]	CRC_ERR_CNT[7:0]	CRC error count.	
78h	-	R	[7:0]	-	Reserved	
79h	-	R	[7:0]	-	Reserved	
7Ah	-	R	[7:0]	FDEF[7:0]	Error flags of failure detection. (Read-only)	
7Bh	82h	R	[7:0]	CHIPNAME[2][7:0]	Chip name 0. (Read-only)	
7Ch	78h	R	[7:0]	CHIPNAME[1][7:0]	Chip name 1. (Read-only)	
7Dh	0Ah	R	[7:0]	CHIPNAME[0][7:0]	Chip name 2. (Read-only)	
7Eh	00h	R	[7:0]	-	Reserved.	

8.1.2 Register table: Page 1 (OTP function)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 01h for page 1.	-
01h	00h	R/W	[7:6]	-	Reserved.	-
			[5:0]	OTP_GROUP[5:0]	OTP group select.	-
02h	99h	R/W	[7:0]	WOTP[7:0]	OTP program command.	-
			[7:3]	-	Reserved.	-
			[2]	OTP_RELOAD	OTP reload function enable/disable.	-
			[1]	OTP_RD	OTP read function enable/disable.	-
			[0]	OTP_WR	OTP write function enable/disable.	-
03h	00h	R/W	[7:1]	-	Reserved.	-
			[0]	OTP_INDEX[8]	OTP address for read.	-
04h	00h	R/W	[7:0]	OTP_INDEX[7:0]	OTP address for read.	-
05h	00h	R/W	[7:0]	PDOB[7:0]	OTP data for read only.	-
06h	00h	R	[7:0]	OTP_DIN[7:0]	OTP program input data.	-
07h	00h	R/W	[7:0]	OTP_DIN[7:0]	OTP program input data.	-
08h	5Ah	R/W	[7:0]	OTP_MANUAL[7:0]	OTP manual program command.	-
09h	00h	R/W	[7:0]	-	Reserved	-
0Ah	5Ah	R/W	[7:0]	EEP_PWD[7:0]	EEPROM software reload enable.	-
			[7]	EEP_CKSUM_FAIL	EEPROM check sum fail. (Read only)	-
0Bh	00h	R	[6:1]	-	Reserved.	-
			[0]	EEP_RL_CMD	EEPROM software triggered reload.	-
			[7]	R_SIDEN_XOR	Inverse SIDEN hardware pin setting.	-
			[6:5]	-	Reserved.	-
			[4]	EESEL	EEPROM controlled by System or Driver IC.	-
			[3:2]	-	Reserved.	-
			[1:0]	OTP_GAM_SEL[1:0]	Analog gamma table reload select.	-
0Dh	00h	R	[7:0]	TCON_CKSUM[7:0]	EEPROM checksum value calculate by TCON.	-
0Eh	00h	R	[7:0]	EEPROM_CKSUM[7:0]	EEPROM checksum value read from EEPROM.	-
			[7:1]	-	Reserved.	-
0Fh	00h	R	[0]	FDEF[6]	Error flag of OTP programming.	-

8.1.3 Register table: Page 2 (Digital gamma: red, positive)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 02h for page 2.	-
01h	00h	R/W	[7:0]	PGMA1R[7:0]	Positive gamma X1 (data 0) reference : Red	Group 15, 2 times
02h	04h	R/W	[7:0]	PGMA2R[7:0]	Positive gamma X2 (data 1) reference : Red	
03h	08h	R/W	[7:0]	PGMA3R[7:0]	Positive gamma X3 (data 2) reference : Red	
04h	0Ch	R/W	[7:0]	PGMA4R[7:0]	Positive gamma X4 (data 3) reference : Red	
05h	14h	R/W	[7:0]	PGMA5R[7:0]	Positive gamma X5 (data 5) reference : Red	
06h	1Ch	R/W	[7:0]	PGMA6R[7:0]	Positive gamma X6 (data 7) reference : Red	
07h	24h	R/W	[7:0]	PGMA7R[7:0]	Positive gamma X7 (data 9) reference : Red	
08h	2Ch	R/W	[7:0]	PGMA8R[7:0]	Positive gamma X8 (data 11) reference : Red	
09h	34h	R/W	[7:0]	PGMA9R[7:0]	Positive gamma X9 (data 13) reference : Red	
0Ah	3Ch	R/W	[7:0]	PGMA10R[7:0]	Positive gamma X10 (data 15) reference : Red	
0Bh	5Ch	R/W	[7:0]	PGMA11R[7:0]	Positive gamma X11 (data 23) reference : Red	
0Ch	7Ch	R/W	[7:0]	PGMA12R[7:0]	Positive gamma X12 (data 31) reference : Red	
0Dh	BCh	R/W	[7:0]	PGMA13R[7:0]	Positive gamma X13 (data 47) reference : Red	
0Eh	FCh	R/W	[7:0]	PGMA14R[7:0]	Positive gamma X14 (data 63) reference : Red	
0Fh	3Ch	R/W	[7:0]	PGMA15R[7:0]	Positive gamma X15 (data 79) reference : Red	
10h	7Ch	R/W	[7:0]	PGMA16R[7:0]	Positive gamma X16 (data 95) reference : Red	
11h	FCh	R/W	[7:0]	PGMA17R[7:0]	Positive gamma X17 (data 127) reference : Red	
12h	7Ch	R/W	[7:0]	PGMA18R[7:0]	Positive gamma X18 (data 159) reference : Red	
13h	BCh	R/W	[7:0]	PGMA19R[7:0]	Positive gamma X19 (data 175) reference : Red	
14h	FCh	R/W	[7:0]	PGMA20R[7:0]	Positive gamma X20 (data 191) reference : Red	
15h	3Ch	R/W	[7:0]	PGMA21R[7:0]	Positive gamma X21 (data 207) reference : Red	
16h	7Ch	R/W	[7:0]	PGMA22R[7:0]	Positive gamma X22 (data 223) reference : Red	
17h	9Ch	R/W	[7:0]	PGMA23R[7:0]	Positive gamma X23 (data 231) reference : Red	
18h	BCh	R/W	[7:0]	PGMA24R[7:0]	Positive gamma X24 (data 239) reference : Red	
19h	C4h	R/W	[7:0]	PGMA25R[7:0]	Positive gamma X25 (data 241) reference : Red	
1Ah	CCh	R/W	[7:0]	PGMA26R[7:0]	Positive gamma X26 (data 243) reference : Red	
1Bh	D4h	R/W	[7:0]	PGMA27R[7:0]	Positive gamma X27 (data 245) reference : Red	
1Ch	DCh	R/W	[7:0]	PGMA28R[7:0]	Positive gamma X28 (data 247) reference : Red	
1Dh	E4h	R/W	[7:0]	PGMA29R[7:0]	Positive gamma X29 (data 249) reference : Red	
1Eh	ECh	R/W	[7:0]	PGMA30R[7:0]	Positive gamma X30 (data 251) reference : Red	
1Fh	F4h	R/W	[7:0]	PGMA31R[7:0]	Positive gamma X31 (data 253) reference : Red	
20h	F8h	R/W	[7:0]	PGMA32R[7:0]	Positive gamma X32 (data 254) reference : Red	
21h	00h	R/W	[7:6]	PGMA1R[9:8]	Positive gamma X1 (data 0) reference : Red	
			[5:4]	PGMA2R[9:8]	Positive gamma X2 (data 1) reference : Red	
			[3:2]	PGMA3R[9:8]	Positive gamma X3 (data 2) reference : Red	
			[1:0]	PGMA4R[9:8]	Positive gamma X4 (data 3) reference : Red	
22h	00h	R/W	[7:6]	PGMA5R[9:8]	Positive gamma X5 (data 5) reference : Red	
			[5:4]	PGMA6R[9:8]	Positive gamma X6 (data 7) reference : Red	
			[3:2]	PGMA7R[9:8]	Positive gamma X7 (data 9) reference : Red	
			[1:0]	PGMA8R[9:8]	Positive gamma X8 (data 11) reference : Red	
23h	00h	R/W	[7:6]	PGMA9R[9:8]	Positive gamma X9 (data 13) reference : Red	
			[5:4]	PGMA10R[9:8]	Positive gamma X10 (data 15) reference : Red	
			[3:2]	PGMA11R[9:8]	Positive gamma X11 (data 23) reference : Red	
			[1:0]	PGMA12R[9:8]	Positive gamma X12 (data 31) reference : Red	
24h	05h	R/W	[7:6]	PGMA13R[9:8]	Positive gamma X13 (data 47) reference : Red	
			[5:4]	PGMA14R[9:8]	Positive gamma X14 (data 63) reference : Red	
			[3:2]	PGMA15R[9:8]	Positive gamma X15 (data 79) reference : Red	
			[1:0]	PGMA16R[9:8]	Positive gamma X16 (data 95) reference : Red	
25h	6Ah	R/W	[7:6]	PGMA17R[9:8]	Positive gamma X17 (data 127) reference : Red	
			[5:4]	PGMA18R[9:8]	Positive gamma X18 (data 159) reference : Red	
			[3:2]	PGMA19R[9:8]	Positive gamma X19 (data 175) reference : Red	
			[1:0]	PGMA20R[9:8]	Positive gamma X20 (data 191) reference : Red	
26h	FFh	R/W	[7:6]	PGMA21R[9:8]	Positive gamma X21 (data 207) reference : Red	
			[5:4]	PGMA22R[9:8]	Positive gamma X22 (data 223) reference : Red	
			[3:2]	PGMA23R[9:8]	Positive gamma X23 (data 231) reference : Red	
			[1:0]	PGMA24R[9:8]	Positive gamma X24 (data 239) reference : Red	
27h	FFh	R/W	[7:6]	PGMA25R[9:8]	Positive gamma X25 (data 241) reference : Red	
			[5:4]	PGMA26R[9:8]	Positive gamma X26 (data 243) reference : Red	
			[3:2]	PGMA27R[9:8]	Positive gamma X27 (data 245) reference : Red	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	PGMA28R[9:8]	Positive gamma X28 (data 247) reference : Red	
			[7:6]	PGMA29R[9:8]	Positive gamma X29 (data 249) reference : Red	
28h	FFh	R/W	[5:4]	PGMA30R[9:8]	Positive gamma X30 (data 251) reference : Red	
			[3:2]	PGMA31R[9:8]	Positive gamma X31 (data 253) reference : Red	
			[1:0]	PGMA32R[9:8]	Positive gamma X32 (data 254) reference : Red	
29h	FCh	R/W	[7:6]	PGMA33R[7:0]	Positive gamma X33 (data 255) reference : Red	
2Ah	C0h	R/W	[7:6]	PGMA33R[9:8]	Positive gamma X33 (data 255) reference : Red	
			[5:0]	-	Reserved	

8.1.4 Register table: Page 3 (Digital gamma: green, positive)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 03h for page 3.	-
01h	00h	R/W	[7:0]	PGMA1G[7:0]	Positive gamma X1 (data 0) reference : Green	Group 16, 2 times
02h	04h	R/W	[7:0]	PGMA2G[7:0]	Positive gamma X2 (data 1) reference : Green	
03h	08h	R/W	[7:0]	PGMA3G[7:0]	Positive gamma X3 (data 2) reference : Green	
04h	0Ch	R/W	[7:0]	PGMA4G[7:0]	Positive gamma X4 (data 3) reference : Green	
05h	14h	R/W	[7:0]	PGMA5G[7:0]	Positive gamma X5 (data 5) reference : Green	
06h	1Ch	R/W	[7:0]	PGMA6G[7:0]	Positive gamma X6 (data 7) reference : Green	
07h	24h	R/W	[7:0]	PGMA7G[7:0]	Positive gamma X7 (data 9) reference : Green	
08h	2Ch	R/W	[7:0]	PGMA8G[7:0]	Positive gamma X8 (data 11) reference : Green	
09h	34h	R/W	[7:0]	PGMA9G[7:0]	Positive gamma X9 (data 13) reference : Green	
0Ah	3Ch	R/W	[7:0]	PGMA10G[7:0]	Positive gamma X10 (data 15) reference : Green	
0Bh	5Ch	R/W	[7:0]	PGMA11G[7:0]	Positive gamma X11 (data 23) reference : Green	
0Ch	7Ch	R/W	[7:0]	PGMA12G[7:0]	Positive gamma X12 (data 31) reference : Green	
0Dh	BCh	R/W	[7:0]	PGMA13G[7:0]	Positive gamma X13 (data 47) reference : Green	
0Eh	FCh	R/W	[7:0]	PGMA14G[7:0]	Positive gamma X14 (data 63) reference : Green	
0Fh	3Ch	R/W	[7:0]	PGMA15G[7:0]	Positive gamma X15 (data 79) reference : Green	
10h	7Ch	R/W	[7:0]	PGMA16G[7:0]	Positive gamma X16 (data 95) reference : Green	
11h	FCh	R/W	[7:0]	PGMA17G[7:0]	Positive gamma X17 (data 127) reference : Green	
12h	7Ch	R/W	[7:0]	PGMA18G[7:0]	Positive gamma X18 (data 159) reference : Green	
13h	BCh	R/W	[7:0]	PGMA19G[7:0]	Positive gamma X19 (data 175) reference : Green	
14h	FCh	R/W	[7:0]	PGMA20G[7:0]	Positive gamma X20 (data 191) reference : Green	
15h	3Ch	R/W	[7:0]	PGMA21G[7:0]	Positive gamma X21 (data 207) reference : Green	
16h	7Ch	R/W	[7:0]	PGMA22G[7:0]	Positive gamma X22 (data 223) reference : Green	
17h	9Ch	R/W	[7:0]	PGMA23G[7:0]	Positive gamma X23 (data 231) reference : Green	
18h	BCh	R/W	[7:0]	PGMA24G[7:0]	Positive gamma X24 (data 239) reference : Green	
19h	C4h	R/W	[7:0]	PGMA25G[7:0]	Positive gamma X25 (data 241) reference : Green	
1Ah	CCh	R/W	[7:0]	PGMA26G[7:0]	Positive gamma X26 (data 243) reference : Green	
1Bh	D4h	R/W	[7:0]	PGMA27G[7:0]	Positive gamma X27 (data 245) reference : Green	
1Ch	DCh	R/W	[7:0]	PGMA28G[7:0]	Positive gamma X28 (data 247) reference : Green	
1Dh	E4h	R/W	[7:0]	PGMA29G[7:0]	Positive gamma X29 (data 249) reference : Green	
1Eh	ECh	R/W	[7:0]	PGMA30G[7:0]	Positive gamma X30 (data 251) reference : Green	
1Fh	F4h	R/W	[7:0]	PGMA31G[7:0]	Positive gamma X31 (data 253) reference : Green	
20h	F8h	R/W	[7:0]	PGMA32G[7:0]	Positive gamma X32 (data 254) reference : Green	
21h	00h	R/W	[7:6]	PGMA1G[9:8]	Positive gamma X1 (data 0) reference : Green	
			[5:4]	PGMA2G[9:8]	Positive gamma X2 (data 1) reference : Green	
			[3:2]	PGMA3G[9:8]	Positive gamma X3 (data 2) reference : Green	
			[1:0]	PGMA4G[9:8]	Positive gamma X4 (data 3) reference : Green	
22h	00h	R/W	[7:6]	PGMA5G[9:8]	Positive gamma X5 (data 5) reference : Green	
			[5:4]	PGMA6G[9:8]	Positive gamma X6 (data 7) reference : Green	
			[3:2]	PGMA7G[9:8]	Positive gamma X7 (data 9) reference : Green	
			[1:0]	PGMA8G[9:8]	Positive gamma X8 (data 11) reference : Green	
23h	00h	R/W	[7:6]	PGMA9G[9:8]	Positive gamma X9 (data 13) reference : Green	
			[5:4]	PGMA10G[9:8]	Positive gamma X10 (data 15) reference : Green	
			[3:2]	PGMA11G[9:8]	Positive gamma X11 (data 23) reference : Green	
			[1:0]	PGMA12G[9:8]	Positive gamma X12 (data 31) reference : Green	
24h	05h	R/W	[7:6]	PGMA13G[9:8]	Positive gamma X13 (data 47) reference : Green	
			[5:4]	PGMA14G[9:8]	Positive gamma X14 (data 63) reference : Green	
			[3:2]	PGMA15G[9:8]	Positive gamma X15 (data 79) reference : Green	
			[1:0]	PGMA16G[9:8]	Positive gamma X16 (data 95) reference : Green	
25h	6Ah	R/W	[7:6]	PGMA17G[9:8]	Positive gamma X17 (data 127) reference : Green	
			[5:4]	PGMA18G[9:8]	Positive gamma X18 (data 159) reference : Green	
			[3:2]	PGMA19G[9:8]	Positive gamma X19 (data 175) reference : Green	
			[1:0]	PGMA20G[9:8]	Positive gamma X20 (data 191) reference : Green	
26h	FFh	R/W	[7:6]	PGMA21G[9:8]	Positive gamma X21 (data 207) reference : Green	
			[5:4]	PGMA22G[9:8]	Positive gamma X22 (data 223) reference : Green	
			[3:2]	PGMA23G[9:8]	Positive gamma X23 (data 231) reference : Green	
			[1:0]	PGMA24G[9:8]	Positive gamma X24 (data 239) reference : Green	
27h	FFh	R/W	[7:6]	PGMA25G[9:8]	Positive gamma X25 (data 241) reference : Green	
			[5:4]	PGMA26G[9:8]	Positive gamma X26 (data 243) reference : Green	
			[3:2]	PGMA27G[9:8]	Positive gamma X27 (data 245) reference : Green	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	PGMA28G[9:8]	Positive gamma X28 (data 247) reference : Green	
			[7:6]	PGMA29G[9:8]	Positive gamma X29 (data 249) reference : Green	
28h	FFh	R/W	[5:4]	PGMA30G[9:8]	Positive gamma X30 (data 251) reference : Green	
			[3:2]	PGMA31G[9:8]	Positive gamma X31 (data 253) reference : Green	
			[1:0]	PGMA32G[9:8]	Positive gamma X32 (data 254) reference : Green	
29h	FCh	R/W	[7:6]	PGMA33G[7:0]	Positive gamma X33 (data 255) reference : Green	
2Ah	C0h	R/W	[7:6]	PGMA33G[9:8]	Positive gamma X33 (data 255) reference : Green	
			[5:0]	-	Reserved	

8.1.5 Register table: Page 4 (Digital gamma: blue, positive)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 04h for page 4.	-
01h	00h	R/W	[7:0]	PGMA1B[7:0]	Positive gamma X1 (data 0) reference : Blue	Group 17, 2 times
02h	04h	R/W	[7:0]	PGMA2B[7:0]	Positive gamma X2 (data 1) reference : Blue	
03h	08h	R/W	[7:0]	PGMA3B[7:0]	Positive gamma X3 (data 2) reference : Blue	
04h	0Ch	R/W	[7:0]	PGMA4B[7:0]	Positive gamma X4 (data 3) reference : Blue	
05h	14h	R/W	[7:0]	PGMA5B[7:0]	Positive gamma X5 (data 5) reference : Blue	
06h	1Ch	R/W	[7:0]	PGMA6B[7:0]	Positive gamma X6 (data 7) reference : Blue	
07h	24h	R/W	[7:0]	PGMA7B[7:0]	Positive gamma X7 (data 9) reference : Blue	
08h	2Ch	R/W	[7:0]	PGMA8B[7:0]	Positive gamma X8 (data 11) reference : Blue	
09h	34h	R/W	[7:0]	PGMA9B[7:0]	Positive gamma X9 (data 13) reference : Blue	
0Ah	3Ch	R/W	[7:0]	PGMA10B[7:0]	Positive gamma X10 (data 15) reference : Blue	
0Bh	5Ch	R/W	[7:0]	PGMA11B[7:0]	Positive gamma X11 (data 23) reference : Blue	
0Ch	7Ch	R/W	[7:0]	PGMA12B[7:0]	Positive gamma X12 (data 31) reference : Blue	
0Dh	BCh	R/W	[7:0]	PGMA13B[7:0]	Positive gamma X13 (data 47) reference : Blue	
0Eh	FCh	R/W	[7:0]	PGMA14B[7:0]	Positive gamma X14 (data 63) reference : Blue	
0Fh	3Ch	R/W	[7:0]	PGMA15B[7:0]	Positive gamma X15 (data 79) reference : Blue	
10h	7Ch	R/W	[7:0]	PGMA16B[7:0]	Positive gamma X16 (data 95) reference : Blue	
11h	FCh	R/W	[7:0]	PGMA17B[7:0]	Positive gamma X17 (data 127) reference : Blue	
12h	7Ch	R/W	[7:0]	PGMA18B[7:0]	Positive gamma X18 (data 159) reference : Blue	
13h	BCh	R/W	[7:0]	PGMA19B[7:0]	Positive gamma X19 (data 175) reference : Blue	
14h	FCh	R/W	[7:0]	PGMA20B[7:0]	Positive gamma X20 (data 191) reference : Blue	
15h	3Ch	R/W	[7:0]	PGMA21B[7:0]	Positive gamma X21 (data 207) reference : Blue	
16h	7Ch	R/W	[7:0]	PGMA22B[7:0]	Positive gamma X22 (data 223) reference : Blue	
17h	9Ch	R/W	[7:0]	PGMA23B[7:0]	Positive gamma X23 (data 231) reference : Blue	
18h	BCh	R/W	[7:0]	PGMA24B[7:0]	Positive gamma X24 (data 239) reference : Blue	
19h	C4h	R/W	[7:0]	PGMA25B[7:0]	Positive gamma X25 (data 241) reference : Blue	
1Ah	CCh	R/W	[7:0]	PGMA26B[7:0]	Positive gamma X26 (data 243) reference : Blue	
1Bh	D4h	R/W	[7:0]	PGMA27B[7:0]	Positive gamma X27 (data 245) reference : Blue	
1Ch	DCh	R/W	[7:0]	PGMA28B[7:0]	Positive gamma X28 (data 247) reference : Blue	
1Dh	E4h	R/W	[7:0]	PGMA29B[7:0]	Positive gamma X29 (data 249) reference : Blue	
1Eh	ECh	R/W	[7:0]	PGMA30B[7:0]	Positive gamma X30 (data 251) reference : Blue	
1Fh	F4h	R/W	[7:0]	PGMA31B[7:0]	Positive gamma X31 (data 253) reference : Blue	
20h	F8h	R/W	[7:0]	PGMA32B[7:0]	Positive gamma X32 (data 254) reference : Blue	
21h	00h	R/W	[7:6]	PGMA1B[9:8]	Positive gamma X1 (data 0) reference : Blue	
			[5:4]	PGMA2B[9:8]	Positive gamma X2 (data 1) reference : Blue	
			[3:2]	PGMA3B[9:8]	Positive gamma X3 (data 2) reference : Blue	
			[1:0]	PGMA4B[9:8]	Positive gamma X4 (data 3) reference : Blue	
22h	00h	R/W	[7:6]	PGMA5B[9:8]	Positive gamma X5 (data 5) reference : Blue	
			[5:4]	PGMA6B[9:8]	Positive gamma X6 (data 7) reference : Blue	
			[3:2]	PGMA7B[9:8]	Positive gamma X7 (data 9) reference : Blue	
			[1:0]	PGMA8B[9:8]	Positive gamma X8 (data 11) reference : Blue	
23h	00h	R/W	[7:6]	PGMA9B[9:8]	Positive gamma X9 (data 13) reference : Blue	
			[5:4]	PGMA10B[9:8]	Positive gamma X10 (data 15) reference : Blue	
			[3:2]	PGMA11B[9:8]	Positive gamma X11 (data 23) reference : Blue	
			[1:0]	PGMA12B[9:8]	Positive gamma X12 (data 31) reference : Blue	
24h	05h	R/W	[7:6]	PGMA13B[9:8]	Positive gamma X13 (data 47) reference : Blue	
			[5:4]	PGMA14B[9:8]	Positive gamma X14 (data 63) reference : Blue	
			[3:2]	PGMA15B[9:8]	Positive gamma X15 (data 79) reference : Blue	
			[1:0]	PGMA16B[9:8]	Positive gamma X16 (data 95) reference : Blue	
25h	6Ah	R/W	[7:6]	PGMA17B[9:8]	Positive gamma X17 (data 127) reference : Blue	
			[5:4]	PGMA18B[9:8]	Positive gamma X18 (data 159) reference : Blue	
			[3:2]	PGMA19B[9:8]	Positive gamma X19 (data 175) reference : Blue	
			[1:0]	PGMA20B[9:8]	Positive gamma X20 (data 191) reference : Blue	
26h	FFh	R/W	[7:6]	PGMA21B[9:8]	Positive gamma X21 (data 207) reference : Blue	
			[5:4]	PGMA22B[9:8]	Positive gamma X22 (data 223) reference : Blue	
			[3:2]	PGMA23B[9:8]	Positive gamma X23 (data 231) reference : Blue	
			[1:0]	PGMA24B[9:8]	Positive gamma X24 (data 239) reference : Blue	
27h	FFh	R/W	[7:6]	PGMA25B[9:8]	Positive gamma X25 (data 241) reference : Blue	
			[5:4]	PGMA26B[9:8]	Positive gamma X26 (data 243) reference : Blue	
			[3:2]	PGMA27B[9:8]	Positive gamma X27 (data 245) reference : Blue	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	PGMA28B[9:8]	Positive gamma X28 (data 247) reference : Blue	
			[7:6]	PGMA29B[9:8]	Positive gamma X29 (data 249) reference : Blue	
			[5:4]	PGMA30B[9:8]	Positive gamma X30 (data 251) reference : Blue	
			[3:2]	PGMA31B[9:8]	Positive gamma X31 (data 253) reference : Blue	
			[1:0]	PGMA32B[9:8]	Positive gamma X32 (data 254) reference : Blue	
28h	FFh	R/W	[7:6]	PGMA33B[7:0]	Positive gamma X33 (data 255) reference : Blue	
29h	FCh	R/W	[7:6]	PGMA33B[7:0]	Positive gamma X33 (data 255) reference : Blue	
2Ah	C0h	R/W	[7:6]	PGMA33B[9:8]	Positive gamma X33 (data 255) reference : Blue	
			[5:0]	-	Reserved	

8.1.6 Register table: Page 5 (Digital gamma: red, negative)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 05h for page 0.	-
01h	00h	R/W	[7:0]	NGMA1R[7:0]	Negative gamma X1 (data 0) reference : Red	Group 18, 2 times
02h	04h	R/W	[7:0]	NGMA2R[7:0]	Negative gamma X2 (data 1) reference : Red	
03h	08h	R/W	[7:0]	NGMA3R[7:0]	Negative gamma X3 (data 2) reference : Red	
04h	0Ch	R/W	[7:0]	NGMA4R[7:0]	Negative gamma X4 (data 3) reference : Red	
05h	14h	R/W	[7:0]	NGMA5R[7:0]	Negative gamma X5 (data 5) reference : Red	
06h	1Ch	R/W	[7:0]	NGMA6R[7:0]	Negative gamma X6 (data 7) reference : Red	
07h	24h	R/W	[7:0]	NGMA7R[7:0]	Negative gamma X7 (data 9) reference : Red	
08h	2Ch	R/W	[7:0]	NGMA8R[7:0]	Negative gamma X8 (data 11) reference : Red	
09h	34h	R/W	[7:0]	NGMA9R[7:0]	Negative gamma X9 (data 13) reference : Red	
0Ah	3Ch	R/W	[7:0]	NGMA10R[7:0]	Negative gamma X10 (data 15) reference : Red	
0Bh	5Ch	R/W	[7:0]	NGMA11R[7:0]	Negative gamma X11 (data 23) reference : Red	
0Ch	7Ch	R/W	[7:0]	NGMA12R[7:0]	Negative gamma X12 (data 31) reference : Red	
0Dh	BCh	R/W	[7:0]	NGMA13R[7:0]	Negative gamma X13 (data 47) reference : Red	
0Eh	FCh	R/W	[7:0]	NGMA14R[7:0]	Negative gamma X14 (data 63) reference : Red	
0Fh	3Ch	R/W	[7:0]	NGMA15R[7:0]	Negative gamma X15 (data 79) reference : Red	
10h	7Ch	R/W	[7:0]	NGMA16R[7:0]	Negative gamma X16 (data 95) reference : Red	
11h	FCh	R/W	[7:0]	NGMA17R[7:0]	Negative gamma X17 (data 127) reference : Red	
12h	7Ch	R/W	[7:0]	NGMA18R[7:0]	Negative gamma X18 (data 159) reference : Red	
13h	BCh	R/W	[7:0]	NGMA19R[7:0]	Negative gamma X19 (data 175) reference : Red	
14h	FCh	R/W	[7:0]	NGMA20R[7:0]	Negative gamma X20 (data 191) reference : Red	
15h	3Ch	R/W	[7:0]	NGMA21R[7:0]	Negative gamma X21 (data 207) reference : Red	
16h	7Ch	R/W	[7:0]	NGMA22R[7:0]	Negative gamma X22 (data 223) reference : Red	
17h	9Ch	R/W	[7:0]	NGMA23R[7:0]	Negative gamma X23 (data 231) reference : Red	
18h	BCh	R/W	[7:0]	NGMA24R[7:0]	Negative gamma X24 (data 239) reference : Red	
19h	C4h	R/W	[7:0]	NGMA25R[7:0]	Negative gamma X25 (data 241) reference : Red	
1Ah	CCh	R/W	[7:0]	NGMA26R[7:0]	Negative gamma X26 (data 243) reference : Red	
1Bh	D4h	R/W	[7:0]	NGMA27R[7:0]	Negative gamma X27 (data 245) reference : Red	
1Ch	DCh	R/W	[7:0]	NGMA28R[7:0]	Negative gamma X28 (data 247) reference : Red	
1Dh	E4h	R/W	[7:0]	NGMA29R[7:0]	Negative gamma X29 (data 249) reference : Red	
1Eh	ECh	R/W	[7:0]	NGMA30R[7:0]	Negative gamma X30 (data 251) reference : Red	
1Fh	F4h	R/W	[7:0]	NGMA31R[7:0]	Negative gamma X31 (data 253) reference : Red	
20h	F8h	R/W	[7:0]	NGMA32R[7:0]	Negative gamma X32 (data 254) reference : Red	
21h	00h	R/W	[7:6]	NGMA1R[9:8]	Negative gamma X1 (data 0) reference : Red	
			[5:4]	NGMA2R[9:8]	Negative gamma X2 (data 1) reference : Red	
			[3:2]	NGMA3R[9:8]	Negative gamma X3 (data 2) reference : Red	
			[1:0]	NGMA4R[9:8]	Negative gamma X4 (data 3) reference : Red	
22h	00h	R/W	[7:6]	NGMA5R[9:8]	Negative gamma X5 (data 5) reference : Red	
			[5:4]	NGMA6R[9:8]	Negative gamma X6 (data 7) reference : Red	
			[3:2]	NGMA7R[9:8]	Negative gamma X7 (data 9) reference : Red	
			[1:0]	NGMA8R[9:8]	Negative gamma X8 (data 11) reference : Red	
23h	00h	R/W	[7:6]	NGMA9R[9:8]	Negative gamma X9 (data 13) reference : Red	
			[5:4]	NGMA10R[9:8]	Negative gamma X10 (data 15) reference : Red	
			[3:2]	NGMA11R[9:8]	Negative gamma X11 (data 23) reference : Red	
			[1:0]	NGMA12R[9:8]	Negative gamma X12 (data 31) reference : Red	
24h	05h	R/W	[7:6]	NGMA13R[9:8]	Negative gamma X13 (data 47) reference : Red	
			[5:4]	NGMA14R[9:8]	Negative gamma X14 (data 63) reference : Red	
			[3:2]	NGMA15R[9:8]	Negative gamma X15 (data 79) reference : Red	
			[1:0]	NGMA16R[9:8]	Negative gamma X16 (data 95) reference : Red	
25h	6Ah	R/W	[7:6]	NGMA17R[9:8]	Negative gamma X17 (data 127) reference : Red	
			[5:4]	NGMA18R[9:8]	Negative gamma X18 (data 159) reference : Red	
			[3:2]	NGMA19R[9:8]	Negative gamma X19 (data 175) reference : Red	
			[1:0]	NGMA20R[9:8]	Negative gamma X20 (data 191) reference : Red	
26h	FFh	R/W	[7:6]	NGMA21R[9:8]	Negative gamma X21 (data 207) reference : Red	
			[5:4]	NGMA22R[9:8]	Negative gamma X22 (data 223) reference : Red	
			[3:2]	NGMA23R[9:8]	Negative gamma X23 (data 231) reference : Red	
			[1:0]	NGMA24R[9:8]	Negative gamma X24 (data 239) reference : Red	
27h	FFh	R/W	[7:6]	NGMA25R[9:8]	Negative gamma X25 (data 241) reference : Red	
			[5:4]	NGMA26R[9:8]	Negative gamma X26 (data 243) reference : Red	
			[3:2]	NGMA27R[9:8]	Negative gamma X27 (data 245) reference : Red	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	NGMA28R[9:8]	Negative gamma X28 (data 247) reference : Red	
			[7:6]	NGMA29R[9:8]	Negative gamma X29 (data 249) reference : Red	
			[5:4]	NGMA30R[9:8]	Negative gamma X30 (data 251) reference : Red	
			[3:2]	NGMA31R[9:8]	Negative gamma X31 (data 253) reference : Red	
			[1:0]	NGMA32R[9:8]	Negative gamma X32 (data 254) reference : Red	
28h	FFh	R/W				
29h	FCh	R/W	[7:6]	NGMA33R[7:0]	Negative gamma X33 (data 255) reference : Red	
2Ah	C0h	R/W	[7:6]	NGMA33R[9:8]	Negative gamma X33 (data 255) reference : Red	
			[5:0]	-	Reserved	

8.1.7 Register table: Page 6 (Digital gamma: green, negative)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 06h for page 6.	-
01h	00h	R/W	[7:0]	NGMA1G[7:0]	Negative gamma X1 (data 0) reference : Green	Group 19, 2 times
02h	04h	R/W	[7:0]	NGMA2G[7:0]	Negative gamma X2 (data 1) reference : Green	
03h	08h	R/W	[7:0]	NGMA3G[7:0]	Negative gamma X3 (data 2) reference : Green	
04h	0Ch	R/W	[7:0]	NGMA4G[7:0]	Negative gamma X4 (data 3) reference : Green	
05h	14h	R/W	[7:0]	NGMA5G[7:0]	Negative gamma X5 (data 5) reference : Green	
06h	1Ch	R/W	[7:0]	NGMA6G[7:0]	Negative gamma X6 (data 7) reference : Green	
07h	24h	R/W	[7:0]	NGMA7G[7:0]	Negative gamma X7 (data 9) reference : Green	
08h	2Ch	R/W	[7:0]	NGMA8G[7:0]	Negative gamma X8 (data 11) reference : Green	
09h	34h	R/W	[7:0]	NGMA9G[7:0]	Negative gamma X9 (data 13) reference : Green	
0Ah	3Ch	R/W	[7:0]	NGMA10G[7:0]	Negative gamma X10 (data 15) reference : Green	
0Bh	5Ch	R/W	[7:0]	NGMA11G[7:0]	Negative gamma X11 (data 21) reference : Green	
0Ch	7Ch	R/W	[7:0]	NGMA12G[7:0]	Negative gamma X12 (data 31) reference : Green	
0Dh	BCh	R/W	[7:0]	NGMA13G[7:0]	Negative gamma X13 (data 47) reference : Green	
0Eh	FCh	R/W	[7:0]	NGMA14G[7:0]	Negative gamma X14 (data 63) reference : Green	
0Fh	3Ch	R/W	[7:0]	NGMA15G[7:0]	Negative gamma X15 (data 79) reference : Green	
10h	7Ch	R/W	[7:0]	NGMA16G[7:0]	Negative gamma X16 (data 95) reference : Green	
11h	FCh	R/W	[7:0]	NGMA17G[7:0]	Negative gamma X17 (data 127) reference : Green	
12h	7Ch	R/W	[7:0]	NGMA18G[7:0]	Negative gamma X18 (data 159) reference : Green	
13h	BCh	R/W	[7:0]	NGMA19G[7:0]	Negative gamma X19 (data 175) reference : Green	
14h	FCh	R/W	[7:0]	NGMA20G[7:0]	Negative gamma X20 (data 191) reference : Green	
15h	3Ch	R/W	[7:0]	NGMA21G[7:0]	Negative gamma X21 (data 207) reference : Green	
16h	7Ch	R/W	[7:0]	NGMA22G[7:0]	Negative gamma X22 (data 223) reference : Green	
17h	9Ch	R/W	[7:0]	NGMA23G[7:0]	Negative gamma X23 (data 231) reference : Green	
18h	BCh	R/W	[7:0]	NGMA24G[7:0]	Negative gamma X24 (data 239) reference : Green	
19h	C4h	R/W	[7:0]	NGMA25G[7:0]	Negative gamma X25 (data 241) reference : Green	
1Ah	CCh	R/W	[7:0]	NGMA26G[7:0]	Negative gamma X26 (data 243) reference : Green	
1Bh	D4h	R/W	[7:0]	NGMA27G[7:0]	Negative gamma X27 (data 245) reference : Green	
1Ch	DCh	R/W	[7:0]	NGMA28G[7:0]	Negative gamma X28 (data 247) reference : Green	
1Dh	E4h	R/W	[7:0]	NGMA29G[7:0]	Negative gamma X29 (data 249) reference : Green	
1Eh	ECh	R/W	[7:0]	NGMA30G[7:0]	Negative gamma X30 (data 251) reference : Green	
1Fh	F4h	R/W	[7:0]	NGMA31G[7:0]	Negative gamma X31 (data 253) reference : Green	
20h	F8h	R/W	[7:0]	NGMA32G[7:0]	Negative gamma X32 (data 254) reference : Green	
21h	00h	R/W	[7:6]	NGMA1G[9:8]	Negative gamma X1 (data 0) reference : Green	
			[5:4]	NGMA2G[9:8]	Negative gamma X2 (data 1) reference : Green	
			[3:2]	NGMA3G[9:8]	Negative gamma X3 (data 2) reference : Green	
			[1:0]	NGMA4G[9:8]	Negative gamma X4 (data 3) reference : Green	
22h	00h	R/W	[7:6]	NGMA5G[9:8]	Negative gamma X5 (data 5) reference : Green	
			[5:4]	NGMA6G[9:8]	Negative gamma X6 (data 7) reference : Green	
			[3:2]	NGMA7G[9:8]	Negative gamma X7 (data 9) reference : Green	
			[1:0]	NGMA8G[9:8]	Negative gamma X8 (data 11) reference : Green	
23h	00h	R/W	[7:6]	NGMA9G[9:8]	Negative gamma X9 (data 13) reference : Green	
			[5:4]	NGMA10G[9:8]	Negative gamma X10 (data 15) reference : Green	
			[3:2]	NGMA11G[9:8]	Negative gamma X11 (data 23) reference : Green	
			[1:0]	NGMA12G[9:8]	Negative gamma X12 (data 31) reference : Green	
24h	05h	R/W	[7:6]	NGMA13G[9:8]	Negative gamma X13 (data 47) reference : Green	
			[5:4]	NGMA14G[9:8]	Negative gamma X14 (data 63) reference : Green	
			[3:2]	NGMA15G[9:8]	Negative gamma X15 (data 79) reference : Green	
			[1:0]	NGMA16G[9:8]	Negative gamma X16 (data 95) reference : Green	
25h	6Ah	R/W	[7:6]	NGMA17G[9:8]	Negative gamma X17 (data 127) reference : Green	
			[5:4]	NGMA18G[9:8]	Negative gamma X18 (data 159) reference : Green	
			[3:2]	NGMA19G[9:8]	Negative gamma X19 (data 175) reference : Green	
			[1:0]	NGMA20G[9:8]	Negative gamma X20 (data 191) reference : Green	
26h	FFh	R/W	[7:6]	NGMA21G[9:8]	Negative gamma X21 (data 207) reference : Green	
			[5:4]	NGMA22G[9:8]	Negative gamma X22 (data 223) reference : Green	
			[3:2]	NGMA23G[9:8]	Negative gamma X23 (data 231) reference : Green	
			[1:0]	NGMA24G[9:8]	Negative gamma X24 (data 239) reference : Green	
27h	FFh	R/W	[7:6]	NGMA25G[9:8]	Negative gamma X25 (data 241) reference : Green	
			[5:4]	NGMA26G[9:8]	Negative gamma X26 (data 243) reference : Green	
			[3:2]	NGMA27G[9:8]	Negative gamma X27 (data 245) reference : Green	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	NGMA28G[9:8]	Negative gamma X28 (data 247) reference : Green	
			[7:6]	NGMA29G[9:8]	Negative gamma X29 (data 249) reference : Green	
			[5:4]	NGMA30G[9:8]	Negative gamma X30 (data 251) reference : Green	
			[3:2]	NGMA31G[9:8]	Negative gamma X31 (data 253) reference : Green	
			[1:0]	NGMA32G[9:8]	Negative gamma X32 (data 254) reference : Green	
28h	FFh	R/W				
29h	FCh	R/W	[7:6]	NGMA33G[7:0]	Negative gamma X33 (data 255) reference : Green	
2Ah	C0h	R/W	[7:6]	NGMA33G[9:8]	Negative gamma X33 (data 255) reference : Green	
			[5:0]	-	Reserved	

8.1.8 Register table: Page 7 (Digital gamma: blue, negative)

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
00h	1Fh	R/W	[7:0]	PAGE[7:0]	Register page selection. 07h for page 7.	-
01h	00h	R/W	[7:0]	NGMA1B[7:0]	Negative gamma X1 (data 0) reference : Blue	Group 20, 2 times
02h	04h	R/W	[7:0]	NGMA2B[7:0]	Negative gamma X2 (data 1) reference : Blue	
03h	08h	R/W	[7:0]	NGMA3B[7:0]	Negative gamma X3 (data 2) reference : Blue	
04h	0Ch	R/W	[7:0]	NGMA4B[7:0]	Negative gamma X4 (data 3) reference : Blue	
05h	14h	R/W	[7:0]	NGMA5B[7:0]	Negative gamma X5 (data 5) reference : Blue	
06h	1Ch	R/W	[7:0]	NGMA6B[7:0]	Negative gamma X6 (data 7) reference : Blue	
07h	24h	R/W	[7:0]	NGMA7B[7:0]	Negative gamma X7 (data 9) reference : Blue	
08h	2Ch	R/W	[7:0]	NGMA8B[7:0]	Negative gamma X8 (data 11) reference : Blue	
09h	34h	R/W	[7:0]	NGMA9B[7:0]	Negative gamma X9 (data 13) reference : Blue	
0Ah	3Ch	R/W	[7:0]	NGMA10B[7:0]	Negative gamma X10 (data 15) reference : Blue	
0Bh	5Ch	R/W	[7:0]	NGMA11B[7:0]	Negative gamma X11 (data 23) reference : Blue	
0Ch	7Ch	R/W	[7:0]	NGMA12B[7:0]	Negative gamma X12 (data 31) reference : Blue	
0Dh	BCh	R/W	[7:0]	NGMA13B[7:0]	Negative gamma X13 (data 47) reference : Blue	
0Eh	FCh	R/W	[7:0]	NGMA14B[7:0]	Negative gamma X14 (data 63) reference : Blue	
0Fh	3Ch	R/W	[7:0]	NGMA15B[7:0]	Negative gamma X15 (data 79) reference : Blue	
10h	7Ch	R/W	[7:0]	NGMA16B[7:0]	Negative gamma X16 (data 95) reference : Blue	
11h	FCh	R/W	[7:0]	NGMA17B[7:0]	Negative gamma X17 (data 127) reference : Blue	
12h	7Ch	R/W	[7:0]	NGMA18B[7:0]	Negative gamma X18 (data 159) reference : Blue	
13h	BCh	R/W	[7:0]	NGMA19B[7:0]	Negative gamma X19 (data 175) reference : Blue	
14h	FCh	R/W	[7:0]	NGMA20B[7:0]	Negative gamma X20 (data 191) reference : Blue	
15h	3Ch	R/W	[7:0]	NGMA21B[7:0]	Negative gamma X21 (data 207) reference : Blue	
16h	7Ch	R/W	[7:0]	NGMA22B[7:0]	Negative gamma X22 (data 223) reference : Blue	
17h	9Ch	R/W	[7:0]	NGMA23B[7:0]	Negative gamma X23 (data 231) reference : Blue	
18h	BCh	R/W	[7:0]	NGMA24B[7:0]	Negative gamma X24 (data 239) reference : Blue	
19h	C4h	R/W	[7:0]	NGMA25B[7:0]	Negative gamma X25 (data 241) reference : Blue	
1Ah	CCh	R/W	[7:0]	NGMA26B[7:0]	Negative gamma X26 (data 243) reference : Blue	
1Bh	D4h	R/W	[7:0]	NGMA27B[7:0]	Negative gamma X27 (data 245) reference : Blue	
1Ch	DCh	R/W	[7:0]	NGMA28B[7:0]	Negative gamma X28 (data 247) reference : Blue	
1Dh	E4h	R/W	[7:0]	NGMA29B[7:0]	Negative gamma X29 (data 249) reference : Blue	
1Eh	ECh	R/W	[7:0]	NGMA30B[7:0]	Negative gamma X30 (data 251) reference : Blue	
1Fh	F4h	R/W	[7:0]	NGMA31B[7:0]	Negative gamma X31 (data 253) reference : Blue	
20h	F8h	R/W	[7:0]	NGMA32B[7:0]	Negative gamma X32 (data 254) reference : Blue	
21h	00h	R/W	[7:6]	NGMA1B[9:8]	Negative gamma X1 (data 0) reference : Blue	
			[5:4]	NGMA2B[9:8]	Negative gamma X2 (data 1) reference : Blue	
			[3:2]	NGMA3B[9:8]	Negative gamma X3 (data 2) reference : Blue	
			[1:0]	NGMA4B[9:8]	Negative gamma X4 (data 3) reference : Blue	
22h	00h	R/W	[7:6]	NGMA5B[9:8]	Negative gamma X5 (data 5) reference : Blue	
			[5:4]	NGMA6B[9:8]	Negative gamma X6 (data 7) reference : Blue	
			[3:2]	NGMA7B[9:8]	Negative gamma X7 (data 9) reference : Blue	
			[1:0]	NGMA8B[9:8]	Negative gamma X8 (data 11) reference : Blue	
23h	00h	R/W	[7:6]	NGMA9B[9:8]	Negative gamma X9 (data 13) reference : Blue	
			[5:4]	NGMA10B[9:8]	Negative gamma X10 (data 15) reference : Blue	
			[3:2]	NGMA11B[9:8]	Negative gamma X11 (data 23) reference : Blue	
			[1:0]	NGMA12B[9:8]	Negative gamma X12 (data 31) reference : Blue	
24h	05h	R/W	[7:6]	NGMA13B[9:8]	Negative gamma X13 (data 47) reference : Blue	
			[5:4]	NGMA14B[9:8]	Negative gamma X14 (data 63) reference : Blue	
			[3:2]	NGMA15B[9:8]	Negative gamma X15 (data 79) reference : Blue	
			[1:0]	NGMA16B[9:8]	Negative gamma X16 (data 95) reference : Blue	
25h	6Ah	R/W	[7:6]	NGMA17B[9:8]	Negative gamma X17 (data 127) reference : Blue	
			[5:4]	NGMA18B[9:8]	Negative gamma X18 (data 159) reference : Blue	
			[3:2]	NGMA19B[9:8]	Negative gamma X19 (data 175) reference : Blue	
			[1:0]	NGMA20B[9:8]	Negative gamma X20 (data 191) reference : Blue	
26h	FFh	R/W	[7:6]	NGMA21B[9:8]	Negative gamma X21 (data 207) reference : Blue	
			[5:4]	NGMA22B[9:8]	Negative gamma X22 (data 223) reference : Blue	
			[3:2]	NGMA23B[9:8]	Negative gamma X23 (data 231) reference : Blue	
			[1:0]	NGMA24B[9:8]	Negative gamma X24 (data 239) reference : Blue	
27h	FFh	R/W	[7:6]	NGMA25B[9:8]	Negative gamma X25 (data 241) reference : Blue	
			[5:4]	NGMA26B[9:8]	Negative gamma X26 (data 243) reference : Blue	
			[3:2]	NGMA27B[9:8]	Negative gamma X27 (data 245) reference : Blue	

Address	Default	Read/Write	D[7:0]	Name	Description	Remark
			[1:0]	NGMA28B[9:8]	Negative gamma X28 (data 247) reference : Blue	
			[7:6]	NGMA29B[9:8]	Negative gamma X29 (data 249) reference : Blue	
			[5:4]	NGMA30B[9:8]	Negative gamma X30 (data 251) reference : Blue	
			[3:2]	NGMA31B[9:8]	Negative gamma X31 (data 253) reference : Blue	
			[1:0]	NGMA32B[9:8]	Negative gamma X32 (data 254) reference : Blue	
28h	FFh	R/W	[7:6]	NGMA33B[7:0]	Negative gamma X33 (data 255) reference : Blue	
29h	FCh	R/W	[7:6]	NGMA33B[9:8]	Negative gamma X33 (data 255) reference : Blue	
2Ah	C0h	R/W	[5:0]	-	Reserved	

8.2 Register Description

8.2.1 Page selection

R00h: Register page selection.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
all	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	1	1	1

PAGE[7:0]: Register page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]									Function	Note
0	0	0	0	0	0	0	0	0	Page 0	-
0	0	0	0	0	0	0	0	1	Page 1	-
:	:	:	:	:	:	:	:	:	:	-
0	0	0	0	0	1	1	1	1	Page 7	-
0	0	0	0	1	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	1	1	1	1	Reserved	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	0	Reserved	-
1	1	1	1	1	1	1	1	1	Reserved	-

8.2.2 Page 0 for normal function setting

R00h: Register page selection. Set to 00h for page 0.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
all	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	1	1	1

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	01h	1/0	STBYB_CMD							
			0	0	0	0	0	0	0	0

STBYB_CMD[7:0]: Standby control.

PAGE[7:0]									Function	Note
0	0	0	0	0	0	0	0	0	Normal mode	Default
0	0	0	0	0	0	0	0	1	Normal mode	-
0	0	0	0	0	0	0	1	0	Normal mode	-
:	:	:	:	:	:	:	:	:	Normal mode	-
0	1	0	1	0	1	0	0	0	Normal mode	-
0	1	0	1	0	1	0	1	1	Standby mode	-
0	1	0	1	0	1	1	0	0	Normal mode	-
:	:	:	:	:	:	:	:	:	Normal mode	-
1	1	1	1	1	1	1	1	1	Normal mode	-

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	02h	1/0	-	TR	DINT[1:0]		-	-	MODE	NB
			0	0	0	1	0	0	0	1

TR: Interface format selection.

TR	Function	Note
0	TTL	Default
1	LVDS	-

DINT[1:0]: Input format selection for TTL / LVDS interface

DINT[1:0]	Function	Note
00	TTL, Parallel 18-bit (RGB 666) / LVDS, 3-lane (6-bit)	-
01	TTL, Parallel 24-bit (RGB 888) / LVDS, 4-lane (8-bit)	Default
10	TTL, Parallel 16-bit / LVDS, 2-lane (8-bit)	-
11	TTL, Serial 8-bit / LVDS, 2-lane (8-bit)	-

MODE: Input timing selection for TTL / LVDS interface.

MODE	Function	Note
0	DE only mode	Default
1	Sync mode	-

NB: Panel type selection.

NB	Function	Note
0	Normally white	-
1	Normally black	Default

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	03h	1/0	RL	TB	INV[1:0]		INTL	-	RS[1:0]	
			0	0	1	1	0	0	0	0

RL: Horizontal shift direction. (Effective when FCS=0.)

FCS	Hardware pin RL	Register value R03h[7]	Function
1	1	X	Forward (S1 to S480)
	0		Reverse (S480 to S1)
0	1	1	Reverse (S480 to S1)
		0	Forward (S1 to S480)
	0	1	Forward (S1 to S480)
		0	Reverse (S480 to S1)

TB: Vertical shift direction. (Effective when FCS=0.)

FCS	Hardware pin TB	Register value R03h[6]	Function
1	1	X	Forward (G1 to G840)
	0		Reverse (G840 to G1)
0	1	1	Reverse (G840 to G1)
		0	Forward (G1 to G840)
	0	1	Forward (G1 to G840)
		0	Reverse (G840 to G1)

INV[1:0]: Inversion type selection.

INV[1:0]		Function	Note
0	0	Column inversion	-
0	1	3 dot (line) inversion	-
1	0	6 dot (2 line) inversion	-
1	1	Dot inversion	Default

Column inversion

[illegible]

odd frame

even frame

3 dot (line) inversion

+	-	+	-
+	-	+	-
+	-	+	-
-	+	-	+
-	+	-	+
-	+	-	+
+	-	+	-
+	-	+	-
+	-	+	-
-	+	-	+
-	+	-	+
-	+	-	+

odd frame

even frame

6 dot (2 line) inversion

+	-	+	-
+	-	+	-
+	-	+	-
-	+	-	+
-	+	-	+
-	+	-	+
+	-	+	-
+	-	+	-
+	-	+	-
-	+	-	+
-	+	-	+
-	+	-	+

-	+	-	+
-	+	-	+
-	+	-	+
+	-	+	-
+	-	+	-
+	-	+	-
-	+	-	+
-	+	-	+
-	+	-	+
+	-	+	-
+	-	+	-
+	-	+	-

odd frame

even frame

Dot inversion

[illegible]

odd frame

even frame

Figure 8.1: Four inversion types

RS[1:0]: Typical resolution selection.

RS[1:0]		Function	Note
0	0	480RGBx272	Default
0	1	400RGBx240	-
1	0	360RGBx240	-
1	1	320RGBx240	-

R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	04h	1/0	RBEXC	HSP	VSP	CLOCKP	-	-	PON	POFF
			0	0	0	0	0	0	0	0

RBEXC: Exchange R data and B data.

RBEXC	Function	Note
0	Do not exchange	Default
1	Exchange R data and B data	-

HSP: HS polarity for TTL / LVDS interface.

HSP	Function	Note
0	Low pulse	Default
1	High pulse	-

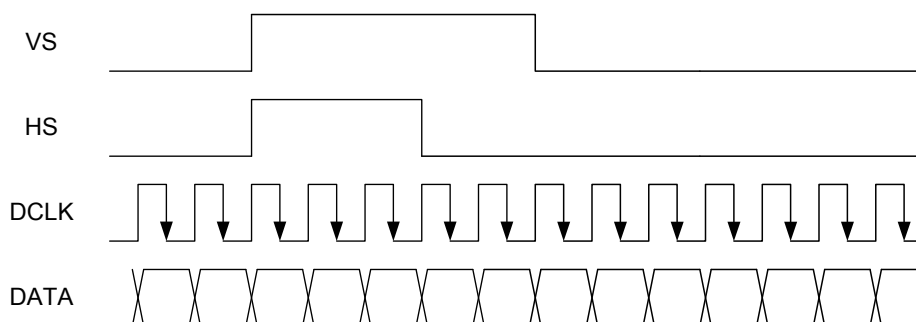
VSP: VS polarity for TTL / LVDS interface.

VSP	Function	Note
0	Low pulse	Default
1	High pulse	-

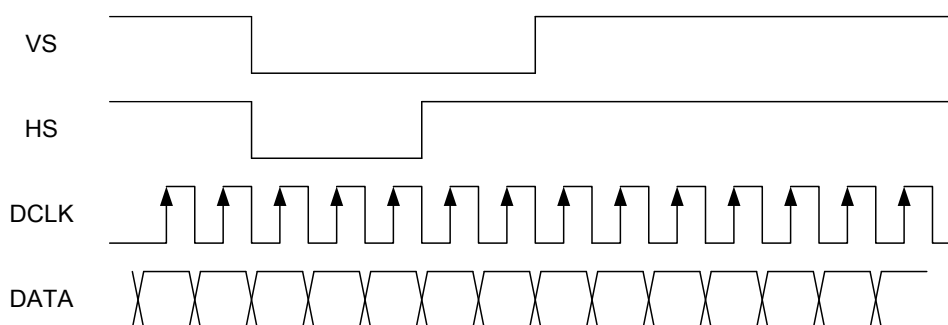
CLOCKP: Clock polarity for TTL interface.

CLOCKP	Function	Note
0	Rising edge	Default
1	Falling edge	-

Example1: CLOCKP=1, VSP=1, HSP=1



Example2: CLOCKP=0, VSP=0, HSP=0 (default setting)



PON: Power on pattern selection.

PON	Function	Note
0	Black pattern	Default
1	White pattern	-

POFF: Power off pattern selection.

NB	POFF	Function	Note
1	0	Black pattern	Default
1	1	White pattern	-
0	0	White pattern	-
0	1	Black pattern	-

R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	05h	1/0	GASEN	SPFEN	SPFSEL	BISTEN	-	-	-	
			1	1	0	0	1	1	1	1

GASEN: GAS function enable.

GASEN	Function	Note
0	Disable	-
1	Enable	Default

SPFEN: Self protection mode enable.

SPFEN	Function	Note
0	Disable	-
1	Enable	Default

SPFSEL: Self protection mode pattern selection.

SPFSEL	Function	Note
0	Black	Default
1	White	-

BISTEN: BIST mode enable. It is effective when FCS=0.

BISTEN	Function	Note
0	Normal mode	Default
1	BIST mode	-

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	06h	1/0	VBP[7:0]							
			0	0	0	0	0	1	0	1

VBP[7:0]: Vertical back porch adjustment. Minimum value is 2H.

VBP[7:0]								Function	Note
0	0	0	0	0	0	0	0	2 H	-
0	0	0	0	0	0	0	1	2 H	-
0	0	0	0	0	0	1	0	2 H	-
0	0	0	0	0	0	1	1	3 H	-
:	:	:	:	:	:	:	:	:	-
0	0	0	0	0	1	0	1	5 H	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255 H	-

R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	07h	1/0	HBP[7:0]							
			0	0	0	1	0	0	0	0

HBP[7:0]: Horizontal back porch adjustment. Minimum value is 5 DCLK.

HBP[7:0]								Function	Note
0	0	0	0	0	0	0	0	5 DCLK	-
:	:	:	:	:	:	:	:	5 DCLK	-
0	0	0	0	0	1	0	1	5 DCLK	-
0	0	0	0	0	1	1	0	6 DCLK	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	0	16 DCLK	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255 DCLK	-

R08h: Timing for source driver control.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	08h	1/0	-	-	-	THZBS	SD_VBLAST[1:0]		SD_VB[1:0]	
			0	0	0	0	0	0	0	0

THZBS: Output timing Thzb (HZ time before bank 0) control.

THZBS	Thzb	Note
0	7 PCLK	Default
1	0 PCLK	-

SD_VBLAST[1:0]: Set source output in the last line of V-blanking. (VBL in the figure.)

SD_VBLAST[1:0]	Function	Note
0 0	Same to other lines in V-blanking	Default
0 1	Black pattern	-
1 0	Same to other lines in V-blanking	
1 1	White pattern	

SD_VB[1:0]: Set source output in the V-blanking except last line. (VB in the figure.)

SD_VB[1:0]	Function	Note
0 0	Keep steady, output the last bank of the last line	Default
0 0	Keep 0V	-
0 1	High-Z	-
1 1	Keep toggling, output the three banks of the last line	-

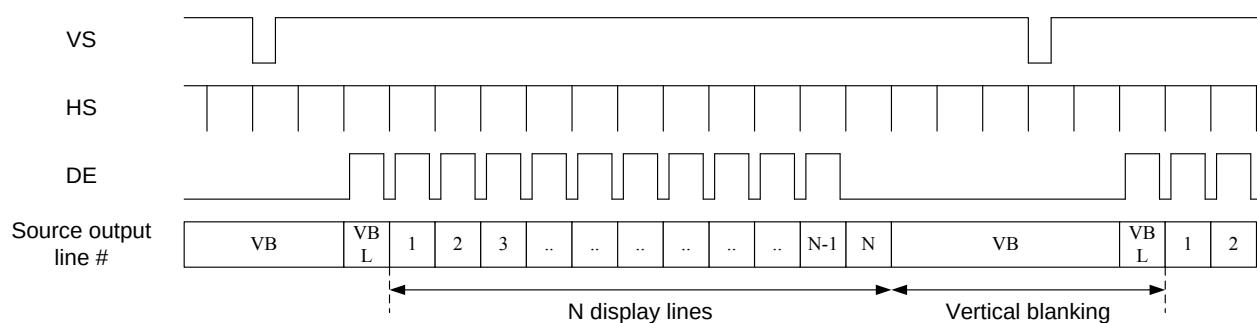


Figure 8.2: Source output in vertical blanking

R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	09h	1/0	PCR[1:0]		ENDRV	EQ0W[4:0]				
			1	0	0	0	1	0	0	0

PCR[1:0]: Source buffer driving timing control. Source channels are separated to two groups, with Tsw = Tsw0 and Tsw1.

PCR[1:0]		Function	Note
0	0	Tsw0 = 2 PCLK , Tsw1 = 2 PCLK	-
0	1	Tsw0 = 2 PCLK , Tsw1 = 4 PCLK	-
1	0	Tsw0 = 2 PCLK , Tsw1 = 6 PCLK	Default
1	1	Tsw0 = 2 PCLK , Tsw1 = 10 PCLK	-

Note: PCLK is pixel clock frequency, which equals to clock frequency (DCLK) in parallel RGB and LVDS modes, and is 1/3 of clock frequency in serial RGB mode.

ENDRV: Source buffer driving ability selection.

ENDRV	Function	Note
0	100%	Default
1	200%	-

EQ0W[4:0]: Source output timing Teq0 (time for source output pre-charging to ground) control. Teq0=EQ0W[4:0] *2 PCLK, minimum 4 PCLK. It is suggested to set Teq0 to 10%~20% of one line.

EQ1W[4:0]					Function	Note
0	0	0	0	0	4 PCLK	-
0	0	0	0	1	4 PCLK	-
0	0	0	1	0	4 PCLK	Default
0	0	0	1	1	6 PCLK	
:	:	:	:	:	:	-
0	1	0	0	0	16 PCLK	
:	:	:	:	:	:	
1	1	1	1	1	62 PCLK	-

R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Ah	1/0	BC[2:0]			EQ1W[4:0]				
			0	1	1	0	0	0	0	0

BC[2:0]: Source buffer bias current selection.

BC[2:0]			Function	Note
0	0	0		-
0	0	1		-
0	1	0		-
0	1	1		Default
1	0	0		-
1	0	1		-
1	1	0		-
1	1	1		-

EQ1W[4:0]: Source output timing Teq1 (source output pre-charging to VDD/VCL) control.
 $Teq1 = EQ1W[4:0] * 2 \text{ PCLK}$.

EQ1W[4:0]					Function	Note
0	0	0	0	0	0 PCLK	Default
0	0	0	0	1	2 PCLK	-
0	0	0	1	0	4 PCLK	-
:	:	:	:	:	:	-
1	1	1	1	1	62 PCLK	-

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Bh	1/0	MFPCS[3:0]				POCSD[1:0]		POCGM[1:0]	
			0	0	0	0	0	0	0	0

MFPCS[3:0]: Period of multiple frame polarity control, maximum 4096 frames.

MFPCS[3:0]				Function	Note
0	0	0	0	Normal	Default
0	0	0	1	2 frames	-
0	0	1	0	4 frames	-
1	0	1	1	2048 frames	
1	1	0	0	4096 frames	
:	:	:	:		
1	1	1	1	4096 frames	-

POCSD[1:0]: Source output offset cancelling selection.

POCSD[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

POCGM[1:0]: Gamma offset cancelling selection.

POCGM[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

T_SDPOP					T_POCGM				
POCSD[1:0]	00	01	10	11	POCGM[1:0]	00	01	10	11
Frame 1					Frame 1				
Line 1	1	1	1	0	line 1	1	1	=SDPOP	0
Line 2	0	1	0		line 2	1	1		
Line 3	0	0	1		line 3	1	1		
Line 4	1	0	0		line 4	1	1		
Line 5	1	1	1		line 5	1	1		
Line 6	0	1	0		line 6	1	1		
Line 7	0	0	1		line 7	1	1		
Line 8	1	0	0		line 8	1	1		
Frame 2					Frame 2				
Line 1	0	0	0	0	line 1	0	1	=SDPOP	0
Line 2	1	0	1		line 2	0	1		
Line 3	1	1	0		line 3	0	1		
Line 4	0	1	1		line 4	0	1		
Line 5	0	0	0		line 5	0	1		
Line 6	1	0	1		line 6	0	1		
Line 7	1	1	0		line 7	0	1		
Line 8	0	1	1		line 8	0	1		
Frame 3					Frame 3				
Line 1	0	0	0	0	line 1	1	0	=SDPOP	0
Line 2	1	0	1		line 2	1	0		
Line 3	1	1	0		line 3	1	0		
Line 4	0	1	1		line 4	1	0		
Line 5	0	0	0		line 5	1	0		
Line 6	1	0	1		line 6	1	0		
Line 7	1	1	0		line 7	1	0		
Line 8	0	1	1		line 8	1	0		
Frame 4					Frame 4				
Line 1	1	1	1	0	line 1	0	0	=SDPOP	0
Line 2	0	1	0		line 2	0	0		
Line 3	0	0	1		line 3	0	0		
Line 4	1	0	0		line 4	0	0		
Line 5	1	1	1		line 5	0	0		
Line 6	0	1	0		line 6	0	0		
Line 7	0	0	1		line 7	0	0		
Line 8	1	0	0		line 8	0	0		

R0Ch, R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Ch	1/0	-	-	BANK0OFS[5:0]					
			0	0	0	0	0	0	0	0
0	0Dh	1/0	-	-	BANK1OFS[5:0]					
			0	0	0	0	0	0	0	0

BANK[1:0]OFS[5:0]: Bank timing control. BANK0OFS[5:0] sets the timing offset of the end of bank 0, and BANK1OFS[5:0] sets the timing offset of the end of bank 1. Offset Tbank0ofs and Tbank1ofs can be set between -31PCLK to +31PCLK.

$$T_{bank0} = (H_{total} - 3 \cdot T_{hzb}) \cdot 1/3 + T_{bank0ofs}$$

$$T_{bank1} = (H_{total} - 3 \cdot T_{hzb}) \cdot 2/3 - T_{bank0} + T_{bank1ofs}$$

$$T_{bank2} = (H_{total} - 3 \cdot T_{hzb}) - T_{bank0} - T_{bank1}$$

BANK0OFS[5:0]	Tbank0ofs	Note
00h	0 PCLK	Default
01h	-31 PCLK	-
02h	-30 PCLK	-
:	..	
20h	0 PCLK	
:	..	
3Fh	+31 PCLK	-

BANK1OFS[5:0]	Tbank1ofs	Note
00h	0 PCLK	Default
01h	-31 PCLK	-
02h	-30 PCLK	-
:	..	
20h	0 PCLK	
:	..	
3Fh	+31 PCLK	-

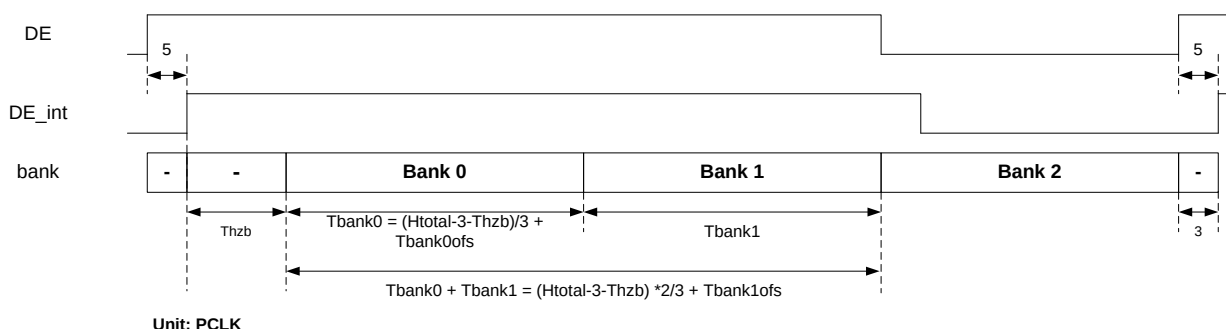


Figure 8.3: Bank timing control

R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Eh	1/0	-	TOEB[6:0]						
			0	0	0	0	1	0	0	0

TOEB[6:0]: Gate output turn on timing control. TOEB = TOEB[6:0]*1 PCLK, minimum 2 PCLK.

TOEB[6:0]							Function	Note
0	0	0	0	0	0	0	2 PCLK	-
0	0	0	0	0	0	1	2 PCLK	-
0	0	0	0	0	1	0	2 PCLK	-
:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	8 PCLK	Default
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	127 PCLK	-

Note: TOEB + TOEF < Htotal/6.

R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	0Fh	1/0	-	TOEF[6:0]						
			0	0	0	0	1	0	0	0

TOEF[6:0]: Gate output turn off timing control. TOEF = TOEF[6:0]*1 PCLK, minimum 2 PCLK.

TOEF[6:0]							Function	Note
0	0	0	0	0	0	0	2 PCLK	-
0	0	0	0	0	0	1	2 PCLK	-
0	0	0	0	0	1	0	2 PCLK	-
:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	8 PCLK	Default
:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	127 PCLK	-

Note: TOEB + TOEF < Htotal/6.

R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	10h	1/0	-	GDSEQ[2:0]						
			0	0	0	0	0	0	0	0

GDSEQ[2:0]: Gate scan type selection.

GDSEQ[2:0]			Function	Note
0	0	0	Type 0	Default
0	0	1	Type 1	-
0	1	0	Type 2	-
0	1	1	Type 3	-
1	0	0	Type 4	-
1	0	1	Type 5	-
1	1	0	Type 0	-
1	1	1	Type 0	-

R14h, R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	14h	1/0	-	-	-	-	GATEPASS[3:0]			
			0	0	0	0	1	0	1	0
0	15h	1/0	GATENUM[7:0]							
			1	0	0	0	1	1	0	0

GATEPASS[3:0]: Password to enable adjustable vertical resolution selection.

GATEPASS[3:0]				Function	Note
0	0	0	0	Disable	-
:	:	:	:	Disable	-
0	1	0	1	Enable	-
:	:	:	:	Disable	-
1	0	1	0	Disable	Default
:	:	:	:	Disable	-
1	1	1	1	Disable	-

GATENUM[7:0]: Adjustable vertical resolution selection. It is effective only if GATEPASS[3:0] is set to 0101b. When enabled, vertical resolution Vactive is set to GATENUM[7:0]*2. Valid range of GATENUM[7:0] is 60~140 (Vactive = 120~280).

GATENUM[7:0]								Vactive	Note
0	0	0	0	0	0	0	0	Reserved	-
0	0	0	0	0	0	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	0	1	1	1	Reserved	-
0	1	1	1	1	0	0	0	120	-
0	1	1	1	1	0	0	1		
:	:	:	:	:	:	:	:	:	-
1	0	0	0	1	0	1	1	278	-
1	0	0	0	1	1	0	0	280	Default
1	0	0	0	1	1	0	1	Reserved	-
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1	Reserved	-

R16h, R17h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	16h	1/0	-				HSETPASS[2:0]			
			0	0	0	0	1	0	1	0
0	17h	1/0	-	HSETNUM[6:0]						
			0	1	1	1	1	0	0	0

HSETPASS[3:0]: Password to enable adjustable horizontal resolution selection.

HSETPASS[3:0]				Function	Note
0	0	0	0	Disable	-
:	:	:	:	Disable	-
0	1	0	1	Enable	-
:	:	:	:	Disable	-
1	0	1	0	Disable	Default
:	:	:	:	Disable	-
1	1	1	1	Disable	-

HSETNUM[6:0]: Adjustable horizontal resolution selection. It is effective only if HSETPASS[3:0] is set to 0101b. When enabled, Hactive = HSETNUM[6:0]*4. Valid range of HSETNUM[6:0] is 30 to 120 (Hactive = 120~480, multiple of 4)

HSETNUM[6:0]							Hactive	Note
0	0	0	0	0	0	0	Reserved	(min.)
0	0	0	0	0	0	1	Reserved	-
:	:	:	:	:	:	:		-
0	0	1	1	1	1	0	120:	-
:	:	:	:	:	:	:		
1	1	1	0	1	1	1	476	-
1	1	1	1	0	0	0	480	Default
1	1	1	1	0	0	1	Reserved	-
:	:	:	:	:	:	:		
1	1	1	1	1	1	1	Reserved	-

R18h, R19h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	18h	1/0	BISTHBS[7:0]							
			0	0	0	0	0	0	0	0
0	19h	1/0	BISTVBS[3:0]				-	-	H_OSCLK_SEL[1:0]	
			0	0	0	0	0	0	0	0

BISTHBS[7:0]: Horizontal blanking selection in BIST and self protection mode. H-blanking for the four typical resolutions and adjustable resolution (when setting GATEPASS[3:0] or HSETPASS[3:0]) in the unit of PCLK is shown below. Note that PCLK in BIST and self protection mode is the internal clock frequency selected by BISTCLKS[1:0].

BISTHBS[7:0]	H-blanking					Note
	480RGB x272	400RGB x240	260RGB x240	320RGB x240	adjustable	
00h	120	160	144	128	Hactive*0.25 + 40	-
01h	121	161	145	129	Hactive*0.25 + 41	-
02h	122	162	146	130	Hactive*0.25 + 42	-
:	:	:	:	:	:	-
FFh	375	415	399	383	Hactive*0.25 + 295	-

BISTVBS[3:0]: Vertical blanking selection in BIST and self protection mode. V-blanking for the four typical resolutions and adjustable resolution (when setting GATEPASS[3:0] or HSETPASS[3:0]) in the unit of lines is shown below.

BISTVBS[3:0]	V-blanking					Note
	480RGB x272	400RGB x240	260RGB x240	320RGB x240	adjustable	
0h	40	72	120	160	10	-
1h	56	88	136	176	26	-
2h	72	104	152	192	42	-
:	:	:	:	:	:	-
Fh	280	312	360	400	250	-

BISTCLKS[1:0]: Internal clock frequency selection in BIST and self protection mode. It is effective when adjustable resolution is enabled (by setting GATEPASS[3:0] or HSETPASS[3:0]).

H_OSCLK_SEL[1:0]		Function	Note
0	0	11 MHz	Default
0	1	5.5 MHz	-
1	0	2.75 MHz	-
1	1	1.375 MHz	-

R1Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Ah	1/0	FFLAGPOL	TPSYNC_FAIL_ENB	FFLAGEN	TPSVBEN	TPSYNCPOL	TPSYNCS[2:0]		
			0	1	0	0	0	0	1	1

FFLAGPOL: FFLAG polarity selection.

FFLAGPOL	Function	Note
0	FFLAG is normally 0	Default
1	FFLAG is normally 1	-

TPSYNC_FAIL_ENB: Set TPSYNC state in GAS or SP mode.

TPSYNC_FAIL_ENB	Function	Note
0	0V	-
1	Keeps normal	Default

FFLAGEN: TESTO0 output enable.

FFLAGEN	Function	Note
0	Disable, TESTO0 = 0	Default
1	Enable, TESTO0 = FFLAG	-

TPSVBEN: TPS signal state in vertical blanking selection.

TPSVBEN	Function	Note
0	Stopped	Default
1	Keeps toggling	-

TPSYNCPOL: TPSYNC output polarity selection.

TPSYNCPOL	Function	Note
0	Normal	Default
1	Inverted	-

TPSYNCS[2:0]: TPSYNC output selection.

TPSYNCS[2:0]			Function	Note
0	0	0	Shifted HS	-
0	0	1	VDEN	-
0	1	0	Shifted VS	-
0	1	1	TPS	Default
1	0	0	FFLAG	-
1	0	1	Reserved	-
1	1	0	GAS (0: normal, 1: GAS mode)	-
1	1	1	Shifted HS	-

R1Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Bh	1/0	TPS_OFS[7:0]							
			0	0	1	0	0	0	0	0

TPS_OFS[7:0]: TPS signal offset (Ttpd) setting.

TPS_OFS[7:0]								Function	Note
0	0	0	0	0	0	0	0	2 PCLK	-
0	0	0	0	0	0	0	1	3 PCLK	-
:	:	:	:	:	:	:	:		
0	0	1	0	0	0	0	0	34 PCLK	Default
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1	257 PCLK	-

R1Ch, R1Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Ch	1/0	-	-	-	-	PTSEL[3:0]			
			0	0	0	0	1	1	1	1
0	1Dh	1/0	BIST_GRAY[7:0]							
			1	0	0	0	0	0	0	0

PTSEL[3:0]: BIST pattern selection.

RS[3:0]				Function	Note
0	0	0	0	Black	-
0	0	0	1	White	-
0	0	1	0	Red	-
0	0	1	1	Green	-
0	1	0	0	Blue	-
0	1	0	1	Color bar	-
0	1	1	0	16 grayscale	-
0	1	1	1	Checker board (16x16)	-
1	0	0	0	Crosstalk	-
1	0	0	1	Flicker pattern	-
1	0	1	0	RGBW	-
1	0	1	1	Gray selected by BIST_GRAY[7:0]	-
1	1	0	0	White border	-
1	1	0	1	Black	-
1	1	1	0	Black	-
1	1	1	1	Auto loop from pattern 0 to 12	Default

BIST_GRAY[7:0]: BIST pattern 11 (PTSEL[1:0] = 1011b) grayscale selection. Default is grayscale 128.

BIST_GRAY[7:0]	Function	Note
00h	GS0 (black)	-
01h	GS1	-
:	:	-
80h	GS128	Default
:	:	-
FFh	GS255 (white)	-

R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	1Eh	1/0	FDENB[7:0]							
			1	0	0	0	1	0	0	0

FDENB[7]: OTP reload failure detection enable.

FDENB[6]: OTP programming failure detection enable.

FDENB[5]: EEPROM reload failure detection enable.

FDENB[4]: Input signals from TTL/LVDS failure detection enable.

FDENB[3]: CRC error detection enable.

FDENB[2]: Source data latch failure detection enable.

FDENB[1]: VDD voltage abnormal detection enable.

FDENB[0]: LVDS unlock detection enable.

FDENB[7] FDENB[3]	Function	Note
0	Enable	-
1	Disable	Default

FDENB[6] FDENB[5] FDENB[4] FDENB[2] FDENB[1] FDENB[0]	Function	Note
0	Enable	Default
1	Disable	-

R1Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	17h	1/0	VCOMS[7:0]							
			1	0	0	0	0	0	0	0

VCOMS[7:0]: VCOM level selection.

VCOM= -0.2 - VCOMS[7:0] *0.01V.

VCOMS[7:0]								Function	Note
0	0	0	0	0	0	0	0	-0.20V	-
0	0	0	0	0	0	0	1	-0.21V	-
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	-1.48V	Default
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	0	-2.74V	-
1	1	1	1	1	1	1	1	-2.75V	-

R20h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	20h	1/0	VCOMSOFs[7:0]							
			0	0	0	0	0	0	0	0

VCOMSOFs[7:0]: VCOMS[7:0] offset value for multiply frame polarity control. It is effective when MFPCS[7:0] ≠ 0h.

VCOM = -0.2 - (VCOMS[7:0] + VCOMSOFs[6:0]) * 0.01V when VCOMSOFs[7] = 0.

VCOM = -0.2 - (VCOMS[7:0] - VCOMSOFs[6:0]) * 0.01V when VCOMSOFs[7] = 1.

VCOMS[7:0]								Function	Note
0	0	0	0	0	0	0	0	+0	Default
0	0	0	0	0	0	0	1	+1	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	+127	-
1	0	0	0	0	0	0	0	-0	-
1	0	0	0	0	0	0	1	-1	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	-127	-

R21h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	21h	1/0	-	-	-	VCOMEN	VGHEN	VGLEN	AVDDNEN	AVDDPEN
			0	1	1	1	1	1	1	1

VCOMEN: VCOM regulator enable.

VCOMEN	Function	Note
0	Disable	-
1	Enable	Default

VGHEN: VGH charge pump enable.

VGLEN	Function	Note
0	Disable	Default
1	Enable	-

VGLEN: VGL charge pump enable.

VGHEN	Function	Note
0	Disable	Default
1	Enable	-

AVDDNEN: AVDDN charge pump enable.

AVDDNEN	Function	Note
0	Disable	Default
1	Enable	-

AVDDPEN: AVDDP charge pump enable.

AVDDPEN	Function	Note
0	Disable	Default
1	Enable	-

R22h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	22h	1/0				AVDDPS[4:0]				
			0	0	0	0	1	1	0	1

AVDDPS[3:0]: select AVDDP level. $AVDDP = 5V + AVDDPS[4:0] * 0.1V$, maximum 7V.

AVDDPS[4:0]					Function	Note
0	0	0	0	0	5 V	-
0	0	0	0	1	5.1 V	-
:	:	:	:	:	:	-
0	1	1	0	1	6.3 V	Default
:	:	:	:	:	:	-
1	0	1	0	0	7 V	-
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R23h:

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	23h	1/0	AVDDNS[4:0]							
			0	0	0	0	1	1	0	1

AVDDNS[4:0]: select AVDDN level. $AVDDN = -5V - AVDDNS[4:0] * 0.1V$, minimum -7V.

AVDDNS[4:0]					Function	Note
0	0	0	0	0	-5V	-
0	0	0	0	1	-5.1V	-
:	:	:	:	:	:	-
0	1	1	0	1	-6.3V	Default
:	:	:	:	:	:	-
1	0	1	0	0	-7V	-
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R24h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	24h	1/0	VGHS[3:0]				-	VGLS[2:0]		
			0	1	1	1	0	0	1	1

VGHS[3:0]: VGH voltage selection, $VGH = 7.2V + VGHS[3:0] * 1.2V$, maximum 24V.

VGHS[3:0]				Function	Note
0	0	0	0	7.2V	-
0	0	0	1	8.4V	-
0	0	1	0	9.6V	-
:	:	:	:	:	-
0	1	1	1	15.6V	Default
:	:	:	:	:	-
1	1	0	1	22.8V	-
1	1	1	0	24V	-
1	1	1	1	24V	-

Note: (1) $VGH + |VGL| < 32V$.

VGLS[2:0]: VGL voltage selection, $VGL = -8V - VGLS[2:0] * 1V$.

VGLS[2:0]			Function	Note
0	0	0	-8V	-
0	0	1	-9V	-
0	1	0	-10V	-
0	1	1	-11V	Default
1	0	0	-12V	-
1	0	1	-13V	-
1	1	0	-14V	-
1	1	1	-15V	-

Note: (1) $VGH + |VGL| < 32V$.

R25h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	25h	1/0	-	-	-	VGMPHS[4:0]				
			0	0	0	1	0	1	0	0

VGMPHS[4:0]: select VGMPH level, $VGMPHO = 4V + 0.1V \times VGMPHS[4:0]$, max 6.7V.

VGMPHS[4:0]					Function	Note
0	0	0	0	0	4V	-
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	1	0	0	6V	Default
:	:	:	:	:	:	-
1	1	0	1	1	6.7V	-
1	1	1	0	0	Reserved	
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R26h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	26h	1/0	-	-	-	VGMNHS[4:0]				
			0	0	0	1	0	1	0	0

VGMNHS[4:0]: select VGMNH level, $VGMNH = -4V - 0.1V \times VGMNHS[4:0]$ V, minimum -6.7V.

VGMNHS[4:0]					Function	Note
0	0	0	0	0	-4V	-
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	1	0	0	-6V	Default
:	:	:	:	:	:	-
1	1	0	1	1	-6.7V	-
1	1	1	0	0	Reserved	
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

R27h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	27h	1/0	-	-	-		AVDD_FCP[1:0]		AVDDNX 3	AVDDPX 3
			0	0	0	0	0	0	1	1

AVDD_FCP[1:0]: AVDDP and AVDDN charge pump period selection.

AVDD_FCP[1:0]	Function	Note
0	0.5 bank	Default
0	1 bank	-
1	2 banks	-
1	1 line	-

AVDDNX3: AVDDN boosting mode selection.

AVDDNX3	Function	Note
0	2X	-
1	3X	Default

AVDDPX3: AVDDP boosting mode selection.

AVDDPX3	Function	Note
0	2X	-
1	3X	Default

R28h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	28h	1/0	VGHL_LIMIT	-	VGHL_FCP[1:0]		-	VGLXS	VGHXS[1:0]	
			0	0	0	0	1	1	1	1

VGHL_LIMIT: VGH-VGL voltage limiter enable. When enabled, if VGHS[3:0] is set to make VGH higher than VGL+30V, it will be limited to be VGL+30V.

VGHL_LIMIT	Function	Note
0	No limit	Default
1	VGH-VGL≤30V	-

VGHL_FCP[1:0]: VGH and VGL charge pump period selection.

VGHL_FCP[1:0]	Function	Note
0 0	1 bank	Default
0 1	2 banks	-
1 0	1 line	-
1 1	2 line	-

VGLXS: VGL boosting mode selection.

VGLXS	Function	Note
0	2X	-
1	3X	Default

VGHXS[1:0]: VGH boosting mode selection.

VGHXS[1:0]	Function	Note
0 0	2X	-
0 1	3X	-
1 0	4X	-
1 1	4X	Default

R29h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	29h	1/0	VGMNHEN	VGMPHEN	-	-	-	-	VCOMD[1:0]	
			1	1	1	1	0	0	0	1

VGMNHEN: VGMNH regulator enable.

VGMNHEN	Function	Note
0	Disable	-
1	Enable	Default

VGMPHEN: VGMPH regulator enable.

VGMPHEN	Function	Note
0	Disable	-
1	Enable	Default

VCOMD[1:0]: select VCOM driving capability.

VCOMD[1:0]	Function	Note
0 0	50%	-

0	1	100%	-
1	0	150%	-
1	1	200%	Default

R2Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	2Ah	1/0	-	-	-	VGMPLS[4:0]				
			0	0	0	0	0	0	0	0

VGMPLS[4:0]: VGMPL level selection. $VGMPL = VGMPLS[4:0] / 133 * VGMPH$.

VGMPLS[4:0]					Function	Note
0	0	0	0	0	4/133 * VGMPH	Default
0	0	0	0	1	5/133 * VGMPH	-
:	:	:	:	:		-
1	1	1	1	1	35/133 * VGMPH	-

R2Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	2Bh	1/0	-	-	-	VGMNLS[4:0]				
			0	0	0	0	0	0	0	0

VGMNLS[4:0]: VGMNL level selection. $VGMNL = VGMNLS[4:0] / 133 * VGMNH$.

VGMNLS[4:0]					Function	Note
0	0	0	0	0	4/133 * VGMNH	Default
0	0	0	0	1	5/133 * VGMNH	-
:	:	:	:	:		-
1	1	1	1	1	35/133 * VGMNH	-

R2Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	2Ch	1/0	-	-	-	-	-	-	GASLOA DEN	COM_OT P
			1	0	1	0	1	0	1	0

GASLOADEN: Restart power on sequence when exiting GAS mode.

GASLOADEN	Function	Note
0	Do not restart	-
1	Restart	Default

COM_OTP: Select whether VCOMS[7:0] is loaded from OTP or EEPROM if both are available. Only effective when EEPEN=1.

EEPEN	COM_OTP	Function	Note
0	0	VCOMS[7:0] value from OTP	Default
0	1		-
1	0	VCOMS[7:0] value from OTP	-
1	1	VCOMS[7:0] value from EEPROM	-

R38h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	38h	1/0	-	DLL_BA NK	AGING	LVDS_F MT	LVDS_RXB[1:0]		LVDS_VB[1:0]	
			0	0	0	0	0	1	0	1

DLL_BANK: LVDS low frequency operation.

DLL_BANK	Function	Note
0	LVDS normal speed	Default
1	LVDS lower speed demand	-

AGING: LVDS data lanes enable in self protection mode.

AGING	Function	Note
0	Always enabled	Default
1	LVDS lane 0,1,3 disabled in self protection mode.	-

LVDS_FMT: LVDS data format selection.

LVDS_FMT	Function	Note
0	JEIDA (or NS)	Default
1	VESA (or Thine)	-

LVDS_RXB[1:0]: LVDS receiver bias current selection.

LVDS_RXB[1:0]		Function	Note
0	0	75%	-
0	1	100%	Default
1	0	128%	-
1	1	150%	-

LVDS_VB[1:0]: LVDS DLL bias current selection.

LVDS_VB[1:0]		Function	Note
0	0	75%	-
0	1	100%	Default
1	0	128%	-
1	1	150%	-

R39h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	39h	1/0	-	-	LVDS_BW[1:0]		LVDS_CPB[3:0]			
			0	0		0	0	0	1	0

LVDS_BW[1:0]: LVDS DLL bandwidth selection.

LVDS_BW[1:0]		Function	Note
0	0	100%	-
0	1	110%	Default
1	0	120%	-
1	1	130%	-

LVDS_CPB[3:0]: LVDS charge pump current selection.

LVDS_CPB[3:0]				Function	Note
0	0	0	0	25%	-
0	0	0	1	50%	-
0	0	1	0	75%	Default
0	0	1	1	100%	-
0	1	0	0	125%	-
0	1	0	1	150%	-
0	1	1	0	175%	-
0	1	1	1	200%	-
1	0	0	0	225%	-
1	0	0	1	250%	-
1	0	1	0	275%	-
1	0	1	1	300%	-
1	1	0	0	325%	-
1	1	0	1	350%	-
1	1	1	0	375%	-
1	1	1	1	400%	-

R3Ah~ R3Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	40h	1/0	-	-	-	-	-	LVDS_TUNE_C[2:0]		
			0	0	0	0	0	0	0	0
1	41h	1/0	-	LVDS_TUNE_D0[2:0]			-	LVDS_TUNE_D1[2:0]		
			0	0	0	0	0	0	0	0
1	42h	1/0	-	LVDS_TUNE_D2[2:0]			-	LVDS_TUNE_D3[2:0]		
			0	0	0	0	0	0	0	0

LVDS_TUNE_C[2:0]: LVDS clock lane delay adjustment.

LVDS_TUNE_D[3:0][2:0]: LVDS data lane 3 to 0 delay adjustment.

LVDS_TUNE_C[2:0] LVDS_TUNE_D[3:0][2:0]			Function	Note
0	0	0	Delay 0T (no delay)	Default
0	0	1	Delay 1T	-
0	1	0	Delay 2T	-
0	1	1	Delay 3T	
1	0	0	Delay 4T	
1	0	1	Delay 5T	
1	1	0	Delay 6T	
1	1	1	Delay 7T	-

Note: 1T is one time unit.

R3Fh~R40h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	3Fh	1/0	-					TS_VEN	TS_SEL[1:0]	
			0	0	0	0	0	0	0	0
1	40h	1/0	-	TS_DGMEN[1:0]		TS_DGM_MS	TS_DGM_RT	TS_VGM_EN	TS_VCO_MEN	TS_VGH_LEN
			0	0	0	0	0	0	0	0

TS_SEL[1:0]: Temperature range selection from external temperature sensor.

TS_SEL[1:0]	Function	Note
0	Room temperature	Default
0	Low temperature	-
1	High tempura	-

TS_DGMEN[1:0]: Enable dynamic digital gamma settings loaded from OTP.

TS_DGMEN[1:0]	Function	Note
0	Disable. If W2 is programmed, load W2. Else load W1.	Default
0		-
1	Selected by temperature input TS_SEL[1:0].	
1	Selected manually by TS_DGM_MS.	-

TS_DGM_MS: Manually select digital gamma settings (W1 or W2) when TS_DGMEN[1:0] = 11.

TS_DGM_MS	Function	Note
0	W2	Default
1	W1	-

TS_DGM_RT: Select digital gamma settings (W1 or W2) for room temperature (TS_SEL[1:0]=00) when TS_DGMEN[1:0] = 10.

TS_DGM_RT	Function	Note
0	W2	Default
1	W1	-

TS_VEN: Enable dynamic settings of VCOM, VGMPH/PL/NH/NL and VGH/VGL referring to TS_SEL[1:0].

TS_VEN	Function	Note
0	Disable	Default
1	Enable	-

TS_VGMEN: VGMPH/PL/NH/NL level controlled by TS_SEL[1:0]. Only effective when TS_VEN = 1.

TS_VGMEN	Function	Note
0	Disable	Default
1	Enable	-

TS_VCOMEN: VCOM level controlled by TS_SEL[1:0]. Only effective when TS_VEN = 1.

TS_VCOMEN	Function	Note
0	Disable	Default
1	Enable	-

TS_VGHLEN: VGH, VGL level controlled by TS_SEL[1:0]. Only effective when TS_VEN = 1.

TS_VGHLEN	Function	Note
0	Disable	Default
1	Enable	-

R41h, R42h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	41h	1/0	VCOMS_HT[7:0]							
			1	0	0	0	0	0	0	0
1	42h	1/0	VCOMS_LT[7:0]							
			1	0	0	0	0	0	0	0

VCOMS_HT[7:0], VCOMS_LT[7:0]: VCOM level selection at high / low temperature, effective when TS_VCOMEN = 1. Definition is same to VCOMS[7:0].

R43h, R44h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	43h	1/0	VGHS_HT[3:0]				-	VGLS_HT[2:0]		
			0	1	1	1	0	0	1	1
0	44h	1/0	VGHS_LT[3:0]				-	VGLS_LT[2:0]		
			0	1	1	1	0	0	1	0

VGHS_HT[3:0], VGHS_LT[3:0]: VGH level selection at high / low temperature, effective when TS_VGHLEN = 1. Definition is same to VGHS[3:0].

VGLS_HT[2:0], VGLS_LT[2:0]: VGL level selection at high / low temperature, effective when TS_VGHLEN = 1. Definition is same to VGLS[2:0].

R45h ~ R51h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	45h	1/0	-	-	-	VGMPHS_HT[4:0]				
			0	0	1	1	0	1	0	0
0	46h	1/0	-	-	-	VGMNHS_HT[4:0]				
			1	0	1	1	0	1	0	0
0	47h	1/0	-	-	-	VGMPHS_LT[4:0]				
			0	1	1	1	0	1	0	0
0	48h	1/0	-	-	-	VGMNHS_LT[4:0]				
			0	1	1	1	0	1	0	0
0	49h	1/0	-	-	-	-	VGMPLS_HT[4]	VGMNLS_HT[4]	VGMPLS_LT[4]	VGMNLS_LT[4]
			0	0	0	0	0	0	0	0
0	50h	1/0	VGMPLS_HT[3:0]				VGMNLS_HT[3:0]			
			0	0	0	0	0	0	0	0
0	51h	1/0	VGMPLS_LT[3:0]				VGMNLS_LT[3:0]			
			0	0	0	0	0	0	0	0

VGMPHS_HT[4:0], VGMPHS_LT[4:0]: VGMPH level selection at high high / low temperature, effective when TS_VGMEN = 1. Definition is same to VGMPHS[4:0].

VGMNHS_HT[4:0], VGMNHS_LT[4:0]: VGMNH level selection at high high / low temperature, effective when TS_VGMEN = 1. Definition is same to VGMNHS[4:0].

VGMPLS_HT[4:0], VGMPLS_LT[4:0]: VGMPH level selection at high high / low temperature, effective when TS_VGMEN = 1. Definition is same to VGMPLS[4:0].

VGMNLS_HT[4:0], VGMNLS_LT[4:0]: VGMNL level selection at high high / low temperature, effective when TS_VGMEN = 1. Definition is same to VGMNLS[4:0].

R4Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	4Ch	1/0	-	CRC_OUT_SWAP	CRC_TYPE[1:0]		CRC_IN_SWAP[1:0]		CRC_INI_SEL	CRC_EN
			0	0	0	0	0	0	0	0

CRC_OUT_SWAP: CRC calculated data output order selection.

CRC OUTPUT SWAP	CRC type	CRC_SUMO[23:16]	CRC_SUMO[15:8]	CRC_SUMO[7:0]
0	24-bit	[23:16]	[15:8]	[7:0]
	16-bit	0	[15:8]	[7:0]
	8-bit	0	0	[7:0]
1	24-bit	[7:0]	[15:8]	[23:16]
	16-bit	0	[7:0]	[15:8]
	8-bit	0	0	[7:0]

CRC_TYPE[1:0]: CRC type selection.

CRC_TYPE[1:0]		Function	Note
0	0	24-bit (CRC-24)	Default
0	1	16-bit (CRC-16-CCITT)	-
1	0	8-bit (CRC-8-ATM)	-
1	1		-

CRC_IN_SWAP[1:0]: CRC input RGB data order selection.

CRC_INPUT_SWAP[1:0]		input data for CRC engine			Note
		D[23:16]	D[15:8]	D[7:0]	
0	0	R[7:0]	G[7:0]	B[7:0]	Default
0	1	R[0:7]	G[0:7]	B[0:7]	-
1	0	B[7:0]	G[7:0]	R[7:0]	-
1	1	B[0:7]	G[0:7]	R[0:7]	-

CRC_INI_SEL: CRC initial value selection.

CRC_INI_SEL	Function	Note
0	000000h	Default
1	FFFFFFh	-

CRC_EN: CRC function enable.

CRC_EN	Function	Note
0	Disable	Default
1	Enable	-

R4Dh~R4F: Predicted CRC result input from the system.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	4Dh	1/0	CRC_SUMI[23:16]							
			0	0	0	0	0	0	0	0
0	4Eh	1/0	CRC_SUMI[15:8]							
			0	0	0	0	0	0	0	0
0	4Fh	1/0	CRC_SUMI[7:0]							
			0	0	0	0	0	0	0	0

R51h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	51h	1/0	CHIP_ID[3:0]				VER_ID[3:0]			
			0	0	0	0	0	0	0	1

R52h~R54h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	52h	1/0	-	-	ROB[5:0]					
			0	0	0	1	0	0	0	0
0	53h	1/0	-	-	GOB[5:0]					
			0	0	0	1	0	0	0	0
0	54h	1/0	-	-	BOB[5:0]					
			0	0	0	1	0	0	0	0

ROB[5:0]: Offset (brightness) of red.

GOB[5:0]: Offset (brightness) of green.

BOB[5:0]: Offset (brightness) of blue.

ROB[5:0] GOB[5:0] BOB[5:0]	Function	Note
00h	-16	
01h	-15	-
02h	-14	
:	:	
10h	0	Default
:	:	
3Fh	+47	

R55h~R57h: Gain (contrast) of red.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	55h	1/0	Rr_C[7:0]							
			1	0	0	0	0	0	0	0
0	56h	1/0	Gg_C[7:0]							
			1	0	0	0	0	0	0	0
0	57h	1/0	Bb_C[7:0]							
			1	0	0	0	0	0	0	0

Rr_C[7:0]: Gain (contrast) of red.

Gg_C[7:0]: Gain (contrast) of green.

Bb_C[7:0]: Gain (contrast) of blue.

Rr_C[7:0] Gg_C[7:0] Bb_C[7:0]	Function	Note
00h	128/256	
01h	129/256	-
02h	130/256	
:	:	
80h	256/256	Default
:	:	
3Fh	383/256	

R58h~R5Dh:

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Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	58h	1/0	-	-	Rg_C[5:0]					
			0	0	0	0	0	0	0	0
0	59h	1/0	-	-	Rb_C[5:0]					
			0	0	0	0	0	0	0	0
0	5Ah	1/0	-	-	Gr_C[5:0]					
			0	0	0	0	0	0	0	0
0	5Bh	1/0	-	-	Gb_C[5:0]					
			0	0	0	0	0	0	0	0
0	5Ch	1/0	-	-	Br_C[5:0]					
			0	0	0	0	0	0	0	0
0	5Dh	1/0	-	-	Bg_C[5:0]					
			0	0	0	0	0	0	0	0

Rg_C[5:0]: Mutual gain from green to red.

Rb_C[5:0]: Mutual gain from blue to red.

Gr_C[5:0]: Mutual gain from red to green.

Gb_C[5:0]: Mutual gain from blue to green.

Br_C[5:0]: Mutual gain from red to blue.

Bg_C[5:0]: Mutual gain from red to green.

Rg_C[5:0], Rb_C[5:0], Gr_C[5:0], Gb_C[5:0], Br_C[5:0], Bg_C[5:0]	Function	Note
00h	0/512	Default
01h	1/512	-
02h	2/512	-
	:	-
20h	32/512	-
	:	-
3Fh	63/512	-

R73h~R75h: CRC calculated result output.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	73h	1	CRC_SUMO[23:16]							
			0	0	0	0	0	0	0	0
0	74h	1	CRC_SUMO[15:8]							
			0	0	0	0	0	0	0	0
0	75h	1	CRC_SUMO[7:0]							
			0	0	0	0	0	0	0	0

R76h~R77h: CRC error count.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	76h	1	CRC_ERR_CNT[7:0]							
			0	0	0	0	0	0	0	0
0	77h	1	CRC_ERR_CNT[15:8]							
			0	0	0	0	0	0	0	0

R7A:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	7A	1	FDEF[7:0]							
			0	0	0	0	0	0	0	0

FDEF[7:0]: Error flags of eight failure modes.

FDEF[7] FDEF[6] FDEF[5] FDEF[4] FDEF[3] FDEF[2] FDEF[1] FDEF[0]	Function	Note
0	Normal	Default
1	Fail	

R7Bh~R7Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0	7B	1	CHIPNAME0[7:0]							
			1	0	0	0	0	0	1	0
0	7C	1	CHIPNAME1[7:0]							
			0	1	1	1	1	0	0	0
0	7D	1	CHIPNAME2[7:0]							
			0	0	0	0	1	0	1	0

CHIPNAME[0:2][7:0]: Read only registers with fixed values 82h, 78h and 0Ah.

8.2.3 Page 1 for OTP program sequence setting

R00h: Register page selection. Set to 01h for page 1.

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
all	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	1	1	1

R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	01h	1/0	-	-	OTP_Group[5:0]					
			0	0	0	0	0	0	0	0

(TBD)

OTP_Group[5:0]	Reg. mapping	Note
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
23		
25		
26		
27		
28		
29		

R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	02h	1/0	WOTP[7:0]							
			1	0	0	1	1	0	0	1

WOTP[7:0]: OTP program command enable/disable.

WOTP[7:0]								Function	Note
0	0	0	0	0	0	0	0	Disable	-
:	:	:	:	:	:	:	:	Disable	-
0	1	1	0	0	1	0	1	Disable	-
0	1	1	0	0	1	1	0	Enable	-
0	1	1	0	0	1	1	1	Disable	-

:	:	:	:	:	:	:	:	Disable	-
1	0	0	1	1	0	0	1	Disable	Default
:	:	:	:	:	:	:	:	Disable	-
1	1	1	1	1	1	1	1	Disable	-

R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	03h	1/0	-	-	-	-	-	OTP_RELOAD	OTP_RD	OTP_WR
			0	0	0	0	0	0	0	0

OTP_RELOAD: OTP reload function enable.

OTP_RELOAD	Function	Note
0	Disable	Default
1	Enable	-

OTP_RD: OTP read function enable.

OTP_RD	Function	Note
0	Disable	Default
1	Enable	-

OTP_WR: OTP write function enable.

OTP_WR	Function	Note
0	Disable	Default
1	Enable	-

R04h~R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	04h	1	-	-	-	-	-	-	-	OTP_IND EX[8]
			0	0	0	0	0	0	0	0
	05h		OTP_INDEX[7:0]							
			0	0	0	0	0	0	0	0

OTP_INDEX[8:0]: OTP address for read.

R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	06h	1/0	PDOB[7:0]							
			0	0	0	0	0	0	0	0

PDOB[7:0]: OTP read out data. (Read only)

R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Ah	1/0	EEP_PWD[7:0]							
			0	1	0	1	1	0	1	0

EEP_PWD[7:0]: EEPROM software reload password

EEP_PWD[7:0]									Function	Note
0	0	0	0	0	0	0	0	0	Disable	-
:	:	:	:	:	:	:	:	:	Disable	-
0	1	0	1	1	0	1	0	0	Disable	Default
:	:	:	:	:	:	:	:	:	Disable	-
1	0	1	0	0	1	0	1	1	Enable	-
:	:	:	:	:	:	:	:	:	Disable	-
1	0	0	1	1	0	0	0	1	Disable	-
:	:	:	:	:	:	:	:	:	Disable	-
1	1	1	1	1	1	1	1	1	Disable	-

R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Bh	1/0	EEP_CK SUM_FAI L	-	-	-	-	-	-	EEP_RL _CMD
			0	0	0	0	0	0	0	0

EEP_CKSUM_FAIL: EEPROM Check-sum fail. (Read only)

EEP_CKSUM_FAIL	Function	Note
0	-	-
1	Check-sum fail	-

EEP_RL_CMD: EEPROM software triggered reload, it's auto cleared register.

EEP_RL_CMD	Function	Note
0	-	-
1	Reload trigger	-

R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Ch	1/0	-	-	-	-	-	-	-	EESEL
			0	0	0	0	0	0	0	0

EESEL: EEPROM controlled by System or Driver IC

EESEL	Function	Note
0	EEPROM controlled by Driver IC	Default
1	EEPROM controlled by System	-

R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Dh	1	TCON_CKSUM[7:0]							
			0	0	0	0	0	0	0	0

TCON_CKSUM[7:0]: The Check-sum of TCON calculator. (read only)

R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Eh	1	EEPROM_CKSUM[7:0]							
			0	0	0	0	0	0	0	0

EEPROM_CKSUM[7:0]: The Check-sum of read from EEPROM. (read only)

R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
1	0Fh	1	-	-	-	-	-	-	-	FDEF[6]
			0	0	0	0	0	0	0	0

FDEF[6]: Error flag of OTP programming, same to page 0, R7Ah[6]. (Read only)

FDEF[6]	Function	Note
0	Normal	-
1	Fail	-

8.3 EEPROM mapping table

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	Dummy data = 8'h52								52
1	0	TR	DINT[1:0]		0	MODE[1:0]		NB	
2	RL	TB	INV[1:0]		INTL		RS[1:0]		
3	RBEXC	HSP	VSP	CLOCKP	0		PON	POFF	
4	GASEN	SPFEN	SPFSEL	BISTEN	0				
5	VSTS[7:0]								
6	HSTS[7:0]								
7	0		BISRDLY1 0T	THZBS	LASTBLK_ DATA	SD_GND_V			
8	PCR[1:0]		ENDRV	EQ0W[4:0]					
9	BC[2:0]			EQ1W[4:0]					
10	MFPCS[3:0]				POCSD[1:0]		POCGM[1:0]		
11	0		BANK0OFS[5:0]						
12	0		BANK1OFS[5:0]						
13	0		TOEB[6:0]						
14	0		TOEF[6:0]						
15	0								
16	0								
17	0								
18	0								
19	0				GATEPASS[3:0]				
20	GATENUM[7:0]								
21					HSETPASS[3:0]				
22	HSETNUM[7:0]								
23	BISTHBS[6:0]								
24	reserved		BISTVBS[3:0]				BISTCLKS[1:0]		
25	FFLAGP OL	TPSYNC_F AIL_ENB	FFLAGEN	TPSVBEN	TPSYNCP OL	TPSYNCS[2:0]			
26	TPS_OFS[7:0]								
27	0				PTSEL[3:0]				
28	BIST_GRAY[7:0]								
29	FDENB[7:0]								
30	VCOMS[7:0]								
31	VCOMSOFS[7:0]								
32	0			VCOMEN	VGHEN	VGLEN	AVDDNE N	AVDDPE N	
33	0			AVDDPS[4:0]					
34	0			AVDDNS[4:0]					
35	0	VGHS[3:0]				VGLS[2:0]			
36	0			VGMPHS[4:0]					
37	0			VGMNHS[4:0]					

38	reserved				AVDD_FCP[1:0]		AVDDNX 3	AVDDPX3	
39	VGHL_L IMIT	0	VGHL_FCP[1:0]		0	VGLXS	VGHXS[1:0]		
40	VGMNH EN	VGMPHEN	OCPEN	0			VCOMD[1:0]		
41	VGMPLS[7:0]								
42	VGMNLS[7:0]								
43	0							COM_OT P	
44	0								
45	0								
46	0								
47	0								
48	0								
49	0								
50	0								
51	0								
52	0								
53	0								
54	0								
55	0	DLL_BANK	AGING	LVDS_FMT	LVDS_RXB[1:0]		LVDS_VB[1:0]		
56	0		LVDS_BW[1:0]		LVDS_CPB[3:0]				
57	0					LVDS_TUNE_C[2:0]			
58	0	LVDS_TUNE_D0[2:0]			0	LVDS_TUNE_D1[2:0]			
59	0	LVDS_TUNE_D2[2:0]			0	LVDS_TUNE_D3[2:0]			
60	0								
61	0								
62	0					TS_VEN	TS_SEL[1:0]		
63	0	TS_DGMEN[1:0]		TS_DGM_ MS	TS_DGM_ RT	TS_VGM EN	TS_VCO MEN	TS_VGHL EN	
64	VCOMS_HT[7:0]								
65	VCOMS_LT[7:0]								
66	VGHS_HT[3:0]				0	VGLS_HT[2:0]			
67	VGHS_LT[3:0]				0	VGLS_LT[2:0]			
68	0			VGMPHS_HT[4:0]					
69	0			VGMNHS_HT[4:0]					
70	0			VGMPHS_LT[4:0]					
71	0			VGMNHS_LT[4:0]					
72	0				VGMNLS_L T[4]	VGMPLS LT[4]	VGMNLS HT[4]	VGMPLS HT[4]	
73	VGMNLS_HT[3:0]				VGMPLS_HT[3:0]				
74	VGMNLS_LT[3:0]				VGMPLS_LT[3:0]				

75	CRC_OUT_SWAP	CRC_TYPE[1:0]	CRC_IN_SWAP[1:0]	CRC_IN_SEL	CRC_EN
76	CRC_SUMI[23:16]				
77	CRC_SUMI[15:8]				
78	CRC_SUMI[7:0]				
79	VENDER_ID0[7:0]				
80	VENDER_ID1[7:0]				
81	0	ROB[5:0]			
82	0	GOB[5:0]			
83	0	BOB[5:0]			
84	Rr_C[7:0]				
85	Gg_C[7:0]				
86	Bb_C[7:0]				
87	0	Rg_c[5:0]			
88	0	Rb_c[5:0]			
89	0	Gr_c[5:0]			
90	0	Gb_c[5:0]			
91	0	Br_c[5:0]			
92	0	Bg_c[5:0]			
93	0				
94	PGMA1R[7:0]				
95	PGMA2R[7:0]				
96	PGMA3R[7:0]				
97	PGMA4R[7:0]				
98	PGMA5R[7:0]				
99	PGMA6R[7:0]				
100	PGMA7R[7:0]				
101	PGMA8R[7:0]				
102	PGMA9R[7:0]				
103	PGMA10R[7:0]				
104	PGMA11R[7:0]				
105	PGMA12R[7:0]				
106	PGMA13R[7:0]				
107	PGMA14R[7:0]				
108	PGMA15R[7:0]				
109	PGMA16R[7:0]				
110	PGMA17R[7:0]				
111	PGMA18R[7:0]				
112	PGMA19R[7:0]				
113	PGMA20R[7:0]				
114	PGMA21R[7:0]				

115	PGMA22R[7:0]				
116	PGMA23R[7:0]				
117	PGMA24R[7:0]				
118	PGMA25R[7:0]				
119	PGMA26R[7:0]				
120	PGMA27R[7:0]				
121	PGMA28R[7:0]				
122	PGMA29R[7:0]				
123	PGMA30R[7:0]				
124	PGMA31R[7:0]				
125	PGMA32R[7:0]				
126	PGMA1R[9:8]	PGMA2R[9:8]	PGMA3R[9:8]	PGMA4R[9:8]	
127	PGMA5R[9:8]	PGMA6R[9:8]	PGMA7R[9:8]	PGMA8R[9:8]	
128	PGMA9R[9:8]	PGMA10R[9:8]	PGMA11R[9:8]	PGMA12R[9:8]	
129	PGMA13R[9:8]	PGMA14R[9:8]	PGMA15R[9:8]	PGMA16R[9:8]	
130	PGMA17R[9:8]	PGMA18R[9:8]	PGMA19R[9:8]	PGMA20R[9:8]	
131	PGMA21R[9:8]	PGMA22R[9:8]	PGMA23R[9:8]	PGMA24R[9:8]	
132	PGMA25R[9:8]	PGMA26R[9:8]	PGMA27R[9:8]	PGMA28R[9:8]	
133	PGMA29R[9:8]	PGMA30R[9:8]	PGMA31R[9:8]	PGMA32R[9:8]	
134	PGMA33R[7:0]				
135	PGMA33R[9:8]	0			
136	PGMA1G[7:0]				
137	PGMA2G[7:0]				
138	PGMA3G[7:0]				
139	PGMA4G[7:0]				
140	PGMA5G[7:0]				
141	PGMA6G[7:0]				
142	PGMA7G[7:0]				
143	PGMA8G[7:0]				
144	PGMA9G[7:0]				
145	PGMA10G[7:0]				
146	PGMA11G[7:0]				
147	PGMA12G[7:0]				
148	PGMA13G[7:0]				
149	PGMA14G[7:0]				
150	PGMA15G[7:0]				
151	PGMA16G[7:0]				
152	PGMA17G[7:0]				
153	PGMA18G[7:0]				
154	PGMA19G[7:0]				

155	PGMA20G[7:0]				
156	PGMA21G[7:0]				
157	PGMA22G[7:0]				
158	PGMA23G[7:0]				
159	PGMA24G[7:0]				
160	PGMA25G[7:0]				
161	PGMA26G[7:0]				
162	PGMA27G[7:0]				
163	PGMA28G[7:0]				
164	PGMA29G[7:0]				
165	PGMA30G[7:0]				
166	PGMA31G[7:0]				
167	PGMA32G[7:0]				
168	PGMA1G[9:8]	PGMA2G[9:8]	PGMA3G[9:8]	PGMA4G[9:8]	
169	PGMA5G[9:8]	PGMA6G[9:8]	PGMA7G[9:8]	PGMA8G[9:8]	
170	PGMA9G[9:8]	PGMA10G[9:8]	PGMA11G[9:8]	PGMA12G[9:8]	
171	PGMA13G[9:8]	PGMA14G[9:8]	PGMA15G[9:8]	PGMA16G[9:8]	
172	PGMA17G[9:8]	PGMA18G[9:8]	PGMA19G[9:8]	PGMA20G[9:8]	
173	PGMA21G[9:8]	PGMA22G[9:8]	PGMA23G[9:8]	PGMA24G[9:8]	
174	PGMA25G[9:8]	PGMA26G[9:8]	PGMA27G[9:8]	PGMA28G[9:8]	
175	PGMA29G[9:8]	PGMA30G[9:8]	PGMA31G[9:8]	PGMA32G[9:8]	
176	PGMA33G[7:0]				
177	PGMA33G[9:8]	0			
178	PGMA1B[7:0]				
179	PGMA2B[7:0]				
180	PGMA3B[7:0]				
181	PGMA4B[7:0]				
182	PGMA5B[7:0]				
183	PGMA6B[7:0]				
184	PGMA7B[7:0]				
185	PGMA8B[7:0]				
186	PGMA9B[7:0]				
187	PGMA10B[7:0]				
188	PGMA11B[7:0]				
189	PGMA12B[7:0]				
190	PGMA13B[7:0]				
191	PGMA14B[7:0]				
192	PGMA15B[7:0]				
193	PGMA16B[7:0]				
194	PGMA17B[7:0]				

195	PGMA18B[7:0]				
196	PGMA19B[7:0]				
197	PGMA20B[7:0]				
198	PGMA21B[7:0]				
199	PGMA22B[7:0]				
200	PGMA23B[7:0]				
201	PGMA24B[7:0]				
202	PGMA25B[7:0]				
203	PGMA26B[7:0]				
204	PGMA27B[7:0]				
205	PGMA28B[7:0]				
206	PGMA29B[7:0]				
207	PGMA30B[7:0]				
208	PGMA31B[7:0]				
209	PGMA32B[7:0]				
210	PGMA1B[9:8]	PGMA2B[9:8]	PGMA3B[9:8]	PGMA4B[9:8]	
211	PGMA5B[9:8]	PGMA6B[9:8]	PGMA7B[9:8]	PGMA8B[9:8]	
212	PGMA9B[9:8]	PGMA10B[9:8]	PGMA11B[9:8]	PGMA12B[9:8]	
213	PGMA13B[9:8]	PGMA14B[9:8]	PGMA15B[9:8]	PGMA16B[9:8]	
214	PGMA17B[9:8]	PGMA18B[9:8]	PGMA19B[9:8]	PGMA20B[9:8]	
215	PGMA21B[9:8]	PGMA22B[9:8]	PGMA23B[9:8]	PGMA24B[9:8]	
216	PGMA25B[9:8]	PGMA26B[9:8]	PGMA27B[9:8]	PGMA28B[9:8]	
217	PGMA29B[9:8]	PGMA30B[9:8]	PGMA31B[9:8]	PGMA32B[9:8]	
218	PGMA33B[7:0]				
219	PGMA33B[9:8]	0			
220	NGMA1R[7:0]				
221	NGMA2R[7:0]				
222	NGMA3R[7:0]				
223	NGMA4R[7:0]				
224	NGMA5R[7:0]				
225	NGMA6R[7:0]				
226	NGMA7R[7:0]				
227	NGMA8R[7:0]				
228	NGMA9R[7:0]				
229	NGMA10R[7:0]				
230	NGMA11R[7:0]				
231	NGMA12R[7:0]				
232	NGMA13R[7:0]				
233	NGMA14R[7:0]				
234	NGMA15R[7:0]				

235	NGMA16R[7:0]				
236	NGMA17R[7:0]				
237	NGMA18R[7:0]				
238	NGMA19R[7:0]				
239	NGMA20R[7:0]				
240	NGMA21R[7:0]				
241	NGMA22R[7:0]				
242	NGMA23R[7:0]				
243	NGMA24R[7:0]				
244	NGMA25R[7:0]				
245	NGMA26R[7:0]				
246	NGMA27R[7:0]				
247	NGMA28R[7:0]				
248	NGMA29R[7:0]				
249	NGMA30R[7:0]				
250	NGMA31R[7:0]				
251	NGMA32R[7:0]				
252	NGMA1R[9:8]	NGMA2R[9:8]	NGMA3R[9:8]	NGMA4R[9:8]	
253	NGMA5R[9:8]	NGMA6R[9:8]	NGMA7R[9:8]	NGMA8R[9:8]	
254	NGMA9R[9:8]	NGMA10R[9:8]	NGMA11R[9:8]	NGMA12R[9:8]	
255	NGMA13R[9:8]	NGMA14R[9:8]	NGMA15R[9:8]	NGMA16R[9:8]	
256	NGMA17R[9:8]	NGMA18R[9:8]	NGMA19R[9:8]	NGMA20R[9:8]	
257	NGMA21R[9:8]	NGMA22R[9:8]	NGMA23R[9:8]	NGMA24R[9:8]	
258	NGMA25R[9:8]	NGMA26R[9:8]	NGMA27R[9:8]	NGMA28R[9:8]	
259	NGMA29R[9:8]	NGMA30R[9:8]	NGMA31R[9:8]	NGMA32R[9:8]	
260	NGMA33R[7:0]				
261	NGMA33R[9:8]	0			
262	NGMA1G[7:0]				
263	NGMA2G[7:0]				
264	NGMA3G[7:0]				
265	NGMA4G[7:0]				
266	NGMA5G[7:0]				
267	NGMA6G[7:0]				
268	NGMA7G[7:0]				
269	NGMA8G[7:0]				
270	NGMA9G[7:0]				
271	NGMA10G[7:0]				
272	NGMA11G[7:0]				
273	NGMA12G[7:0]				
274	NGMA13G[7:0]				

275	NGMA14G[7:0]				
276	NGMA15G[7:0]				
277	NGMA16G[7:0]				
278	NGMA17G[7:0]				
279	NGMA18G[7:0]				
280	NGMA19G[7:0]				
281	NGMA20G[7:0]				
282	NGMA21G[7:0]				
283	NGMA22G[7:0]				
284	NGMA23G[7:0]				
285	NGMA24G[7:0]				
286	NGMA25G[7:0]				
287	NGMA26G[7:0]				
288	NGMA27G[7:0]				
289	NGMA28G[7:0]				
290	NGMA29G[7:0]				
291	NGMA30G[7:0]				
292	NGMA31G[7:0]				
293	NGMA32G[7:0]				
294	NGMA1G[9:8]	NGMA2G[9:8]	NGMA3G[9:8]	NGMA4G[9:8]	
295	NGMA5G[9:8]	NGMA6G[9:8]	NGMA7G[9:8]	NGMA8G[9:8]	
296	NGMA9G[9:8]	NGMA10G[9:8]	NGMA11G[9:8]	NGMA12G[9:8]	
297	NGMA13G[9:8]	NGMA14G[9:8]	NGMA15G[9:8]	NGMA16G[9:8]	
298	NGMA17G[9:8]	NGMA18G[9:8]	NGMA19G[9:8]	NGMA20G[9:8]	
299	NGMA21G[9:8]	NGMA22G[9:8]	NGMA23G[9:8]	NGMA24G[9:8]	
300	NGMA25G[9:8]	NGMA26G[9:8]	NGMA27G[9:8]	NGMA28G[9:8]	
301	NGMA29G[9:8]	NGMA30G[9:8]	NGMA31G[9:8]	NGMA32G[9:8]	
302	NGMA33G[7:0]				
303	NGMA33G[9:8]	0			
304	NGMA1B[7:0]				
305	NGMA2B[7:0]				
306	NGMA3B[7:0]				
307	NGMA4B[7:0]				
308	NGMA5B[7:0]				
309	NGMA6B[7:0]				
310	NGMA7B[7:0]				
311	NGMA8B[7:0]				
312	NGMA9B[7:0]				
313	NGMA10B[7:0]				
314	NGMA11B[7:0]				

315	NGMA12B[7:0]				
316	NGMA13B[7:0]				
317	NGMA14B[7:0]				
318	NGMA15B[7:0]				
319	NGMA16B[7:0]				
320	NGMA17B[7:0]				
321	NGMA18B[7:0]				
322	NGMA19B[7:0]				
323	NGMA20B[7:0]				
324	NGMA21B[7:0]				
325	NGMA22B[7:0]				
326	NGMA23B[7:0]				
327	NGMA24B[7:0]				
328	NGMA25B[7:0]				
329	NGMA26B[7:0]				
330	NGMA27B[7:0]				
331	NGMA28B[7:0]				
332	NGMA29B[7:0]				
333	NGMA30B[7:0]				
334	NGMA31B[7:0]				
335	NGMA32B[7:0]				
336	NGMA1B[9:8]	NGMA2B[9:8]	NGMA3B[9:8]	NGMA4B[9:8]	
337	NGMA5B[9:8]	NGMA6B[9:8]	NGMA7B[9:8]	NGMA8B[9:8]	
338	NGMA9B[9:8]	NGMA10B[9:8]	NGMA11B[9:8]	NGMA12B[9:8]	
339	NGMA13B[9:8]	NGMA14B[9:8]	NGMA15B[9:8]	NGMA16B[9:8]	
340	NGMA17B[9:8]	NGMA18B[9:8]	NGMA19B[9:8]	NGMA20B[9:8]	
341	NGMA21B[9:8]	NGMA22B[9:8]	NGMA23B[9:8]	NGMA24B[9:8]	
342	NGMA25B[9:8]	NGMA26B[9:8]	NGMA27B[9:8]	NGMA28B[9:8]	
343	NGMA29B[9:8]	NGMA30B[9:8]	NGMA31B[9:8]	NGMA32B[9:8]	
344	NGMA33B[7:0]				
345	NGMA33B[9:8]	0			
346	expected EEPROM checksum				

9. AC/DC Characteristics

9.1 AC characteristics

9.1.1TTL interface

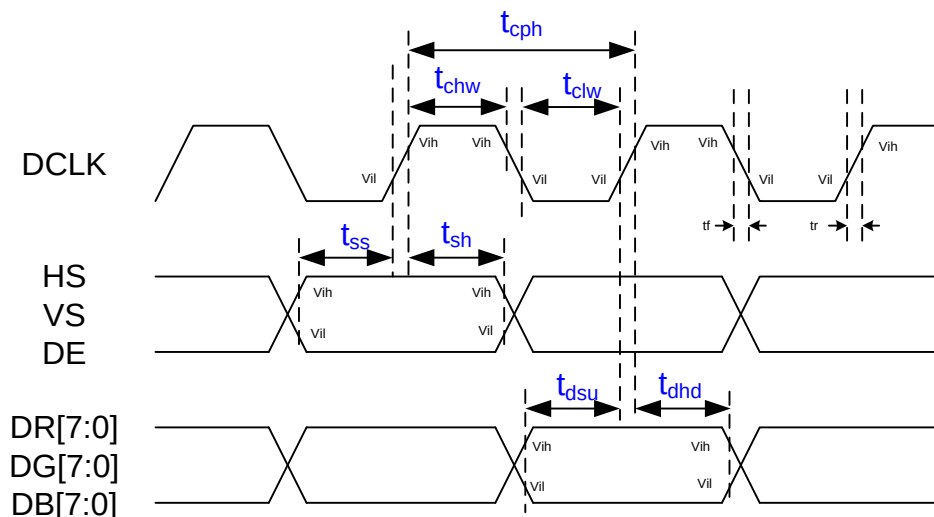


Figure 9.1: TTL input AC characteristics

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK period	T_{cph}	16.8	-	-	ns
DCLK clock high width	T_{chw}	6	-	-	ns
DCLK clock low width	T_{clw}	6	-	-	ns
VS setup time	T_{ss}	5	-	-	ns
VS hold time	T_{sh}	5	-	-	ns
HS setup time	T_{ss}	5	-	-	ns
HS hold time	T_{sh}	5	-	-	ns
DE setup time	T_{ss}	5	-	-	ns
DE hold time	T_{sh}	5	-	-	ns
Data setup time	T_{dsu}	5	-	-	ns
Data hold time	T_{dhd}	5	-	-	ns
Input signal rising time	T_r	-	-	10	ns
Input signal falling time	T_f	-	-	10	ns

Note: DCLK frequency is 60MHz for serial RGB, 20MHz for parallel RGB.

Table 9.1: TTL input timing parameter

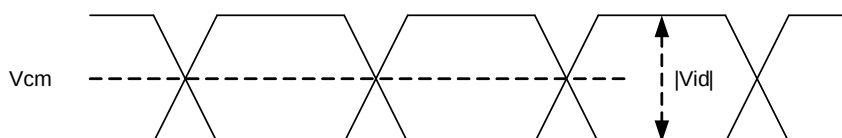
9.1.2 LVDS interface

(VDD1=VDD2=2.7 to 3.6V, VSS1=VSS2=VSSA=0V, T_{OP} = -40 to 105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Differential input high Threshold voltage	V _{th}	V _{cm} =1.2V	-	-	+0.1	V
Differential input low threshold voltage	V _{tl}		-0.1	-	-	V
Differential input common Mode voltage	V _{cm}	-	1	1.2	1.8- V _{id} /2	V
Differential input voltage	V _{id}	-	0.2	-	0.6	V
Differential input leakage Current	I _{lvleak}	-	-10	-	+10	μA
Termination Resistor	Z _{id}	-	80	100	120	Ω

Single-ended:

LVCLKP (R),
LVCLKN (R),
LVD [3:0]P(R),
LVD [3:0]N(R)



Differential:

LVCLKP (R)-LVCLKN (R),
LVD [3:0]P(R)-
LVD [3:0]N(R)

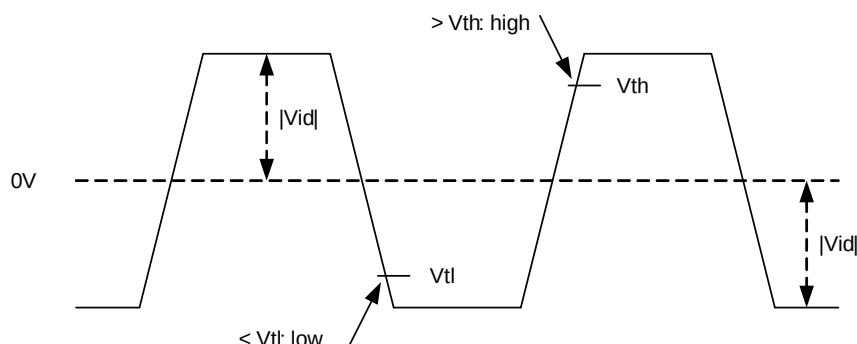
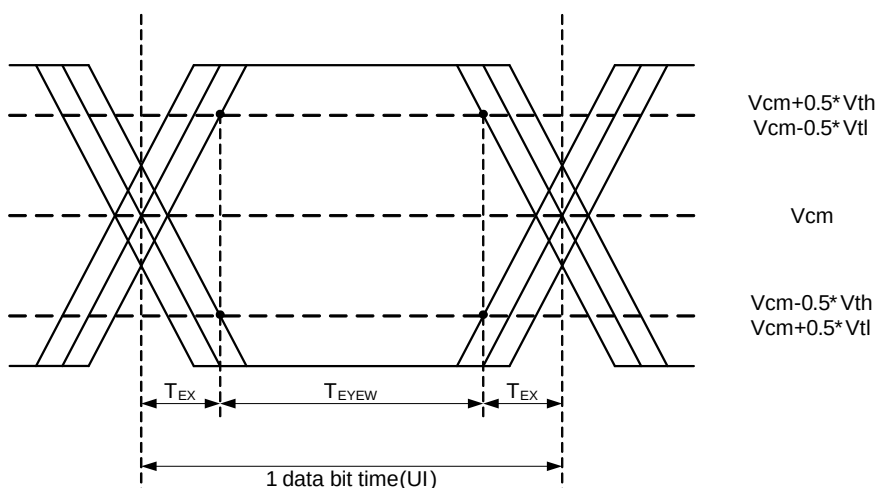


Figure 9.2: LVDS input

Single-ended:

**LVD [3:0]P,
LVD [3:0]N**



Differential:

LVD [3:0]P-LVD [3:0]N

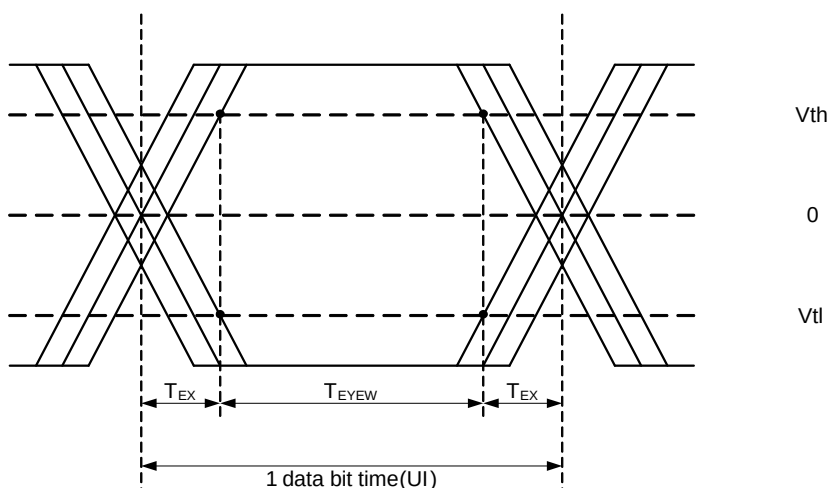


Figure 9.3: LVDS input eye diagram

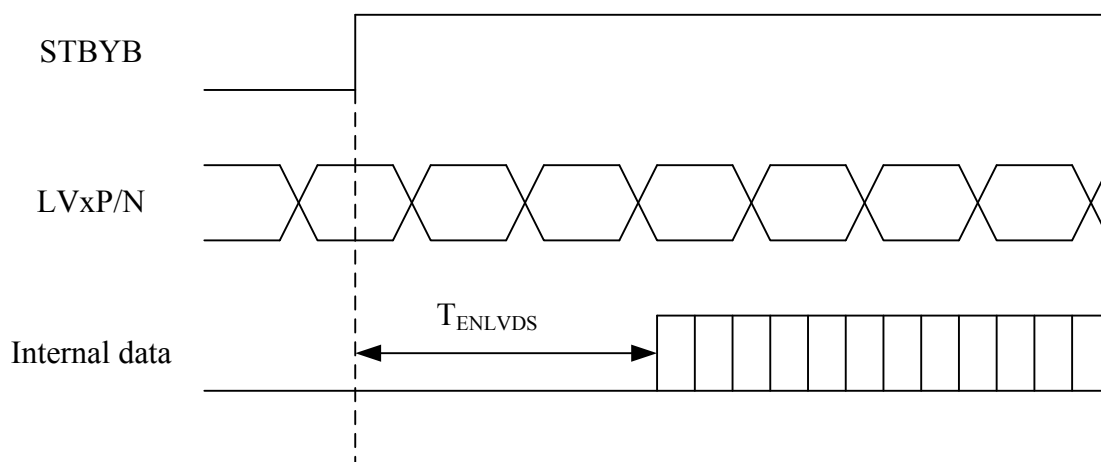


Figure 9.4: LVDS wake up time

9.1.2.1 4- or 3-lane LVDS interface

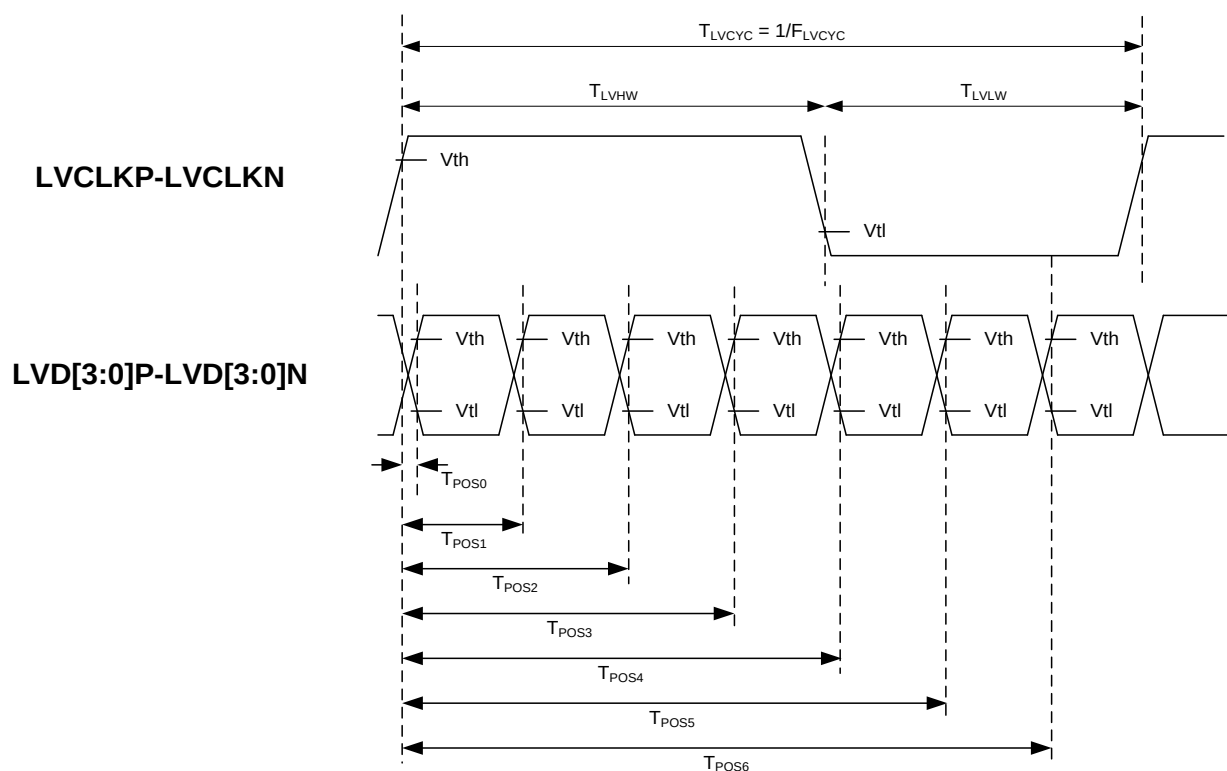


Figure 9.5: LVDS input timing, 4- or 3-lane

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	FLVCYC	TBD	-	30	MHz
Clock period	TLVCYC	33	-	TBD	nsec
1 data bit time	UI	-	1/7	-	TLVCYC
Clock high time	LVHW	2.9	4	4.1	UI
Clock low time	LVLW	2.9	3	4.1	UI
Position n (n=0~6)	TPOS[n]	n-0.2	n	n+0.2	UI
Input eye width	TEYEW	0.6	-	-	UI
Input eye border	TEX	-	-	0.2	UI
LVDS wake up time	TENLVDS	-	-	250	μs

Table 9.2: LVDS input timing parameters, 4- or 3-lane

9.1.2.2 2-lane LVDS interface

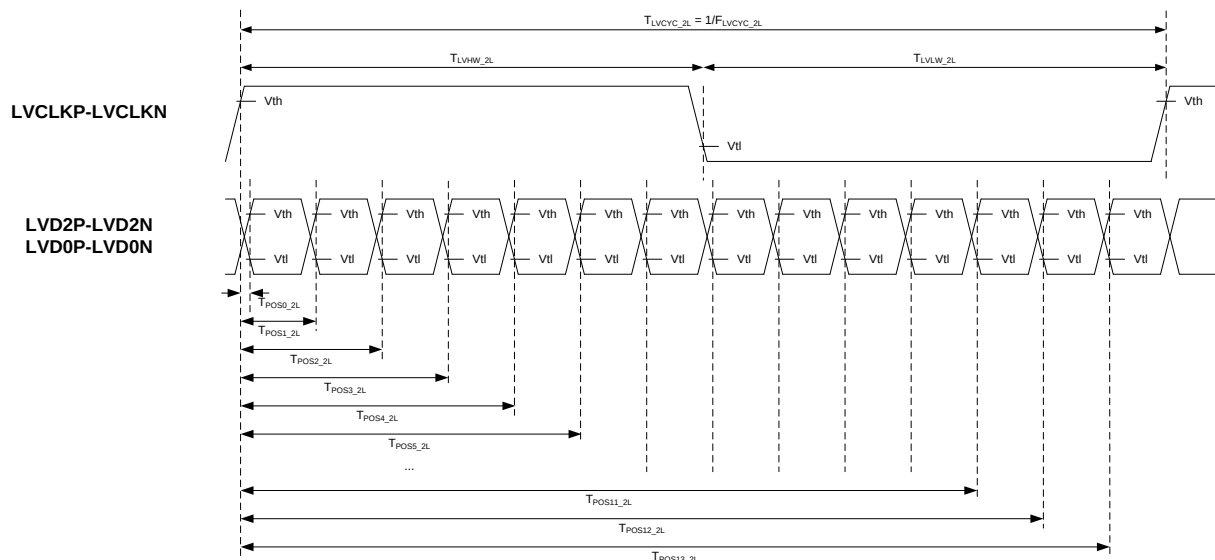


Figure 9.6: LVDS input timing, 2-lane

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	FLVCCYC_2L	TBD	-	15	MHz
Clock period	TLVCCYC_2L	66	-	TBD	nsec
1 data bit time	UI_2L	-	1/14	-	TLVCCYC_2L
Clock high time	LVHW_2L	6	7	8	UI
Clock low time	LVLW_2L	6	7	8	UI
Position n (n=0~13)	TPOS[n]_2L	n-0.2	n	n+0.2	UI
Input eye width	TEYEW	0.6	-	-	UI
Input eye border	TEX	-	-	0.2	UI
LVDS wake up time	TENLVDS	-	-	250	μs

Table 9.3: LVDS input timing parameters, 2-lane

9.1.3 LVDS with SSC

The LVDS receiver supports spread spectrum clocking (SSC). Modulation frequency is proportional to LVDS clock frequency.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Modulation frequency	SSC _{MF}	LVDS clock frequency centered at 30MHz.	-	-	75	KHz
		LVDS clock frequency centered at 20MHz.	-	-	50	KHz
		LVDS clock frequency centered at 10MHz.	-	-	25	KHz
		LVDS clock frequency centered at 3MHz.	-	-	7.5	KHz
Modulation rate	SSC _{MR}	LVDS clock frequency + SSC _{MR} is in the range of 3~30MHz.	-	-	±5	%

Table 9.4: SSC limitation of LVDS interface