HX8310-A Data Sheet

128RGB x 160 dot, 260,000-Color TFT Controller Driver with Internal RAM

Preliminary Version 0.6

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Himax Technologies , Inc.
No.605, Chungshan Rd., Hsinhua,
Tainan County, 712, Taiwan. R.O.C.

TEL: 886-6-505-0880
FAX: 886-6-505-0891

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HX8310-A

128RGB x 160 dot, 260,000 color TFT controller driver with internal RAM

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General Description

This manual is described the Himax's HX8310-A 128RGB*160 dots resolution driving controller. The HX8310-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 128RGB*160 dots at maximum.

The HX8310-A has five system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, an 68-system 18-/16-/9-/8-bit bus interface, VSYNC interface (internal clock, DB17-0) , serial data transfer interface and RGB18-/16-/6-bit bus interface (DOTCLOCK, VSYNC, HSYNC, ENABLE, PD17-0). In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers. The HX8310-A also supports various functions to reduce the power consumption of a LCD system via software control, such as an standby mode, sleep mode and 8-color display mode,

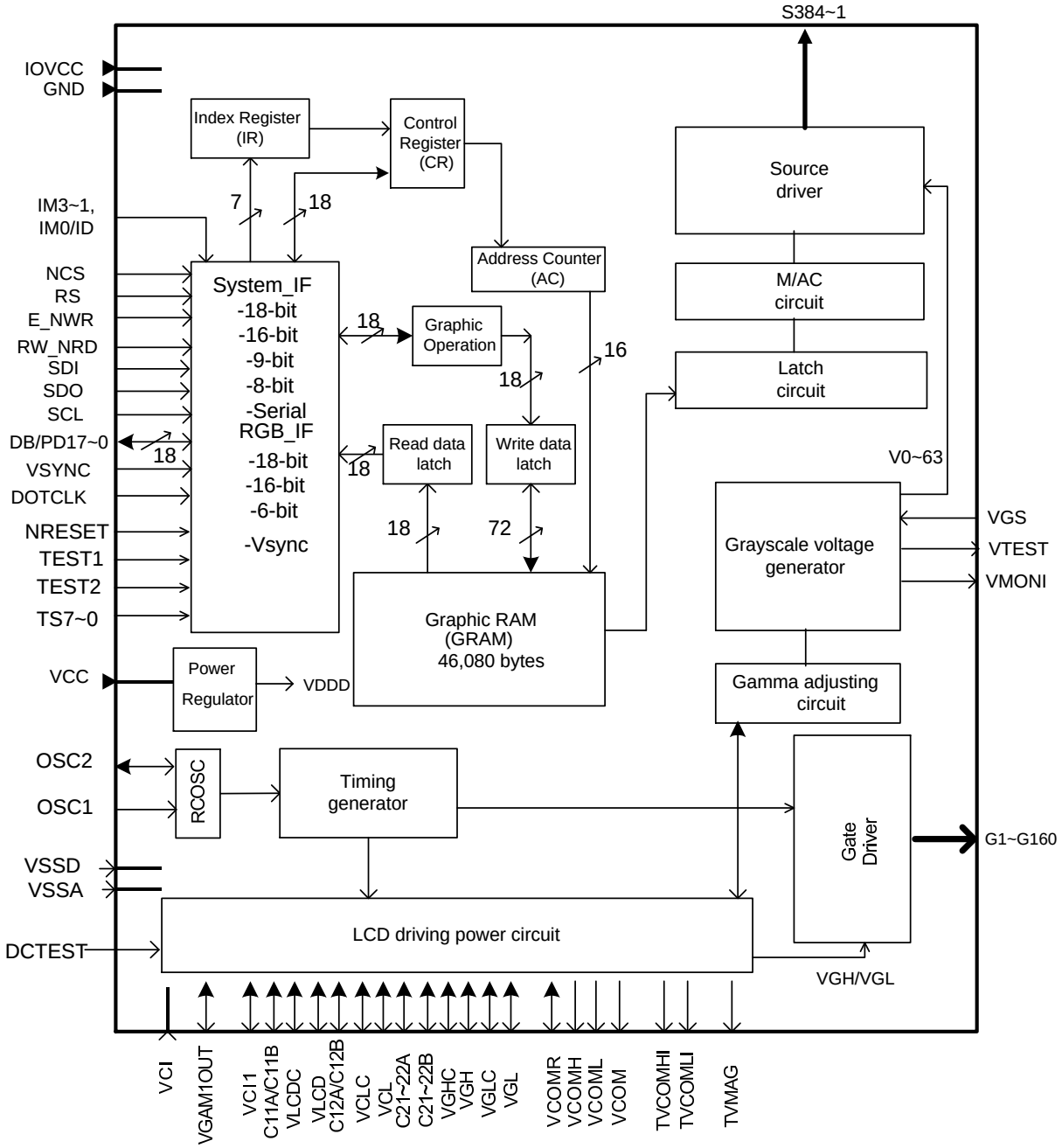
The HX8310-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

Features

- Single chip solution to drive a TFT panel
- 128RGB x 160-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support interface:
  - 80 system interface (8-/9-/16-/18-bit bus)
  - 68 system interface (8-/9-/16-/18-bit bus)
  - Serial Data Transfer Interface
  - RGB interface (6-/16-/18-bit bus)
  - VSYNC data transfer interface
- Internal graphics RAM capacity: 46,080 bytes
- The 260,000 colors can be displayed at the same time with gamma correction
- The vertical scroll display function in line units
- Internal operation circuit of liquid crystal display:
  - Source channel: 384
  - Gate line: 160
- To write data in a window-RAM address area by using a window-address function
- Bit-operation functions for graphics transaction:
  - The write data mask function in bit unit
  - The logical operation in pixel unit and conditional write function
- Low-power consumption architecture supports:
  - VCI = 2.5 to 3.3 V (internal reference voltage)
  - IOVCC = 1.65 to 3.3 V (Interface IO)
  - VCC = 2.4 to 3.3 V (corresponding low-voltage operation)
  - VLCD=4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - standby mode
    - sleep mode
- n-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Internal oscillator and hardware reset function
- γ - correction function which makes 262,144 colors available simultaneously
- Vertical scrolling function
- Step–up circuit to step up liquid crystal driving voltages up to 6 times

1. Device Overview

1.1 Block Diagram



1.2 Pin Description

<table>
<tr><th colspan="4">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Descriptions</th></tr>
<tr><td>IM3~0</td><td>I</td><td>4</td><td>VSSD/
IOVCC</td><td>Select the MPU interface mode as listed below
<table>
<tr><th>IM0</th><th>IM1</th><th>IM2</th><th>IM3(ID)</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit interface, 68-system</td><td>DB17-10, 8-1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8-bit interface, 68-system</td><td>DB17-10-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit interface, 80-system</td><td>DB17-10, 8-1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit interface, 80-system</td><td>DB17-10</td></tr>
<tr><td>ID</td><td>0</td><td>1</td><td>0</td><td>Serial data transfer interface</td><td>DB1-0</td></tr>
<tr><td>*</td><td>1</td><td>1</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>18-bit interface, 68-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9-bit interface, 68-system</td><td>DB17-9</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit interface, 80-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>9-bit interface, 80-system</td><td>DB17-9</td></tr>
<tr><td>*</td><td>*</td><td>1</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
</table>
Note: If the serial data transfer interface was selected, IM0 pin is used like the ID setting for the device code in transfer data.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>MPU</td><td>The signal for register index or register command select .
Low: Register index or internal status (in read operation);
High: Register command.
Connect to IOVCC or VSSD level when serial data transfer interface is selected.</td></tr>
<tr><td>E_NWR</td><td>I</td><td>1</td><td>MPU</td><td>In 80-system bus interface mode, serves as a write strobe signal. Write data at “low” level. In 68-system Interface mode, serves as an ENABLE signal to control data read/write operation.</td></tr>
<tr><td>RW_NRD</td><td>I</td><td>1</td><td>MPU</td><td>Low: Write；High: Read
Serves as a read signal and reads data at the low level in I80 system interface. Fix it to IOVCC or VSSD level when using serial data transfer interface.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVCC level.
Low: Selected (access enabled)
The polarity of the ENABLE signal is inverted by the EPL bit.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>Enable</td><td>Update</td></tr>
<tr><td>0</td><td>1</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>0</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>1</td><td>Enable</td><td>Update</td></tr>
</table></td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td>Serial data transfer input in serial data transfer interface mode. Data would be input on the rising edge of the SCL signal. Fixed to either IOVCC or VSSD if not in use.</td></tr>
<tr><td>SCL</td><td>I</td><td>1</td><td>MPU</td><td>A synchronizing clock signal in serial data transfer interface mode.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. Fix to the IOVCC level when not used.
If VSPL=0: Active low.
If VSPL=1: Active high.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. Fix to the IOVCC level when not used.
If HSPL=0: Active low.
If HSPL=1: Active high.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal. Fix to the IOVCC level when not used.
If DPL=0: Data are input on the rising edge of DOTCLK.
If DPL=1: Data are input on the falling edge of DOTCLK.</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
VCOMR	I	1	Variable Resistor or open	A VCOMH reference voltage. When adjusting VCOMH externally, set registers to halt the VCOMH internal adjusting circuit and place a variable resistor between VGAM1OUT and VSSD. Otherwise, leave this pin open and adjust VCOMH by setting the internal register of the HX8310-A.
VLCD	I	1	Stabilizing capacitor, VLCDC	An output from the step-up circuit1,of twice the VCI1 level. Connect to a stabilizing capacitor between VSSD and VLCD. Place a schotkey barrier diode (see “configuration of the power supply”).VLCD=4.0 to 5.5V
VGH	I	1	VGHC	A power supply for the TFT LCD’s gate driver. Connect to VGHC. Max. VGH = 16.5V
VGL	I	1	VGLC	A power supply for the TFT LCD’s gate driver. Connect to VGLC. Min. VGL = -14.0V
VCL	I	1	VCLC	A power supply for the VCOML level. Connect to VCLC. VCL=0 ~ -3.3V
TEST1	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
TEST2	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel use .
VCI	I	1	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VCILVL	I	1	Power supply	Generates a reference voltage (VCI1OUT,REGP) from the VCILVL level according to the ratio determined by the VC2-0 BITS. Connect to VCI on the FPC.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial data transfer output in serial data transfer interface mode. Data would be output on the falling edge of the SCL signal. Fixed to either IOVCC or VSSD if not in use.
S1~384	O	384	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0,DATA IN THE ram address “0000” is output from S1.If SS=1,the same data in the ram address “0000” is output from S396. S1,S4,S7,…display red (R),S2,S5,S8,…display green (G),and S3,S6,S9,…display blue(B) (SS=0).
G1~160	O	160	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM	O	2	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel**.**
VCOMH	O	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	O	1	Stabilizing capacitor or open	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VCOML output stops and a capacitor for stabilization is not needed.
FLM	O	1	MPU or open	A frame head pulse (amplitude: IOVCC-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it
VLCDC	O	1	VLCD	A power supply for the source driver outputs. A reference voltage for the step-up circuit2
VGHC	O	1	Stabilizing capacitor, VGH	An output from the step-up circuit2.or 4~6 time the VCI1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGHC. Place a schottkey barrier diode between VCI and VGHC.Pleace a schottkey barrier diode (see “configuration of the power supply ”).VGHC=16.5V
VGLC	O	1	Stabilizing capacitor, VGL	An output from the step-up circuit2.or -3~-5 time the VCI1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGLC. Place a schottkey barrier diode between VCI and VGHC.Pleace a schottkey barrier diode (see “configuration of the power supply ”). Min. VGLC = -16.5V
VCLC	O	1	Stabilizing capacitor, VCL	An output from the step-up circuit of 1-tme the VCI1 level. Connect to stabilizing capacitor .VCLC=0~-3.3V
TS0~7	O	8	Open	Test pins. Disconnect them.
VMONI	O	1	Open	A test pin. Disconnect it.
IOVCCDUM1	O	1	Input pin	Internal IOVCC level outputs. When adjacent input pins are fixed to the IOVCC level, short-circuit them.
IOVSSDDUM 1~3	O	3	Input pin	Internal VSSD level outputs. When neighboring input pins are fixed to the VSSD level, short-circuit them.
VTESTOUT	O	1	-	A test pin. Disconnect it.
TVCOMHI	O	1	Stabilizing capacitor	A test pin for VCOMH. Connect with the capacitor 0.1uF.
TVCOMLI	I/O	1	Stabilizing Capacitor	A test pin for VCOML. Connect with the capacitor 0.1uF.
TVMAG	O	1	Stabilizing capacitor	A test pin for VCOML. Connect with the capacitor 0.1uF.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B C21A, C21B C22A, C22B	I/O	8	Step-up Capacitor	connect these pins to the capacitors for the step-up circuit 2. according to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0~17/PD0~17	I/O	18	MPU	When Operates in system interface mode, it is used liked a 18-bit bi-directional data bus. 8-bit bus: use DB8-DB1 9-bit bus: use DB8-DB0 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use PD17-PD12 16-bit bus: use PD17-PD13 and PD11-PD1 18-bit bus: use PD17-PD0 Connected unused pins to the IOVCC or VSSD level.
REGP	I/O	1	Test pin	A test pin for VGAM1OUT. Disconnect it.
VCI1OUT	I/O	1	Stabilizing Capacitor	A reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
VGAM1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM between VSSD and VGL from the refernce voltage between VCI and VSSD that is generated internally. The factor of step-up can be set through an internal register. Connect a capacitor for stabilization. As it is the reference voltage for generating VgoffOUT. Connect to an external power supply lower than VGL, if not using the adjustment circuit 2.
TESTO1, 2	-	2	-	Dummy pads. Disconnect them.
DUMMY1~31	-	31	Open	Dummy pads. Disconnect them.
VCMDUM11~15	-	5	Open	Dummy pads . Can be wiring to the COG panel from VCOM1.
VCMDUM21~25	-	5	Open	Dummy pads . Can be wiring to the COG panel from VCOM2.
DUMMYR1~8	-	8	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3 and DUMMYR6 are short-circuited within the chip. DUMMYR4 and DUMMYR5 are short-circuited withinthe chip. DUMMYR7 and DUMMYR8 are short-circuited within the chip.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCC	-	1	Power supply	A power supply for the internal logic. VCC = 2.4 ~ 3.3V
IOVCC	-	1	Power supply	Power supply for interface pin. IOVCC = 1.65 ~3.3 V. Connecte to VCC on the FPC if IOVCC = VCC for preventing noise when using the COG method.
VSSD	-	1	Power supply	Ground for the logic side. VSSD = 0V
VSSA	-	1	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.

1.3 Pin assignments

. Chip Size : 16040 um x 1165 um
. Chip thickness :400um (typ.)
. Pad Location : PAD center
. Coordinate Origin : Chip Center
.Au Bump Size :
1. 56um x 47um
Corner dummy
No.179, No.728

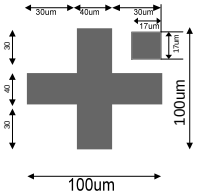
2. 59um x 91um
Input :
No.1 to No.159

3. 26um x 85um
Staggered LCD output side:
No.180 to No.727

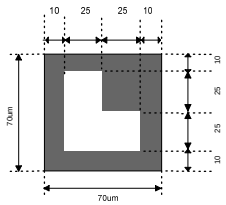
4. 85um X 26um
Staggered LCD output side:
No.160 to No.178
No.729 to No.747

. Au bump pitch:
. Au bump height : 15um(typ.)
. Numbers in the figure corresponds to pad coordinate numbers.

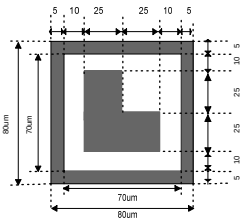
. Alignment Mark
A. Arrangement : Two places
Coordinate (X,Y) = (-7890, -452.5)
Coordinate (X,Y) = (7890, -452.5)



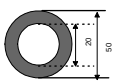
B-1. Coordinate (X, Y) = (7900, 395.5)



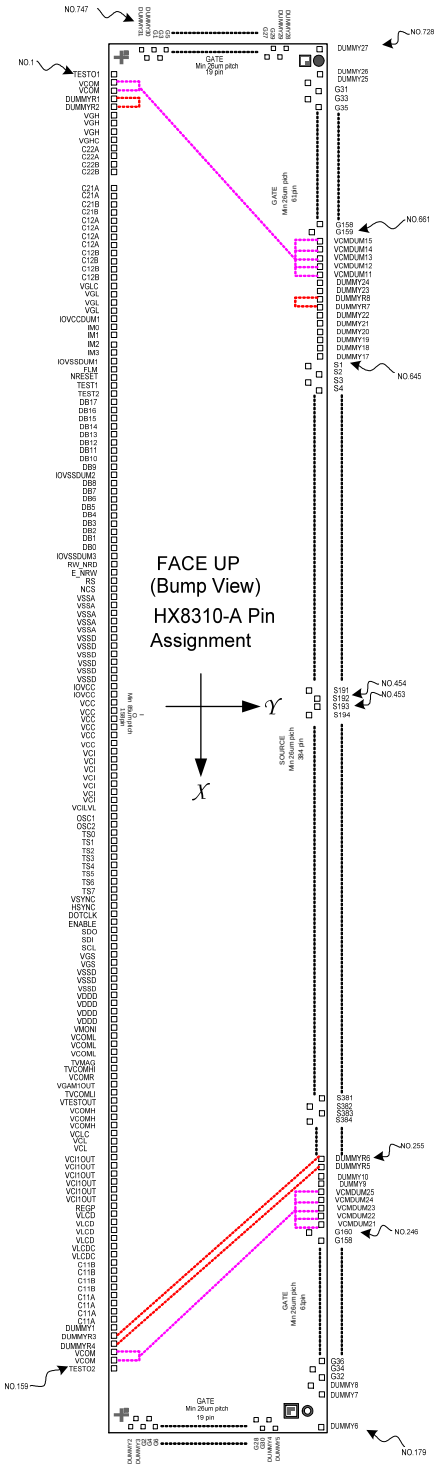
B-2. Coordinate (X, Y) = (-7900, 395.5)



C-1. Coordinate (X, Y) = (7844, 482.5)



C-2. Coordinate (X, Y) = (-7844, 482.5)



PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	TESTO1	-7565	-462	61	E_NWR	-1938	-462	121	TVMAG	3996	-462	181	DUMMY8	7584	355
2	VCOM	-7480	-462	62	RS	-1853	-462	122	TVCOMHI	4081	-462	182	G32	7558	465
3	VCOM	-7395	-462	63	NCS	-1768	-462	123	VCOMR	4166	-462	183	G34	7532	355
4	DUMMYR1	-7260	-462	64	VSSA	-1558	-462	124	VGAM1OUT	4251	-462	184	G36	7506	465
5	DUMMYR2	-7175	-462	65	VSSA	-1473	-462	125	TVCOMLI	4368	-462	185	G38	7480	355
6	VGH	-7090	-462	66	VSSA	-1388	-462	126	VTESTOUT	4548	-462	186	G40	7454	465
7	VGH	-6842	-462	67	VSSA	-1303	-462	127	VCOMH	4633	-462	187	G42	7428	355
8	VGH	-6757	-462	68	VSSA	-1218	-462	128	VCOMH	4718	-462	188	G44	7402	465
9	VGHC	-6672	-462	69	VSSD	-1039	-462	129	VCOMH	4803	-462	189	G46	7376	355
10	C22A	-6587	-462	70	VSSD	-954	-462	130	VCLC	4928	-462	190	G48	7350	465
11	C22A	-6502	-462	71	VSSD	-869	-462	131	VCL	5013	-462	191	G50	7324	355
12	C22B	-6417	-462	72	VSSD	-784	-462	132	VCL	5098	-462	192	G52	7298	465
13	C22B	-6332	-462	73	VSSD	-699	-462	133	VCI1OUT	5215	-462	193	G54	7272	355
14	C21A	-6247	-462	74	VSSD	-614	-462	134	VCI1OUT	5300	-462	194	G56	7246	465
15	C21A	-6162	-462	75	IOVCC	-497	-462	135	VCI1OUT	5385	-462	195	G58	7220	355
16	C21B	-6077	-462	76	IOVCC	-412	-462	136	VCI1OUT	5470	-462	196	G60	7194	465
17	C21B	-5992	-462	77	VCC	-264	-462	137	VCI1OUT	5555	-462	197	G62	7168	355
18	C12A	-5907	-462	78	VCC	-179	-462	138	VCI1OUT	5640	-462	198	G64	7142	465
19	C12A	-5822	-462	79	VCC	-94	-462	139	REGP	5725	-462	199	G66	7116	355
20	C12A	-5737	-462	80	VCC	-9	-462	140	VLCD	5983	-462	200	G68	7090	465
21	C12A	-5652	-462	81	VCC	76	-462	141	VLCD	6068	-462	201	G70	7012	465
22	C12B	-5567	-462	82	VCC	161	-462	142	VLCD	6153	-462	202	G72	6986	355
23	C12B	-5482	-462	83	VCI	246	-462	143	VLCD	6238	-462	203	G74	6960	465
24	C12B	-5397	-462	84	VCI	331	-462	144	VLCDC	6323	-462	204	G76	6934	355
25	C12B	-5312	-462	85	VCI	416	-462	145	VLCDC	6408	-462	205	G78	6908	465
26	VGLC	-5133	-462	86	VCI	501	-462	146	C11B	6493	-462	206	G80	6882	355
27	VGL	-5048	-462	87	VCI	586	-462	147	C11B	6578	-462	207	G82	6856	465
28	VGL	-4963	-462	88	VCI	671	-462	148	C11B	6663	-462	208	G84	6830	355
29	VGL	-4878	-462	89	VCI	756	-462	149	C11B	6748	-462	209	G86	6804	465
30	IOVCCDUM1	-4668	-462	90	VCILVL	920	-462	150	C11A	6833	-462	210	G88	6778	355
31	IM0	-4583	-462	91	OSC1	1037	-462	151	C11A	6918	-462	211	G90	6752	465
32	IM1	-4498	-462	92	OSC2	1122	-462	152	C11A	7003	-462	212	G92	6726	355
33	IM2	-4413	-462	93	TS0	1278	-462	153	C11A	7088	-462	213	G94	6700	465
34	IM3	-4233	-462	94	TS1	1363	-462	154	DUMMY1	7199	-462	214	G96	6674	355
35	IOVSSDDUM1	-4148	-462	95	TS2	1448	-462	155	DUMMYR3	7284	-462	215	G98	6648	465
36	FLM	-4063	-462	96	TS3	1533	-462	156	DUMMYR4	7369	-462	216	G100	6622	355
37	NRESET	-3978	-462	97	TS4	1618	-462	157	VCOM	7454	-462	217	G102	6596	465
38	TEST1(VDC_ENB)	-3893	-462	98	TS5	1703	-462	158	VCOM	7539	-462	218	G104	6570	355
39	TEST2	-3808	-462	99	TS6	1788	-462	159	TESTO2	7624	-462	219	G106	6544	465
40	DB17	-3723	-462	100	TS7	1873	-462	160	DUMMY2	7902	-258	220	G108	6518	355
41	DB16	-3638	-462	101	VSYNC	1958	-462	161	DUMMY3	7792	-232	221	G110	6492	465
42	DB15	-3553	-462	102	HSYNC	2043	-462	162	G2	7902	-206	222	G112	6466	355
43	DB14	-3468	-462	103	DOTCLK	2128	-462	163	G4	7792	-180	223	G114	6440	465
44	DB13	-3383	-462	104	ENABLE	2213	-462	164	G6	7902	-154	224	G116	6414	355
45	DB12	-3298	-462	105	SDO	2298	-462	165	G8	7792	-128	225	G118	6388	465
46	DB11	-3213	-462	106	SDI	2383	-462	166	G10	7902	-102	226	G120	6362	355
47	DB10	-3128	-462	107	SCL	2468	-462	167	G12	7792	-76	227	G122	6336	465
48	DB9	-3043	-462	108	VGS	2592	-462	168	G14	7902	-50	228	G124	6310	355
49	IOVSSDDUM2	-2958	-462	109	VGS	2677	-462	169	G16	7792	-24	229	G126	6284	465
50	DB8	-2873	-462	110	VSSD	2841	-462	170	G18	7902	2	230	G128	6258	355
51	DB7	-2788	-462	111	VSSD	2926	-462	171	G20	7792	28	231	G130	6232	465
52	DB6	-2703	-462	112	VSSD	3011	-462	172	G22	7902	54	232	G132	6206	355
53	DB5	-2618	-462	113	VDDD	3221	-462	173	G24	7792	80	233	G134	6180	465
54	DB4	-2533	-462	114	VDDD	3306	-462	174	G26	7902	106	234	G136	6154	355
55	DB3	-2448	-462	115	VDDD	3391	-462	175	G28	7792	132	235	G138	6128	465
56	DB2	-2363	-462	116	VDDD	3476	-462	176	G30	7902	158	236	G140	6102	355
57	DB1	-2278	-462	117	VMONI	3561	-462	177	DUMMY4	7792	184	237	G142	6076	465
58	DB0	-2193	-462	118	VCOML	3678	-462	178	DUMMY5	7902	210	238	G144	6050	355
59	IOVSSDDUM3	-2108	-462	119	VCOML	3763	-462	179	DUMMY6	7917	484	239	G146	6024	465
60	RW_NRD	-2023	-462	120	VCOML	3848	-462	180	DUMMY7	7610	465	240	G148	5998	355

No.	Pad name	X	Y
241	G150	5972	465
242	G152	5946	355
243	G154	5920	465
244	G156	5894	355
245	G158	5868	465
246	G160	5842	355
247	VCMDUM21	5709	465
248	VCMDUM22	5657	465
249	VCMDUM23	5605	465
250	VCMDUM24	5553	465
251	VCMDUM25	5501	465
252	DUMMY9	5449	465
253	DUMMY10	5320	465
254	DUMMYR5	5268	465
255	DUMMYR6	5216	465
256	DUMMY11	5190	355
257	DUMMY12	5164	465
258	DUMMY13	5138	355
259	DUMMY14	5112	465
260	DUMMY15	5086	355
261	DUMMY16	5060	465
262	S384	5034	355
263	S383	5008	465
264	S382	4982	355
265	S381	4956	465
266	S380	4930	355
267	S379	4904	465
268	S378	4878	355
269	S377	4852	465
270	S376	4826	355
271	S375	4800	465
272	S374	4774	355
273	S373	4748	465
274	S372	4722	355
275	S371	4696	465
276	S370	4670	355
277	S369	4644	465
278	S368	4618	355
279	S367	4592	465
280	S366	4566	355
281	S365	4540	465
282	S364	4514	355
283	S363	4488	465
284	S362	4462	355
285	S361	4436	465
286	S360	4410	355
287	S359	4384	465
288	S358	4358	355
289	S357	4332	465
290	S356	4306	355
291	S355	4280	465
292	S354	4254	355
293	S353	4228	465
294	S352	4202	355
295	S351	4176	465
296	S350	4150	355
297	S349	4124	465
298	S348	4098	355
299	S347	4072	465
300	S346	4046	355
301	S345	4020	465
302	S344	3994	355
303	S343	3968	465
304	S342	3942	355
305	S341	3916	465
306	S340	3890	355
307	S339	3864	465
308	S338	3838	355
309	S337	3812	465
310	S336	3786	355
311	S335	3760	465
312	S334	3734	355
313	S333	3708	465
314	S332	3682	355
315	S331	3656	465
316	S330	3630	355
317	S329	3604	465
318	S328	3578	355
319	S327	3552	465
320	S326	3526	355
321	S325	3500	465
322	S324	3474	355
323	S323	3448	465
324	S322	3422	355
325	S321	3396	465
326	S320	3370	355
327	S319	3344	465
328	S318	3318	355
329	S317	3292	465
330	S316	3266	355
331	S315	3240	465
332	S314	3214	355
333	S313	3188	465
334	S312	3162	355
335	S311	3136	465
336	S310	3110	355
337	S309	3084	465
338	S308	3058	355
339	S307	3032	465
340	S306	3006	355
341	S305	2980	465
342	S304	2954	355
343	S303	2928	465
344	S302	2902	355
345	S301	2876	465
346	S300	2850	355
347	S299	2824	465
348	S298	2798	355
349	S297	2772	465
350	S296	2746	355
351	S295	2720	465
352	S294	2694	355
353	S293	2668	465
354	S292	2642	355
355	S291	2616	465
356	S290	2590	355
357	S289	2564	465
358	S288	2538	355
359	S287	2512	465
360	S286	2486	355
361	S285	2460	465
362	S284	2434	355
363	S283	2408	465
364	S282	2382	355
365	S281	2356	465
366	S280	2330	355
367	S279	2304	465
368	S278	2278	355
369	S277	2252	465
370	S276	2226	355
371	S275	2200	465
372	S274	2174	355
373	S273	2148	465
374	S272	2122	355
375	S271	2096	465
376	S270	2070	355
377	S269	2044	465
378	S268	2018	355
379	S267	1992	465
380	S266	1966	355
381	S265	1940	465
382	S264	1914	355
383	S263	1888	465
384	S262	1862	355
385	S261	1836	465
386	S260	1810	355
387	S259	1784	465
388	S258	1758	355
389	S257	1732	465
390	S256	1706	355
391	S255	1680	465
392	S254	1654	355
393	S253	1628	465
394	S252	1602	355
395	S251	1576	465
396	S250	1550	355
397	S249	1524	465
398	S248	1498	355
399	S247	1472	465
400	S246	1446	355
401	S245	1420	465
402	S244	1394	355
403	S243	1368	465
404	S242	1342	355
405	S241	1316	465
406	S240	1290	355
407	S239	1264	465
408	S238	1238	355
409	S237	1212	465
410	S236	1186	355
411	S235	1160	465
412	S234	1134	355
413	S233	1108	465
414	S232	1082	355
415	S231	1056	465
416	S230	1030	355
417	S229	1004	465
418	S228	978	355
419	S227	952	465
420	S226	926	355
421	S225	900	465
422	S224	874	355
423	S223	848	465
424	S222	822	355
425	S221	796	465
426	S220	770	355
427	S219	744	465
428	S218	718	355
429	S217	692	465
430	S216	666	355
431	S215	640	465
432	S214	614	355
433	S213	588	465
434	S212	562	355
435	S211	536	465
436	S210	510	355
437	S209	484	465
438	S208	458	355
439	S207	432	465
440	S206	406	355
441	S205	380	465
442	S204	354	355
443	S203	328	465
444	S202	302	355
445	S201	276	465
446	S200	250	355
447	S199	224	465
448	S198	198	355
449	S197	172	465
450	S196	146	355
451	S195	120	465
452	S194	94	355
453	S193	68	465
454	S192	-68	465
455	S191	-94	355
456	S190	-120	465
457	S189	-146	355
458	S188	-172	465
459	S187	-198	355
460	S186	-224	465
461	S185	-250	355
462	S184	-276	465
463	S183	-302	355
464	S182	-328	465
465	S181	-354	355
466	S180	-380	465
467	S179	-406	355
468	S178	-432	465
469	S177	-458	355
470	S176	-484	465
471	S175	-510	355
472	S174	-536	465
473	S173	-562	355
474	S172	-588	465
475	S171	-614	355
476	S170	-640	465
477	S169	-666	355
478	S168	-692	465
479	S167	-718	355
480	S166	-744	465
481	S165	-770	355
482	S164	-796	465
483	S163	-822	355
484	S162	-848	465
485	S161	-874	355
486	S160	-900	465
487	S159	-926	355
488	S158	-952	465
489	S157	-978	355
490	S156	-1004	465
491	S155	-1030	355
492	S154	-1056	465
493	S153	-1082	355
494	S152	-1108	465
495	S151	-1134	355
496	S150	-1160	465
497	S149	-1186	355
498	S148	-1212	465
499	S147	-1238	355
500	S146	-1264	465

No.	Pad name	X	Y
501	S145	-1290	355
502	S144	-1316	465
503	S143	-1342	355
504	S142	-1368	465
505	S141	-1394	355
506	S140	-1420	465
507	S139	-1446	355
508	S138	-1472	465
509	S137	-1498	355
510	S136	-1524	465
511	S135	-1550	355
512	S134	-1576	465
513	S133	-1602	355
514	S132	-1628	465
515	S131	-1654	355
516	S130	-1680	465
517	S129	-1706	355
518	S128	-1732	465
519	S127	-1758	355
520	S126	-1784	465
521	S125	-1810	355
522	S124	-1836	465
523	S123	-1862	355
524	S122	-1888	465
525	S121	-1914	355
526	S120	-1940	465
527	S119	-1966	355
528	S118	-1992	465
529	S117	-2018	355
530	S116	-2044	465
531	S115	-2070	355
532	S114	-2096	465
533	S113	-2122	355
534	S112	-2148	465
535	S111	-2174	355
536	S110	-2200	465
537	S109	-2226	355
538	S108	-2252	465
539	S107	-2278	355
540	S106	-2304	465
541	S105	-2330	355
542	S104	-2356	465
543	S103	-2382	355
544	S102	-2408	465
545	S101	-2434	355
546	S100	-2460	465
547	S99	-2486	355
548	S98	-2512	465
549	S97	-2538	355
550	S96	-2564	465
551	S95	-2590	355
552	S94	-2616	465
553	S93	-2642	355
554	S92	-2668	465
555	S91	-2694	355
556	S90	-2720	465
557	S89	-2746	355
558	S88	-2772	465
559	S87	-2798	355
560	S86	-2824	465
561	S85	-2850	355
562	S84	-2876	465
563	S83	-2902	355
564	S82	-2928	465
565	S81	-2954	355
566	S80	-2980	465

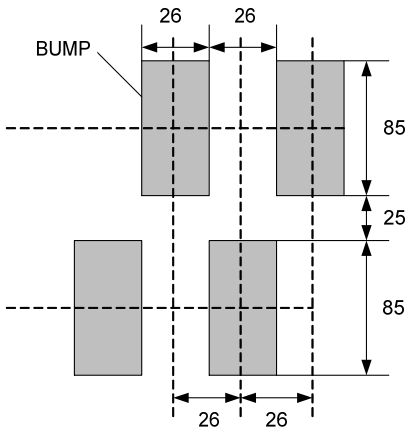
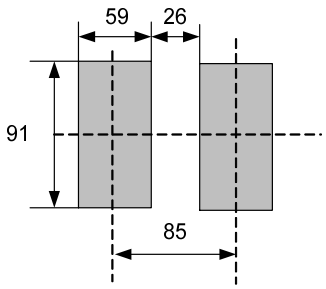
No.	Pad name	X	Y
567	S79	-3006	355
568	S78	-3032	465
569	S77	-3058	355
570	S76	-3084	465
571	S75	-3110	355
572	S74	-3136	465
573	S73	-3162	355
574	S72	-3188	465
575	S71	-3214	355
576	S70	-3240	465
577	S69	-3266	355
578	S68	-3292	465
579	S67	-3318	355
580	S66	-3344	465
581	S65	-3370	355
582	S64	-3396	465
583	S63	-3422	355
584	S62	-3448	465
585	S61	-3474	355
586	S60	-3500	465
587	S59	-3526	355
588	S58	-3552	465
589	S57	-3578	355
590	S56	-3604	465
591	S55	-3630	355
592	S54	-3656	465
593	S53	-3682	355
594	S52	-3708	465
595	S51	-3734	355
596	S50	-3760	465
597	S49	-3786	355
598	S48	-3812	465
599	S47	-3838	355
600	S46	-3864	465
601	S45	-3890	355
602	S44	-3916	465
603	S43	-3942	355
604	S42	-3968	465
605	S41	-3994	355
606	S40	-4020	465
607	S39	-4046	355
608	S38	-4072	465
609	S37	-4098	355
610	S36	-4124	465
611	S35	-4150	355
612	S34	-4176	465
613	S33	-4202	355
614	S32	-4228	465
615	S31	-4254	355
616	S30	-4280	465
617	S29	-4306	355
618	S28	-4332	465
619	S27	-4358	355
620	S26	-4384	465
621	S25	-4410	355
622	S24	-4436	465
623	S23	-4462	355
624	S22	-4488	465
625	S21	-4514	355
626	S20	-4540	465
627	S19	-4566	355
628	S18	-4592	465
629	S17	-4618	355
630	S16	-4644	465
631	S15	-4670	355
632	S14	-4696	465

No.	Pad name	X	Y
633	S13	-4722	355
634	S12	-4748	465
635	S11	-4774	355
636	S10	-4800	465
637	S9	-4826	355
638	S8	-4852	465
639	S7	-4878	355
640	S6	-4904	465
641	S5	-4930	355
642	S4	-4956	465
643	S3	-4982	355
644	S2	-5008	465
645	S1	-5034	355
646	DUMMY17	-5060	465
647	DUMMY18	-5086	355
648	DUMMY19	-5112	465
649	DUMMY20	-5138	355
650	DUMMY21	-5164	465
651	DUMMY22	-5190	355
652	DUMMYR7	-5216	465
653	DUMMYR8	-5268	465
654	DUMMY23	-5320	465
655	DUMMY24	-5449	465
656	VCMDUM11	-5501	465
657	VCMDUM12	-5553	465
658	VCMDUM13	-5605	465
659	VCMDUM14	-5657	465
660	VCMDUM15	-5709	465
661	G159	-5842	355
662	G157	-5868	465
663	G155	-5894	355
664	G153	-5920	465
665	G151	-5946	355
666	G149	-5972	465
667	G147	-5998	355
668	G145	-6024	465
669	G143	-6050	355
670	G141	-6076	465
671	G139	-6102	355
672	G137	-6128	465
673	G135	-6154	355
674	G133	-6180	465
675	G131	-6206	355
676	G129	-6232	465
677	G127	-6258	355
678	G125	-6284	465
679	G123	-6310	355
680	G121	-6336	465
681	G119	-6362	355
682	G117	-6388	465
683	G115	-6414	355
684	G113	-6440	465
685	G111	-6466	355
686	G109	-6492	465
687	G107	-6518	355
688	G105	-6544	465
689	G103	-6570	355
690	G101	-6596	465
691	G99	-6622	355
692	G97	-6648	465
693	G95	-6674	355
694	G93	-6700	465
695	G91	-6726	355
696	G89	-6752	465
697	G87	-6778	355
698	G85	-6804	465

No.	Pad name	X	Y
699	G83	-6830	355
700	G81	-6856	465
701	G79	-6882	355
702	G77	-6908	465
703	G75	-6934	355
704	G73	-6960	465
705	G71	-6986	355
706	G69	-7012	465
707	G67	-7090	465
708	G65	-7116	355
709	G63	-7142	465
710	G61	-7168	355
711	G59	-7194	465
712	G57	-7220	355
713	G55	-7246	465
714	G53	-7272	355
715	G51	-7298	465
716	G49	-7324	355
717	G47	-7350	465
718	G45	-7376	355
719	G43	-7402	465
720	G41	-7428	355
721	G39	-7454	465
722	G37	-7480	355
723	G35	-7506	465
724	G33	-7532	355
725	G31	-7558	465
726	DUMMY25	-7584	355
727	DUMMY26	-7610	465
728	DUMMY27	-7917	484
729	DUMMY28	-7902	210
730	DUMMY29	-7792	184
731	G29	-7902	158
732	G27	-7792	132
733	G25	-7902	106
734	G23	-7792	80
735	G21	-7902	54
736	G19	-7792	28
737	G17	-7902	2
738	G15	-7792	-24
739	G13	-7902	-50
740	G11	-7792	-76
741	G9	-7902	-102
742	G7	-7792	-128
743	G5	-7902	-154
744	G3	-7792	-180
745	G1	-7902	-206
746	DUMMY30	-7792	-232
747	DUMMY31	-7902	-258

Alignment mark	X	Y
1-A	-7890	-452.5
1-B	7890	-452.5
2-A	7900	395.5
2-B	-7900	395.5
3-A	7844	482.5
3-B	-7844	482.5

BUMP Arrangement

S1 ~ S384	
I/O pins	

2. Interface

2.1. System Interface

The HX8310-A supports three system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, a 68-system 18-/16-/9-/8-bit bus interface and a serial data transfer bus interface. The interface mode is selected by the IM3-0 pins setting.
The HX8310-A includes an index register (IR), which is stored the index data of internal control register and RAM. There are two 18-bit bus control registers, which are used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the second read data operations is valid.

Table2. 1 Register Selection (18-/16-/9-/8- Bit System Interface)

80- / 68-system Bus

Operations	RS	80-system		68-system	
		NWR	NRD	E	RW
Writes Indexes into IR	0	0	1	1	0
Reads internal status	0	1	0	1	1
Writes data into control register or GRAM	1	0	1	1	0
Reads control register or GRAM data	1	1	0	1	1

Table2. 2 Register Selection (Serial Data Transfer Interface)

Start Bytes

Operations	RW	RS
Writes Indexes into IR	0	0
Reads internal status	1	0
Writes data into control register or GRAM	0	1
Reads data from control register or GRAM	1	1

2.1.1 80-/ 68-System Interface

18-bit bus Interface

The 80-system 18-bit parallel data transfer can be used by setting IM3-0 pins to “1010”. And the 68-system 18-bit parallel data transfer can be used by setting IM3-0 pins to “1000”. The Figure2.1 is the example of interface with i80/m68 microcomputer and the Figure2.2 is the data format of 18-bit system interface.

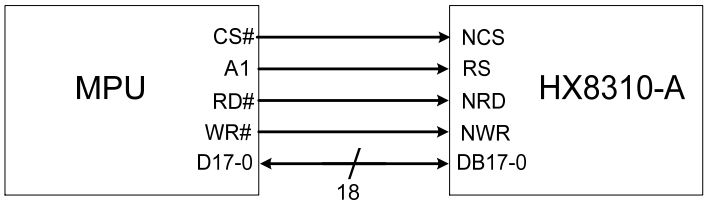


Figure2. 1 Example of 80- / 68- System 18-bit bus Interface

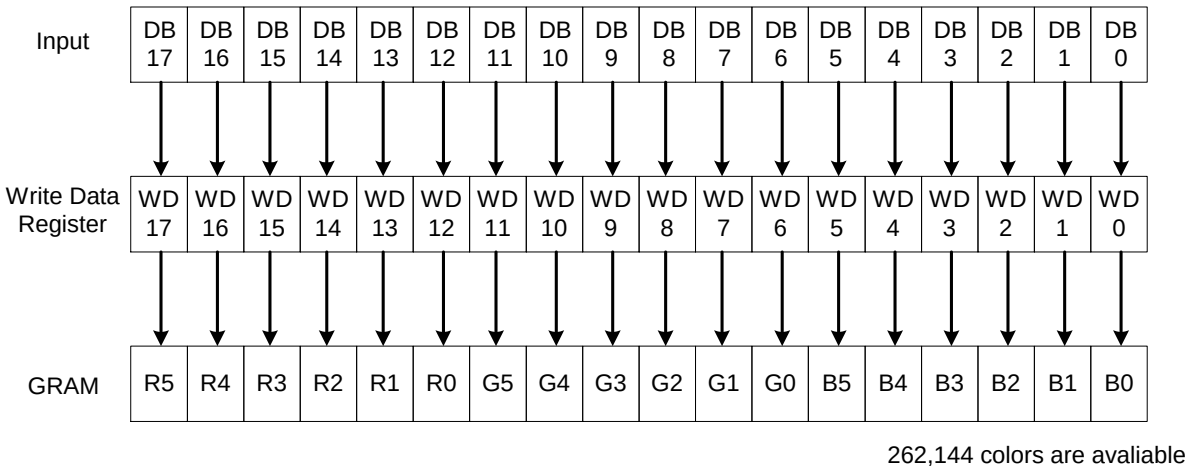


Figure2. 2 Data Format of 18-bit bus System Interface

16-bit bus Interface

The 80-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to “0010”. And the 68-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to “0000”. The data written to GRAM is expanded to 18-bit bus data automatically in the LSI. Unused pins(DB9, DB0) must be fixed to the VCC or VSSD level. The Figure2.3 is the example of interface with 16-bit i80/m68 microcomputer bus and the Figure2.4 is the data format of 16-bit bus system interface.

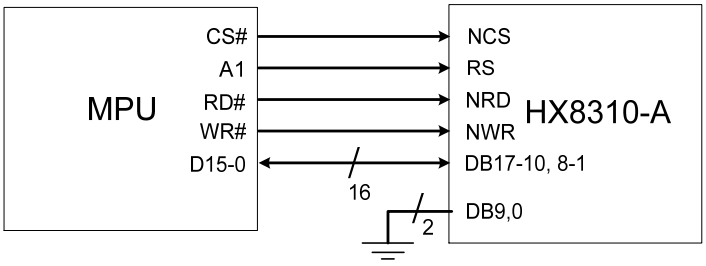


Figure2. 3 Example of 80- / 68- System 16-bit bus Interface

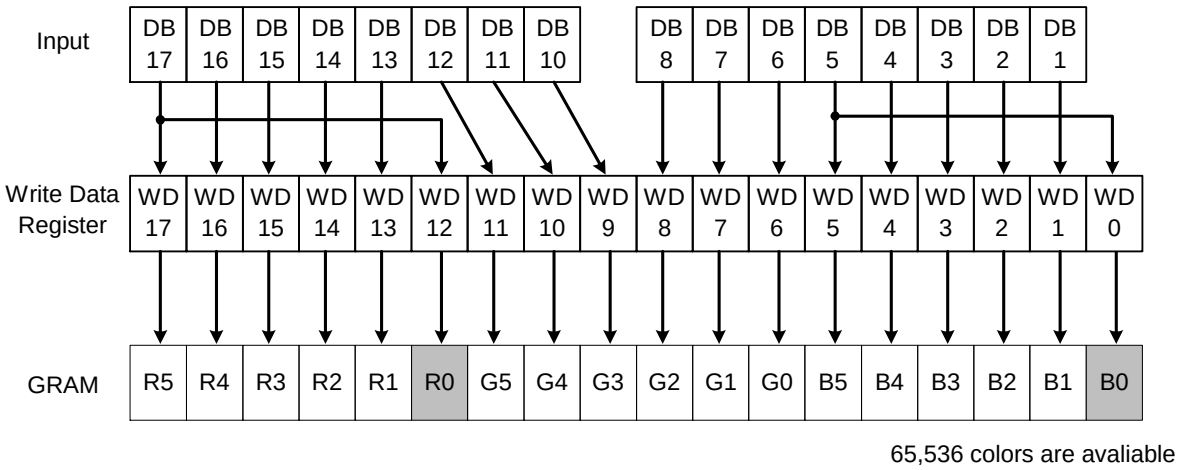


Figure2. 4 Data Format of 16-bit bus System Interface

9-bit bus Interface

The 80-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to “1011”. And the 68-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to “1001”. In 80-/68- system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and the 18-bit GRAM write data are divided into lower and upper bits , and then the upper bits are transferred first. Unused pins(DB8-0) must be fixed to the VCC or VSSD level. Ensure that upper bytes have to be written when writing the index register.

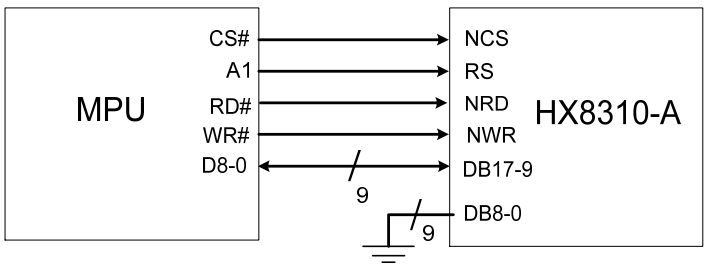


Figure2. 5 Example of 80- / 68- System 9-bit bus Interface

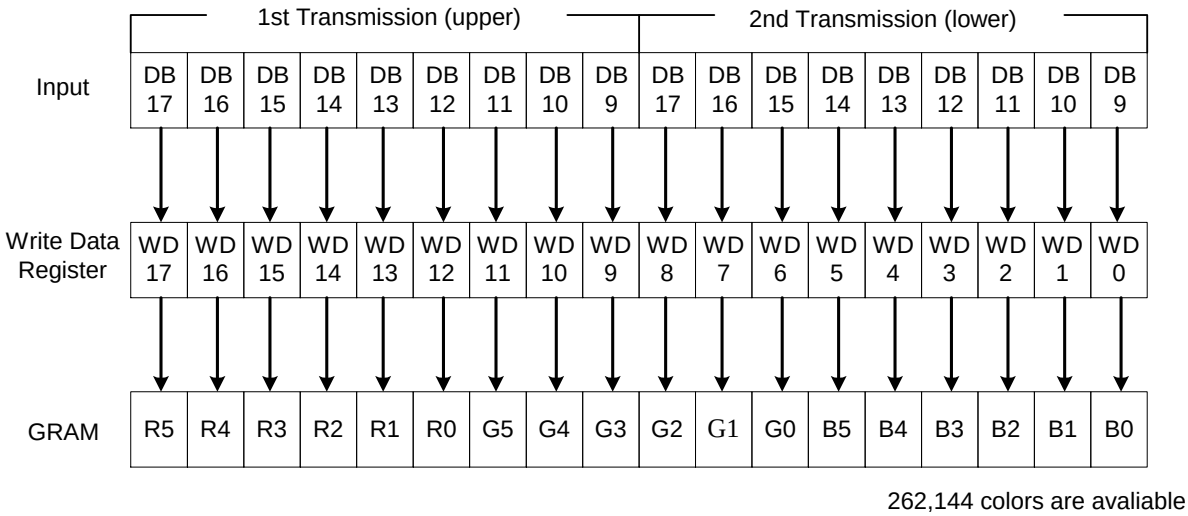


Figure2. 6 Data Format of 9-bit bus System Interface

8-bit bus Interface

The 80-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0011”. And the 68-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0001”. In 80-/68- system 8-bit bus parallel data transfer mode, the 16-bit bus instruction and the 18-bit GRAM write data are divided into lower and upper bits , and then the upper bits are transferred first.

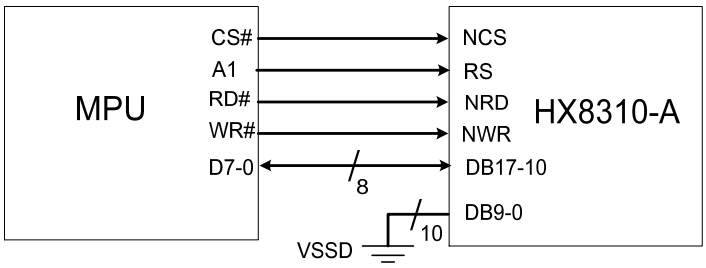


Figure2. 7 Example of 80- / 68- System 8-bit bus Interface

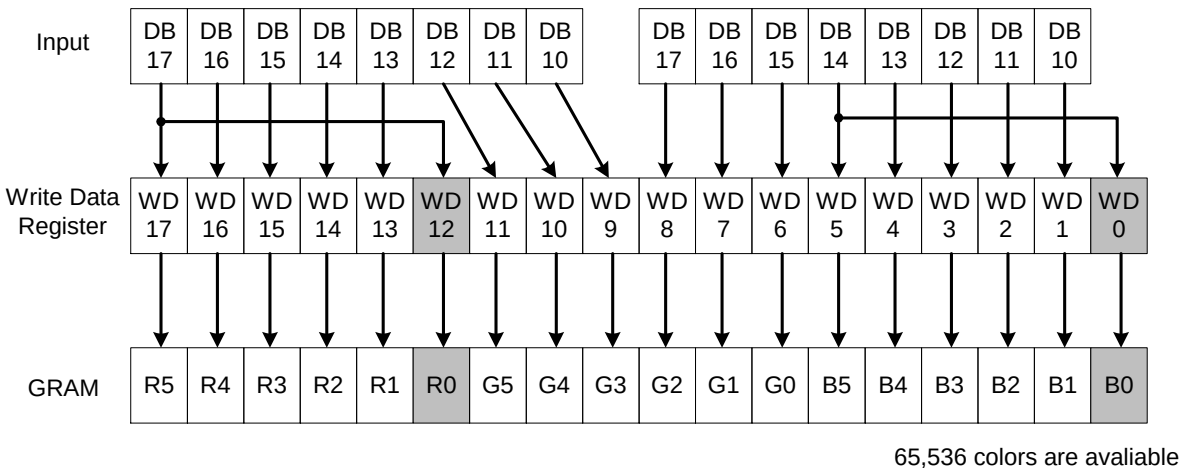


Figure2. 8 Data Format of 8-bit bus System Interface

2.1.2 Serial Data Transfer Interface

The HX8310-A supports the serial data transfer interface by setting IM3-1 pins to “010”. The serial data transfer interface mode is enabled through the chip select line (NCS), and accessed via a three-wire control consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock line (SCL). When HX8310-A is set up for serial data transfer interface mode, the IM0(ID) pin is used as an ID pin and then the DB17-0 pins, which are not used, must be fixed at VCC or VSSD.

In serial data transfer interface mode, the HX8310-A can transfer initially with the start byte at the falling edge of NCS input and finish the transfer at the rising edge of a NCS input.

When the chip select line (NCS) of HX8310-A set active low, the start byte will be transferred first. The start byte is make up of 6-bit bus device identification code, register select (RS) bit and read/write operation (RW) bit. The five upper bits of the 6-bit bus device identification code must be set 01110 and the least significant bit of the identification code can be determined by the IM0/ID pin. The register select bit (RS) is the seventh bit of the start byte. The cases of write data to the index register or read the status must be setting RS = 0, and the cases of write or read an instruction or GRAM data must be setting RS = 1. The read or write function is selected according to the eighth bit of the start byte (RW bit). The data is received when RW = 0, and is transmitted when RW = 1. Table2.3 list different conditions when change the RS and RW bit.

When the serial data transfer interface is enabled, the HX8310-A starts taking in start byte and subsequent data that is transferred with the MSB first. Further, The registers of 16-bit bus format can be divide to the upper eight bits as the first byte and lower eight bits as the second byte. The HX8310-A executed the write data operation to the GRAM after two-byte and then automatically expanded to the 18-bit bus format (Figure2.9). When the read status/register operation are executed, the prior byte after start byte is invalid, and then the HX8310-A starts to read correct status/register data from second byte. As well as, when the read GRAM data operation, the prior five bytes of GRAM read data after the start byte are invalid. The HX8310-A starts to read correct GRAM data from the sixth byte.

Table2. 3 The Function of RS and RW Bit

RS	RW	Function
0	0	Index register set
0	1	Status read
1	0	Register or GRAM data write
1	1	Register or GRAM data read

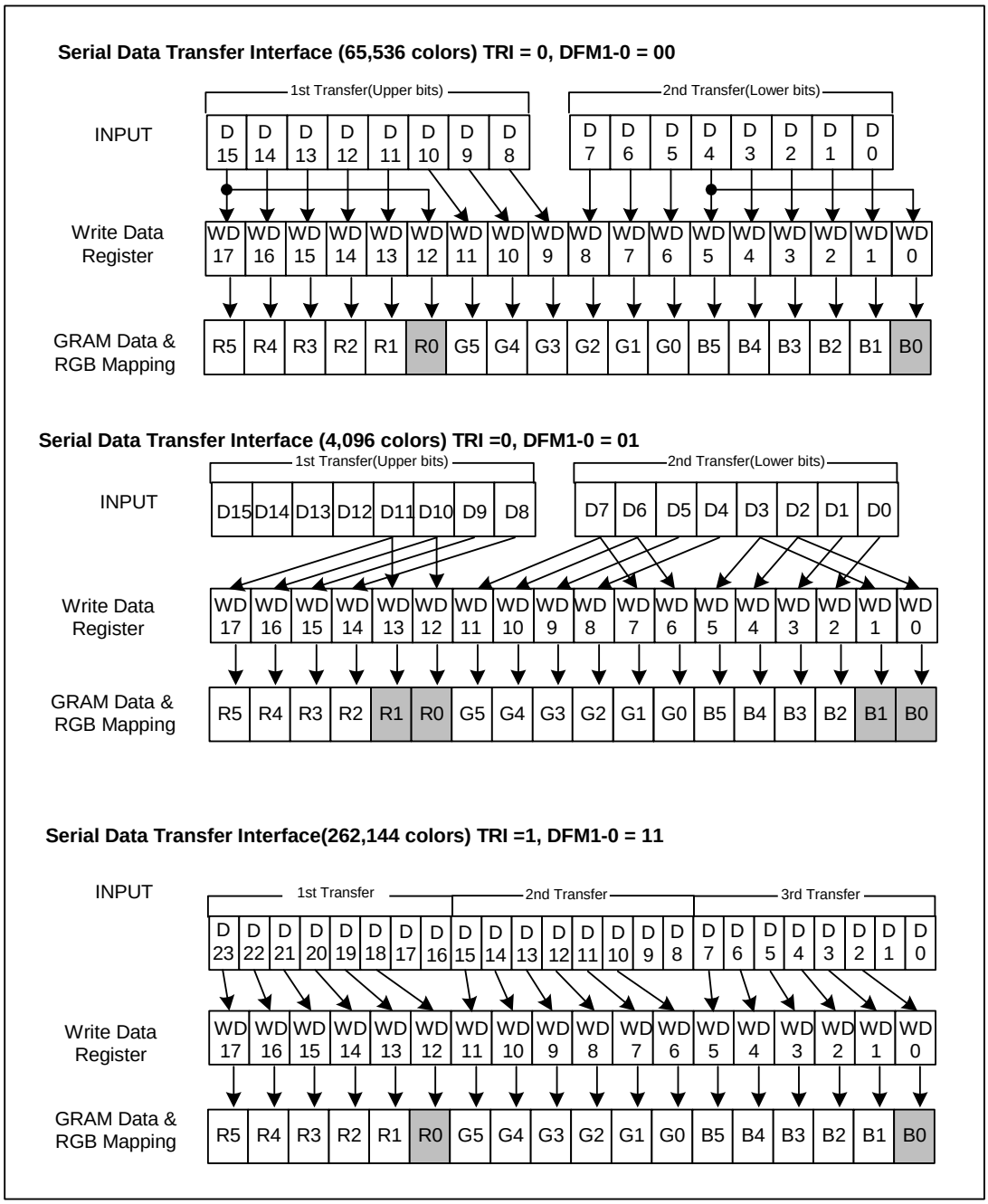


Figure2. 9 Data Format of Serial Data Transfer Interface GRAM

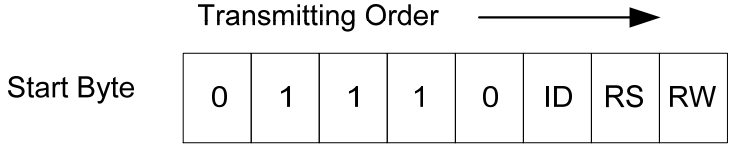
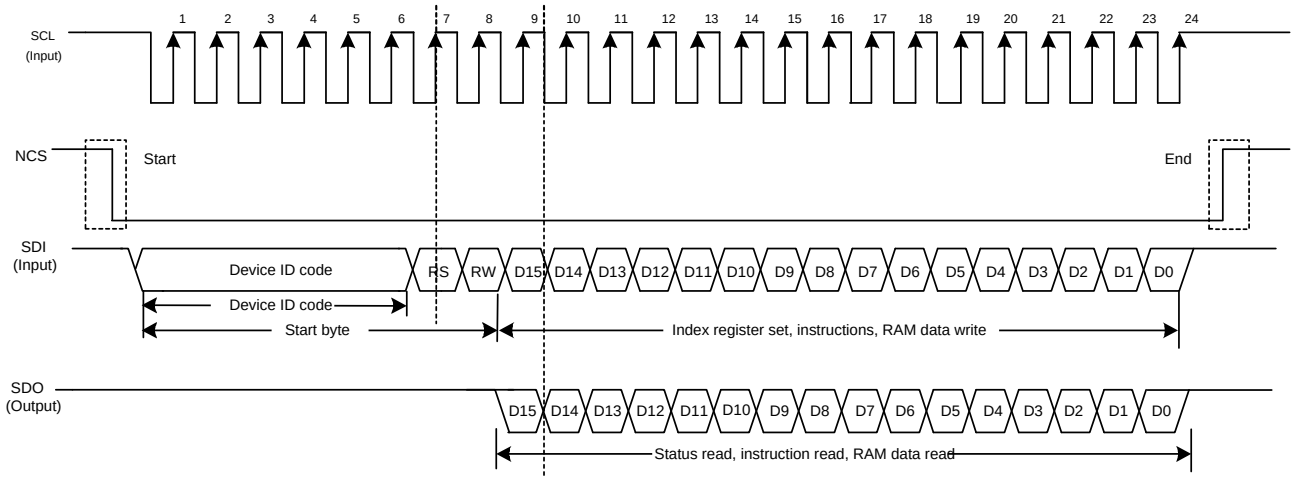
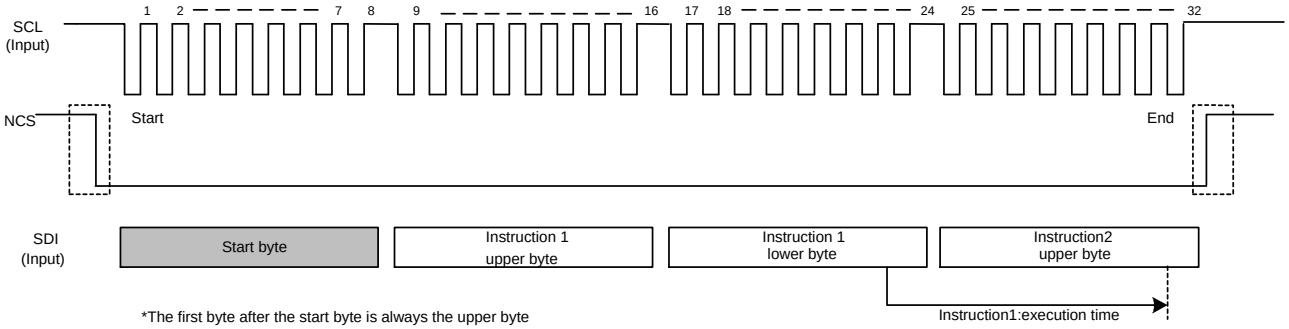


Figure2. 10 Start Byte Format of Serial Interface

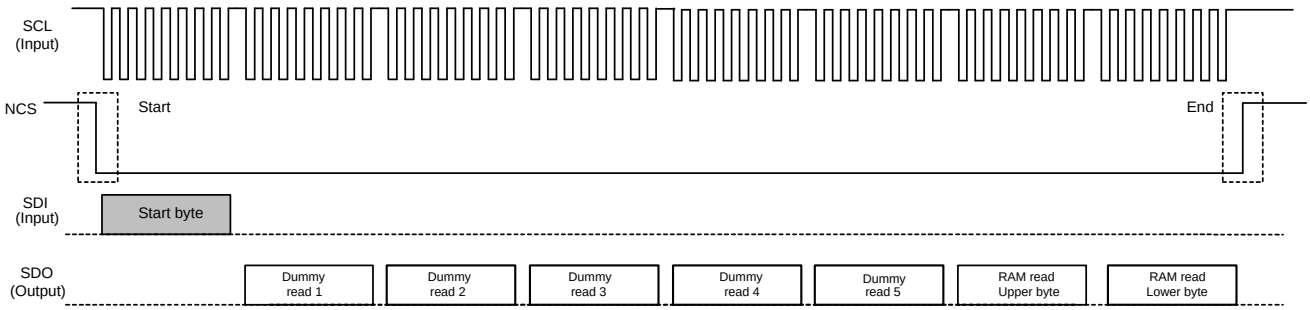
A)Basic Timing Transfer Format through Clock-Synchronized Serial Data Transfer Interface



B)Timing of Consecutive Data-write through Clock-synchronized Serial Data Transfer Interface

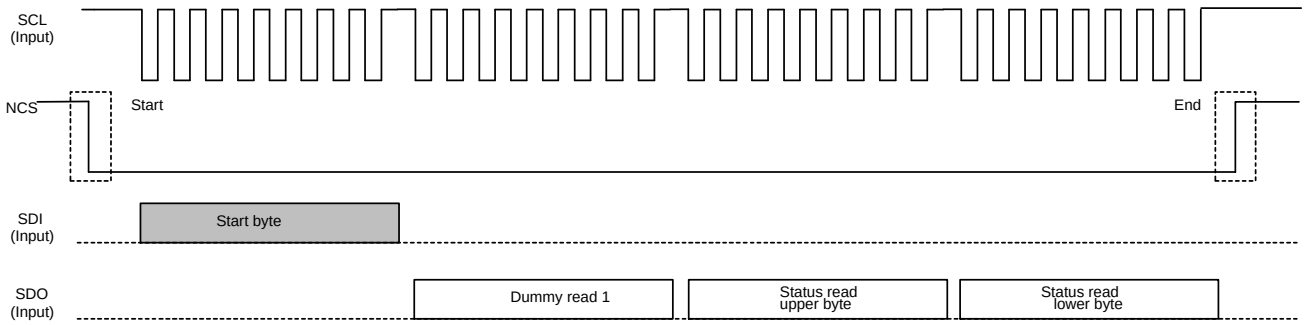


C) Timing Format of GRAM-Data Read



Note: A RAM data read operation follows 5-byte dummy read operations.

D) Timing Format of Status Read/ Instruction Read



Note: One byte of the read data after the start byte are invalid. The HX8310 starts to read the correct status or instruction data from the second byte

Figure2. 11 Data transfer through Serial Data Transfer Interface

2.2 VSYNC Interface

The HX8310-A supports the VSYNC interface mode that executed the display operation by the internal clocks generated from internal oscillators and synchronized with the frame synchronization signal VSYNC. When the VSYNC interface mode is selected, the interface display a moving picture through system interface with minimum modification that re-write display data to the internal GRAM in a high speed RAM function. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

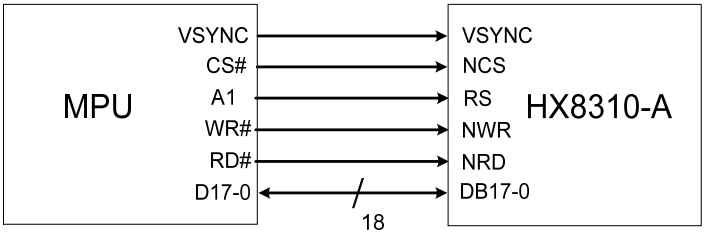


Figure2. 12 VSYNC Interface to MPU

When the HX8310-A is set up in VSYNC interface mode, the interface is used high speed write function (HWM=1) to display a moving picture when writing data to GRAM in high speed with low power consumption. Therefore, the VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It require GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP,BP and display lines duration(NL):

$$Internal\ ocillator\ clock\ (f_{osc})[Hz] = Frame\ Frequency \times [Display\ Lines(NL) + FP + BP] \times Clock\ Cycle\ Per\ Line(RTN) \times frequency\ \ fluctuation$$

The parameter of frequency fluctuation is ascribe to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

The minimum speed for RAM can be computed by the following formula:

$$Min\ RAM\ Write\ Speed\ [Hz] \geqq \frac{128 \times DisplayLines(NL) \times f_{osc}}{[BackPorch(BP) + DisplyLines(NL) - MARGIN\ lines] \times ClockCyclePerLine(RTN)}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the HX8310-A start the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting a internal oscillator clock (fosc) first.
An example of internal ocillator clock (fosc) and minimum speed for RAM writing set up in VSYNC interface mode is as follows.

Example
Display size: 128RGB*160 lines
Lines of be used: 160 lines (10011)
FP: 2 lines (0010)
BP:14 lines (1110)

Frequency fluctuation: 5%
Frame frequency: 60Hz

Internal oscillator clock (fosc) [Hz] = 60 × [160 + 2 +14] × 16 × (1.05/0.95) ≒ 187kHz

The Min. RAM Write Speed [Hz] ≧ 128 × 160 × 187k /{ [14 + 160-2] × 16} ≒ 1.39MHz

In this example, the minimum RAM write speed of VSYNC interface is 1.39MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the HX8310-A initiate the display operation and make it possible to re-write the display area set previously. Further, If the display area is different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.

When the HX8310-A make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 2.12 illustrates the process of VSNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.

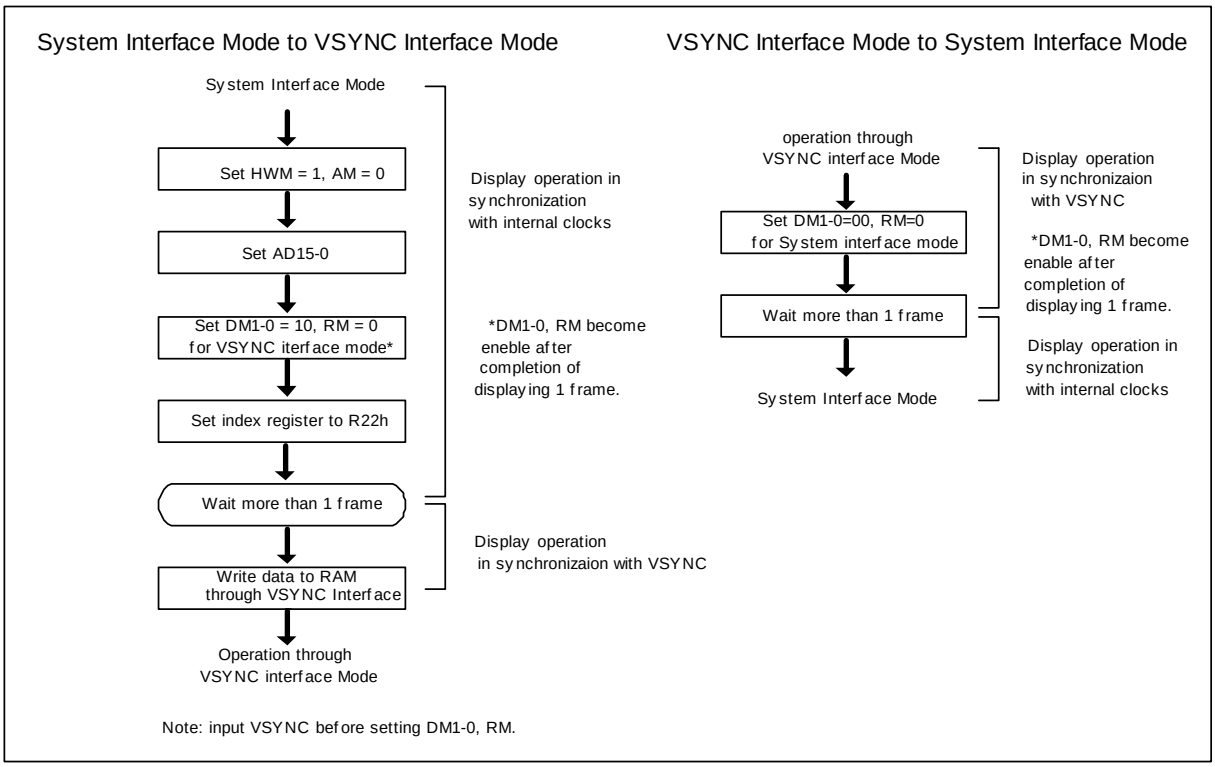


Figure2. 13 VSYNC interface with internal clock and system interface with internal clock mode transition

When HX8310-A is set up on VSYNC interface mode, use the high-speed RAM write mode (HWM=1) to access RAM in high speed with low power consumption when display a moving picture. But the partial display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

2.3 RGB Interface

The HX8310-A supports the RGB interface that display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE) be described on Table 2.5. The RGB interface can be used by setting DM1-0=01 and RM=1. In RGB interface mode, with use of high-speed RAM write mode (HWM=1) and a window address function , enables to display data in a moving picture area and makes it possible to transfer the display only by re-writing a screen with minimum data transfers.

Table2. 4 RIM Bit Set

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit bus RGB interface	PD17-0
0	1	16-bit bus RGB interface	PD17-13, 11-1
1	0	6-bit bus RGB interface	PD17-12
1	1	Ignore	

Table2. 5 EPL and ENABLE Set

EPL	ENABLE	RAM Write	RAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

When the HX8310-A set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continues until the next input of the VSYNC signal.

The HX8310-A supports two types of RGB interface mode, the difference between them is the RAM access using the RGB interface (PD17-0) or system interface (DB17-0). The data be written to the internal GRAM synchronized with DOTCLK inputs when ENABLE is setting low. Contrary to set ENABLE high, the data write to the GRRAM would be used the system interface. Further, when selected to use system interface, set ENABLE high to stop using the RGB interface for writing data, and then set the RAM access setting bit bus (RM) low to invert RAM access operation by using system interface. After that, set address AD15-0 on falling edges of VSYNC and then set the index field of register (R22h) to access RAM via the system interface. The HX8310-A allows rewriting data in the still picture area by using the system interface when displaying a moving picture in RGB interface mode. When return to use RGB interface to access RAM, set address AD 15-0, RAM access setting bit bus (RM=1) and the index field of register (R22h) before accessing RAM via RGB interface.

The Figure2.13 are shown the procedure of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

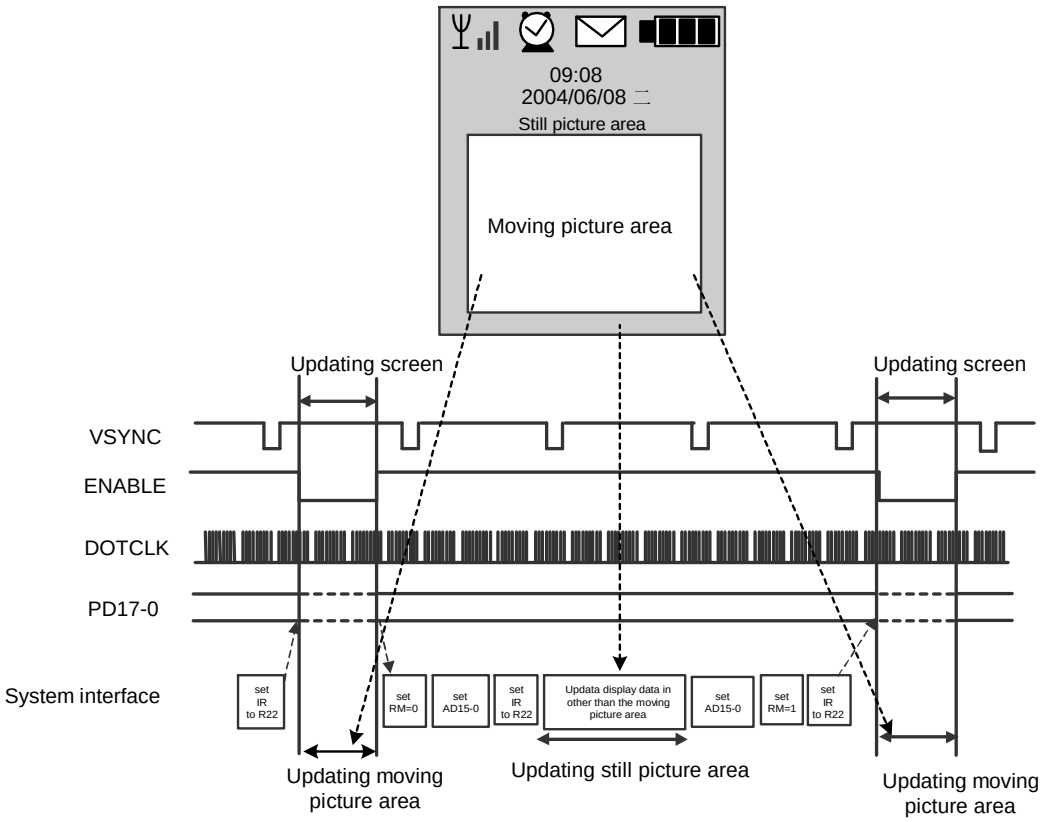


Figure2. 14 Example of update the still and moving picture

When set up in RGB interface mode, the used of high–speed RAM write mode to write data to the internal GRAM and GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal. It is the same with VSYNC interface mode, partial screen display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

When the HX8310-A make the transition with system interface mode and RGB interface mode, the sequence of switching process must be follow as Figure2.14.

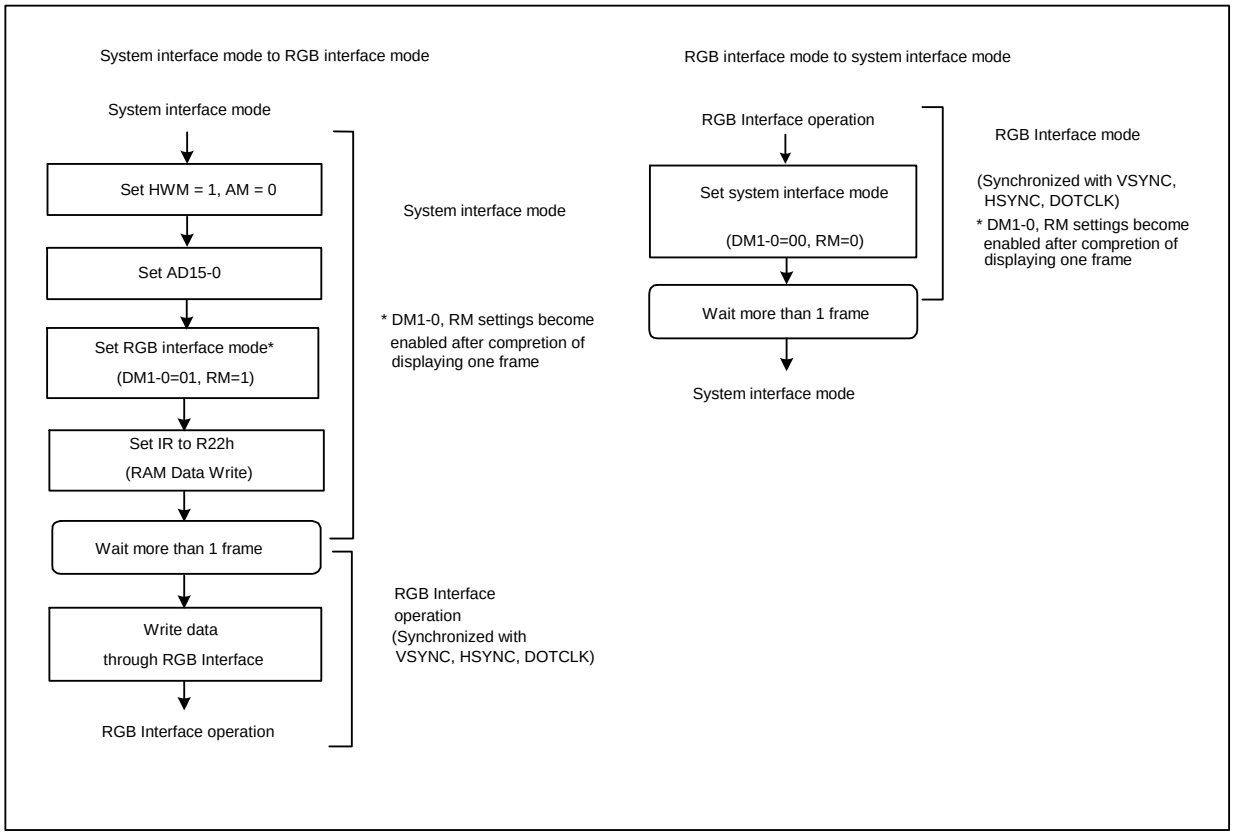


Figure2. 15 Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure2.15.

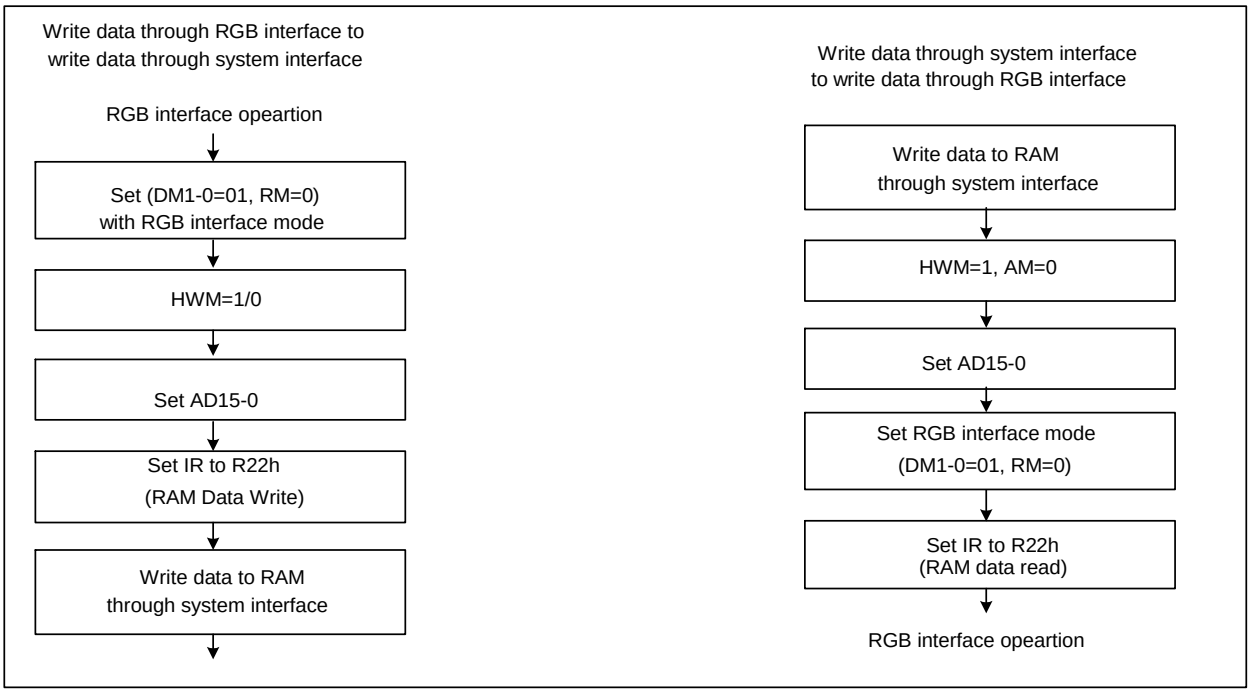


Figure2. 16 RAM data write sequence through System Interface or RGB Interface during RGB Interface Mode

The HX8310-A supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

18-bit bus RGB interface

The 18-bit interface can be used by setting RIM1-0 bits to “00”. The Figure 2.16 is the example of 18-bit RGB interface with LCD Controller and HX8310-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE). The Figure2.17 is the data format of 18-bit RGB interface.

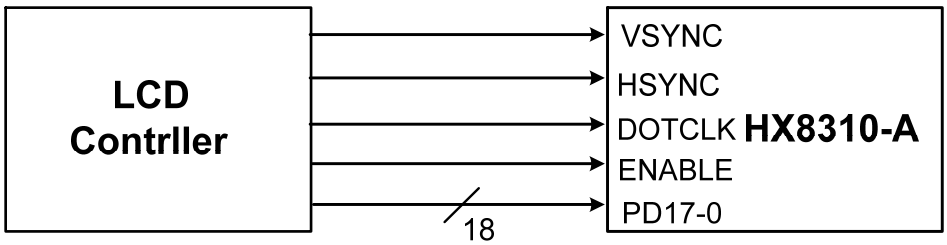


Figure2. 17 18-bit RGB interface

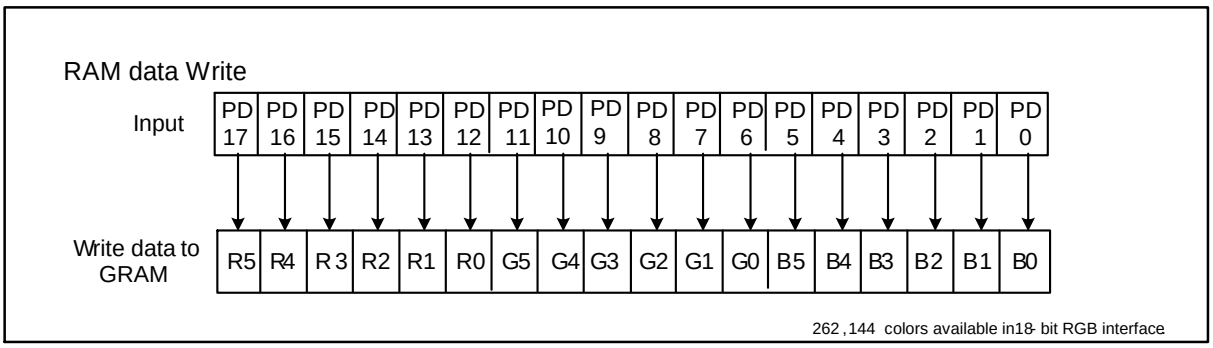


Figure2. 18 Data format for 18-bit interface

16-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “01”. The Fig 2.18 is the example of 16-bit bus RGB interface with LCD Controller and HX8310-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-13, PD11-1 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins(PD9, PD0) must be fixed to the VCC or VSSD level. The Figure2.19 is the data format of 16-bit RGB interface.

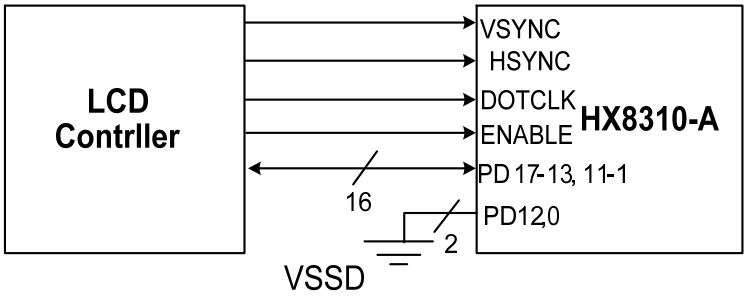


Figure2. 19 16-bit RGB interface

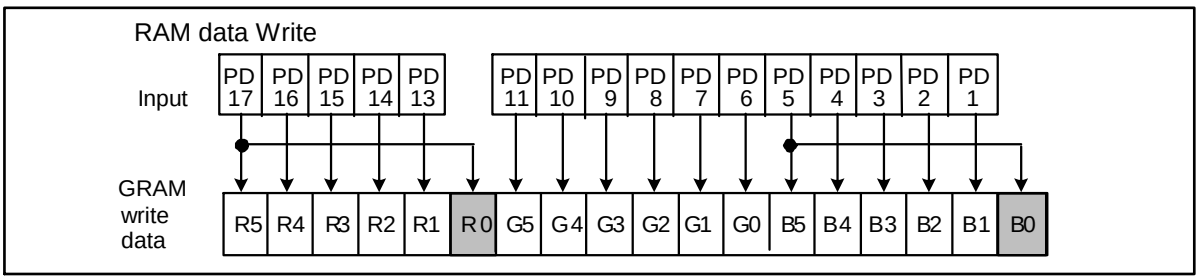


Figure2. 20 Data format for16-bit interface

6-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “10”. The Figure2.20 is the example of 16-bit bus RGB interface with LCD Controller and HX8310-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-12 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins(PD11-0) must be fixed to the VCC or VSSD level. The Figure2.21 is the data format of 16-bit bus RGB interface.

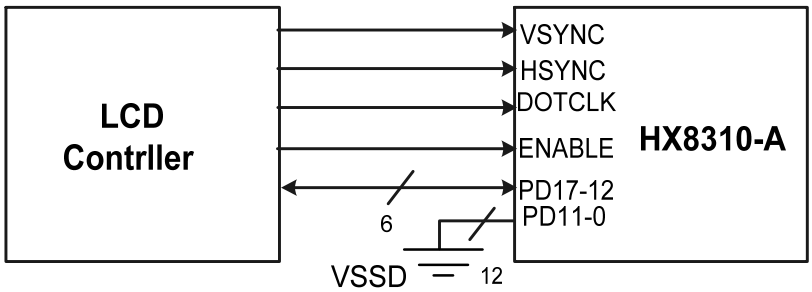
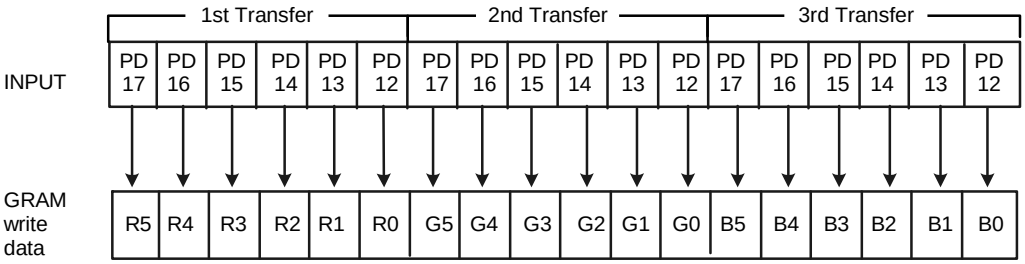


Figure2. 21 6-bit RGB interface

RAM data write



262,144 colors are available in 6-bit system interface.

Figure2. 22 Data format for 6-bit interface

The Figure 2.22 and Figure 2.23 is the timing relationship of system interface and RGB interface.

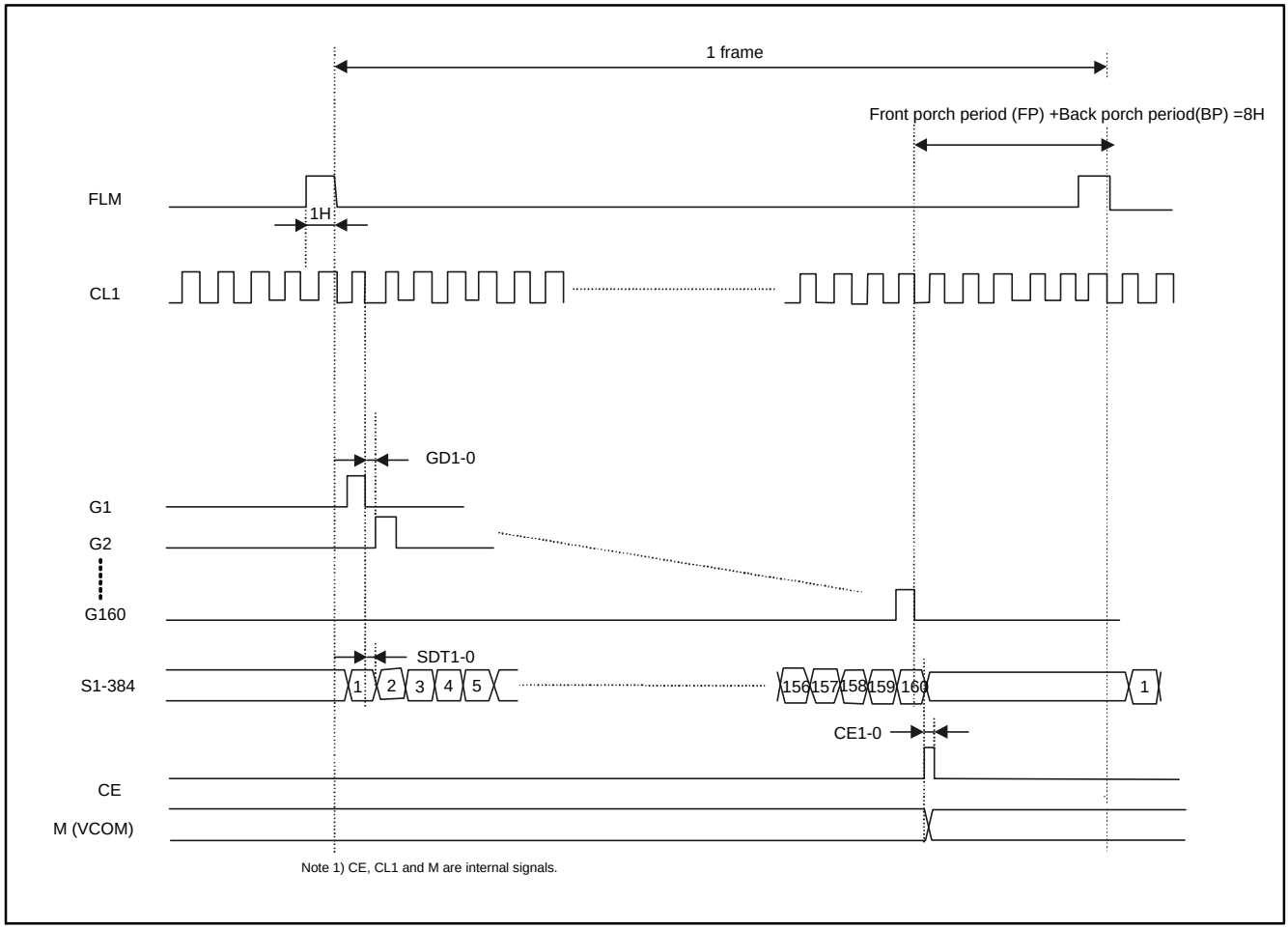


Figure2. 23 Timing Relationship of System Interface Mode

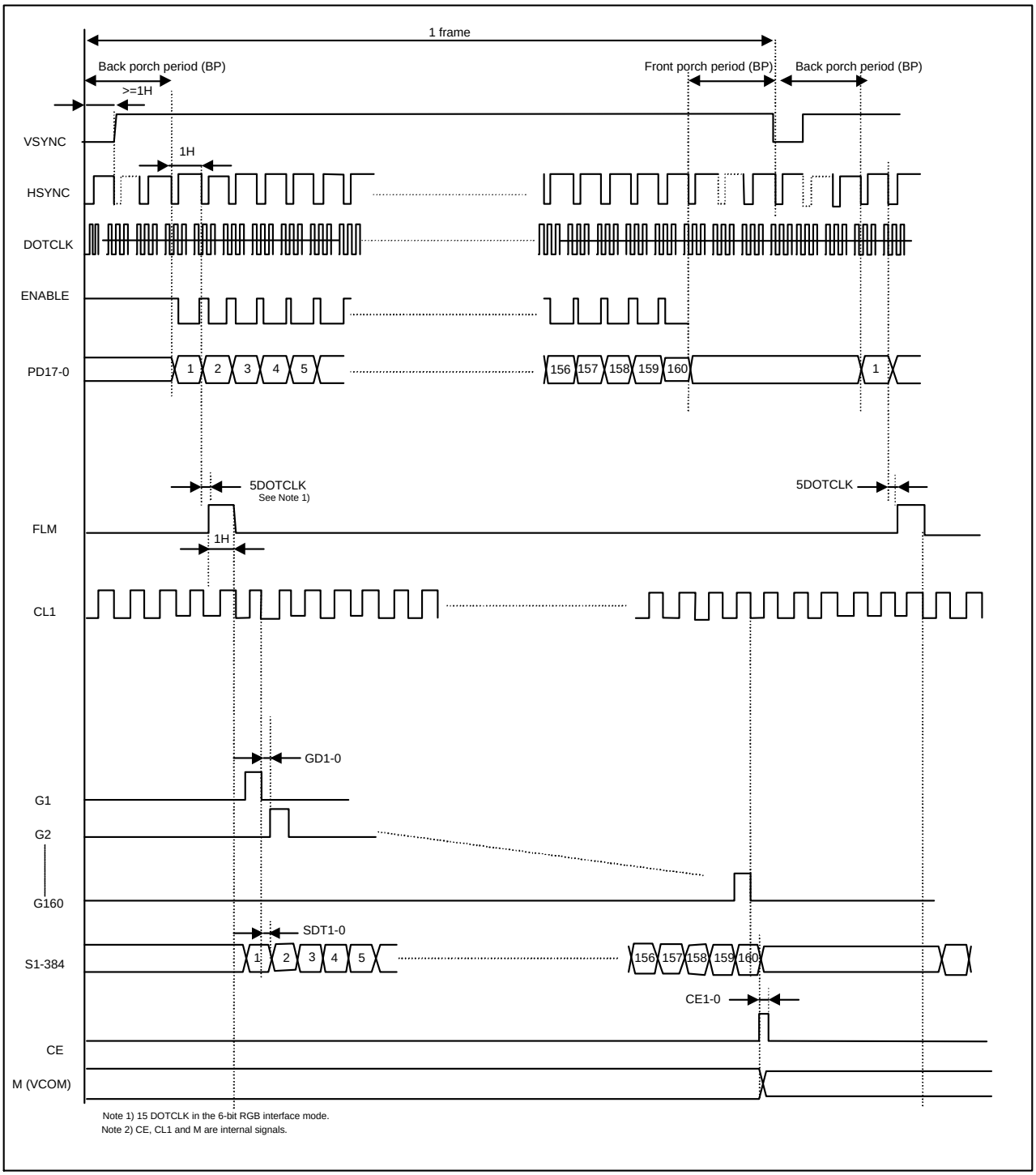


Figure2. 24 Timing Relationship of RGB Interface Mode

3. Function Description

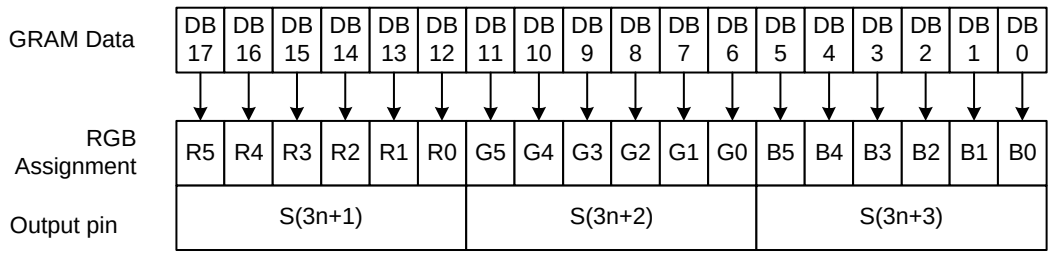
3.1 Graphics RAM

The HX8310-A have an internal graphics RAM that stores 46,080 bytes bit-pattern data, where one pixel is expressed by 18 bits. The GRAM address map is listed as follow:

Table3. 1 GRAM address and display panel position (SS =”0”)

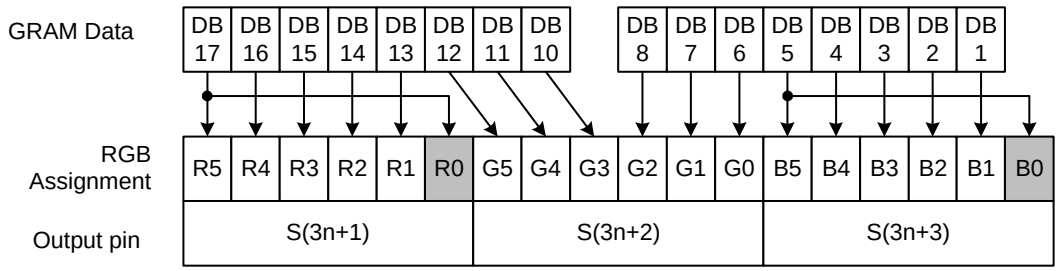
S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S373	S374	S375	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=1	GS=0	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G160	G1	0000H			0001H			0002H			---	007CH			007DH			007EH			007FH		
G159	G2	0100H			0101H			0102H			---	017CH			017DH			017EH			017FH		
G158	G3	0200H			0201H			0202H			---	027CH			027DH			027EH			027FH		
G157	G4	0300H			0301H			0302H			---	037CH			037DH			037EH			037FH		
G156	G5	0400H			0401H			0402H			---	047CH			047DH			047EH			047FH		
G155	G6	0500H			0501H			0502H			---	057CH			057DH			057EH			057FH		
G154	G7	0600H			0601H			0602H			---	067CH			067DH			067EH			067FH		
G153	G8	0700H			0701H			0702H			---	077CH			077DH			077EH			077FH		
G152	G9	0800H			0801H			0802H			---	087CH			087DH			087EH			087FH		
G151	G10	0900H			0901H			0902H			---	097CH			097DH			097EH			097FH		
G150	G11	0A00H			0A01H			0A02H			---	0A7CH			0A7DH			0A7EH			0A7FH		
G149	G12	0B00H			0B01H			0B02H			---	0B7CH			0B7DH			0B7EH			0B7FH		
G148	G13	0C00H			0C01H			0C02H			---	0C7CH			0C7DH			0C7EH			0C7FH		
G147	G14	0D00H			0D01H			0D01H			---	0D7CH			0D7DH			0D7EH			0D7FH		
G146	G15	0E00H			0E01H			0E01H			---	0E7CH			0E7DH			0E7EH			0E7FH		
⋮	⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	G151	9600H			9601H			9602H			---	967CH			967DH			967EH			967FH		
G9	G152	9700H			9701H			9702H			---	977CH			977DH			977EH			977FH		
G8	G153	9800H			9801H			9802H			---	987CH			987DH			987EH			987FH		
G7	G154	9900H			9901H			9902H			---	997CH			997DH			997EH			997FH		
G6	G155	9A00H			9A01H			9A02H			---	9A7CH			9A7DH			9A7EH			9A7FH		
G5	G156	9B00H			9B01H			9B02H			---	9B7CH			9B7DH			9B7EH			9B7FH		
G4	G157	9C00H			9C01H			9C02H			---	9C7CH			9C7DH			9C7EH			9C7FH		
G3	G158	9D00H			9D01H			9D02H			---	9D7CH			9D7DH			9D7EH			9D7FH		
G2	G159	9E00H			9E01H			9E02H			---	9E7CH			9E7DH			9E7EH			9E7FH		
G1	G160	9F00H			9F01H			9F02H			---	9F7CH			9F7DH			9F7EH			9F7FH		

80-System/68-System 18-bit bus Interface



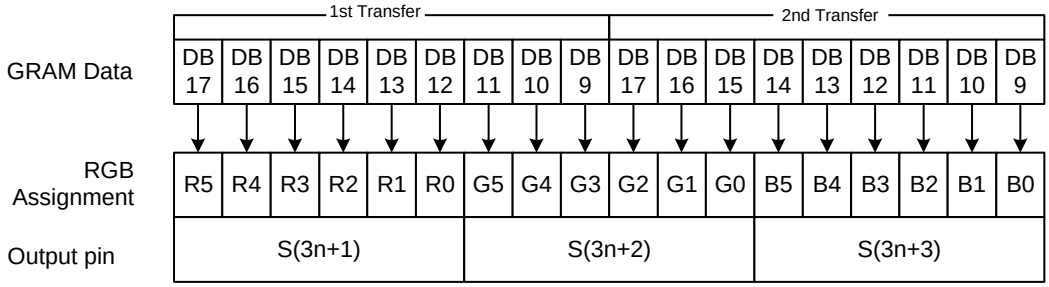
Note: n = lower eight bits of address (0 to 127)

80-System/68-System 16-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

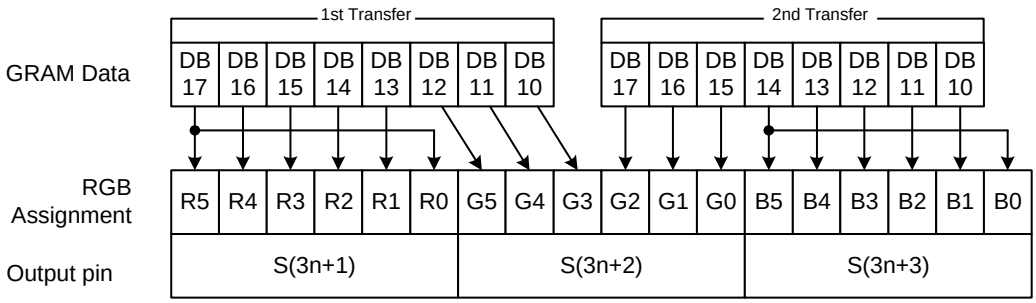
80-System/68-System 9-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

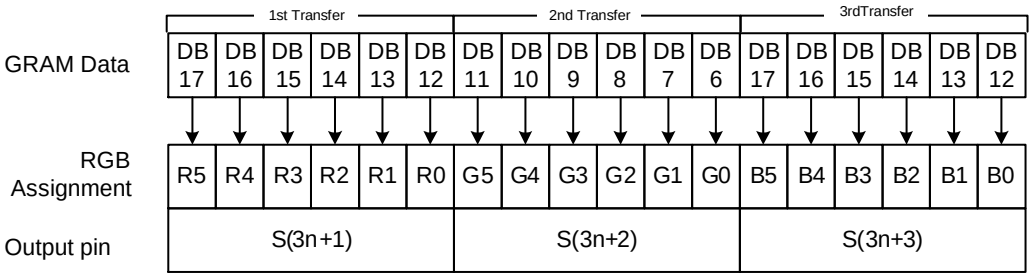
Figure3. 1 GRAM data and display data of 18-/16-9- bit system interface (SS = "0", BGR = "0")

80-System/68-System 8-bit bus Interface (2 transfers/pixel)



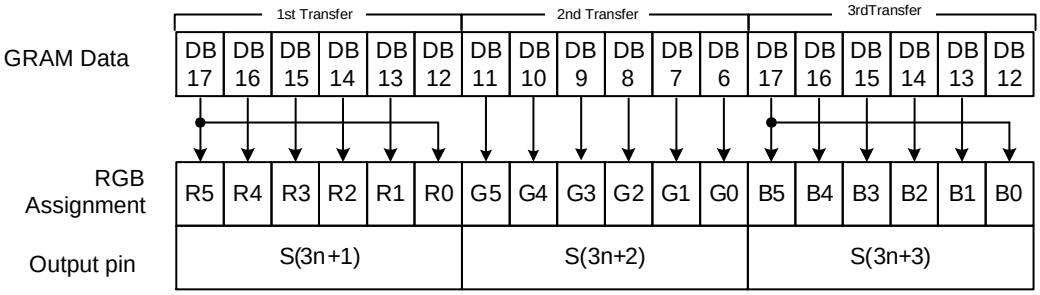
Note: n = lower eight bits of address (0 to 127)

80-System/68-System 8-bi t Interface (3 transfers, 262k colors: TRI=1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

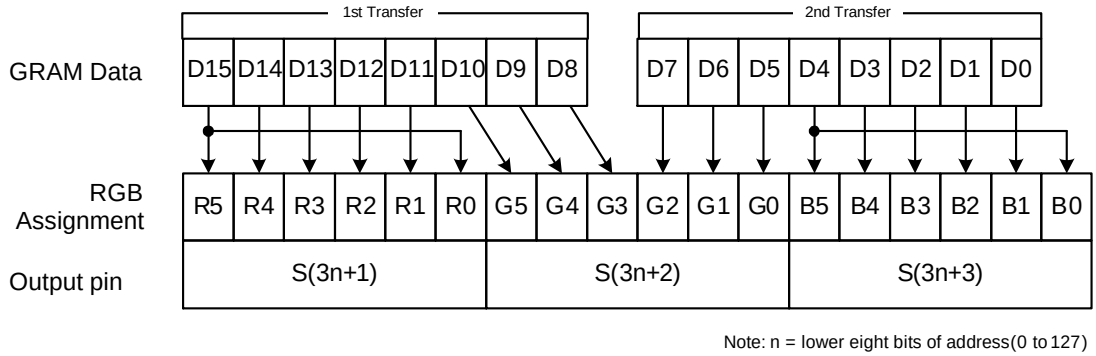
80-System/68-System 8-bi t Interface (3 transfers, 65k colors: TRI=1, DFM1-0=11)



Note: n = lower eight bits of address(0 to 127)

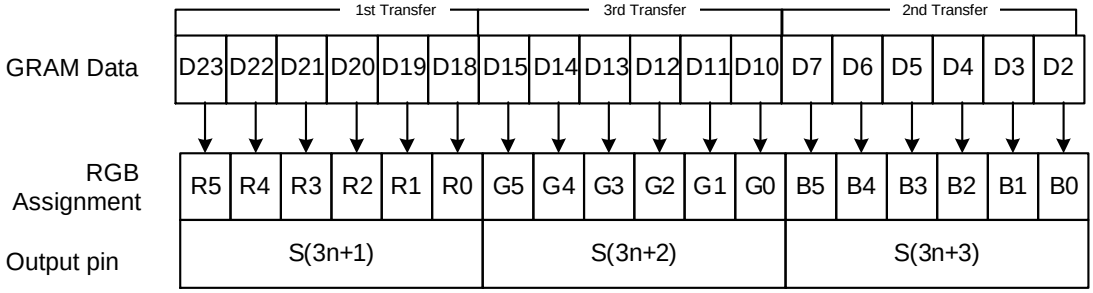
Figure3. 2 GRAM data and display data of 8-bit system interface (SS = “0”, BGR = “0”)

Serial Data Transfer Interface (2 transfers/65k colors: TRI = 0)



Note: n = lower eight bits of address(0 to 127)

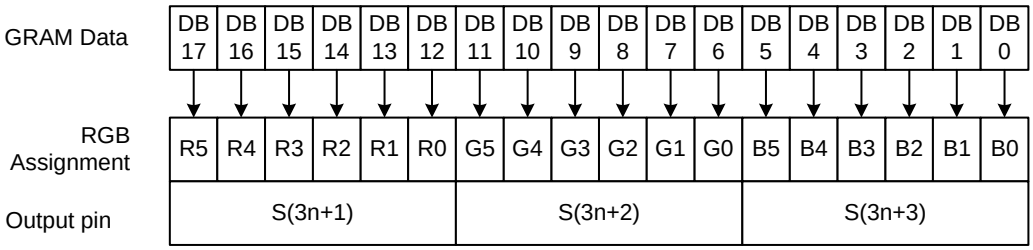
Serial Data Transfer Interface (3 transfers/262k colors: TRI = 1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

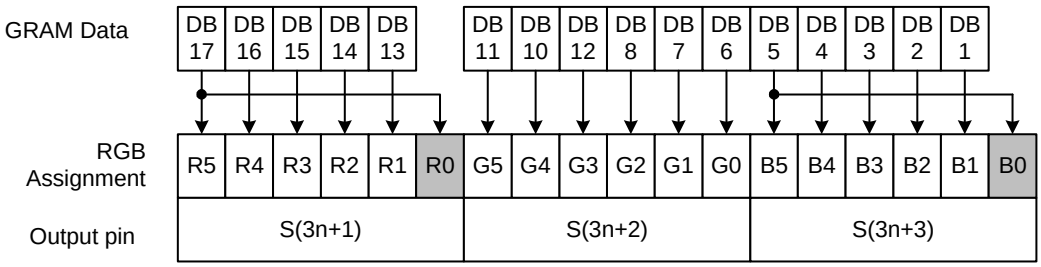
Figure3. 3 GRAM data and display data of Serial Data Transfer interface (SS = "0", BGR = "0")

18-Bit RGB Interface



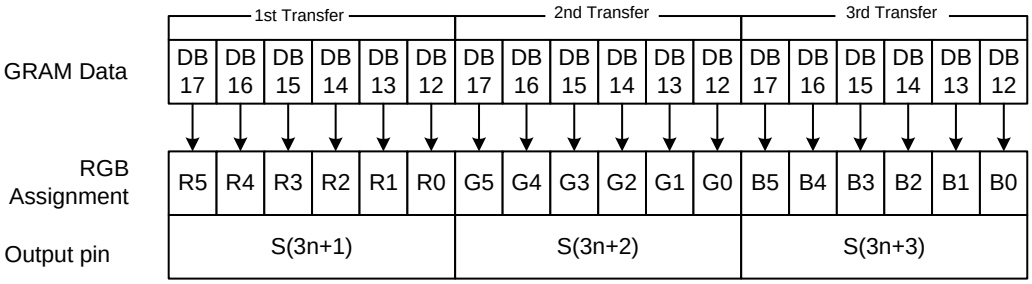
Note: n = lower eight bits of address (0 to 127)

16-Bit RGB Interface



Note: n = lower eight bits of address (0 to 127)

6-Bit RGB Interface



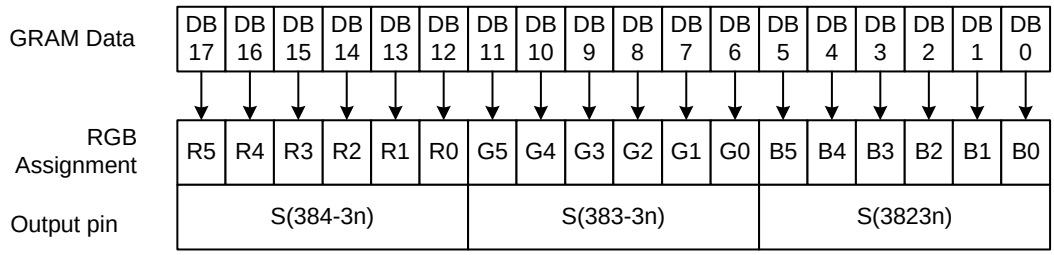
Note: n = lower eight bits of address (0 to 127)

Figure3. 4 GRAM data and display data: RGB interface (SS = "0", BGR = "0")

Table3. 2 GRAM address and display panel position (SS =”1”)

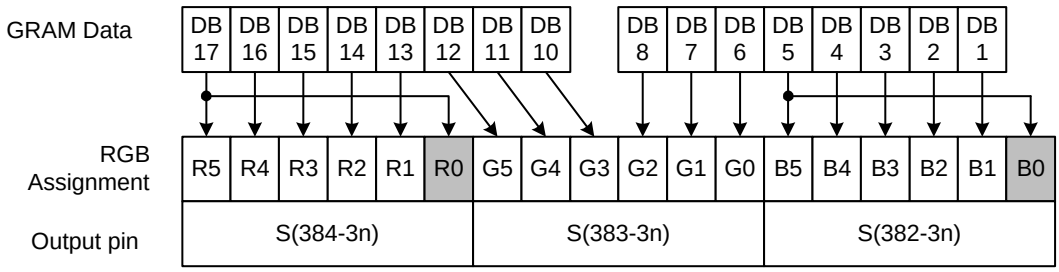
S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	---------	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=0	GS=1	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---------	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G1	G160	007FH			007EH			007DH			007CH			---------	0002H			0001H			0000H		
G2	G159	017FH			017EH			017DH			017CH			---------	0102H			0101H			0100H		
G3	G158	027FH			027EH			027DH			027CH			---------	0202H			0201H			0200H		
G4	G157	037FH			037EH			037DH			037CH			---------	0302H			0301H			0300H		
G5	G156	047FH			047EH			047DH			047CH			---------	0402H			0401H			0400H		
G6	G155	057FH			057EH			057DH			057CH			---------	0502H			0501H			0500H		
G7	G154	067FH			067EH			067DH			067CH			---------	0602H			0601H			0600H		
G8	G153	077FH			077EH			077DH			077CH			---------	0702H			0701H			0700H		
G9	G152	087FH			087EH			087DH			087CH			---------	0802H			0801H			0800H		
G10	G151	097FH			097EH			097DH			097CH			---------	0902H			0901H			0900H		
G11	G150	0A7FH			0A7EH			0A7DH			0A7CH			---------	0A02H			0A01H			0A00H		
G12	G149	0B7FH			0B7EH			0B7DH			0B7CH			---------	0B02H			0B01H			0B00H		
G13	G148	0C7FH			0C7EH			0C7DH			0C7CH			---------	0C02H			0C01H			0C00H		
G14	G147	0D7FH			0D7EH			0D7DH			0D7CH			---------	0D02H			0D01H			0D00H		
⋮	⋮	⋮			⋮			⋮			⋮			---------	⋮			⋮			⋮		
G149	G12	947FH			947EH			947DH			947CH			---------	9402H			9401H			9400H		
G150	G11	957FH			957EH			957DH			957CH			---------	9502H			9501H			9500H		
G151	G10	967FH			967EH			967DH			967CH			---------	9602H			9601H			9600H		
G152	G9	977FH			977EH			977DH			977CH			---------	9702H			9701H			9700H		
G153	G8	987FH			987EH			987DH			987CH			---------	9802H			9801H			9800H		
G154	G7	997FH			997EH			997DH			997CH			---------	9902H			9901H			9900H		
G155	G6	9A7FH			9A7EH			9A7DH			9A7CH			---------	9A02H			9A01H			9A00H		
G156	G5	9B7FH			9B7EH			9B7DH			9B7CH			---------	9B02H			9B01H			9B00H		
G157	G4	9C7FH			9C7EH			9C7DH			9C7CH			---------	9C02H			9C01H			9C00H		
G158	G3	9D7FH			9D7EH			9D7DH			9D7CH			---------	9D02H			9D01H			9D00H		
G159	G2	9E7FH			9E7EH			9E7DH			9E7CH			---------	9E02H			9E01H			9E00H		
G160	G1	9F7FH			9F7EH			9F7DH			9F7CH			---------	9F02H			9F01H			9F00H		

80-System 18-bit bus Interface



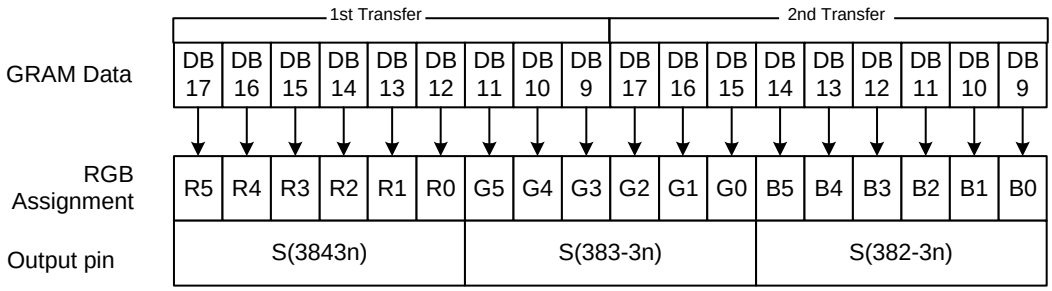
Note: n = lower eight bits of address (0 to 127)

80-System 16-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

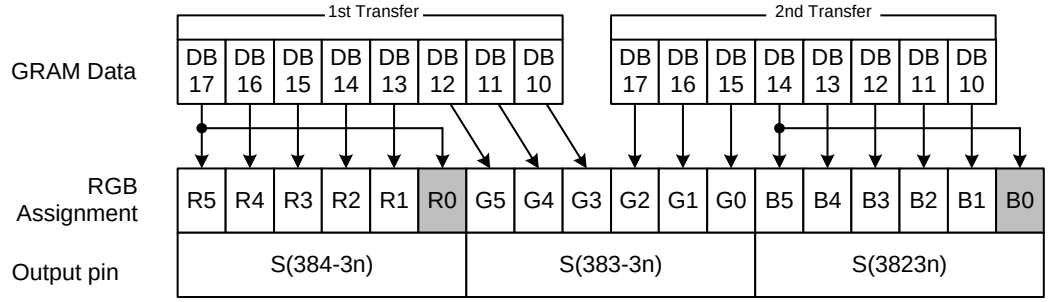
80-System 9-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

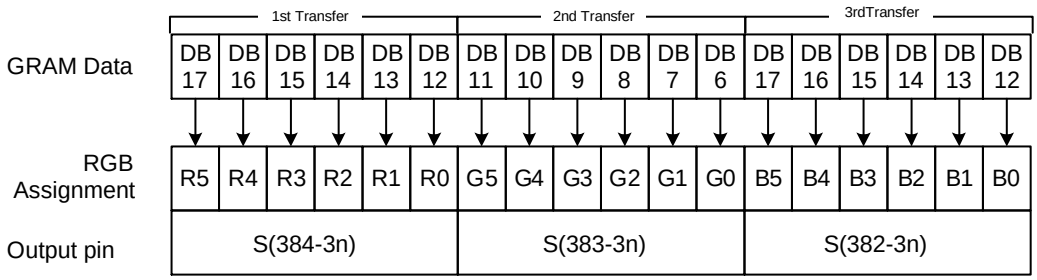
Figure3. 5 GRAM data and display data of 18-/16-/9- bit system interface (SS = "1", BGR = "1")

80-System 8-bit bus Interface/ Serial Data Transfer Interface (2 transfers/pixel)



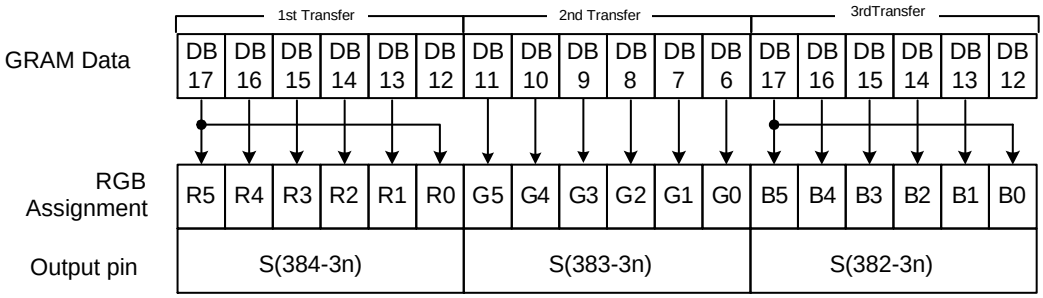
Note: n = lower eight bits of address (0 to 127)

80-System/68-System 8-bi t Interface (3 transfers, 262k colors: TRI=1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

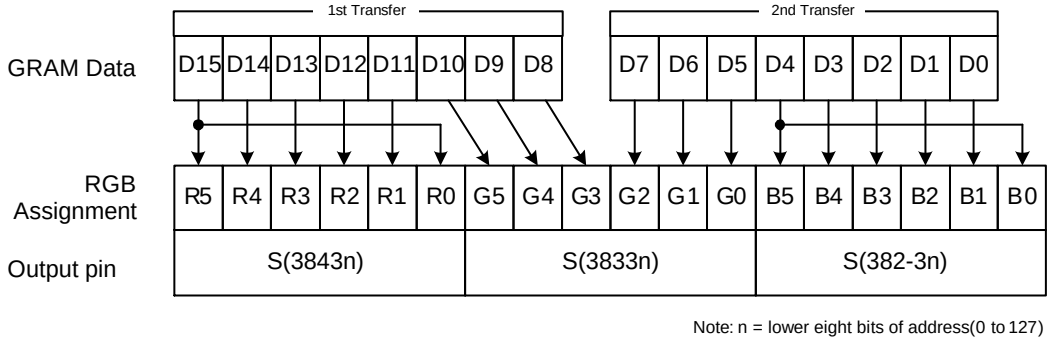
80-System/68-System 8-bi t Interface (3 transfers, 65k colors: TRI=1, DFM1-0=11)



Note: n = lower eight bits of address(0 to 127)

Figure3. 6 GRAM data and display data of 8-bit system interface (SS = "1", BGR = "1")

Serial Data Transfer Interface (2 transfers/65k colors: TRI = 0)



Serial Data Transfer Interface (3 transfers/262k colors: TRI = 1, DFM1-0=10)

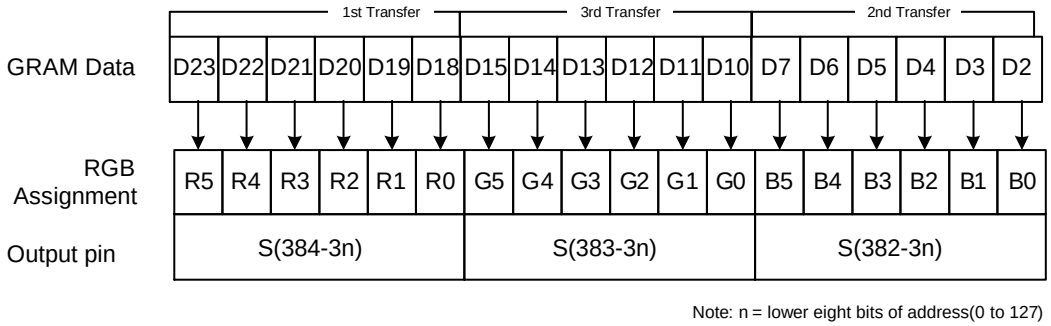
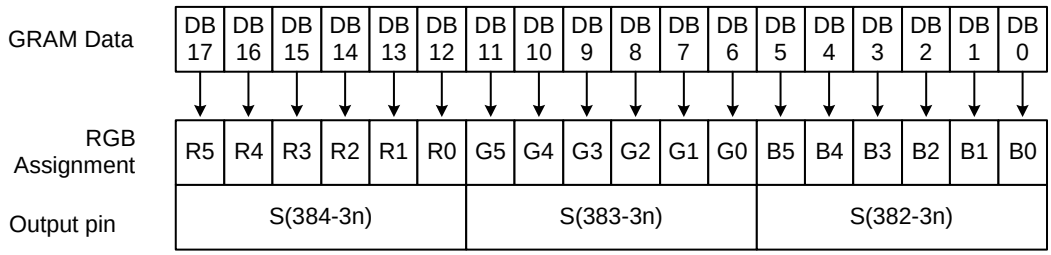


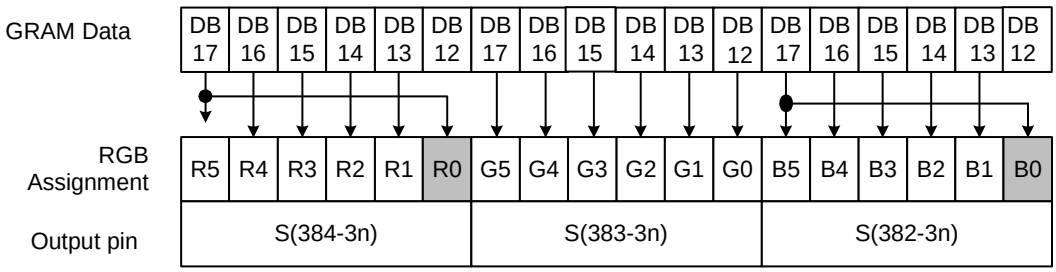
Figure3. 7 GRAM data and display data of Serial Data transfer interface (SS = "1", BGR = "1")

18-Bit Interface



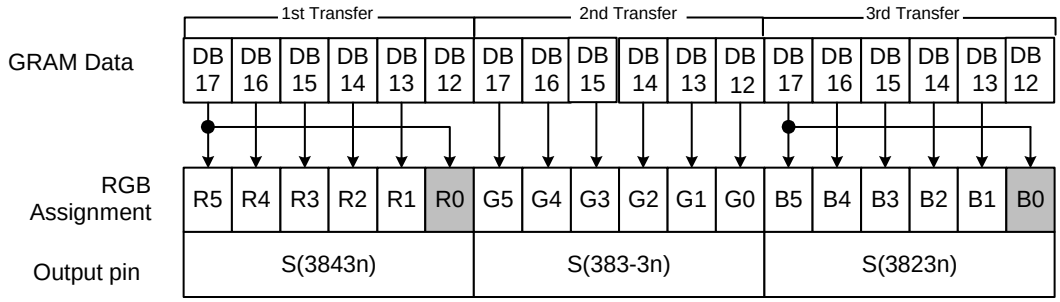
Note: n = lower 8bits of address (0 to 127)

16-Bit Interface



Note: n = lower 8bits of address (0 to 127)

6-Bit Interface



Note: n = lower 8bits of address (0 to 127)

Figure3. 8 GRAM data and display data: RGB interface (SS = “1”, BGR = “1”)

3.1.1 Window Address Function

The HX8310-A contains a 16-bit bus address counter (AC) which assigns address for writing pixel data to GRAM. The most eight bits of AC are express Y address (line address) and the lower eight bits of AC are express X address (pixel address). Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (AM bit and I/D bits) setting. However, the AC will be not updated after reading from GRAM.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0). Therefore , the data can be written consecutively without thinking a data wrap by those bit function. The address setting of window and GRAM are listed as following:

The window address setting range:

00H≦HSA7-0≦HEA7-0≦7FH
00H≦VSA7-0≦VEA7-0≦9FH

GRAM address setting range:

HSA7-0≦AD7-0≦HEA7-0
VSA7-0≦AD15-8≦VEA7-0

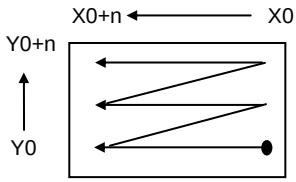
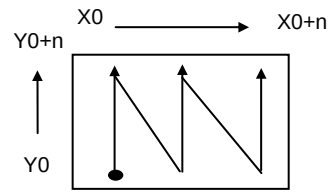
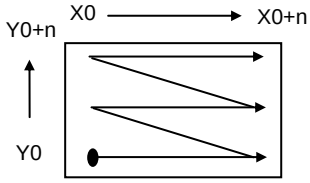
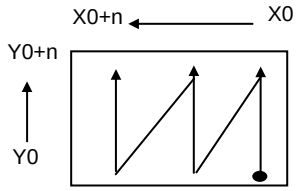
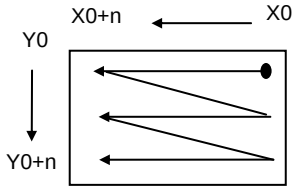
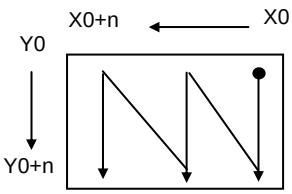
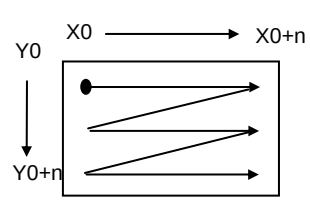
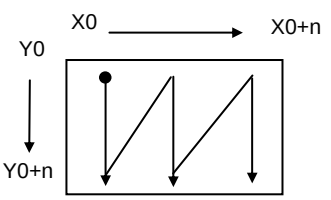
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure3. 9 Address Update Direction Settings

3.1.2 High-Speed Burst RAM Write Function

The HX8310-A incorporates high-speed burst RAM write function that writes data to the internal GRAM about one forth the time of the normal RAM write operation. This function is very useful in high-speed displaying applications such as animation, motion picture and so on.

When the high- speed burst RAM write function is selected (setting HWM=1), data are temporarily stored to the internal registers by executing four times write operation merged with one word and then written to the GRAM at once.

When four-word data (72-bits) is written to the on-chip GRAM, the next four-word data can be written to an internal registers so that high-speed and consecutive RAM writing can be executed.

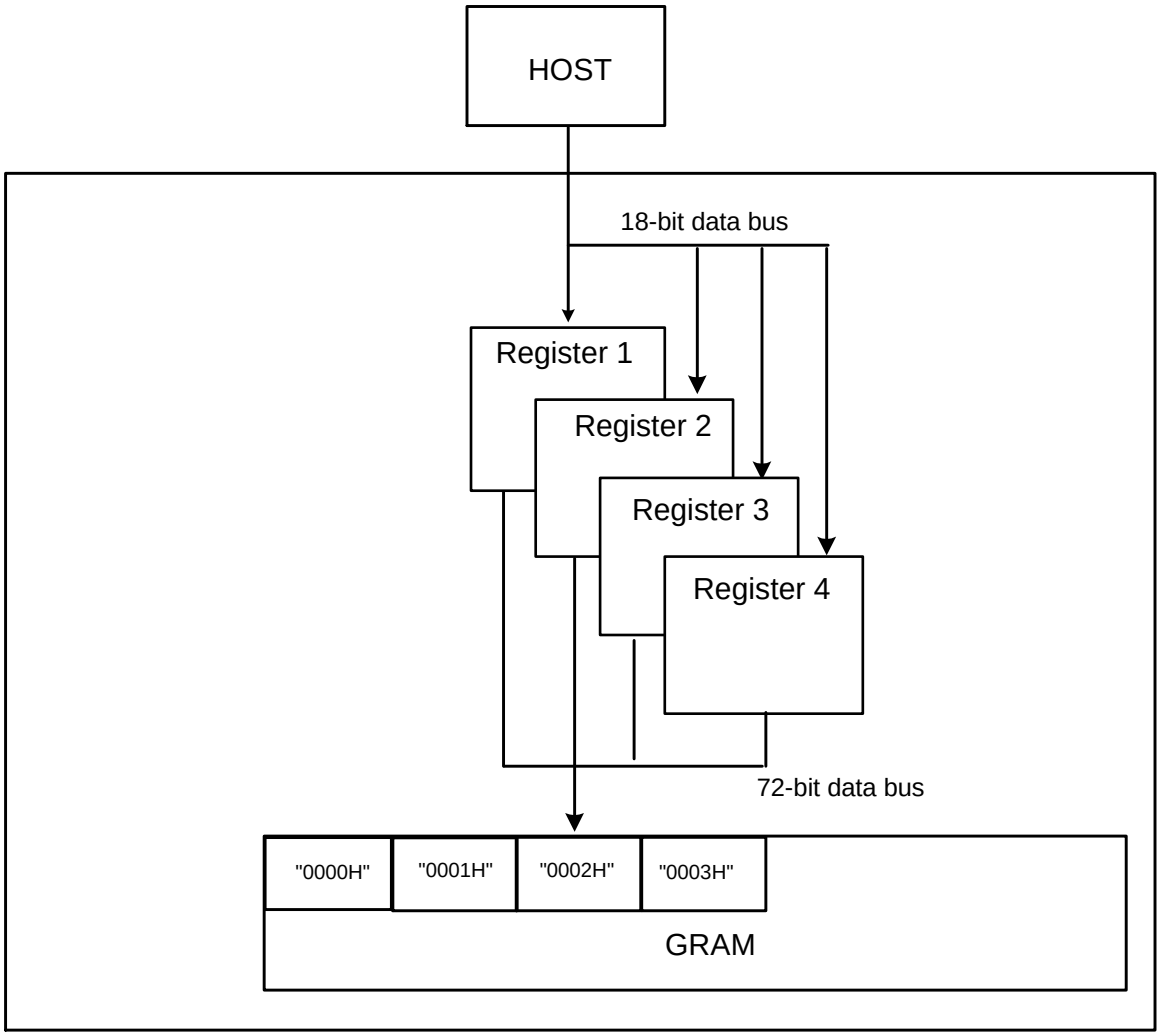
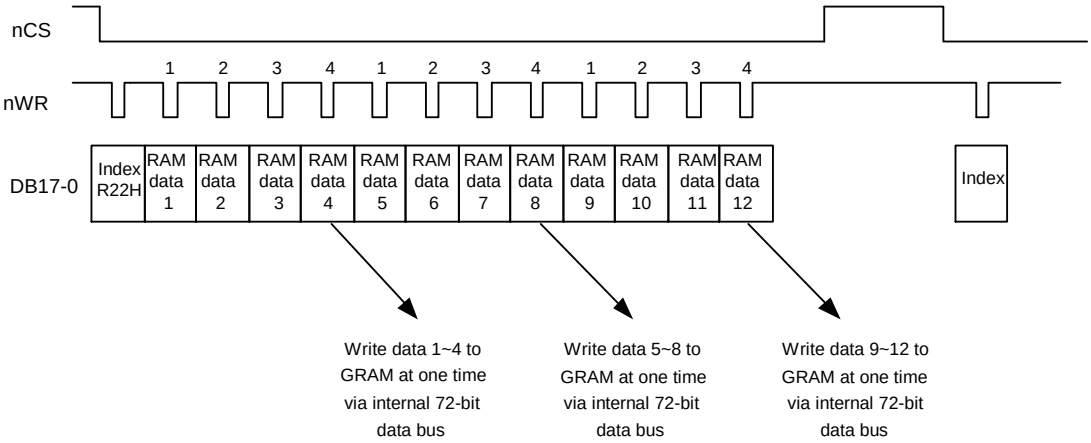


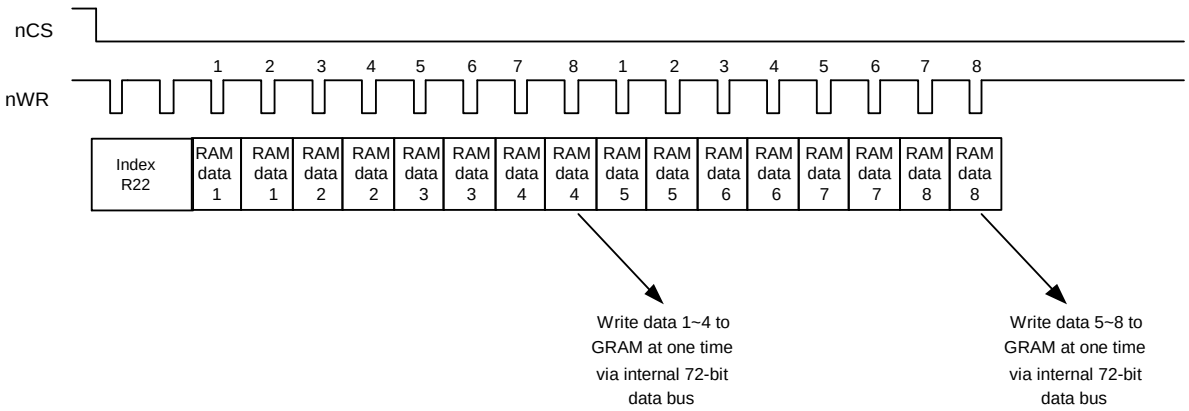
Figure3. 10 The Operation of High-speed Burst RAM function

(a)Example of the Operation of High-speed Consecutive Writing to RAM (16-bit bus interface)



NOTE:
1.When high-speed RAM write is canceled, the next instruction can be executed only after the RAM write execution time has elapsed.
2.When I/D=0, the lower two bits of the start address must be set to 11.
3.When I/D=1, the lower two bits of the start address must be set to 00.

(b)Example of the Operation of High-speed Consecutive Writing to RAM (9-bit bus system interface)



NOTE:
1.Since data is written to GRAM every four words in high-speed RAM write function, data will be stored eight times to internal register before written to GRAM when using 9-bit bus interface.
2.When I/D=0, the lower two bits of the start address must be set to 11.
3.When I/D=1, the lower two bits of the start address must be set to 00.

Figure3. 11 Example of the Operation of High-Speed Consecutive Writing to RAM

When use the high-speed RAM write mode, the following items should be note:

Table3. 3 Comparison between Normal and High-Speed RAM Write Operation

	Normal RAM write (HWM=0)	High-Speed RAM Write (HWM=1)
RAM address set	Specified by word	I/D0 bit =0: Set lower two bits to 11 I/D0 bit =1: Set lower two bits to 00
RAM read	Read by word	×
RAM write	Written by word	Dummy write operations may have to be inserted according to a window address range specification.
Write mask function	¢	¢
Graphics operation function	¢	×
Window address	Set by word unit	Set by four-word unit
AM setting	AM =1/0	AM = 0

¢ : Can be used
× : Cannot be used

Note1. The Graphic operations cannot be used.
Note2. When using the high-speed RAM write mode. The data are written to RAM each 4 words. And the address is set, the lower two bits of the address must be set to the values as below.
Set the lower two bits of the address to 11, If I/D0 = 0.
Set the lower two bits of the address to 00, If I/D0 = 1.
Note3. The data are written to RAM based on each 4 words . The last RAM written operation will not be done. If the number of writing to RAM less than four words.
Note4. The RAM can not be read. If HWM bit had been set to 1. Anyway, HWM bit must be set to 0, if want to read data from RAM.
Note5. The high-speed RAM write and normal RAM write can not be operated at the same time.
Note6. If the high-speed RAM write had been used and a window address-range had been set, dummy write operations may be necessary to match the window address setting.

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4×N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1-0, HEA1-0). Number of total writing operations includes dummy writes each row must be 4×N.

Table3. 4 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

Number of Dummy Write Operations Inserted at the Start of a Row	HSA1	HSA0
0	0	0
1	0	1
2	1	0
3	1	1

Table3. 5 Number of Dummy Write Operation in High-Speed RAM Write (HEA Bits)

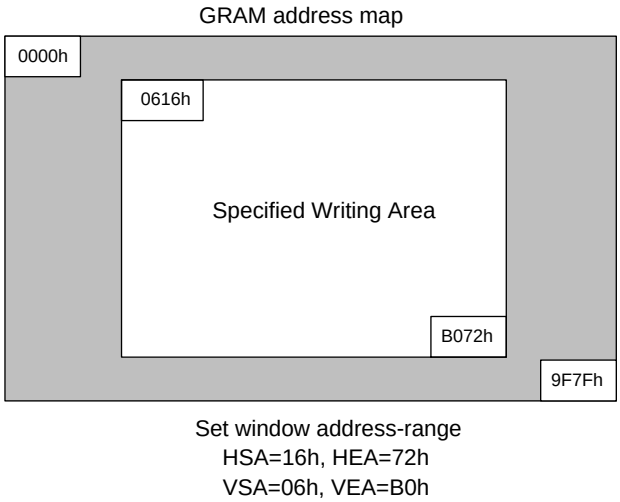
Number of Dummy Write Operations Inserted at the End of a Row	HEA1	HEA0
3	0	0
2	0	1
1	1	0
0	1	1

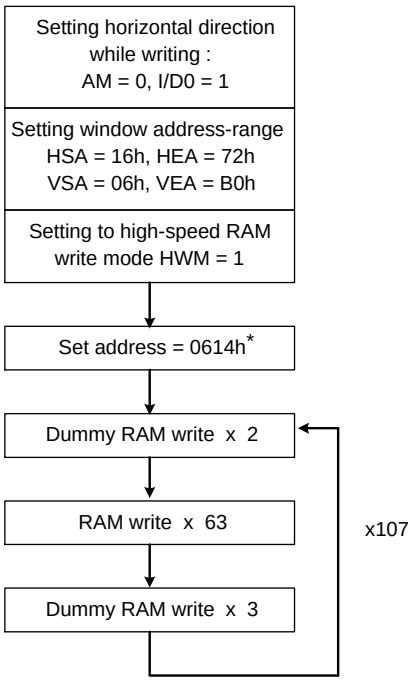
The access of each row must consist of 4×N operations, including the dummy writes

Horizontal access count = 4×N
= First dummy write count + write data count + last dummy write count

An example of high-speed RAM write with a window address-range specified:

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA = 26h, HEA = 64h).





Note: The address set for high speed GRAM write must be 00 or 11 according to I/D bit. Dummy write would not write any data into GRAM.

Figure3. 12 Example of the High-Speed RAM Write with a Window Address-Range Specification

3.2 Graphics Operation Function

Enable write-data Mask function

The write-data mask function executes the operation of writing the corresponding bits to GRAM when the corresponding bits of the write data mask register (WM17-0) are given “0” and out of writing the corresponding bits of GRAM when the corresponding bits of the write data mask register (WM17-0) are given “1” contrary. Furthermore, the data sent from microcomputer are expanded into 18 bits internally in the 8/16-bit bus system interface, and 16-bit bus RGB interface. But in 18-bit bus system or RGB interface , data are not expanded.

When executes the write-data mask function, the GRAM data not overwritten but retained. This function is usually used when only corresponding bits of one specific pixel are rewritten or a designated display color is changed separately.

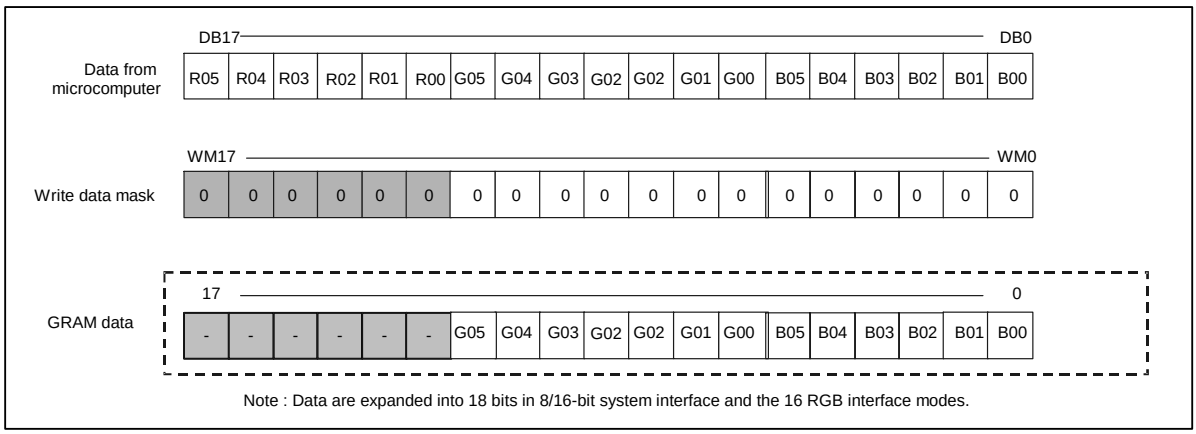


Figure3. 13 Write data mask function

3.3 Display Function

3.3.1 Scan Mode Setting

The HX8310-A can set SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8310-A.

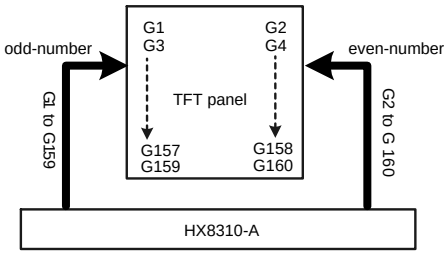
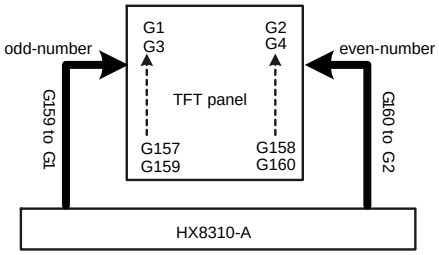
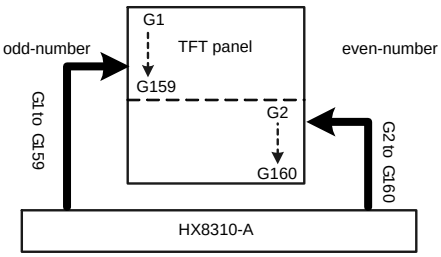
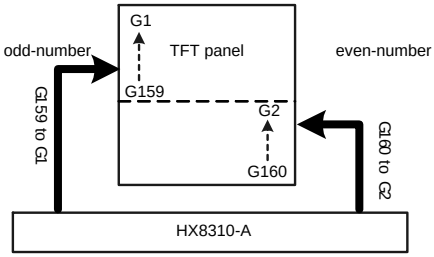
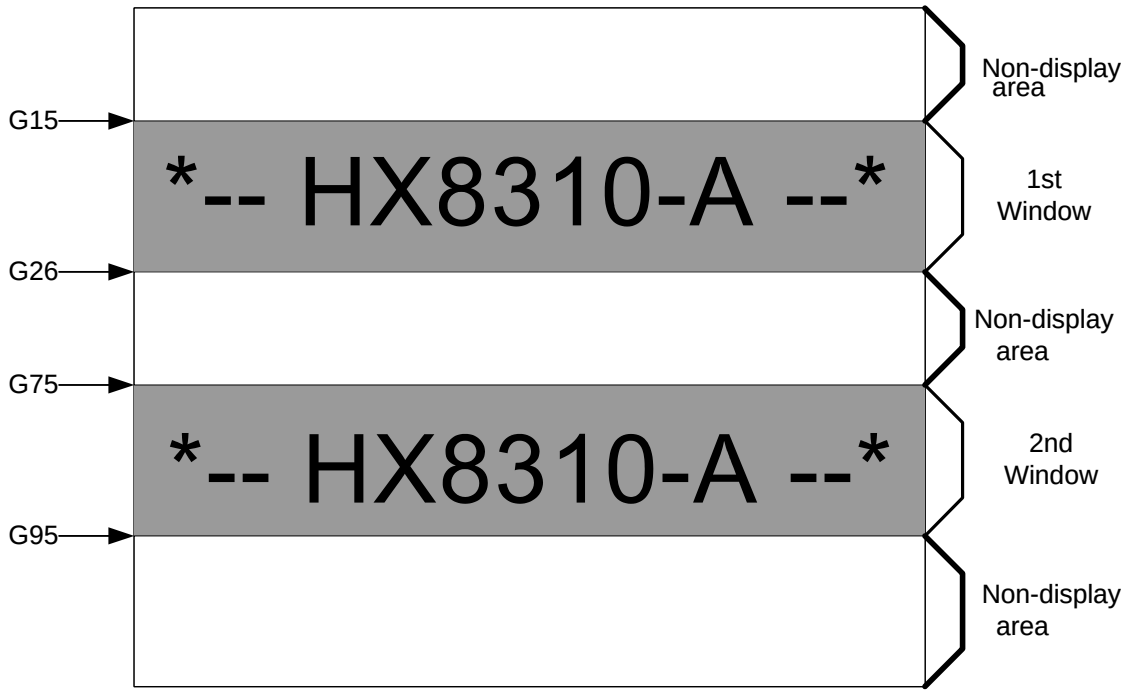
SM	GS	Scan direction
0	0	 G1, G2, G3, G4,.... G157, G158, G159, G160
0	1	 G160, G159, G158, G157,.... G4, G3, G2, G1
1	0	 G1, G3, G5,.... G157, G159, G2, G4, G6,.... G158, G160
1	1	 G160, G158, G156, ... G4, G2, G159, G157, G155,.... G3, G1

Figure3. 14 SCAN Mode Setting

3.3.2 Partial Screen Display

The HX8310-A has one or two screens driving functions. The position of display screen register(R14h and R15h) can display at any position of the whole screen. The numbers of display lines that display on the first and second windows must be less than total LCD-driving lines setting (NL4..0). The rest display area in the screen, should be white display if the type of LCD is normally white and should be black display if the type of LCD is normally black. Therefore, the partial display can reduce the power consumption.

As the below, the first window start line from the SS1(7..0) and end line at SE1(7..0), that are specified by the 1st Display Window Driving Position Register(R14h). The second window start line from SS2(7..0) and end line at SE2(7..0), that are specified by 2nd Display Window Driving Position Register(R15h). And the second display window is availed when the SPT bit is set to 1. The number of the total selection driving lines included the 1st and 2nd display window must be equal to or less than the LCD Drive Line(NL).



Number of Scan Line : NL(4-0) = "10011" (160 lines)
1st Screen Setting : SS1(7-0) = "0E"h , SE1(7-0) = "19"h
2nd Screen Setting : SS2(7-0) = "4A"h , SE2(7-0) = "5E"h , SPT=1

Figure3. 15 Partial Screen Display Example in 2-Window Driving

The conditions as following must be contented when setting the start line SS1(7..0) and end line SE1(7..0) of the 1st display window at register (R14h) and the start line SS2(7..0) and end line SE2(7..0) of the 2nd display window at register (R15h).

Note: That incorrect display may occur if the condition setting are not contented.

Table3. 6 Conditions on the One Screen Driving (SPT = 0)

Condition: 0 £ SS1(7-0) £ SE1(7-0) £ NL

Register Settings	Display Operation
SE1(7..0) - SS1(7..0) +1 = NL	Whole-Screen Display The area of SE1(7..0)-SS1(7..0) is normally displayed
0 < SE1(7..1) - SS1(7..0) +1 < NL	Partial screen display The area of SE1(7..0)-SS1(7..0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Note: The SS2(7-0) and SE2(7-0) settings are ignored.

Table3. 7 Condition on the Two Screen Driving (SPT = 1)

Condition: 0 £ SS1(7-0) £ SE1(7-0) < SS2(7-0) £ SE2(7-0) £ NL

Register Settings	Display Operation
(SE1(7..0) - SS1(7..0) +1) + (SE2(7..0) - SS2(7..0)+1) = NL	Whole-Screen Display The area of (SE27..20) - (SS17..10) is normally displayed
(SE1(7..0) - SS1(7..0) +1) + (SE2(7..0) - SS2(7..0) +1) < NL	Partial Screen Display The area of SE1(7..0) - SS1(7..0) and SE2(7..0) - SS2(7..0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

The driver outputs for non-display area on partial display can be specified. Set the values to match the characteristics for the panel.

Table3. 8 Source Output in Non-Display Area in Partial Display

PT1	PT0	Source Output in Non-Display Area		VCOM output
		Positive Polarity	Negative Polarity	
0	0	V63	V0	VCOMH↔VCOML
0	1	V63	.V0	VCOMH↔VCOML
1	0	VSSD	VSSD	VCOMH↔VCOML
1	1	Hi-Z	Hi-Z	-

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

Table3. 9 Gate Output in Non-Display Area in Partial Display

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

Setting of the partial display should follow the flow shown as below

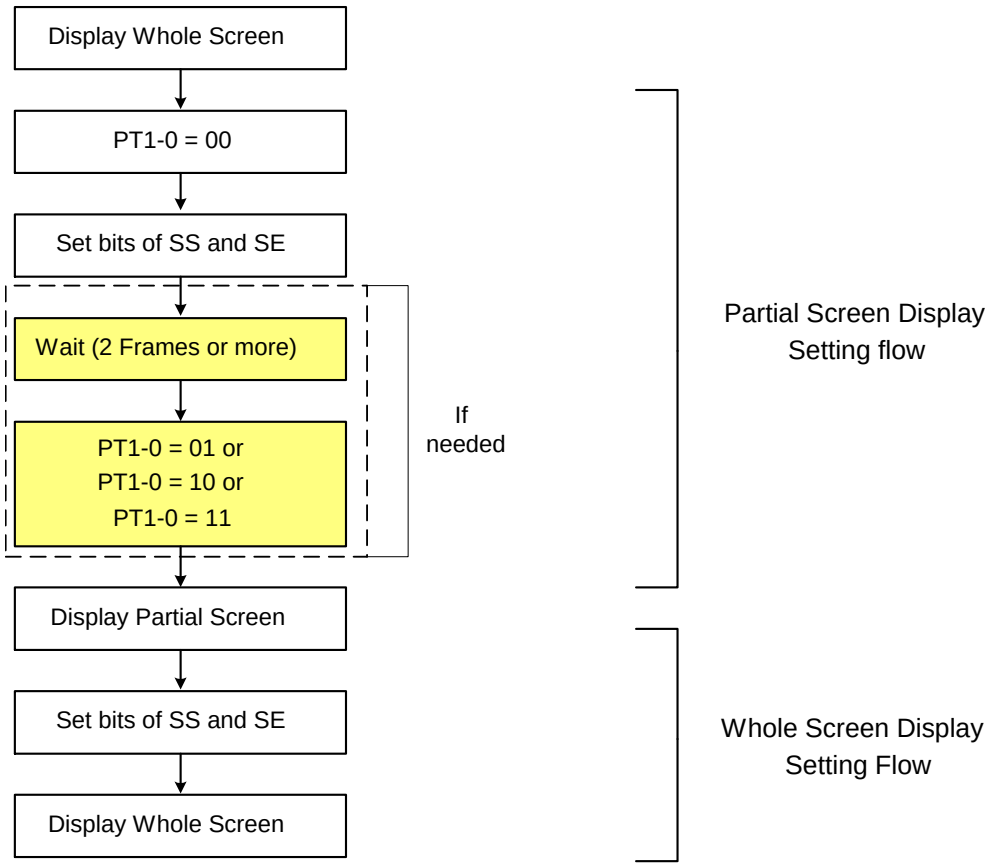


Figure3. 16 Partial Display Setting Flow

3.3.3 8-Color Display

The HX8310-A supports an 8-color display mode. The grayscale level to be used is V0 and V63 with R5 , G5 , B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

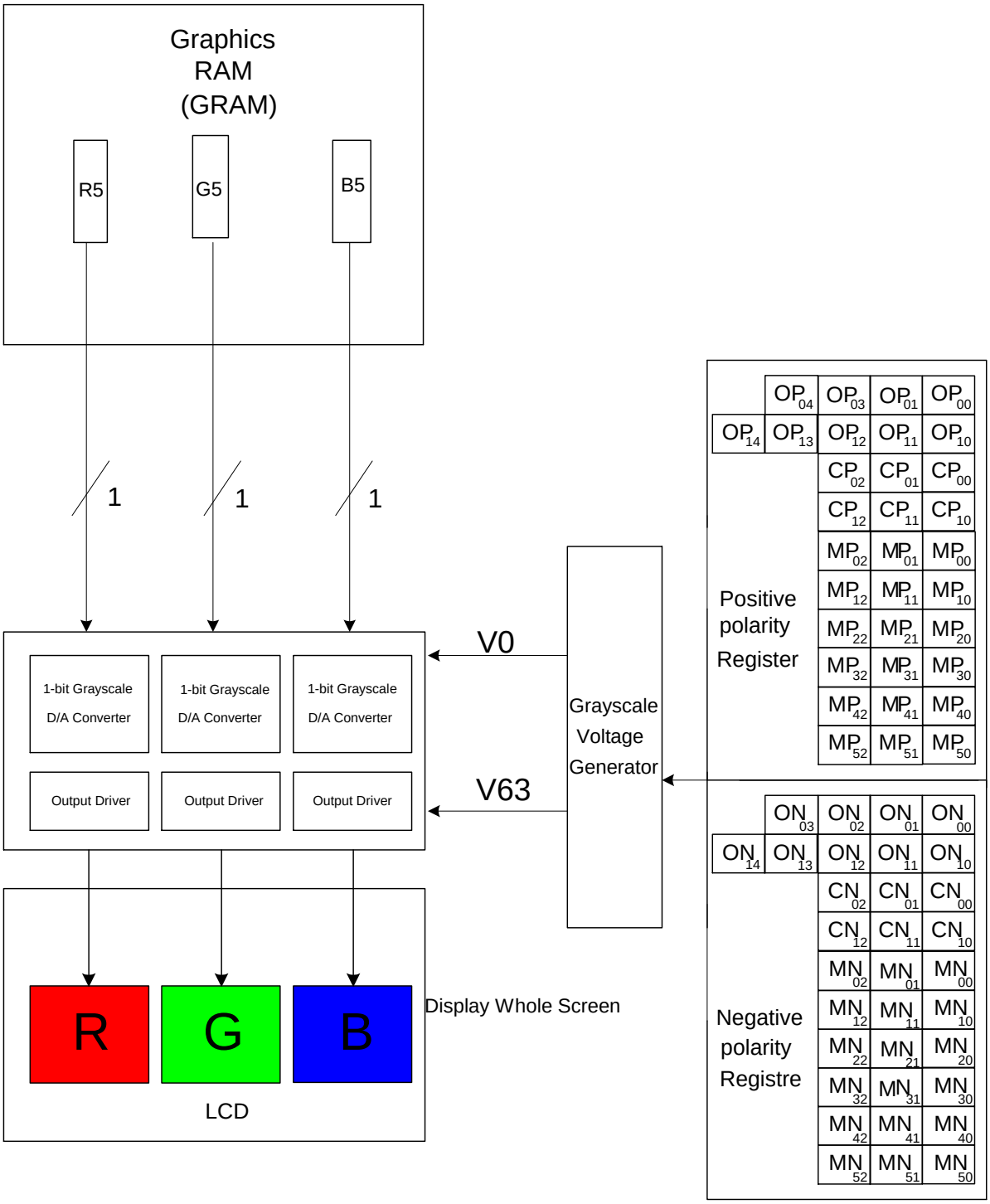


Figure3. 17 Grayscale Control in 8-Color Mode

The follow figure is the switch sequence between the 262,144-color mode and 8-color mode:

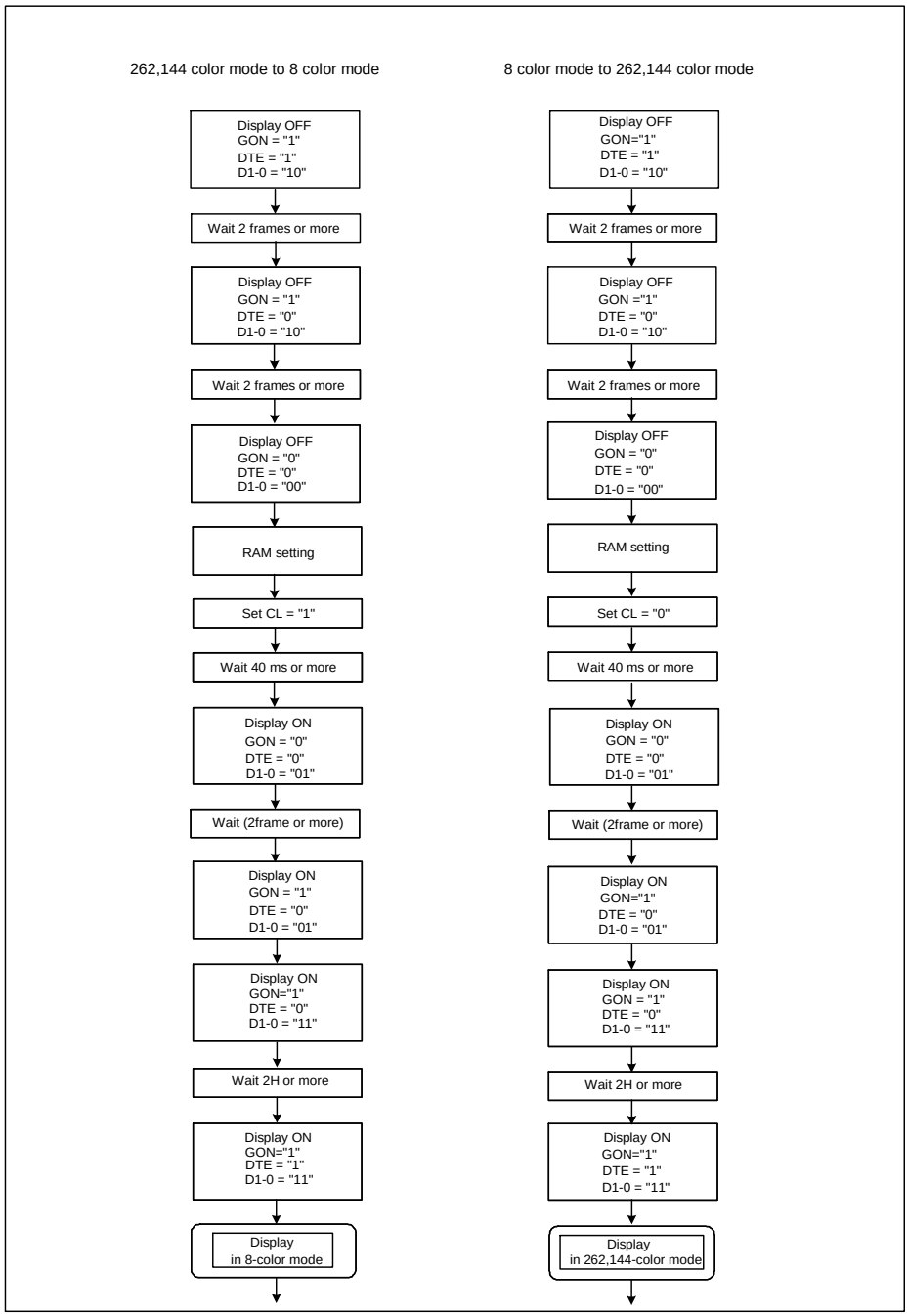


Figure3. 18 Switch Sequence between 262,144-color Mode and 8-color Mode

3.3.4 N-line Inversion LCD Drive

The HX8310-A supports frame inversion and n-line inversion LCD current driving, which n chooses 1~64. The inversion operation is controlled by POL (Polarity of Liquid Crystal) signal which interval is set by NW5-0 bits in R02h register. The HX8310-A internally transfers POL signal for alternating the VCOM voltage and alternates source output voltage according to gamma register with POL signal , which changes the polarity of LCD driving voltage. When a display quality problem occurs, the n-line inversion LCD drive can improve the quality by setting proper n value.
The value of n also represented by the NW bits+1, which represented LCD alternating frequency becomes high when the number of inversion lines were setting a smaller value, hence ,in the LCD cells, the charge or discharge current is increased.

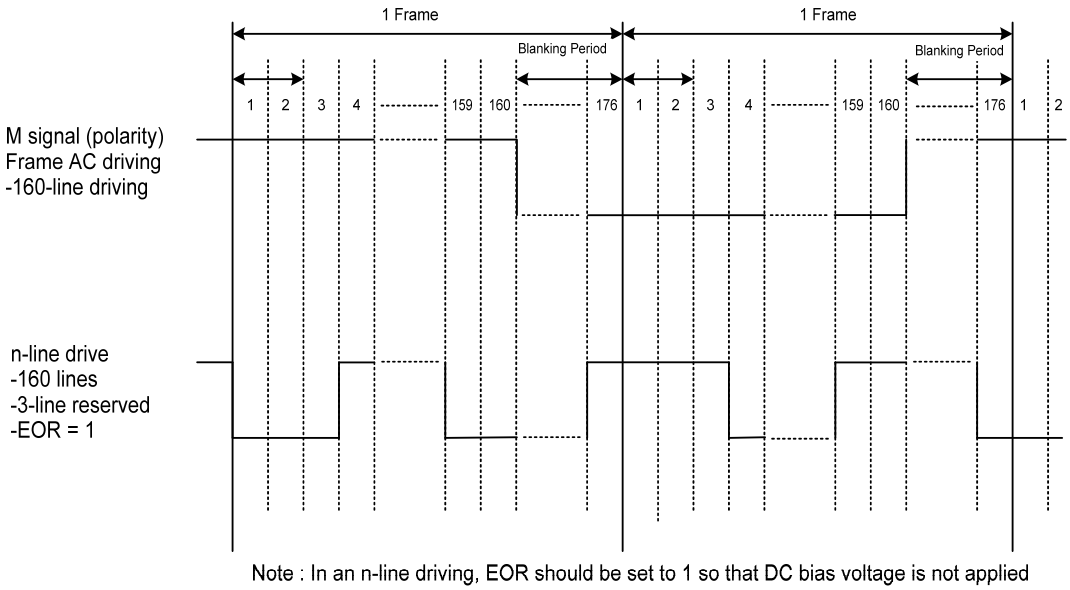


Figure3. 19 N-line Inversion Driving Diagram

3.3.5 Interlaced Driving Function

The HX8310-A has a interlaced function that divided one frame into 3 fields to drive the LCD to avoid flicker To confirm the display quality with the actual LCD display then determined the number of fields. As following table, the gate selection where the number of field is 3 (setting FLD1-0 = 11) and as following figure the output waveform when 3 field interlaced driving is performed is shown.

Table3. 10 Combined with the GS and FLD Setting

GS = 0

FLD1-0	11		
Gate \ **Field**	1	2	3
G1	*		
G2		*	
G3			*
G4	*		
G5		*	
G6			*
G7	*		
G8		*	
G9			*
:	:	:	:
G157			
G158	*		
G159		*	
G160			*

GS = 1

FLD1-0	11		
Gate \ **Field**	1	2	3
G160	*		
G159		*	
G158			*
G157	*		
:		*	
G9			*
G8	*		
G7		*	
G6			*
G5	:	:	:
G4			
G3	*		
G2		*	
G1			*

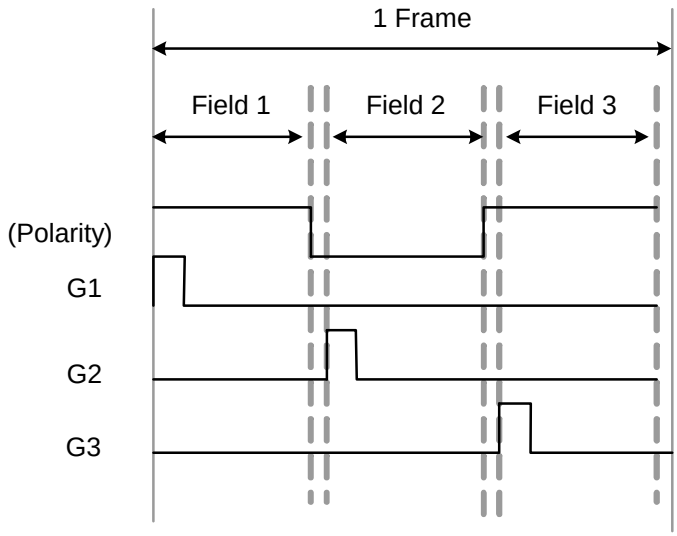


Figure3. 20 Output Timing for Interlaced Gate Signals (Three-Field is Selected)

3.3.6 AC Driving Alternating Timing

LCD must be driven by alternating voltage polarity between liquid crystal layer. The operation of AC drive timing in each type is shown below. The period of AC drive timing is the same as the period of POL signal which is controlled by the value in register R02h (NW).

In frame-inversion AC drive, LCD-driving signal alternates after one frame finishing display and then a FP or back-porch blanking period are inserted. During the blanking period all gate outputs are remain Vgoff. In interlaced drive, LCD-driving signal alternates after one field finishing display and then a blanking period is inserted. The sum of blanking periods in three field is equal to the sum of BP and FP blanking period set in a frame. For n-line inversion AC drive, LCD-driving signal alternates before every n-line display starts. Back-porch blanking period is inserted before all display operations starting and front-porch blanking period is inserted after the completion of all display operations.

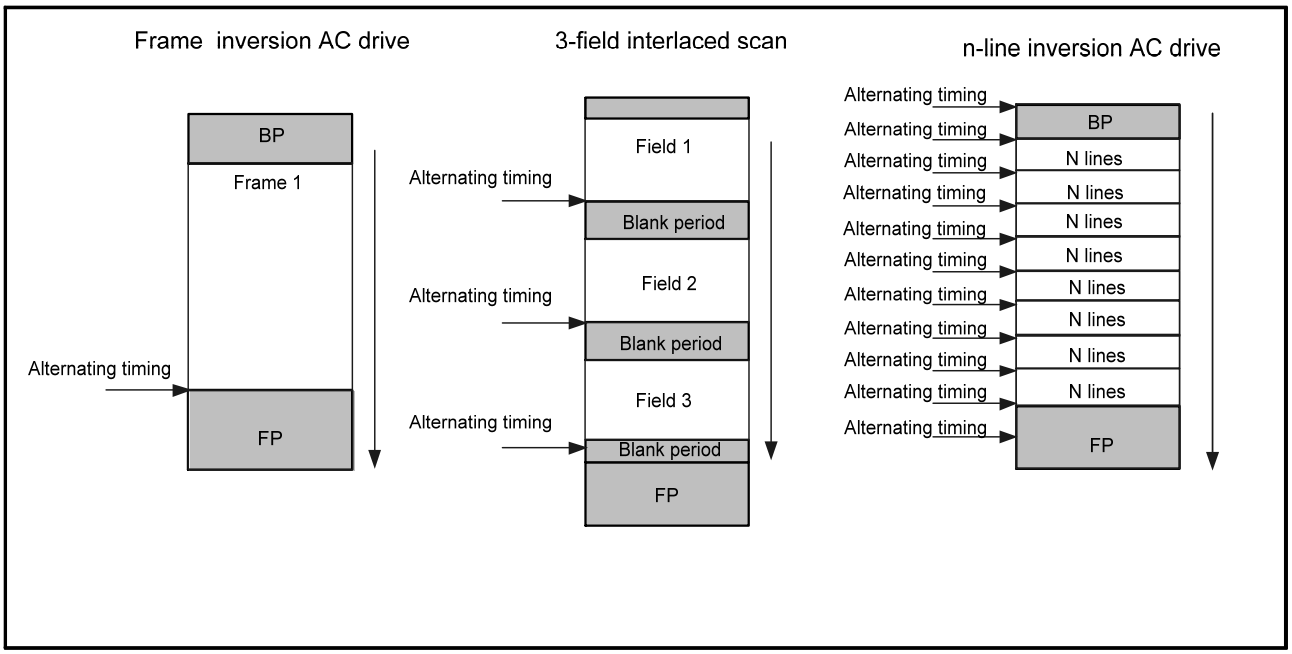


Figure3. 21 AC Driving Alternating Timing Diagram

3.4 Frame-Frequency Adjustment Function

The HX8310-A supports frequency adjustment function of frame frequency stably that can adjust the frame frequency via the register (DIV,RTN bits) setting in R0Bh during the oscillation frequency.

An animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching (an animated display) is required, the frame frequency can be set higher.

Relationship between LCD Drive Duty and Frame Frequency

The LCD driving duty and the frame frequency is obtained by the following calculation. The frame frequency can be adjusted in the 1-H line period bit (RTN) and in the operation clock division bit (DIV) by write the instruction to the relative register.

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL+BP+FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

Example Calculation : To set the maximum frame frequency to 60 Hz

Number of drive lines: 152 lines (NL=”10010”)

1-line period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1 Division

fosc = 60 Hz × (0 + 16) clock × 1 division × (152+16) lines = 161 (KHz)

In this case, the R-C oscillation frequency becomes 161 KHz. The external resistance value of the R-C oscillator must be adjusted so that the frequency of internal R-C oscillator is equal to 161KHz. The display duty can be changed by the partial display with the same frequency setting as above.

3.5 γ-Correction Function

The HX8310-A incorporates gamma adjustment function for the 262,144-color display(64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

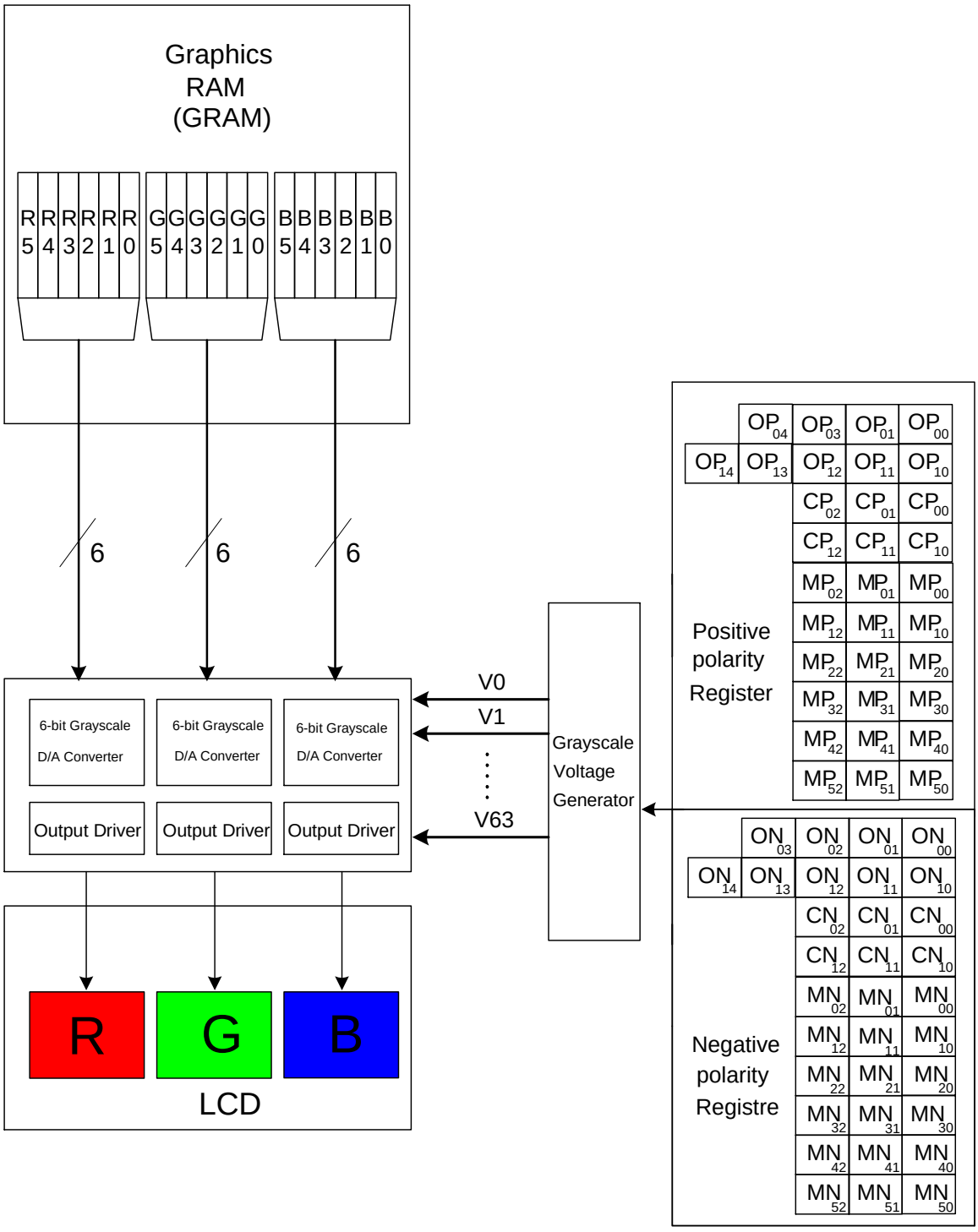


Figure3. 22 Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment , the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

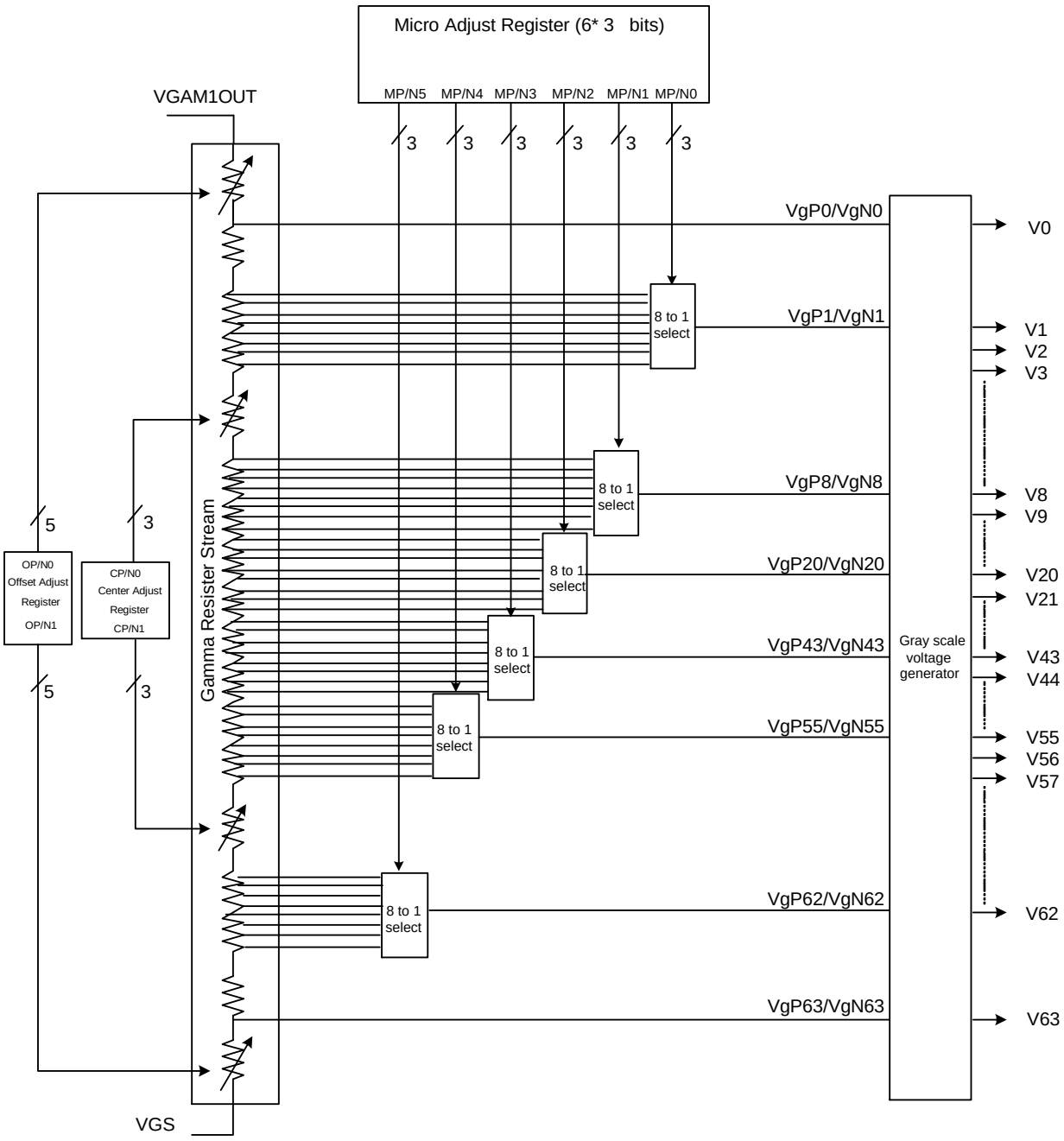


Figure3. 23 Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This HX8310-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

1. Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

2. Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

3. Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors(MP/N0~5), each of which has 8 inputs and generate one reference voltage output (Vg(P/N)1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Table3. 11 Gamma-Adjustment Registers

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity , each one including eight gamma reference voltages. (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

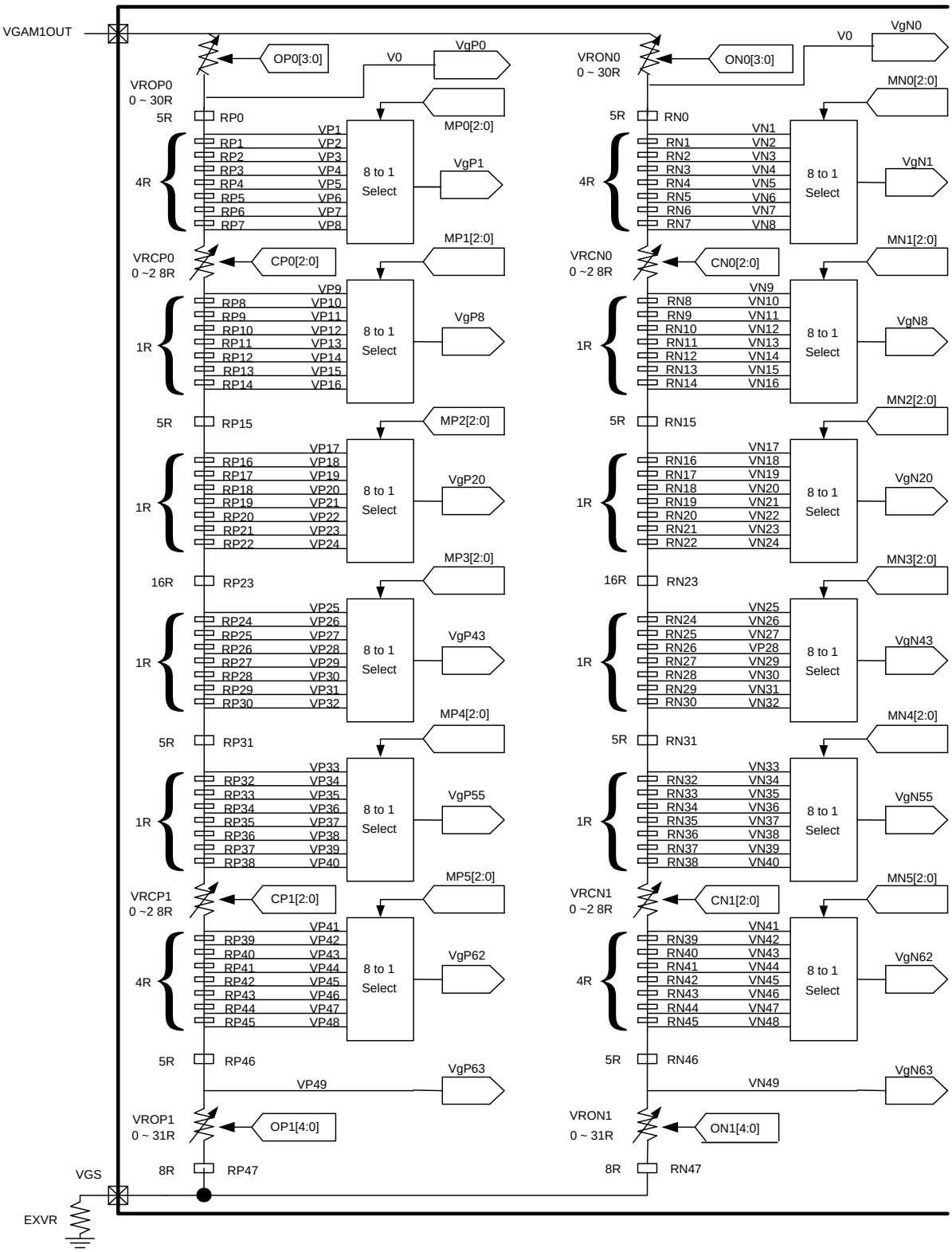


Figure3. 24 Gamma Resister Stream and Gamma Reference Voltage

Variable resister

There are two types of variable resistors, one is for center adjustment, the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship are shown below.

Table3. 12 Offset Adjustment 0 Table3. 13 Offset Adjustment 1 Table3. 14 Center Adjustment

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selector and the relationship are shown below.

Table3. 15 Output Voltage of 8 to 1 Selector

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

The grayscale levels are determined by the following formulas

Table3. 16 Voltage Calculation Formula (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	----	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	V2P8
	MP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	----	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1 ; SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1

VD=(VGAM1OUT-VGS)

([sumRP(sumRN/(sumRP+sumRN)]/[sumRP×sumRN/(sumRP+sumRN)+EXVR]

Table3. 17 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Grayscale Voltage	Formula
V0	VgP0
V1	VgP1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VgP8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgP20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgP43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgP55
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VgP62
V63	VgP63

Note: The following relationship should be retained.

VLCD – V0 > 0.5V
VLCD – V8 > 1.1V
V55-VSSD > 1.1V

Table3. 18 Voltage Calculation Formula (Negative Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VGAM1OUT-VD(VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VGAM1OUT-VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VGAM1OUT-VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VGAM1OUT-VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VGAM1OUT-VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VGAM1OUT-VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VGAM1OUT-VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VGAM1OUT-VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VGAM1OUT-VD((VRON0+33R) /sumRN	VN8
VgN8	MN1 2-0=000	VGAM1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
	MN1 2-0=001	VGAM1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VGAM1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VGAM1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VGAM1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VGAM1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VGAM1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VGAM1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	MN2 2-0=000	VGAM1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VGAM1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
	MN2 2-0=010	VGAM1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VGAM1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VGAM1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VGAM1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VGAM1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VGAM1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	MN3 2-0=000	VGAM1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VGAM1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VGAM1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
	MN3 2-0=011	VGAM1OUT-VD((VRON0+71R+VRCN0) /sumRN	VNP8
	MN3 2-0=100	VGAM1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VGAM1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VGAM1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VGAM1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	MN4 2-0=000	VGAM1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VGAM1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VGAM1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VGAM1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
	MN4 2-0=100	VGAM1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VGAM1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VGAM1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VGAM1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	MN5 2-0=000	VGAM1OUT-VD((VRON0+87R+VRCP0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VGAM1OUT-VD((VRON0+91R+VRCP0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VGAM1OUT-VD((VRON0+95R+VRCP0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VGAM1OUT-VD((VRON0+99R+VRCP0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VGAM1OUT-VD((VRON0+103R+VRCP0+VRCN1)/sumRN	VN45
	MN5 2-0=101	VGAM1OUT-VD((VRON0+107R+VRCP0+VRCN1)/sumRN	VN46
	MN5 2-0=110	VGAM1OUT-VD((VRON0+111R+VRCP0+VRCN1)/sumRN	VN47
	MN5 2-0=111	VGAM1OUT-VD((VRON0+115R+VRCP0+VRCN1)/sumRN	VN48
VgN63	-	VGAM1OUT-VD((VRON0+120R+VRCP0+VRCN1)/sumRN	VN49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1 ; SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1

VD = (VGAM1OUT-VGS)

([sumRP(sumRN/(sumRP+sumRN)]/[sumRP(sumRN/(sumRP+sumRN)+EXVR]

Table3. 19 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Grayscale Voltage	Formula
V0	VgN0
V1	VgN1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VgN8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgN20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgN43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgN55
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VgN62
V63	VgN63

Note: The following relationship should be retained.

VLCD – V0 > 0.5V
VLCD – V8 > 1.1V
V55-VSSD > 1.1V

Table3. 20 GRAM Data and Grayscale Level

GRAM Data Set-up RGB	Selected Grayscale		GRAM Data Set-up RGB	Selected Grayscale		GRAM Data Set-up RGB	Selected Grayscale		GRAM Data Set-up RGB	Selected Grayscale	
	N	P		N	P		N	P		N	P
000000	V0	V63	010000	V16	V47	100000	V32	V31	110000	V48	V15
000001	V1	V62	010001	V17	V46	100001	V33	V30	110001	V49	V14
000010	V2	V61	010010	V18	V45	100010	V34	V29	110010	V50	V13
000011	V3	V60	010011	V19	V44	100011	V35	V28	110011	V51	V12
000100	V4	V59	010100	V20	V43	100100	V36	V27	110100	V52	V11
000101	V5	V58	010101	V21	V42	100101	V37	V26	110101	V53	V10
000110	V6	V57	010110	V22	V41	100110	V38	V25	110110	V54	V9
000111	V7	V56	010111	V23	V40	100111	V39	V24	110111	V55	V8
001000	V8	V55	011000	V24	V39	101000	V40	V23	111000	V56	V7
001001	V9	V54	011001	V25	V38	101001	V41	V22	111001	V57	V6
001010	V10	V53	011010	V26	V37	101010	V42	V21	111010	V58	V5
001011	V11	V52	011011	V27	V36	101011	V43	V20	111011	V59	V4
001100	V12	V51	011100	V28	V35	101100	V44	V19	111100	V60	V3
001101	V13	V50	011101	V29	V34	101101	V45	V18	111101	V61	V2
001110	V14	V49	011110	V30	V33	101110	V46	V17	111110	V62	V1
001111	V15	V48	011111	V31	V32	101111	V47	V16	111111	V63	V0

Relationship between GRAM Data and Output Level (REV = "0")

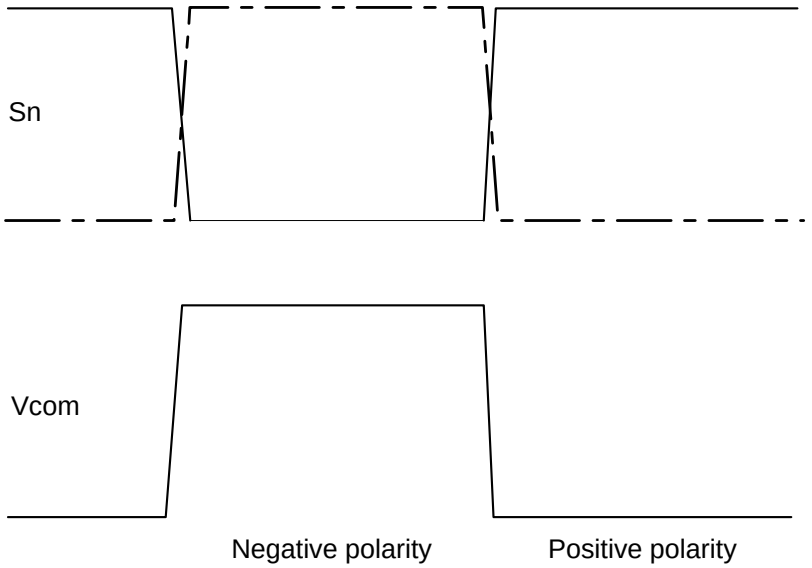
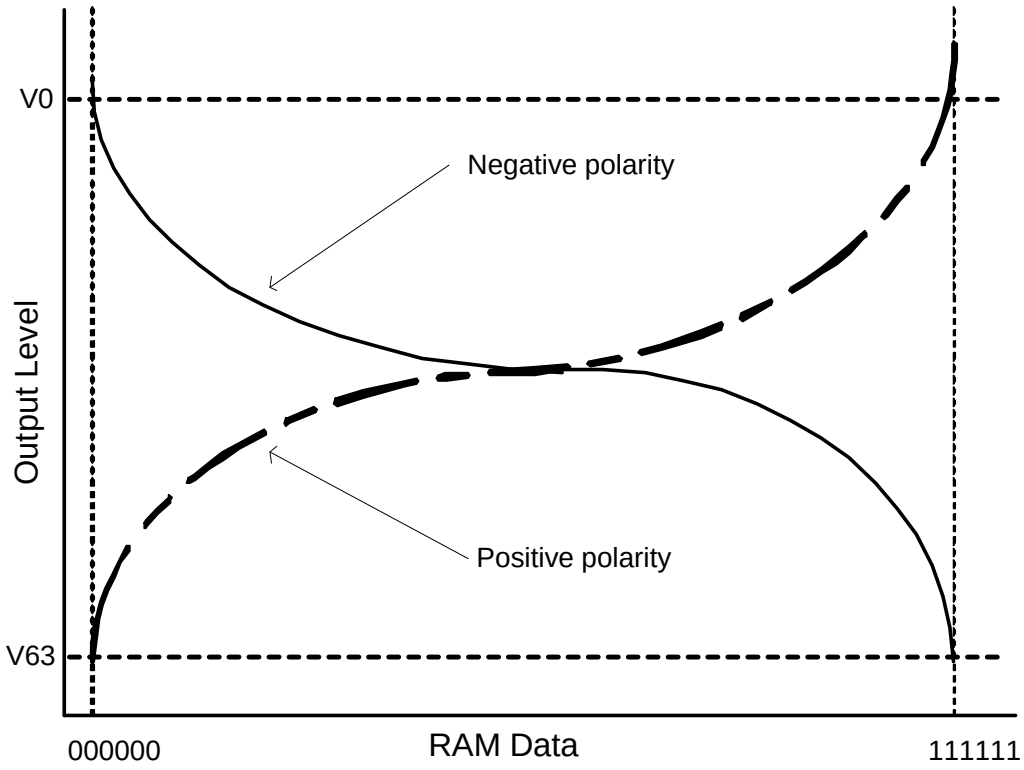


Figure3. 25 Relationship between Source Output and VCOM



(Same characteristic for each RGB)

Figure3. 26 Relationship between GRAM Data and Output Level

3.6 Oscillator

The HX8310-A can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor(Rf). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the DC Electrical Characteristics section.

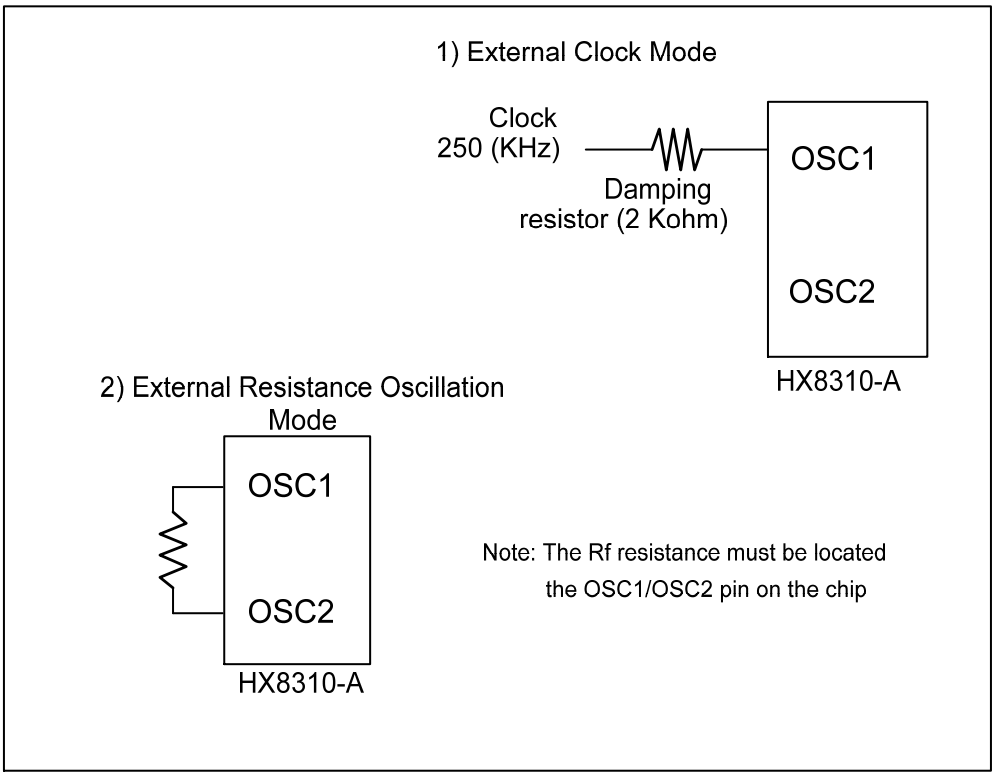


Figure3. 27 Oscillation Circuit

Table3. 21 External Resistance Value and R-C Oscillation Frequency (Temperally Defined)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fOSC	kHz	Rf = 200kΩ, VCC = 3.0V	TBD	300	TBD

4. Registers

The HX8310-A is a single chip with 18-bit bus architecture. The data read from/ write to internal GRAM through the 18-bit data format. When the internal operation of the HX8310-A want to start, first send the control information which is temporarily stored in the registers described as below to allow high-speed interface with a high-performance MPU. The internal operation of the HX8310-A is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (E_NWR), and the data bus signals (DB17-0), control the HX8310-A register.

There are eight categories of registers that is follows:

- Select the index
- Read back the status
- Control the display functions
- Control power management and save power function
- Process or operate the graphics data
- Set internal GRAM addresses for partial data updating
- Transfer data to and from the internal GRAM with High Speed Function
- Set grayscale level for the internal embedded grayscale gamma adjustment

The following specify the explanation of registers such as register format and bit function.

Table4. 1 List Table of Register Set

Register No.	Register	E_NWR	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
IR	Index	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
R00h	Start Oscillation	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
	Device Code Read	R	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	
R01h	Driver Output Control(1)	W	1	0	0	0	0	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (0)	NL2 (1)	NL1 (0)	NL0 (1)	
R02h	LCD AC driving Control	W	1	0	0	0	0	FLD1 (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
R03h	Power Control (1)	W	1	0	0	0	0	0	BT2 (0)	BT1 (0)	BT0 (0)	DC02 (0)	DC01 (0)	DC00 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)	
R05h	Entry Mode	W	1	0	0	0	BGR (0)	0	0	HWM (0)	0	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0	
R06h	16-bits Compare Register	W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	
R07h	Display Control (1)	W	1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON 0	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
R08h	Display Control (2)	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
R09h	Power Control (2)	W	1	0	0	0	0	0	0	DCM1 (0)	DCM0 (0)	DC12 (0	DC11 (0)	DC10 (0)	0	DK (0)	SAP2 (1)	SAP1 (0)	SAP0 (0)	
R0Ah	External Display Interface Control	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	0	0	PTG1 (0)	PTG0 (0)	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
R0Bh	Frame Cycle Adjustment Control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1	CE0	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
R0Ch	Power Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2 (0)	VC1 (0)	VC0 (0)	
R0Dh	Power Control (4)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
R0Eh	Power Control (5)	W	1	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
R0Fh	Gate Scan Start Position	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
R10h	CP/WM 18/16-bit Selection	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F	
R11h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	
R14h	First Screen Driving Position	W	1	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	
R15h	Second Screen Driving Position	W	1	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
R16h	Horizontal RAM Address Position	W	1	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (0)	HEA2 (0)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
R17h	Vertical RAM Address Position	W	1	VEA7 (1)	VEA6 (0)	VEA5 (0)	VEA4 (0)	VEA3 (0)	VEA2 (0)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	
R20h	16-bits RAM Write Data Mask	W	1	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R21h	RAM Address Set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
R22h	RAM data Write/Read	R	1	RAM WD17-0 /RAM (RD17-0)																
R23h	18-bits RAM Write Data Mask (1)	W	1	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R24h	18-bits RAM Write Data Mask (2)	W	1	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
R25h	18-bits Compare Register (1)	W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0	
R26h	18-bits Compare Register (2)	W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12	

Register No.	Register	E_NWR	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
R30h	r Control (1)	W	1	0	0	0	0	0	MP 12 (0)	MP 11 (0)	MP 10 (0)	0	0	0	0	0	MP 02 (0)	MP 01 (0)	MP 00 (0)	
R31h	r Control (2)	W	1	0	0	0	0	0	MP 32 (0)	MP P31 (0)	MP 30 (0)	0	0	0	0	0	MP 22 (0)	MP 21 (0)	MP 20 (0)	
R32h	r Control (3)	W	1	0	0	0	0	0	MP52 (0)	MP 51 (0)	MP 50 (0)	0	0	0	0	0	MP 42 (0)	MP 41 (0)	MP 40 (0)	
R33h	r Control (4)	W	1	0	0	0	0	0	CP 12 (0)	CP 11 (0)	CP 10 (0)	0	0	0	0	0	CP 02 (0)	CP 01 (0)	CP00 (0)	
R34h	r Control (5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)	
R35h	r Control (6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)	
R36h	r Control (7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)	
R37h	r Control (8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)	
R3Ah	r Control (9)	W	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)					OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)	
R3Bh	r Control (10)	W	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)					ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)	

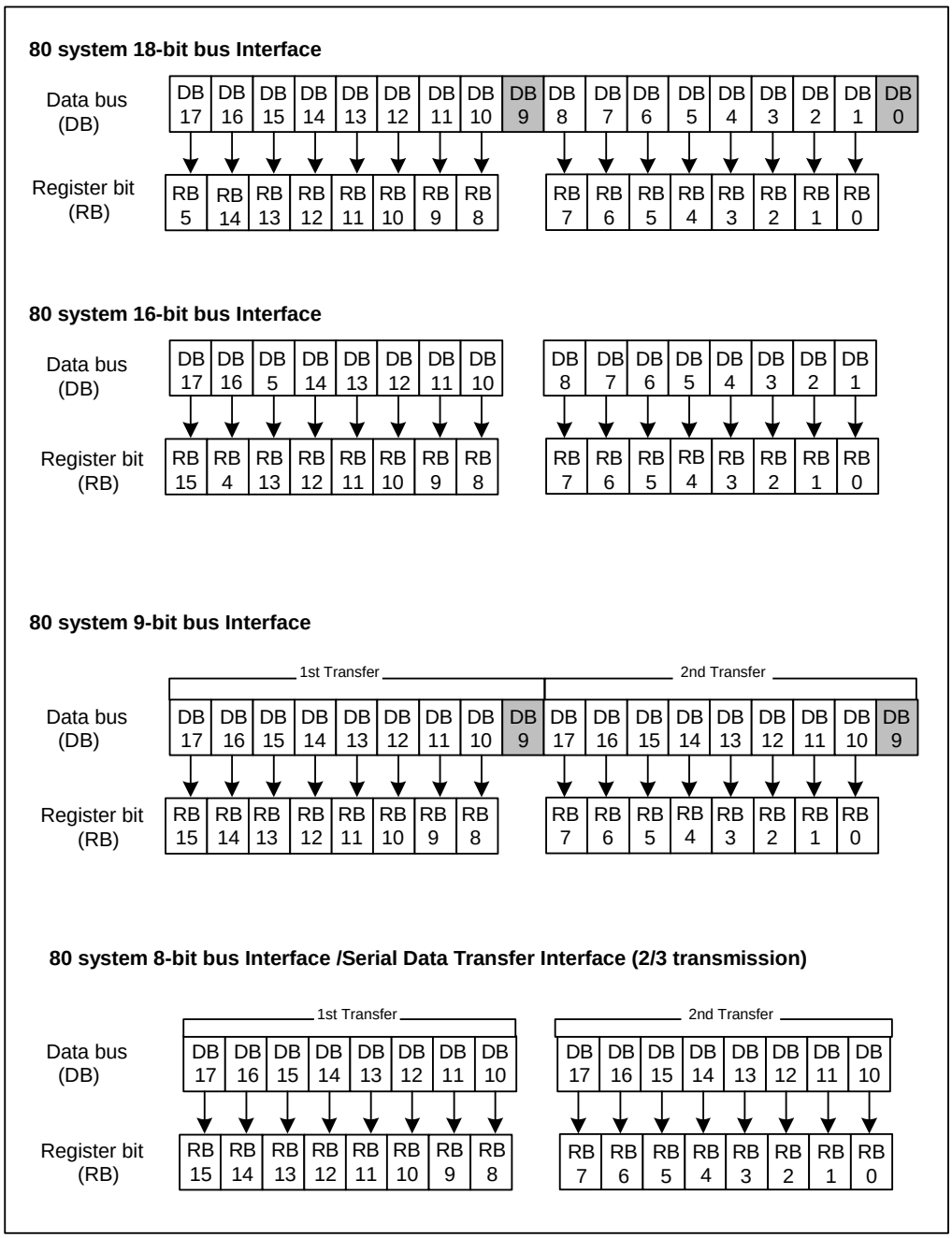


Figure4. 1 80 System interface mode

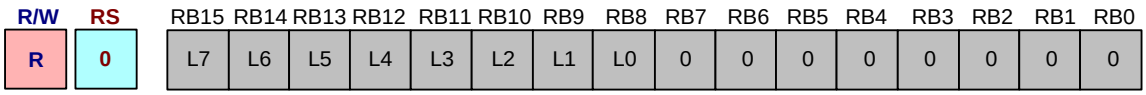
4.1 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure4. 2 Index Register

Index register (IR) specifies Index of the register from R00h to R4Fh. It sets the register number (ID6-0) in the range from 000000b to 1111111b in binary form.

4.2 Status Read Register



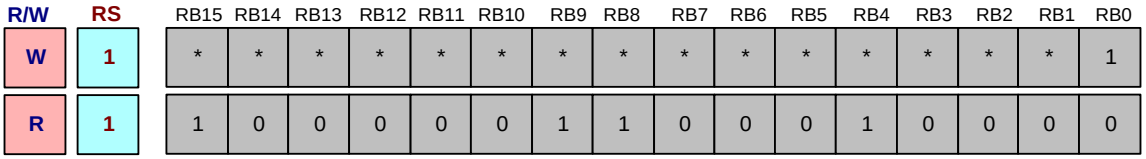
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure4. 3 Status Read Register

Status Read Register for reading the internal status of the HX8310-A.

L7–0: Indicate the position of driving line, where the liquid crystal display is driven at present.

4.3 Start Oscillation Register (R00h)



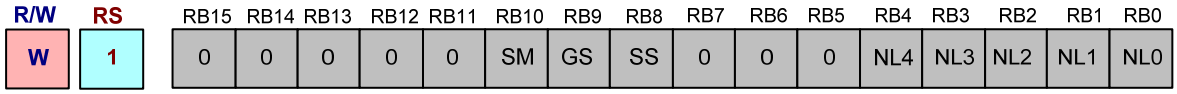
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Figure4. 4 Start Oscillation Register (R00h)

Start Oscillation Register restarts the oscillator from the suspend state at the standby mode. After setting this register, and wait at least 10 ms for oscillation stabilizing before setting the next register.

When the read commend is issued, 8310h is read.

4.4 Driver Output Control Register (R01h)



R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure4. 5 Driver Output Control Register (R01h)

NL4–0: Specify the number of scan lines for the LCD driver can be adjusted by every 8 lines. Select the setting value for the panel size or higher.

Table4. 2 NL bits and Scan Line

NL4	NL3	NL2	NL1	NL0	Gate Driver Used	Number of Scan Line	Display Size
0	0	0	0	0	Ignore	Ignore	Ignore
0	0	0	0	1	G1~G16	16	384*16 dots
0	0	0	1	0	G1~G24	24	384 *24dots
0	0	0	1	1	G1~G32	32	384*32 dots
0	0	1	0	0	G1~G40	40	384*40 dots
0	0	1	0	1	G1~G48	48	384 *48dots
0	0	1	1	0	G1~G56	56	384*56 dots
0	0	1	1	1	G1~G64	64	384*64 dots
0	1	0	0	1	G1~G72	72	384*72 dots
:	:	:	:	:	:	:	:
1	0	0	0	0	G1~G136	136	384*136 dots
1	0	0	0	1	G1~G144	144	384*144 dots
1	0	0	1	0	G1~G152	152	384*152 dots
1	0	0	1	1	G1~G160	160	384*160 dots
:	:	:	:	:	:	:	:
1	1	1	1	1	G1~G160	160	384*160 dots

SS: The source driver output shift direction selected. When SS=0, the shift direction from S1 to S384. When SS = 1, the shift direction from S384 to S1.

GS: Specify the shift direction of gate driver output. When GS = 0, the shift direction from G1 to G160. When GS = 1, the shift direction from G160 to G1,.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

4.5 LCD Driving Waveform Control Register (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure4. 6 LCD-Driving-Waveform Control Register (R02h)

NW5–0: Specify the number of n lines that will alternate POL signal when B/C = 1. The inversion is occurred every n + 1 line, and the 1st to the 64th lines can be selected.

EOR: EOR=1 will force POL signal alternate at the beginning of a frame in n-line inversion driving mode (B/C=1), no matter the last interval of POL signal is over or not in last frame. Therefore, EOR bit is used when the POL signal is not completely alternated in some number of drive line in LCD display area. For details, see the “N-line Inversion LCD Drive” section.

B/C: When B/C = 0, POL signal alternates in every frame for LCD drive. When B/C = 1, POL signal alternates in each n line specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “N-line Inversion LCD Drive” section.

FLD1-0: Set the number of n field for interlaced driving mode. For details, see the "Interlaced driving function section".

Table4. 3 FLD bits and Interlaced field

FLD1	FLD0	Number of field
0	0	Ignore
0	1	1 field
1	0	Ignore
1	1	3 fields

4.6 Power control Register 1 (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	BT2	BT1	BT0	DC02	DC01	DC00	AP2	AP1	AP0	SLP	STB

Figure4. 7 Power Control Register 1 (R03h)

STB: When STB = "1", the HX8310-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. Anyway, have not any external clock are supplied. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0")
b. Start the oscillation

Within the standby mode, the GRAM data and regiser content may be lost. For preventing this, they have to set again after the standby mode is exited.

SLP: When SLP = 1, the HX8310-A into the sleep mode, where the internal display operations are suspend except for the R-C oscillator, thus the current consumption can be reduced. Within the sleep mode, the GRAM data and register content cannot be accessed although they are retained.

AP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP2–0 = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

Table4. 4 AP Bits and amount of current in Operational Amplifier

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	Ignore
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

BT2–0: Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced. The different setting values of VLCD, VGH and VGL is got as follow figure that connect with C22 or not.

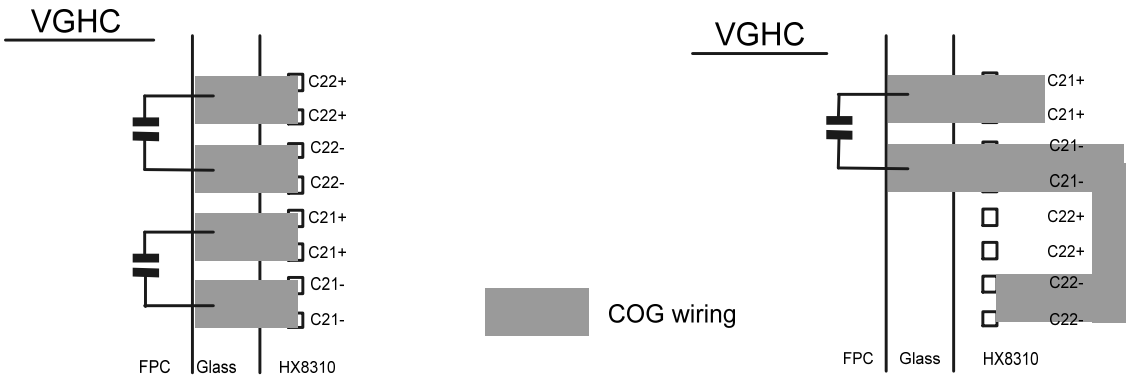


Figure4. 8 Different Connection of C22 Capacitor

Table4. 5 BT Bits and VLCD,VGH and VGL Outputs

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x VCI1	-1 x VCI1	6 x VCI1	-5 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B, C22 A/B
0	0	1	2 x VCI1	-1 x VCI1	6 x VCI1	-4 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	0	2 x VCI1	-1 x VCI1	6 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	1	2 x VCI1	-1 x VCI1	5 x VCI1	-5 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	0	2 x VCI1	-1 x VCI1	5 x VCI1	-4 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	1	2 x VCI1	-1 x VCI1	5 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	0	2 x VCI1	-1 x VCI1	4x VCI1	-4x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	-	-	-	-	Setting Disable

Table4. 6 BT Bits and VLCD,VGH and VGL Outputs (without CapacitoC22)

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x VCI1	-1 x VCI1	4 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B,
0	0	1	2 x VCI1	-1 x VCI1	4 x VCI1	-2 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
0	1	0	2 x VCI1	-1 x VCI1	4 x VCI1	-1 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
0	1	1	2 x VCI1	-1 x VCI1	3 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	0	0	2 x VCI1	-1 x VCI1	3 x VCI1	-2 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	0	1	2 x VCI1	-1 x VCI1	3 x VCI1	-1 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	1	0	2 x VCI1	-1 x VCI1	2x VCI1	-2x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	-	-	-	-	Setting Disable

Note: The factors of step-up for VGH are derived from VCI1 when VLCD and VCI2 are shorted. The conditions of VLCD ≦ 5.5V, VCL ≦ -3.3V, VGH ≦ 16.5V, and VGL ≦-16.5V must be satisfied.

DC02–00: Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

Table4. 7 Operation Frequency of Step-up Circuit 1 (fdcdc1)

fosc = R-C oscillation frequency

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1
0	0	0	fosc / 4
0	0	1	fosc / 8
0	1	0	fosc / 16
0	1	1	fosc / 32
1	0	0	fosc / 64
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

4.7 Entry Mode Register (R05h)

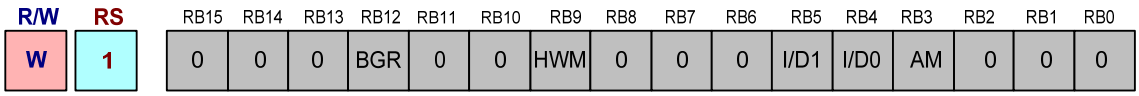


Figure4. 9 Entry Mode Register (R05h)

AM: The updating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D[1...0].

I/D[1..0]: The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the update method with I/D1-0 & AM bit.

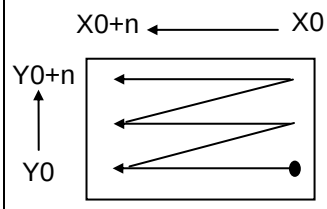
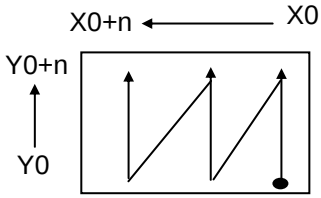
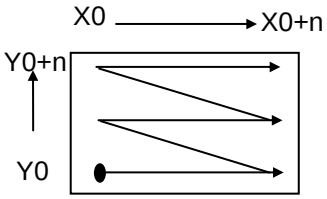
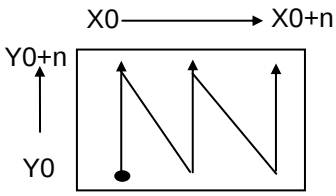
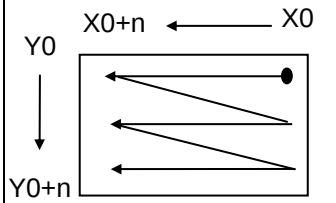
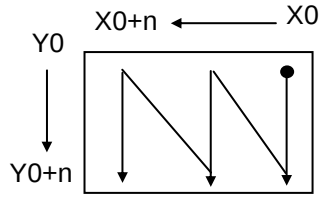
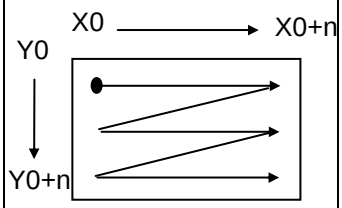
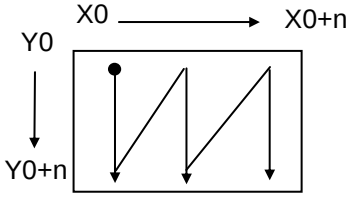
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure4. 10 Address Direction Settings

HWM: When HWM=1 (high-speed write mode), four words are written to GRAM in one time.

BGR: The order of <R><G><B> dot color. When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order. Setting BGR will change the bit order of (WM17-0) in the same way.

4.8 16-bit Compare Register (R06h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CP 15	CP 14	CP 13	CP 12	CP 11	CP 10	CP 9	CP 8	CP 7	CP 6	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

Figure4. 11 16-bit Compare Register (R06h)

The write date sent from the microcomputer is modified in the HX8310A and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

CP15-0: Set the 16-bits compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

4.9 Display Control Register 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure4. 12 Display Control Register 1 (R07h)

D1–0: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with all of the source outputs are set to the VSSD level. Because of this, the HX8310-A can control the charging current for the LCD with AC driving.

Control the display on/off while control GON and DTE. When D1–0 = 01, the internal display of the HX8310-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table4. 8 D Bits and Operation

D1	D0	Source Output	HX8310-A Internal Display Operations	Gate-Driver Control Signals (CPV, FLM, M) (CPV,STV,POL)
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	Non-lit display	Operate	Operate
1	1	Display	Operate	Operate

Notes: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

REV: REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

Table4. 9 Display Control Instruction

REV	GRAM data	Source output level							
		Display area		Non-display area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 . . 18'h3FFFF	V63 . . V0	V0 . . V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 . . 18'h3FFFF	V0 . . V63	V63 . . V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z

CL: CL = 1, the display mode is set to the 8-color display mode. For details, see the section on the 8-color display mode section.

Table4. 10 CL Bit for 8-Color Display

CL	Number of Display Colors
0	262,144
1	8

Note: The display 262,144 colors when 18/9 bit bus interface is using, and display 65,536 colors when 16/8 bit bus interface is using.

DTE, GON: Specify the output level of gate line. VCOM level becomes VSSD when GON = 0.

Table4. 11 GON and DTE bits

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Note: GON bit is used in the gate driver. Control according to the bits' values is executed by the gate driver. For details, see the data sheet of the gate driver.

SPT: When SPT = 1, the 2-division LCD drive is performed so a LCD can be divided 2 split display windows. For details, see the Partial Screen Display Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st display window. When VLE2 = 1, a vertical scroll is performed in the 2nd display window. Vertical scrolling on the two windows cannot be controlled at the same time.

Table4. 12 VLE Bits

VLE2	VLE1	1st Display Window	2nd Display Window
0	0	Fixed display	Fixed display
0	1	Scrolled display	Fixed display
1	0	Fixed display	Scrolled display
1	1	Ignore	Ignore

PT1-0: When partial display is in use, these bits determine the source output in the non-display area. For details, see the Partial Screen Display Function section. The output on the source lines during the periods of the front and BP are also determined by PT1-0.

Table4. 13 PT Bits for Source and Gate Output in Non-Display Area of Partial Display

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	VCOM output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VCOMH↔VCOML
0	1	V63	.V0	Reference to PTG1-0	VCOMH↔VCOML
1	0	VSSD	VSSD	Reference to PTG1-0	VCOMH↔VCOML
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

4.10 Display Control Register 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSPL	HSPL	DPL	EPL	FP3	FP2	FP1	FP0	ISC3	ISC2	ISC1	ISC0	BP3	BP2	BP1	BP0

Figure4. 13 Display Control Register 2 (R08h)

EPL: Specify the polarity of Enable pin in RGB interface mode.

Table4. 14 EPL bit and Enable pin

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to PD17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to PD17-0

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

ISC3-0: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

Table4. 15 ISC bit setting

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

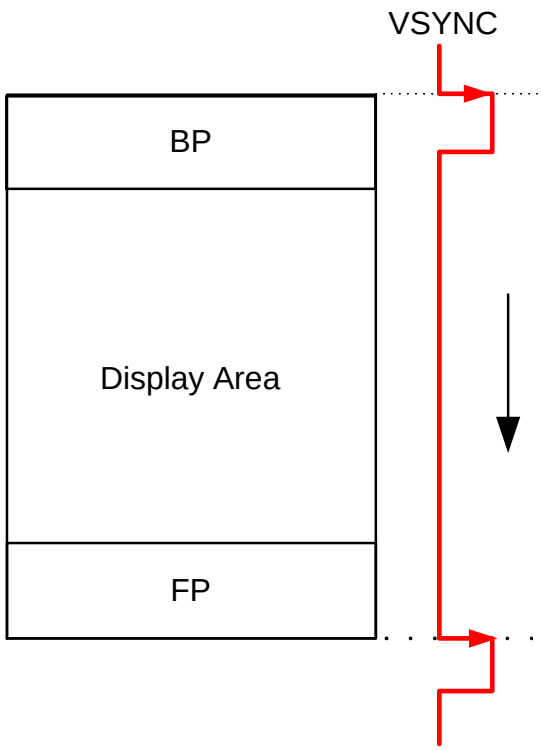
BP3-0: Specify the amount of scan line for back porch(BP).
FP3-0: Specify the amount of scan line for front porch (FP).

The setting vale, ensure that:
BP + FP ≦ 16 lines
PB ≧ 2 lines
FP ≧ 2 lines

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by he display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

Table4. 16 BP/FP bits

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	Number of FP Line	Number of BP Line
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	3 lines	
0	1	0	0	4 lines	
0	1	0	1	5 lines	
0	1	1	0	6 lines	
0	1	1	1	7 lines	
1	0	0	0	8 lines	
1	0	0	1	9 lines	
1	0	1	0	10 lines	
1	0	1	1	11 lines	
1	1	0	0	12 lines	
1	1	0	1	13 lines	
1	1	1	0	14 lines	
1	1	1	1	Ignore	



Note: The output signal is delay 2 lines timing from the VSYNC to the LCD

Figure4. 14 BP/FP

Table4. 17 BP3-0, FP3-0 Setting dependent on the operation mode

Operation Mode	Number of Interlace Scan Field	BP	FP	BP + FP
System Interface	FLD1-0 = 01	≥2 lines	≥2 lines	≤ 16 lines
	FLD1-0 = 11	3 lines	5 lines	-
RGB Interface	-	≥2 lines	≥2 lines	≤ 16 lines
VSYNC Interface	-	≥2 lines	≥2 lines	16 lines

4.11 Power control Register 2 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	DCM1	DCM0	DC12	DC11	DC10	0	DK	SAP2	SAP1	SAP0

Figure4. 15 Power Control Register 2 (R09h)

SAP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP2–0 = 000, the current consumption can be reduced by stopping the operational amplifier.

Table4. 18 SAP Bits and amount of current in Operational Amplifier

SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	Stop
0	0	1	Setting Disable
0	1	0	0.62
0	1	1	0.71
1	0	0	1
1	0	1	1.25
1	1	0	1.43
1	1	1	Setting Disable

DK: ON/OFF the operation of step-up circuit 1. When power on, the VLCD no output until VGHC is set up completely. For detail, see the Power Supply Setting Sequence.

Table4. 19 DK bit for the operation of step-up circuit 1

DK	Operation of step-up circuit 1
0	ON
1	OFF

DC12–10: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

Table4. 20 Operation Frequency of Step-up Circuit 2 (fdcdc2)

fosc = R-C oscillation frequency

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2
0	0	0	fosc / 8
0	0	1	fosc / 16
0	1	0	fosc / 32
0	1	1	fosc / 64
1	0	0	fosc / 128
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

Note : Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

DCM1-0: Set the set-up frequency in a blank period during 8-color mode (CL=”1”).

Table4. 21 Step-up frequency setting

DCM1	DCM0	Step-up frequency
0	0	Ignore
0	1	1/2 x fdcdc1,2
1	0	1/4 x fdcdc1,2
1	1	1/8 x fdcdc1,2

4.12 External Display Interface Control Register 1 (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM1	DFM0	0	0	PTG1	PTG0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

Figure4. 16 External Display Interface Control Register 1 (R0Ah)

RIM1- 0: Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

Table4. 22 RIM bit for the Transfer Mode of RGB interface

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode(1 transfer/pixel)
0	1	16-bit bus RGB interface Mode(1 transfer/pixel)
1	0	6-bit bus RGB interface Mode(3 transfers/pixel)
1	1	Ignore

DM1-0: Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode(RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

Table4. 23 DM bit for the Operation Mode of LCD display

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

Table4. 24 RM bit for the access interface of GRAM

RM	Access Interface
0	System interface / VSYNC interface
1	RGB interface

Note: the register is set only through the system interface.
Note : A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

PTG1-0: Specify the scan mode of gate driver in non-display area.

Table4. 25 PTG bit setting

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

TRI: When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus Interface. When TRI=0, 8-bit bus interface mode is unselected.

DFM1-0: Specify the data format when TRI=1, for 8-bit bus interface or serial data transfer interface. DFM1-0=10, 262K color mode. DFM1-0=11, 65K color mode.

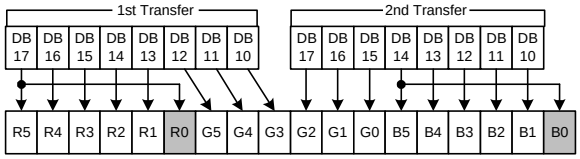
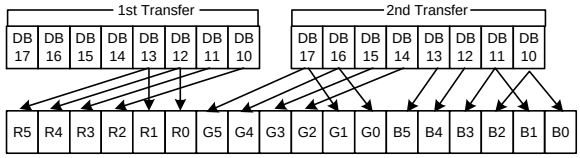
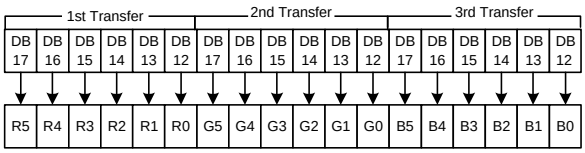
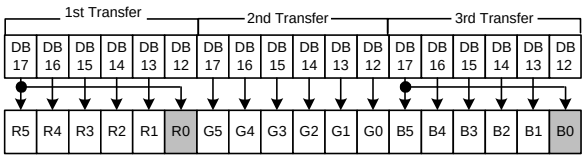
DFM1	DFM0	TRI	8-bit interfface data format
0	0	0	
0	1	0	
1	*	0	Ignore
0	*	1	Ignore
1	0	1	
1	1	1	

Figure4. 17 The setting of DFM and TRI (1)

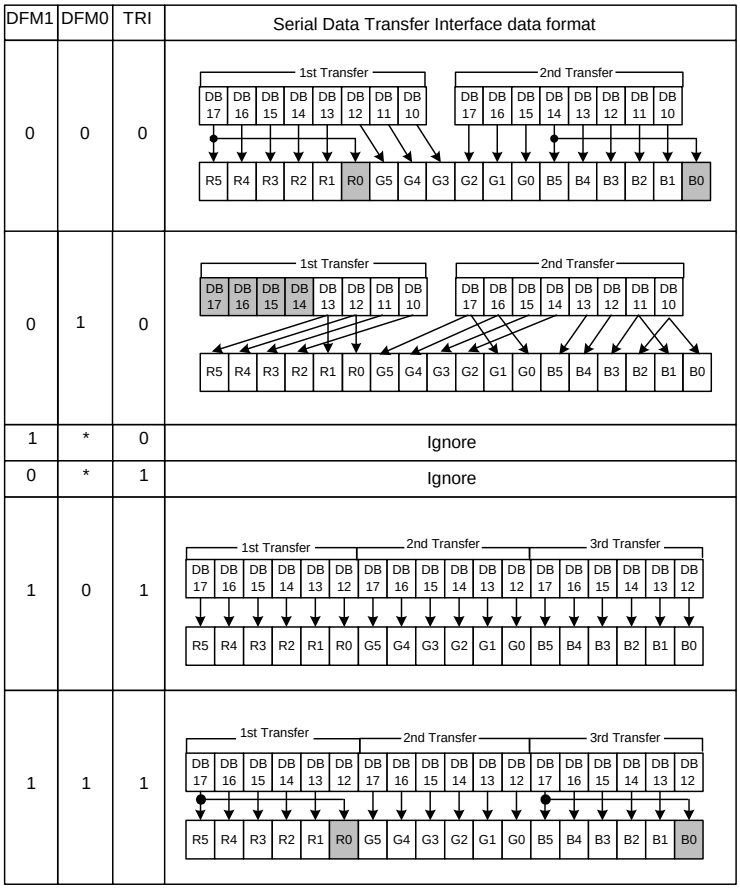


Figure4. 18 The setting of DFM and TRI (2)

4.13 Frame Cycle Control Register (R0Bh)

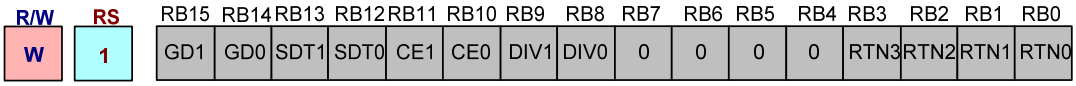


Figure4. 19 Frame Cycle Control Register (R0Bh)

RTN3-0: Set the 1-line period in a clock unit.

Table4. 26 RTN Bits and Clock Cycles

Clock cycles=1/internal operation clock frequency

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Line
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
:	:	:	:	:
1	1	0	1	29
1	1	1	0	30
1	1	1	1	31

DIV1-0: The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

Table4. 27 DIV Bits and Clock Frequency

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL+BP+FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

CE1-0: CE period can be set with CE1-0.

Table4. 28 CE Bits for Equalized Period

CE1	CE 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock cycle	8 clock cycles
1	0	2 clock cycles	16 clock cycles
1	1	3 clock cycles	24 clock cycles

SDT1-0: Set delay amount from falling edge of the gate output signal for the source outputs.

Table4. 29 SDT Bits for Source Output Delay

SDT1	SDT0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	1 clock cycle	8 clock cycles
0	1	2 clock cycles	16 clock cycles
1	0	3 clock cycles	24 clock cycles
1	1	4 clock cycles	32 clock cycles

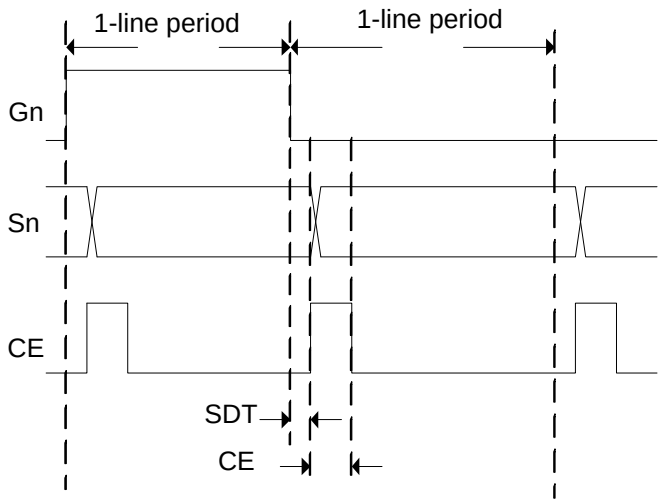


Figure4. 20 Equalized Period and Source Output Delay

GD1-0: Set amount of non-overlap for the gate output.

Table4. 30 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulse

GD 1	GD 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (source clock: DOTCLK)
0	0	0 clock cycle	0 clock cycle
0	1	4 clock cycles	32 clock cycles
1	0	6 clock cycles	48 clock cycles
1	1	8 clock cycles	64 clock cycles

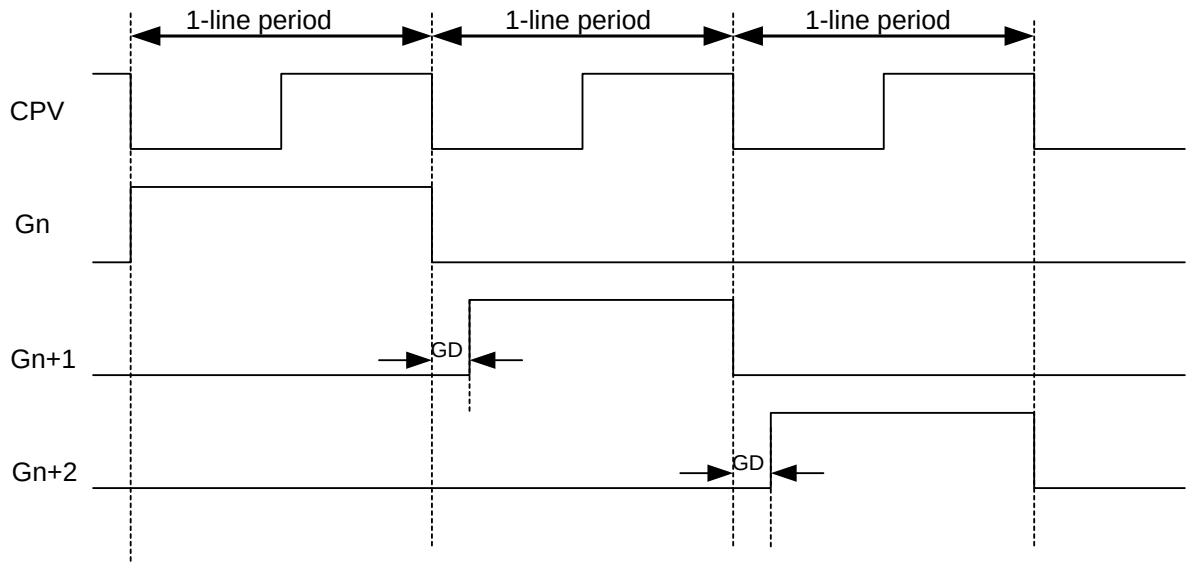


Figure4. 21 Non-overlap Time between Two Adjacent Gate Output Pulse

Table4. 31 Clock Source for Interface Mode

Interface mode	Clock Source
System interface mode	R-C oscillator
RGB interface more	DOTCLK
VSYNC interface mode	R-C oscillator

4.14 Power Control Register 3 (R0Ch)

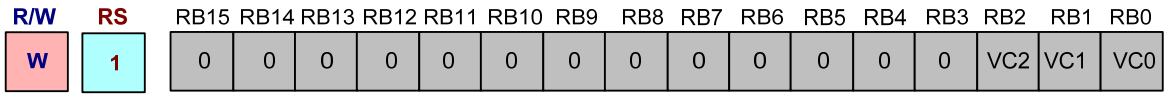


Figure4. 22 Power Control Register 2 (R0Ch)

VC2-0: Set the reference voltage of VGAM1OUT and VCI1 by adjusting the rate of VCI.

Table4. 32 VC Settings and Internal Reference Voltage

VC2	VC1	VC0	Internal reference voltage (REGP) of VGM1OUT and VCI1
0	0	0	VCI
0	0	1	0.92 x VCI
0	1	0	0.87 x VCI
0	1	1	0.83 x VCI
1	0	0	0.76 x VCI
1	0	1	0.73 x VCI
1	1	0	0.68 x VCI
1	1	1	Hi-z

4.15 Power Control Register 4 (R0Dh)

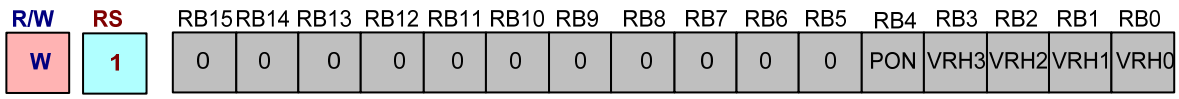


Figure4. 23 Power Control Register 3 (R0Dh)

VRH3-0: Set the magnification of amplification for VGAM1OUT voltage. (VCOM, reference voltage for grayscale voltage) It allows magnify the amplification of REGP from 1.38 to 1.83 times.

Table4. 33 VRH Bits and VGAM1OUT Voltage

VRH3	VRH2	VRH1	VRH0	VGAM1OUT Voltage
0	0	0	0	REGP x 1.33 times
0	0	0	1	REGP x 1.45 times
0	0	1	0	REGP x 1.55 times
0	0	1	1	REGP x 1.65 times
0	1	0	0	REGP x 1.75 times
0	1	0	1	REGP x 1.80 times
0	1	1	0	REGP x 1.85 times
0	1	1	1	Stopped
1	0	0	0	REGP x 1.900 times
1	0	0	1	REGP x 2.175 times
1	0	1	0	REGP x 2.325 times
1	0	1	1	REGP x 2.475 times
1	1	0	0	REGP x 2.625 times
1	1	0	1	REGP x 2.700 times
1	1	1	0	REGP x 2.775 times
1	1	1	1	Stopped

Notes: Adjust VC2-0 and VRH3-0 so that the VGAM1OUT voltage is lower than 5.0 V.
Note: Set the VC and VRH bits so that VGAM1OUT is less than (VLCD-0.5)V

PON: ON/OFF the operation of step-up circuit 3. PON = 0 is to stop and PON = 1 to start operation.

4.16 Power Control Register 5 (0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure4. 24 Power Control Register 4 (R0Eh)

VCM4-0: Set the VCOMH voltage (voltage of higher side when VCOM is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VGAM1OUT voltage. When VCM4-0 = “11111”, stop the internal volume adjustment and adjust the VCOMH with external resistance from VCOMR.

Table4. 34 VCM4-0 Bits and VCOMH Voltage

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VGAM1OUT x 0.40
0	0	0	0	1	VGAM1OUT x 0.42
0	0	0	1	0	VGAM1OUT x 0.44
:	:	:	:	:	:
0	1	1	1	0	VGAM1OUT x 0.68
0	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister),
1	0	0	0	0	VGAM1OUT x 0.70
1	0	0	0	1	VGAM1OUT x 0.72
1	0	0	1	0	VGAM1OUT x 0.74
:	:	:	:	:	:
1	1	1	0	0	VGAM1OUT x 0.94
1	1	1	0	1	VGAM1OUT x 0.96
1	1	1	1	0	VGAM1OUT x 0.98
1	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister),

Notes: Adjust VGAM1OUT and VCM4-0 so that the VCOMH voltage is lower than VGAM1OUT.

VDV4-0: Sets the amplification factors for VCOM and Vgoff while VCOM AC drive is being performed. It is possible to setup from 0.6 to 1.23 times of VGAM1OUT. When VCOMG = 0, the setup is invalid.

Table4. 35 VDV4-0 Bits and VCOM Amplitude

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VGAM1OUT x 0.60
0	0	0	0	1	VGAM1OUT x 0.63
0	0	0	1	0	VGAM1OUT x 0.66
0	0	0	1	1	VGAM1OUT x 0.69
:	:	:	:	:	:
0	1	1	0	0	VGAM1OUT x 0.96
0	1	1	0	1	VGAM1OUT x 0.99
0	1	1	1	0	VGAM1OUT x 1.02
0	1	1	1	1	Inhibition
1	0	0	0	0	VGAM1OUT x 1.05
1	0	0	0	1	VGAM1OUT x 1.08
1	0	0	1	0	VGAM1OUT x 1.11
1	0	0	1	1	VGAM1OUT x 1.14
1	0	1	0	0	VGAM1OUT x 1.17
1	0	1	0	1	VGAM1OUT x 1.20
1	0	1	1	0	VGAM1OUT x 1.23
1	0	1	1	1	Inhibition
1	1	--	--	--	

Notes: Adjust VGAM1OUT and VDV4-0 so that the VCOM and Vgoff amplitudes are lower than 6.0V.

VCOMG: When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ -VCI +0.5V). When VCOMG = 0, VCOML voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, when VCOMG = 0, setting of the VDV4-0 is invalid. In this case, adjustment of VCOM/Vgoff A/C amplitude must be adjust with VCOMH using VCM4-0.

4.17 Gate Scan Posistion Register (R0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

Figure4. 25 Gate Scan Posistion Register (R0Fh)

SCN4-0: Set the scanning starting position of the gate driver.

Table4. 36 SCN bits and Scanning Start Position for Gate Driver

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G160	G1	G160
0	0	0	0	1	G9	G152	G17	G144
0	0	0	1	0	G17	G144	G33	G128
0	0	0	1	1	G25	G136	G49	G112
0	0	1	0	0	G33	G128	G65	G96
0	0	1	0	1	G41	G120	G81	G80
0	0	1	1	0	G49	G112	G97	G64
0	0	1	1	1	G57	G104	G113	G48
0	1	0	0	0	G65	G96	G129	G32
0	1	0	0	1	G73	G88	G145	G16
0	1	0	1	0	G81	G80	G2	G159
0	1	0	1	1	G89	G72	G18	G143
0	1	1	0	0	G97	G64	G34	G127
0	1	1	0	1	G105	G56	G50	G111
0	1	1	1	0	G113	G48	G66	G95
0	1	1	1	1	G121	G40	G82	G79
1	0	0	0	0	G129	G32	G98	G63
1	0	0	0	1	G137	G24	G114	G47
1	0	0	1	0	G145	G16	G130	G31
1	0	0	1	1	G153	G8	G146	G15

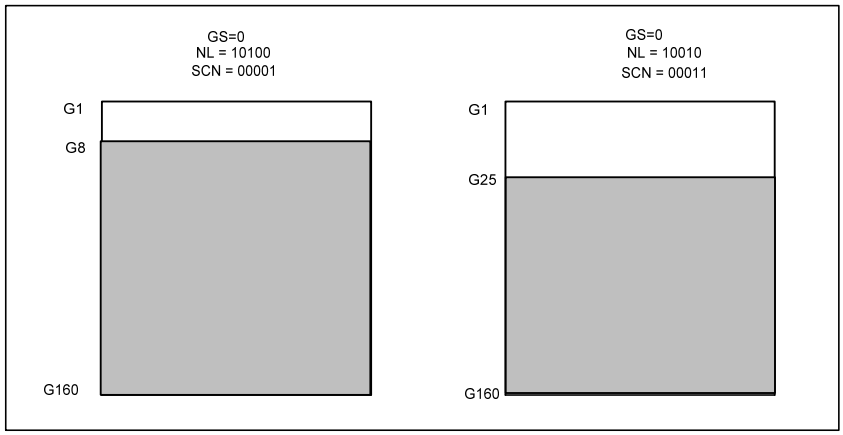


Figure4. 26 SCN bits and Scanning Start Position for Gate Driver

Note: Don't set NL, SCN over the end position of gate line (G160)
Note: Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 160.

4.18 CP/WM 18/16-bit Selection Register (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F

Figure4. 27 CP/WM 18/16-bit Selection Register (R10h)

F: Set the CP/WM to 18/16-bit mode.

Table4. 37 F bit

F	CP/WM
0	Set the CP/WM to 16 bit mode
1	Set the CP/WM to 18 bit mode

4.19 Vertical Scroll Control Register (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure4. 28 Vertical Scroll Control Register (R11h)

VL7–0: Specify the amount of scrolling line from 0 to 160 in the display to enable smooth vertical scrolling. If GRAM address mapping would exceed “9Fxx”H, GRAM address mapping would restart from “00xx”H after the data in “9Fxx”H of GRAM being displayed. The display-start line (VL7–0) is valid only when VLE1 = 1 or VLE2 = 1. The display-start line is fixed to zero when VLE2-1 = 00. (VLE1 is the 1st display window vertical-scroll enable bit, and VLE2 is the 2nd display window vertical-scroll enable bit.)

Table4. 38 VL bits and Scrolling Length

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Length
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
:	:	:	:	:		:	:	:
1	0	0	1	1	1	0	1	157 lines
1	0	0	1	1	1	1	0	158 lines
1	0	0	1	1	1	1	1	159 lines

4.20 First Display Window Driving Position Register (R14h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	SS 17	SS 16	SS 15	SS 14	SS 13	SS 12	SS 11	SS 10

Figure4. 29 First Screen Driving Position Register (R14h)

SS17–0: Specify the driving start position for the first display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver.

SE17–0: Specify the driving end position for the first display window in a line unit. The LCD driving is performed to the 'setting value + 1' gate driver. See the Partial-Screen Display Function section for details.

4.21 Second Display Window Driving Position Register (R15h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	SS 27	SS 26	SS 25	SS 24	SS 23	SS 22	SS 21	SS 20

Figure4. 30 Second Screen Driving Position Register (R15h)

SS27–0: Specify the driving start position for the second display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver. The second display window is driven when SPT = 1.

SE27–0: Specify the driving end position for the second display window in a line unit. The LCD driving is performed to the ' setting value + 1' gate driver.

Note: Ensure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤9Fh. For details, see the Partial Screen Display Function section.

4.22 Horizontal RAM Address Position Register (R16h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HAE 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0

Figure4. 31 Horizontal RAM Address Position Register (R44h)

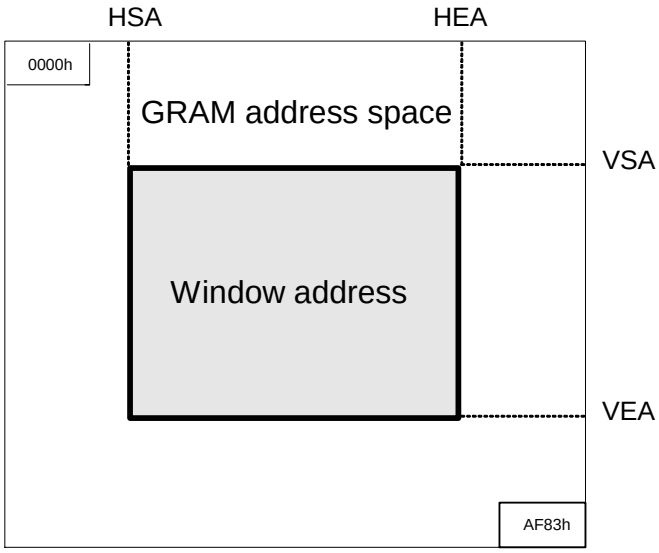
HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA7-0.Ensure that “00”h ≤HSA7-0 ≤HEA7-0 ≤”7F”h.

4.23 Vertical RAM Address Position Register (R17h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure4. 32 Vertical RAM Address Position Register (R45h)

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA7-0 to the address specified by VEA7-0. Ensure that "00"h ≤VSA7-0 ≤VEA7-0 ≤"9F"h



Window address setting range
"00"h ≤HSA7-0 ≤HEA7-0 ≤"7F"h
"00"h ≤VSA7-0 ≤VEA7-0 ≤"9F"h

Figure4. 33 Window Address Setting Range

Note1. The window address range must be within the GRAM address space.
Note2. Data are written to GRAM in four-words when operating in high speed mode so dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

4.24 16-bit RAM Write Data Mask Register (R20h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure4. 34 16-bit RAM Write Data Mask Register (R20h)

WM15–0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. The GRAM cannot be accessed in standby mode. When 16-/8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

4.25 RAM Address Register (R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure4. 35 RAM Address Register (R21h)

AD15–0: Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

Table4. 39 GRAM address mapping

AD15-AD0	GRAM Setting
“0000” h – “007F” h	Bitmap data for G1
“0100” h – “017F” h	Bitmap data for G2
“0200” h – “027F” h	Bitmap data for G3
:	:
“9D00” h – “9D7F” h	Bitmap data for G158
“9E00” h – “9E7F” h	Bitmap data for G159
“9F00” h – “9F7F” h	Bitmap data for G160

4.26 Write Data Register (R22h)

R/W	RS		RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1		WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
			PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
		RGB-I/F mode:	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure4. 36 Write Data Register (R22h)

WD17–0 : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

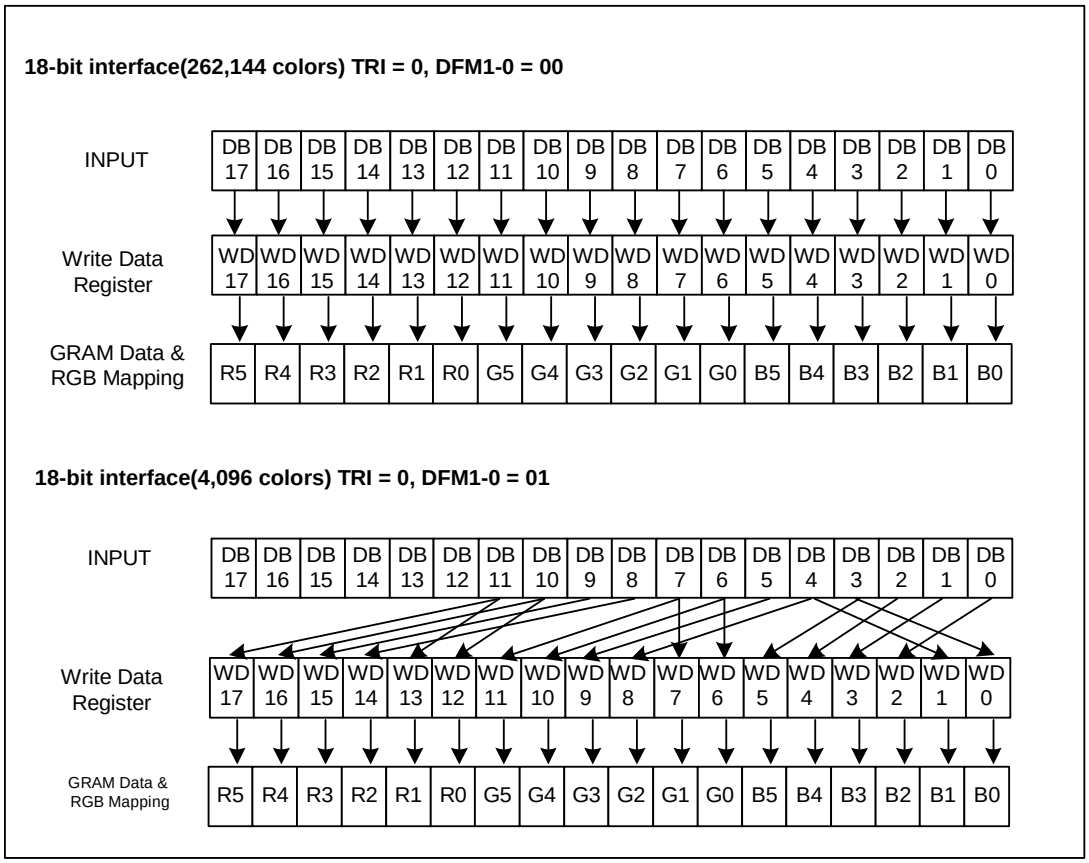


Figure4. 37 Bit Mapping of One Pixel Data: Input Data (18-bit Interface) Written to GRAM through Write Data Register

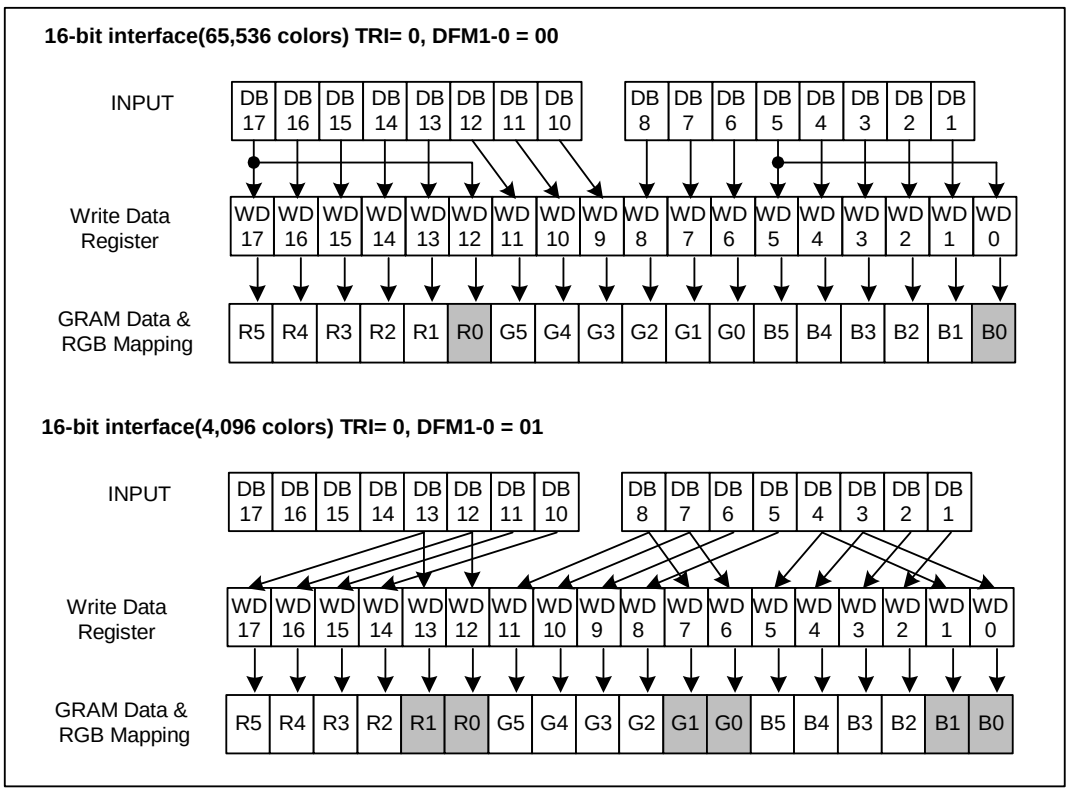


Figure4. 38 Bit Mapping of One Pixel Data: Input Data (16-bit Interface) Written to GRAM through Write Data Register

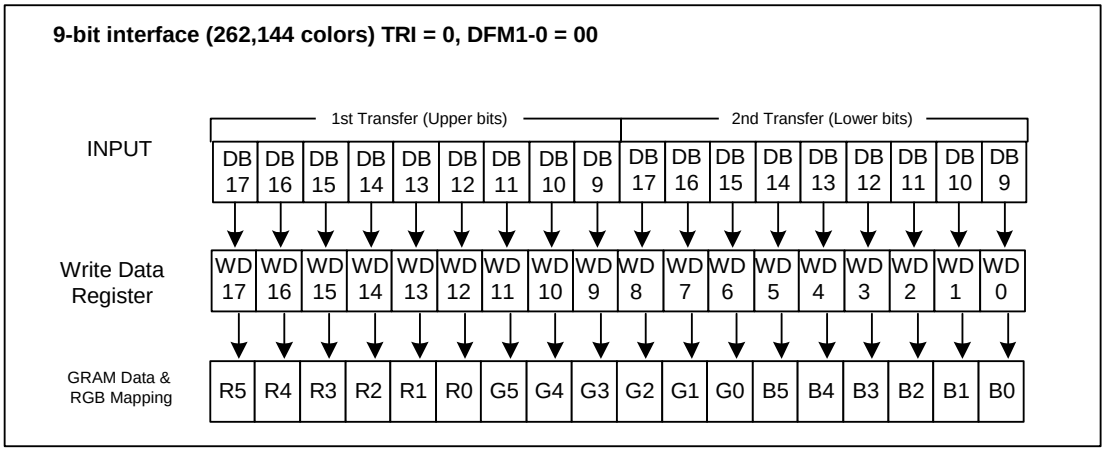
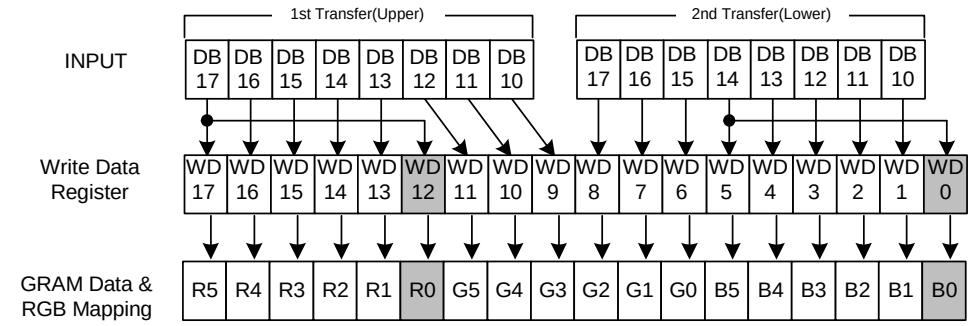
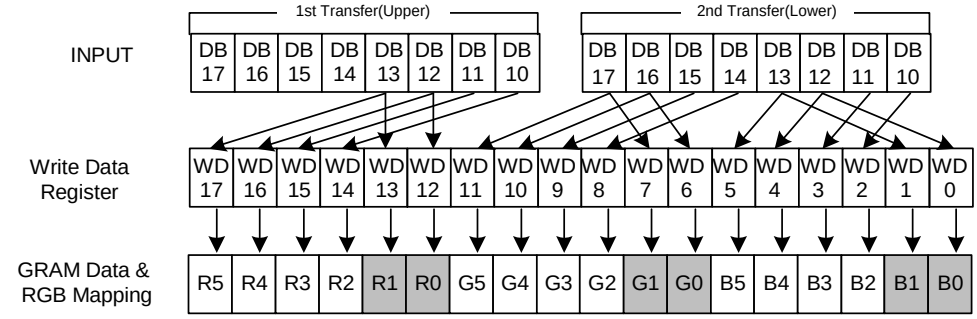


Figure4. 39 Bit Mapping of One Pixel Data: Input Data (9-bit Interface) Written to GRAM through Write Data Register

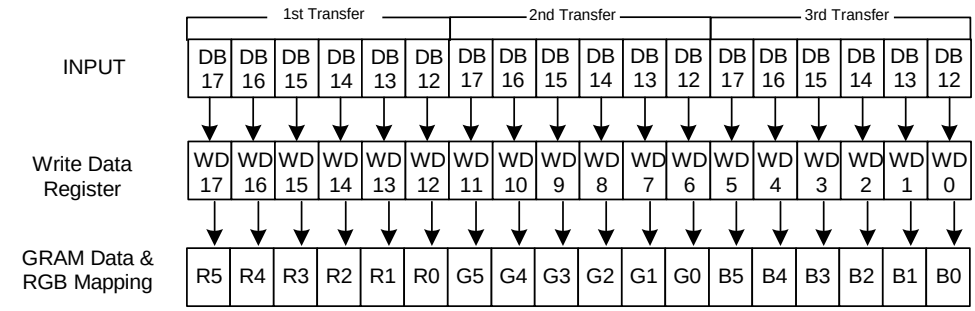
8-bit interface (65,536 colors) TRI = 0, DFM1-0 = 00



8-bit interface (262,144 colors) TRI =1, DFM1-0 = 10



8-bit interface (4,096 colors) TRI =0, DFM1-0 = 01



8-bit interface (65,536 colors) TRI =1, DFM1-0 = 11

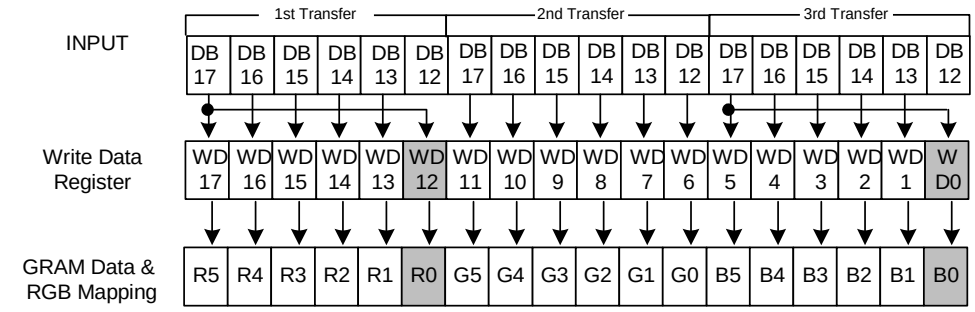


Figure4. 40 Bit Mapping of One Pixel Data: Input Data (8-bit Interface) Written to GRAM through Write Data Register

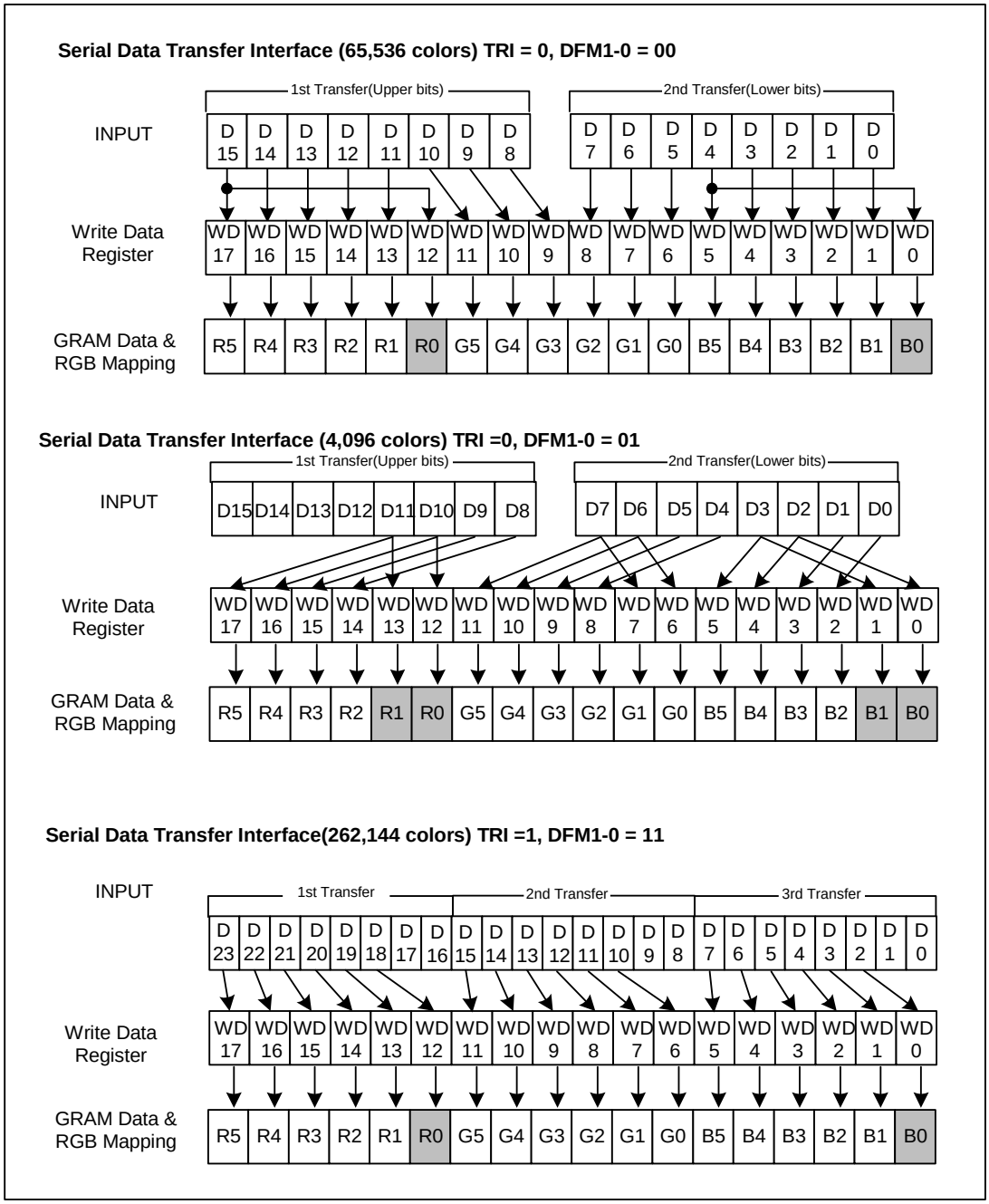
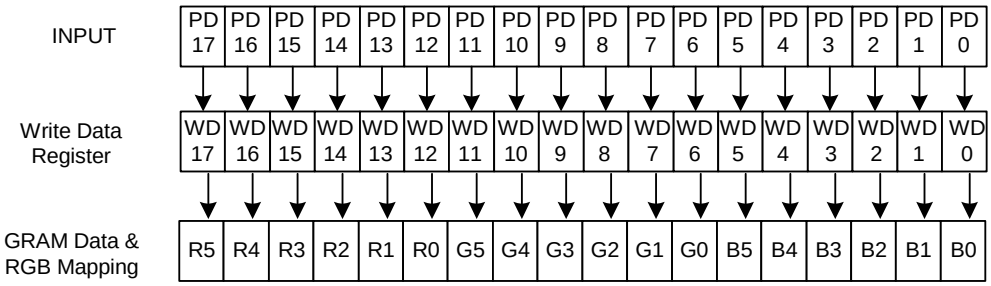


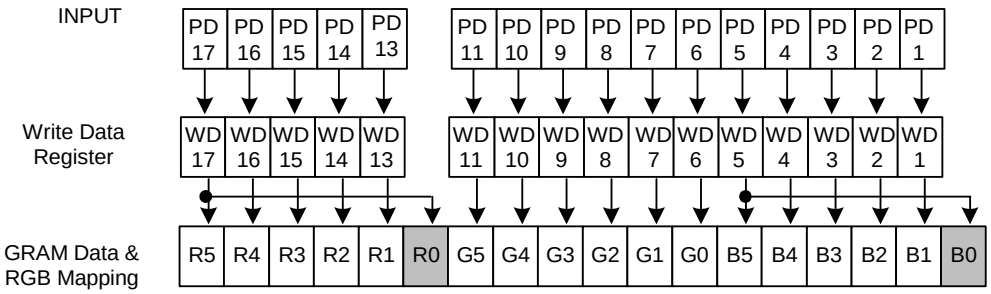
Figure4. 41 Bit Mapping of One Pixel Data: Input Data (Serial Data Transfer interface) Written to GRAM through Write Data Register

18-bit RGB interface (262,144 colors)



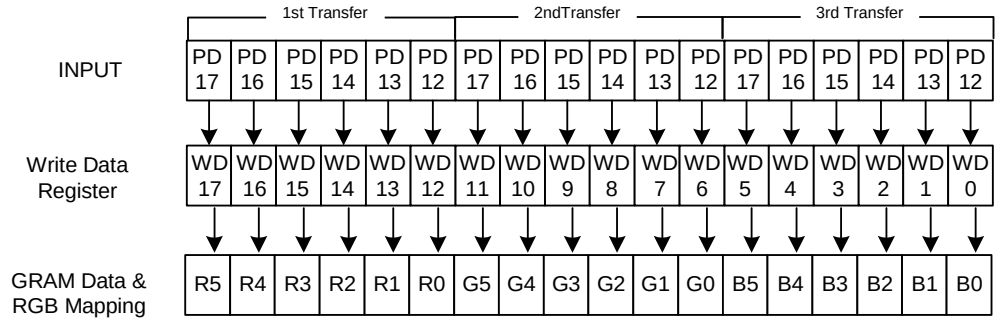
Set the index register when writing data through an RGB interface.

16-bit RGB interface (65,563 colors)



Set the index register when writing data through an RGB interface.

6-bit RGB interface (262,144 colors)



Set the index register when writing data through an RGB interface.

Figure4. 42 Bit Mapping of One Pixel Data: Input Data (18/16/6-bit RGB Interface) Written to GRAM through Write Data Register

4.27 Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure4. 43 Read Data Register (R22h)

RD17–0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

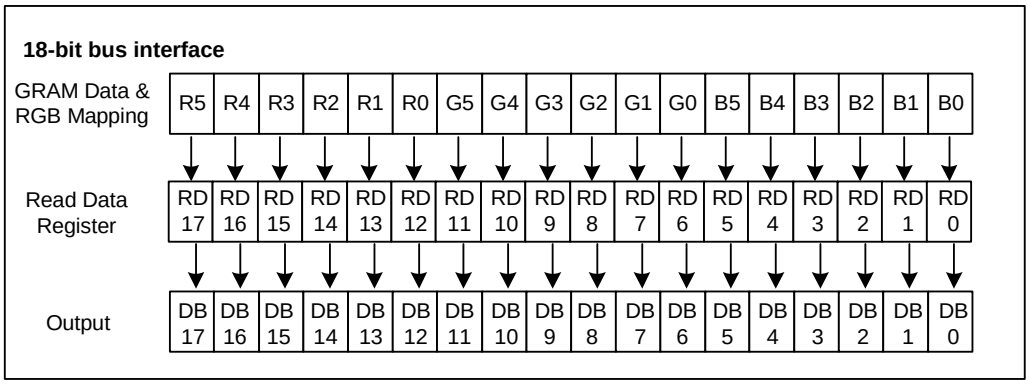


Figure4. 44 Output Data Read from GRAM through Read Data Register in 18-bit Interface Mode

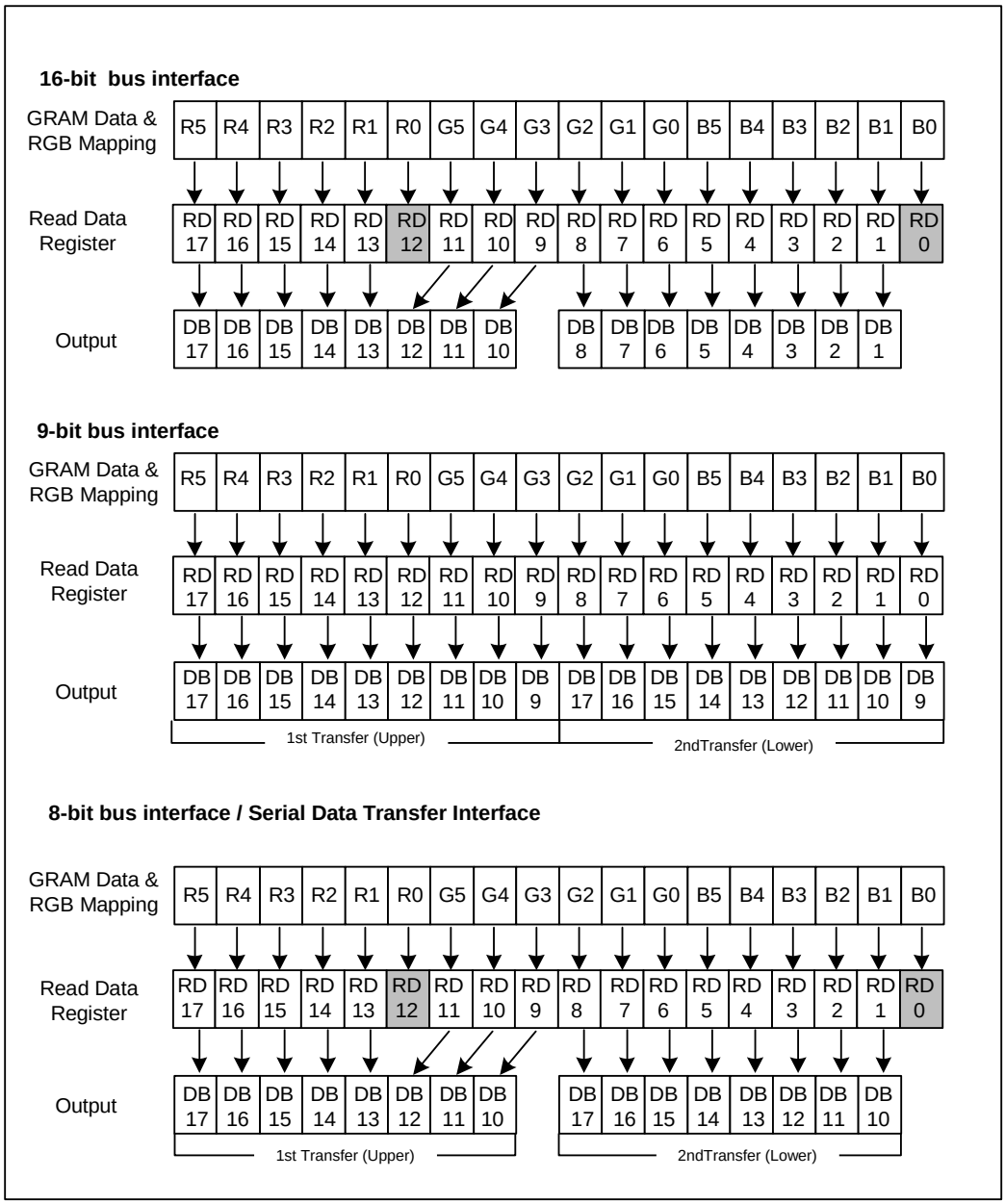


Figure4. 45 Output Data Read from GRAM through Read Data Register in 16- /9- /8-bit Interface Mode

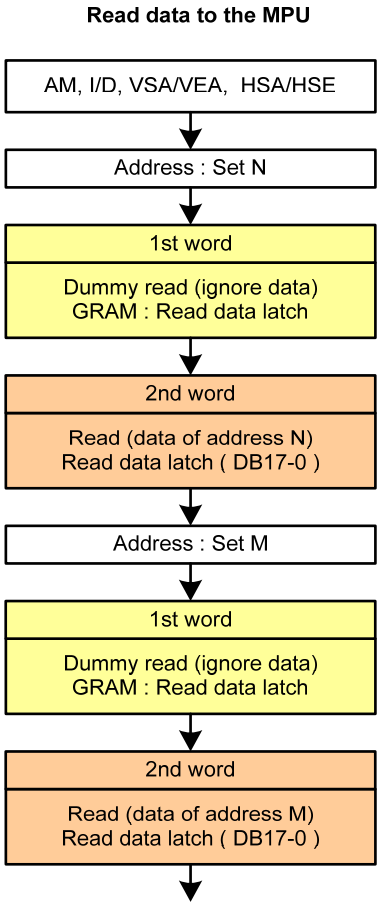


Figure4. 46 Flow Chart of GRAM Read Data

4.28 18-bit RAM Write Data Mask Register 1 (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	0	0	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure4. 47 18-bit RAM Write Data Mask Register 1 (R23h)

4.29 18-bit RAM Write Data Mask Register 2 (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	WM 17	WM 16	WM 15	WM 14	WM 13	WM 12

Figure4. 48 18-bit RAM Write Data Mask Register 2 (R24h)

WM17–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM17 = 1, this bit mask the write data of RB17 and does not write to the GRAM. Similarly, the WM16~WM0 bit masks the write data of RB16~RB0 in a bit unit. For details, see the Graphics Operation Function section.

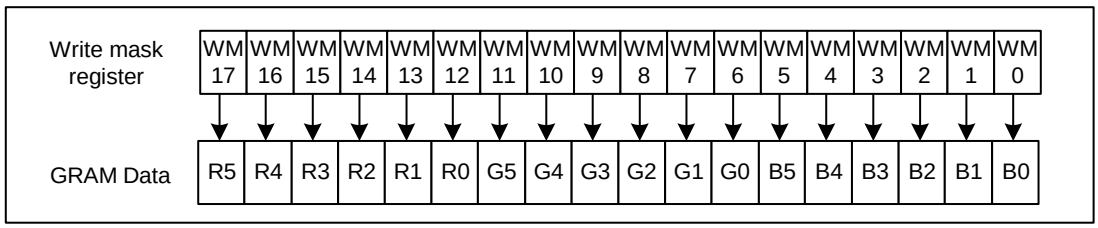


Figure4. 49 GRAM Write Data Mask

Note: Please set R10h to 0001h, when WM17~0 in using.

4.30 18-bit Compare Register 1 (R25h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	CP 11	CP 10	CP 9	CP 8	CP 7	CP 6	0	0	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

Figure4. 50 18-bit Compare Register 1(R25h)

4.31 18-bit Compare Register 2 (R26h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	CP 17	CP 16	CP 15	CP 14	CP 13	CP 12

Figure4. 51 18-bit Compare Register 2 (R26h)

CP17–0: Set the 18-bits compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

Note: Please set R10h to 0001h, when CP17~0 in using.

4.32 Gamma Control Register Set

Gamma Control Register 1~10 (R30h~R3Bh)

	R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R30	W	1	0	0	0	0	0	MP1 (2)	MP1 (1)	MP1 (0)	0	0	0	0	0	MP0 (2)	MP0 (1)	MP0 (0)
R31	W	1	0	0	0	0	0	MP3 (2)	MP3 (1)	MP3 (0)	0	0	0	0	0	MP2 (2)	MP2 (1)	MP2 (0)
R32	W	1	0	0	0	0	0	MP5 (2)	MP3 (1)	MP5 (0)	0	0	0	0	0	MP4 (2)	MP4 (1)	MP4 (0)
R33	W	1	0	0	0	0	0	CP1 (2)	CP1 (1)	CP1 (0)	0	0	0	0	0	CP0 (2)	CP0 (1)	CP0 (0)
R34	W	1	0	0	0	0	0	MN1 (2)	MN1 (1)	MN1 (0)	0	0	0	0	0	MN0 (2)	MN0 (1)	MN0 (0)
R35	W	1	0	0	0	0	0	MN3 (2)	MN3 (1)	MN3 (0)	0	0	0	0	0	MN2 (2)	MN2 (1)	MN2 (0)
R36	W	1	0	0	0	0	0	MN5 (2)	MN5 (1)	MN5 (0)	0	0	0	0	0	MN4 (2)	MN4 (1)	MN4 (0)
R37	W	1	0	0	0	0	0	CN1 (2)	CN1 (1)	CN1 (0)	0	0	0	0	0	CN0 (2)	CN0 (1)	CN0 (0)
R3A	W	1	0	0	0	OP1 (4)	OP1 (3)	OP1 (2)	OP1 (1)	OP1 (0)	0	0	0	0	OP0 (3)	OP0 (2)	OP0 (1)	OP0 (0)
R3B	W	1	0	0	0	ON1 (4)	ON1 (3)	ON1 (2)	ON1 (1)	ON1 (0)	0	0	0	0	ON0 (3)	ON0 (2)	ON0 (1)	ON0 (0)

MP5-0 (2:0): Gamma adjustment register for positive polarity output
CP1-0 (2:0): Gamma gradient adjustment register for positive polarity output
MN5-0 (2:0): Gamma adjustment register for negative polarity output
CN1-0 (2:0: Gamma gradient adjustment register for negative polarity output
OP0 (3:0)/OP1 (4:0): Amplification adjustment resistor for positive polarity output
ON0 (3:0)/ON1 (4:0): Amplification average adjustment resistor for negative polarity output

Figure4. 52 Gamma Control Register 1~10 (R30h~R3Bh)

4.33 Initialization

Output Pin Initialization

1. Driver output pins (Source outputs): Output VSSD level
2. Driver output pins (Gate outputs): Output VGH level
3.Oscillator output pin (OSC2): Output oscillation signal

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SS = 0, GS = 0, SM = 0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Power control 1 (BT2-0 = 000, DC02-10 = 000, AP2–0 = 000: LCD power off, SLP = 0,STB = 0: Standby mode off)
5. Entry mode set (BGR = 0, HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move)
6. Display control 1 (PT1-0 = 00, VLE2-1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL =0: 262144-color mode, REV = 0, D1–0 = 00: Display off)
7. Display control 2 (VSPL = 0, HSPL = 0, DPL = 0, EPL = 0, FP3-0 = 1000, ISC3-0 = 0000, BP3-0 = 0000)
8. Power control 2 (DCM1-0 = 00, DC12-10 = 000, DK = 0, SAP2–0 = 100)
9. External display interface control 1 (TRI = 0, DFM1-0 = 00, PTG1-0 = 00, RM = 0: System interface, DM1-0 = 00: internal clock operation, RIM1-0 = 00: 18-bit RGB interface)
10. Frame cycle control (GD1-0 = 00, SDT1-0 = 00, CE1-0 = 00: No equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clocks in 1-line period)
11. Power control 3 (VC2-0 = 000)
12. Power control 4 (PON=0,VRH3-0 = 0000)
13. Power control 4 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
14. Gate scan starting position (SCN4-0 = 00000)
15. Vertical scroll (VL7–0 = 00000000)
16. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
17. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
18. Horizontal RAM address position (HEA7-0 = 10000011, HSA7-0 = 00000000)
19. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
20. RAM write data mask (WM15–0 = 000000000000000h: No mask)
21. RAM address set (AD15–0 = 0000h)
22. RAM write data mask (WM17–0 = 00000000000000000h: No mask)
23. Gamma control
    (MP02-00 = 000, MP12-10 = 000, MP22-20 = 000, MP32-30 = 000,
    MP42-40 = 000, MP52-50 = 000, CP02-00 = 000, CP12-10 = 000)
    (MN02-00 = 000, MN12-10 = 000,MN22-20 = 000, MN32-30 = 000,
    MN42-40 = 000, MN52-50 = 000, CN02-00 = 000, CN12-10 = 000)
    (OP03-00 =0000,OP14-10=00000,ON03-00=0000,ON14-10=0000)

4.34 Reset Function

The HX8310-A is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from the MPU can be accepted. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

GRAM Data Initialization:

It must be initialized by software while display is off (D1-0=00)

5. Power Generation

5.1 Specification

The specification of power supply circuit and pins connection are shown as following table:

Table5. 1 The adoptability of Capacitor

Pins connection	Recommended voltage	Capacity
TVCOMHI, TVCOMLI, TMAG	6V	0.1 µF (B characteristics)
VDDD, VGAM1OUT, VCIOUT, VCLC, VCOMH, VCOML, C11A/B, C12A/B	6V	1 µF (B characteristics)
VLCD, C21A/B, C22A/B	10V	1 µF
VGHC, VGLC	25V	1 µF

Table5. 2 The adoptability of Schottkey diode

Pins connection	Feature
VSSD – VGL (VCI – VGH)	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

Table5. 3 The adoptability of Variable resistor

Pins to connect	Resusabce
VCOMR	> 200 kΩ

5.2 Power supply Circuit

The power supply circuit of HA8310A preside over generating supply voltages to drive a LCD panel.

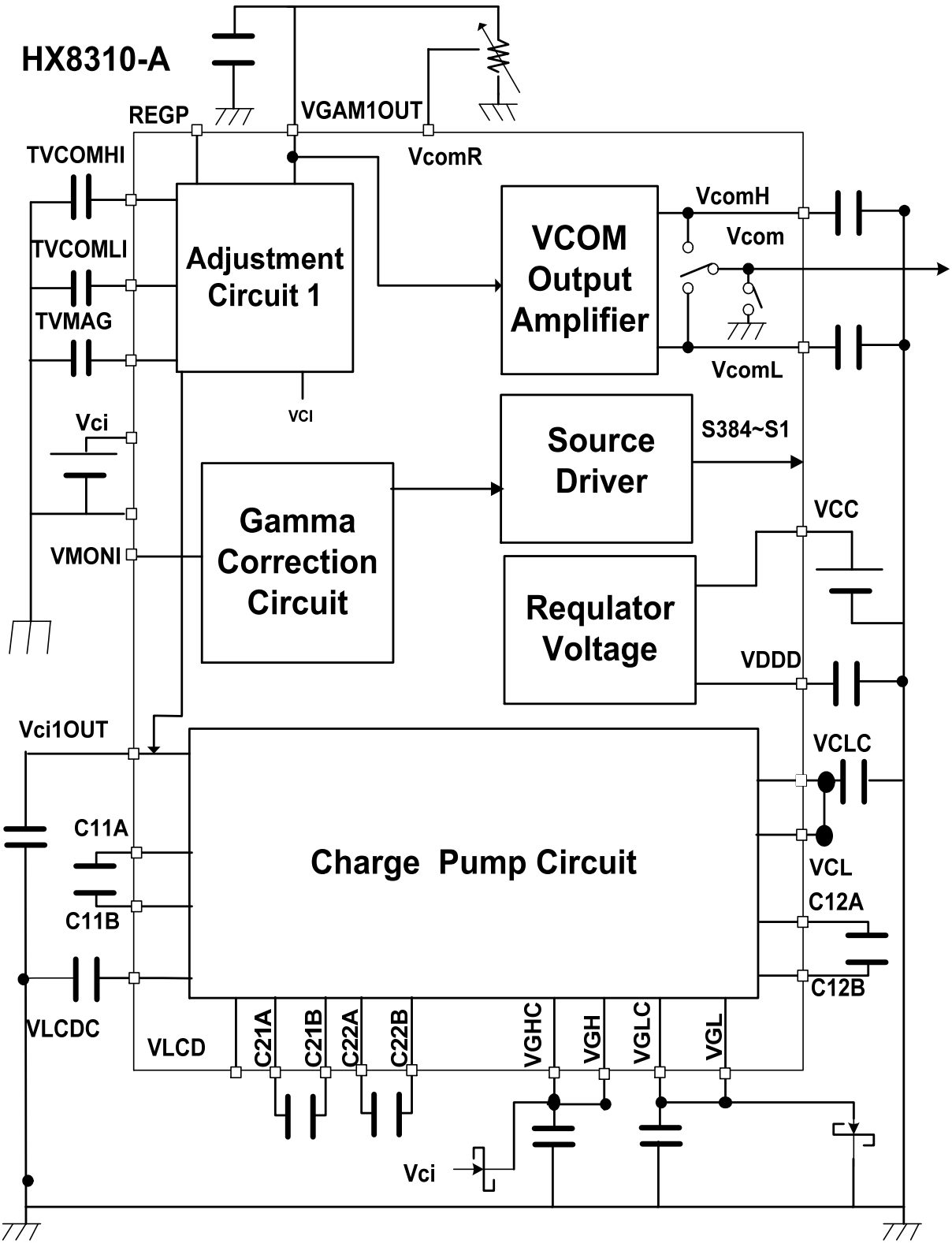


Figure5. 1 Block Diagram of Power Supply Circuit

5.3 Voltage Setting

The voltage setting pattern diagram of the HX8310-A illustrates as following figure. The outputs of VLCDC, VGH, VGL, VCL are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption. When the VCOM voltage alternating cycle is high, the large current will be consumed.

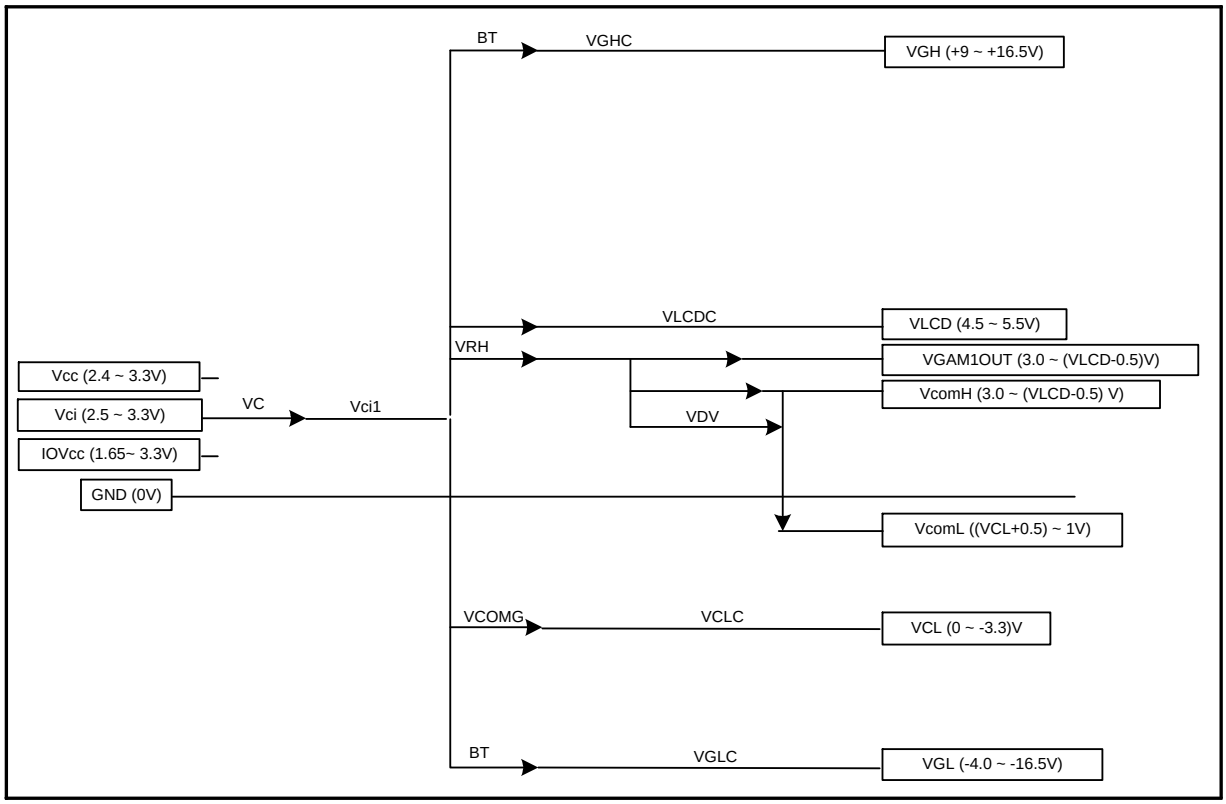


Figure5. 2 Voltage setting diagram

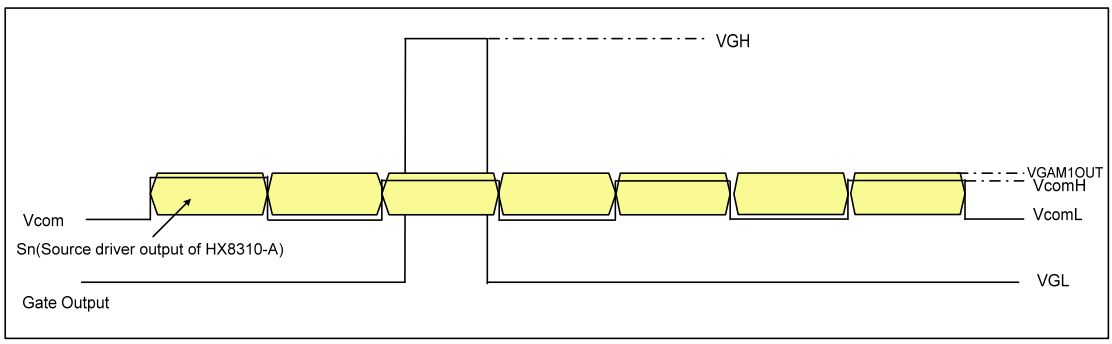


Figure5. 3 The applied voltage of the TFT display

5.4 Register Setting

The following are the sequences of register setting flow that applied to the HA8310-A driving the TFT display.

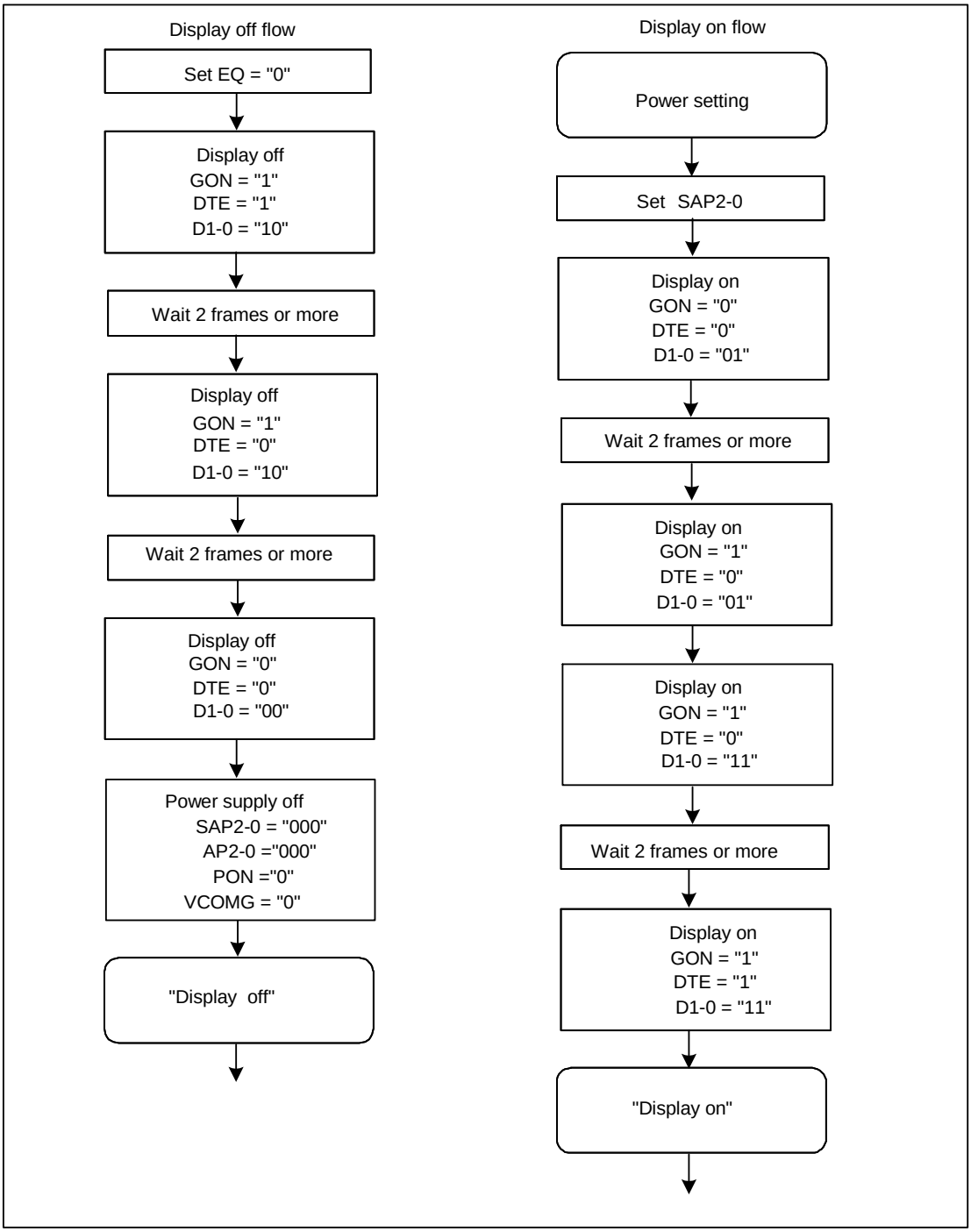


Figure5. 4 Register setting sequence

Standby mode and Sleep Mode setting flow:

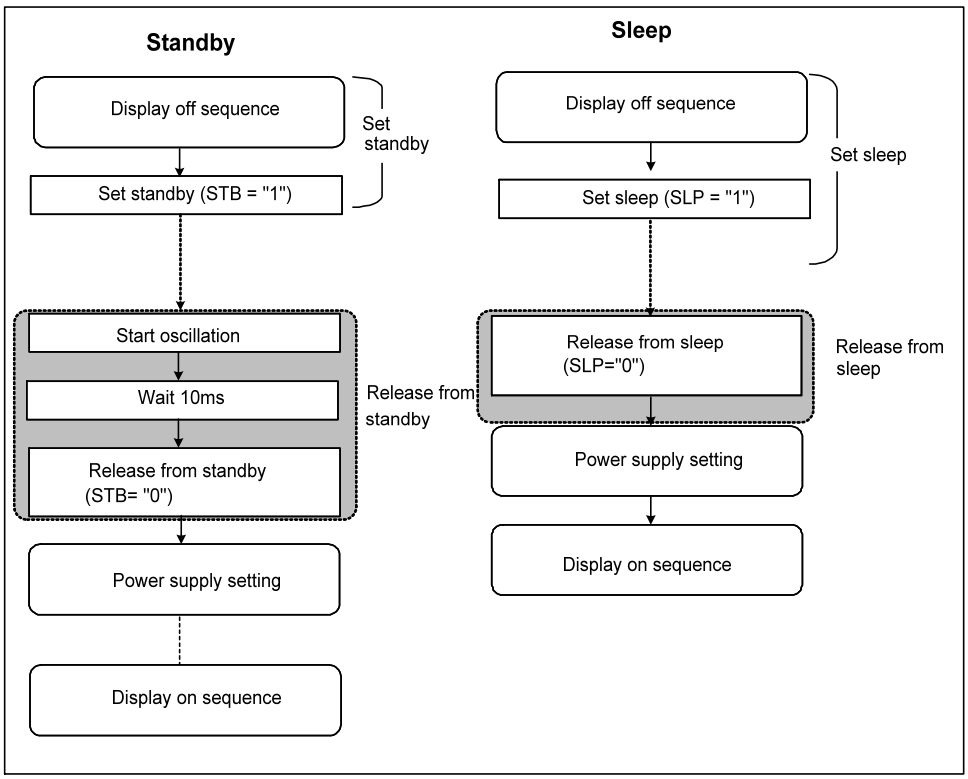


Figure5. 5 Standby Mode and Sleep Mode Setting Sequence

5.5 Power Supply Setting

The power supply setting sequence of the HX8310-A is as below.

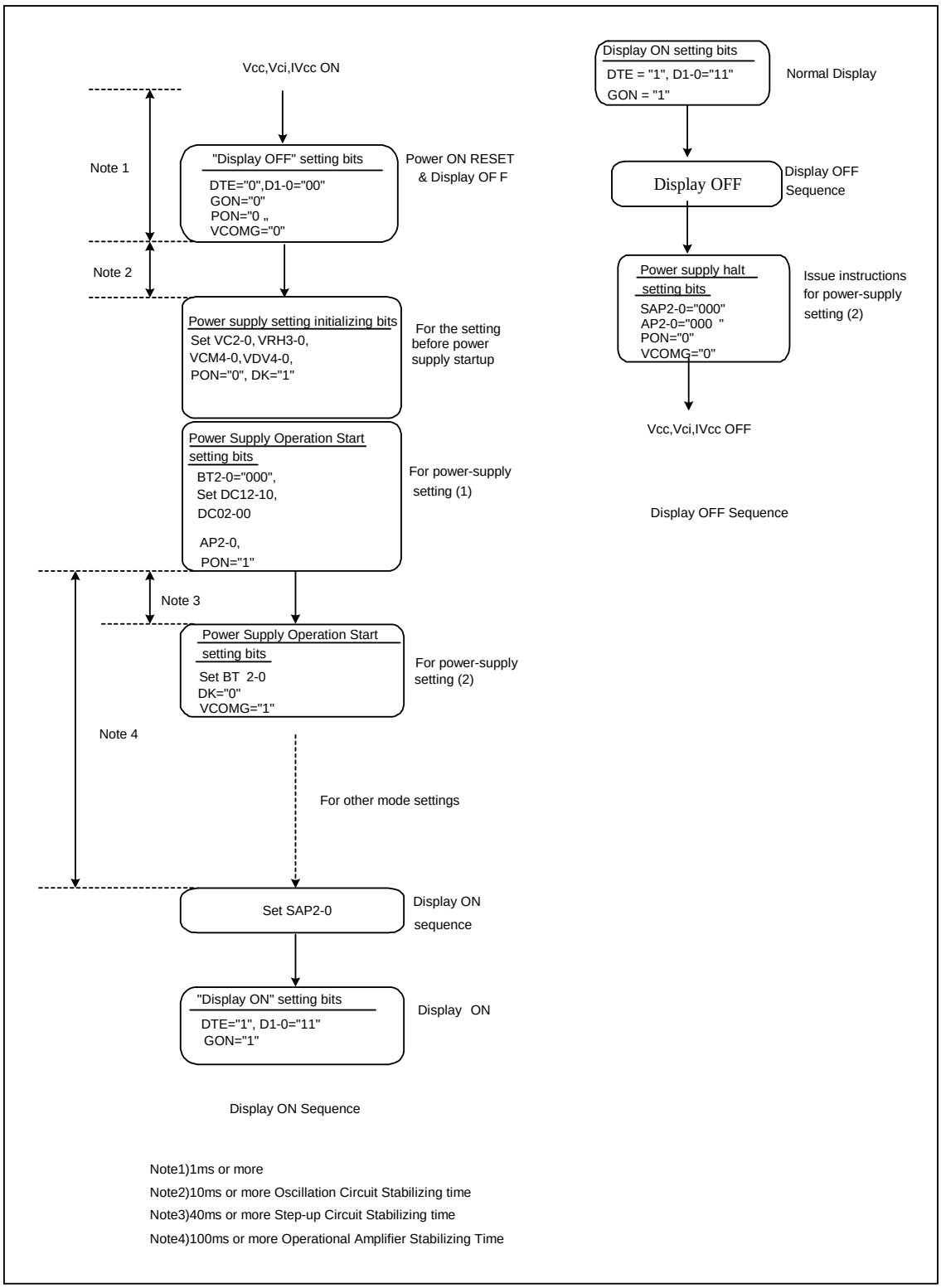


Figure5. 6 Power Supply Setting Flow

6. Electrical Characteristic

6.1 Absolute Maximum Ratings

The absolute maximum ratings is list on Table 6.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Table 6. 1 Absolute Maximum Rating

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - VSSA	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	VLCD - VSSA	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	VSSA -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	VLCD - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - VSSA	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	VSSA - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC + 0.3	1
Operating temperature	Topr	˚C	-40 ~ + 85	8, 9
Storage temperature	Tstg	˚C	-55 ~ + 110	8, 9

Notes:
1. VCC, VSSD must be maintained
2. (High) (VCC=VCC) ≥ VSSD (Low), (High) IOVCC ≥ VSSD (Low).
3. Make sure (High) VCI ≥ VSSD (Low).
4. Make sure (High) VLCD ≥ ASSD (Low).
5. Make sure (High) VLCD ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85℃.
9. This temperature specifications apply to the TCP package

6.2 AC Characteristic

Table 6. 2 AC Characteristics (VCC = 1.8 ~ 3.3V , Ta = -40 ~ 85 °C)

Table 6.2. 1 Clock Characteristics (VCC = 1.8 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	f_{cp}	KHz	T.B.D	T.B.D	T.B.D	VCC= 1.8 ~ 3.3V
External clock duty ratio	Duty	%	T.B.D	T.B.D	T.B.D	VCC= 1.8 ~ 3.3V
External clock rise time	trcp	µs	-	-	T.B.D	VCC= 1.8 ~ 3.3V
External clock fall time	tfcp	µs	-	-	T.B.D	VCC= 1.8 ~ 3.3V
R-C oscillation clock	f_{OSC}	KHz	T.B.D	T.B.D	T.B.D	Rf = 200K ohm , VCC=3V

Table 6. 3 80-system Bus Interface Timing Characteristics

Table 6. 3. 1 Normal Write Mode (HWM = 0)/ (VCC = 1.8 ~ 2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCR}	ns	T.B.D	-	T.B.D	-
Write low-level pulse width		PW_{LW}	ns	T.B.D	-	-	T.B.D
Read low-level pulse width		PW_{LR}	ns	T.B.D	-	-	T.B.D
Write high-level pulse width		PW_{HW}	ns	T.B.D	-	-	T.B.D
Read high-level pulse width		PW_{HR}	ns	T.B.D	-	-	T.B.D
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	T.B.D	T.B.D
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	T.B.D	-	T.B.D	-
	Read (RS to NCS, RW_NRD)			T.B.D	-	-	-
Address hold time		t_{AH}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSW}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{H}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDR}	ns	--	-	T.B.D	T.B.D
Read data hold time		t_{DHR}	ns	T.B.D	-	-	T.B.D

Table 6. 3. 2 High-Speed Write Mode (HWM = 1) / (VCC = 1.8 ~ 2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCR}	ns	T.B.D	-	T.B.D	-
Write low-level pulse width		PW_{LW}	ns	T.B.D	-	-	T.B.D
Read low-level pulse width		PW_{LR}	ns	T.B.D	-	-	T.B.D
Write high-level pulse width		PW_{HW}	ns	T.B.D	-	-	T.B.D
Read high-level pulse width		PW_{HR}	ns	T.B.D	-	-	T.B.D
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	T.B.D	T.B.D
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	T.B.D	-	T.B.D	-
	Read (RS to NCS, RW_NRD)			T.B.D	-	-	-
Address hold time		t_{AH}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSW}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{H}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDR}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHR}	ns	T.B.D	-	-	T.B.D

Table 6. 3. 3 Normal Write Mode (HWM = 0) / (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCR}	ns	T.B.D	-	T.B.D	-
Write low-level pulse width		PW_{LW}	ns	T.B.D	-	-	T.B.D
Read low-level pulse width		PW_{LR}	ns	T.B.D	-	-	T.B.D
Write high-level pulse width		PW_{HW}	ns	T.B.D	-	-	T.B.D
Read high-level pulse width		PW_{HR}	ns	T.B.D	-	-	T.B.D
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	T.B.D	T.B.D
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	T.B.D	-	T.B.D	-
	Read (RS to NCS , RW_NRD)			T.B.D	-	-	-
Address hold time		t_{AH}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSW}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{H}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDR}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHR}	ns	T.B.D	-	-	T.B.D

Table 6. 3. 4 High-Speed Write Mode (HWM = 1) /(VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCR}	ns	T.B.D	-	T.B.D	-
Write low-level pulse width		PW_{LW}	ns	T.B.D	-	-	T.B.D
Read low-level pulse width		PW_{LR}	ns	T.B.D	-	-	T.B.D
Write high-level pulse width		PW_{HW}	ns	T.B.D	-	-	T.B.D
Read high-level pulse width		PW_{HR}	ns	T.B.D	-	-	T.B.D
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	T.B.D	T.B.D
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	T.B.D	-	T.B.D	-
	Read (RS to NCS, RW_NRD)			T.B.D	-	-	-
Address hold time		t_{AH}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSW}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{H}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDR}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHR}	ns	T.B.D	-	-	T.B.D

Table 6.4 Serial Data Transfer Interface Timing Characteristics

Table 6.4.1 (VCC=1.8~2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	T.B.D	-	T.B.D	-
	Read (transmitted)	t_{SCYC}	μs	T.B.D	-	T.B.D	-
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	T.B.D	-	T.B.D	-
	Read (transmitted)	t_{SCH}	ns	T.B.D	-	T.B.D	-
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	T.B.D	-	T.B.D	-
	Read (transmitted)	t_{SCL}	ns	T.B.D	-	T.B.D	-
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	T.B.D	T.B.D
Chip select set up time		t_{CSU}	ns	T.B.D	-	-	T.B.D
Chip select hold time		t_{CH}	ns	T.B.D	-	-	T.B.D
Serial input data set up time		t_{SISU}	ns	T.B.D	-	-	T.B.D
Serial input data hold time		t_{SIH}	ns	T.B.D	-	-	T.B.D
Serial output data set up time		t_{SOD}	ns	-	-	T.B.D	T.B.D
Serial output data hold time		t_{SOH}	ns	T.B.D	-	-	T.B.D

Table 6.4.2 (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	T.B.D	-	T.B.D	T.B.D
	Read (transmitted)	t_{SCYC}	μs	T.B.D	-	T.B.D	T.B.D
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	T.B.D	-	T.B.D	-
	Read (transmitted)	t_{SCH}	ns	T.B.D	-	T.B.D	-
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	T.B.D	-	T.B.D	-
	Read (transmitted)	t_{SCL}	ns	T.B.D	-	T.B.D	-
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	T.B.D	T.B.D
Chip select set up time		t_{CSU}	ns	T.B.D	-	-	T.B.D
Chip select hold time		t_{CH}	ns	T.B.D	-	-	T.B.D
Serial input data set up time		t_{SISU}	ns	T.B.D	-	-	T.B.D
Serial input data hold time		t_{SIH}	ns	T.B.D	-	-	T.B.D
Serial output data set up time		t_{SOD}	ns	-	-	T.B.D	T.B.D
Serial output data hold time		t_{SOH}	ns	T.B.D	-	-	T.B.D

Table 6. 5 RGB Interface Timing Characteristics

Table 6. 5.1 18-/16-bit Bus RGB Interface Mode, Normal Write Mode (HWM = 0) /(VCC=1.8~2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width	Write	PW_{EH}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EH}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width	Write	PW_{EL}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EL}	ns	T.B.D	-	T.B.D	-
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.2 18-/16-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1)/ (VCC=1.8~2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width	Write	PW_{EH}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EH}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width	Write	PW_{EL}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EL}	ns	T.B.D	-	T.B.D	-
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.3 18-/16-bit Bus RGB Interface Mode, Normal Write Mode (HWM = 0) / (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width		PW_{EL}	ns	T.B.D	-	-	T.B.D
		PW_{EL}	ns	T.B.D	-	-	T.B.D
Enable high-level pulse width		PW_{EH}	ns	T.B.D	-	-	T.B.D
		PW_{EH}	ns	T.B.D	-	-	T.B.D
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.4 18-/16-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1) / (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width		PW_{EH}	ns	T.B.D	-	-	T.B.D
		PW_{EH}	ns	T.B.D	-	-	T.B.D
Enable low-level pulse width		PW_{EL}	ns	T.B.D	-	-	T.B.D
		PW_{EL}	ns	T.B.D	-	-	T.B.D
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.5 6-bit Bus RGB Interface Mode, Normal Write Mode (HWM = 0) / (VCC=1.8~2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width	Write	PW_{EH}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EH}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width	Write	PW_{EL}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EL}	ns	T.B.D	-	T.B.D	-
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	--	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.6 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 1)/ (VCC=1.8~2.4V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width	Write	PW_{EH}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EH}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width	Write	PW_{EL}	ns	T.B.D	-	T.B.D	-
	Read	PW_{EL}	ns	T.B.D	-	T.B.D	-
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.7 6-bit Bus RGB Interface Mode, High-Speed Write Mode (HWM = 0)/ (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable low-level pulse width		PW_{EL}	ns	T.B.D	-	-	T.B.D
		PW_{EL}	ns	T.B.D	-	-	T.B.D
Enable high-level pulse width		PW_{EH}	ns	T.B.D	-	-	T.B.D
		PW_{EH}	ns	T.B.D	-	-	T.B.D
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	-	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

Table 6.5.8 6-bit Bus RGB Interface Mode,High-Speed Write Mode (HWM = 1) / (VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Enable cycle time	Write	t_{CYCE}	ns	T.B.D	-	T.B.D	-
	Read	t_{CYCE}	ns	T.B.D	-	T.B.D	-
Enable high-level pulse width		PW_{EH}	ns	T.B.D	-	-	T.B.D
		PW_{EH}	ns	T.B.D	-	-	T.B.D
Enable low-level pulse width		PW_{EL}	ns	T.B.D	-	-	T.B.D
		PW_{EL}	ns	T.B.D	-	-	T.B.D
Enable rise / fall time		t_{Er} , t_{Ef}	ns	-	-	T.B.D	T.B.D
Setup time(RS,E_NWR to NCS , E)		t_{ASE}	ns	T.B.D	-	-	T.B.D
Address hold time		t_{AHE}	ns	T.B.D	-	-	T.B.D
Write data set up time		t_{DSWE}	ns	T.B.D	-	-	T.B.D
Write data hold time		t_{HE}	ns	T.B.D	-	-	T.B.D
Read data delay time		t_{DDRE}	ns	--	-	T.B.D	T.B.D
Read data hold time		t_{DHRE}	ns	T.B.D	-	-	T.B.D

6.3 DC Charcateristic

Table 6. 6 (VCC = 1.8 ~ 3.3V , Ta = -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VCC= 1.8 ~ 3.3V	T.B.D	-	T.B.D	-
Input low voltage	V_{IL}	V	VCC= 1.8 ~ 3.3V	T.B.D	-	T.B.D	-
Output high voltage(1) (DB0-15 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	T.B.D	-	-	-
Output low voltage (DB0-15 Pins)	V_{OL1}	V	VCC= 1.8 ~ 2.4V I_{OL} = 0.1mA	-	-	T.B.D	-
			VCC= 2.4 ~ 3.3V I_{OL} = 0.1mA	-	-	T.B.D	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ VCC	T.B.D	-	T.B.D	-
Current consumption during normal operation (VCC – VSSD)	I_{OP}	µA	VCC=3.0V , Ta=25°C , f_{OSC} = 177KHz (176 Line) GRAM data = 0000h	-	T.B.D	T.B.D	-
Current consumption during standby mode (VCC – VSSD)	I_{ST}	µA	VCC=3V , Ta=25°C	-	T.B.D	T.B.D	-
LCD Drive Power Supply Current (VLCDC-VSSD)	I_{LCD}	µA	VCC=3V , VGAM1OUT=5.0V VLCDC=5.5V , f_{OSC} = 177KHz (160 line) , Ta=25°C, GRAM data = 0000h, REV=”0”, SAP=”001”, ON4-0=”0”, OP4-0=”0”, MP52-00=”0”, MN52-00=”0”, CP12-00=”0” CN12-00=”0	-	T.B.D	T.B.D	-
LCD Driving Voltage (VLCDC-VSSD)	VLCDC	V	-	T.B.D	-	T.B.D	-
Output voltage deviation		mV	-	-	T.B.D	-	-
Dispersion of the Average Output Voltage	V	mV	-	T.B.D	-	T.B.D	-

6.4 Clock Characteristics

Table 6. 7 Clock Characteristics (VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fOSC	kHz	Rf = 200kΩ, VCC = 3.0V	TBD	300	TBD

6.5 Reset Timing Characteristics

Table 6. 8 Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Timing diagram	Min.	Typ.	Max.
Reset low-level width	tRES	ms	Figure 6.6	1	-	-
Reset rise time	trRES	μs	Figure 6.6	-	-	10

6.6 LCD driver output Characteristics

Table 6.9 LCD Driver Output Characteristics

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Driver output delay time	tdd	μs	VCC=3V, VLCD=5.5V, VGAM1OUT=5.0V, RC oscillation: fosc =315kHz (160 lines), Ta=25°C REV=0, SAP=010, AP=010, 0N14-00=0, 0P14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF • when the level changes from a same grayscale level on all pins • Time to reach +/-35mV when VCOM polarity inverts	-	35	-

6.7 Timing Charcateristic

80-system Bus Operation

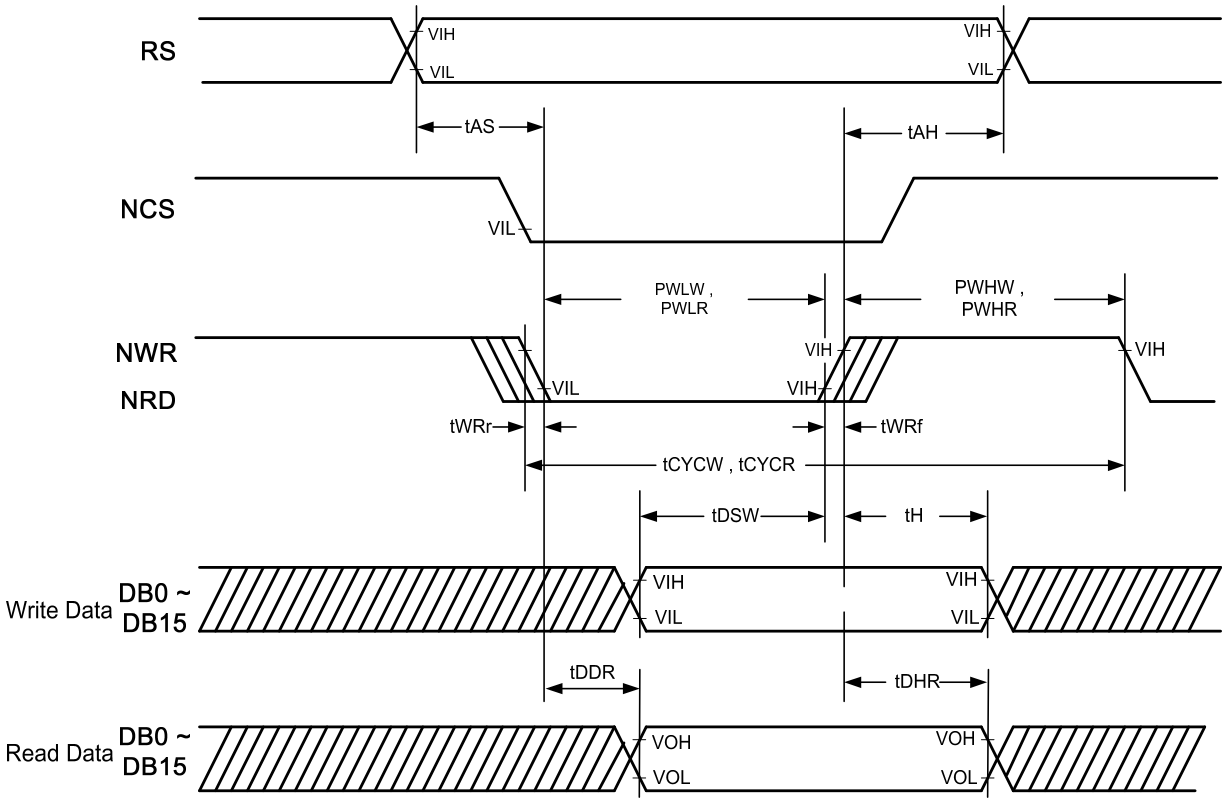


Figure6. 1 80-system Bus Timing

68-system Bus Operation

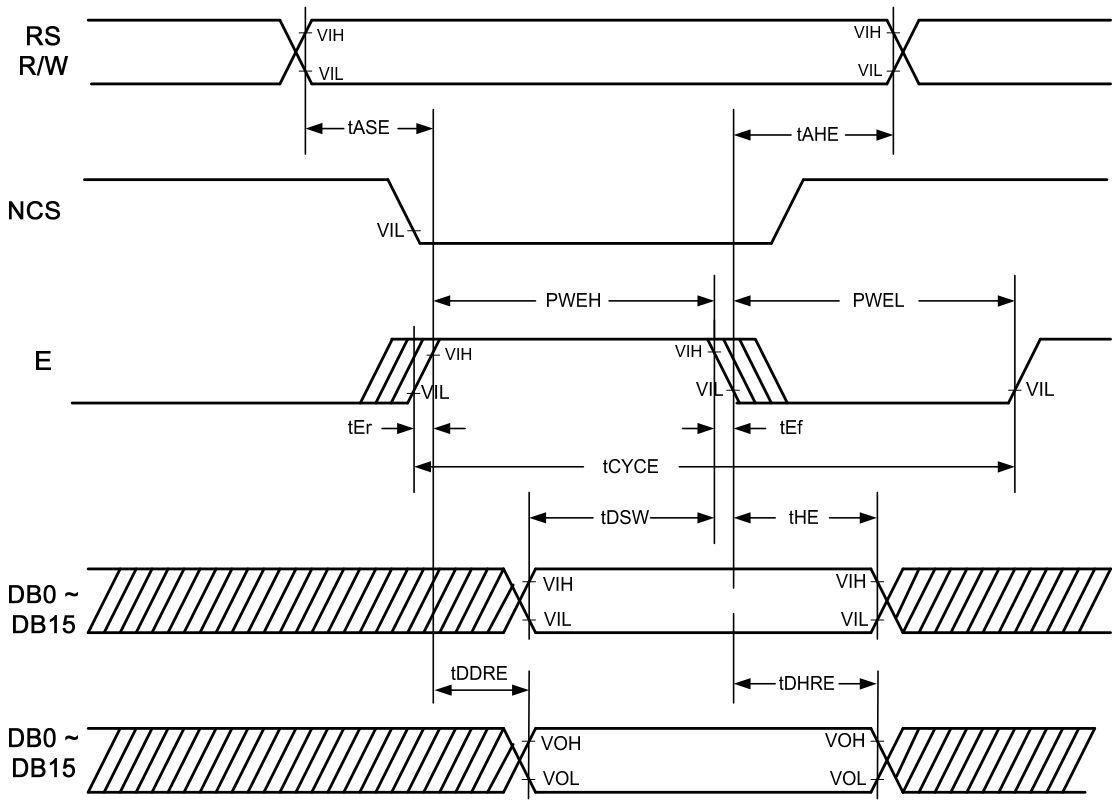


Figure6. 2 68-system Bus Operation

Clock Synchronized Serial Data Transfer Interface Operation

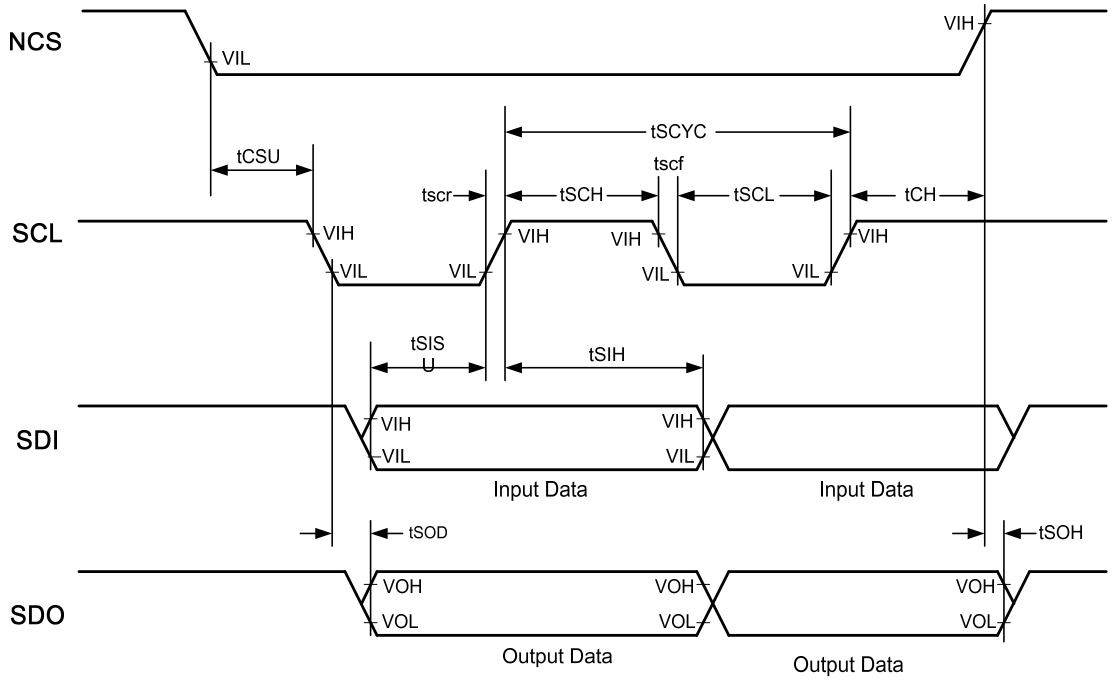


Figure6. 3 Clock Synchronized Serial Data Transfer Interface Timing

RGB Interface Operation

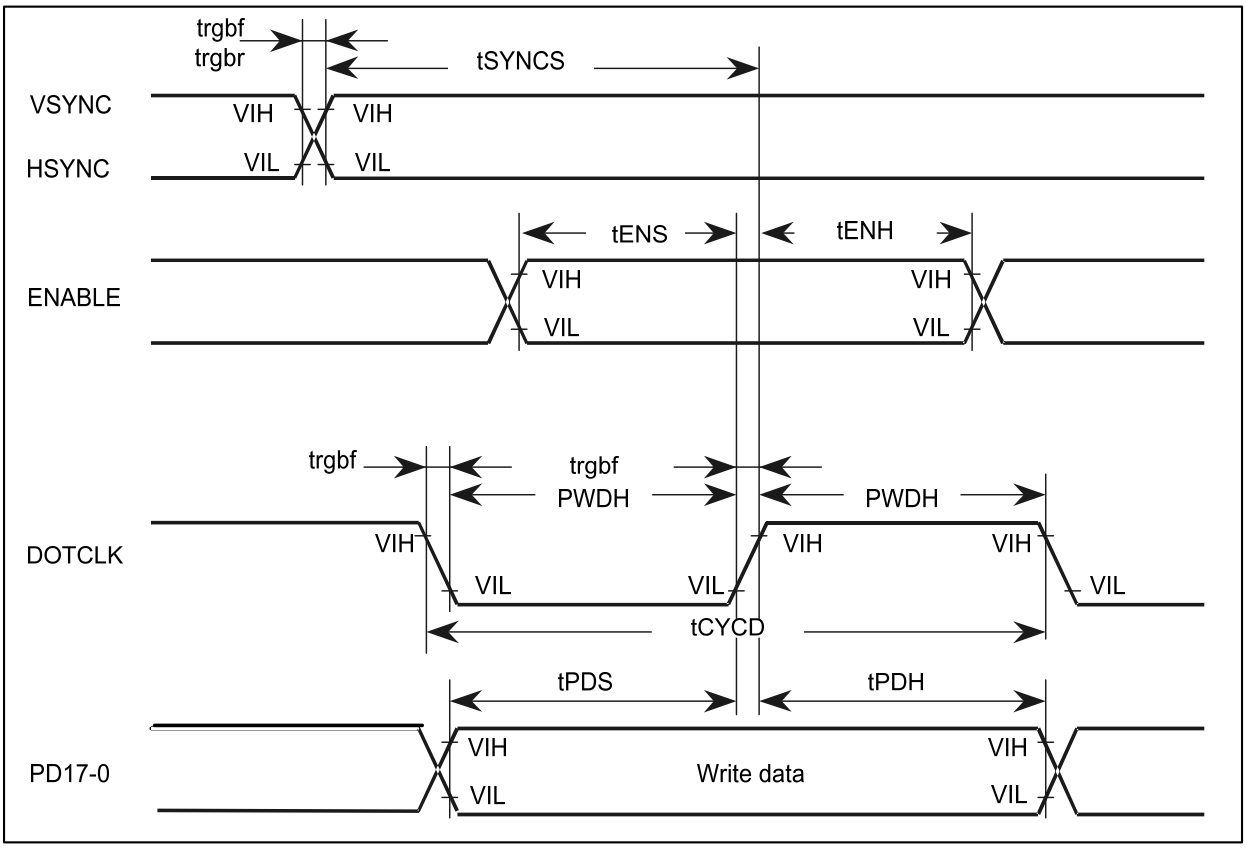


Figure6. 4 RGB Interface Operation

LCD Driving Output

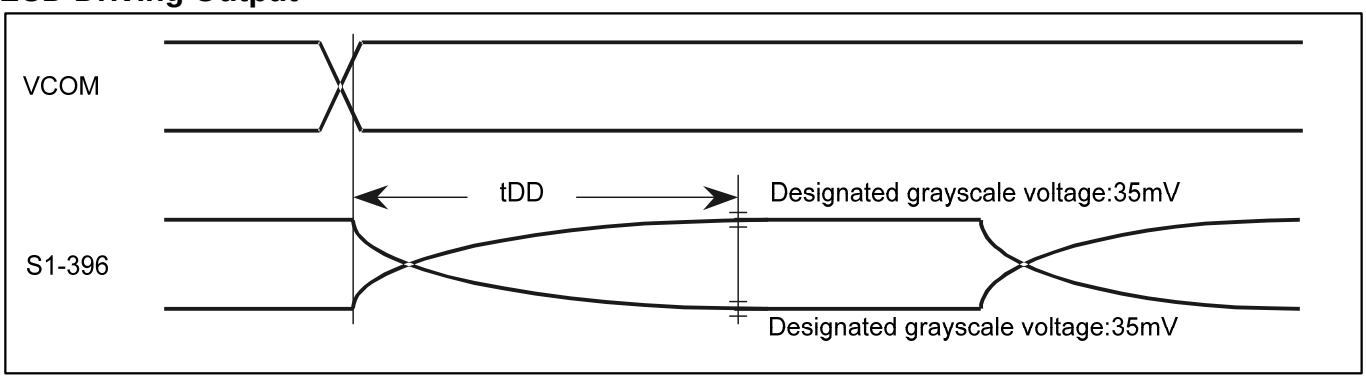


Figure6. 5 LCD Driving Output

Reset Operation

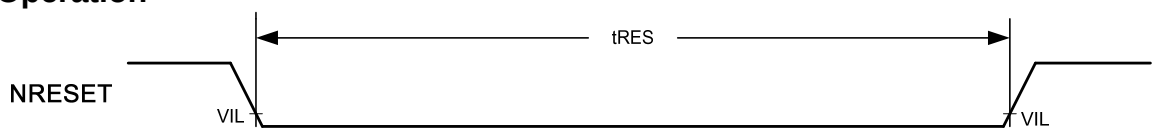


Figure6. 6 Reset Timing

7. System Configuration

7.1 System Diagram

The system configuration diagram illustrates as following:

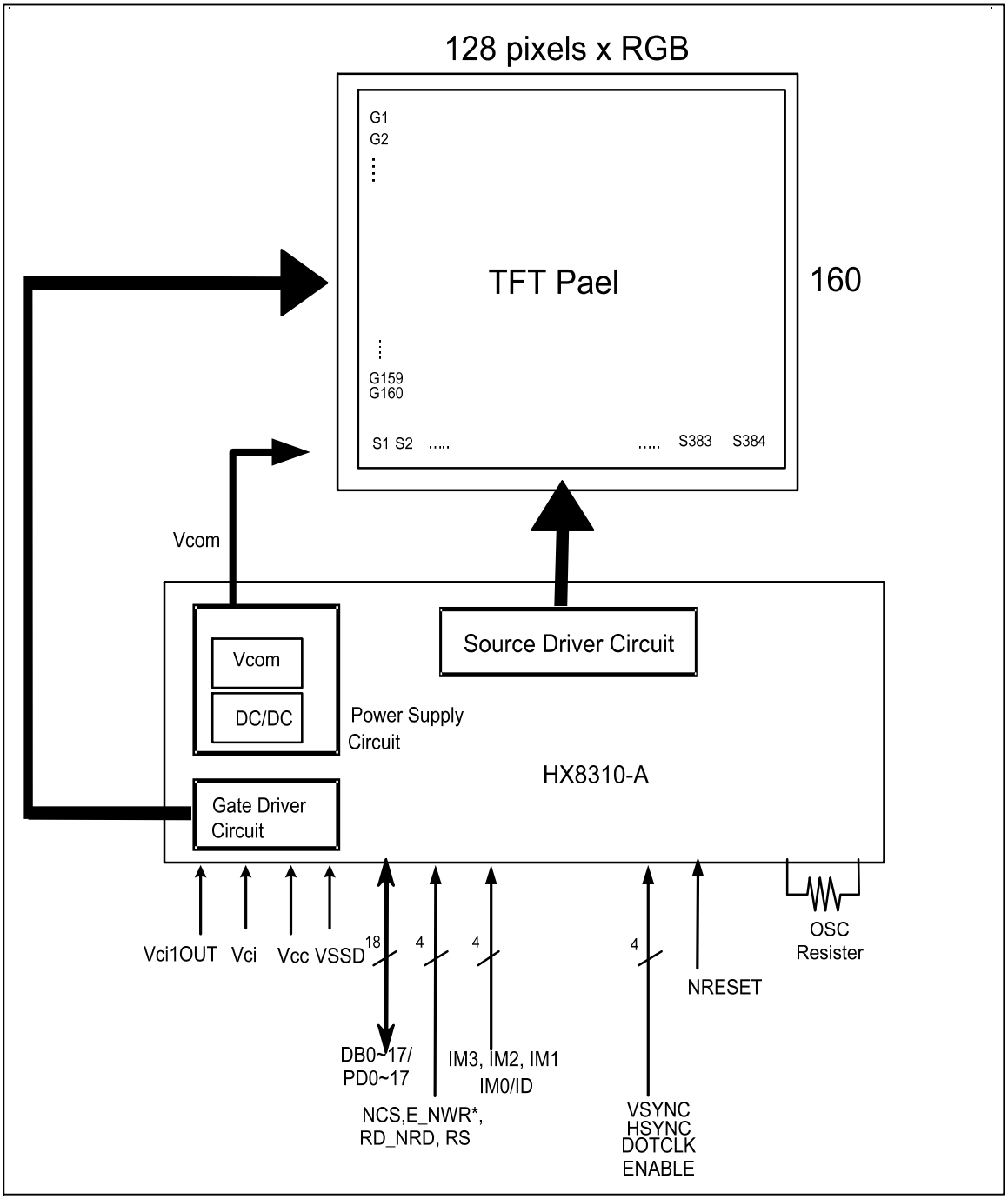
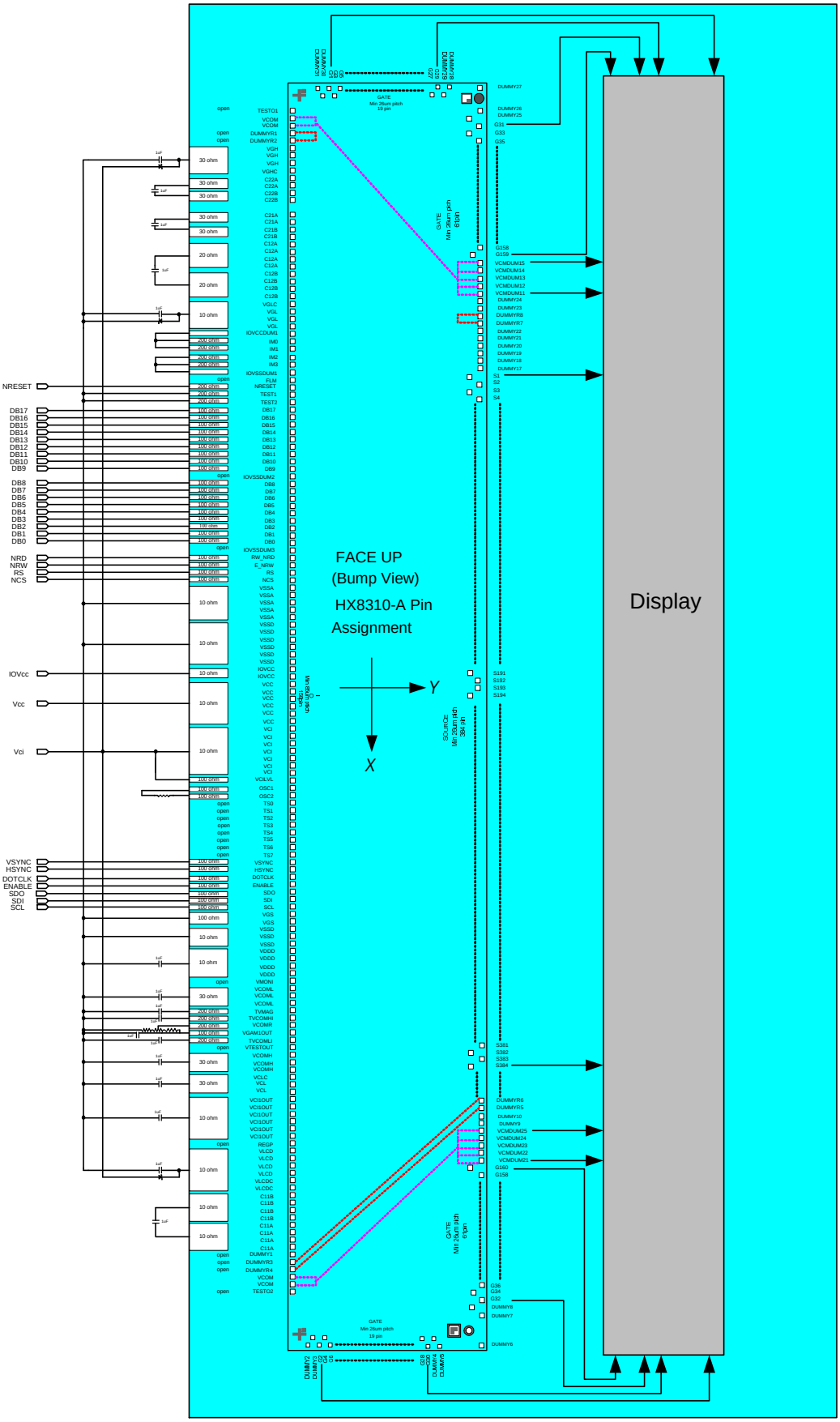


Figure7. 1 System Diagram of HX8310-A

7.2 Layout Recommendation



Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
0.1	2004/10/8	New Setup 1
0.2	2004/10/12	1. Modified the Product name HX8310-A 2. Page 13: Change the VCMDUM1-10 to VCMDUM11~15 and VCMDUM21~25 3. Page 14: Modified the description of IOVCC 4. Page 15: Modified the figure 5. Page 16: Modified the name of pad VCMDUMxx 6. Page 79: Re-build the Table4.1 and Modified the contents of Chapter 4 7. Page 119: Modified the Block Diagram of Power Supply Circuit
0.3	2004/11/11	1. Page 79: Modified the List Table of Register Set. 2. Page 88: Added the Register R06. 3. Page 89: Modified the Table 4.11. 4. Page 104: Modified the Table 4.36. 5. Page 105: Added the Register R10. 6. Page 108: Modified the Register R20. 7. Page 118: Modified the Register R23. 8. Page 118: Modified the Register R24. 9. Page 118: Added the Register R25. 10. Page 118: Added the Register R26
0.4	2004/12/3	1. Page 12: Modified the TVCOMHI and TVMAG. 2. Page 144: Added the Layout Recommendation.
0.5	2004/12/10	1. Page 15: Modified the Pin Assignments. 2. Page 19: Modified the BUMP Arrangement. 3. Page 144: Modified the Layout Recommendation.
0.6	2005/2/15	1. Page 10: Modified the Pin Description. 2. Page 20: Modified the System Interface, the Table 2.1, and the Table 2.2. 3. Page 21: Modified the 18-bit bus Interface, and the 16-bit bus Interface. 4. Page 22: Modified the 9-bit bus Interface. 5. Page 23: Modified the 8-bit bus Interface. 6. Page 24: Modified the Serial Data Transfer Interface, and the Table 2.3. 7. Page 25: Modified the Figure 2.9, and the Figure 2.10. 8. Page 26: Modified the Figure 2.11. 9. Page 27: Modified the Figure 2.12, and the Equation. 10. Page 28. Modified the Equations. 11. Page 30: Modified the Table 2.4. 12. Page 34: Modified the Figure 2.17. 13. Page 57: Modified the Partial Screen Display. 14. Page 58: Modified the Table 3.8, and the Table 3.9. 15. Page 64: Modified the Figure 3.21. 16. Page 76: Modified the Figure 3.25. 17. Page 77: Modified the Figure 3.27, and the Table 3.21. 18. Page 79: Modified the Table 4.1. 19. Page 83: Modified the Driver Output Control Register. 20. Page 85: Modified the Figure 4.8. 21. Page 88: Modified the 16-bit Compare Register.

Version	EFF.DATE	DESCRIPTION OF CHANGES
		22. Page 119: Modified the Figure 4.52. 23. Page 126: Modified the Figure 5.5.