DATA SHEET

(DOC No. HX8340-A-DS)

HX8340-A

176RGB x 220 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

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Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This manual describes the Himax's HX8340-A 176RGB*220 dots resolution driving controller. The HX8340-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 176RGB*220 dots at maximum.

The HX8340-A can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8340-A also supports various functions to reduce the power consumption of a LCD system via software control, such as an standby mode, sleep mode and 8-color display mode, The HX8340-A has four system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, VSYNC interface (internal clock, DB17-0), serial data transfer interface and RGB18-/16-/6-bit bus interface (DOTCLOCK, VSYNC, HSYNC, ENABLE, PD17-0). In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write mode and widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers.

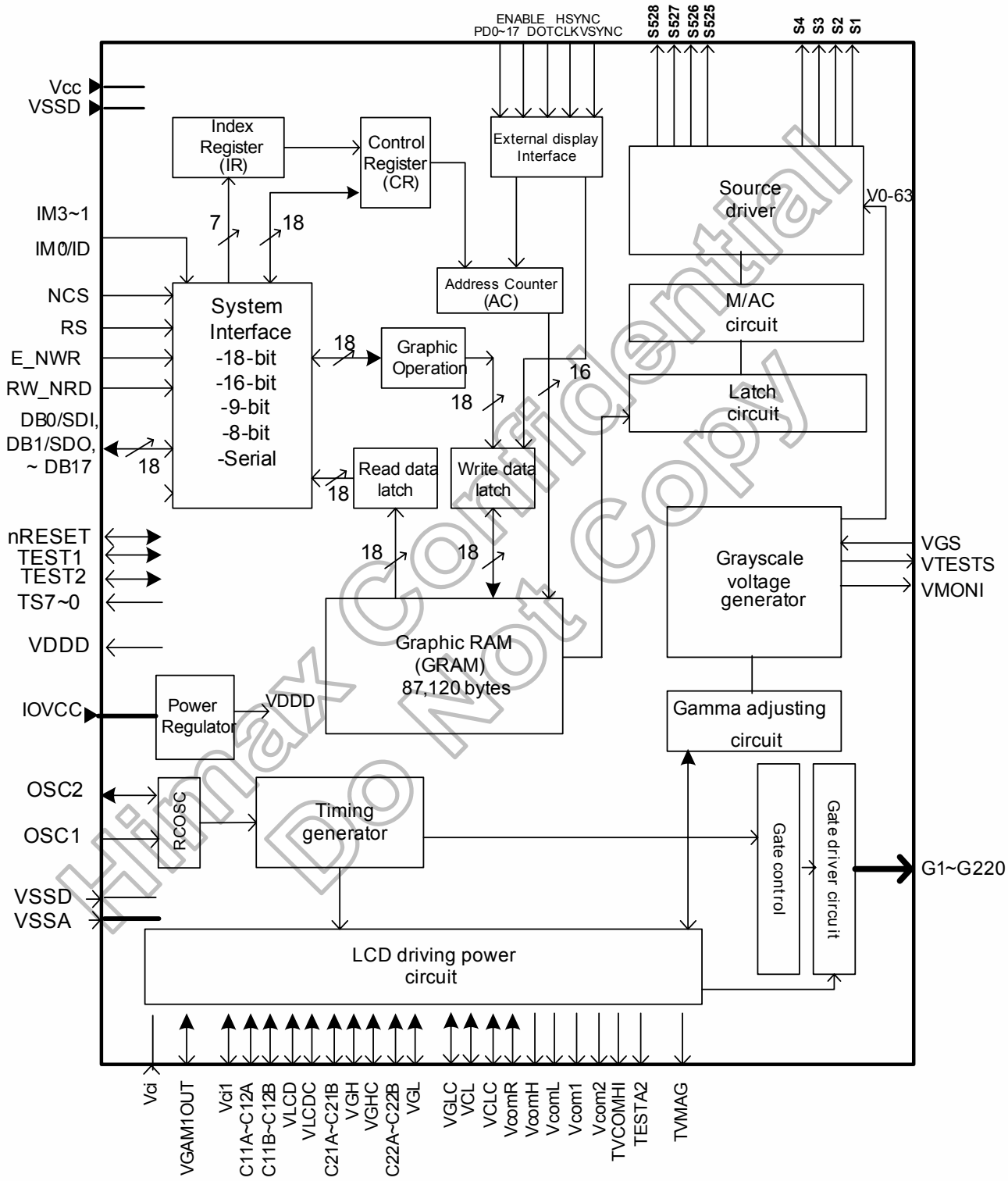
The HX8340-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

2 .Features

- Single chip solution to drive a TFT panel
- 176RGB x 220-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support interface:
  - 80 System interface (8-/9-/16-/18-bit bus)
  - Serial Data Transfer Interface
  - RGB interface (6-/16-/18-bit bus)
  - VSYNC data transfer interface
- Internal graphics RAM capacity: 87,120 bytes
- The 262,144 colors can be displayed at the same time with gamma correction
- The vertical scroll display function in line units
- Internal operation circuit of liquid crystal display:
  - Source channel: 528
  - Gate line: 220
- To write data in a window-RAM address area by using a window-address function
- Bit-operation functions for graphics transaction:
  - The write data mask function in bit unit
  - The logical operation in pixel unit and conditional write function
- Low-power consumption architecture supports:
  - Vci = 2.5 to 3.3 V (internal reference voltage)
  - Vcc = 2.4 to 3.3 V (corresponding low-voltage operation)
  - IOVcc = 1.65 to 3.3 V (Interface I/O operation)
  - VLCD = 4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - Standby mode
    - Sleep mode
- N-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Internal oscillator and hardware reset function

3. Device Overview

3.1 Block Diagram



3.2 Pin Description

<table>
<tr><th colspan="6">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="2">Description</th></tr>
<tr><td>IM3-1, IM0</td><td>I</td><td>4</td><td>VSSD/ IOVcc</td><td colspan="2">Select the MPU interface mode as listed below
<table>
<tr><th>IM0 (ID)</th><th>IM1</th><th>IM2</th><th>IM3</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system</td><td>DB17-10, 8-1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 80-system</td><td>DB17-10</td></tr>
<tr><td>ID</td><td>0</td><td>1</td><td>0</td><td>Serial data transfer interface</td><td>DB1-0</td></tr>
<tr><td>*</td><td>1</td><td>1</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface, 80-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>9-bit bus interface, 80-system</td><td>DB17-9</td></tr>
<tr><td>*</td><td>*</td><td>1</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
</table>
Note: If the serial data transfer interface was selected, IM0 pin is used like the ID setting for the device code in transfer data.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">The signal for register index or register command select.
Low: Register index or internal status (in read operation);
High: Register command.
Connect to IOVcc or VSSD level when serial data transfer interface is selected.</td></tr>
<tr><td>VLD</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Fix to VSSD</td></tr>
<tr><td>E_NWR/SCL</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Serves as a write signal and writes data at the rising edge in i80 system interface.
Serves as the synchronous clock signal in serial data transfer interface.
Fix it to IOVCC level when using serial data transfer interface.</td></tr>
<tr><td>RW_NRD</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Low: Write；High: Read
Serves as a read signal and reads data at the low level in i80 system interface. Fix it to IOVcc level when using serial data transfer interface.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVcc level.
Low: Selected (access enabled)
The polarity of the ENABLE signal is inverted by the EPL bit.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>Enable</td><td>Update</td></tr>
<tr><td>0</td><td>1</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>0</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>1</td><td>Enable</td><td>Update</td></tr>
</table></td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Frame synchronizing signal. The polarity of the VSYNC signal is selected by VSPL bit.
0: Start in the low level, 1: Start in the high level
Fix to the IOVcc level when not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Frame synchronizing signal. The polarity of the HSYNC signal is selected by HSPL bit.
0: Start in the low level, 1: Start in the high level.
Fix to the IOVcc level when not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Dot clock signal. Fix to the IOVcc level when not used.
If DPL=0: Data are latched on the rising edge of DOTCLK.
If DPL=1: Data are latched on the falling edge of DOTCLK.</td></tr>
<tr><td>PD0~17</td><td>I</td><td>18</td><td>MPU</td><td colspan="2">An 18-bit bus RGB data bus in 80-system interface mode. Fix the unused pins to either the VSSD level or the IOVcc level.
6-bit bus: use PD17-PD12
16-bit bus: use PD17-PD13 and PD11-PD1
18-bit bus: use PD17-PD0</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
VcomR	I	1	Variable Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VGAM1OUT and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8340-A.
VLCD	I	10	VLCDC	A power supply for the source driver outputs. A reference voltage for the step-up circuit2.
VGH	I	4	VGHC	A power supply for the TFT LCD's gate driver. Connect to VGHC.
VGL	I	5	VGLC	A power supply for the TFT LCD's gate driver. Connect to VGLC.
VCL	I	7	VCLC	A power supply for the VcomL level. Connect to VCLC.
TEST1	I	1	VSSD	A test pin. **Make sure to fix it to the VSSD level.**
TEST2	I	1	VSSD	A test pin. **Make sure to fix it to the VSSD level.**
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
Vci	I	1	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VciLVL	I	1	Power Supply	Generates a reference voltage (VciOUT, REGP) from the VciLVL level according to the ratio determined by the VC2-0 BITS. Connect to Vci on the FPC.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S528	O	528	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0, DATA IN THE ram address “0000” is output from S1.If SS=1, the same data in the ram address “0000” is output from S528. S1, S4, S7…display red (R), S2, S5, S8…display green (G), and S3, S6, S9…display blue (B) (SS=0).
G1~G220	O	220	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
Vcom1, Vcom2	O	4	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VcomH and VcomL is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel.
VcomH	O	4	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of Vcom amplitude generated in driving the Vcom alternation.
VcomL	O	4	Stabilizing Capacitor or open	When the Vcom alternation is driven, this pin indicates a low level of Vcom amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
FLM	O	1	MPU or open	A frame head pulse (amplitude: IOVcc-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it.
Vci1	O	8	Stabilizing Capacitor Vci1	An internal reference voltage. The amplitude between Vci and VSSD is determined by the VC2-0 bits.
VMONI	O	1	Open	A test pin. **Disconnect it.**
TS0 ~ 7		8	Open	A test pin. **Disconnect it.**
VTESTS	O	1	Open	A test pin. **Disconnect it.**
IOVccDUM1~4	O	4	Input pin	Internal IOVcc level outputs. When adjacent input pins are fixed to the IOVcc level, short-circuit them.
IOVSSDDUM 1~7	O	7	Input pin	Internal VSSD level outputs. When neighboring input pins are fixed to the VSSD level, short-circuit them.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A, C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B, C21A, C21B, C22A, C22B	I/O	6	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0_SDI	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Input pin in Serial Data Transfer interface. The input data is latched by the rising edge of the SCL signal on the chip.
DB1_SDO	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Output pin operate in Serial Data Transfer interface, the data is output by the falling edge of the SCL signal on the chip. If operate in Serial Data Transfer interface, do not connect the DB1_SDO pin to VSSD.
DB2~17	I/O	16	MPU	Operates liked a 18-bit bi-directional data bus 8-bit bus: use DB17-DB10 9-bit bus: use DB17-DB9 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 **Connected unused pins to the IOVcc or VSSD level.**
REGP	I/O	1	Test pin	A test pin for VGAM1OUT. Disconnect it.
Vci1	I/O	1	VciOUT	A reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
VGAM1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM2 between VSSD and VLCD from the reference voltage between Vci and VSSD that is generated internally. VGAM1OUT serves as a source driver grayscale reference voltage VGAM2, a VcomH level reference voltage, and a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT = 3.0 ~ (VLCD – 0.5)V
TVCOMHI	I/O	1	Open	A test pin for VcomH. **It must be connected with the capacitor 0.1uF to VSSD.**
TESTA2	I/O	1	Open	A test pin for VcomL. **It must be connected with the capacitor 0.1uF to VSSD.**
TVMAG	I/O	1	Open	A test pin for VcomL. **It must be connected with the capacitor 0.1uF to VSSD.**
VDDD_O	-	4	Open	Test pins. **Disconnect them.**
VDDD	O	1	Stabilizing capacitor	Internal logic voltage output (1.8V fixed)
DUMMY1,3	-	2	-	Test oins. **Disconnect them.**
HDUMMY2	-	1	-	Test oins. **Disconnect them.**
DUMMY4-25	-	22	-	Dummy pads. Can be connected to the wiring to the COG panel.
DUMMYR1-4	-	4	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3, DUMMYR4 are short-circuited within the chip.
VGLDUM1~4	-	4	-	Outputs the internal VGL level. Use as dummy gate output pins.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
Vcc	-	1	Power supply	A power supply for the internal logic. Vcc=2.4 ~ 3.3V
IOVcc	-	1	Power supply	A power supply for the interface pins. When using the COG method, usually connect to Vcc on the FPC to prevent noise. Voltage range: 1.65 ~ 3.3V
VSSA	-	1	Power supply	Analogy ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSD	-	1	Power supply	Ground for the internal RAM. VSSD=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.

3.3 Pin assignment

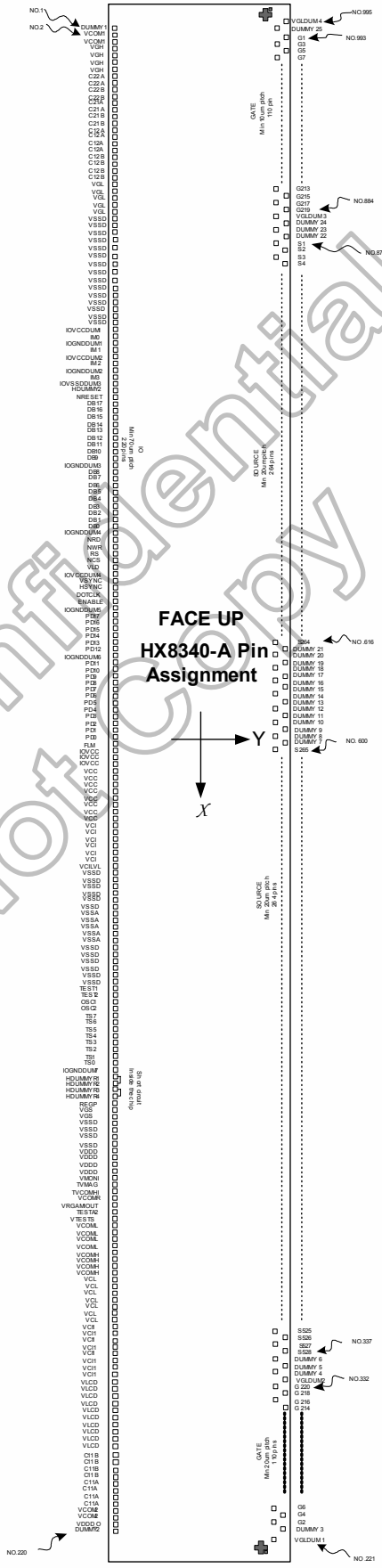
. Chip Size : 16400um x 862um
Include seal ring : 20x2um
Include scribe line : 40x2 um

. Chip thickness :400um(typ.)
. Pad Location : PAD Center
. Coordinate Origin : Chip Center
. Au Bump Size :

1. 50um x 120um
Input :
No.1 to No.220

2. 20um x 96um
Staggered LCD output side:
No.221 to No.995

- Au bump pitch: Refer to Pad Coordinate.
- Au bump height : 15um(typ.)
- Numbers in the figure corresponds to pad coordinate numbers.



3.3.1 PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY1	-7805	-306	66	DB7	-3255	-306	131	VSSA	1365	-306	196	VCI1	6125	-306
2	VCOM	-7735	-306	67	DB6	-3185	-306	132	VSSA	1435	-306	197	VCI1	6195	-306
3	VCOM	-7665	-306	68	DB5	-3115	-306	133	VSSA	1505	-306	198	VCI1	6265	-306
4	VGH	-7595	-306	69	DB4	-3045	-306	134	VSSA	1575	-306	199	VLCD	6335	-306
5	VGH	-7525	-306	70	DB3	-2975	-306	135	VSSD	1645	-306	200	VLCD	6405	-306
6	VGH	-7455	-306	71	DB2	-2905	-306	136	VSSD	1715	-306	201	VLCD	6475	-306
7	VGH	-7385	-306	72	DB1	-2835	-306	137	VSSD	1785	-306	202	VLCD	6545	-306
8	C22A	-7315	-306	73	DB0	-2765	-306	138	VSSD	1855	-306	203	VLCD	6615	-306
9	C22A	-7245	-306	74	IOGNDDUM4	-2695	-306	139	VSSD	1925	-306	204	VLCD	6685	-306
10	C22B	-7175	-306	75	NRD	-2625	-306	140	VSSD	1995	-306	205	VLCD	6755	-306
11	C22B	-7105	-306	76	NWR	-2555	-306	141	TEST1	2065	-306	206	VLCD	6825	-306
12	C21A	-7035	-306	77	RS	-2485	-306	142	TEST2	2135	-306	207	VLCD	6895	-306
13	C21A	-6965	-306	78	NCS	-2415	-306	143	OSC1	2205	-306	208	VLCD	6965	-306
14	C21B	-6895	-306	79	VLD	-2345	-306	144	OSC2	2275	-306	209	C11B	7035	-306
15	C21B	-6825	-306	80	IOVCCDUM4	-2275	-306	145	TS7	2415	-306	210	C11B	7105	-306
16	C12A	-6755	-306	81	VSYNC	-2205	-306	146	TS6	2485	-306	211	C11B	7175	-306
17	C12A	-6685	-306	82	HSYNC	-2135	-306	147	TS5	2555	-306	212	C11B	7245	-306
18	C12A	-6615	-306	83	DOTCLK	-2065	-306	148	TS4	2625	-306	213	C11A	7315	-306
19	C12A	-6545	-306	84	ENABLE	-1995	-306	149	TS3	2695	-306	214	C11A	7385	-306
20	C12B	-6475	-306	85	IOGNDDUM5	-1925	-306	150	TS2	2765	-306	215	C11A	7455	-306
21	C12B	-6405	-306	86	PD17	-1855	-306	151	TS1	2835	-306	216	C11A	7525	-306
22	C12B	-6335	-306	87	PD16	-1785	-306	152	TS0	2905	-306	217	VCOM	7595	-306
23	C12B	-6265	-306	88	PD15	-1715	-306	153	IOGNDDUM7	2975	-306	218	VCOM	7665	-306
24	VGL	-6195	-306	89	PD14	-1645	-306	154	HDUMMYR1	3045	-306	219	VDDD_O	7735	-306
25	VGL	-6125	-306	90	PD13	-1575	-306	155	HDUMMYR2	3115	-306	220	DUMMY2	7805	-306
26	VGL	-6055	-306	91	PD12	-1505	-306	156	HDUMMYR3	3185	-306	221	VGLDUM1	7850	318
27	VGL	-5985	-306	92	IOGNDDUM6	-1435	-306	157	HDUMMYR4	3255	-306	222	DUMMY3	7830	193
28	VGL	-5915	-306	93	PD11	-1365	-306	158	REGP	3325	-306	223	G2	7810	318
29	VSSD	-5845	-306	94	PD10	-1295	-306	159	VGS	3395	-306	224	G4	7790	193
30	VSSD	-5775	-306	95	PD9	-1225	-306	160	VGS	3465	-306	225	G6	7770	318
31	VSSD	-5705	-306	96	PD8	-1155	-306	161	VSSD	3535	-306	226	G8	7750	193
32	VSSD	-5635	-306	97	PD7	-1085	-306	162	VSSD	3605	-306	227	G10	7730	318
33	VSSD	-5565	-306	98	PD6	-1015	-306	163	VSSD	3675	-306	228	G12	7710	193
34	VSSD	-5495	-306	99	PD5	-945	-306	164	VSSD	3745	-306	229	G14	7690	318
35	VSSD	-5425	-306	100	PD4	-875	-306	165	VDDD	3815	-306	230	G16	7670	193
36	VSSD	-5355	-306	101	PD3	-805	-306	166	VDDD	3885	-306	231	G18	7650	318
37	VSSD	-5285	-306	102	PD2	-735	-306	167	VDDD	3955	-306	232	G20	7630	193
38	VSSD	-5215	-306	103	PD1	-665	-306	168	VDDD	4025	-306	233	G22	7610	318
39	VSSD	-5145	-306	104	PD0	-595	-306	169	VMONI	4095	-306	234	G24	7590	193
40	VSSD	-5075	-306	105	FLM	-525	-306	170	TVMAG	4165	-306	235	G26	7570	318
41	VSSD	-5005	-306	106	IOVCC	-442	-306	171	TVCOMHI	4235	-306	236	G28	7550	193
42	VSSD	-4935	-306	107	IOVCC	-372	-306	172	VCOMR	4305	-306	237	G30	7530	318
43	VSSD	-4865	-306	108	IOVCC	-302	-306	173	VGAM1OUT	4375	-306	238	G32	7510	193
44	IOVCCDUM1	-4795	-306	109	VCC	-217	-306	174	TESTA2	4445	-306	239	G34	7490	318
45	IM0	-4725	-306	110	VCC	-147	-306	175	VTESTOUT	4565	-306	240	G36	7470	193
46	IOGNDDUM1	-4655	-306	111	VCC	-77	-306	176	VCOML	4635	-306	241	G38	7450	318
47	IM1	-4585	-306	112	VCC	-7	-306	177	VCOML	4705	-306	242	G40	7430	193
48	IOVCCDUM2	-4515	-306	113	VCC	63	-306	178	VCOML	4775	-306	243	G42	7410	318
49	IM2	-4445	-306	114	VCC	133	-306	179	VCOML	4845	-306	244	G44	7390	193
50	IOGNDDUM2	-4375	-306	115	VCC	203	-306	180	VCOMH	4960	-306	245	G46	7370	318
51	IM3	-4305	-306	116	VCC	273	-306	181	VCOMH	5030	-306	246	G48	7350	193
52	IOVCCDUM3	-4235	-306	117	VCI	372	-306	182	VCOMH	5100	-306	247	G50	7330	318
53	HDUMMY2	-4165	-306	118	VCI	442	-306	183	VCOMH	5170	-306	248	G52	7310	193
54	NRESET	-4095	-306	119	VCI	512	-306	184	VCL	5240	-306	249	G54	7290	318
55	DB17	-4025	-306	120	VCI	582	-306	185	VCL	5310	-306	250	G56	7270	193
56	DB16	-3955	-306	121	VCI	652	-306	186	VCL	5380	-306	251	G58	7250	318
57	DB15	-3885	-306	122	VCI	722	-306	187	VCL	5450	-306	252	G60	7230	193
58	DB14	-3815	-306	123	VCILVL	805	-306	188	VCL	5520	-306	253	G62	7210	318
59	DB13	-3745	-306	124	VSSD	875	-306	189	VCL	5590	-306	254	G64	7190	193
60	DB12	-3675	-306	125	VSSD	945	-306	190	VCL	5660	-306	255	G66	7170	318
61	DB11	-3605	-306	126	VSSD	1015	-306	191	VCI1	5775	-306	256	G68	7150	193
62	DB10	-3535	-306	127	VSSD	1085	-306	192	VCI1	5845	-306	257	G70	7130	318
63	DB9	-3465	-306	128	VSSD	1155	-306	193	VCI1	5915	-306	258	G72	7110	193
64	IOGNDDUM3	-3395	-306	129	VSSD	1225	-306	194	VCI1	5985	-306	259	G74	7090	318
65	DB8	-3325	-306	130	VSSA	1295	-306	195	VCI1	6055	-306	260	G76	7070	193

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad nae	X	Y	No.	Pad name	X	Y
261	G78	7050	318	326	G208	5750	193	391	S474	4450	318	456	S409	3150	193
262	G80	7030	193	327	G210	5730	318	392	S473	4430	193	457	S408	3130	318
263	G82	7010	318	328	G212	5710	193	393	S472	4410	318	458	S407	3110	193
264	G84	6990	193	329	G214	5690	318	394	S471	4390	193	459	S406	3090	318
265	G86	6970	318	330	G216	5670	193	395	S470	4370	318	460	S405	3070	193
266	G88	6950	193	331	G218	5650	318	396	S469	4350	193	461	S404	3050	318
267	G90	6930	318	332	G220	5630	193	397	S468	4330	318	462	S403	3030	193
268	G92	6910	193	333	VGLDUM2	5610	318	398	S467	4310	193	463	S402	3010	318
269	G94	6890	318	334	DUMMY4	5590	193	399	S466	4290	318	464	S401	2990	193
270	G96	6870	193	335	DUMMY5	5570	318	400	S465	4270	193	465	S400	2970	318
271	G98	6850	318	336	DUMMY6	5550	193	401	S464	4250	318	466	S399	2950	193
272	G100	6830	193	337	S528	5530	318	402	S463	4230	193	467	S398	2930	318
273	G102	6810	318	338	S527	5510	193	403	S462	4210	318	468	S397	2910	193
274	G104	6790	193	339	S526	5490	318	404	S461	4190	193	469	S396	2890	318
275	G106	6770	318	340	S525	5470	193	405	S460	4170	318	470	S395	2870	193
276	G108	6750	193	341	S524	5450	318	406	S459	4150	193	471	S394	2850	318
277	G110	6730	318	342	S523	5430	193	407	S458	4130	318	472	S393	2830	193
278	G112	6710	193	343	S522	5410	318	408	S457	4110	193	473	S392	2810	318
279	G114	6690	318	344	S521	5390	193	409	S456	4090	318	474	S391	2790	193
280	G116	6670	193	345	S520	5370	318	410	S455	4070	193	475	S390	2770	318
281	G118	6650	318	346	S519	5350	193	411	S454	4050	318	476	S389	2750	193
282	G120	6630	193	347	S518	5330	318	412	S453	4030	193	477	S388	2730	318
283	G122	6610	318	348	S517	5310	193	413	S452	4010	318	478	S387	2710	193
284	G124	6590	193	349	S516	5290	318	414	S451	3990	193	479	S386	2690	318
285	G126	6570	318	350	S515	5270	193	415	S450	3970	318	480	S385	2670	193
286	G128	6550	193	351	S514	5250	318	416	S449	3950	193	481	S384	2650	318
287	G130	6530	318	352	S513	5230	193	417	S448	3930	318	482	S383	2630	193
288	G132	6510	193	353	S512	5210	318	418	S447	3910	193	483	S382	2610	318
289	G134	6490	318	354	S511	5190	193	419	S446	3890	318	484	S381	2590	193
290	G136	6470	193	355	S510	5170	318	420	S445	3870	193	485	S380	2570	318
291	G138	6450	318	356	S509	5150	193	421	S444	3850	318	486	S379	2550	193
292	G140	6430	193	357	S508	5130	318	422	S443	3830	193	487	S378	2530	318
293	G142	6410	318	358	S507	5110	193	423	S442	3810	318	488	S377	2510	193
294	G144	6390	193	359	S506	5090	318	424	S441	3790	193	489	S376	2490	318
295	G146	6370	318	360	S505	5070	193	425	S440	3770	318	490	S375	2470	193
296	G148	6350	193	361	S504	5050	318	426	S439	3750	193	491	S374	2450	318
297	G150	6330	318	362	S503	5030	193	427	S438	3730	318	492	S373	2430	193
298	G152	6310	193	363	S502	5010	318	428	S437	3710	193	493	S372	2410	318
299	G154	6290	318	364	S501	4990	193	429	S436	3690	318	494	S371	2390	193
300	G156	6270	193	365	S500	4970	318	430	S435	3670	193	495	S370	2370	318
301	G158	6250	318	366	S499	4950	193	431	S434	3650	318	496	S369	2350	193
302	G160	6230	193	367	S498	4930	318	432	S433	3630	193	497	S368	2330	318
303	G162	6210	318	368	S497	4910	193	433	S432	3610	318	498	S367	2310	193
304	G164	6190	193	369	S496	4890	318	434	S431	3590	193	499	S366	2290	318
305	G166	6170	318	370	S495	4870	193	435	S430	3570	318	500	S365	2270	193
306	G168	6150	193	371	S494	4850	318	436	S429	3550	193	501	S364	2250	318
307	G170	6130	318	372	S493	4830	193	437	S428	3530	318	502	S363	2230	193
308	G172	6110	193	373	S492	4810	318	438	S427	3510	193	503	S362	2210	318
309	G174	6090	318	374	S491	4790	193	439	S426	3490	318	504	S361	2190	193
310	G176	6070	193	375	S490	4770	318	440	S425	3470	193	505	S360	2170	318
311	G178	6050	318	376	S489	4750	193	441	S424	3450	318	506	S359	2150	193
312	G180	6030	193	377	S488	4730	318	442	S423	3430	193	507	S358	2130	318
313	G182	6010	318	378	S487	4710	193	443	S422	3410	318	508	S357	2110	193
314	G184	5990	193	379	S486	4690	318	444	S421	3390	193	509	S356	2090	318
315	G186	5970	318	380	S485	4670	193	445	S420	3370	318	510	S355	2070	193
316	G188	5950	193	381	S484	4650	318	446	S419	3350	193	511	S354	2050	318
317	G190	5930	318	382	S483	4630	193	447	S418	3330	318	512	S353	2030	193
318	G192	5910	193	383	S482	4610	318	448	S417	3310	193	513	S352	2010	318
319	G194	5890	318	384	S481	4590	193	449	S416	3290	318	514	S351	1990	193
320	G196	5870	193	385	S480	4570	318	450	S415	3270	193	515	S350	1970	318
321	G198	5850	318	386	S479	4550	193	451	S414	3250	318	516	S349	1950	193
322	G200	5830	193	387	S478	4530	318	452	S413	3230	193	517	S348	1930	318
323	G202	5810	318	388	S477	4510	193	453	S412	3210	318	518	S347	1910	193
324	G204	5790	193	389	S476	4490	318	454	S411	3190	193	519	S346	1890	318
325	G206	5770	318	390	S475	4470	193	455	S410	3170	318	520	S345	1870	193

No.	Pad name	X	Y
521	S344	1850	318
522	S343	1830	193
523	S342	1810	318
524	S341	1790	193
525	S340	1770	318
526	S339	1750	193
527	S338	1730	318
528	S337	1710	193
529	S336	1690	318
530	S335	1670	193
531	S334	1650	318
532	S333	1630	193
533	S332	1610	318
534	S331	1590	193
535	S330	1570	318
536	S329	1550	193
537	S328	1530	318
538	S327	1510	193
539	S326	1490	318
540	S325	1470	193
541	S324	1450	318
542	S323	1430	193
543	S322	1410	318
544	S321	1390	193
545	S320	1370	318
546	S319	1350	193
547	S318	1330	318
548	S317	1310	193
549	S316	1290	318
550	S315	1270	193
551	S314	1250	318
552	S313	1230	193
553	S312	1210	318
554	S311	1190	193
555	S310	1170	318
556	S309	1150	193
557	S308	1130	318
558	S307	1110	193
559	S306	1090	318
560	S305	1070	193
561	S304	1050	318
562	S303	1030	193
563	S302	1010	318
564	S301	990	193
565	S300	970	318
566	S299	950	193
567	S298	930	318
568	S297	910	193
569	S296	890	318
570	S295	870	193
571	S294	850	318
572	S293	830	193
573	S292	810	318
574	S291	790	193
575	S290	770	318
576	S289	750	193
577	S288	730	318
578	S287	710	193
579	S286	690	318
580	S285	670	193
581	S284	650	318
582	S283	630	193
583	S282	610	318
584	S281	590	193
585	S280	570	318

No.	Pad name	X	Y
586	S279	550	193
587	S278	530	318
588	S277	510	193
589	S276	490	318
590	S275	470	193
591	S274	450	318
592	S273	430	193
593	S272	410	318
594	S271	390	193
595	S270	370	318
596	S269	350	193
597	S268	330	318
598	S267	310	193
599	S266	290	318
600	S265	270	193
601	DUMMY7	250	318
602	DUMMY8	230	193
603	DUMMY9	210	318
604	DUMMY10	170	318
605	DUMMY11	130	318
606	DUMMY12	90	318
607	DUMMY13	50	318
608	DUMMY14	0	318
609	DUMMY15	-50	318
610	DUMMY16	-90	318
611	DUMMY17	-130	318
612	DUMMY18	-170	318
613	DUMMY19	-210	318
614	DUMMY20	-230	193
615	DUMMY21	-250	318
616	S264	-270	193
617	S263	-290	318
618	S262	-310	193
619	S261	-330	318
620	S260	-350	193
621	S259	-370	318
622	S258	-390	193
623	S257	-410	318
624	S256	-430	193
625	S255	-450	318
626	S254	-470	193
627	S253	-490	318
628	S252	-510	193
629	S251	-530	318
630	S250	-550	193
631	S249	-570	318
632	S248	-590	193
633	S247	-610	318
634	S246	-630	193
635	S245	-650	318
636	S244	-670	193
637	S243	-690	318
638	S242	-710	193
639	S241	-730	318
640	S240	-750	193
641	S239	-770	318
642	S238	-790	193
643	S237	-810	318
644	S236	-830	193
645	S235	-850	318
646	S234	-870	193
647	S233	-890	318
648	S232	-910	193
649	S231	-930	318
650	S230	-950	193

No.	Pad name	X	Y
651	S229	-970	318
652	S228	-990	193
653	S227	-1010	318
654	S226	-1030	193
655	S225	-1050	318
656	S224	-1070	193
657	S223	-1090	318
658	S222	-1110	193
659	S221	-1130	318
660	S220	-1150	193
661	S219	-1170	318
662	S218	-1190	193
663	S217	-1210	318
664	S216	-1230	193
665	S215	-1250	318
666	S214	-1270	193
667	S213	-1290	318
668	S212	-1310	193
669	S211	-1330	318
670	S210	-1350	193
671	S209	-1370	318
672	S208	-1390	193
673	S207	-1410	318
674	S206	-1430	193
675	S205	-1450	318
676	S204	-1470	193
677	S203	-1490	318
678	S202	-1510	193
679	S201	-1530	318
680	S200	-1550	193
681	S199	-1570	318
682	S198	-1590	193
683	S197	-1610	318
684	S196	-1630	193
685	S195	-1650	318
686	S194	-1670	193
687	S193	-1690	318
688	S192	-1710	193
689	S191	-1730	318
690	S190	-1750	193
691	S189	-1770	318
692	S188	-1790	193
693	S187	-1810	318
694	S186	-1830	193
695	S185	-1850	318
696	S184	-1870	193
697	S183	-1890	318
698	S182	-1910	193
699	S181	-1930	318
700	S180	-1950	193
701	S179	-1970	318
702	S178	-1990	193
703	S177	-2010	318
704	S176	-2030	193
705	S175	-2050	318
706	S174	-2070	193
707	S173	-2090	318
708	S172	-2110	193
709	S171	-2130	318
710	S170	-2150	193
711	S169	-2170	318
712	S168	-2190	193
713	S167	-2210	318
714	S166	-2230	193
715	S165	-2250	318

No.	Pad name	X	Y
716	S164	-2270	193
717	S163	-2290	318
718	S162	-2310	193
719	S161	-2330	318
720	S160	-2350	193
721	S159	-2370	318
722	S158	-2390	193
723	S157	-2410	318
724	S156	-2430	193
725	S155	-2450	318
726	S154	-2470	193
727	S153	-2490	318
728	S152	-2510	193
729	S151	-2530	318
730	S150	-2550	193
731	S149	-2570	318
732	S148	-2590	193
733	S147	-2610	318
734	S146	-2630	193
735	S145	-2650	318
736	S144	-2670	193
737	S143	-2690	318
738	S142	-2710	193
739	S141	-2730	318
740	S140	-2750	193
741	S139	-2770	318
742	S138	-2790	193
743	S137	-2810	318
744	S136	-2830	193
745	S135	-2850	318
746	S134	-2870	193
747	S133	-2890	318
748	S132	-2910	193
749	S131	-2930	318
750	S130	-2950	193
751	S129	-2970	318
752	S128	-2990	193
753	S127	-3010	318
754	S126	-3030	193
755	S125	-3050	318
756	S124	-3070	193
757	S123	-3090	318
758	S122	-3110	193
759	S121	-3130	318
760	S120	-3150	193
761	S119	-3170	318
762	S118	-3190	193
763	S117	-3210	318
764	S116	-3230	193
765	S115	-3250	318
766	S114	-3270	193
767	S113	-3290	318
768	S112	-3310	193
769	S111	-3330	318
770	S110	-3350	193
771	S109	-3370	318
772	S108	-3390	193
773	S107	-3410	318
774	S106	-3430	193
775	S105	-3450	318
776	S104	-3470	193
777	S103	-3490	318
778	S102	-3510	193
779	S101	-3530	318
780	S100	-3550	193

No.	Pad name	X	Y
781	S99	-3570	318
782	S98	-3590	193
783	S97	-3610	318
784	S96	-3630	193
785	S95	-3650	318
786	S94	-3670	193
787	S93	-3690	318
788	S92	-3710	193
789	S91	-3730	318
790	S90	-3750	193
791	S89	-3770	318
792	S88	-3790	193
793	S87	-3810	318
794	S86	-3830	193
795	S85	-3850	318
796	S84	-3870	193
797	S83	-3890	318
798	S82	-3910	193
799	S81	-3930	318
800	S80	-3950	193
801	S79	-3970	318
802	S78	-3990	193
803	S77	-4010	318
804	S76	-4030	193
805	S75	-4050	318
806	S74	-4070	193
807	S73	-4090	318
808	S72	-4110	193
809	S71	-4130	318
810	S70	-4150	193
811	S69	-4170	318
812	S68	-4190	193
813	S67	-4210	318
814	S66	-4230	193
815	S65	-4250	318
816	S64	-4270	193
817	S63	-4290	318
818	S62	-4310	193
819	S61	-4330	318
820	S60	-4350	193
821	S59	-4370	318
822	S58	-4390	193
823	S57	-4410	318
824	S56	-4430	193
825	S55	-4450	318
826	S54	-4470	193
827	S53	-4490	318
828	S52	-4510	193
829	S51	-4530	318
830	S50	-4550	193
831	S49	-4570	318
832	S48	-4590	193
833	S47	-4610	318
834	S46	-4630	193
835	S45	-4650	318
836	S44	-4670	193
837	S43	-4690	318
838	S42	-4710	193
839	S41	-4730	318
840	S40	-4750	193
841	S39	-4770	318
842	S38	-4790	193
843	S37	-4810	318
844	S36	-4830	193
845	S35	-4850	318

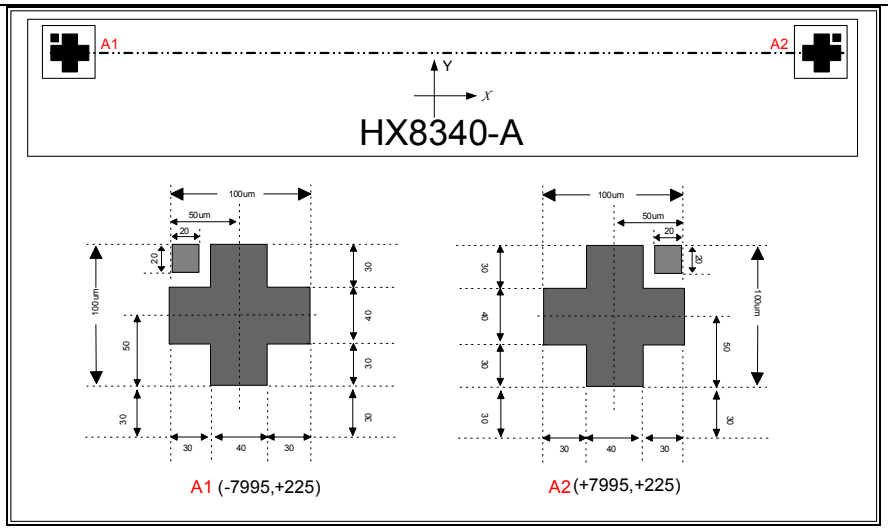
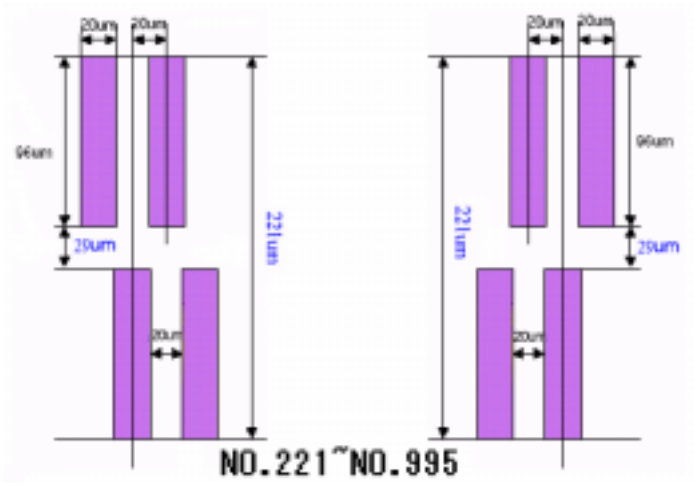
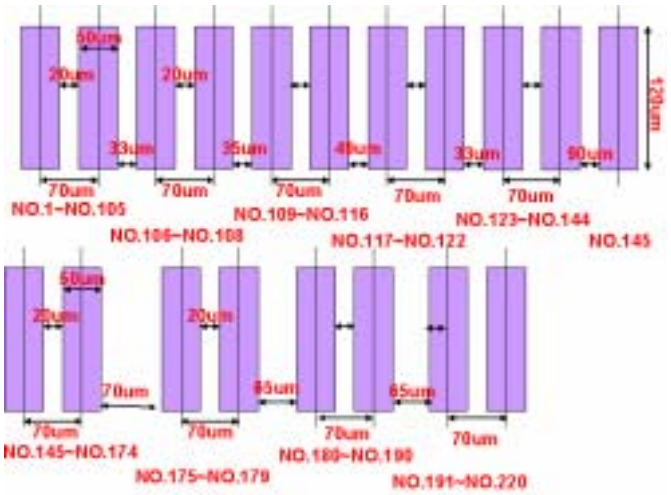
No.	Pad name	X	Y
846	S34	-4870	193
847	S33	-4890	318
848	S32	-4910	193
849	S31	-4930	318
850	S30	-4950	193
851	S29	-4970	318
852	S28	-4990	193
853	S27	-5010	318
854	S26	-5030	193
855	S25	-5050	318
856	S24	-5070	193
857	S23	-5090	318
858	S22	-5110	193
859	S21	-5130	318
860	S20	-5150	193
861	S19	-5170	318
862	S18	-5190	193
863	S17	-5210	318
864	S16	-5230	193
865	S15	-5250	318
866	S14	-5270	193
867	S13	-5290	318
868	S12	-5310	193
869	S11	-5330	318
870	S10	-5350	193
871	S9	-5370	318
872	S8	-5390	193
873	S7	-5410	318
874	S6	-5430	193
875	S5	-5450	318
876	S4	-5470	193
877	S3	-5490	318
878	S2	-5510	193
879	S1	-5530	318
880	DUMMY22	-5550	193
881	DUMMY23	-5570	318
882	DUMMY24	-5590	193
883	VGLDUM3	-5610	318
884	G219	-5630	193
885	G217	-5650	318
886	G215	-5670	193
887	G213	-5690	318
888	G211	-5710	193
889	G209	-5730	318
890	G207	-5750	193
891	G205	-5770	318
892	G203	-5790	193
893	G201	-5810	318
894	G199	-5830	193
895	G197	-5850	318
896	G195	-5870	193
897	G193	-5890	318
898	G191	-5910	193
899	G189	-5930	318
900	G187	-5950	193
901	G185	-5970	318
902	G183	-5990	193
903	G181	-6010	318
904	G179	-6030	193
905	G177	-6050	318
906	G175	-6070	193
907	G173	-6090	318
908	G171	-6110	193
909	G169	-6130	318
910	G167	-6150	193

No.	Pad name	X	Y
911	G165	-6170	318
912	G163	-6190	193
913	G161	-6210	318
914	G159	-6230	193
915	G157	-6250	318
916	G155	-6270	193
917	G153	-6290	318
918	G151	-6310	193
919	G149	-6330	318
920	G147	-6350	193
921	G145	-6370	318
922	G143	-6390	193
923	G141	-6410	318
924	G139	-6430	193
925	G137	-6450	318
926	G135	-6470	193
927	G133	-6490	318
928	G131	-6510	193
929	G129	-6530	318
930	G127	-6550	193
931	G125	-6570	318
932	G123	-6590	193
933	G121	-6610	318
934	G119	-6630	193
935	G117	-6650	318
936	G115	-6670	193
937	G113	-6690	318
938	G111	-6710	193
939	G109	-6730	318
940	G107	-6750	193
941	G105	-6770	318
942	G103	-6790	193
943	G101	-6810	318
944	G99	-6830	193
945	G97	-6850	318
946	G95	-6870	193
947	G93	-6890	318
948	G91	-6910	193
949	G89	-6930	318
950	G87	-6950	193
951	G85	-6970	318
952	G83	-6990	193
953	G81	-7010	318
954	G79	-7030	193
955	G77	-7050	318
956	G75	-7070	193
957	G73	-7090	318
958	G71	-7110	193
959	G69	-7130	318
960	G67	-7150	193
961	G65	-7170	318
962	G63	-7190	193
963	G61	-7210	318
964	G59	-7230	193
965	G57	-7250	318
966	G55	-7270	193
967	G53	-7290	318
968	G51	-7310	193
969	G49	-7330	318
970	G47	-7350	193
971	G45	-7370	318
972	G43	-7390	193
973	G41	-7410	318
974	G39	-7430	193
975	G37	-7450	318

No.	Pad name	X	Y
976	G35	-7470	193
977	G33	-7490	318
978	G31	-7510	193
979	G29	-7530	318
980	G27	-7550	193
981	G25	-7570	318
982	G23	-7590	193
983	G21	-7610	318
984	G19	-7630	193
985	G17	-7650	318
986	G15	-7670	193
987	G13	-7690	318
988	G11	-7710	193
989	G9	-7730	318
990	G7	-7750	193
991	G5	-7770	318
992	G3	-7790	193
993	G1	-7810	318
994	DUMMY25	-7830	193
995	VGLDUM4	-7850	318

Alignment mark	X	Y
A1	-7995	225
A2	7995	225

3.4 BUMP Arrangement

Alignment Mark	
S1 ~ S528 G1~ G220	
I/O pins	

4. Interface

4.1. System Interface

The HX8340-A supports two system interfaces: an 80-system 18-/16-/9-/8-bit bus interface and a serial data transfer bus interface. The interface mode is selected by the IM3-0 pins setting. The system interface enables instruction setting and RAM access.

The HX8340-A includes an index register (IR) be stored index data of internal control register and RAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting RS=0. Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. The IR will be indexed to these two control registers through data bus by setting RS=1. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

Operations	E_NWR	RW_NRD	RW	RS
Writes Indexes into IR	0	1	0	0
Reads internal status	1	0	1	0
Writes data into control register or GRAM	0	1	0	1
Reads control register or GRAM data	1	0	1	1

Table 4. 1 Register Selection (18-/16-/9-/8- Bit System Interface)

Start Bytes

Operations	R/W Bit	RS
Writes Indexes into IR	0	0
Reads internal status	1	0
Writes data into control register or GRAM	0	1
Reads data from control register or GRAM	1	1

Table 4. 2 Register Selection (Serial Data Transfer Interface)

4.1.1 80-System

80 system 18-bit bus Interface

The 80-system 18-bit parallel data transfer can be used by setting IM3-0 pins to "1010". The Figure 4.1 is the example of interface with i80Microcomputer and the Figure 4.2 is the data format of 18-bit system interface.

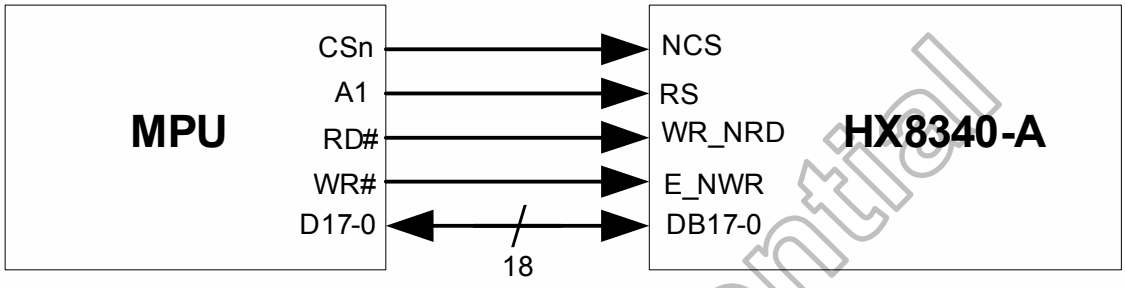


Figure 4. 1 Example of 80 System 18-bit bus Interface

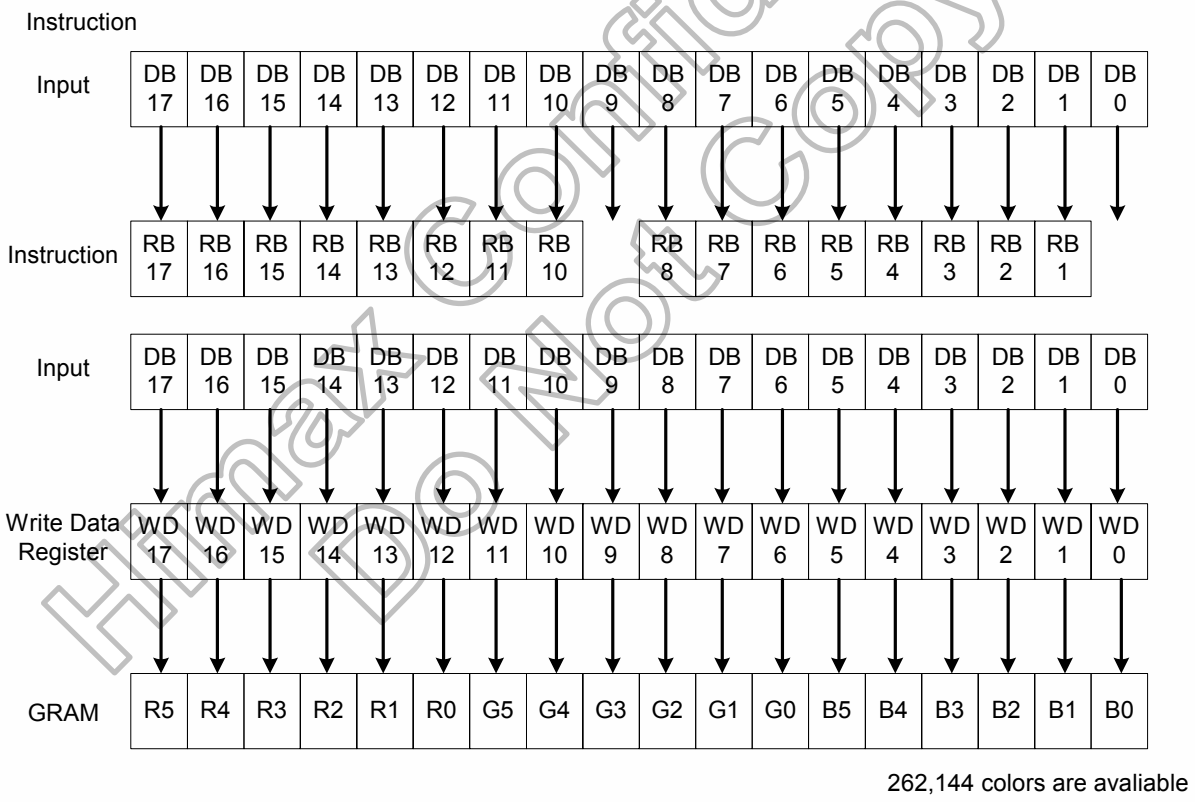


Figure 4. 2 Data Format of 18-bit bus System Interface

80 system 16-bit bus Interface

The 80-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to “0010”. The data written to GRAM is expanded to 18-bit bus data automatically in the LSI. Unused pins (DB9, DB0) must be fixed to the IOVcc or VSSD level. The Figure4.3 is the example of interface with 16-bit bus i80Microcomputer and the Figure 4.4 is the data format of 16-bit bus system interface.

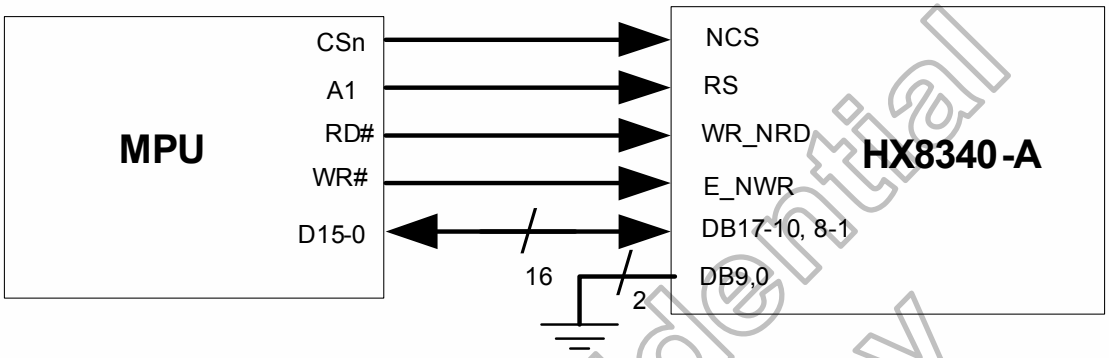


Figure 4. 3 Example of 80 System 16-bit bus Interface

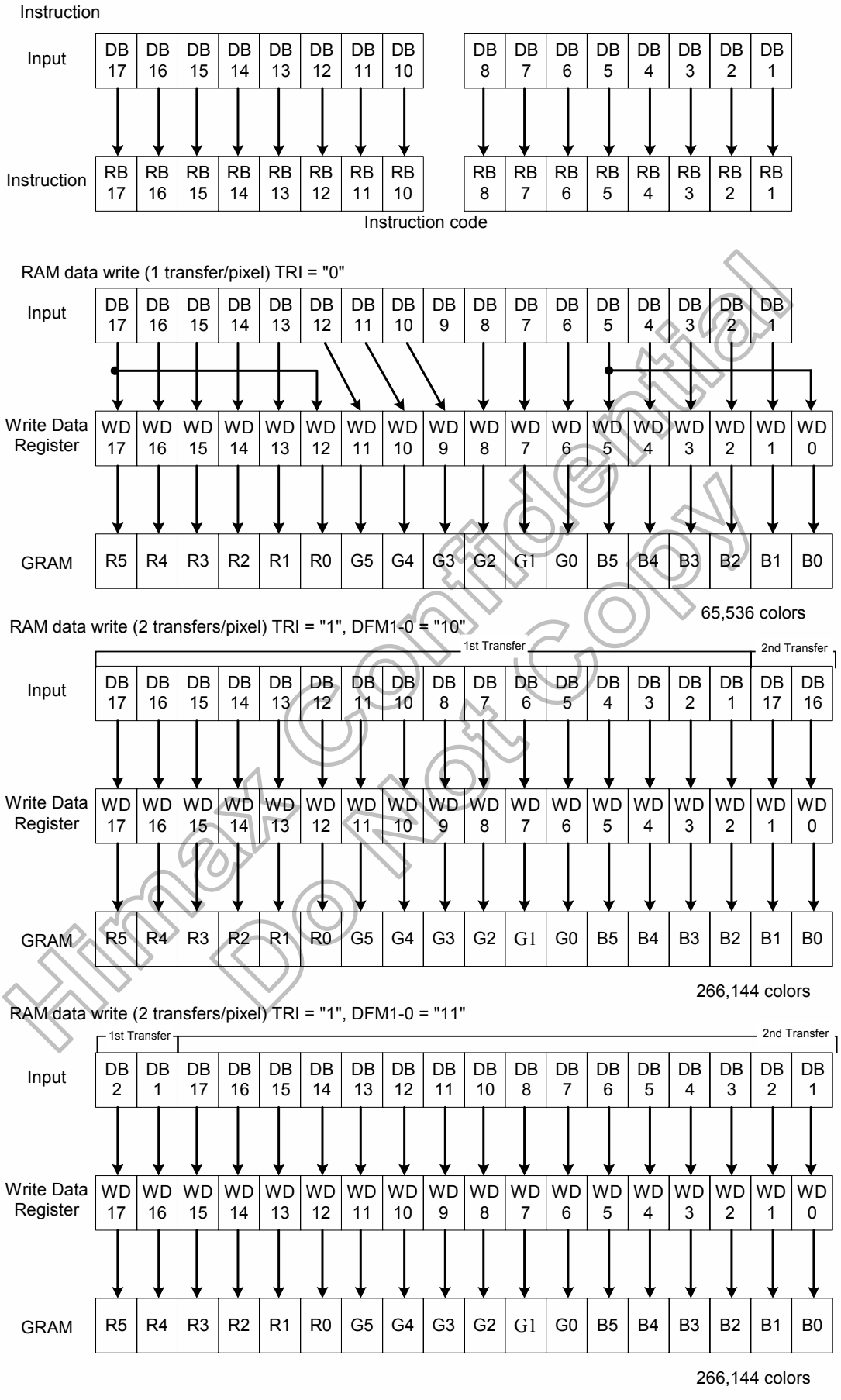


Figure 4. 4 Data Format of 16-bit bus System Interface

80-system 9-bit bus Interface

The 80-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to "1011". In 80- system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper nine bits, and then the upper nine bits are transferred first. Unused pins (DB8-0) must be fixed to the IOVcc or VSSD level. Ensure that upper bytes have to be written when writing the index register.

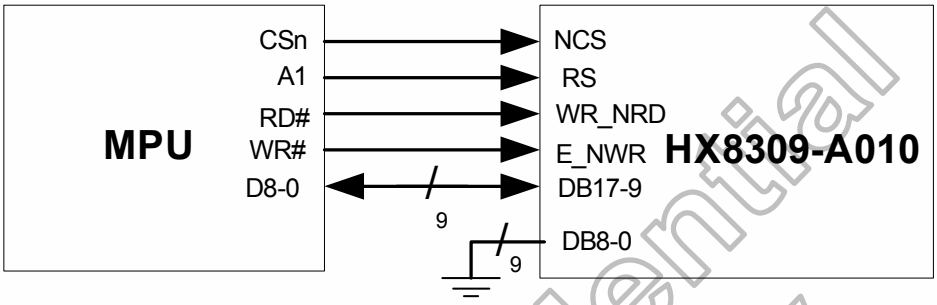


Figure 4. 5 Example of 80 System 9-bit bus Interface

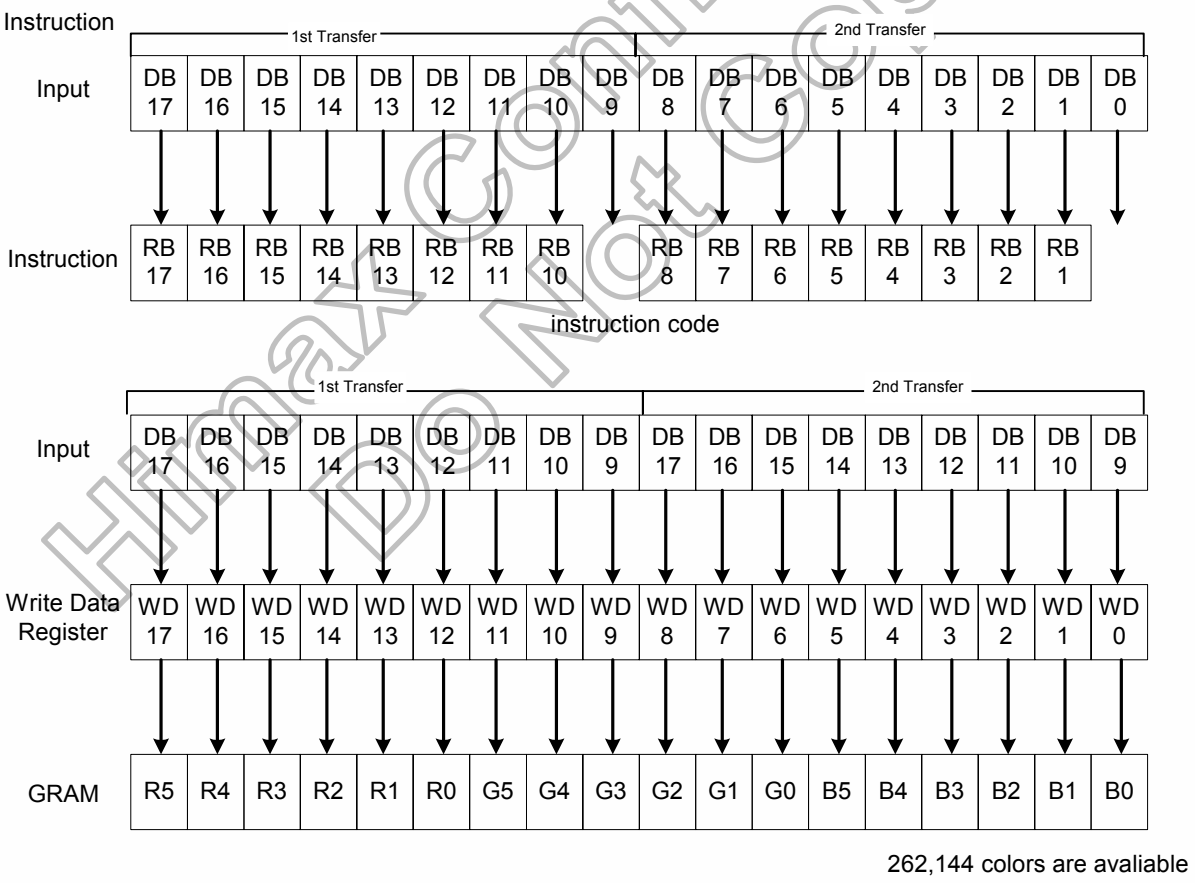


Figure 4. 6 Data Format of 9-bit bus System Interface

80 System 8-bit bus Interface

The 80-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0011”. In 80- system 8-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper eight bits, and then the upper eight bits are transferred first. Furthermore, the GRAM write data can be expanded into 16-bit bus automatically in internal process. Unused pins (DB9-0) must be fixed to the IOVcc or VSSD level.

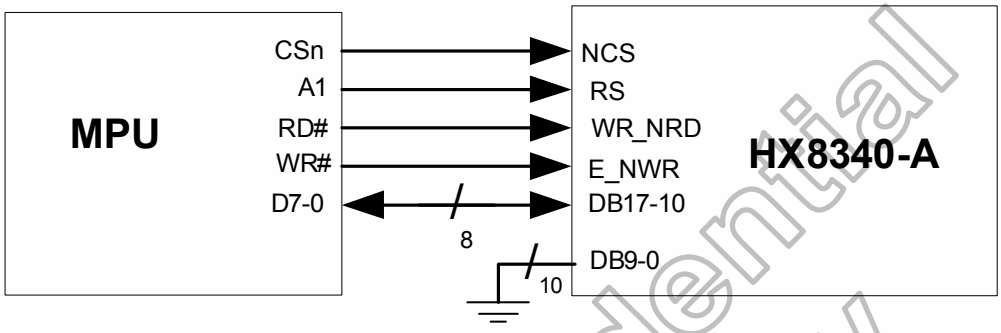


Figure 4. 7 Example of 80 System 8-bit bus Interface

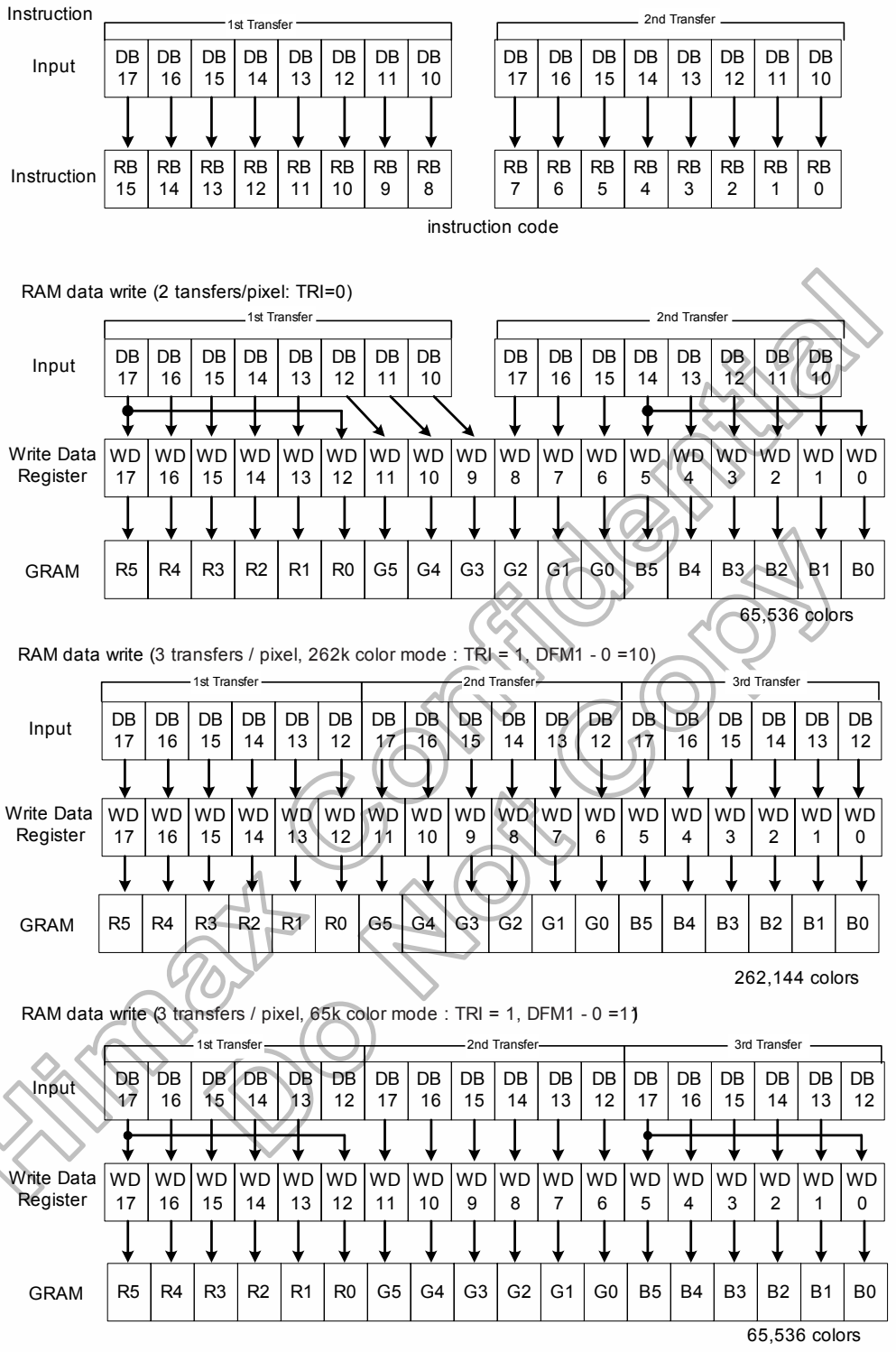
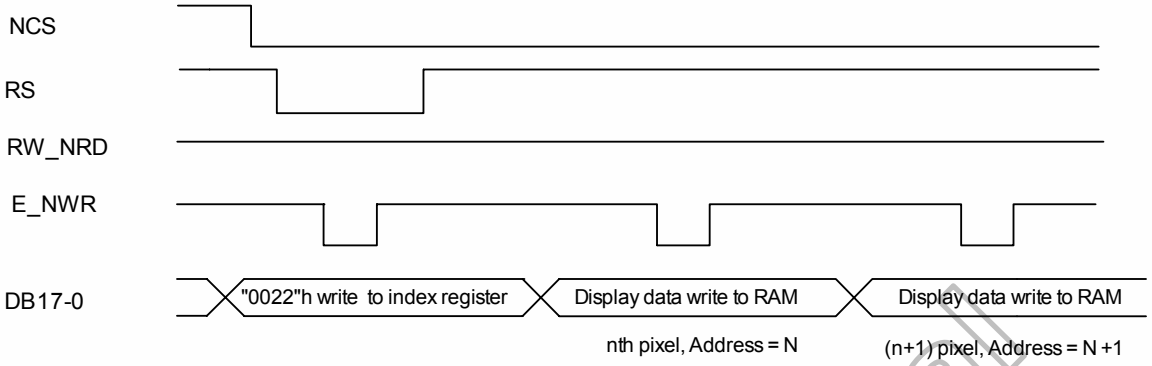
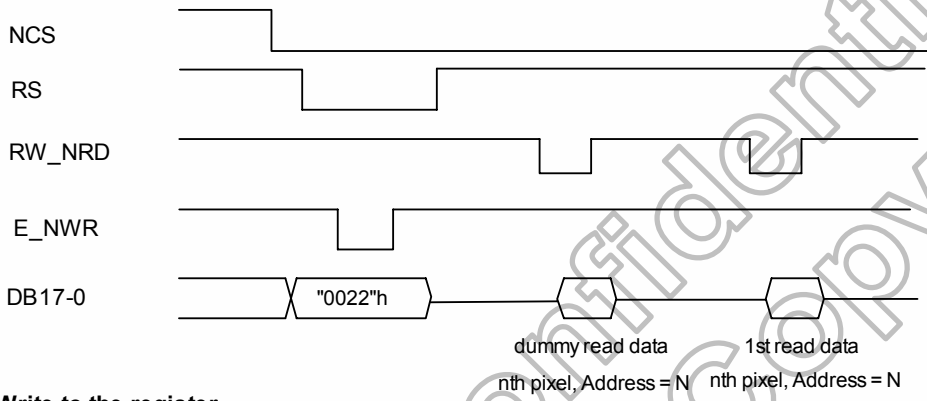


Figure 4. 8 Data Format of 8-bit bus System Interface

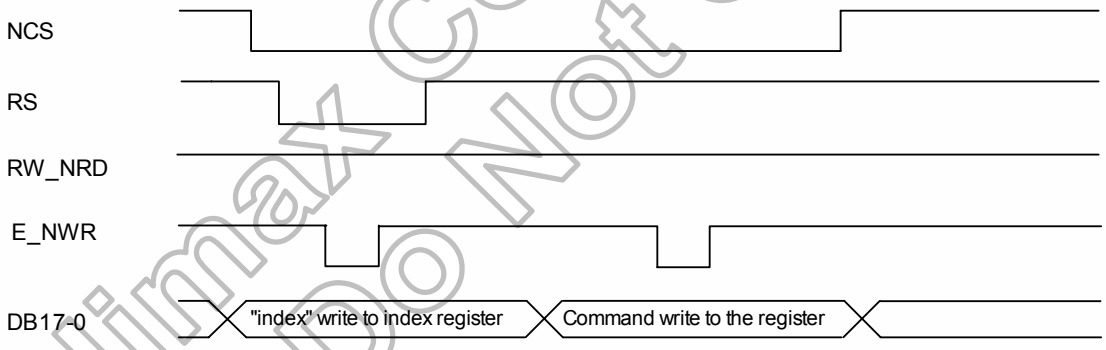
Write to the graphic RAM



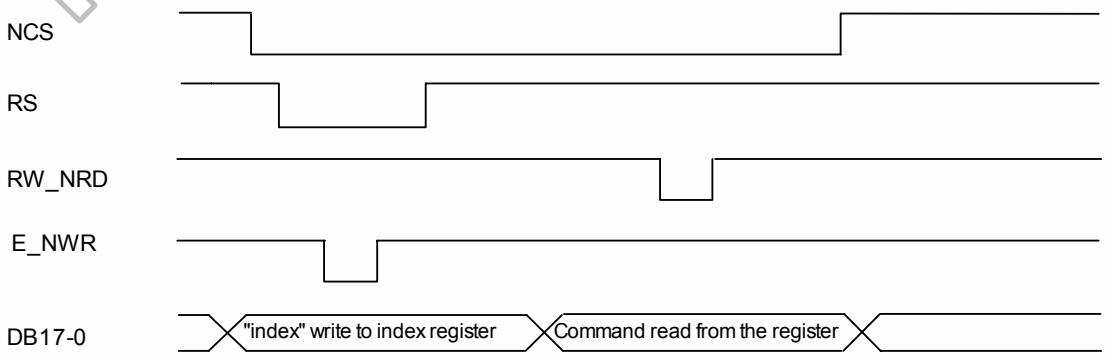
Read the graphic RAM



Write to the register



Read the register



I80 - 18/16 bit interface : D17~D10 = 00h, D8~D1 = Index value

Figure 4. 9 18 / 16-bit Parallel Bus Interface Timing (for i80 series MPU)

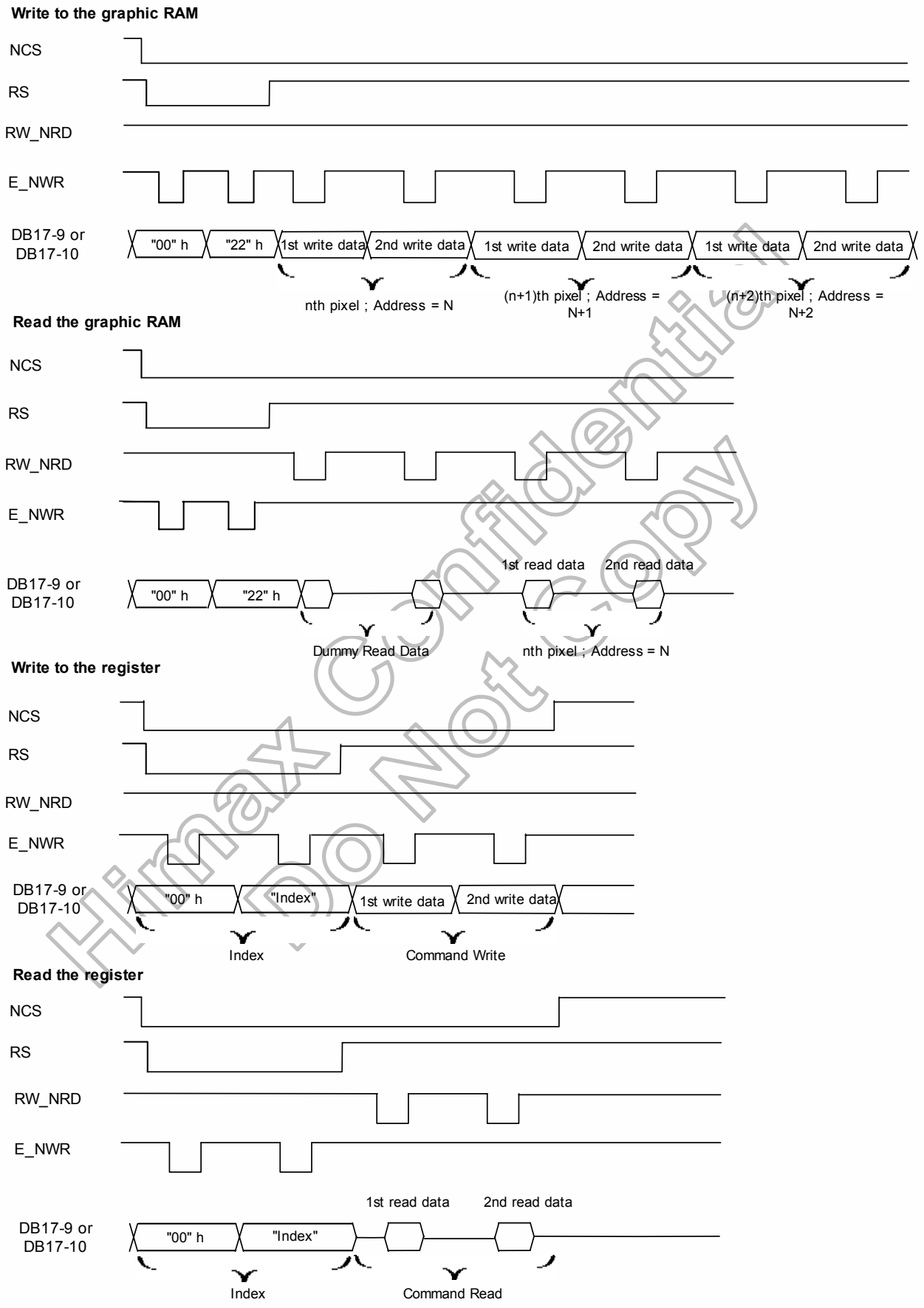
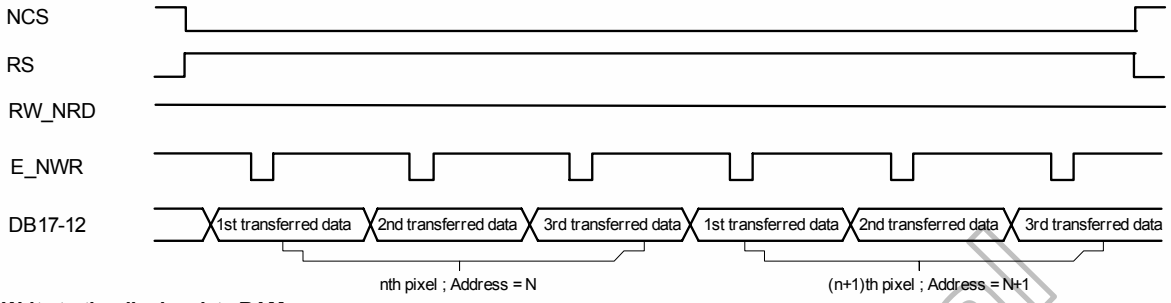


Figure 4. 10 9 / 8-bit Parallel Bus Interface Timing (for i80 series MPU)

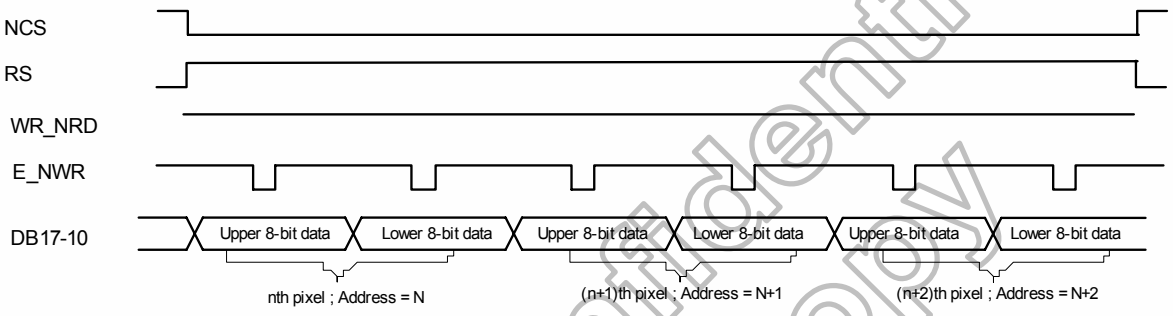
Write to the display data RAM

18/16-bit display data (6-bit x 3 transfers transfers)



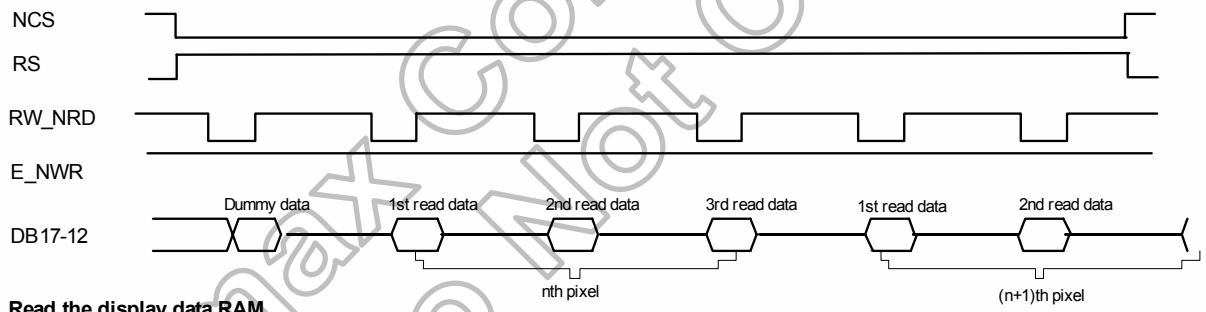
Write to the display data RAM

16-bit display data (8-bit x 2 transfers, TRI=0)



Read the display data RAM

18/16-bit display data (6-bit x 3 transfers, TRI=1)



Read the display data RAM

16-bit display data (8-bit x 2 transfers, TRI=0)

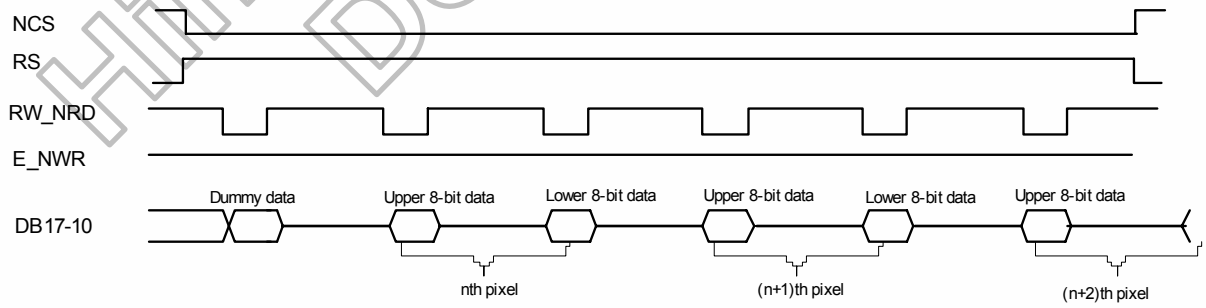


Figure 4. 11 8-bit Parallel Bus Interface Timing (for i80 series MPU)

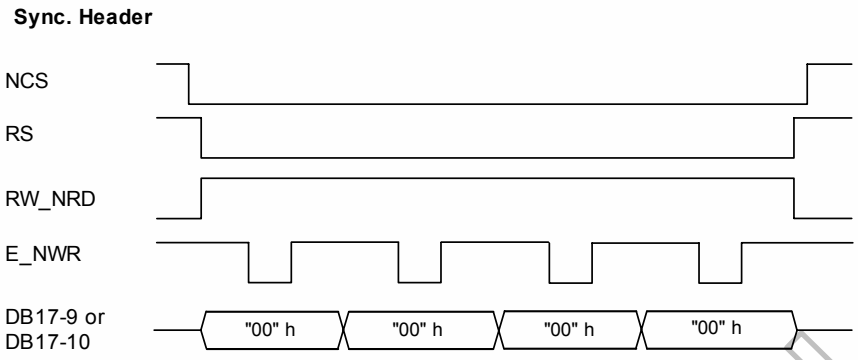


Figure 4. 12 Sync. Header for 9/8-bit Parallel Bus Interface Timing (for i80 series MPU)

4.1.2 Serial Data Transfer Interface

The HX8340-A supports the serial data transfer interface by setting IM3-1 pins to "010". The serial data transfer interface mode is enabled through the chip select line (NCS), and accessed via a three-wire control consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock line (SCL). When HX8340-A is set up for serial data transfer interface mode, the IM0 (ID) pin is used as an ID pin.

In serial data transfer interface mode, the HX8340-A can transfer initially with the start byte at the falling edge of NCS input and finish the transfer at the rising edge of a NCS input.

When the chip select line (NCS) of HX8340-A is set active low, the start byte will be transferred first. The start byte is make up of 6-bit bus device identification code, register select (RS) bit and read /write operation (R/W) bit. The five upper bits of 6-bit bus device identification code must be set 01110 and the least significant bit bus of the identification code can be determined by the IM0/ID pin. Furthermore, two different internal addresses of HX8340-A can be assigned to the register select bit (RS) that is the seventh bit bus of the start byte. The cases of write data to the index register or read the status must be setting RS = 0, and then the cases of write or read an instruction or GRAM data must be setting RS = 1. The read or write function is selected according to the eighth bit bus of the start byte (R/W bit). The data is received when R/W = 0, and is transmitted when R/W = 1. Table 4.3 is list different conditions when change the RS and R/W bit.

When the serial data transfer interface is enabled, the HX8340-A starts taking in start byte and subsequent data that is transferred with the MSB first. Further, the registers of 16-bit bus format can be dividing to the upper eight bits as the first byte and lower eight bits as second byte when HX8340-A are executed from the MSB after transferring two bytes. The HX8340-A executed the write data operation to the GRAM after two-byte and then automatically expanded to the 18-bit bus format (Figure 4.13). When the read status/register operation is executed, the prior byte after start byte is invalid, and then the HX8340-A starts to read correct status/register data from second byte. As well as, when the read GRAM data operation, the prior five bytes of GRAM read data after the start byte are invalid. The HX8340-A starts to read the correct GRAM data from the sixth byte.

RS	R/W	Function
0	0	Index register set
0	1	Status read
1	0	Register or GRAM data write
1	1	Register or GRAM data read

Table 4. 3 The Function of RS and R/W Bit bus

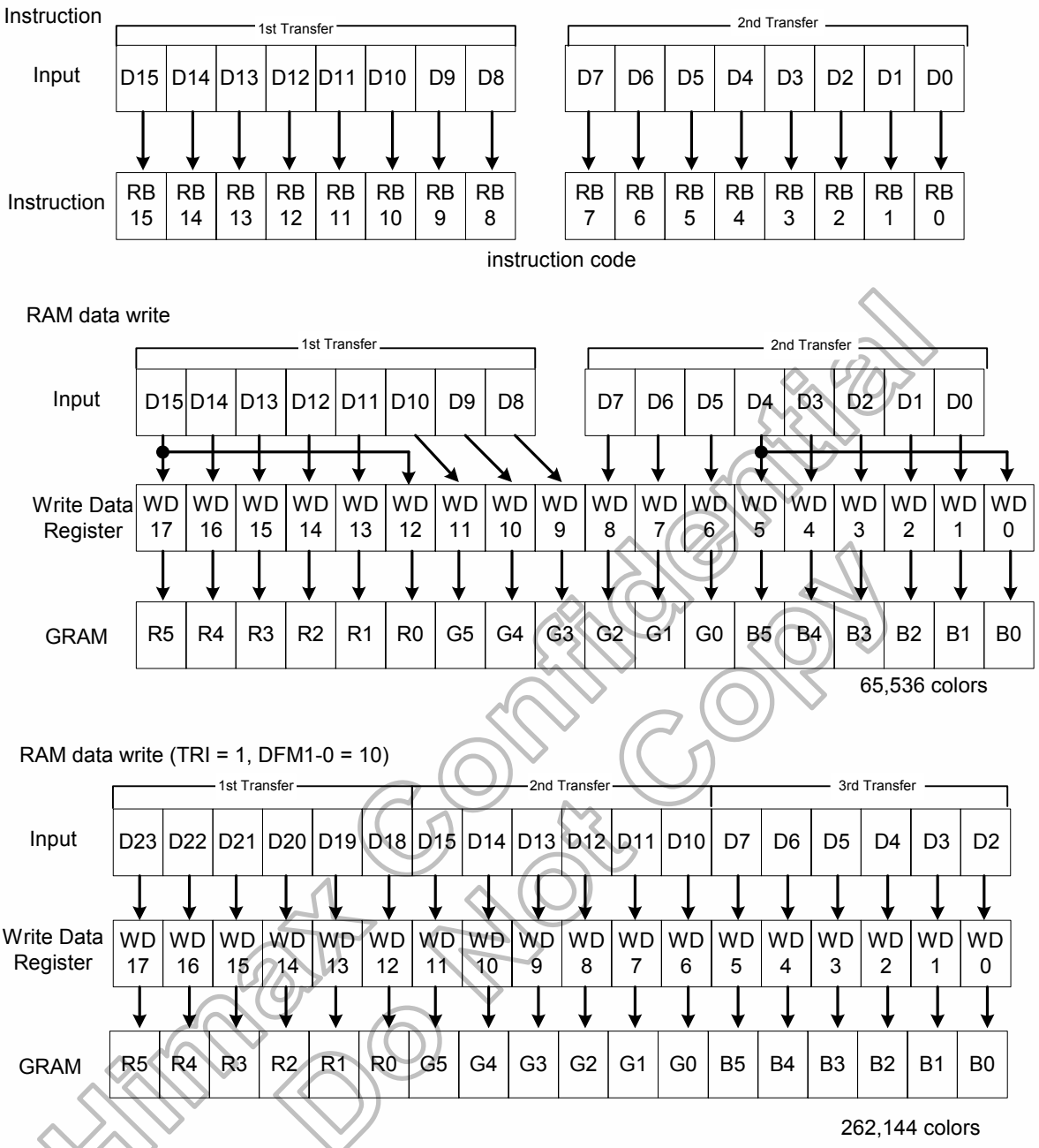
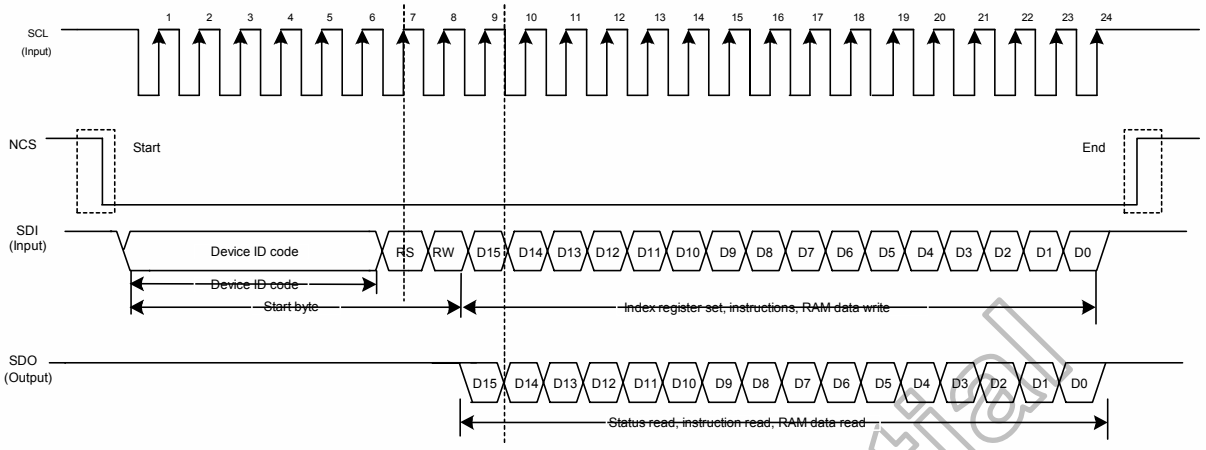
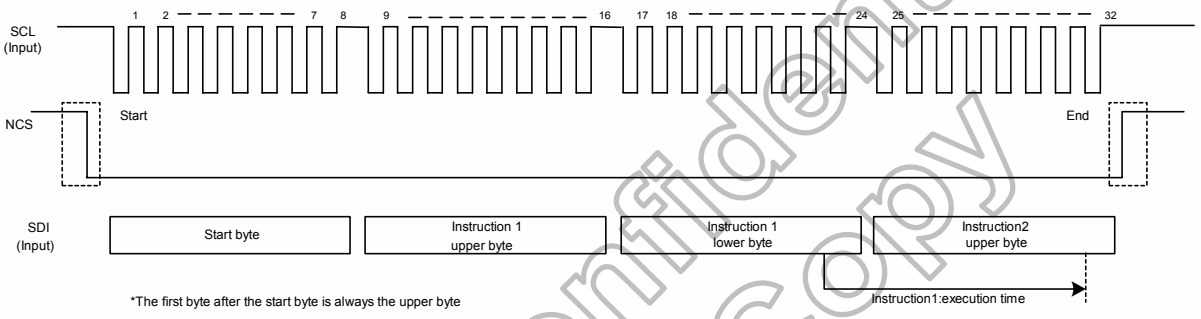


Figure 4. 13 Data Format of Serial Data Transfer Interface GRAM

A)Basic Timing Transfer Format through Clock-Synchronized Serial Data Transfer Interface

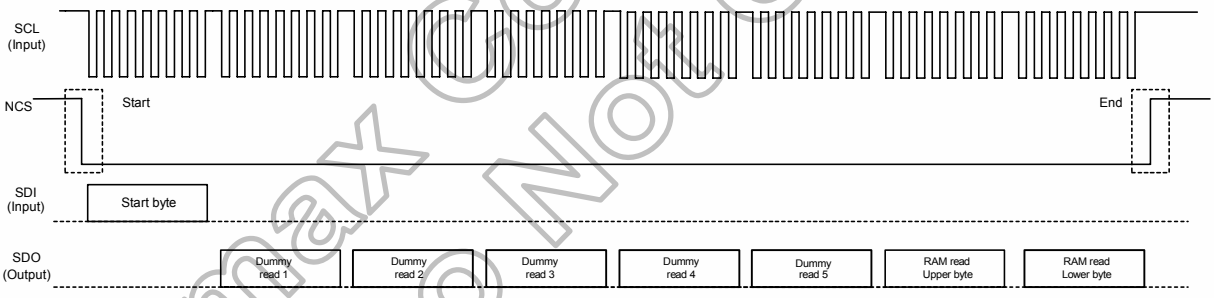


B)Timing of Consecutive Data-write through Clock-synchronized Serial Data Transfer Interface



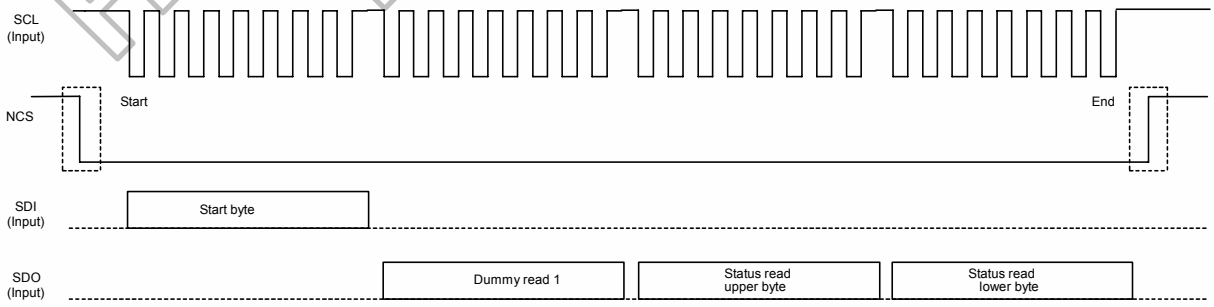
*The first byte after the start byte is always the upper byte

C) Timing Format of GRAM-Data Read



Note: A RAM data read operation follows 5-byte dummy read operations.

D) Timing Format of Status Read/ Instruction Read



Note: One byte of the read data after the start byte are invalid. The HX8309-A starts to read the correct status or instruction data from the second byte

Figure 4. 14 Data Transfer through Serial Data Transfer Interface

4.2 Vsync Interface

The HX8340-A supports the VSYNC interface mode that executes the display operation by the internal clocks. The internal clocks is generated from internal oscillators and synchronized with the frame synchronization signal VSYNC. When the VSYNC interface mode is selected, the interface display a moving picture through system interface with minimum modification that re-writes display data to the internal GRAM in a high speed RAM function. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

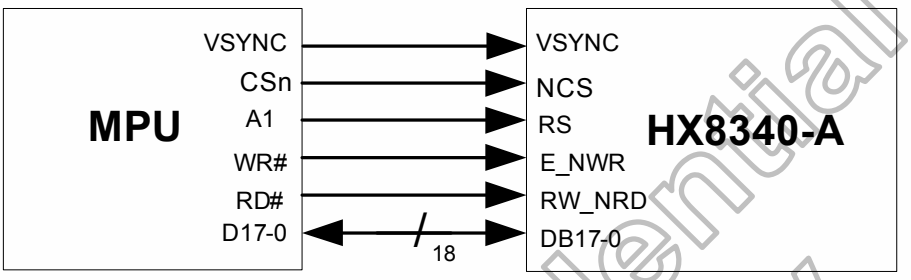


Figure 4. 15 VSYNC Interface to MPU

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 4. 4 DIM Bit Set

When the HX8340-A is set up in VSYNC interface mode, the interface is used to display a moving picture when writing data to GRAM in high speed with low power consumption. Therefore, the VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It requires GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP, BP and display lines duration (NL):

$$Internal\ ocillator\ clock\ (f_{osc})[Hz] = Frame\ Frequency \times [Display\ Lines(NL) + FP + BP] \times RTN \times frequency\ \ fluctuation$$

The parameter of frequency fluctuation is ascribed to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

The minimum speed for RAM can be computed by the following formula:

$$The\ Min.\ RAM\ Write\ Speed\ [Hz] \geqq \frac{176 \times DisplayLines(NL) \times f_{osc}}{[Back\ Porch(BP) + DisplyLines(NL) - margin\ lines] \times RTN}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the HX8340-A start the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting a internal oscillator clock (fosc) first.
An example of internal oscillator clock (fosc) and minimum speed for RAM writing set up in VSYNC interface mode is as follows.

Example

Display size: 176RGB*200 lines
Lines of be used: 200 lines (11000)
FP: 2 lines (0010)
BP: 14 lines (1110)

Frequency fluctuation: 5%
Frame frequency: 60Hz

Internal oscillator clock (fosc) [Hz] = 60 × [200 + 2 +14] × 16 × (1.05/0.95) ≒ 229 kHz
The Min. RAM Write Speed [Hz] ≧ 176 × 200 × 229k /{ [14 + 200 -2] × 16} ≒ 2.37MHz

In this example, the minimum RAM write speed of VSYNC interface is 2.37MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the HX8340-A initiate the display operation and make it possible to re-write the display area set previously. Further, if the display area were different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.

When the HX8340-A make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 4.16 illustrates the process of VSNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.

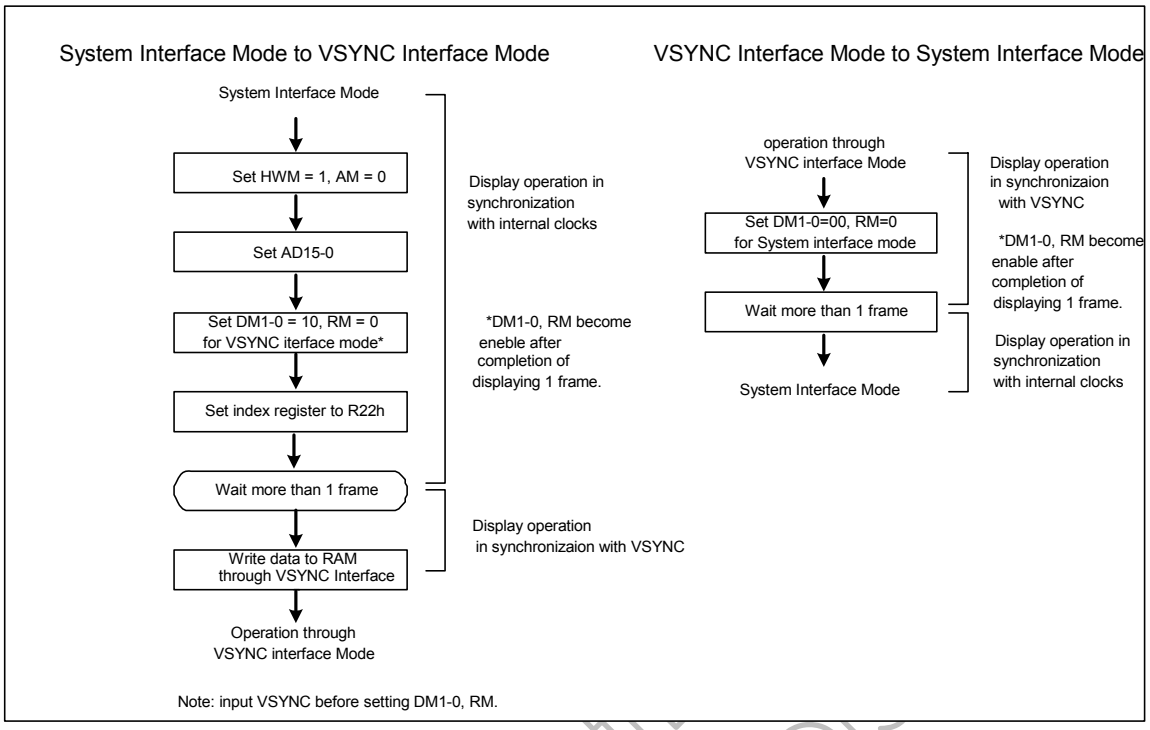


Figure 4. 16 VSYNC Interface with Internal Clock and System Interface with Internal Clock Mode Transition

When HX8340-A is set up on VSYNC interface mode, it would access RAM in high speed with low power consumption for displaying a moving picture. But the partial display function, vertical scroll function and interlaced scan function are invalidity functions in VSYNC interface mode.

4.3 RGB Interface

The HX8340-A supports the RGB interface that display operations that executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE) be described on Table 4.5. The RGB interface can be used by setting DM1-0=01 and RM=1. In RGB interface mode, with use of a window address function, enables to display data in a moving picture area and makes it possible to transfer the display only by re-writing a screen with minimum data transfers.

EPL	ENABLE	RAM Write	RAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

Table 4. 5 EPL and ENABLE Set

When the HX8340-A set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continues until the next input of the VSYNC signal.

The HX8340-A supports two types of RGB interface mode; the difference between them is the RAM access using the RGB interface (PD17-0) or system interface (DB17-0). The data written to the internal GRAM were synchronized with DOTCLK inputs when ENABLE is setting low. Contrary to set ENABLE high, the data written to the GRAM would be entered to the process of using the system interface. Further, when select to use system interface, set ENABLE high to stop using the RGB interface for writing data, and then set the RAM access setting bit bus (RM) low to invert RAM access operation by using system interface. After that, set address AD15-0 on falling edge of VSYNC and then set the index field of register (R22h) to access RAM via the system interface. The HX8340-A allows rewriting data in the still picture area by using the system interface when displaying a moving picture in RGB interface mode. When return to use RGB interface to access RAM, set address AD 15-0, RAM access setting bit bus (RM=1) and the index field of register (R22h) before accessing RAM via RGB interface.

The Figure 4.16 is shown the process of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

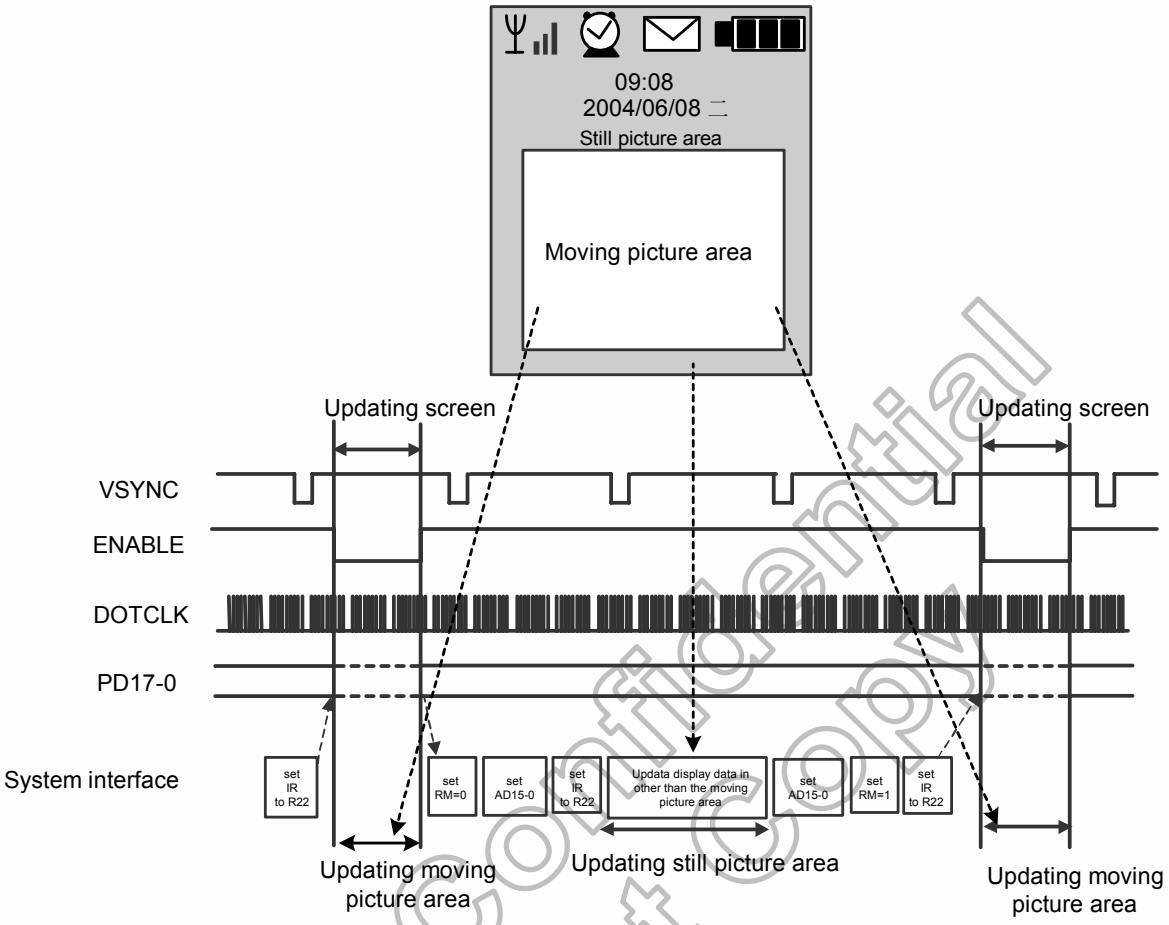


Figure 4. 17 Example of Update Still and Moving Picture

When set up in RGB interface mode, the used of high speed RAM write mode to write data to the internal GRAM and GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal. Such as VSYNC interface mode, partial screen display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

When the HX8340-A make the transition with system interface mode and RGB interface mode, the sequence of switching process must be following as Figure 4.18.

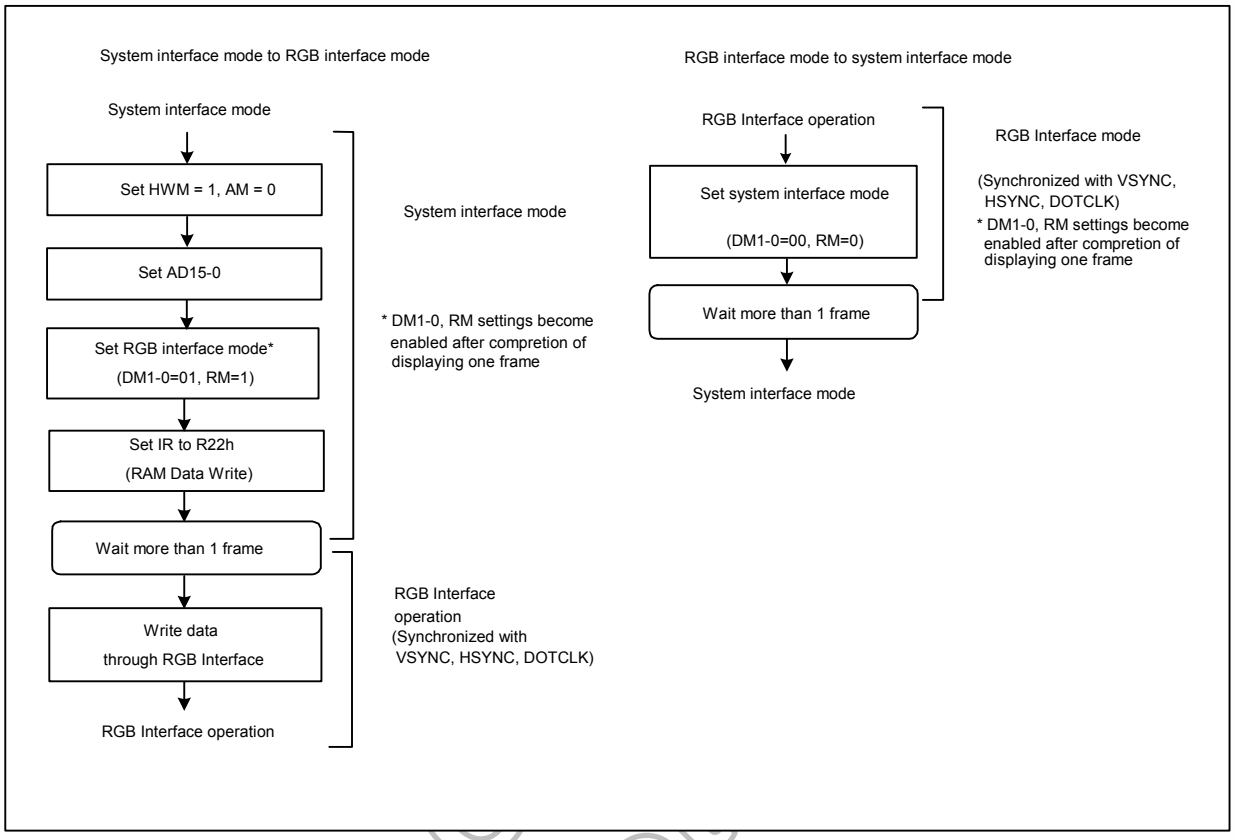


Figure 4. 18 Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure 4.19.

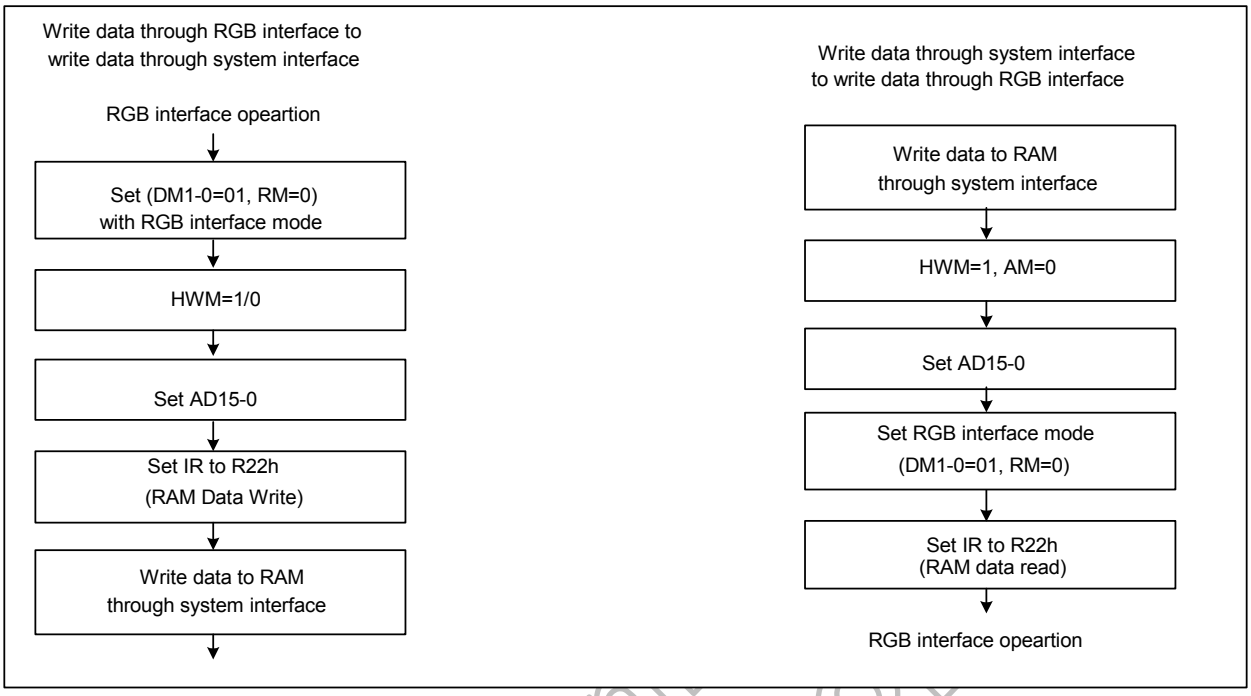


Figure 4. 19 RAM Data Write Sequence through System Interface or RGB Interface during RGB Interface Mode

The HX8340-A supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

18-bit bus RGB interface

The 18-bit interface can be used by setting RIM1-0 bits to “00”. The Figure 4.20 is the example of 18-bit RGB interface with LCD Controller and HX8340-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE). The Figure 4.21 is the data format of 18-bit RGB interface.

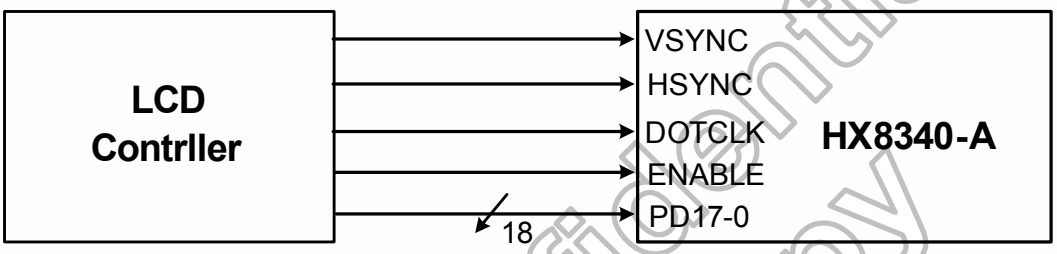


Figure 4. 20 18-bit RGB Interface

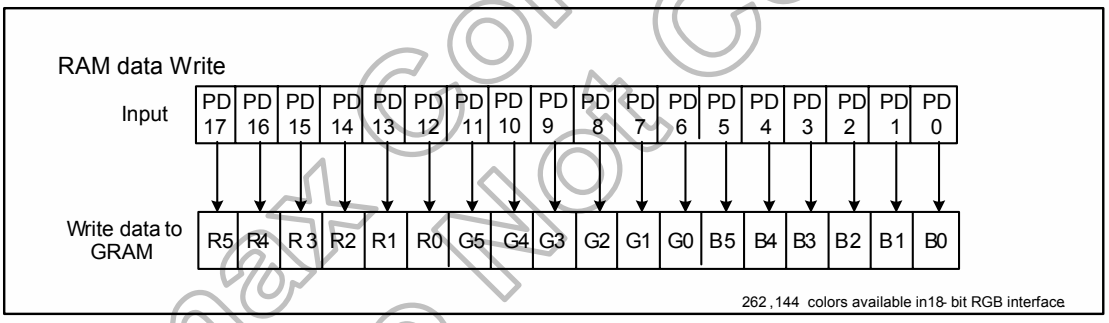


Figure 4. 21 Data Format for 18-bit Interface

16-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “01”. The Figure 4.22 is the example of 16-bit bus RGB interface with LCD Controller and HX8340-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-13, PD11-1 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (PD12, PD0) must be fixed to the IOVcc or VSSD level. The Figure 4.23 is the data format of 16-bit RGB interface.

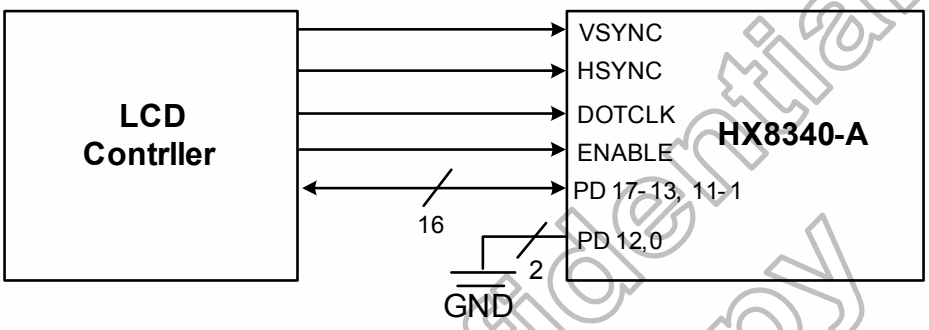


Figure 4. 22 16-bit RGB Interface

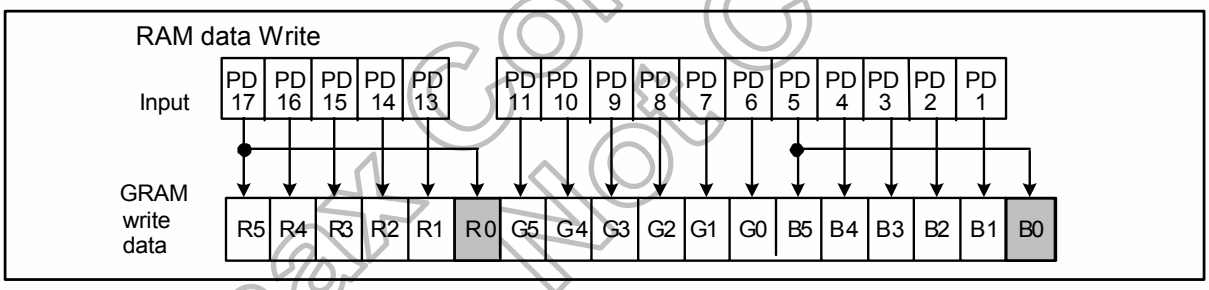


Figure 4. 23 Data Format for16-bit Interface

6-bit bus RGB interface

The 6-bit bus interface can be used by setting RIM1-0 bits to “10”. The Figure 4.24 is the example of 6-bit bus RGB interface with LCD Controller and HX8340-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-12 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins (PD11-0) must be fixed to the IOVcc or VSSD level. The Figure 4.25 is the data format of 6-bit bus RGB interface.

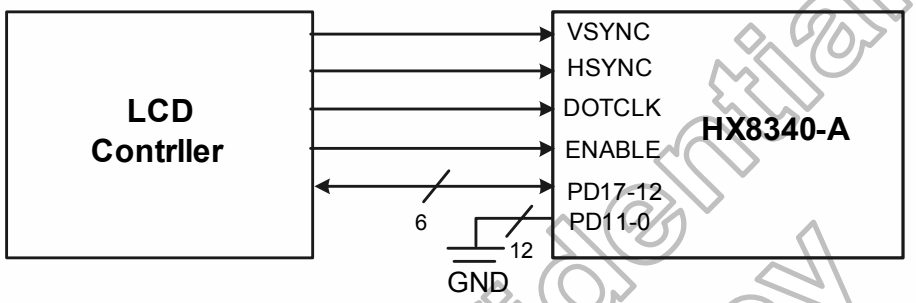


Figure 4. 24 6-bit RGB Interface

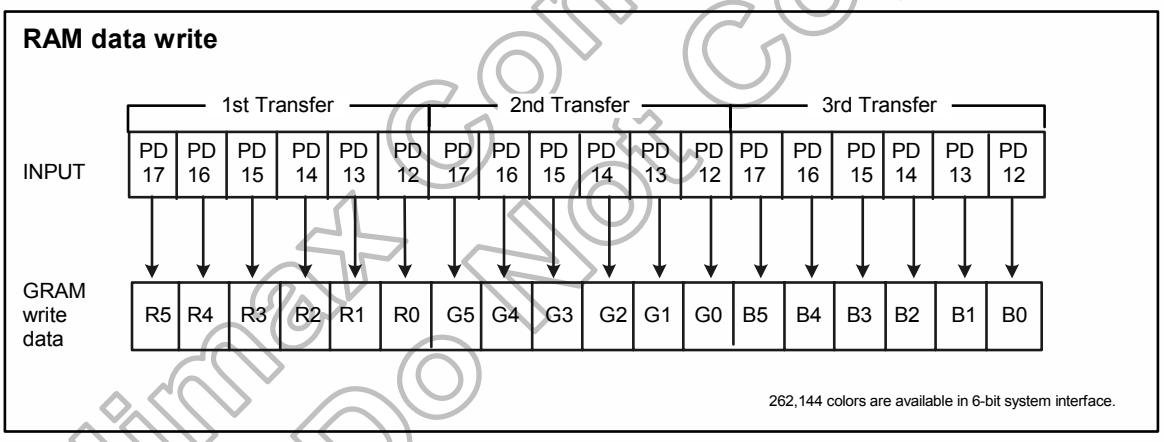


Figure 4. 25 Data Format for 6-bit Interface

5. Function Description

5.1 Graphics RAM

The HX8340-A have an internal graphics RAM that stores 87,120 bytes bit-pattern data, where one pixel is expressed by 18 bits. The GRAM address map is listed as follow:

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=1	GS=0	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G220	G1	0000H			0001H			0002H			---	00ACH			00ADH			00AEH			00AFH		
G219	G2	0100H			0101H			0102H			---	01ACH			01ADH			01AEH			01AFH		
G218	G3	0200H			0201H			0202H			---	02ACH			02ADH			02AEH			02AFH		
G217	G4	0300H			0301H			0302H			---	03ACH			03ADH			03AEH			03AFH		
G216	G5	0400H			0401H			0402H			---	04ACH			04ADH			04AEH			04AFH		
G215	G6	0500H			0501H			0502H			---	05ACH			05ADH			05AEH			05AFH		
G214	G7	0600H			0601H			0602H			---	06ACH			06ADH			06AEH			06AFH		
G213	G8	0700H			0701H			0702H			---	07ACH			07ADH			07AEH			07AFH		
G212	G9	0800H			0801H			0802H			---	08ACH			08ADH			08AEH			08AFH		
G211	G10	0900H			0901H			0902H			---	09ACH			09ADH			09AEH			09AFH		
G210	G11	0A00H			0A01H			0A02H			---	0AACH			0AADH			0AAEH			0AAFH		
G209	G12	0B00H			0B01H			0B02H			---	0BACH			0BADH			0BAEH			0BAFH		
G208	G13	0C00H			0C01H			0C02H			---	0CACH			0CADH			0CAEH			0CAFH		
G207	G14	0D00H			0D01H			0D01H			---	0DACH			0DADH			0DAEH			0DAFH		
G206	G15	0E00H			0E01H			0E01H			---	0EACH			0EADH			0EAEH			0EAFH		
⋮	⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	G211	D200H			D201H			D202H			---	D2ACH			D2ADH			D2AEH			D2AFH		
G9	G212	D300H			D301H			D302H			---	D3ACH			D3ADH			D3AEH			D3AFH		
G8	G213	D400H			D401H			D402H			---	D4ACH			D4ADH			D4AEH			D4AFH		
G7	G214	D500H			D501H			D502H			---	D5ACH			D5ADH			D5AEH			D5AFH		
G6	G215	D600H			D601H			D602H			---	D6ACH			D6ADH			D6AEH			D6AFH		
G5	G216	D700H			D701H			D702H			---	D7ACH			D7ADH			D7AEH			D7AFH		
G4	G217	D800H			D801H			D802H			---	D8ACH			D8ADH			D8AEH			D8AFH		
G3	G218	D900H			D901H			D902H			---	D9ACH			D9ADH			D9AEH			D9AFH		
G2	G219	DA00H			DA01H			DA02H			---	DAACH			DAADH			DAAEH			DAAFH		
G1	G220	DB00H			DB01H			DB02H			---	DBACH			DBADH			DBAEH			DBAFH		

Table 5. 1 GRAM Address and Display Panel Position (SS ="0", BGR = "0")

80-System 18-bit bus Interface

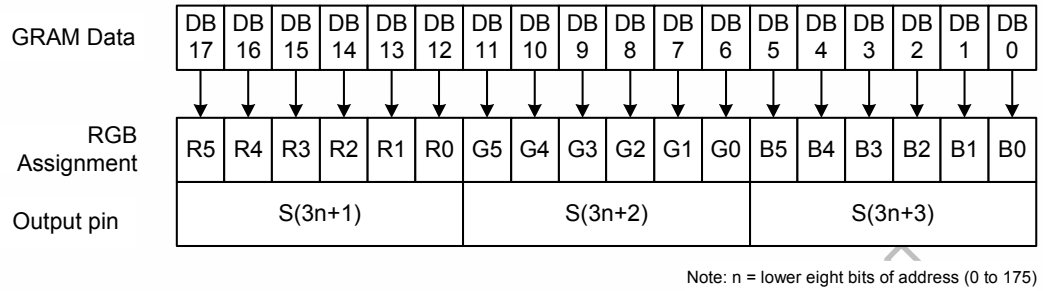
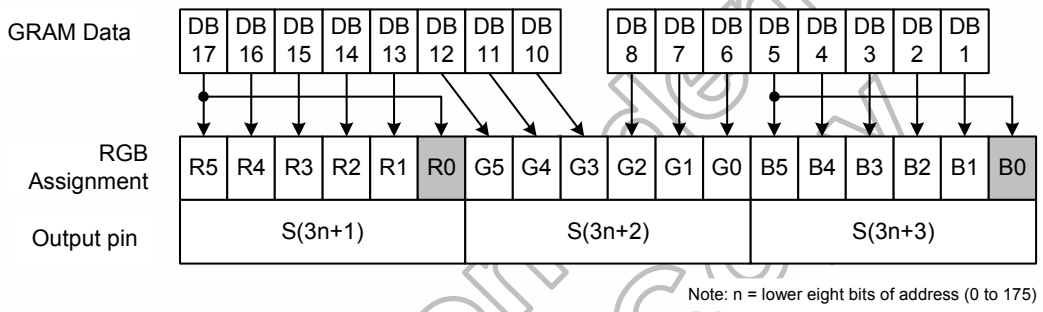
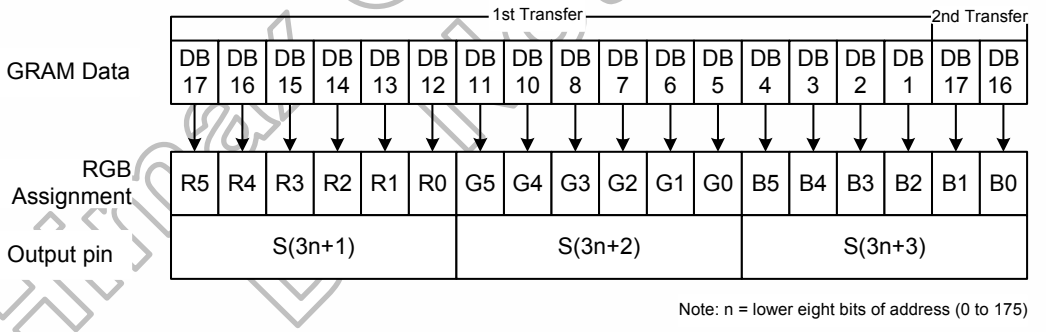


Figure 5. 1 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "0", BGR = "0")

80-System 16-bit bus Interface



80-System 16-bit Interface MSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "10"



80-System 16-bit Interface LSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "11"

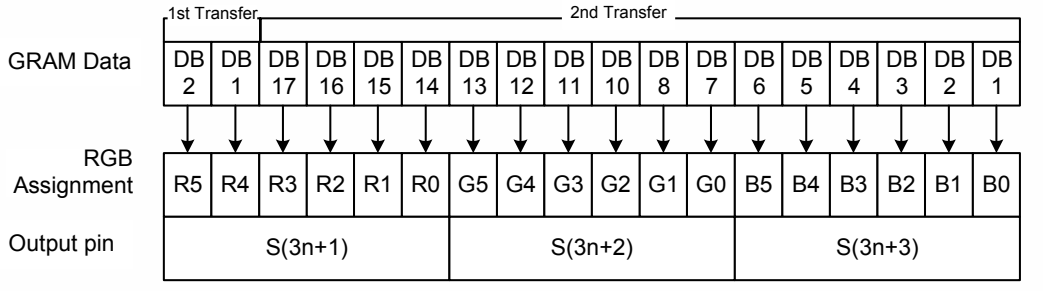


Figure 5. 2 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "0", BGR = "0")

80-System 9-bit bus Interface

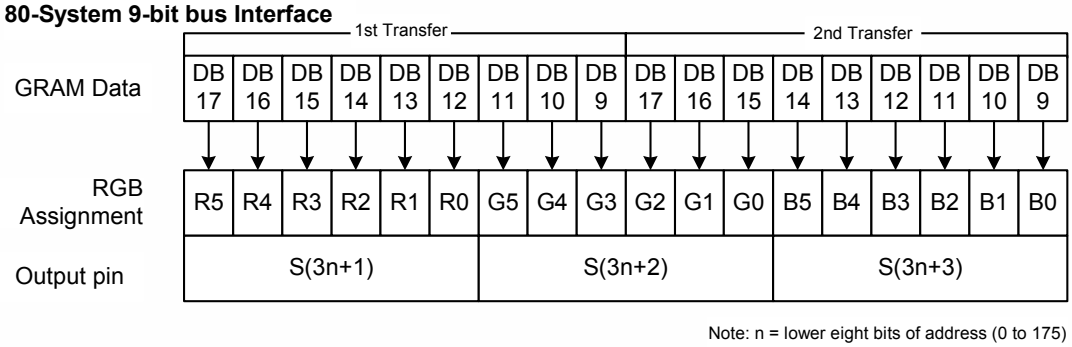
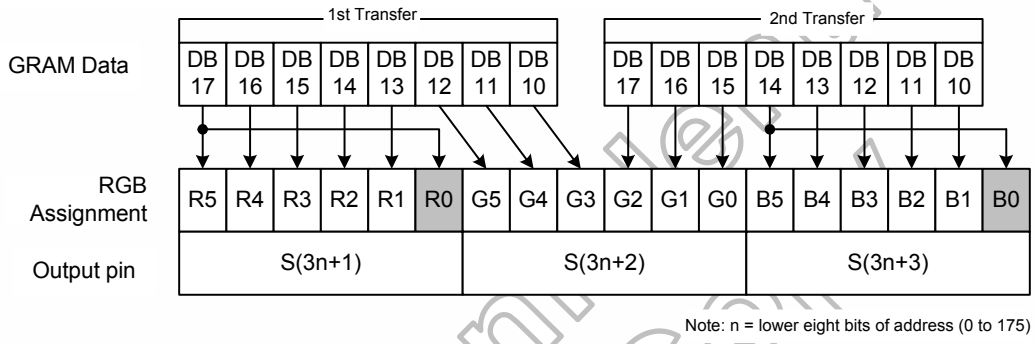
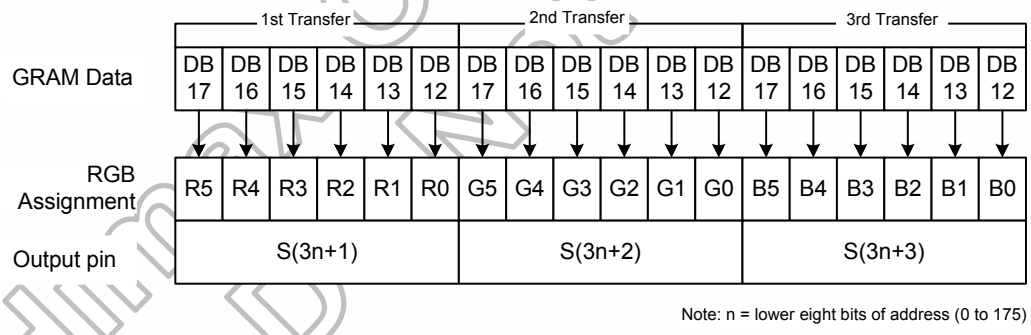


Figure 5. 3 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = "0", BGR = "0")

80-System 8-bit Interface/Serial Data Transfer Interface (2 transfers/ pixel)



80-System 8-bi t Interface (3 transfers/pixel, 262k colors: TRI=1, DFM1-0=10)



80-System 8-bi t Interface (3 transfers/pixel, 65k colors: TRI=1, DFM1-0=11)

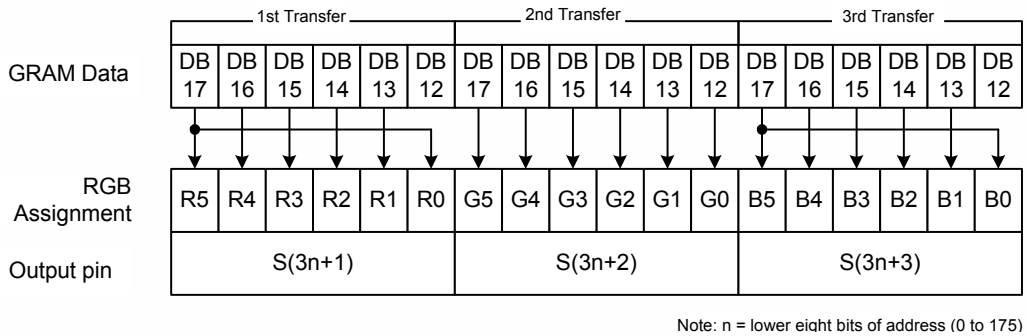
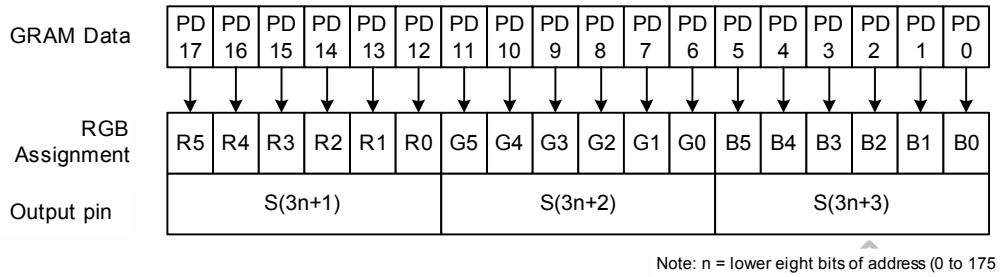


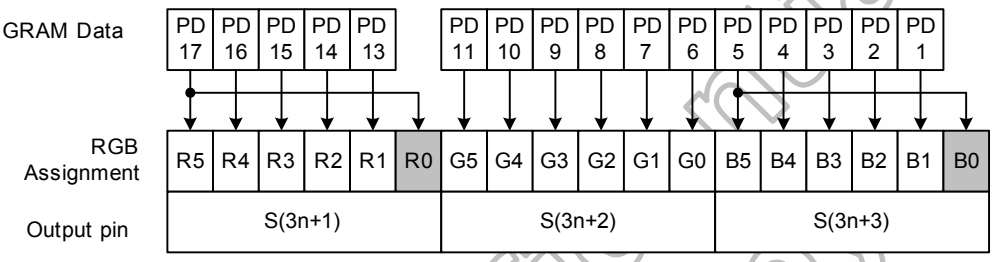
Figure 5. 4 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = "0", BGR = "0")

18-Bit RGB Interface



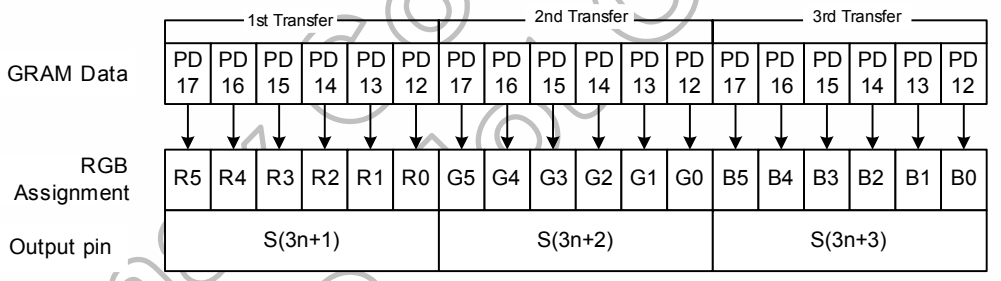
Note: n = lower eight bits of address (0 to 175

16-Bit RGB Interface



Note: n = lower eight bits of address (0 to 175

6-Bit RGB Interface



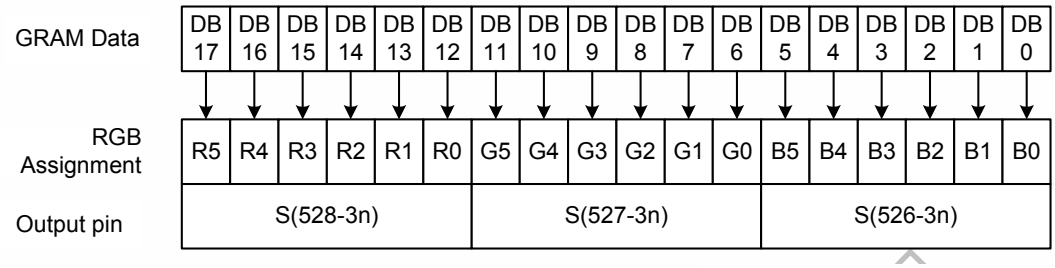
Note: n = lower eight bits of address (0 to 175)

Figure 5. 5 GRAM Data and Display Data of RGB Interface (SS = "0", BGR = "0")

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	---------	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---------	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G1	G220	00AFH			00AEH			00ADH			00ACH			---------	0002H			0001H			0000H		
G2	G219	01AFH			01AEH			01ADH			01ACH			---------	0102H			0101H			0100H		
G3	G218	02AFH			02AEH			02ADH			02ACH			---------	0202H			0201H			0200H		
G4	G217	03AFH			03AEH			03ADH			03ACH			---------	0302H			0301H			0300H		
G5	G216	04AFH			04AEH			04ADH			04ACH			---------	0402H			0401H			0400H		
G6	G215	05AFH			05AEH			05ADH			05ACH			---------	0502H			0501H			0500H		
G7	G214	06AFH			06AEH			06ADH			06ACH			---------	0602H			0601H			0600H		
G8	G213	07AFH			07AEH			07ADH			07ACH			---------	0702H			0701H			0700H		
G9	G212	08AFH			08AEH			08ADH			08ACH			---------	0802H			0801H			0800H		
G10	G211	09AFH			09AEH			09ADH			09ACH			---------	0902H			0901H			0900H		
G11	G210	0AAFH			0AAEH			0AADH			0AACH			---------	0A02H			0A01H			0A00H		
G12	G209	0BAFH			0BAEH			0BADH			0BACH			---------	0B02H			0B01H			0B00H		
G13	G208	0CAFH			0CAEH			0CADH			0CACH			---------	0C02H			0C01H			0C00H		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G213	G8	D4AFH			D4AEH			D4ADH			D4ACH			---------	D402H			D401H			D400H		
G214	G7	D5AFH			D5AEH			D5ADH			D5ACH			---------	D502H			D501H			D500H		
G215	G6	D6AFH			D6AEH			D6ADH			D6ACH			---------	D602H			D601H			D600H		
G216	G5	D7AFH			D7AEH			D7ADH			D7ACH			---------	D702H			D701H			D700H		
G217	G4	D8AFH			D8AEH			D8ADH			D8ACH			---------	D802H			D801H			D800H		
G218	G3	D9AFH			D9AEH			D9ADH			D9ACH			---------	D902H			D901H			D900H		
G219	G2	DAAFH			DAAEH			DAADH			DAACH			---------	DA02H			DA01H			DA00H		
G220	G1	DBAFH			DBAEH			DBADH			DBACH			---------	DB02H			DB01H			DB00H		

Table 5. 2 GRAM Address and Display Panel Position (SS =”1”, BGR=”1”)

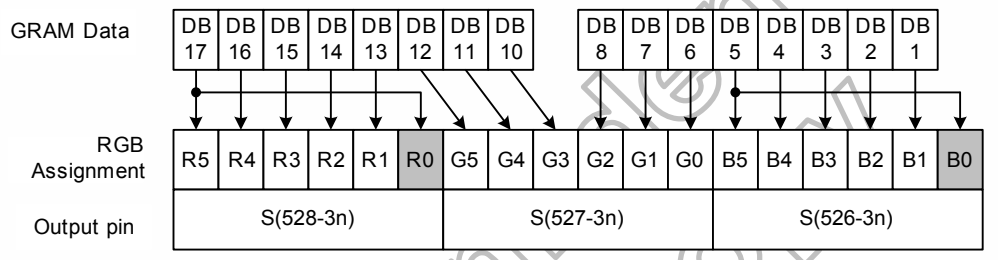
80-System 18-bit bus Interface



Note: n = lower eight bits of address (0 to 175)

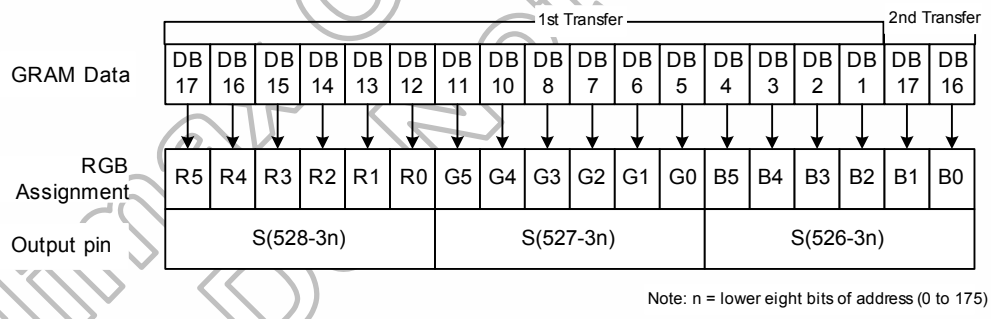
Figure 5. 6 GRAM Data and Display Data of 80-system 18-bit Bus Interface (SS = "1", BGR = "1")

80-System 16-bit bus Interface



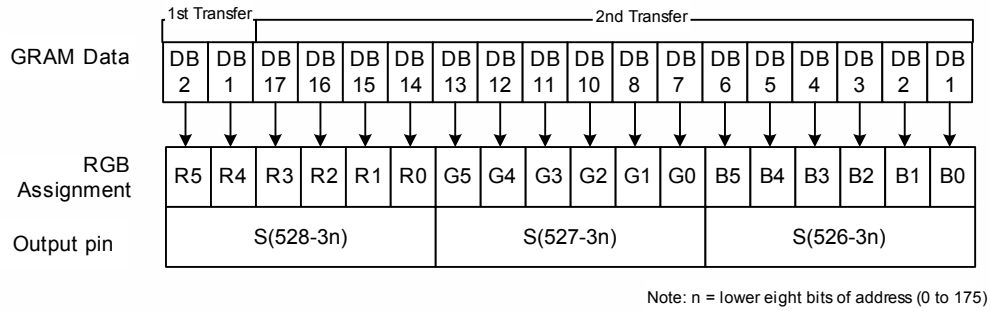
Note: n = lower eight bits of address (0 to 175)

80-System 16-bit Interface MSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "10"



Note: n = lower eight bits of address (0 to 175)

80-System 16-bit Interface LSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM1-0 = "11"



Note: n = lower eight bits of address (0 to 175)

Figure 5. 7 GRAM Data and Display Data of 80-system 16-bit Bus Interface (SS = "1", BGR = "1")

80-System 9-bit bus Interface

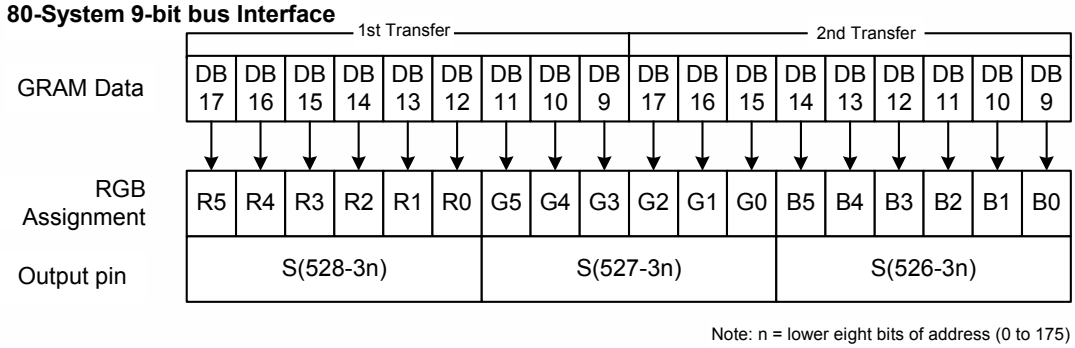
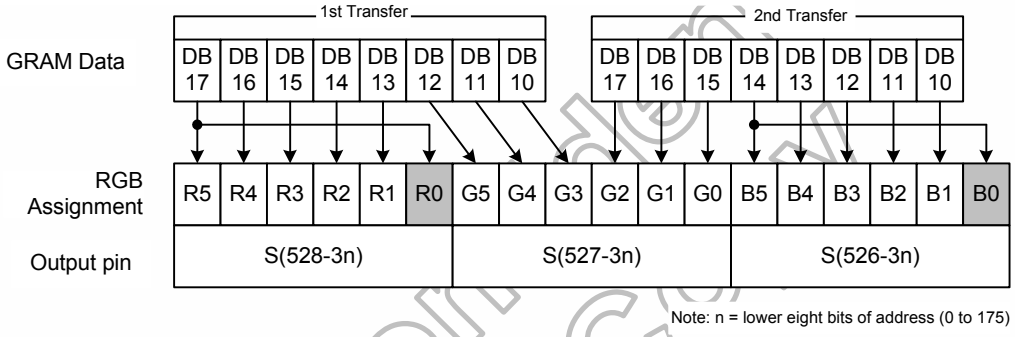
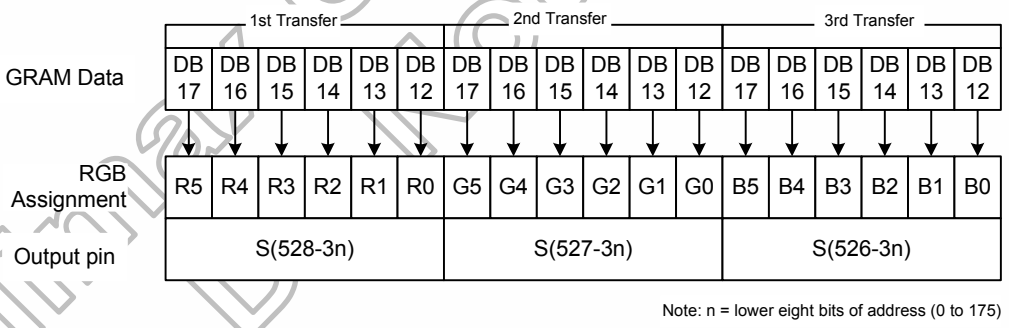


Figure 5. 8 GRAM Data and Display Data of 80-system 9-bit Bus Interface (SS = "1", BGR = "1")

80-System 8-bit Interface/Serial Data Transfer Interface (2 transfers/ pixel)



80-System 8-bi t Interface (3 transfers/pixel, 262k colors: TRI=1, DFM1-0=10)



80-System 8-bi t Interface (3 transfers/pixel, 65k colors: TRI=1, DFM1-0=11)

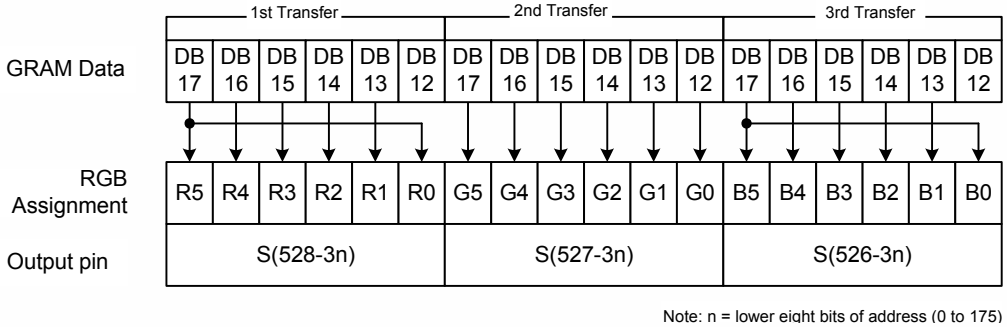
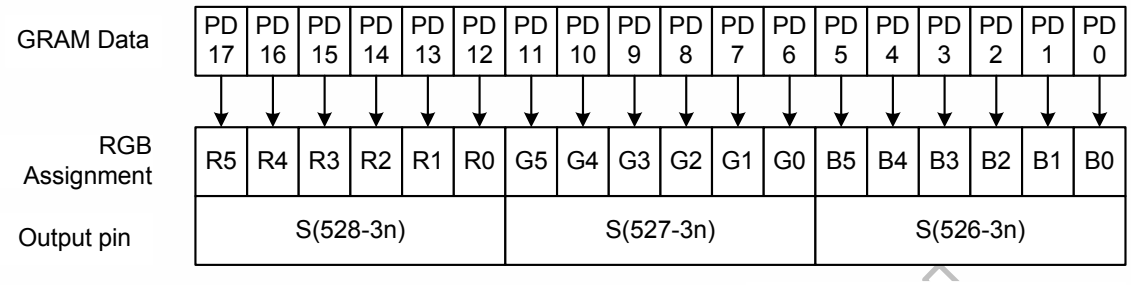


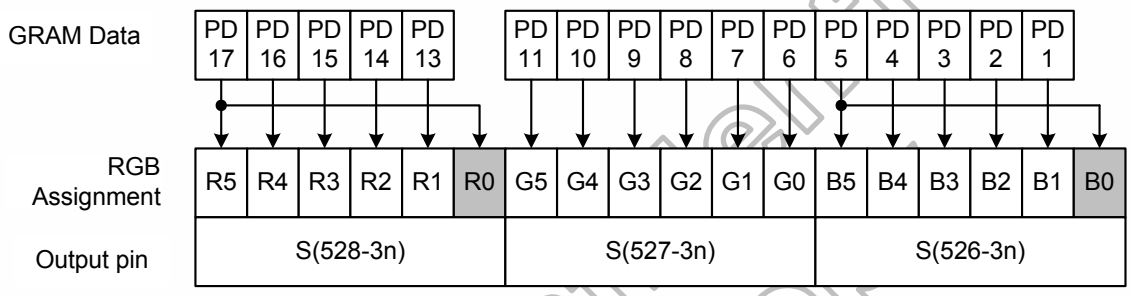
Figure 5. 9 GRAM Data and Display Data of 80-system 8-bit Bus Interface (SS = "1", BGR = "1")

18-Bit RGB Interface



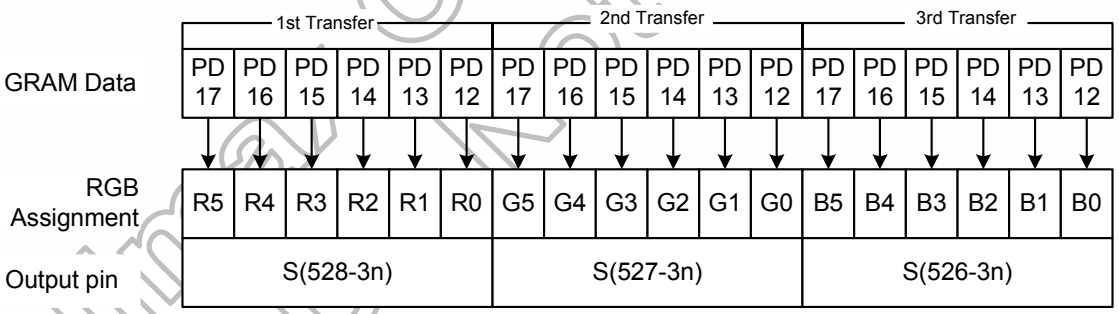
Note: n = lower eight bits of address (0 to 175)

16-Bit RGB Interface



Note: n = lower eight bits of address (0 to 175)

6-Bit RGB Interface



Note: n = lower eight bits of address (0 to 175)

Figure 5. 10 GRAM Data and Display Data of RGB Interface (SS = "1", BGR = "1")

5.1.1 Window Address Function

The HX8340-A contains a GRAM 16-bit bus address counter (AC), which assigns address for writing pixel data to GRAM. The high eight bits of AC are expressed Y address (line address) and the lower eight bits of AC are expressed X address (pixel address). Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (AM bit and I/D bits) setting. However, the AC will be not updated after reading from GRAM.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0). Therefore, data can be written consecutively without thinking a data wrap by those bit function. The address setting of window and GRAM are listed as following:

The window address setting range:

00H≦HSA7-0≦HEA7-0≦AFH
00H≦VSA7-0≦VEA7-0≦DBH

GRAM address setting range:

HSA7-0≦AD7-0≦HEA7-0
VSA7-0≦AD15-8≦VEA7-0

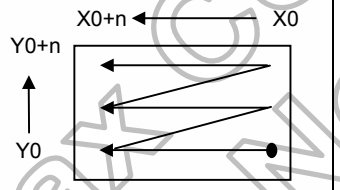
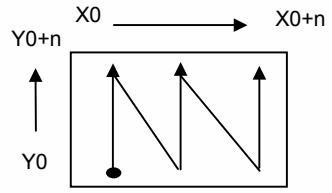
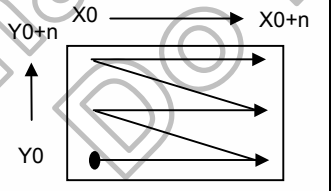
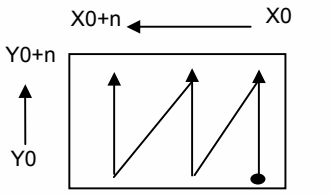
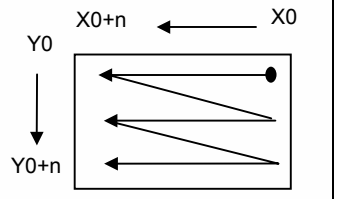
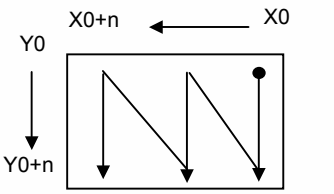
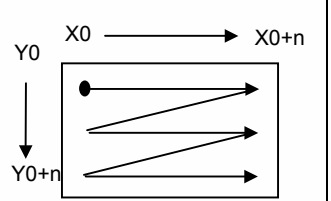
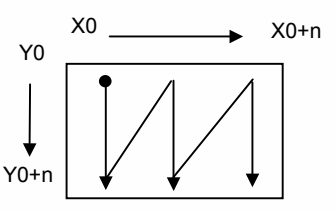
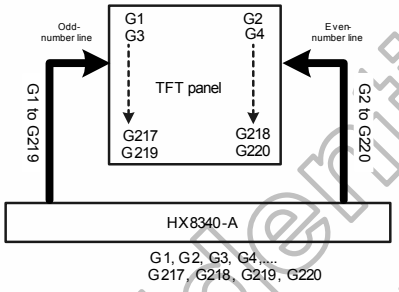
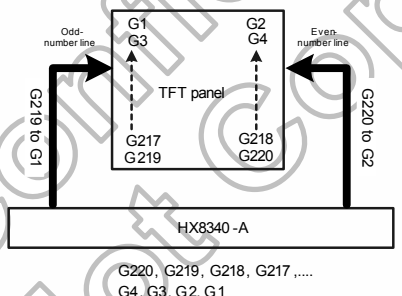
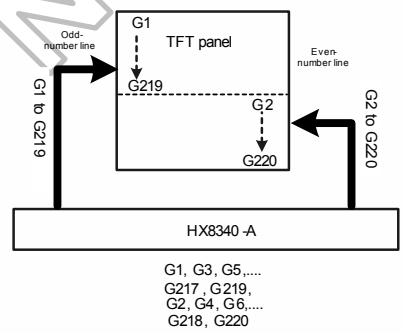
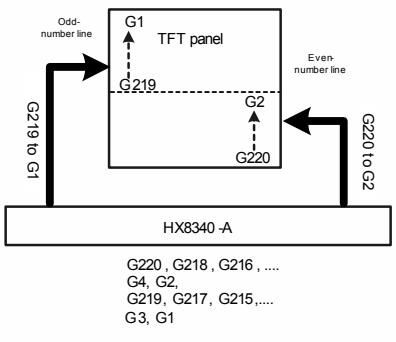
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure 5. 11 Address Update Direction Settings

5.2 Display Function

5.2.1 Scan Mode Setting

The HX8340-A can set SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8340-A.

SM	GS	Scan direction
0	0	
0	1	
1	0	
1	1	

Note: Scan mode setting depends on the design and layout of glass on panel.

Figure 5. 12 SCAN Mode Setting

5.2.2 Partial Screen Display

The HX8340-A has one or two screens driving functions. The position of display screen register (R42h and R43h) can display at any position of the whole screen. The numbers of display lines that display on the first and second windows must be less than total LCD-driving lines setting (NL4-0). The rest display area in the screen should be white display if the type of LCD is normally white and should be black display if the type of LCD is normally black. Therefore, the partial display can reduce the power consumption.

As the below, the first window start line from the SS1 (7-0) and end line at SE1 (7-0), that are specified by the 1st Display Window Driving Position Register (R42h). The second window start line from SS2 (7-0) and end line at SE2 (7-0), that are specified by 2nd Display Window Driving Position Register (R43h). And the second display window is availed when the SPT bit is set to 1. The number of the total selection driving lines included the 1st and 2nd display window must be equal to or less than the LCD Drive Line (NL).

Number of Scan Line: NL(4-0) = "10101" (176 lines)

1st Screen Setting : SS1(7-0) = "0E"h , SE1(7-0) = "19"h
2nd Screen Setting: SS2(7-0) = "4A"h , SE2(7-0) = "5E"h , SPT=1

Figure 5. 13 Partial Screen Display Example in 2-Windows Driving

The conditions of 1st and 2nd Display Window Driving Position Register Setting

The conditions as following must be contented when setting the start line SS1 (7-0) and end line SE1 (7-0) of the 1st display window at register (R42h) and the start line SS2 (7-0) and end line SE2 (7-0) of the 2nd display window at register (R42).

Note: That incorrect display may occur if the condition setting is not contented.

Condition: 0 ≤ SS1 (7-0) ≤ SE1 (7-0) ≤ NL

Register Settings	Display Operation
SE1(7-0) – SS1(7-0) +1 = NL	Whole-Screen Display The area of SE1 (7-0)-SS1 (7-0) is normally displayed
0 < SE1 (7-1) – SS1 (7-0) +1 < NL	Partial screen display The area of SE1 (7-0)-SS1 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Note: The SS2 (7-0) and SE2 (7-0) settings are ignored.

Table 5. 3 Conditions on One Screen Driving (STP = 0)

Condition: 0 ≤ SS1 (7-0) ≤ SE1 (7-0) < SS2 (7-0) ≤ SE2 (7-0) ≤ NL

Register Settings	Display Operation
(SE1 (7-0) – SS1 (7-0) +1) + (SE2 (7-0) – SS2 (7-0)+1) = NL	Whole-Screen Display The area of SE2 (7-0) – SS1 (7-1) is normally displayed
(SE1 (7-0) – SS1 (7-0) +1) + (SE2 (7-0) – SS2 (7-0) +1) < NL	Partial Screen Display The area of SE1 (7-0) – SS1 (7-0) and SE2 (7-0) – SS2 (7-0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Table 5. 4 Condition on Two Screen Driving (STP = 1)

The driver outputs for non-display area on partial display can be specified. Set the values to match the characteristics for the panel.

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	Vcom output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VcomH↔VcomL
0	1	Ignore	Ignore	Reference to PTG1-0	VcomH↔VcomL
1	0	VSSD	VSSD	Reference to PTG1-0	VcomH↔VcomL
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

Table 5. 5 Source and Gate Output in Non-Display Area during Partial Display Function

Setting of the partial display should follow the flow shown as below

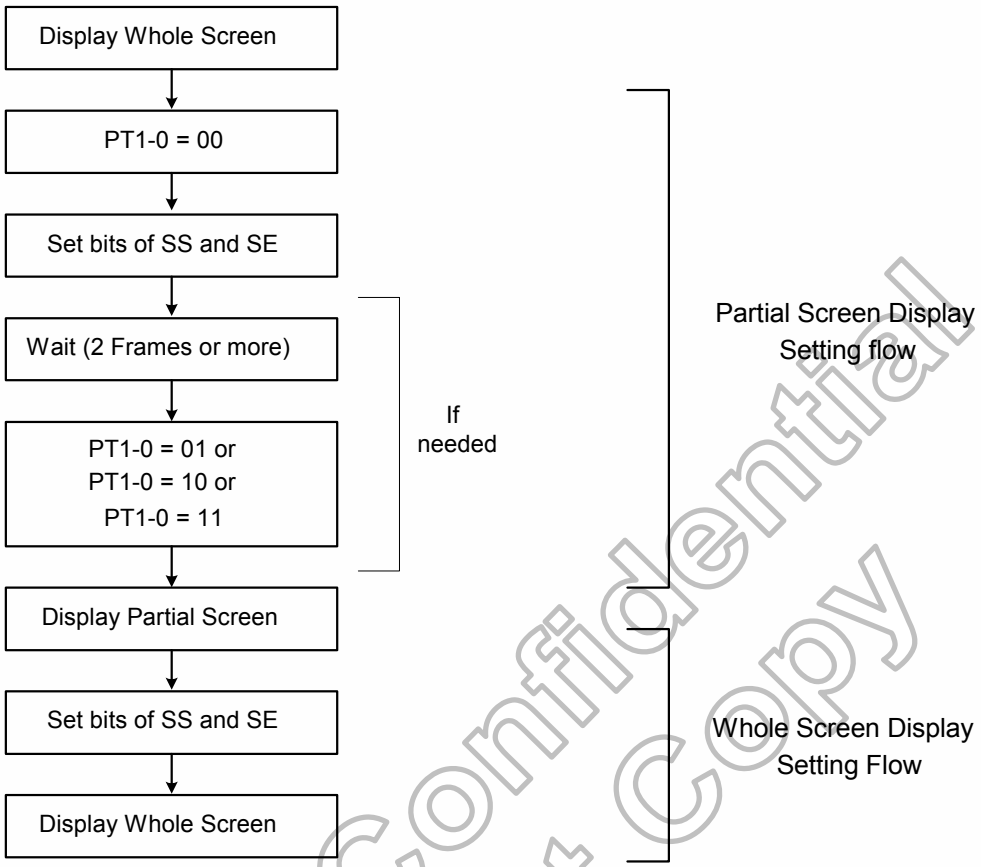


Figure 5. 14 Partial Display Setting Flow

5.2.3 8-Color Display

The HX8340-A supports an 8-color display mode. The grayscale level to be used is V0 and V63 with R5, G5, B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

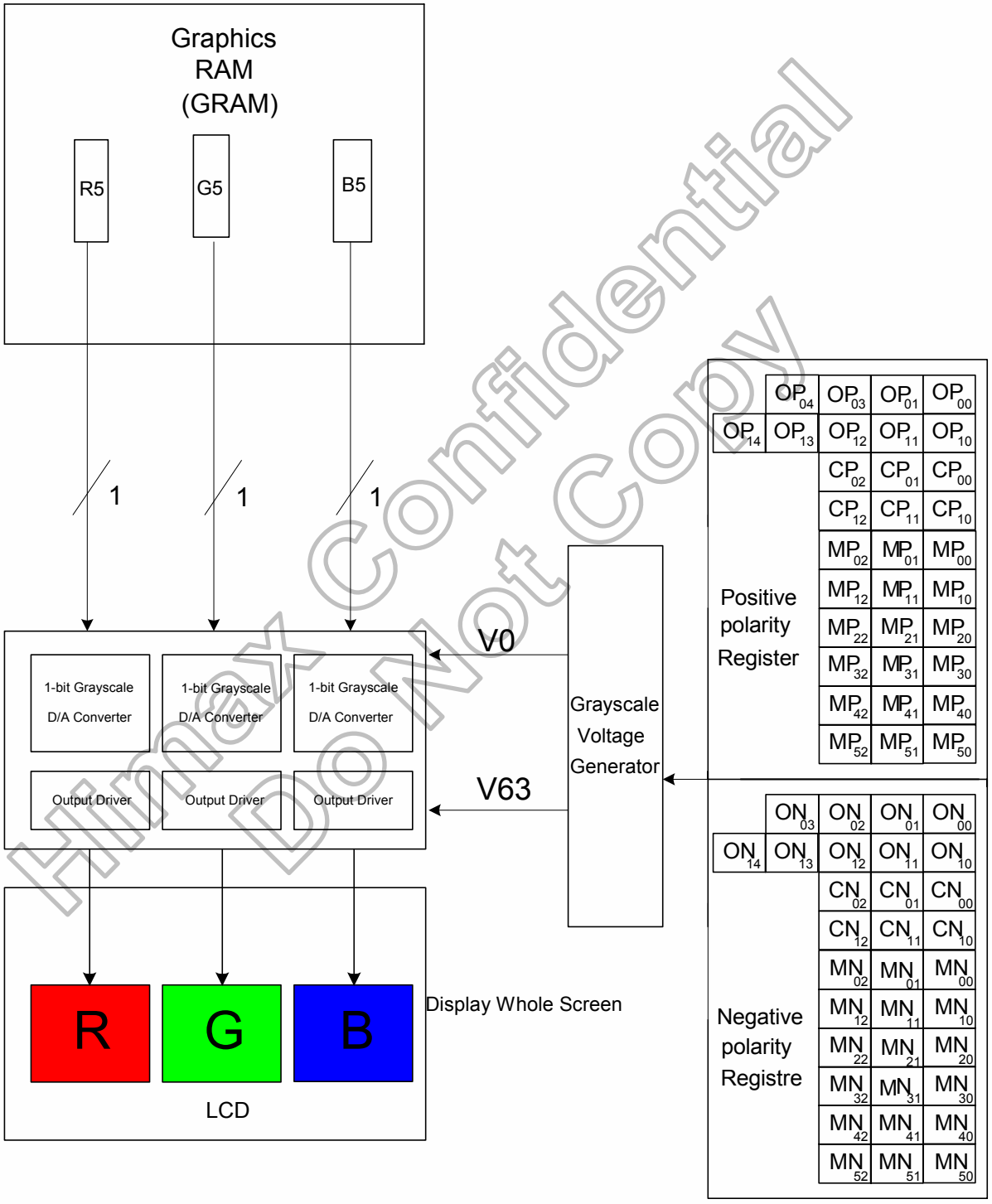


Figure 5. 15 Grayscale Control in 8-Color Mode

The follow figure is the switch sequence between the 262,144-color mode and 8-color mode:

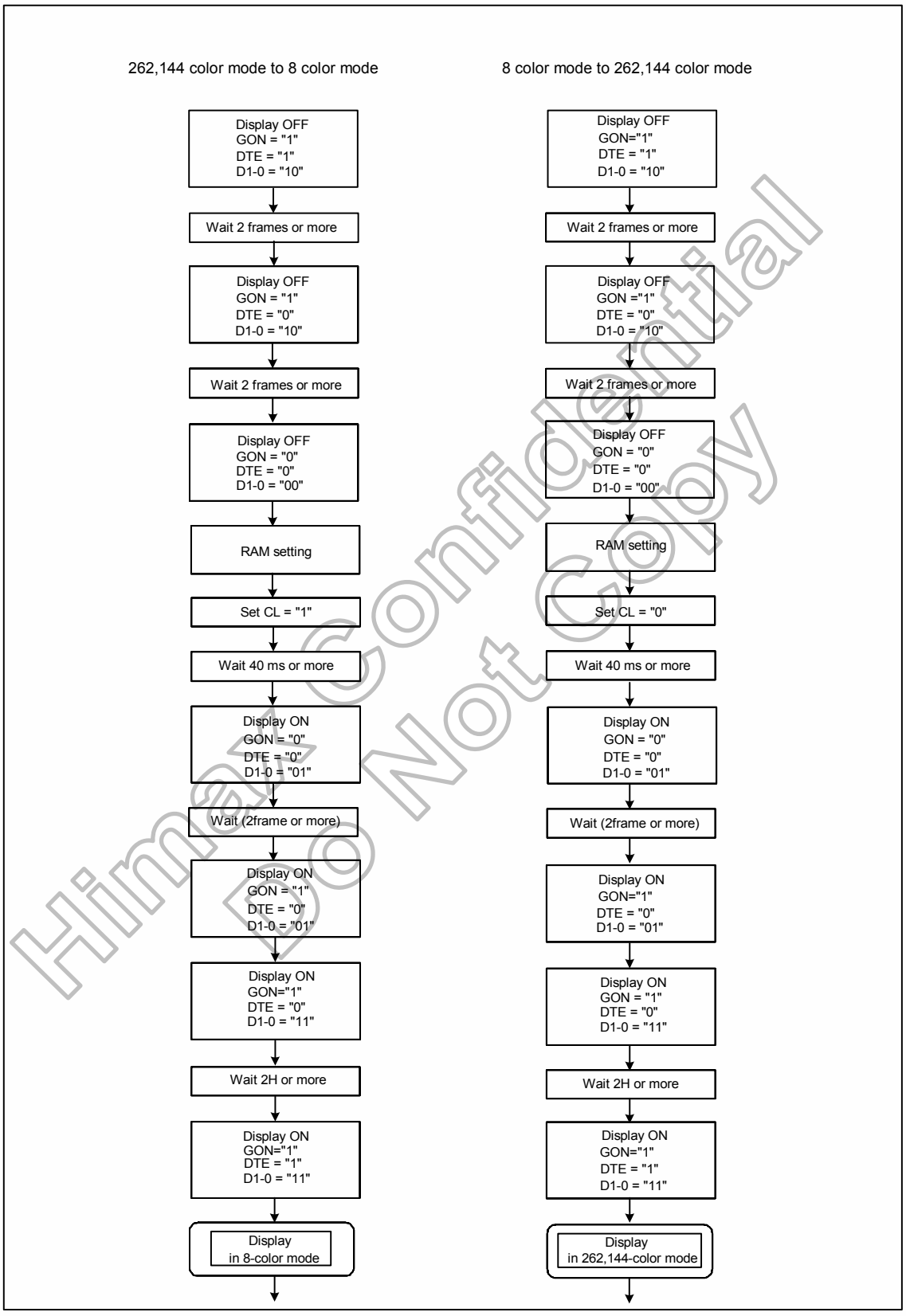
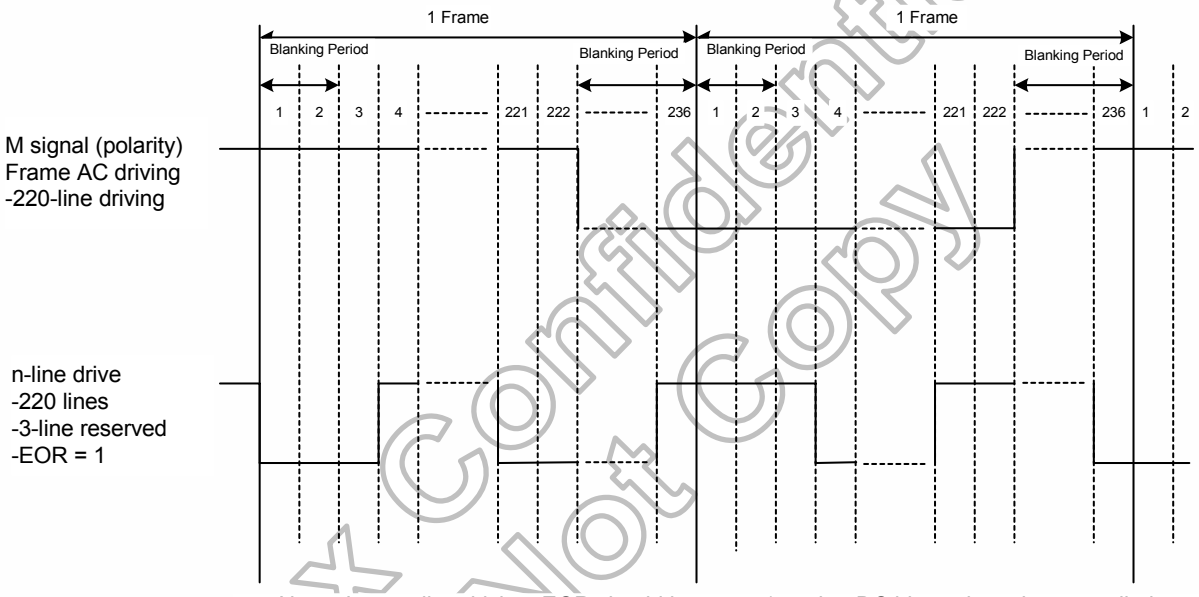


Figure 5. 16 Switch Sequence between 262,144-color Mode and 8-color Mode

5.2.4 N-line Inversion LCD Drive

The HX8340-A supports frame inversion and n-line inversion LCD current driving, which n chooses 1~64. The inversion operation is controlled by POL (Polarity of Liquid Crystal) signal which interval is set by NW5-0 bits in R02h register. The HX8340-A internally transfers POL signal for alternating the VCOM voltage and alternates source output voltage according to gamma register with POL signal, which changes the polarity of LCD driving voltage. When a display quality problem occurs, the n-line inversion LCD drive can improve the quality by setting proper n value.
The value of n also represented by the NW bits+1, which represented LCD alternating frequency becomes high when the number of inversion lines were setting a smaller value, hence, in the LCD cells, the charge or discharge current is increased.



Note : In an n-line driving, EOR should be set to 1 so that DC bias voltage is not applied

Figure 5. 17 N-line Inversion Driving Diagram

5.2.5 Interlaced Driving Function

The HX8340-A has an interlaced function that divided one frame into 3 fields to drive. The LCD to avoid flicker to confirm the display quality with the actual LCD display then determined the number of fields. As following table, the gate selection where the number of field is 3 (setting FLD1-0 = 11) and as following figure the output waveform when 3 field interlaced driving is performed is shown.

GS = 0			
FLD1-0	11		
Gate \ Field	1	2	3
G1	*		
G2		*	
G3			*
G4	*		
G5		*	
G6			*
G7	*		
G8		*	
G9			*
:	:	:	:
G217			
G218	*		
G219		*	
G220			*

GS = 1			
FLD1-0	11		
Gate \ Field	1	2	3
G220	*		
G219		*	
G218			*
G217	*		
:		*	
G9			*
G8	*		
G7		*	
G6			*
G5	:	:	:
G4			
G3	*		
G2		*	
G1			*

Table 5. 6 Combined with GS and FLD Setting

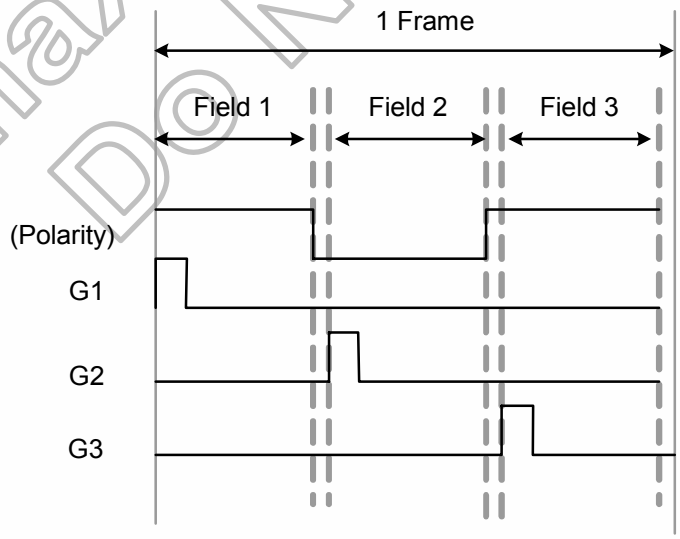


Figure 5. 18 Output Timing for Interlaced Gate Signals (Three-Field is selected)

5.2.6 AC Driving Alternating Timing

LCD must be driven by alternating voltage polarity between liquid crystal layers. The operation of AC drive timing in each type is shown below. The period of AC drive timing is the same as the period of POL signal, which is controlled by the value in register R02h (NW).

In frame-inversion AC drive, LCD-driving signal alternates after one frame finishing display and then a FP or back-porch blanking period are inserted. During the blanking period all gate outputs are remain Vgoff. In interlaced drive, LCD-driving signal alternates after one field finishing display and then a blanking period is inserted. The sum of blanking periods in three fields is equal to the sum of BP and FP blanking period set in a frame. For n-line inversion AC drive, LCD-driving signal alternates before every n-line display starts. Back-porch blanking period is inserted before all display operations starting and front-porch blanking period is inserted after the completion of all display operations.

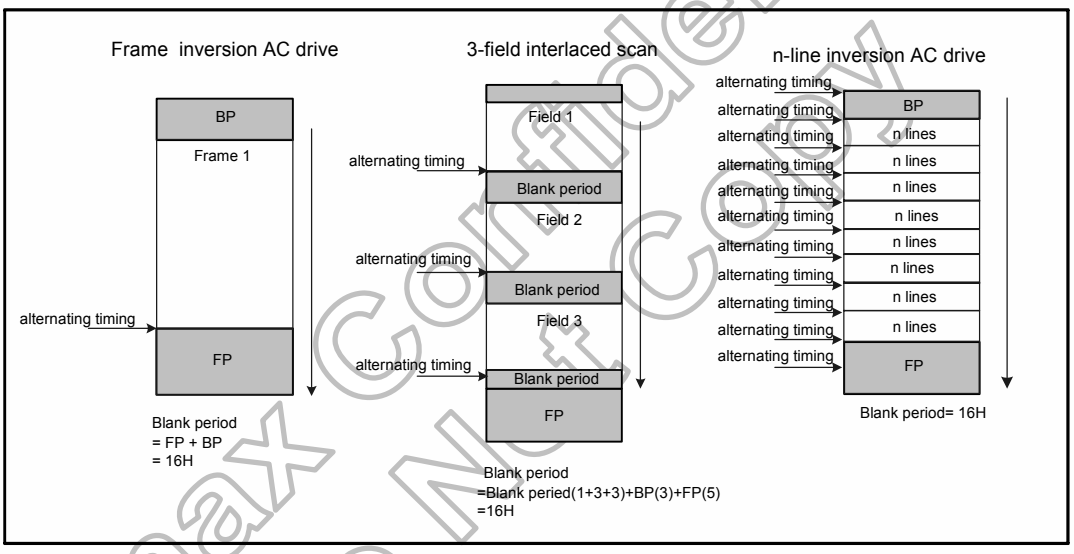


Figure 5. 19 AC Driving Alternating Timing Diagram

5.3 Frame-Frequency Adjustment Function

The HX8340-A supports frequency adjustment function of frame frequency stably that can adjust the frame frequency via the register (DIV, RTN bits) setting in R0Bh during the oscillation frequency.
An animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching (an animated display) is required, the frame frequency can be set higher.

Relationship between LCD Drive Duty and Frame Frequency

The LCD driving duty and the frame frequency is obtained by the following calculation. The frame frequency can be adjusted in the 1-H line period bit (RTN) and in the operation clock division bit (DIV) by write the instruction to the relative register.

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{fosc}{(RTN*6 + 96) * DIV * (NL+BP+FP)} \quad [Hz]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

Example Calculation: to set the maximum frame frequency to 60 Hz

To set frame frequency to 60Hz
Number of drive lines = 220
RTN[3:0]=0000
Operation clock division ration: 1Division
fosc = 60Hz * (0*6+96) clock *1 division * (220+16) lines = 1.36MHz

In this case, the R-C oscillation frequency becomes 1.36MHz. The external resistance value of the R-C oscillator must be adjusted so that the frequency of internal R-C oscillator is equal to 1.36MHz. The display duty can be changed by the partial display with the same frequency setting as above.

5.4 γ-Correction Function

The HX8340-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

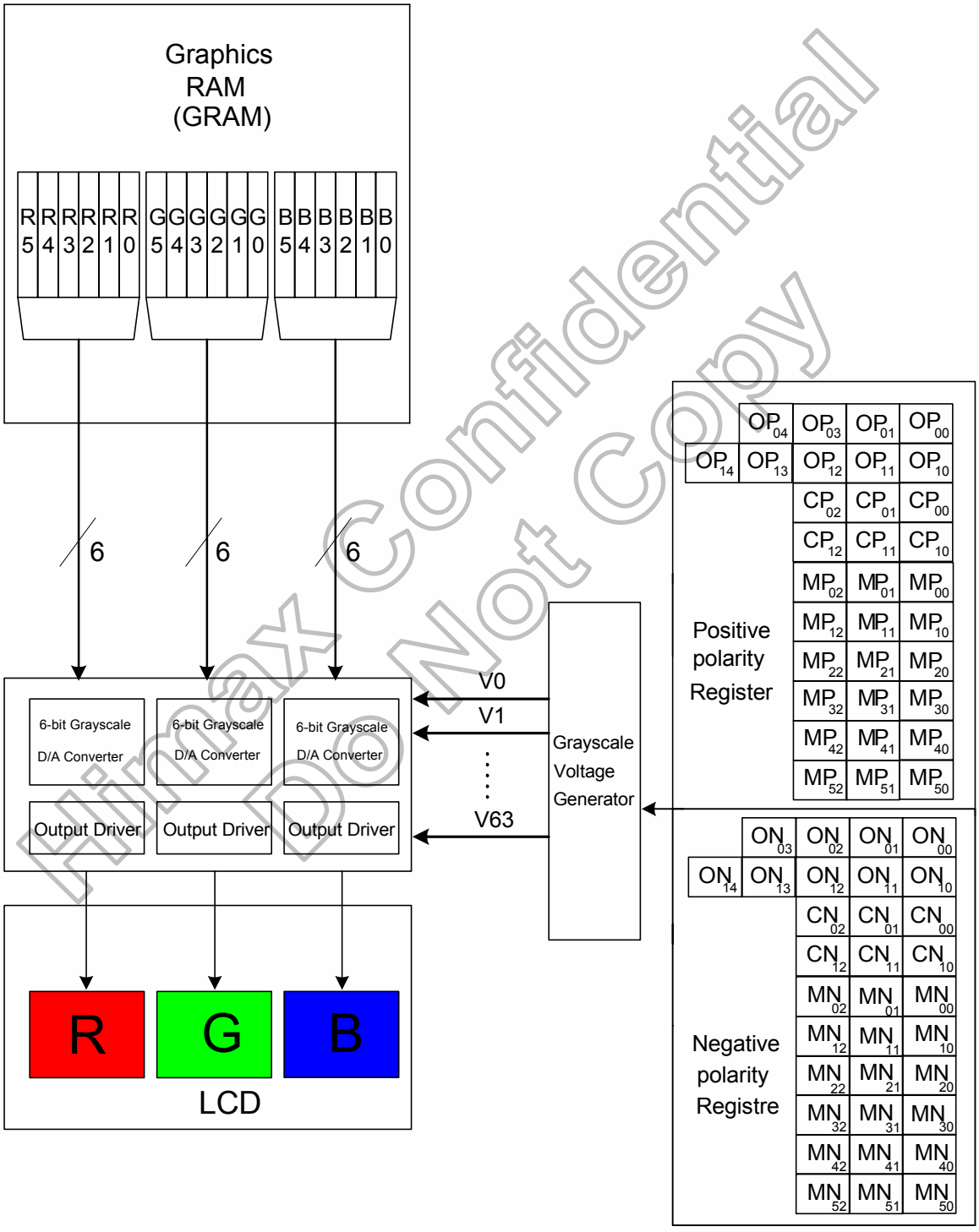


Figure 5. 20 Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62 and 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

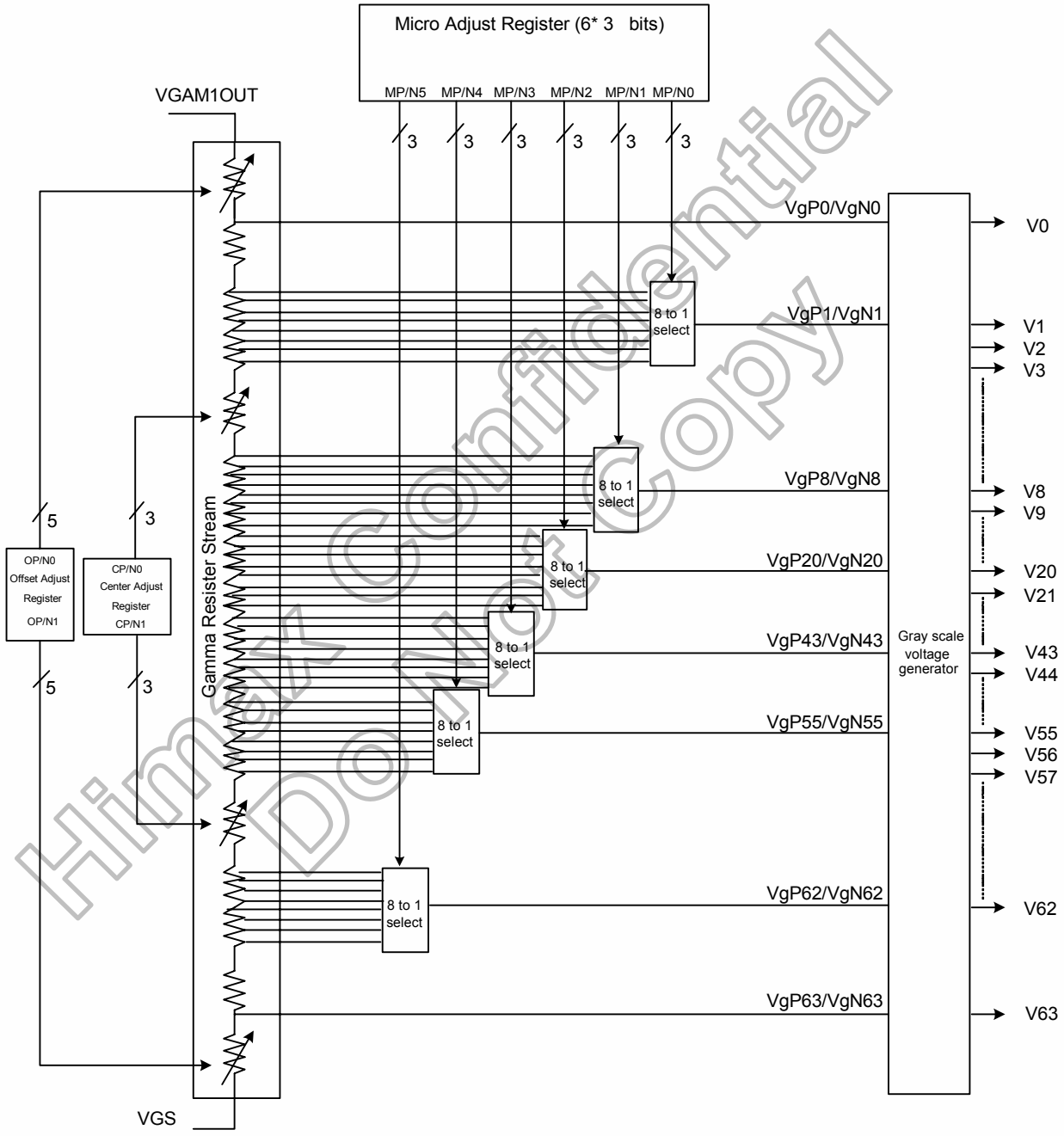


Figure 5. 21 Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This HX8340-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

(1) Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0) for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1) for offset adjustment

Table 5. 7 Gamma-Adjustment Registers

Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (VgP/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

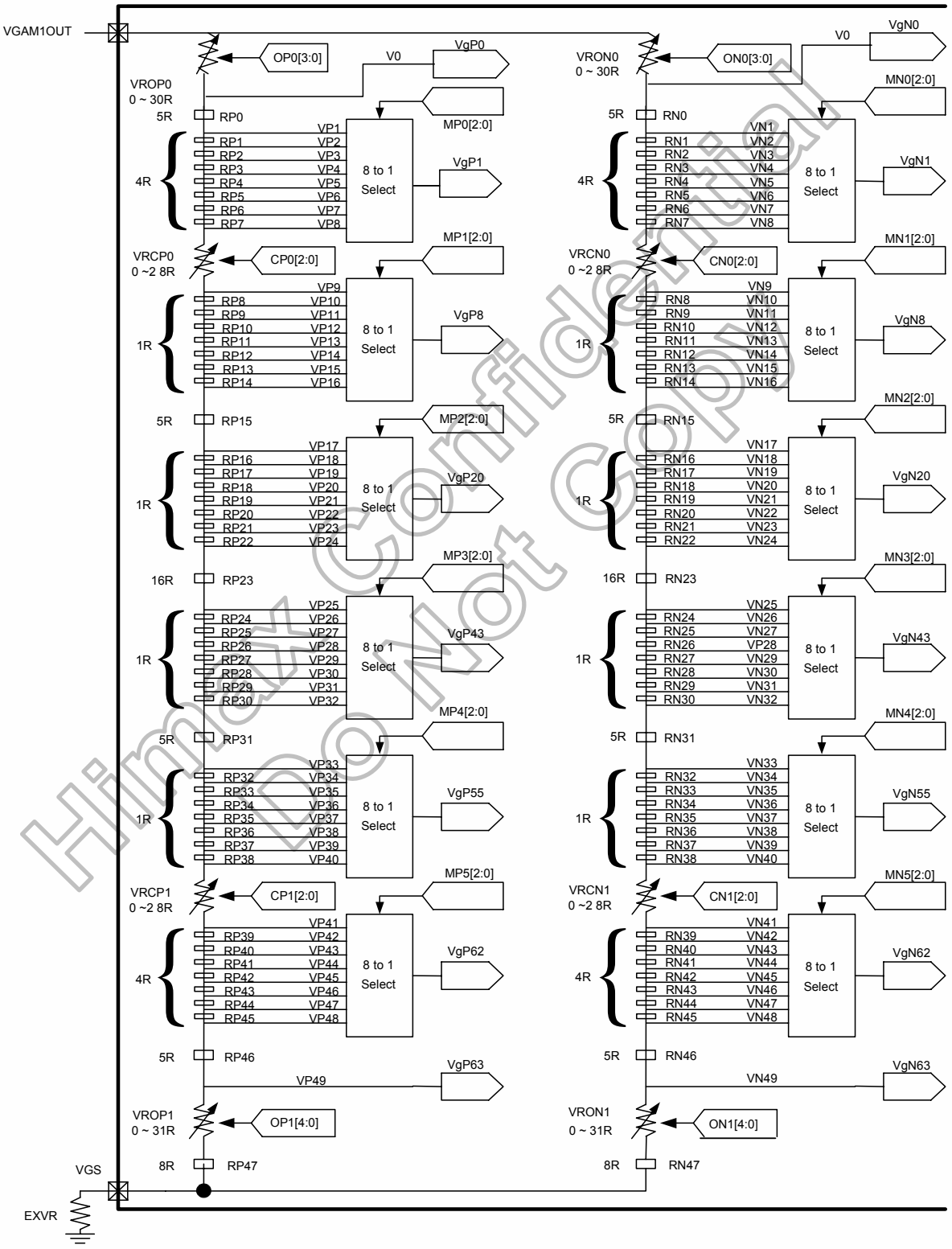


Figure 5. 22 Gamma Resister Stream and Gamma Reference Voltage

Variable resister

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5. 8 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5. 9 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5. 10 Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5. 11 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	-	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	V2P8
	MP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	-	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD=(VGAM1OUT-VGS)
[sumRP× (sumRN/ (sumRP+sumRN))]/ [sumRP×sumRN/ (sumRP+sumRN) +EXVR]

Table 5. 12 Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula
V0	VINP0
V1	VINP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINP2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Table 5. 13 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VGAM1OUT-VD*VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VGAM1OUT-VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VGAM1OUT-VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VGAM1OUT-VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VGAM1OUT-VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VGAM1OUT-VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VGAM1OUT-VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VGAM1OUT-VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VGAM1OUT-VD((VRON0+33R) /sumRN	VN8
VgN8	MN1 2-0=000	VGAM1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
	MN1 2-0=001	VGAM1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VGAM1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VGAM1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VGAM1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VGAM1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VGAM1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VGAM1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	MN2 2-0=000	VGAM1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VGAM1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
	MN2 2-0=010	VGAM1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VGAM1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VGAM1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VGAM1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VGAM1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VGAM1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	MN3 2-0=000	VGAM1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VGAM1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VGAM1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
	MN3 2-0=011	VGAM1OUT-VD((VRON0+71R+VRCN0) /sumRN	VNP8
	MN3 2-0=100	VGAM1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VGAM1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VGAM1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VGAM1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	MN4 2-0=000	VGAM1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VGAM1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VGAM1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VGAM1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
	MN4 2-0=100	VGAM1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VGAM1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VGAM1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VGAM1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	MN5 2-0=000	VGAM1OUT-VD((VRON0+87R+VRCN0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VGAM1OUT-VD((VRON0+91R+VRCN0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VGAM1OUT-VD((VRON0+95R+VRCN0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VGAM1OUT-VD((VRON0+99R+VRCN0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VGAM1OUT-VD((VRON0+103R+VRCN0+VRCN1)/sumRN	VN45
	MN5 2-0=101	VGAM1OUT-VD((VRON0+107R+VRCN0+VRCN1)/sumRN	VN46
	MN5 2-0=110	VGAM1OUT-VD((VRON0+111R+VRCN0+VRCN1)/sumRN	VN47
	MN5 2-0=111	VGAM1OUT-VD((VRON0+115R+VRCN0+VRCN1)/sumRN	VN48
VgN63	-	VGAM1OUT-VD((VRON0+120R+VRCN0+VRCN1)/sumRN	VN49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD = (VGAM1OUT-VGS)
[sumRP(sumRN/(sumRP+sumRN))]/[sumRP(sumRN/(sumRP+sumRN)+EXVR)

Table 5. 14 Voltage Calculation Formula (Negative Polarity)

Grayscale Voltage	Formula
V0	VINN0
V1	VINN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINN2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINN5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINN6
V63	VINN7

Table 5. 15 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Relationship between GRAM Data and Output Level (REV = "0")

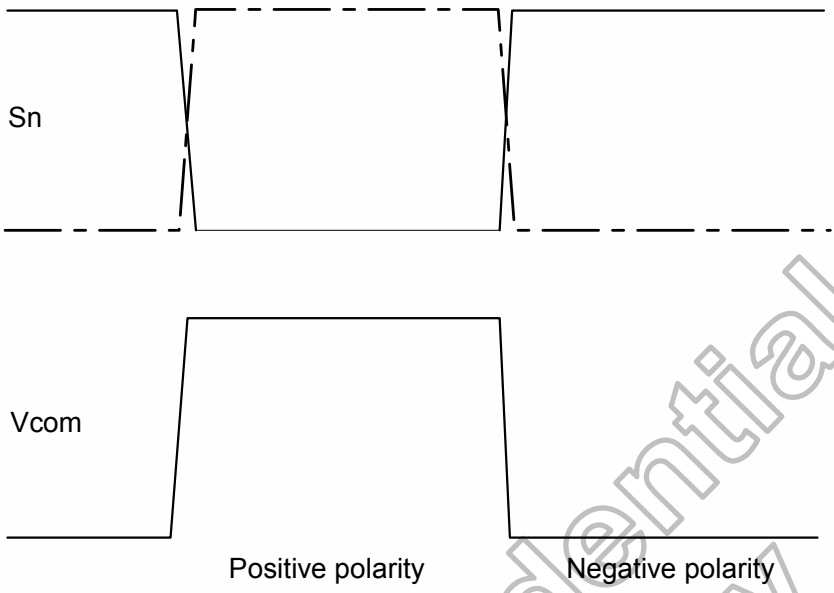
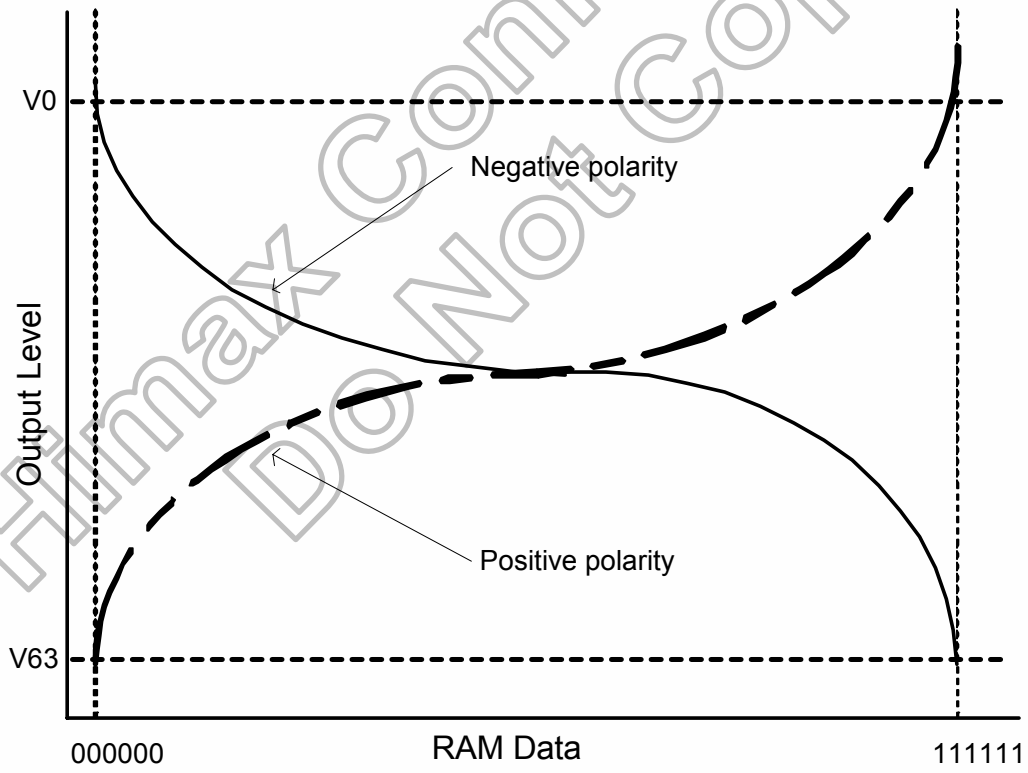


Figure 5. 23 Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 5. 24 Relationship between GRAM Data and Output Level

5.5 Oscillator

The HX8340-A can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor (Rf). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases.

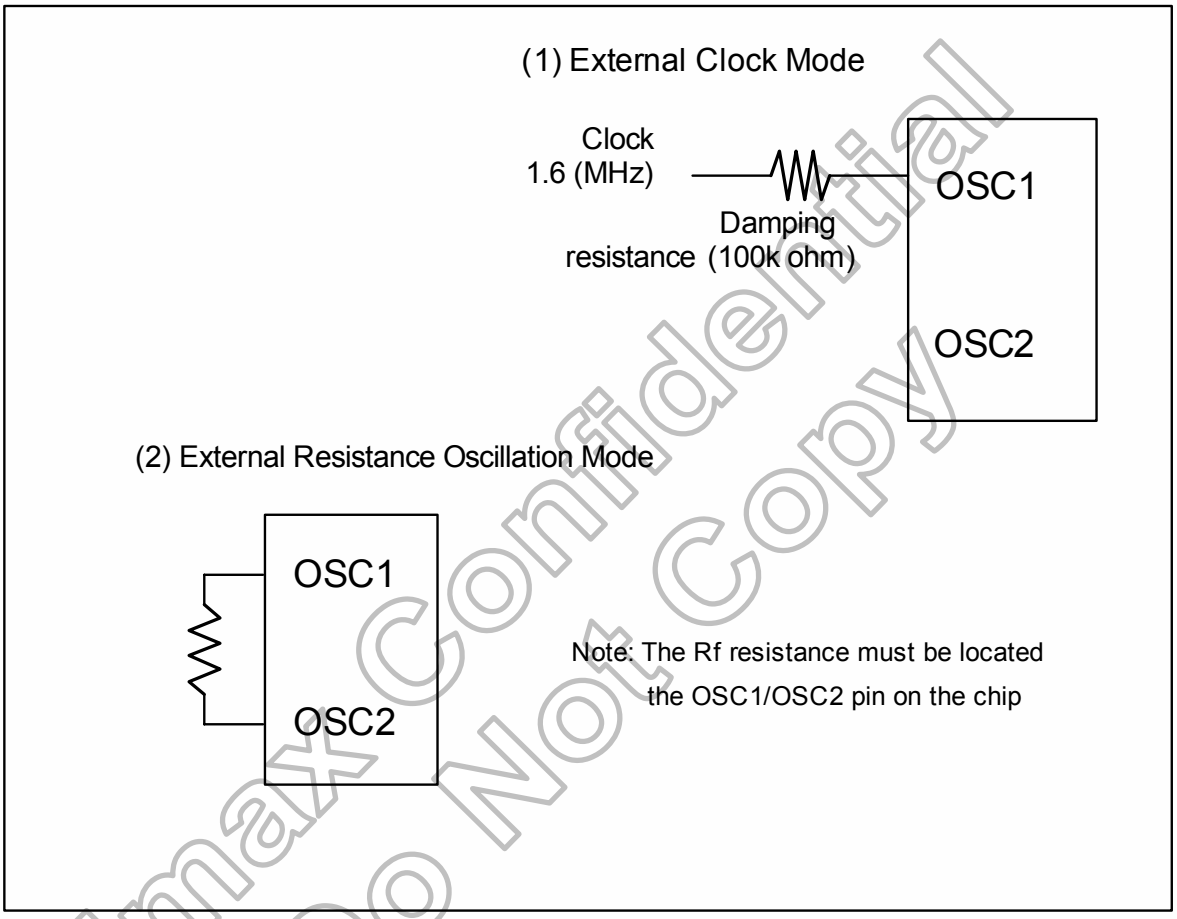


Figure 5. 25 Oscillation Circuit

External Resistance (Rf)	R-C Oscillation Frequency : fosc (KHz)			
	Vcc = 2.4V	Vcc = 2.8V	Vcc = 3.0V	Vcc = 3.3V
30KΩ	1.876MHz	2.352MHz	2.544MHz	2.851MHz
50 KΩ	1.566MHz	1.980MHz	2.155MHz	2.417MHz
70 KΩ	1.355MHz	1.722MHz	1.879MHz	2.106MHz
100 KΩ	1.225MHz	1.554MHz	1.702MHz	1.919MHz
125 KΩ	1.125MHz	1.442MHz	1.580MHz	1.781MHz
150 KΩ	1.052MHz	1.356MHz	1.489MHz	1.692MHz

Table 5. 16 External Resistance Value and R-C Oscillation Frequency (Temporally Define)

6. Introduction

The HX8340-A is a single chip with 18-bit bus architecture. When data read from/ write to internal GRAM through the 18-bit data format. When the internal operation of the HX8340-A wants to start, first send the control information, which is temporarily stored in the registers, described as below to allow high-speed interface with a high-performance MPU. The internal operation of the HX8340-A is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17-0), control the HX8340-A register.

There are nine categories of registers that is following:

- Select the index
- Read back the status
- Control the display functions
- Control power management and save power function
- Process or operate the graphics data
- Set internal GRAM addresses for partial data updating
- Transfer data to and from the internal GRAM with High Speed Function
- Set grayscale level for the internal embedded grayscale gamma adjustment

The following specify the explanation of registers such as register format and bit function.

Register No.	Register	R/W	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
IR	Index	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
R00h	Oscillation Start	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
	Device Code Read	R	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	
R01h	Driver Output Control	W	1	0	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (1)	
R02h	LCD AC driving Control	W	1	0	0	0	0	FLD (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
R03h	Entry Mode	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	0	0	0	0	I/D1 (1)	I/D0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
R04h	Compare Register (1)	W	1	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
R05h	Compare Register (2)	W	1	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	
R07h	Display Control (1)	W	1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
R08h	Display Control (2)	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
R09h	Display Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	
R0Bh	Frame Cycle Adjustment Control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1 (0)	CE0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
R0Ch	External Display Interface Control	W	1	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
R10h	Power Control (1)	W	1	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	AP2 (0)	AP1 (0)	AP0 (0)	0	DK (1)	SLP (0)	STB (0)	
R11h	Power Control (2)	W	1	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)	
R12h	Power Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
R13h	Power Control (4)	W	1	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
R21h	RAM Address Set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
R22h	RAM data Write/Read	W	1	RAM		WD17-0 /RAM			(RD17-0)											
R23h	RAM Write Data Mask (1)	W	1	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R24h	RAM Write Data Mask (2)	W	1	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
R30h	r Control (1)	W	1	0	0	0	0	0	MP 12 (0)	MP 11 (0)	MP 10 (0)	0	0	0	0	0	MP 02 (0)	MP 01 (0)	MP 00 (0)	
R31h	r Control (2)	W	1	0	0	0	0	0	MP 32 (0)	MP P31 (0)	MP 30 (0)	0	0	0	0	0	MP 22 (0)	MP 21 (0)	MP 20 (0)	
R32h	r Control (3)	W	1	0	0	0	0	0	MP52 (0)	MP 51 (0)	MP 50 (0)	0	0	0	0	0	MP 42 (0)	MP 41 (0)	MP 40 (0)	
R33h	r Control (4)	W	1	0	0	0	0	0	CP 12 (0)	CP 11 (0)	CP 10 (0)	0	0	0	0	0	CP 02 (0)	CP 01 (0)	CP00 (0)	
R34h	r Control (5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)	
R35h	r Control (6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)	
R36h	r Control (7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)	
R37h	r Control (8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)	
R38h	r Control (9)	W	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)					OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)	
R39h	r Control (10)	W	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)					ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)	
R40h	Gate Scan Start Position	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
R41h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	
R42h	First Screen Driving Position	W	1	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	
R43h	Second Screen Driving Position	W	1	SE27 (1)	SE26 (1)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (0)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
R44h	Horizontal RAM Address Position	W	1	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
R45h	Vertical RAM Address Position	W	1	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	

Table 6. 1 List Table of Register Set

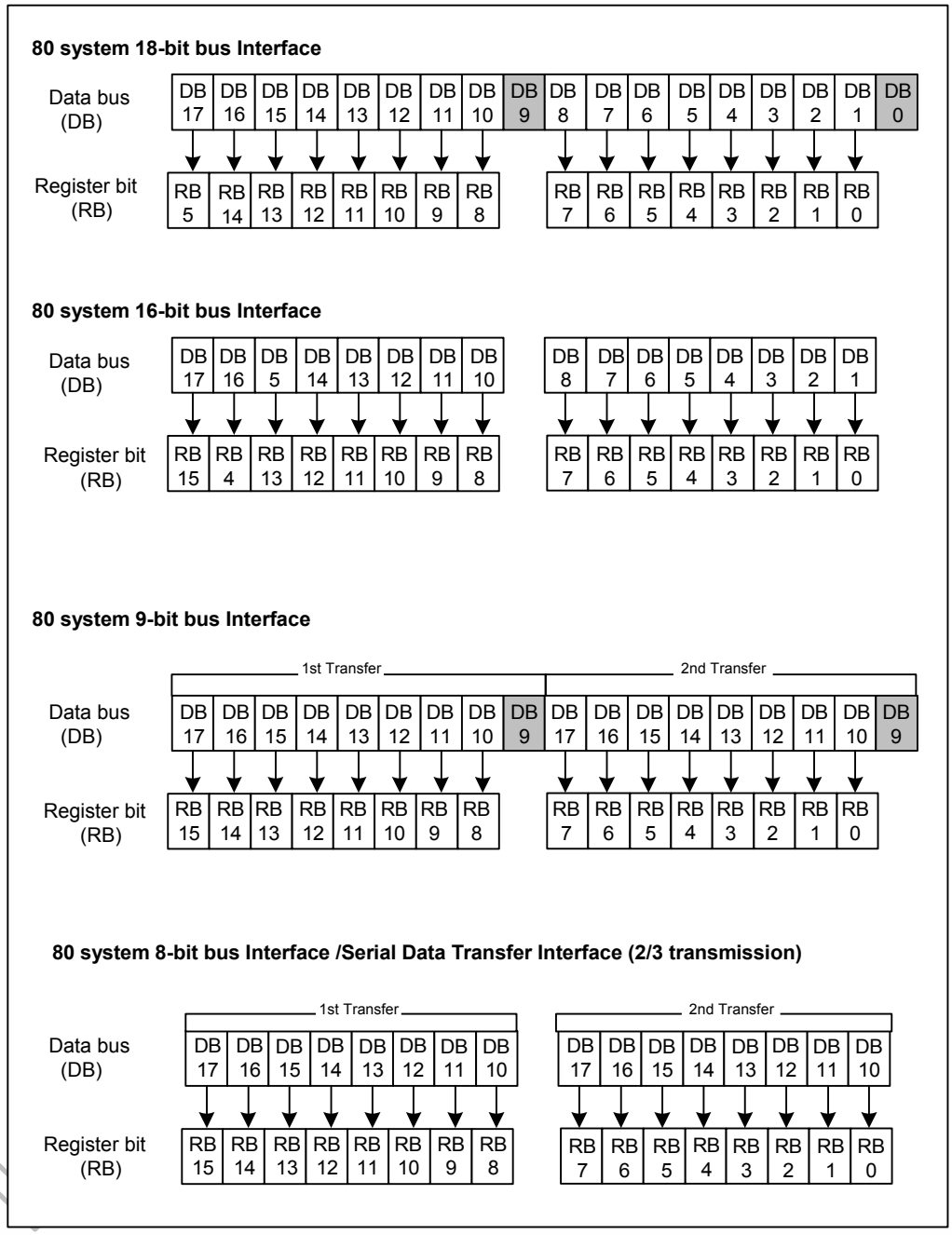


Figure 6. 1 80-System Interface Mode

6.1 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6. 2 Index Register

Index register (IR) specifies Index of the register from R00h to R4Fh. It sets the register number (ID6-0) in the range from 000000b to 1111111b in binary form.

6.2 Status Read Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 6. 3 Status Read Register

Status Read Register for reading the internal status of the HX8340-A.

L7–0: Indicate the position of driving line, where the liquid crystal display is driven at present.

6.3 Start Oscillation Register (R00h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0

Figure 6. 4 Start Oscillation Register (R00h)

Start Oscillation Register restarts the oscillator from the suspend state at the standby mode. After setting this register, and wait at least 10 ms for oscillation stabilizing before setting the next register.

When the read commend is issued, 8340h is read.

6.4 Driver Output Control Register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 6. 5 Driver Output Control Register (R01h)

NL4–0: Specify the number of scan lines for the LCD driver can be adjusted by every 8 lines. Select the setting value for the panel size or higher.

NL4	NL3	NL2	NL1	NL0	Gate Driver Used	Number of Scan Line	Display Size
0	0	0	0	0	Ignore	Ignore	Ignore
0	0	0	0	1	G1~G16	16	528*16 dots
0	0	0	1	0	G1~G24	24	528*24dots
0	0	0	1	1	G1~G32	32	528*32 dots
0	0	1	0	0	G1~G40	40	528*40 dots
0	0	1	0	1	G1~G48	48	528*48dots
0	0	1	1	0	G1~G56	56	528*56 dots
0	0	1	1	1	G1~G64	64	528*64 dots
0	1	0	0	1	G1~G72	72	528*72 dots
:	:	:	:	:	:	:	:
1	1	0	0	0	G1~G200	200	528*200 dots
1	1	0	0	1	G1~G208	208	528*208 dots
1	1	0	1	0	G1~G216	216	528*216 dots
1	1	0	1	1	G1~G220	220	528*220 dots
1	1	1	0	0	G1~G220	220	528*220 dots
1	1	1	0	1	G1~G220	220	528*220 dots
1	1	1	1	0	G1~G220	220	528*220 dots
1	1	1	1	1	G1~G220	220	528*220 dots

Table 6. 2 NL bits and Scan Line

SS: The source driver output shift direction selected. The shift direction from S1 to S528 when SS = 0. And shift direction from S528 to S1 when SS = 1. And if the BGR = 0, <R><G><B> color is assigned from S1. When SS = 1 and BGR = 1, <R><G><B> color is assigned from S528. Re-write to the GRAM after changed the SS bit or BGR bit.

GS: Specify the shift direction of gate driver output. When GS = 0, the shift direction from G1 to G220. When GS = 1, the shift direction from G220 to G1.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to PD17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to PD17-0

Table 6. 3 EPL Bit and Enable Pin

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

6.5 LCD Driving Waveform Register (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 6. 6 LCD-Driving-Waveform Control Register (R02h)

NW5–0: Specify the number of n lines that will alternate POL signal when B/C = 1. The inversion is occurred every n + 1 line, and the 1st to the 64th lines can be selected.

EOR: EOR=1 will force POL signal alternate at the beginning of a frame in n-line inversion driving mode (B/C=1), no matter the last interval of POL signal is over or not in last frame. Therefore, EOR bit is used when the POL signal is not completely alternated in some number of drive lines in LCD display area. For details, see the “N-line Inversion LCD Drive” section.

B/C: When B/C = 0, POL signal alternates in every frame for LCD drive. When B/C = 1, POL signal alternates in each n line specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “N-line Inversion LCD Drive” section.

FLD1-0: Set the number of n field for interlaced driving mode. For details, see the “Interlaced driving function section”.

FLD1	FLD0	Number of field
0	0	Ignore
0	1	1 field
1	0	Ignore
1	1	3 fields

Table 6. 4 FLD Bits and Interlaced Field

6.6 Entry Mode Register (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM1	DFM0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0

Figure 6. 7 Entry Mode Register (R03h)

LG2–0: The compare operation. The data is read from the GRAM by the MPU and is compared with the compare registers (CP17–0) by a compare operation, then write the results to GRAM. For details, see the “Graphics Operation Function section”.

AM: The updating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D [1..0].

I/D[1..0]: The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the update method with I/D1-0 & AM bit.

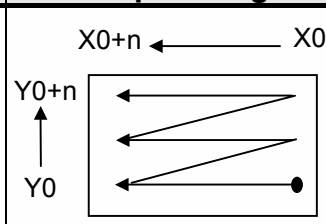
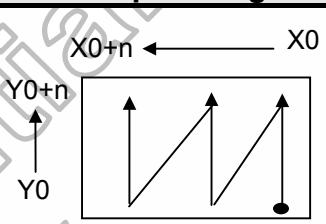
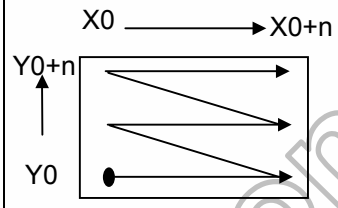
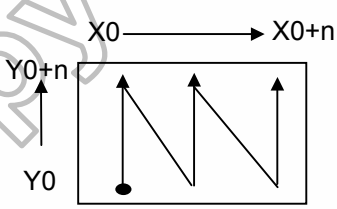
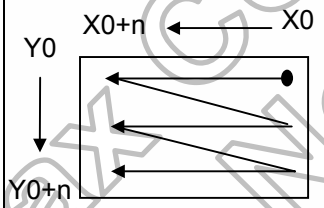
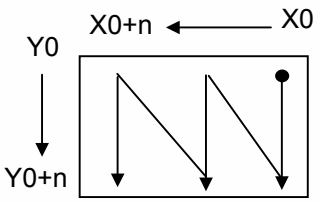
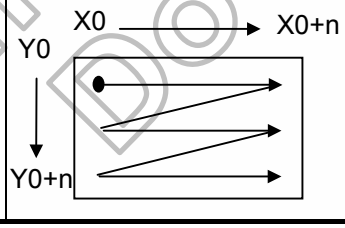
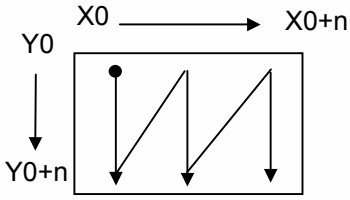
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure 6. 8 Address Direction Settings

BGR: The order of <R><G><B> dot color. When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order. Setting BGR will change the bit order of (CP17-0) and (WM17-0) in the same way.

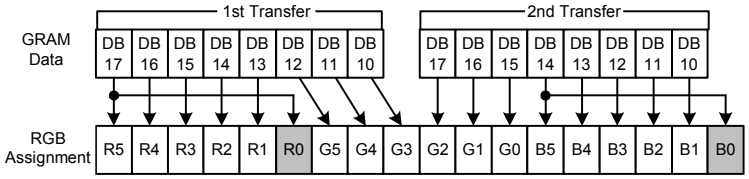
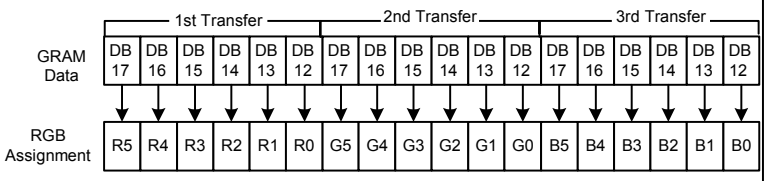
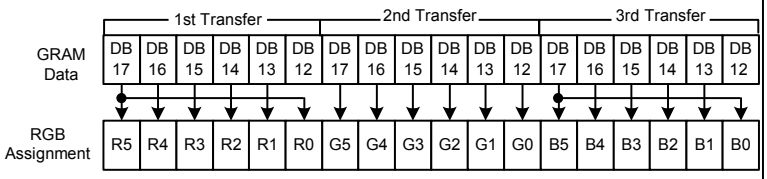
TRI: When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus interface. When TRI=0, 8-bit bus interface mode is unselected.

DFM1-0: Specify the data format when TRI=1, for 8-bit bus interface or serial data transfer interface. DFM1-0=10, 262K color mode. DFM1-0=11, 65K color mode.

DFM1	DFM0	TRI	16-bit interface RAM write data transfer
0	0	0	80-system 16-bit interface (1 transfer/pixel) 65536 colors Available 1st Transfer: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 2nd Transfer: DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 GRAM Data RGB Assignment: R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	80-system 16-bit interface MSB mode (2 transfers/pixel) 262,144 colors Available 1st Transfer: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 2nd Transfer: DB17 DB16 GRAM Data RGB Assignment: R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0
1	1	1	80-system 16-bit interface LSB mode (2 transfers/pixel) 65,536 colors Available 1st Transfer: DB2 DB1 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 2nd Transfer GRAM Data RGB Assignment: R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0

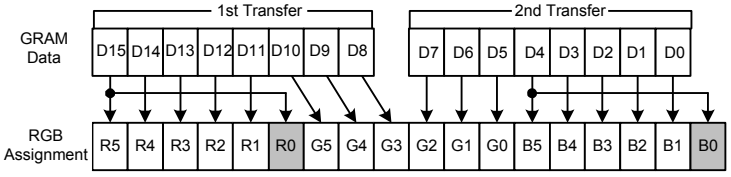
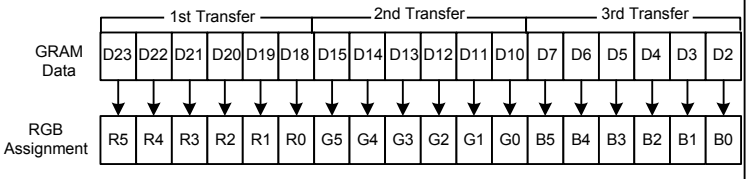
Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

Figure 6. 9 The Setting of DFM and TRI (80-system 16-bit Interface)

DFM1	DFM0	TRI	8-bit interface RAM write data transfer
0	0	0	80-system 8-bit interface (2 transfers/pixel) 65,536 colors Available 
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	80-system 8-bit interface (3 transfers/pixel) 262,144 colors Available 
1	1	1	80-system 8-bit interface (3 transfers/pixel) 65,536 colors Available 

Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

Figure 6. 10 The Setting of DFM and TRI (80-system 8-bit Interface)

DFM1	DFM0	TRI	Serial Data Transfer Interface RAM write data transfer
0	0	0	Serial Data Transfer (2 transfers/pixel) 65536 colors Available 
0	1	0	Ignore
1	*	0	Ignore
0	*	1	Ignore
1	0	1	Serial Data Transfer (3 transfers/pixel) 262,144 colors Available 
1	1	1	Ignore

Note: Instructions are transferred in 8-bit x 2 transfer mode irrespective of TRI, DFM1-0 bits.

Figure 6. 11 The Setting of DFM and TRI (Serial Data Transfer Interface)

6.7 Compare Register Set

The written date is sent from the microprocessor and modified in the HX8340-A, then written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the MPU software processing. For details, see the Graphics Operation Function section.

6.7.1 Compare Register 1 (R04h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0

Figure 6. 12 Compare Register 1 (R04h)

6.7.2 Compare Register 2 (R05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

Figure 6. 13 Compare Register 2 (R05h)

CP17–0: The values of compare register for the compare operation with the data read from the GRAM or written from the MPU.

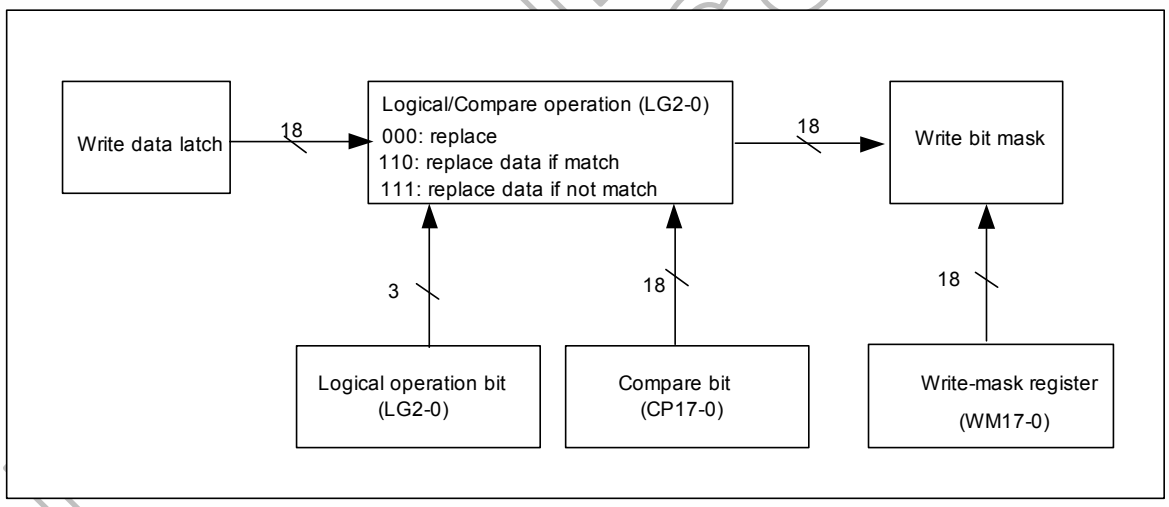


Figure 6. 14 Bit Operation

6.8 Display Control Register Set

6.8.1 Display Control Register 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	PT2	PT1	PT0	VLE2	VLE1	SPT	0	1	GON	DTE	CL	REV	D1	D0

Figure 6. 15 Display Control Register 1 (R07h)

D1–0: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8340-A can control the charging current for the LCD with AC driving.
Control the display on/off while control GON and DTE. When D1–0 = 01, the internal display of the HX8340-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	Source Output	HX8340-A Internal Display Operations	Gate-Driver Control Signals (CPV, FLM, M) (CPV, STV, POL)
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

Note: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

Table 6. 5 D Bits and Operation

REV: REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

REV	GRAM data	Source output level							
		Display area		Non-display area					
				PT1-0=(0,0)		PT1-0=(1,0)		PT1-0=(1,1)	
		Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity	Positive Polarity	Negative Polarity
0	18'h00000 . . 18'h3FFFF	V63 . . V0	V0 . . V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 . . 18'h3FFFF	V0 . . V63	V63 . . V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z

Table 6. 6 Display Control Instruction

CL: CL = 1, the display mode is set to the 8-color display mode. For details, see the section on the 8-color display mode section.

CL	Number of Display Colors
0	262,144
1	8

Note: The display 262,144 colors when 18/9 bit bus interface is using, and display 65,536 colors when 16/8 bit bus interface is using.

Table 6. 7 CL Bit for 8-Color Display

DTE, GON: Specify the output level of gate line. Vcom level is VSSD when GON = 0.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Note: GON bit is used in the gate driver. Control according to the bits' values is executed by the gate driver. For details, see the data sheet of the gate driver.

Table 6. 8 GON and DTE Bits

SPT: When SPT = 1, the 2-division LCD drive is performed so a LCD can be divided 2 split display windows. For details, see the Partial Screen Display Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st display window. When VLE2 = 1, a vertical scroll is performed in the 2nd display window. Vertical scrolling on the two windows cannot be controlled at the same time.

VLE2	VLE1	1st Display Window	2nd Display Window
0	0	Fixed display	Fixed display
0	1	Scrolled display	Fixed display
1	0	Fixed display	Scrolled display
1	1	Ignore	Ignore

Table 6. 9 VLE Bits

PT1-0: When partial display is in use, these bits determine the source output in the non-display area. For details, see the Partial Screen Display Function section. The output on the source lines during the periods of the front and BP are also determined by PT1-0.

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	Vcom output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VcomH↔VcomL
0	1	Ignore	Ignore	Reference to PTG1-0	VcomH↔VcomL
1	0	VSSD	VSSD	Reference to PTG1-0	VcomH↔VcomL
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

Table 6. 10 PT Bits for Source and Gate Output in Non-Display Area of Partial Display

6.8.2 Display Control Register 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

Figure 6. 16 Display Control Register 2 (R08h)

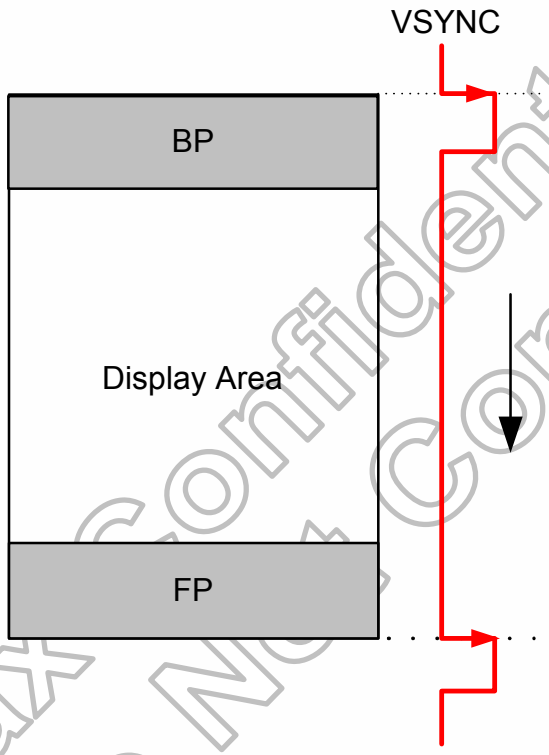
BP3-0: Specify the amount of scan line for back porch (BP).
FP3-0: Specify the amount of scan line for front porch (FP).

The setting vale, ensure that:
BP + FP ≦ 16 lines
PB ≧ 2 lines
FP ≧ 2 lines

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by he display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	Number of FP Line	Number of BP Line
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	3 lines	
:	:	:	:	:	
1	1	0	1	13 lines	
1	1	1	0	14 lines	
1	1	1	1	Ignore	

Table 6. 11 BP/FP Bits Setting



Note: The output signal is delay 2 lines timing from the VSYNC to the LCD

Figure 6. 17 BP/FP

Operation Mode	Number of Interlace Scan Field	BP	FP	BP + FP
System Interface	FLD1-0 = 01	≥2 lines	≥2 lines	≤ 16 lines
	FLD1-0 = 11	3 lines	5 lines	-
RGB Interface	-	≥2 lines	≥2 lines	≤ 16 lines
VSYNC Interface	-	≥2 lines	≥2 lines	16 lines

Table 6. 12 BP3-0, FP3-0 Setting Dependent on Operation Mode

6.8.3 Display Control Register 3 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

Figure 6. 18 Display Control Register 3 (R09h)

PTG1-0: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

Table 6. 13 PTG Bits Setting

ISC3-0: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 70Hz
0	0	0	0	0 frame	
0	0	0	1	3 frames	43 ms
0	0	1	0	5 frames	71 ms
0	0	1	1	7 frames	100 ms
0	1	0	0	9 frames	129 ms
0	1	0	1	11 frames	157 ms
0	1	1	0	13 frames	186 ms
0	1	1	1	15 frames	214 ms
1	0	0	0	17 frames	243 ms
1	0	0	1	19 frames	271 ms
1	0	1	0	21 frames	300 ms
1	0	1	1	23 frames	329 ms
1	1	0	0	25 frames	357 ms
1	1	0	1	27 frames	386 ms
1	1	1	0	29 frames	414 ms
1	1	1	1	31 frames	443 ms

Table 6. 14 ISC Bit2 Setting

6.9 Frame Cycle Control Register (R0Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GD1	GD0	SDT1	SDT0	CE1	CE0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 6. 19 Frame Cycle Control Register (R0Bh)

RTN3-0: Set the 1-line period in a clock unit.

Clock cycles=1/internal operation clock frequency

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Line
0	0	0	0	96
0	0	0	1	102
0	0	1	0	108
:	:	:	:	:
1	0	0	0	144
1	0	0	1	150
:	:	:	:	:
1	1	1	1	186

Table 6. 15 RTN Bits and Clock Cycles

DIV1-0: The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 6Hz period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Table 6. 16 DIV Bits and Clock Frequency

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{(\text{RTN}*6 + 96) * \text{DIV} * (\text{NL}+\text{BP}+\text{FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP≦16

CE1-0: CE period can be set with CE1-0.

CE1	CE 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock cycle	8 clock cycles
1	0	2 clock cycles	16 clock cycles
1	1	3 clock cycles	24 clock cycles

Table 6. 17 CE Bits for Equalized Period

SDT1-0: Set delay amount from falling edge of the gate output signal for the source outputs.

SDT1	SDT0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	1 clock cycle	8 clock cycles
0	1	2 clock cycles	16 clock cycles
1	0	3 clock cycles	24 clock cycles
1	1	4 clock cycles	32 clock cycles

Table 6. 18 SDT Bits for Source Output Delay

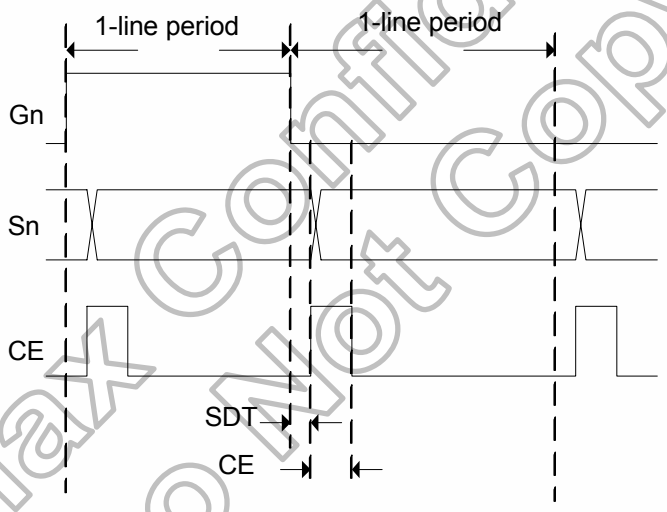


Figure 6. 20 Equalized Period and Source Output Delay

GD1-0: Set amount of non-overlap for the gate output.

GD1	GD0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (source clock: DOTCLK)
0	0	0 clock cycle	0 clock cycle
0	1	4 clock cycle s	32 clock cycle s
1	0	6 clock cycle s	48 clock cycle s
1	1	8 clock cycle s	64 clock cycle s

Table 6. 19 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulses

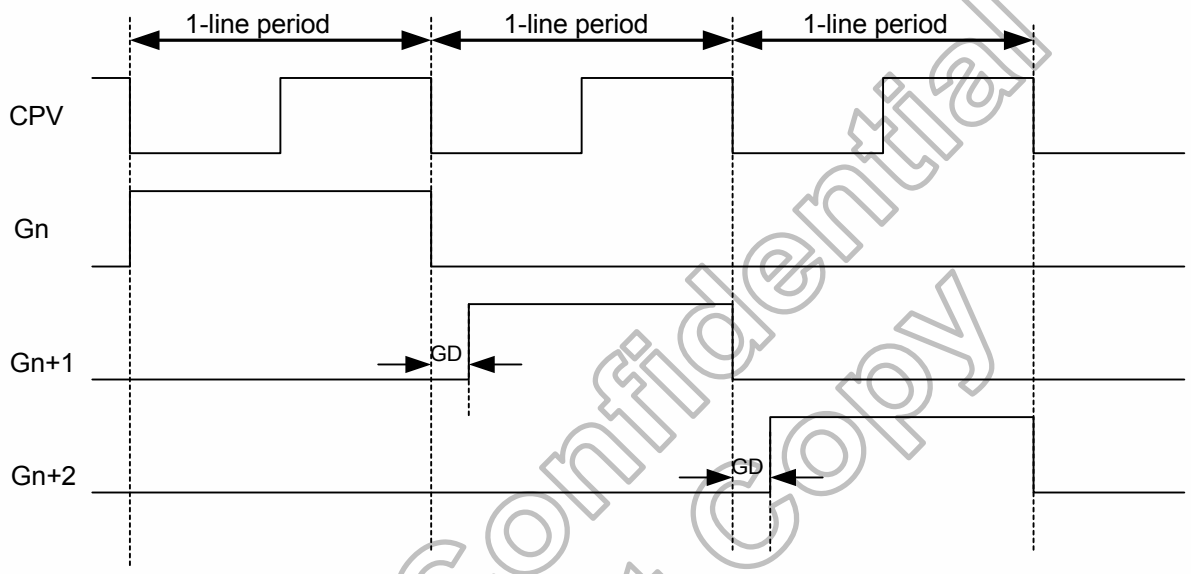


Figure 6. 21 Non-overlap Time between Two Adjacent Gate Output Pulses

Interface mode	Clock Source
System interface mode	R-C oscillator
RGB interface more	DOTCLK
VSYNC interface mode	R-C oscillator

Table 6. 20 Clock Source for Interface Mode

6.10 External Display Interface Control Register (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

Figure 6. 22 External Display Interface Control Register (R0Ch)

RIM1-0: Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode (1 transfer/pixel)
0	1	16-bit bus RGB interface Mode (1 transfer/pixel)
1	0	6-bit bus RGB interface Mode (3 transfers/pixel)
1	1	Ignore

Table 6. 21 RIM Bits for Transfer Mode of RGB interface

DM1-0: Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 6. 22 DM Bits for Operation Mode of LCD display

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	• System interface • VSYNC interface
1	RGB interface

Note: (1) The register is set only through the system interface.
(2) A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

Table 6. 23 RM Bit for Access Interface of GRAM

6.11 Power Control Register Set

6.11.1 Power Control Register 1 (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	SAP2	SAP1	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB

Figure 6. 23 Power Control Register 1 (R10h)

STB: When STB="1", the HX8340-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. Anyway, have not any external clock are supplied. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = “0”)
b. Start the oscillation

Within the standby mode, the GRAM data and register content may be lost. For preventing this, they have to set again after the standby mode is exited.

SLP: When SLP = 1, the HX8340-A into the sleep mode, where the internal display operations are suspend except for the R-C oscillator, thus the current consumption can be reduced. Within the sleep mode, the GRAM data and register content cannot be accessed although they are retained.

DK: ON/OFF the operation of step-up circuit 1. When power on, the VLCDC no output until VGHC is set up completely. For detail, see the power supply setting sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

Table 6. 24 DK Bit for Operation of Step-up Circuit 1

AP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP2–0 = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	Ignore
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

Table 6. 25 AP Bits and Amount of Current in Operational Amplifier

BT2–0: Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x Vci1	-1 x Vci1	6 x Vci1	-5 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B, C22 A/B
0	0	1	2 x Vci1	-1 x Vci1	6 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	0	2 x Vci1	-1 x Vci1	6 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	1	2 x Vci1	-1 x Vci1	5 x Vci1	-5 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	0	2 x Vci1	-1 x Vci1	5 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	1	2 x Vci1	-1 x Vci1	5 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	0	2 x Vci1	-1 x Vci1	4 x Vci1	-4 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	2 x Vci1	-1 x Vci1	4 x Vci1	-3 x Vci1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B

Note: The factors of step-up for VGH are derived from Vci1 when VLCD and Vci2 are shorted. The conditions of VLCD ≦ 5.5V, VCL ≦ -3.3V, VGH ≦ 16.5V, and VGL ≦-16.5V must be satisfied.

Table 6. 26 BT Bits and VLCD and VGH Outputs

SAP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP2–0 = 000, the current consumption can be reduced by stopping the operational amplifier.

SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.67
0	1	0	0.71
0	1	1	0.71
1	0	0	1
1	0	1	1
1	1	0	1.43
1	1	1	1.43

Table 6. 27 SAP Bits and Amount of Current in Operational Amplifier

6.11.2 Power Control Register 2 (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

Figure 6. 24 Power Control Register 2 (R11h)

VC2-0: Set the reference voltage of VGAM1OUT and Vci1 by adjusting the rate of Vci.

VC2	VC1	VC0	Internal reference voltage (REGP) of VGM1OUT and Vci1
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	Ignore
1	1	1	Ignore

Table 6. 28 VC Settings and Internal Reference Voltage

DC02–00: Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1
0	0	0	fosc / 8
0	0	1	fosc / 16
0	1	0	fosc / 32
0	1	1	fosc / 64
1	0	0	fosc / 128
1	0	1	Ignore
1	1	0	Ignore
1	1	1	Ignore

Table 6. 29 Operation Frequency of Step-up Circuit 1

DC12–10: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2
0	0	0	fosc / 16
0	0	1	fosc / 32
0	1	0	fosc / 64
0	1	1	fosc / 128
1	0	0	fosc / 256
1	0	1	Ignore
1	1	0	Ignore
1	1	1	Ignore

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

Table 6. 30 Operation Frequency of Step-up Circuit 2

6.11.3 Power Control Register 3 (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

Figure 6. 25 Power Control Register 3 (R12h)

VRH3-0: Set the magnification of amplification for VGAM1OUT voltage. (VCOM, reference voltage for grayscale voltage) It allows magnify the amplification of REGP from 1.33 to 1.9 times.

VRH3	VRH2	VRH1	VRH0	VGAM1OUT
0	0	0	0	REGP x 1.33
0	0	0	1	REGP x 1.45
0	0	1	0	REGP x 1.55
0	0	1	1	REGP x 1.65
0	1	0	0	REGP x 1.75
0	1	0	1	REGP x 1.80
0	1	1	0	REGP x 1.85
0	1	1	1	Stop
1	0	0	0	REGP x 1.90
1	0	0	1	Ignore
1	0	1	0	Ignore
1	0	1	1	Ignore
1	1	0	0	Ignore
1	1	0	1	Ignore
1	1	1	0	Ignore
1	1	1	1	Ignore

Table 6. 31 VRH Bits and VGAM1OUT Voltage

PON: ON/OFF the operation of step-up circuit 3. PON = 0 is to stop and PON = 1 to start operation.

6.11.4 Power Control Register 4 (R13h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 6. 26 Power Control Register 4 (R13h)

VCM4-0: Set the VcomH voltage (voltage of higher side when Vcom is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VGAM1OUT voltage. When VCM4-0 = “11111”, stop the internal volume adjustment and adjust the VcomH with external resistance from VcomR.

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	VGAM1OUT x 0.40
0	0	0	0	1	VGAM1OUT x 0.42
0	0	0	1	0	VGAM1OUT x 0.44
:	:	:	:	:	:
0	1	1	1	0	VGAM1OUT x 0.68
0	1	1	1	1	Stop the internal volume. VcomH can be adjusted from VcomR with a external VR (variable resister),
1	0	0	0	0	VGAM1OUT x 0.70
1	0	0	0	1	VGAM1OUT x 0.72
1	0	0	1	0	VGAM1OUT x 0.74
:	:	:	:	:	:
1	1	1	0	0	VGAM1OUT x 0.94
1	1	1	0	1	VGAM1OUT x 0.96
1	1	1	1	0	VGAM1OUT x 0.98
1	1	1	1	1	Stop the internal volume. VcomH can be adjusted from VcomR with a external VR (variable resister),

Note: Adjust VGAM1OUT and VCM4-0 so that the VcomH voltage is lower than VGAM1OUT.

Table 6. 32 VCM4-0 Bits and VcomH Voltage

VDV4-0: Sets the amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. It is possible to setup from 0.6 to 1.23 times of VGAM1OUT. When VCOMG = 0, the setup is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VGAM1OUT x 0.60
0	0	0	0	1	VGAM1OUT x 0.63
0	0	0	1	0	VGAM1OUT x 0.66
:	:	:	:	:	:
0	1	1	0	0	VGAM1OUT x 0.96
0	1	1	0	1	VGAM1OUT x 0.99
0	1	1	1	0	VGAM1OUT x 1.02
0	1	1	1	1	Inhibition
1	0	0	0	0	VGAM1OUT x 1.05
1	0	0	0	1	VGAM1OUT x 1.08
1	0	0	1	0	VGAM1OUT x 1.11
1	0	0	1	1	VGAM1OUT x 1.14
1	0	1	0	0	VGAM1OUT x 1.17
1	0	1	0	1	VGAM1OUT x 1.20
1	0	1	1	0	VGAM1OUT x 1.23
1	0	1	1	1	Inhibition
1	1	-	-	-	

Note: Adjust VGAM1OUT and VDV4-0 so that the Vcom and Vgoff amplitudes are lower than 6.0V.

Table 6. 33 VDV4-0 Bits and Vcom Amplitude

VCOMG: When VCOMG = 1, VcomL voltage can output to negative voltage (1.0V ~ -Vci +0.5V). When VCOMG = 0, VcomL voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, when VCOMG = 0, setting of the VDV4-0 is invalid. In this case, adjustment of Vcom/Vgoff A/C amplitude must be adjusted with VcomH using VCM4-0.

6.12 RAM Address Register (R21h)

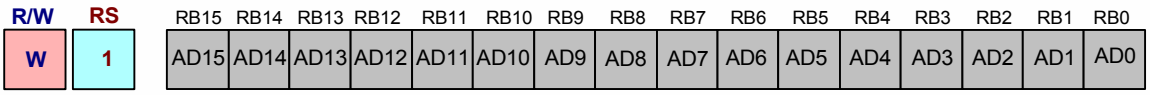


Figure 6. 27 RAM Address Register (R21h)

AD15–0: Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

AD15-AD0	GRAM Setting
“0000” h – “00AF” h	Bitmap data for G1
“0100” h – “01AF” h	Bitmap data for G2
“0200” h – “02AF” h	Bitmap data for G3
:	:
“D900” h – “D9AF” h	Bitmap data for G218
“DA00” h – “DAAF” h	Bitmap data for G219
“DB00” h – “DBAF” h	Bitmap data for G220

Table 6. 34 GRAM Address Mapping

6.13 Write Data Register (R22h)

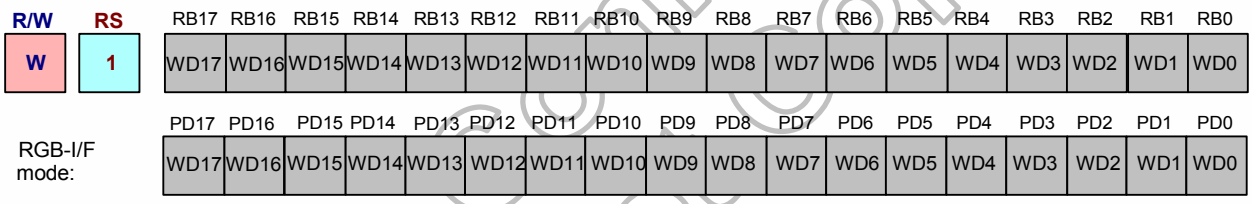


Figure 6. 28 Write Data Register (R22h)

WD17– 0: Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

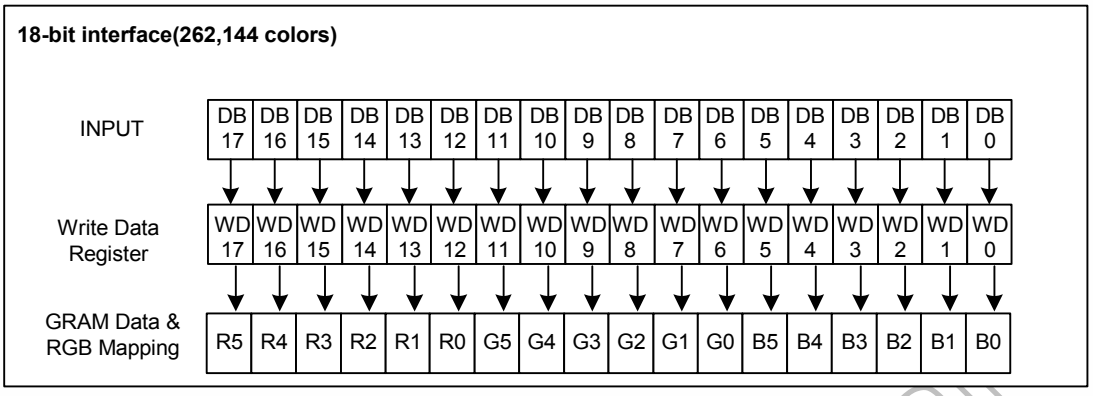


Figure 6. 29 Input Data Written to GRAM through Write Data Register in 18-bit Interface Mode

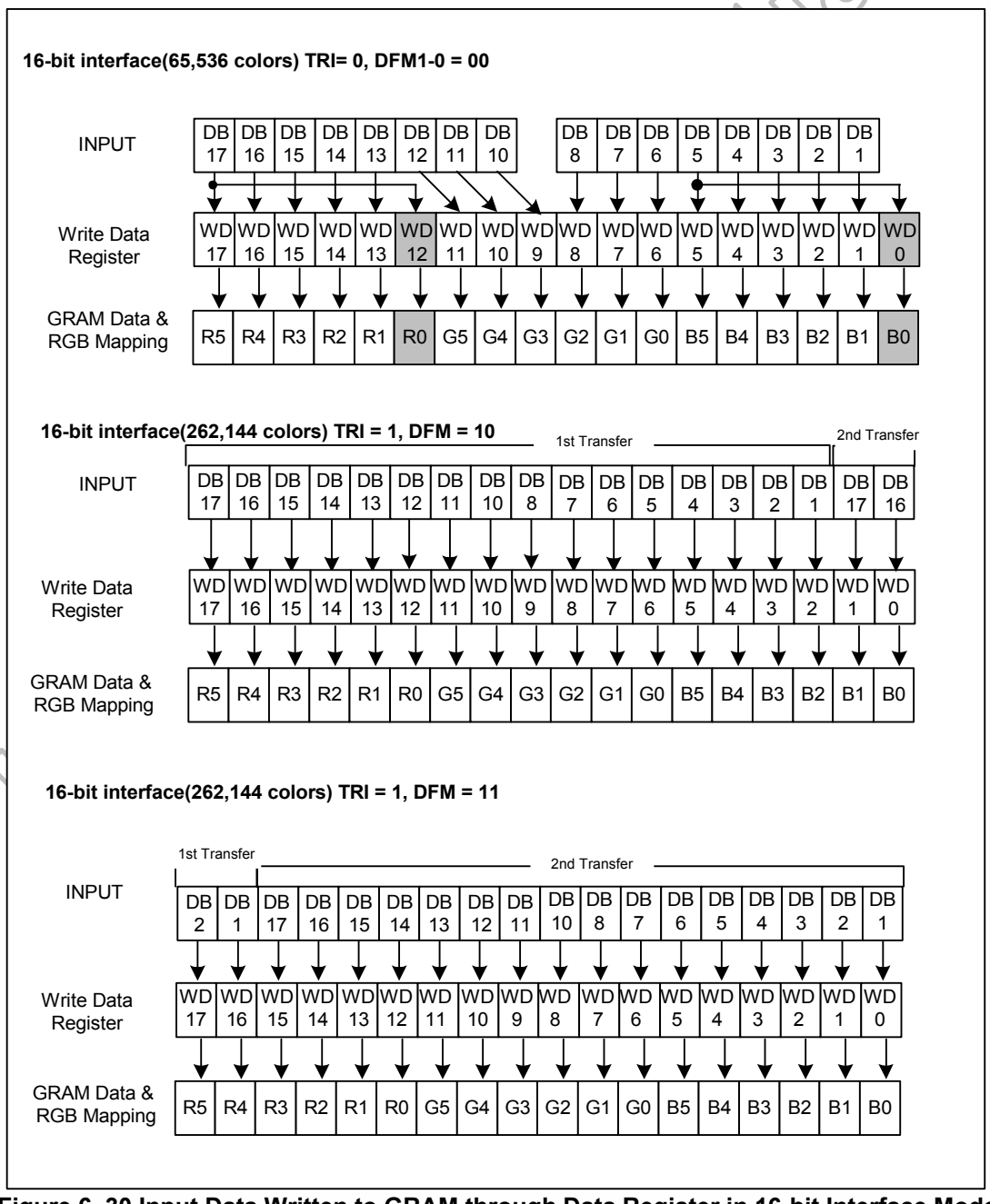


Figure 6. 30 Input Data Written to GRAM through Data Register in 16-bit Interface Mode

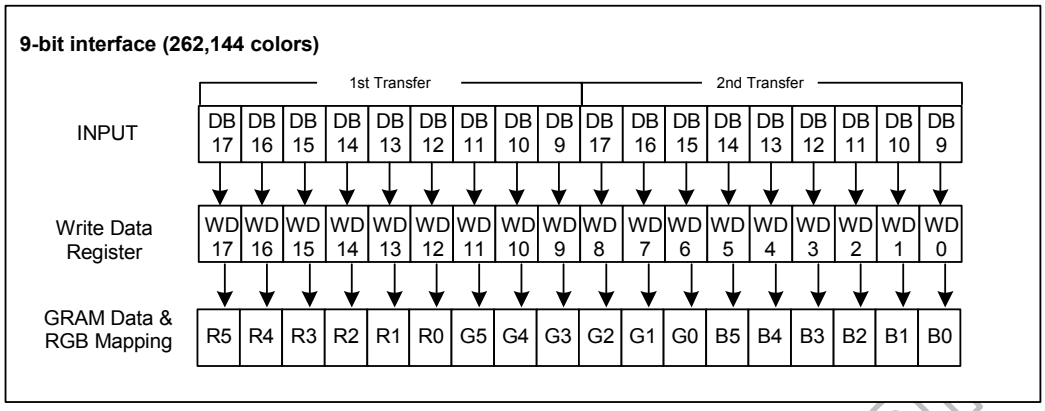


Figure 6. 31 Input Data Written to GRAM through Data Register in 9-bit Interface Mode

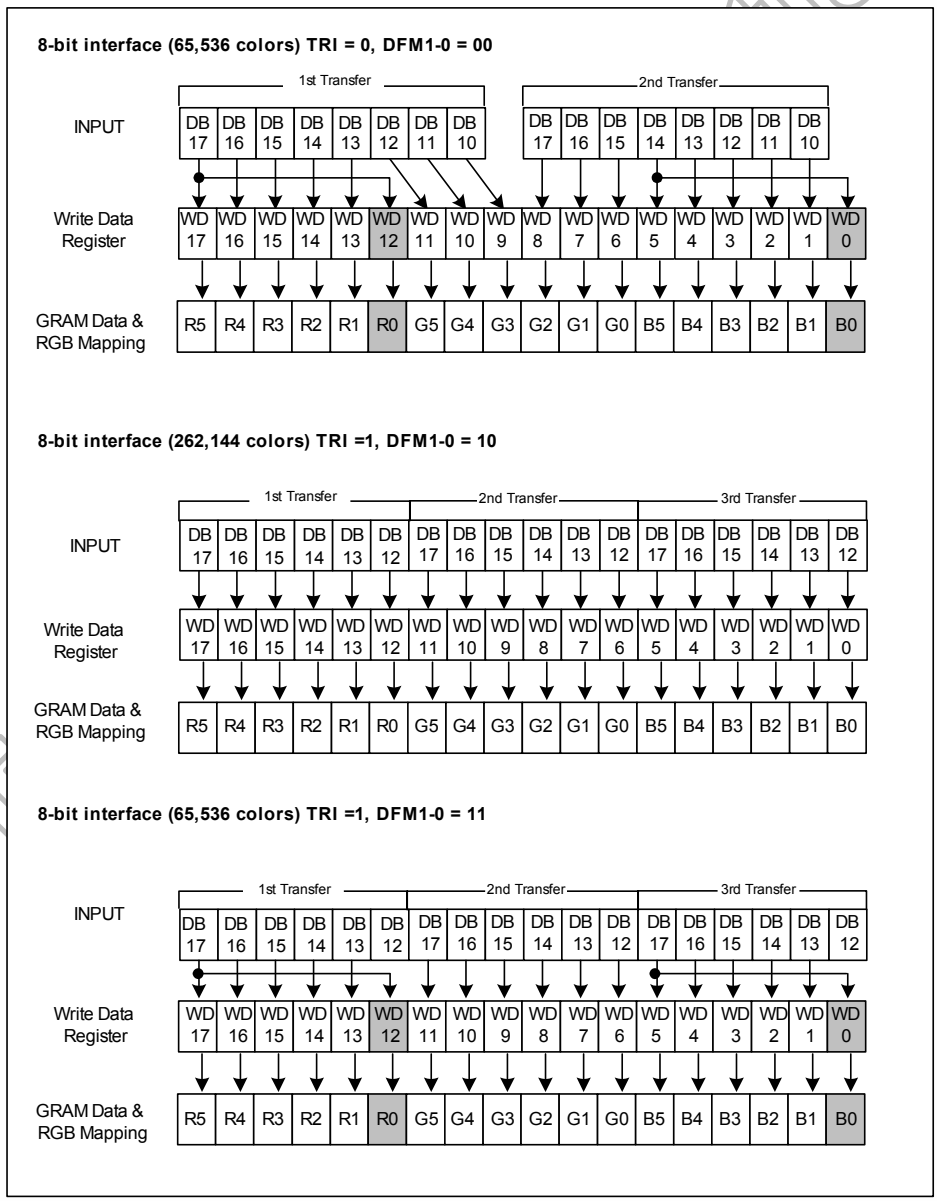


Figure 6. 32 Input Data Written to GRAM through Write Data Register in 8-bit Interface Mode

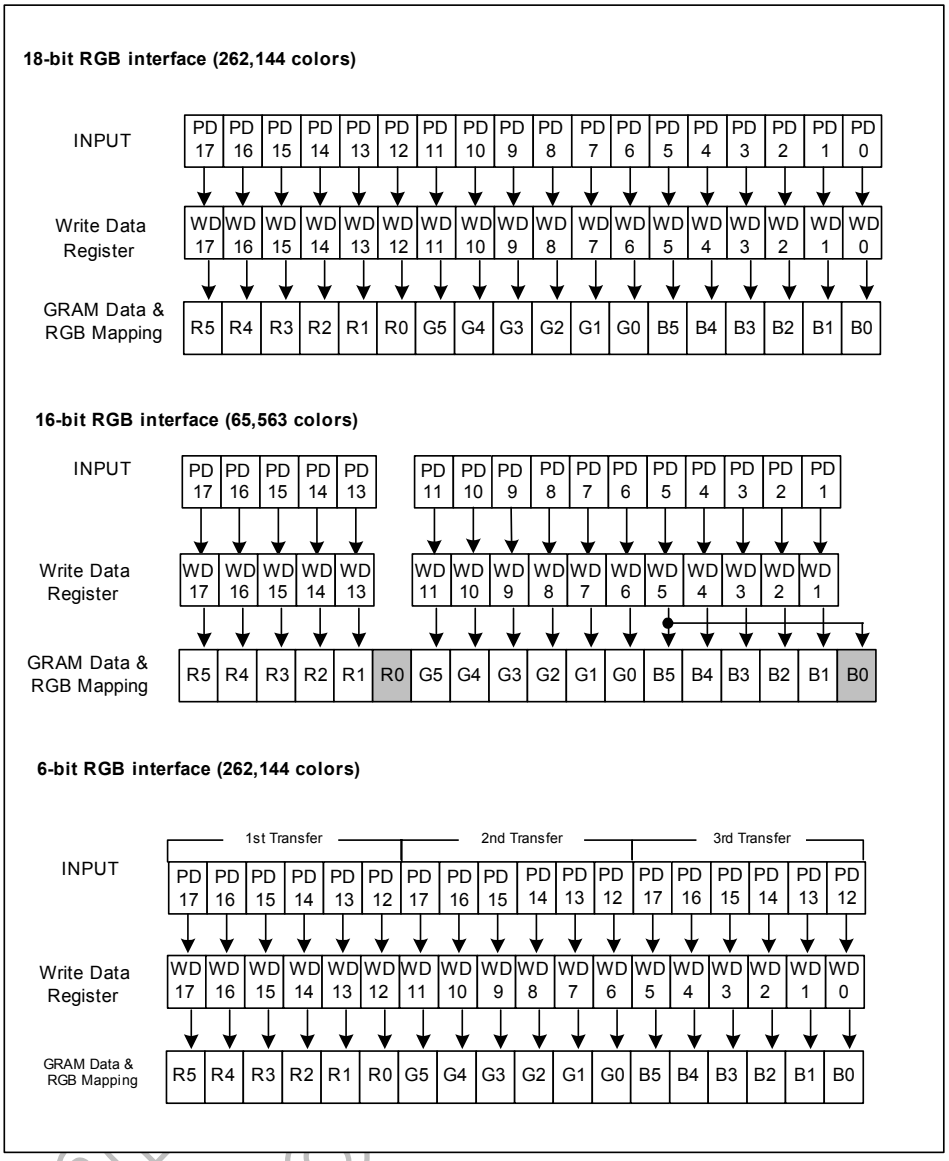


Figure 6. 33 Input Data Written to GRAM through Write Data Register in 18-/16-/6-bit RGB Interface Mode

GRAM data settings RGB	Grayscale	
	Positive	Negative
000000	VINP0	VINN7
000001	43/48*VINP1 + 5/48*VINP0	5/48*VINN7 + 43/48*VINN5
000010	6/48*VINP2 + 42/48*VINP1	42/48*VINN6 + 6/48*VINN5
000011	18/48*VINP2 + 30/48*VINP1	30/48*VINN6 + 18/48*VINN5
000100	25/48*VINP2 + 23/48*VINP1	23/48*VINN6 + 25/48*VINN5
000101	32/48*VINP2 + 16/48*VINP1	16/48*VINN6 + 32/48*VINN5
000110	36/48*VINP2 + 12/48*VINP1	12/48*VINN6 + 36/48*VINN5
000111	40/48*VINP2 + 8/48*VINP1	8/48*VINN6 + 40/48*VINN5
001000	44/48*VINP2 + 4/48*VINP1	4/48*VINN6 + 44/48*VINN5
001001	VINP2	VINN5
001010	4/48*VINP3 + 44/48*VINP2	44/48*VINN5 + 4/48*VINN4
001011	8/48*VINP3 + 40/48*VINP2	40/48*VINN5 + 8/48*VINN4
001100	12/48*VINP3 + 36/48*VINP2	36/48*VINN5 + 12/48*VINN4
001101	16/48*VINP2 + 32/48*VINP2	32/48*VINN5 + 16/48*VINN4
001110	20/48*VINP2 + 28/48*VINP2	28/48*VINN5 + 20/48*VINN4
001111	24/48*VINP2 + 24/48*VINP2	24/48*VINN5 + 24/48*VINN4
010000	28/48*VINP2 + 20/48*VINP2	20/48*VINN5 + 28/48*VINN4
010001	32/48*VINP2 + 16/48*VINP2	16/48*VINN5 + 32/48*VINN4
010010	36/48*VINP2 + 12/48*VINP2	12/48*VINN5 + 36/48*VINN4
010011	40/48*VINP2 + 8/48*VINP2	8/48*VINN5 + 40/48*VINN4
010100	44/48*VINP2 + 4/48*VINP2	4/48*VINN5 + 44/48*VINN4
010101	VINP3	VINN4
010110	3/48*VINP4 + 45/48*VINP3	45/48*VINN4 + 3/48*VINN3
010111	6/48*VINP4 + 42/48*VINP3	42/48*VINN4 + 6/48*VINN3
011000	8/48*VINP4 + 40/48*VINP3	40/48*VINN4 + 8/48*VINN3
011001	10/48*VINP4 + 38/48*VINP3	38/48*VINN4 + 10/48*VINN3
011010	12/48*VINP4 + 36/48*VINP3	36/48*VINN4 + 12/48*VINN3
011011	14/48*VINP4 + 34/48*VINP3	34/48*VINN4 + 14/48*VINN3
011100	16/48*VINP4 + 32/48*VINP3	32/48*VINN4 + 16/48*VINN3
011101	18/48*VINP4 + 30/48*VINP3	30/48*VINN4 + 18/48*VINN3
011110	20/48*VINP4 + 28/48*VINP3	28/48*VINN4 + 20/48*VINN3
011111	22/48*VINP4 + 26/48*VINP3	26/48*VINN4 + 22/48*VINN3
100000	24/48*VINP4 + 24/48*VINP3	24/48*VINN4 + 24/48*VINN3
100001	26/48*VINP4 + 22/48*VINP3	22/48*VINN4 + 26/48*VINN3
100010	28/48*VINP4 + 20/48*VINP3	20/48*VINN4 + 28/48*VINN3
100011	30/48*VINP4 + 18/48*VINP3	18/48*VINN4 + 30/48*VINN3
100100	32/48*VINP4 + 16/48*VINP3	16/48*VINN4 + 32/48*VINN3
100101	34/48*VINP4 + 14/48*VINP3	14/48*VINN4 + 34/48*VINN3
100110	36/48*VINP4 + 12/48*VINP3	12/48*VINN4 + 36/48*VINN3
100111	38/48*VINP4 + 10/48*VINP3	10/48*VINN4 + 38/48*VINN3
101000	40/48*VINP4 + 8/48*VINP3	8/48*VINN4 + 40/48*VINN3
101001	42/48*VINP4 + 6/48*VINP3	6/48*VINN4 + 42/48*VINN3
101010	45/48*VINP4 + 3/48*VINP3	3/48*VINN4 + 45/48*VINN3
101011	VINP4	VINN3
101100	4/48*VINP5 + 44/48*VINP4	44/48*VINN3 + 4/48*VINN2
101101	8/48*VINP5 + 40/48*VINP4	40/48*VINN3 + 8/48*VINN2
101110	12/48*VINP5+ 36/48*VINP4	36/48*VINN3 + 12/48*VINN2
101111	16/48*VINP5 + 32/48*VINP4	32/48*VINN3 + 16/48*VINN2
110000	20/48*VINP5 + 28/48*VINP4	28/48*VINN3 + 20/48*VINN2
110001	24/48*VINP5 + 24/48*VINP4	24/48*VINN3 + 24/48*VINN2
110010	28/48*VINP5 + 20/48*VINP4	20/48*VINN3 + 28/48*VINN2
110011	32/48*VINP5 + 16/48*VINP4	16/48*VINN3 + 32/48*VINN2
110100	36/48*VINP5 + 12/48*VINP4	12/48*VINN3 + 36/48*VINN2
110101	40/48*VINP5 + 8/48*VINP4	8/48*VINN3 + 40/48*VINN2
110110	44/48*VINP5 + 4/48*VINP4	4/48*VINN3 + 44/48*VINN2
110111	VINP5	VINN2
111000	4/48*VINP6 + 44/48*VINP5	44/48*VINN2 + 4/48*VINN1
111001	8/48*VINP6 + 40/48*VINP5	40/48*VINN2 + 8/48*VINN1
111010	12/48*VINP6 + 36/48*VINP5	36/48*VINN2 + 12/48*VINN1
111011	16/48*VINP6 + 32/48*VINP5	32/48*VINN2 + 16/48*VINN1
111100	23/48*VINP6+ 25/48*VINP5	25/48*VINN2 + 23/48*VINN1
111101	30/48*VINP6 + 18/48*VINP5	18/48*VINN2 + 30/48*VINN1
111110	15/48*VINP7 + 33/48*VINP6	43/48*VINN1 + 5/48*VINN0
111111	VINP7	VINN0

Table 6. 35 GRAM Data and Grayscale Level

6.14 Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 6. 34 Read Data Register (R22h)

RD17–0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

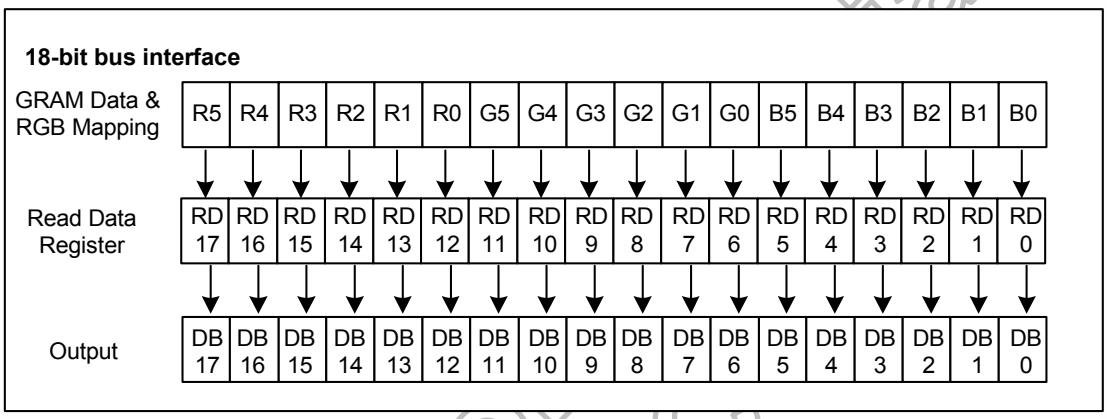


Figure 6. 35 Output Data Read from GRAM through Read Data Register in 18-bit Interface

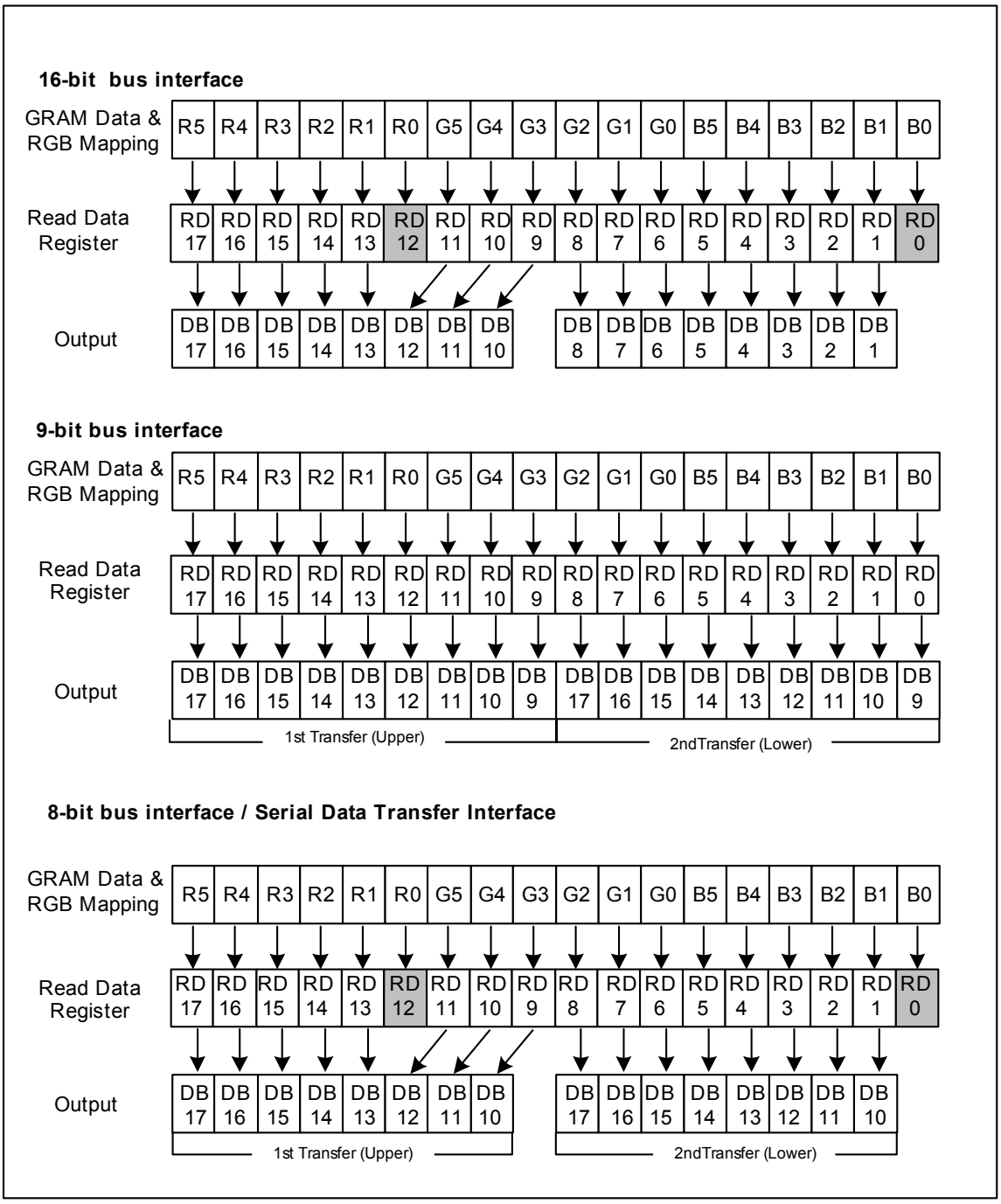


Figure 6. 36 Output Data Read from GRAM through Read Data Register in 16- /9- /8-bit Interface Mode

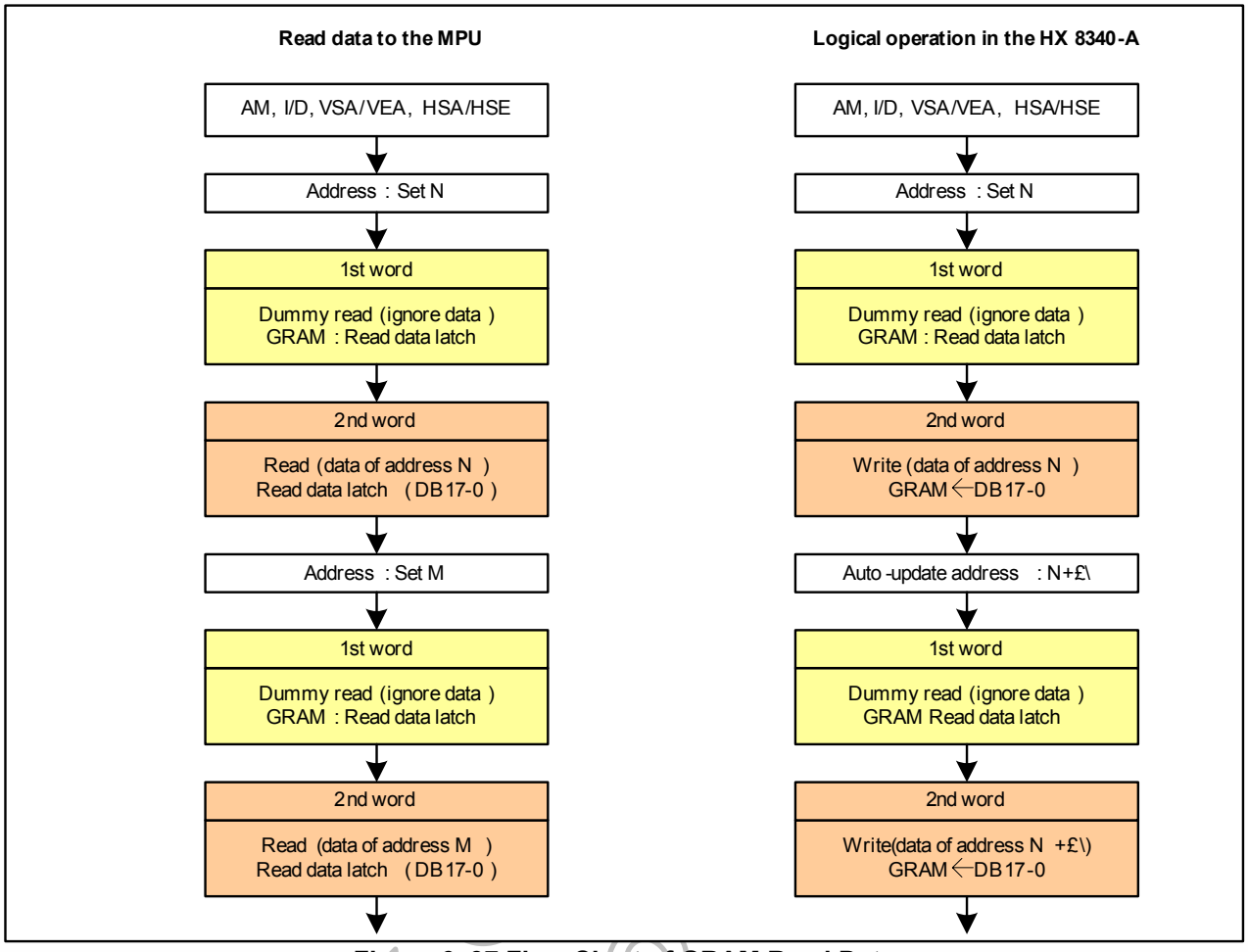


Figure 6. 37 Flow Chart of GRAM Read Data

6.15 Write Data Mask Register Set

6.15.1 Write Data Mask Register 1 (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0

Figure 6. 38 Write Data Mask Register 1 (R23h)

6.15.2 Write Data Mask Register 2 (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12

Figure 6. 39 Write Data Mask Register 1 (R24h)

WM17–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM17 = 1, this bit mask the write data of RB17 and does not write to the GRAM. Similarly, the WM16~WM0 bit masks the write data of RB16~RB0 in a bit unit. For details, see the Graphics Operation Function section.

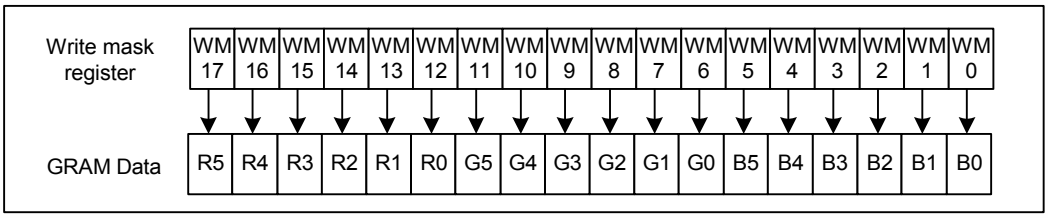


Figure 6. 40 GRAM Write Data Mask

6.16 Gamma Control Register Set

	R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R30	W	1	0	0	0	0	0	MP1 (2)	MP1 (1)	MP1 (0)	0	0	0	0	0	MP0 (2)	MP0 (1)	MP0 (0)
R31	W	1	0	0	0	0	0	MP3 (2)	MP3 (1)	MP3 (0)	0	0	0	0	0	MP2 (2)	MP2 (1)	MP2 (0)
R32	W	1	0	0	0	0	0	MP5 (2)	MP3 (1)	MP5 (0)	0	0	0	0	0	MP4 (2)	MP4 (1)	MP4 (0)
R33	W	1	0	0	0	0	0	CP1 (2)	CP1 (1)	CP1 (0)	0	0	0	0	0	CP0 (2)	CP0 (1)	CP0 (0)
R34	W	1	0	0	0	0	0	MN1 (2)	MN1 (1)	MN1 (0)	0	0	0	0	0	MN0 (2)	MN0 (1)	MN0 (0)
R35	W	1	0	0	0	0	0	MN3 (2)	MN3 (1)	MN3 (0)	0	0	0	0	0	MN2 (2)	MN2 (1)	MN2 (0)
R36	W	1	0	0	0	0	0	MN5 (2)	MN5 (1)	MN5 (0)	0	0	0	0	0	MN4 (2)	MN4 (1)	MN4 (0)
R37	W	1	0	0	0	0	0	CN1 (2)	CN1 (1)	CN1 (0)	0	0	0	0	0	CN0 (2)	CN0 (1)	CN0 (0)
R38	W	1	0	0	0	OP1 (4)	OP1 (3)	OP1 (2)	OP1 (1)	OP1 (0)	0	0	0	0	OP0 (3)	OP0 (2)	OP0 (1)	OP0 (0)
R39	W	1	0	0	0	ON1 (4)	ON1 (3)	ON1 (2)	ON1 (1)	ON1 (0)	0	0	0	0	ON0 (3)	ON0 (2)	ON0 (1)	ON0 (0)

Figure 6. 41 Gamma Control Register 1~10 (R30h~R39h)

MP5-0 [2:0]: Gamma adjustment registers for positive polarity output
CP1-0 [2:0]: Gamma gradient adjustment registers for positive polarity output
MN5-0 [2:0]: Gamma adjustment registers for negative polarity output
CN1-0 [2:0]: Gamma gradient adjustment registers for negative polarity output
OP0 [3:0]/OP1 [4:0]: amplification adjustment resistor for positive polarity output
ON0 [3:0]/ON1 [4:0]: amplification average adjustment resistor for negative polarity output
For details, refer to Gamma Adjustment Function section.

6.17 Gate Scan Position Register (R40h)

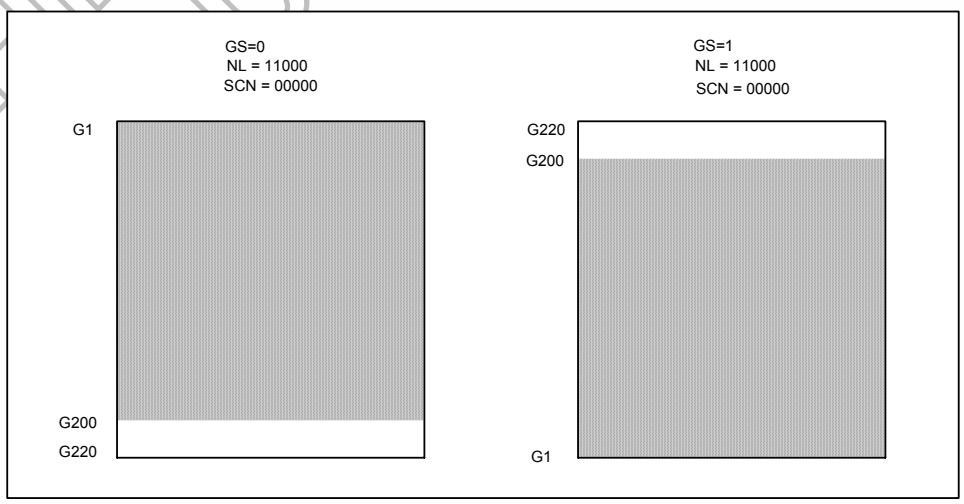
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 6. 42 Gate Scan Position Register (R40h)

SCN4-0: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172
0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107
1	0	1	1	0	G177	G44	G130	G91
1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

Table 6. 36 SCN bits and Scanning Start Position for Gate Driver



Note: (1) Don't set NL, SCN over the end position of gate line (G220)
(2) Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 220.

Figure 6. 43 SCN Bits and Scanning Start Position for Gate Driver

6.18 Vertical Scroll Control Register (R41h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 6. 44 Vertical Scroll Control Register (R41h)

VL7–0: Specify the amount of scrolling line from 0 to 220 in the display to enable smooth vertical scrolling. If GRAM address mapping would exceed “DBxx”H, GRAM address mapping would restart from “00xx”H after the data in “DBxx”H of GRAM being displayed. The display-start line (VL7–0) is valid only when VLE1 = 1 or VLE2 = 1. The display-start line is fixed to zero when VLE2-1 = 00. (VLE1 is the 1st display window vertical-scroll enable bit, and VLE2 is the 2nd display window vertical-scroll enable bit.)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Length
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
:	:	:	:	:	:	:	:	:
1	1	0	1	1	0	0	1	217 lines
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

Table 6. 37 VL Bits and Scrolling Length

6.19 First Display Window Driving Position Register (R42h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

Figure 6. 45 First Screen Driving Position Register (R42h)

SS17–0: Specify the driving start position for the first display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver.

SE17–0: Specify the driving end position for the first display window in a line unit. The LCD driving is performed to the 'setting value + 1' gate driver. See the Partial-Screen Display Function section for details.

6.20 Second Display Window Driving Position Register (R43h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 6. 46 Second Screen Driving Position Register (R43h)

SS27–0: Specify the driving start position for the second display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver. The second display window is driven when SPT = 1.

SE27–0: Specify the driving end position for the second display window in a line unit. The LCD driving is performed to the ' setting value + 1' gate driver.

Note: Ensure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤DBh. For details, see the Partial Screen Display Function section.

6.21 Horizontal RAM Address Position Register (R44h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HAE2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

Figure 6. 47 Horizontal RAM Address Position Register (R44h)

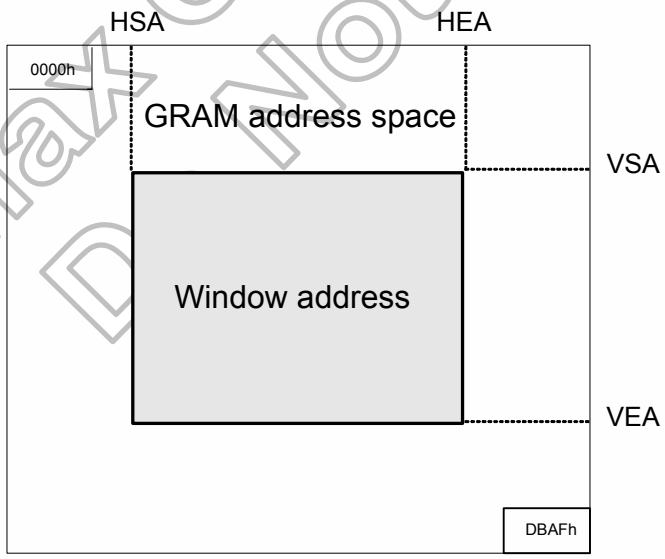
6.22 Vertical RAM Address Position Register (R45h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 6. 48 Vertical RAM Address Position Register (R45h)

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA7-0.Ensure that “00”h ≤HSA7-0 ≤HEA7-0 ≤”AF”h

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA7-0 to the address specified by VEA7-0. Ensure that “00”h ≤VSA7-0 ≤VEA7-0 ≤”DB”h



Window address setting range
“00”h ≤HSA7-0 ≤HEA7-0 ≤”AF”h
“00”h ≤VSA7-0 ≤VEA7-0 ≤”DB”h

Figure 6. 49 Window Address Setting Range

Note: (1) The window address range must be within the GRAM address space.
(2)Data are written to GRAM in four-words when operating in high-speed mode so dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

6.23 Initialization

Output Pin Initialization

(1) Driver output pins (Source outputs): Output VSSD level
(2) Driver output pins (Gate outputs): Output VGH level
(3) Oscillator output pin (OSC2): Output oscillation signal

Instruction Set Initialization

(1) Start oscillation executed
(2) Driver output control (NL4–0 = 11101, SS = 0, GS = 0)
(3) LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
(4) Entry mode set (I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 00: Replace mode)
(5) Compare register (CP17–0: 00000h)
(6) Display control 1 (PT1-0 = 00, VLE2-1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL =0: 262144-color mode, REV = 0, D1–0 = 00: Display off)
(7) Frame cycle control (GD1-0 = 00, SDT1-0 = 00, CE1-0 = 00: No equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clocks in 1-line period)
(8) External display interface control 1 (RIM1-0 = 00: 18-bit RGB interface, DM1-0 = 00: internal clock operation, RM = 0: System interface)
(9) Power control 1 (BT2-0 = 000, DC2–0 = 000, AP2–0 = 000: LCD power off, DK = 1: step-up circuit 1 off, SLP = 0, STB = 0: Standby mode off)
(10) Power control 2 (VC2-0 = 000)
(11) Power control 3 (PON=0, VRH3-0 = 0000)
(12) Power control 4 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
(13) RAM address set (AD15–0 = 0000h)
(14) RAM write data mask (WM17–0 = 000000000000000000: No mask)
(15) Gamma control
(MP02-00 = 000, MP12-10= 000, MP22-20 = 000, MP32-30 = 000, MP42-40 = 000, MP52-50 = 000, CP02-00 = 000, CP12-10 = 000)
(MN02-00 = 000, MN12-10 = 000, MN22-20 = 000, MN32-30 = 000, MN42-40 = 000, MN52-50 = 000, CN02-00 = 000, CN12-10 = 000)
(OP03-00 =0000, OP14-10=00000, ON03-00=0000, ON14-10=0000)
(16) Gate scan starting position (SCN4-0 = 00000)
(17) Vertical scroll (VL7–0 = 00000000)
(18) 1st screen division (SE17-10 = 11011011, SS17-10 = 00000000)
(19) 2nd screen division (SE27-20 = 11011011, SS27-20 = 00000000)
(20) Horizontal RAM address position (HEA7-0 = 10101111, HSA7-0 = 00000000)
(21) Vertical RAM address position (VEA7-0 = 11011011, VSA7-0 = 00000000)

6.24 Reset Function

The HX8340-A is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from the MPU can be accepted. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

GRAM Data Initialization

It must be initialized by software while display is off (D1-0=00).

7. Power Generation

7.1 Specification

The specification of power supply circuit and pins connection are shown as following table:

Pins connection	Recommended voltage	Capacity
VGAM1OUT, VciOUT, VCLC, VcomH,VcomL, C11A/B, C12A/B	6V	1 µF (B characteristics)
VLCDC, C21A/B, C22A/B	10V	1 µF
TVCOMHI, TESTA2, TVMAG	16V	0.1uF
VGHC, VGLC	25V	1 µF

Table 7. 1 Adoptability of Capacitor

Pins connection	Feature
VSSD – VGL (Vci – VGH) (Vci – VLCD)	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

Table 7. 2 Adoptability of Schottkey diode

Reusable	Pins to connect
> 200 kΩ	VcomR

Table 7. 3 Adoptability of Variable resistor

7.2 Power supply Circuit

The power supply circuit of HX8340-A presides over generating supply voltages to drive a LCD panel.

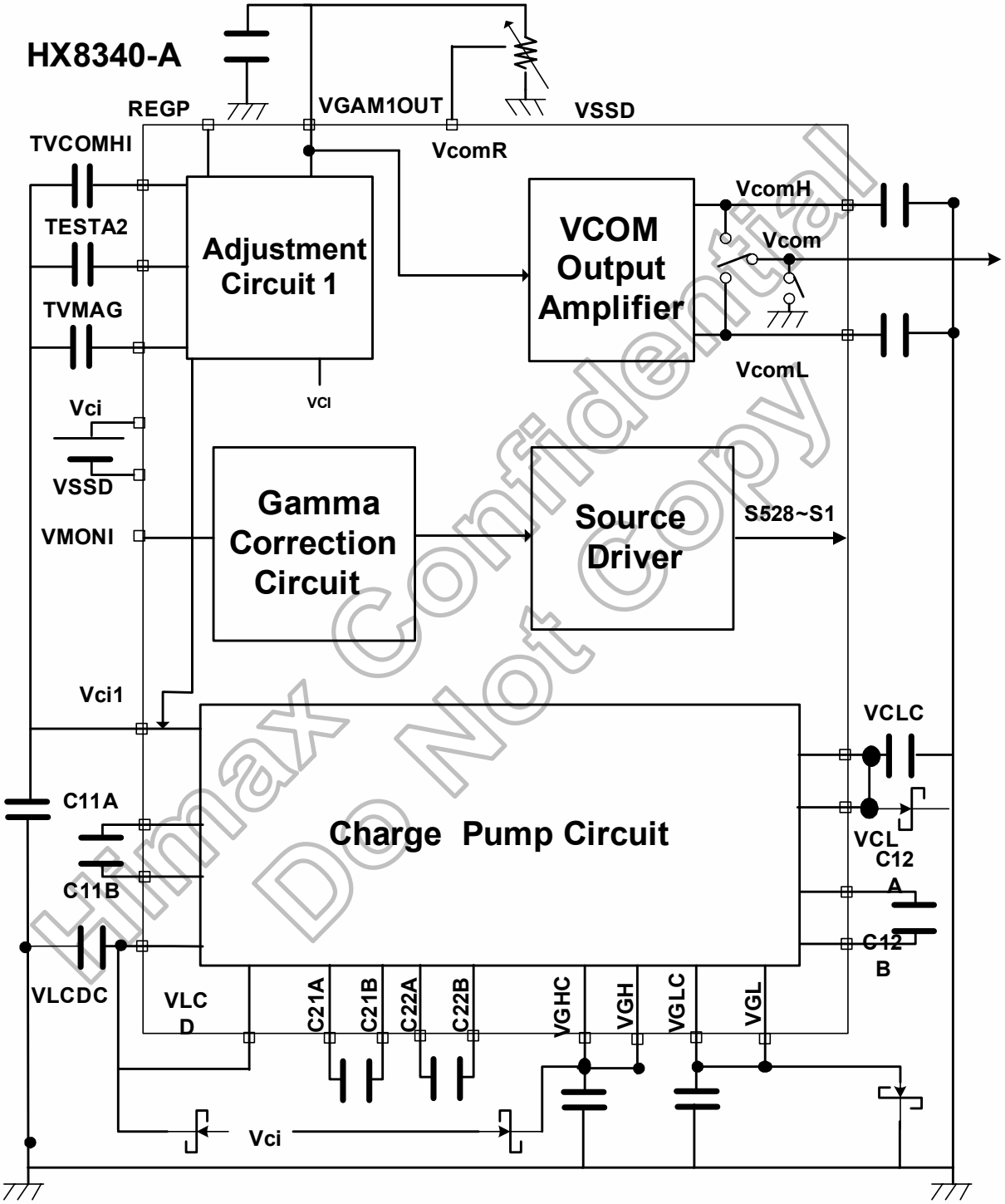


Figure 7. 1 Block Diagram of Power Supply Circuit

7.3 Voltage Setting

The voltage setting pattern diagram of the HX8340-A illustrates as following figure. The outputs of VLCD, VGH, VGL, and VCL are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption. When the Vcom voltage alternating cycle is high, the large current will be consumed.

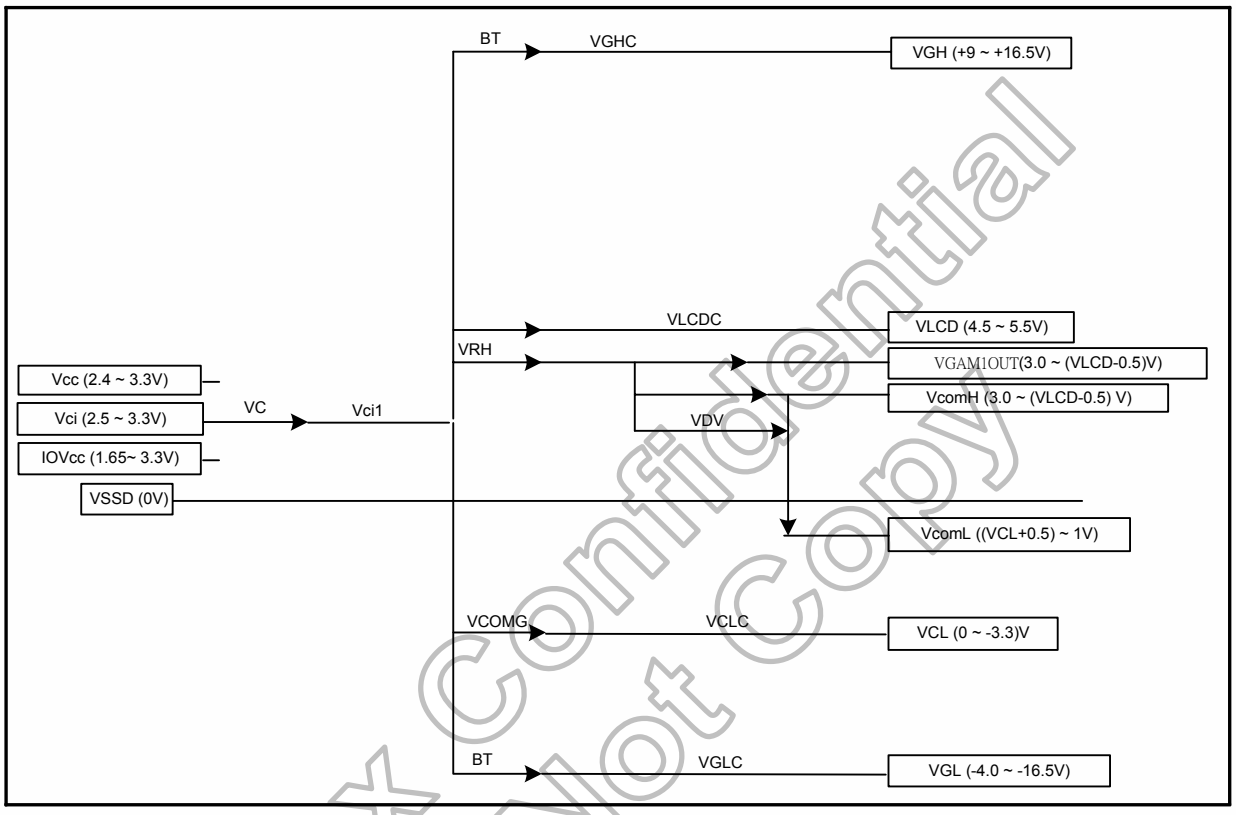


Figure 7. 2 Voltage Setting Diagram

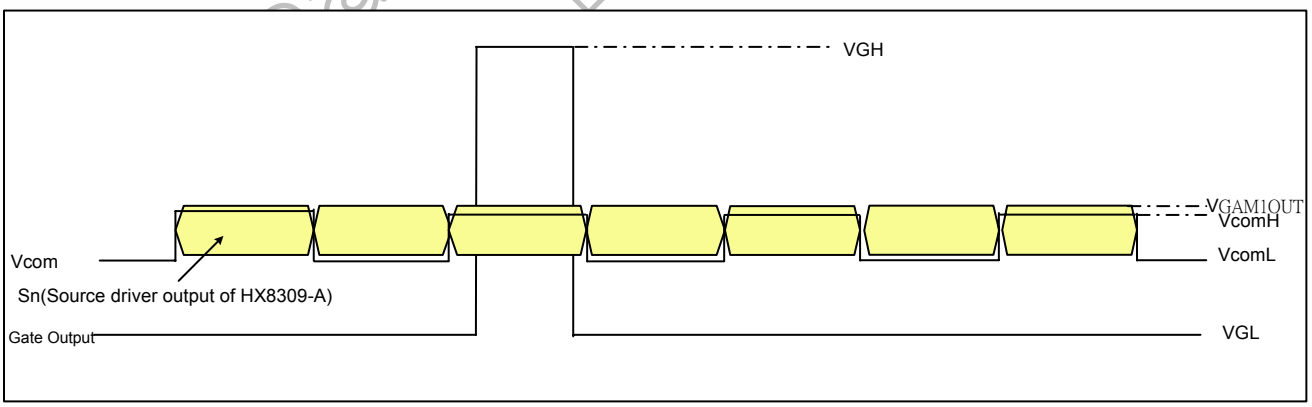


Figure 7. 3 Applied Voltage of TFT Display

7.4 Register Setting

The following are the sequences of register setting flow that applied to the HX8340-A driving the TFT display.

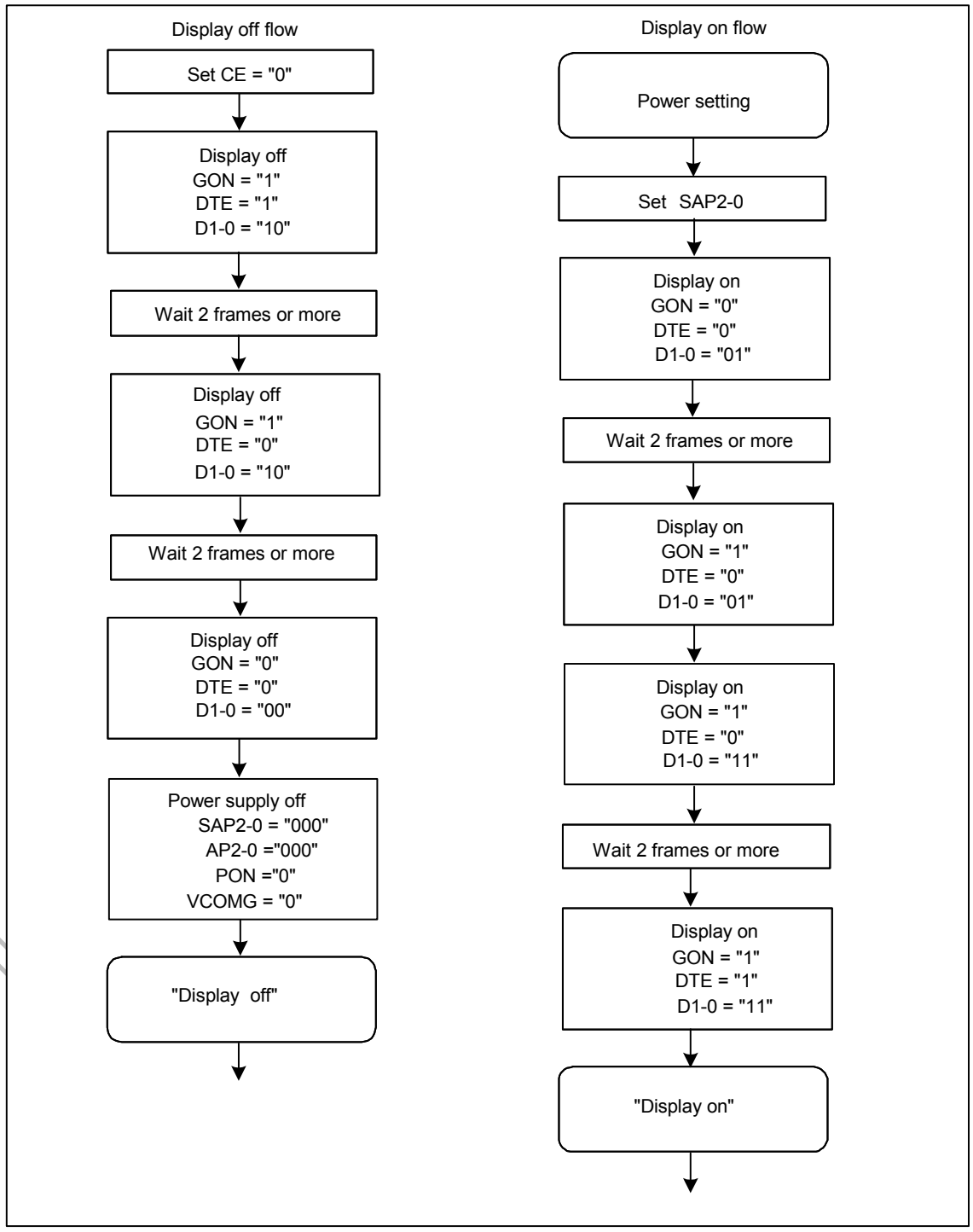


Figure 7. 4 Register Setting Sequence

Standby mode and Sleep Mode setting flow:

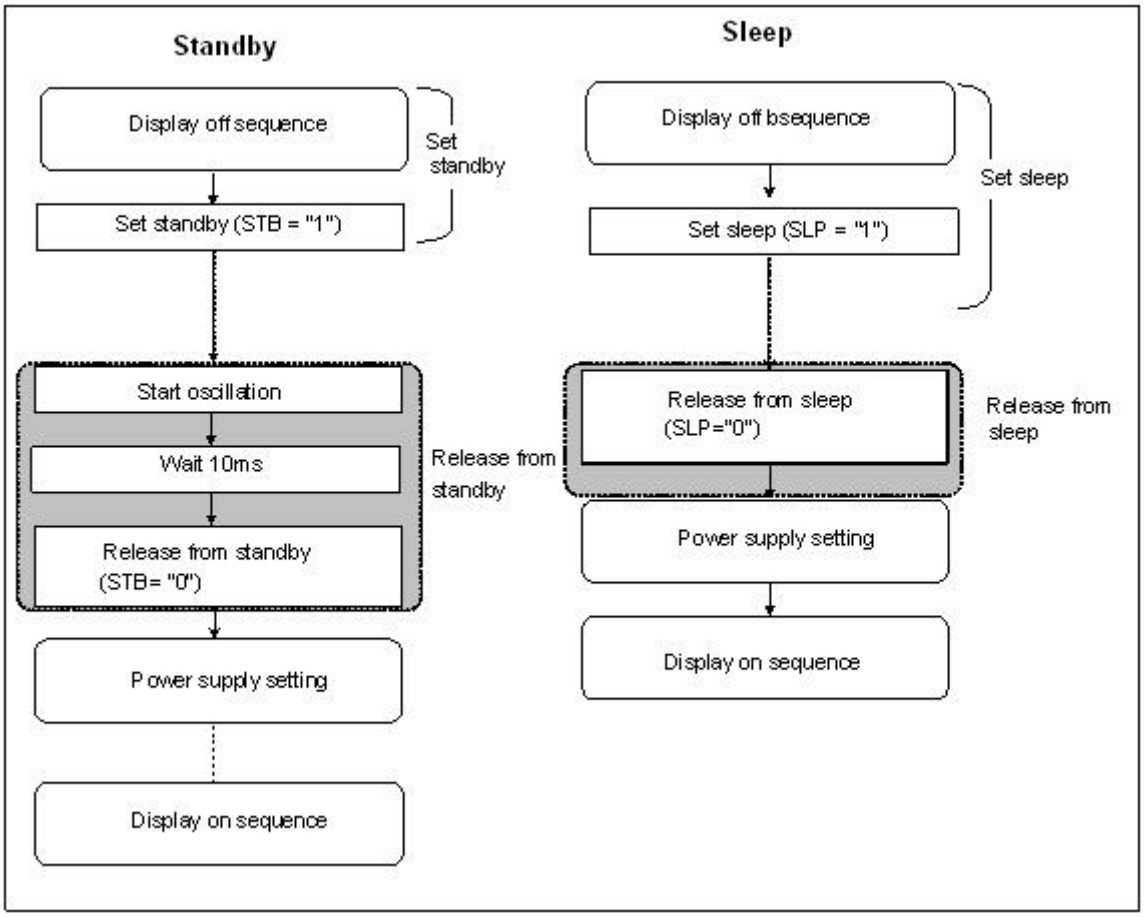


Figure 7. 5 Standby Mode and Sleep Mode Setting Sequence

7.5 Power Supply Setting

The power supply setting sequence of the HX8340-A is follow as blew.

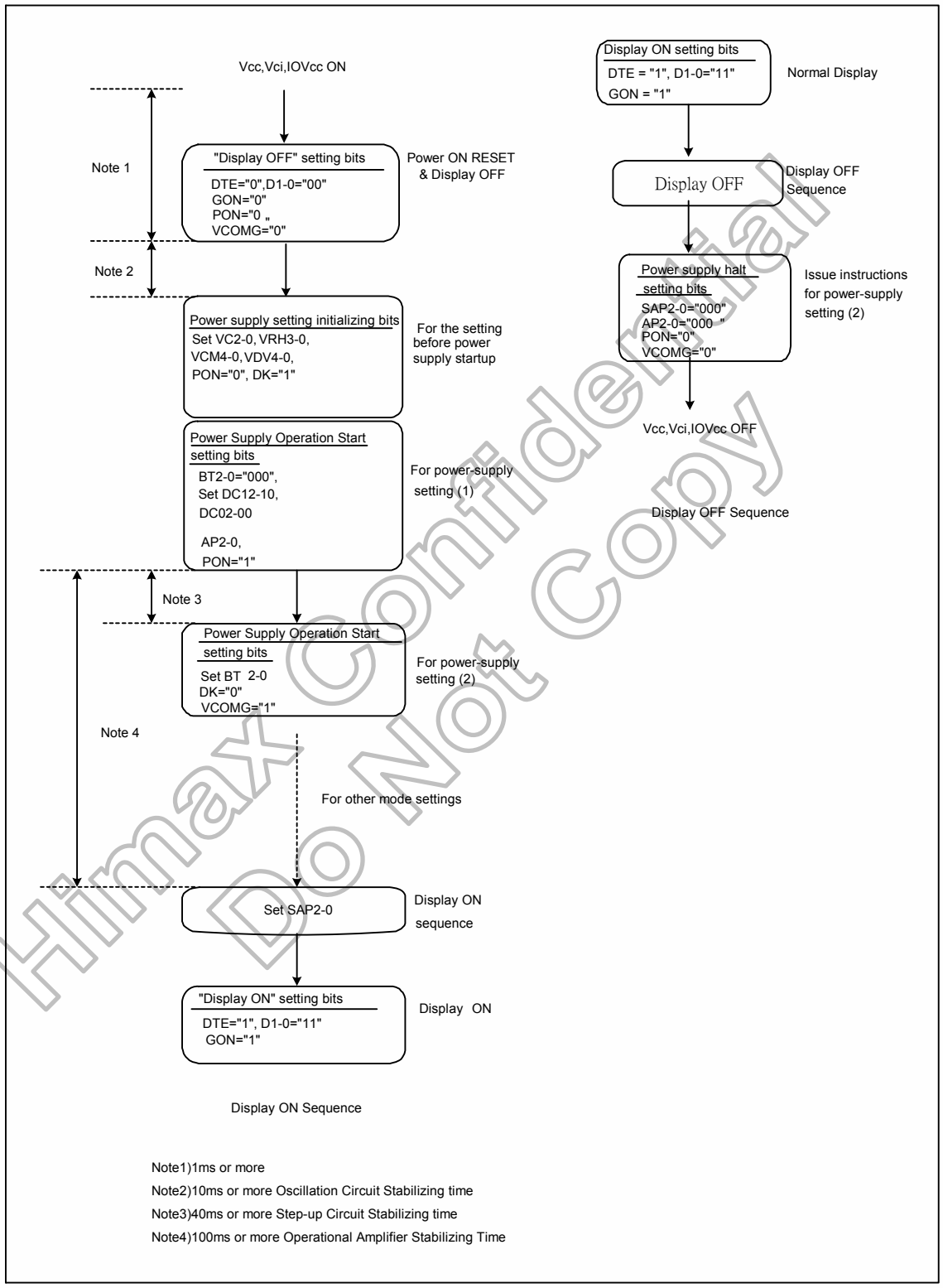


Figure 7. 6 Power Supply Setting Flow

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	Vcc,IOVcc	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	Vci ~ VSSA	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 3	VLCD ~ VSSA	V	-0.3 to +6.0	Note(3)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to +4.6	Note(4)
Power Supply Voltage 5	VLCD ~ VCL	V	-0.3 to +9	Note(5)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note(6)
Power Supply Voltage 7	VSSA ~ VGL	V	-0.3 to +18.5	Note(7)
Input Voltage	Vi	V	-0.3 to Vcc+0.3	-
Operating Temperature	Topr	°C	-40 to +85	Note(8),(9)
Storage Temperature	Tstg	°C	-55 to +110	Note(8),(9)

Note: (1) Vcc, VSSD must be maintained.
(2) To make sure IOVcc ≥ VSSD.
(3) To make sure Vci ≥ VSSA.
(4) To make sure VLCD ≥ VSSA.
(5) To make sure VLCD ≥ VCL.
(6) To make sure VGH ≥ VSSA.
(7) To make sure VSSA ≥ VGL
(8) For die and wafer products, specified up to +85℃.
(9) This temperature specifications apply to the TCP package.

Table 8. 1 Absolute Maximum Rating

8.2 AC Characteristic

Clock Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	f_{cp}	KHz	T.B.D	335	T.B.D	Vcc= 2.4 ~ 3.3V
External clock duty ratio	Duty	%	45	50	55	Vcc=2.4 ~ 3.3V
External clock rise time	Trcp	µs	-	-	0.2	Vcc= 2.4 ~ 3.3V
External clock fall time	Tfcp	µs	-	-	0.2	Vcc= 2.4 ~ 3.3V
R-C oscillation clock	f_{OSC}	KHz	275	335	395	Rf = 130K Ω , Vcc=2.8V

Table 8. 2 Clock Characteristics (Vcc = 2.4 ~ 3.3V)

80-system(18/16 Bits) Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	300	-	-	Figure 8.1
	Read	t_{CYCR}	ns	500	-	-	Figure 8.1
Write low-level pulse width		PW_{LW}	ns	40	-	-	Figure 8.1
Read low-level pulse width		PW_{LR}	ns	250	-	-	Figure 8.1
Write high-level pulse width		PW_{HW}	ns	70	-	-	Figure 8.1
Read high-level pulse width		PW_{HR}	ns	200	-	-	Figure 8.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.1
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	5	-	-	Figure 8.1
	Read (RS to NCS, RW_NRD)			5	-	-	Figure 8.1
Address hold time		t_{AH}	ns	5	-	-	Figure 8.1
Write data setup time		t_{DSW}	ns	15	-	-	Figure 8.1
Write data hold time		t_H	ns	15	-	-	Figure 8.1
Read data delay time		t_{DDR}	ns	-	-	200	Figure 8.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.1

Table 8. 3 Normal Write Mode (IOVcc = 1.65 ~ 2.4V) / (Vcc=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	280	-	-	Figure 8.1
	Read	t_{CYCR}	ns	500	-	-	Figure 8.1
Write low-level pulse width		PW_{LW}	ns	40	-	-	Figure 8.1
Read low-level pulse width		PW_{LR}	ns	250	-	-	Figure 8.1
Write high-level pulse width		PW_{HW}	ns	30	-	-	Figure 8.1
Read high-level pulse width		PW_{HR}	ns	200	-	-	Figure 8.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.1
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	5	-	-	Figure 8.1
	Read (RS to NCS, RW_NRD)			5	-	-	Figure 8.1
Address hold time		t_{AH}	ns	5	-	-	Figure 8.1
Write data setup time		t_{DSW}	ns	15	-	-	Figure 8.1
Write data hold time		t_H	ns	15	-	-	Figure 8.1
Read data delay time		t_{DDR}	ns	-	-	80	Figure 8.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.1

Table 8. 4 Normal Write Mode (IOVcc = 2.4 ~ 3.3V) / (Vcc=2.4~3.3V)

80-system(9/8 Bits) Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	300	-	-	Figure 8.1
	Read	t_{CYCR}	ns	500	-	-	Figure 8.1
Write low-level pulse width		PW_{LW}	ns	40		-	Figure 8.1
Read low-level pulse width		PW_{LR}	ns	250		-	Figure 8.1
Write high-level pulse width		PW_{HW}	ns	30		-	Figure 8.1
Read high-level pulse width		PW_{HR}	ns	200		-	Figure 8.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.1
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	5	-	-	Figure 8.1
	Read (RS to NCS , RW_NRD)			5	-	-	Figure 8.1
Address hold time		t_{AH}	ns	5	-	-	Figure 8.1
Write data set up time		t_{DSW}	ns	15	-	-	Figure 8.1
Write data hold time		t_H	ns	20	-	-	Figure 8.1
Read data delay time		t_{DDR}	ns	-	-	120	Figure 8.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.1

Table 8. 5 Normal Write Mode (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	280	-	-	Figure 8.1
	Read	t_{CYCR}	ns	500	-	-	Figure 8.1
Write low-level pulse width		PW_{LW}	ns	40		-	Figure 8.1
Read low-level pulse width		PW_{LR}	ns	250		-	Figure 8.1
Write high-level pulse width		PW_{HW}	ns	30		-	Figure 8.1
Read high-level pulse width		PW_{HR}	ns	200		-	Figure 8.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.1
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	5	-	-	Figure 8.1
	Read (RS to NCS , RW_NRD)			5	-	-	Figure 8.1
Address hold time		t_{AH}	ns	5	-	-	Figure 8.1
Write data set up time		t_{DSW}	ns	15	-	-	Figure 8.1
Write data hold time		t_H	ns	20	-	-	Figure 8.1
Read data delay time		t_{DDR}	ns	-	-	120	Figure 8.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.1

Table 8. 6 Normal Write Mode (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	100	-	>1ms	Figure 8.2
	Read (transmitted)	t_{SCYC}	μs	350	-	>1ms	Figure 8.2
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	Figure 8.2
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure 8.2
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	Figure 8.2
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure 8.2
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	-	Figure 8.2
Chip select set up time		t_{CSU}	ns	20	-	-	Figure 8.2
Chip select hold time		t_{CH}	ns	60	-	-	Figure 8.2
Serial input data set up time		t_{SISU}	ns	30	-	-	Figure 8.2
Serial input data hold time		t_{SIH}	ns	30	-	-	Figure 8.2
Serial output data set up time		t_{SOD}	ns	-	-	120	Figure 8.2
Serial output data hold time		t_{SOH}	ns	5	-	-	Figure 8.2

Table 8. 7 (IOVcc=1.65~2.4V) / (Vcc=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	100	-	>1ms	Figure 8.2
	Read (transmitted)	t_{SCYC}	μs	350	-	>1ms	Figure 8.2
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	Figure 8.2
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure 8.2
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	Figure 8.2
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure 8.2
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	-	Figure 8.2
Chip select set up time		t_{CSU}	ns	20	-	-	Figure 8.2
Chip select hold time		t_{CH}	ns	60	-	-	Figure 8.2
Serial input data set up time		t_{SISU}	ns	20	-	-	Figure 8.2
Serial input data hold time		t_{SIH}	ns	20	-	-	Figure 8.2
Serial output data set up time		t_{SOD}	ns	-	-	120	Figure 8.2
Serial output data hold time		t_{SOH}	ns	5	-	-	Figure 8.2

Table 8. 8 (IOVcc=2.4~3.3V) / (Vcc=2.4~3.3V)

LCD driver output Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Driver output delay timing	t_{DD}	us	-	35	-	**Figure 8.4** Vci=IOVcc=Vcc=2.8V , Ta=25°C , fOSC = 330KHz, (220 Line) GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, DC0=000, DC1=010,B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=10000, VCOMG=1, CL=0, MP5-0[2:0]=MN5-0[2:0=000, CP1-0[2:0]=CN1-0[2:0]=000, OP0[3:0]= ON0[3:0]=0000 OP1[4:0]= ON1[4:0]=00000

Table 8. 9 Driver output delay timing

Reset Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Reset low level width	t_{RES}	ms	1	-	-	Figure 8.5
Reset rise time	t_{rRES}	ns	-	-	10	Figure 8.5

Table 8. 10 (IOVcc=1.65~3.3V) / (Vcc = 2.4 ~ 3.3V)

8.3 DC Characteristic

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVcc= 1.65 ~ 3.3V	0.8xIOVcc	-	IOVcc	-
Input low voltage	V_{IL}	V	IOVcc= 1.65 ~ 3.3V	-0.3V	-	0.2xIOVcc	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVcc	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVcc= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVcc	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ Vcc	-1	-	1	-
Current consumption during normal operation (Vcc – VSSD)+ (IOVcc-VSSD)	$I_{OP(Vcc)}$	µA	Vci=IOVcc=Vcc=2.8V , Ta=25°C , fOSC = 330KHz (220 Line) GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, DC0=000, DC1=010,B/C=0, BT=001, VC=001, VRH=0011, VCM=10011,VDV=10000, VCOMG=1, CL=0, No panel load	-	150	300	-
Current consumption during normal operation (Vci – VSSD)	$I_{OP(Vci)}$	mA			1.4	1.8	
Current consumption during standby mode (Vcc – VSSD) + (IOVcc-VSSD)	$I_{ST(VCC)}$	µA	Vcc=2.8V , Ta=25°C	-	1	10	-
Current consumption during standby mode (Vci – VSSD)	$I_{ST(VCi)}$	µA			0.5	1	
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 8. 11 DC Characteristic (Vcc = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C)

8.4 Timing Characteristic

80-system Bus Operation

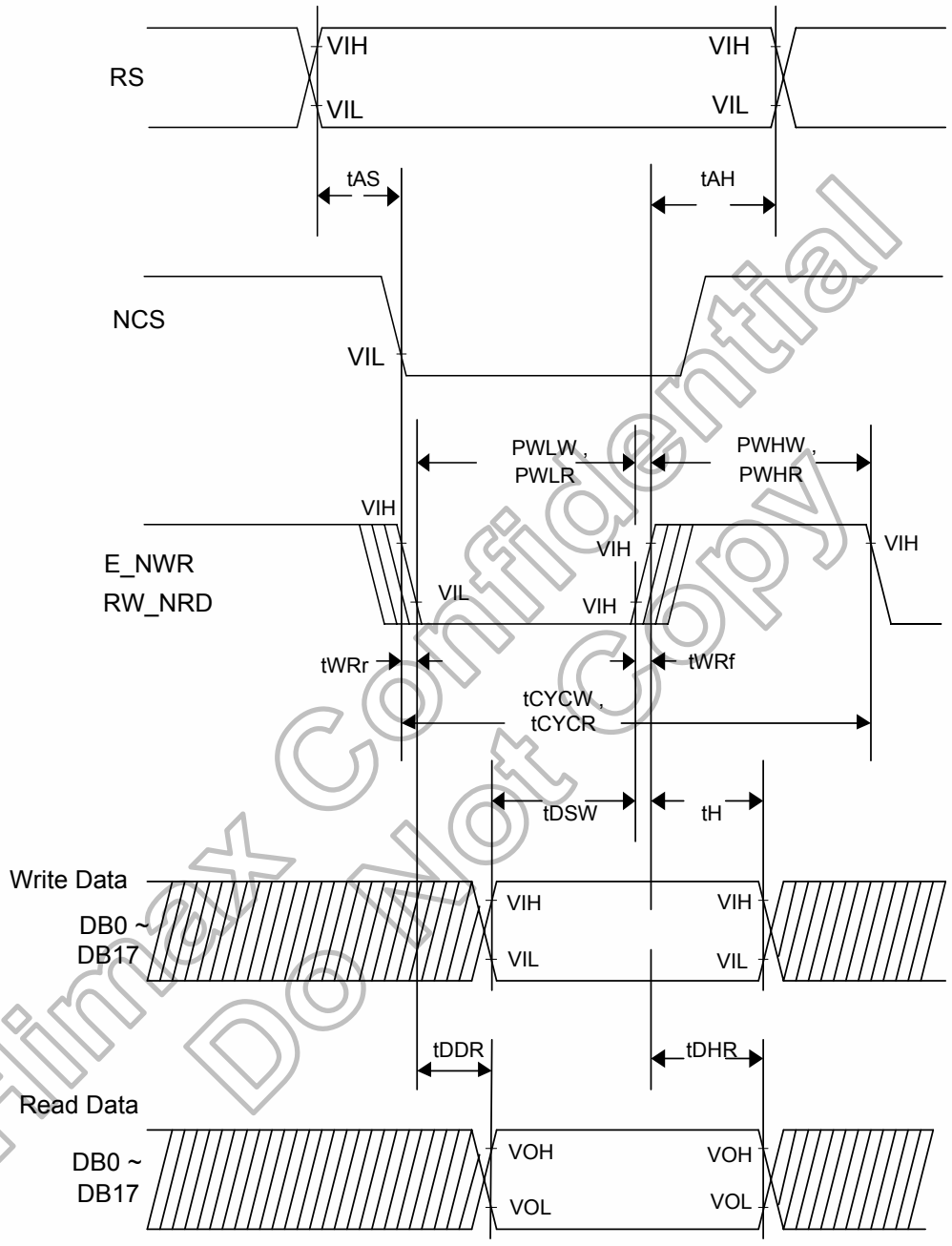


Figure 8. 1 80-system Bus Timing

Clock Synchronized Serial Data Transfer Interface Operation

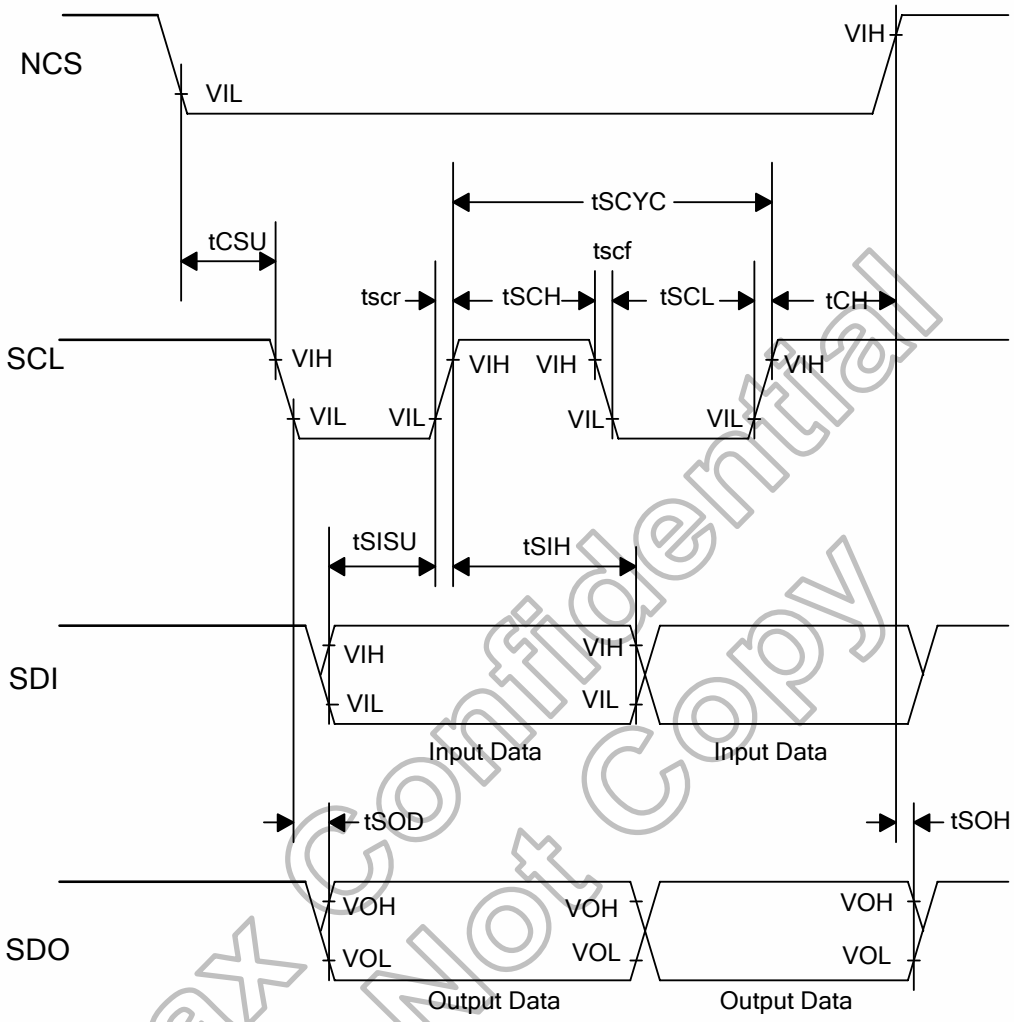


Figure 8. 2 Clock Synchronized Serial Data Transfer Interface Timing

RGB Interface Operation

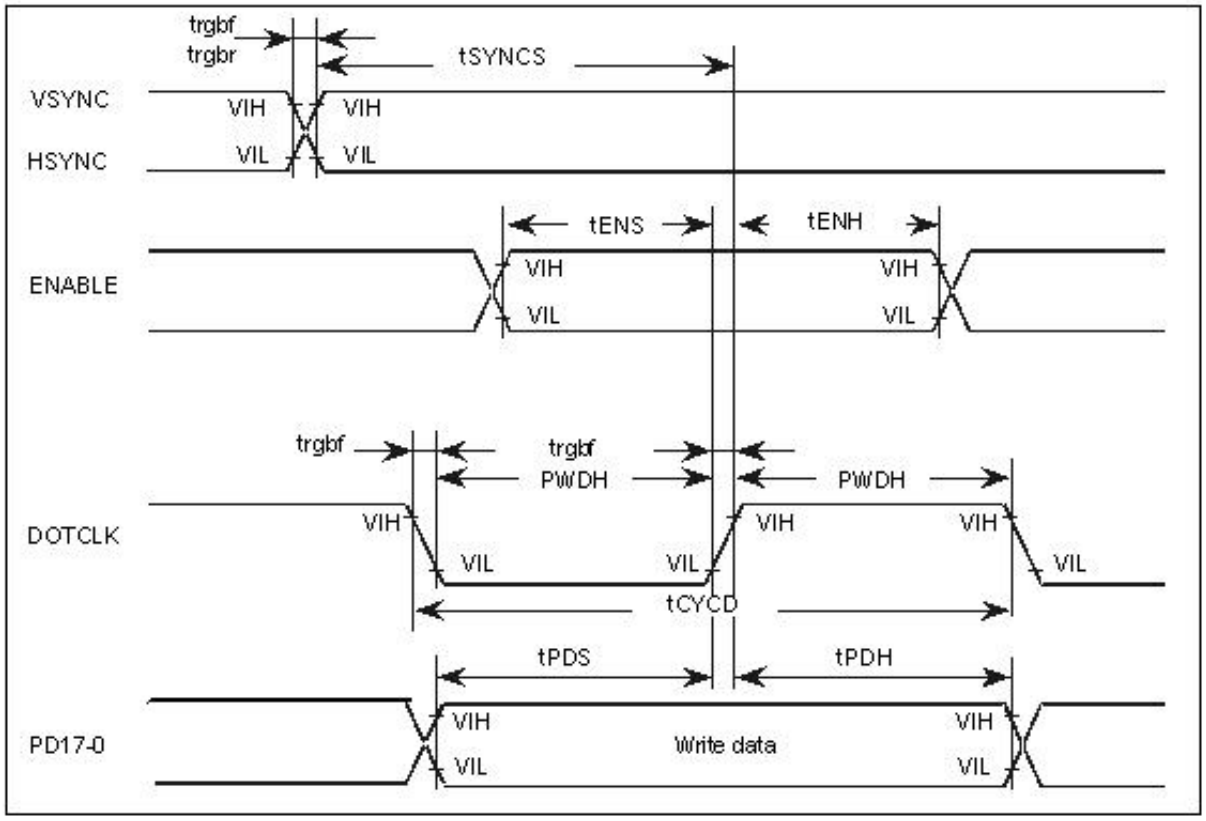


Figure 8. 3 RGB Interface Operation

LCD Driving Output

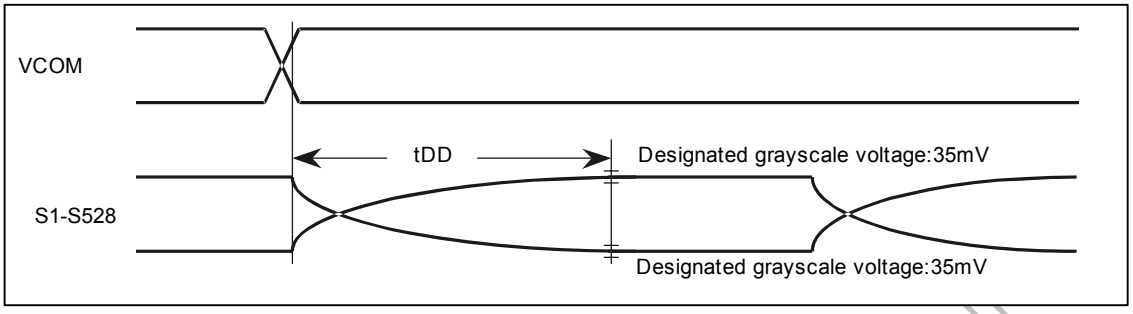


Figure 8. 4 LCD Driving Output

Reset Operation

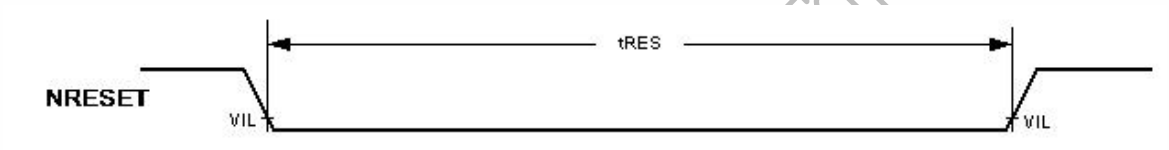


Figure 8. 5 Reset Timing

9. System Configuration

9.1 System Diagram

The system configuration diagram illustrates as following.

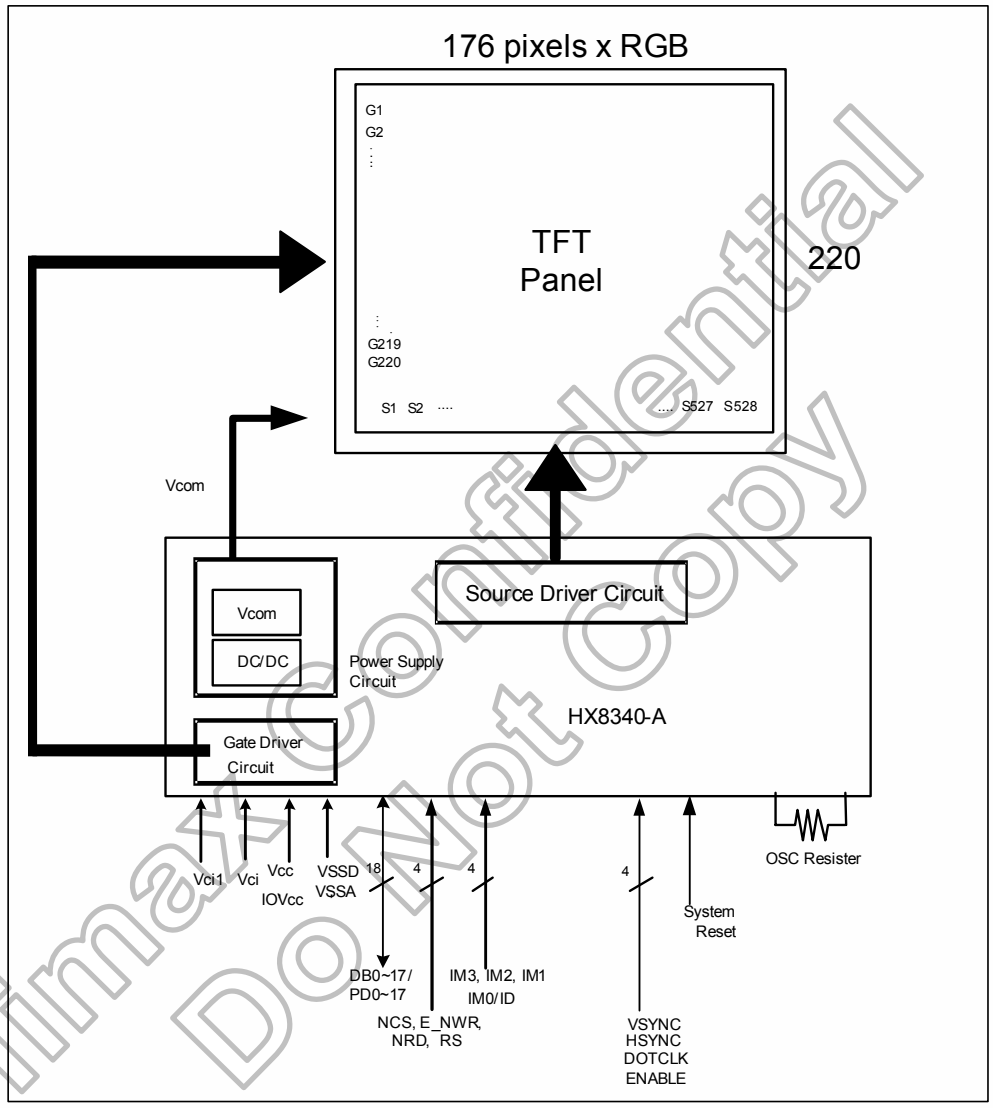
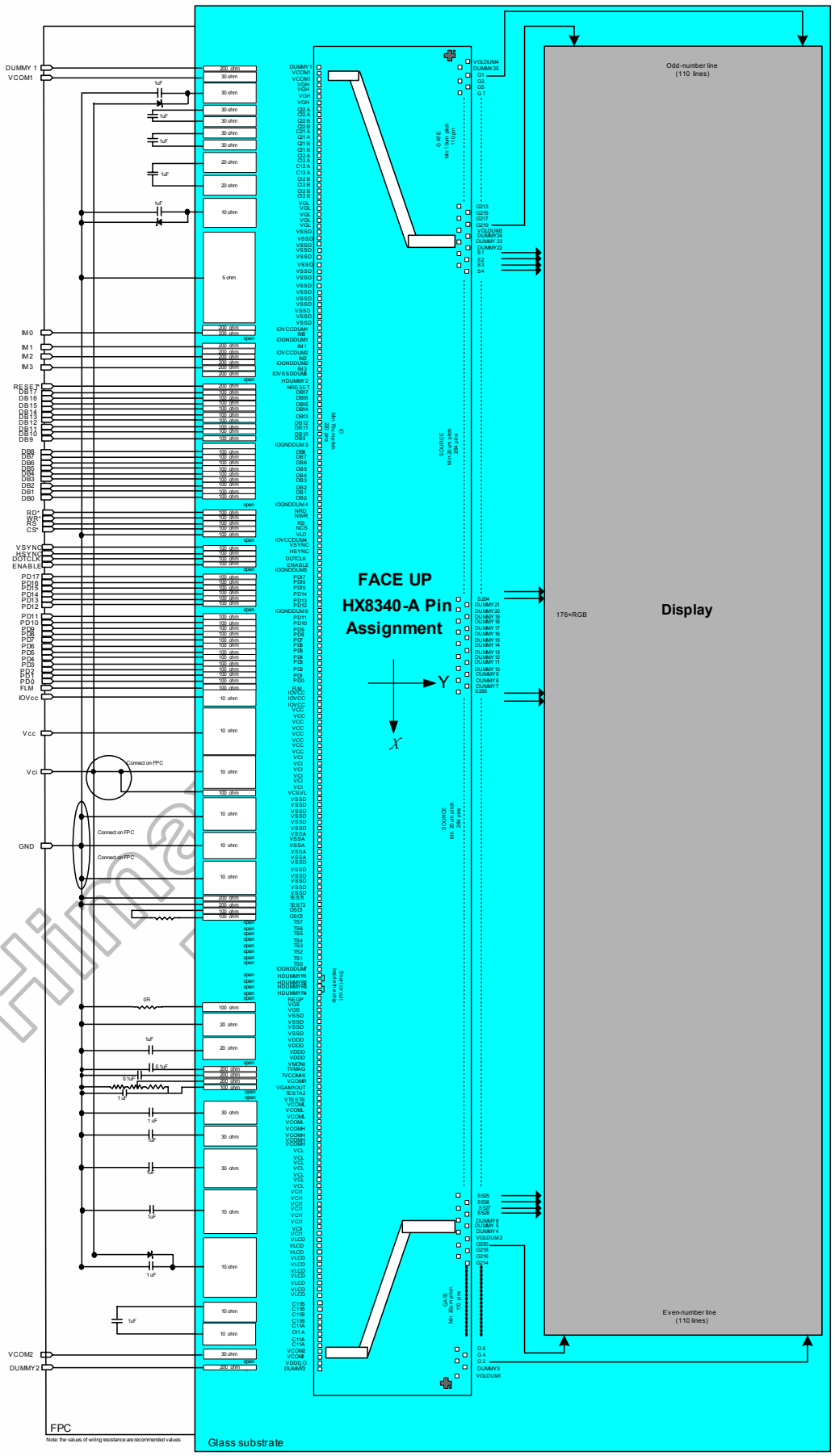


Figure 9. 1 System Diagram of HX8340-A

9.2 Layout Recommendation



10. Ordering information

Part NO.	Package
HX8340-A000 PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400 μm)

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2006/07/14	New setup
02	2006/09/11	1. Remove the contents of unused functions A. High-Speed Burst RAM Write Function B. Graphics Operation Function 2. Mark Chapter 4 sub-titles (4.1~4.23) for content catalog 3. Modify the pin assignment (Remove the Corner dummy information) (Page 16) 4. Corrected the coordinate of alignment mark. (Page 20)
	2006/09/20	1. Remove alignment mark information from pin assignment indication (Page 16) 2. Add in alignment mark information in 3.4 BUMP Arrangement (Page 21)
	2006/09/26	1. Revise the block diagram (Page 10) 2. Modify the pin assignment block for G214~S525 pad position (Page 16, 130) 3. Change the chip size and add in the seal ring, scribe line dimension (Page 16) 4. Update the formula of Frame frequency and the example (Page 64, 91) 5. Modify the Table 5.16 and Figure 5.25 (Page 75) 6. Revise the RTN[3:0] cycle ratio of Table 6.15 (Page 91)
	2006/10/02	1. Change the external oscillator resistor into 100K ohm (Page 75) 2. Remove HWM related descriptions (Page 35, 37, 38, 76, 81, 121~126) 3. Shrink Figure 8. 4 into normal size (Page 128)