DATA SHEET

(DOC No. HX8340-B(T)-DS)

HX8340-B(T)

176RGB x 220 dot, 262k color,
with internal GRAM,
TFT Mobile Single Chip Driver

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1. General Description

This document describes HX8340-B 176RGBx220 dots resolution driving controller. The HX8340-B is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 176RGBx220 dots at maximum.

The HX8340-B can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8340-B also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8340-B supports three interface groups: Command-Parameter interface group, Register-Content interface group and RGB interface mode. Command-Parameter interface mode and Register-Content interface mode are selected by the external pin IFSEL setting, and RGB interface mode is selected by external **RCM[1:0]** pins. This manual description focuses on Register-Content interface mode and RGB interface mode; about the Command-Parameter interface mode, please refer to the HX8340-B(N) datasheet for detail.

2. Features

- Single chip solution to drive a a-TFT LCD panel
- Display Resolution: 176(H) x RGB(H) x 220(V)
- Display Color modes (Register-Content interface mode. (IFSEL= 'L') and RGB interface mode)
  - Normal Display Mode On
    a. System Interface Circuit
      i. 4096(R(4),G(4),B(4)) colors
      ii. 65, 536(R(5),G(6),B(5)) colors
      iii. 262,144(R(6),G(6),B(6)) color
    b. RGB Interface Circuit
      i. 65, 536(R(5),G(6),B(5)) colors
      ii. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    a. 8 (R(1),G(1),B(1)) colors.

- Outputs
  - Source outputs: 528 source lines.
  - Selectable gate line control signal for glass 220 gate lines
  - Adjusted source voltages (V0p ~V63p, V0n ~V63n)

- Display interface:
  - System interface:
    a. 8-/9-/16-/18-bit parallel bus system interface
    b. 3-wires serial bus system interface
  - RGB interface:
    a. 6-/16-/18-bit RGB interface

- Internal graphics RAM capacity: 176 x18x220 bit = 696960bits

- Display features
  - The vertical scroll display function in line units
  - Partial area display mode.
  - Software programmable color depth mode

- On chip
  - OTP memory to store initialization register settings
  - Automatic malfunction recovery for default values (OTP table and other default values reloading after Sleep Out, HW / SW)
  - Internal oscillator and hardware reset function
  - DC/DC converter and charge bump circuit for source, glass gate driving voltage
  - Adjust AC VCOM generation

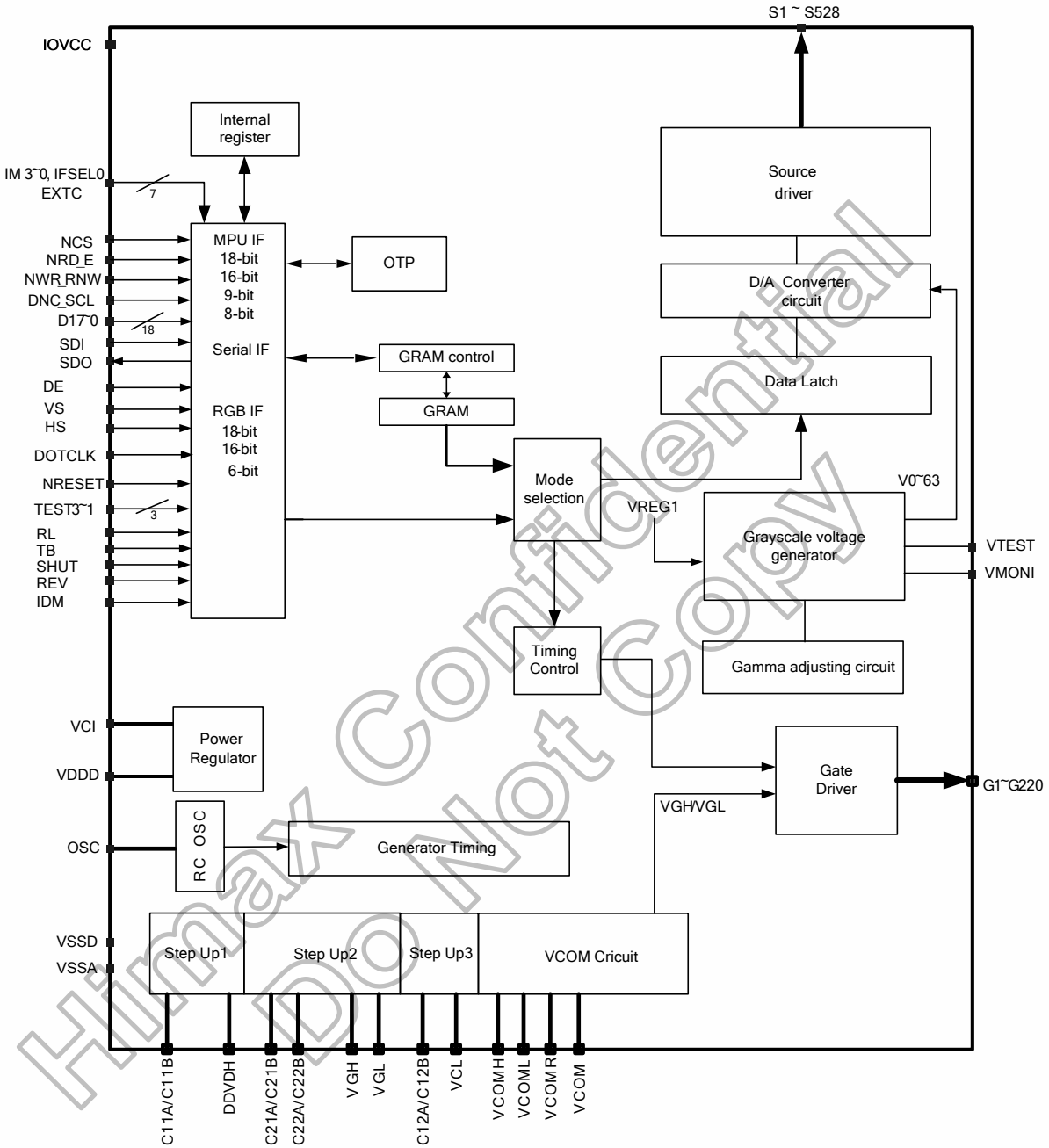
- LCD Driving Inversion Algorithm
  - Frame inversion AC liquid-crystal drive
  - 1~7 line inversion AC liquid-crystal drive

- Input power supply
  - IOVCC = 1.65 to 3.3V (Logic IO power supply voltage range)
  - VCI = 2.5 to 3.3V (Driver power supply voltage range)

- Output voltage levels
  - DDVDH = 5.1 V (Power supply for driver circuit range)
  - VREG1 = 3.3V to 4.8V (Source output voltage range)
  - VGH = +9.0 to +15.3V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
  - VCOMH = 2.5V to 5.0V (Common electrode output high voltage)
  - VCOML = -2.5V to 0.0V (Common electrode output low voltage)

- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Chip on Glass
- Operating temperature range : -40℃~ 85℃

3. Block Diagram



4. Pin Description

4.1 Pin Description

<table>
<tr><th colspan="5">Interface Logic Pin</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM3, IM2, IM1, IM0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>6800 MCU 16-bits Parallel</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>6800 MCU 8-bits Parallel</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel</td></tr>
<tr><td>-</td><td>1</td><td>-</td><td>ID</td><td>Serial interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>6800 MCU 18-bits Parallel</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>6800 MCU 9-bits Parallel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel</td></tr>
</table>
If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MCU</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select input pin.
Low: chip can be accessed;
High: chip cannot be accessed.</td></tr>
<tr><td>DNC</td><td>I</td><td>1</td><td>MCU</td><td>Command / parameter or display data selection pin in parallel bus system interface.
If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>NRD(E)</td><td>I</td><td>1</td><td>MCU</td><td>(NRD) Read enable pin I80 parallel bus system interface.
(E) Read/Write operation enable pin in M68 parallel bus system interface.
If not used, please fix this pin at IOVCC or GND level</td></tr>
<tr><td>NWR(RNW)(SCL)</td><td>I</td><td>1</td><td>MCU</td><td>(NWR) Write enable pin I80 parallel bus system interface.
(RNW) Read/Write select pin in M68 parallel bus system interface.
(SCL) server as serial data clock in serial bus system interface.
If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MCU</td><td>Serial data input pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal.
If not used, please fix this pin at IOVCC or GND level.</td></tr>
<tr><td>SDO</td><td>O</td><td>1</td><td>MCU</td><td>Serial data output pin in serial bus system interface. The data is outputted on the falling edge of SCL signal. SDI and SDO pins are possible to connect together outside of driver IC as one SDA line.
If not used, please let this pin floating.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>18</td><td>MCU</td><td>Input data bus
If not used, please fix this pin at GND level.</td></tr>
<tr><td>VS</td><td>I</td><td>1</td><td>MCU</td><td>Vertical synchronizing signal in RGB interface. Has to be fixed to VSSD level if it is not used.</td></tr>
<tr><td>HS</td><td>I</td><td>1</td><td>MCU</td><td>Horizontal synchronizing signal in RGB interface. Has to be fixed to VSSD level if it is not used.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MCU</td><td>Data enable signal in RGB interface. Has to be fixed to VSSD level if it is not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MCU</td><td>Pixel clock signal in RGB interface. Has to be fixed to VSSD level if is not used.</td></tr>
<tr><td>TE</td><td>O</td><td>1</td><td>MCU</td><td>Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command.
When this pin is not activated (TE function off), this pin is low.
If not used, please let this pin open.</td></tr>
</table>

<table>
<tr><th colspan="5">Mode Select Pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IFSEL</td><td>I</td><td>1</td><td>MPU</td><td>Interface format select pin
<table><tr><th>IFSEL</th><th>Interface Format Selection</th></tr><tr><td>0</td><td>Register-content interface mode</td></tr><tr><td>1</td><td>Command-Parameter interface mode</td></tr></table>In this document, the IFSEL has to be connected to GND and Register-Content interface mode is select.</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>Extended command set access enable bit pin
In Register-content interface mode this pin is invalid.
Internal pull low.</td></tr>
<tr><td>RCM1, RCM0</td><td>I</td><td>2</td><td>MCU</td><td>RGB and System interface mode selection pin.
<table><tr><th>RCM1, RCM0</th><th>MCU and RGB Interface Mode Select</th></tr><tr><td>0x</td><td>System Interface (1)</td></tr><tr><td>10</td><td>RGB Interface (1) (VS+HS+DE)</td></tr><tr><td>11</td><td>RGB Interface (2) (VS+HS)</td></tr></table>As internal RCM[1:0] bits are written, the external pin RCM[1:0] control is invalid, and RGB and System interface mode selection is controlled by internal RCM[1:0] bits.
If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>SRGB</td><td>I</td><td>1</td><td>MCU</td><td>RGB direction select H/W pin for Color filter default setting.
<table><tr><th>SRGB</th><th>RGB Filter Order for Color Filter Default Setting</th></tr><tr><td>0</td><td>S1, S2, S3 filter order =’B’, ‘G’, ‘R’</td></tr><tr><td>1</td><td>S1, S2, S3 filter order =’R’, ‘G’, ‘B’</td></tr></table>As internal BGR bit ise written, the external pin SRGB control is invalid, and RGB filter order is controlled by internal BGR bit.
If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>SMX</td><td>I</td><td>1</td><td>MCU</td><td>Module source output direction H/W select pin.
<table><tr><th>SMX</th><th>Module Source Output Direction</th></tr><tr><td>0</td><td>S528 -> S1</td></tr><tr><td>1</td><td>S1 -> S528</td></tr></table>If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>SMY</td><td>I</td><td>1</td><td>MCU</td><td>Module Gate output direction H/W select pin.
<table><tr><th>SMY</th><th>Module Gate Output Direction</th></tr><tr><td>0</td><td>G1 -> G220</td></tr><tr><td>1</td><td>G220 -> G1</td></tr></table>If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>IDM</td><td>I</td><td>1</td><td>MCU</td><td>Normal mode and Idle mode control pin in RGB I/F.
<table><tr><th>IDM</th><th>Idle Mode H/W Controller</th></tr><tr><td>0</td><td>Normal display (can be changed to Idle mode by S/W)</td></tr><tr><td>1</td><td>Into Idle mode</td></tr></table>As internal IDMON commands are written in RGB interface, the external pin IDM control is invalid, and normal and idle mode selection is controlled by internal IDMON commands.
If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>SHUT</td><td>I</td><td>1</td><td>MCU</td><td>Chip On/ Off H/W control pin in RGB I/F.
<table><tr><th>SHUNT</th><th>Display On/Off in RGB I/F</th></tr><tr><td>0</td><td>Display On</td></tr><tr><td>1</td><td>Display Off</td></tr></table>As internal CSHUT commands be written in RGB interface, the external pin SHUT control is invalid, and chip on/off selection is controlled by internal CSHUT commands.
If not used, please fix this pin to IOVCC or GND.</td></tr>
</table>

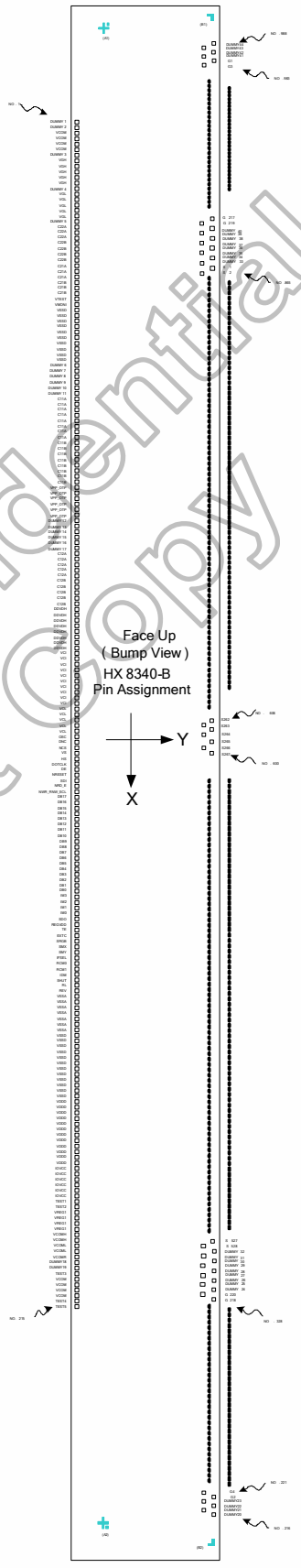
<table>
<tr><th colspan="5">Mode Select Pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>RL</td><td>I</td><td>1</td><td>MCU</td><td>Source output direction H/W select pin in RGB I/F.
<table><tr><th>RL</th><th>Module Source Output Direction</th></tr><tr><td>0</td><td>Normal Direction</td></tr><tr><td>1</td><td>Reverse Direction</td></tr></table>As internal CRL bit be written in RGB interface, the external pin RL control is invalid, and CRL is operated based on external pin SMX setting.
If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>TB</td><td>I</td><td>1</td><td>MCU</td><td>Gate output direction H/W select pin in RGB I/F.
<table><tr><th>TB</th><th>Module Gate Output Direction</th></tr><tr><td>0</td><td>Normal Direction</td></tr><tr><td>1</td><td>Reverse Direction</td></tr></table>As internal CTB bit be written in RGB interface, the external pin TB control is invalid, and CRL is operated based on external pin SMY setting.
If not used, please fix this pin to IOVCC or GND.</td></tr>
<tr><td>REV</td><td>I</td><td>1</td><td>MCU</td><td>Source output data polarity select H/W pin.
<table><tr><th>REV</th><th>Source Output Data Polarity</th></tr><tr><td>0</td><td>Data not reverse</td></tr><tr><td>1</td><td>Data reverse</td></tr></table>As internal INVON commands are written, the external pin REV control is invalid, and INVON commands are operated based on internal NB bit setting.
If not used, please fix this pin to IOVCC or GND.</td></tr>
</table>

Driver Output Pins				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S528	O	528	LCD	Source driver output pins.
G1~G220	O	220	LCD	Gate driver output pins.
IOVCC	P	1	Power Supply	Digital IO Pad power supply. IOVCC = 1.65 ~ 3.3V
VCI	P	1	Power Supply	Analog power supply. VCI = 2.5 ~ 3.3V
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VPP_OTP	P	1	Power supply	Power supply pin used in OTP program mode and operates at 6.5V ± 0.2. If not in OTP program mode, please let it open.
C11A,C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation (DDVDH). Leave this pin open if the internal step-up circuit is not used.
C12A,C12B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation (VCL). Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 2 operations (VGH, VGL). Leave this pin open if the internal step-up circuit is not used.
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
VREG1	O	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
VCOMH	O	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	O	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCOMR	I	1	Resistor or open	A VCOMH reference voltage input. When adjusting VCOMH externally, set registers to halt the VCOMH internal adjusting circuit and connect a variable resistor between VREG1 and GND for VCOMH adjusting.
VCL	O	1	Stabilizing capacitor	A negative voltage of VCI x (-1) output for VCOML circuit.
DDVDH	O	1	Stabilizing capacitor	A power output from the step-up circuit1. Connect to a stabilizing capacitor between GND and DDVDH. DDVDH =5.1V (typ.) when VCI = 2.8V.
VGH	O	1	Stabilizing capacitor	A positive power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT3-0 bits. Connect to a stabilizing capacitor between GND and VGH. VGH=max 15.3V
VGL	O	1	Stabilizing capacitor	A negative power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT(3-0) bits. Connect to a stabilizing capacitor between GND and VGL. VGL=min -13.5V

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
OSC	I	1	External Clock / Open	External oscillator clock input with internal pull-low circuit. That input is valid in test mode enable. Left it opens in normal operation mode.
TEST5-1	I	5	GND	Test pin input (Internal pull low)
REGVDD	I	1	Open	Test pin. Left it opens in normal operation mode.
VMONI	O	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must be left open.
DUMMY1-44	-	32	Open	Dummy pads, Dummy 18 and Dummy 19 are connection pins which can be contact resistance measurement pins.

4.2 Pin Assignment

Chip Size: 13880 um x 700 um
(Including Seal-ring 20 um *2,
Scribe line 40 um *2)
Chip Thickness: 300 um (typ.)
Pad Location: Pad center
Coordinate Origin: Chip center
Au Bump Size:
1. 40 um x 56 um
Input/Output
(No. 1~ No. 215)
2. 18 um x 100 um
Staggered LCD output side
(No. 216 ~ No. 988)



4.3 Pad Coordinates

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY1	-6695	-257	61	C11B	-3095	-257	121	NWR/SCL	505	-257	181	VDDD	4655	-257
2	DUMMY2	-6635	-257	62	C11B	-3035	-257	122	DB17	565	-257	182	VDDD	4715	-257
3	VCOM	-6575	-257	63	C11B	-2975	-257	123	DB16	650	-257	183	VDDD	4775	-257
4	VCOM	-6515	-257	64	C11B	-2915	-257	124	DB15	735	-257	184	VDDD	4835	-257
5	VCOM	-6455	-257	65	C11B	-2855	-257	125	DB14	820	-257	185	VDDD	4895	-257
6	VCOM	-6395	-257	66	VPP_OTP	-2795	-257	126	DB13	905	-257	186	VDDD	4955	-257
7	DUMMY3	-6335	-257	67	VPP_OTP	-2735	-257	127	DB12	990	-257	187	VDDD	5015	-257
8	VGH	-6275	-257	68	VPP_OTP	-2675	-257	128	DB11	1075	-257	188	VDDD	5075	-257
9	VGH	-6215	-257	69	VPP_OTP	-2615	-257	129	DB10	1160	-257	189	VDDD	5135	-257
10	VGH	-6155	-257	70	VPP_OTP	-2555	-257	130	DB9	1245	-257	190	IOVCC	5195	-257
11	VGH	-6095	-257	71	VPP_OTP	-2495	-257	131	DB8	1330	-257	191	IOVCC	5255	-257
12	VGH	-6035	-257	72	DUMMY12	-2435	-257	132	DB7	1415	-257	192	IOVCC	5315	-257
13	DUMMY4	-5975	-257	73	DUMMY13	-2375	-257	133	DB6	1500	-257	193	IOVCC	5375	-257
14	VGL	-5915	-257	74	DUMMY14	-2315	-257	134	DB5	1585	-257	194	IOVCC	5435	-257
15	VGL	-5855	-257	75	DUMMY15	-2255	-257	135	DB4	1670	-257	195	IOVCC	5495	-257
16	VGL	-5795	-257	76	DUMMY16	-2195	-257	136	DB3	1755	-257	196	TEST1	5555	-257
17	VGL	-5735	-257	77	DUMMY17	-2135	-257	137	DB2	1840	-257	197	TEST2	5615	-257
18	VGL	-5675	-257	78	C12A	-2075	-257	138	DB1	1925	-257	198	VREG1	5675	-257
19	DUMMY5	-5615	-257	79	C12A	-2015	-257	139	DB0	2010	-257	199	VREG1	5735	-257
20	C22A	-5555	-257	80	C12A	-1955	-257	140	IM3	2095	-257	200	VREG1	5795	-257
21	C22A	-5495	-257	81	C12A	-1895	-257	141	IM2	2155	-257	201	VREG1	5855	-257
22	C22A	-5435	-257	82	C12A	-1835	-257	142	IM1	2215	-257	202	VCOMH	5915	-257
23	C22B	-5375	-257	83	C12B	-1775	-257	143	IM0	2275	-257	203	VCOMH	5975	-257
24	C22B	-5315	-257	84	C12B	-1715	-257	144	SDO	2335	-257	204	VCOML	6035	-257
25	C22B	-5255	-257	85	C12B	-1655	-257	145	REGVDD	2420	-257	205	VCOML	6095	-257
26	C21A	-5195	-257	86	C12B	-1595	-257	146	TE	2505	-257	206	VCOMR	6155	-257
27	C21A	-5135	-257	87	C12B	-1535	-257	147	EXTC	2590	-257	207	Dummy18	6215	-257
28	C21A	-5075	-257	88	DDVDH	-1475	-257	148	SRGB	2675	-257	208	Dummy19	6275	-257
29	C21B	-5015	-257	89	DDVDH	-1415	-257	149	SMX	2735	-257	209	TEST3	6335	-257
30	C21B	-4955	-257	90	DDVDH	-1355	-257	150	SMY	2795	-257	210	VCOM	6395	-257
31	C21B	-4895	-257	91	DDVDH	-1295	-257	151	IFSEL	2855	-257	211	VCOM	6455	-257
32	VTEST	-4835	-257	92	DDVDH	-1235	-257	152	RCM0	2915	-257	212	VCOM	6515	-257
33	VMONI	-4775	-257	93	DDVDH	-1175	-257	153	RCM1	2975	-257	213	VCOM	6575	-257
34	VSSD	-4715	-257	94	DDVDH	-1115	-257	154	IDM	3035	-257	214	TEST4	6635	-257
35	VSSD	-4655	-257	95	DDVDH	-1055	-257	155	SHUT	3095	-257	215	TEST5	6695	-257
36	VSSD	-4595	-257	96	VCI	-995	-257	156	RL	3155	-257	216	Dummy20	6772	236
37	VSSD	-4535	-257	97	VCI	-935	-257	157	TB	3215	-257	217	Dummy21	6756	116
38	VSSD	-4475	-257	98	VCI	-875	-257	158	REV	3275	-257	218	Dummy22	6740	236
39	VSSD	-4415	-257	99	VCI	-815	-257	159	VSSA	3335	-257	219	Dummy23	6724	116
40	VSSD	-4355	-257	100	VCI	-755	-257	160	VSSA	3395	-257	220	G2	6708	236
41	VSSD	-4295	-257	101	VCI	-695	-257	161	VSSA	3455	-257	221	G4	6692	116
42	VSSD	-4235	-257	102	VCI	-635	-257	162	VSSA	3515	-257	222	G6	6676	236
43	VSSD	-4175	-257	103	VCI	-575	-257	163	VSSA	3575	-257	223	G8	6660	116
44	DUMMY6	-4115	-257	104	VCI	-515	-257	164	VSSA	3635	-257	224	G10	6644	236
45	DUMMY7	-4055	-257	105	VCI	-455	-257	165	VSSA	3695	-257	225	G12	6628	116
46	DUMMY8	-3995	-257	106	VCL	-395	-257	166	VSSD	3755	-257	226	G14	6612	236
47	DUMMY9	-3935	-257	107	VCL	-335	-257	167	VSSD	3815	-257	227	G16	6596	116
48	DUMMY10	-3875	-257	108	VCL	-275	-257	168	VSSD	3875	-257	228	G18	6580	236
49	DUMMY11	-3815	-257	109	VCL	-215	-257	169	VSSD	3935	-257	229	G20	6564	116
50	C11A	-3755	-257	110	VCL	-155	-257	170	VSSD	3995	-257	230	G22	6548	236
51	C11A	-3695	-257	111	OSC	-95	-257	171	VSSD	4055	-257	231	G24	6532	116
52	C11A	-3635	-257	112	DNC	-35	-257	172	VSSD	4115	-257	232	G26	6516	236
53	C11A	-3575	-257	113	NCS	25	-257	173	VSSD	4175	-257	233	G28	6500	116
54	C11A	-3515	-257	114	VS	85	-257	174	VSSD	4235	-257	234	G30	6484	236
55	C11A	-3455	-257	115	HS	145	-257	175	VSSD	4295	-257	235	G32	6468	116
56	C11A	-3395	-257	116	DOTCLK	205	-257	176	VSSD	4355	-257	236	G34	6452	236
57	C11A	-3335	-257	117	DE	265	-257	177	VSSD	4415	-257	237	G36	6436	116
58	C11B	-3275	-257	118	NRESET	325	-257	178	VDDD	4475	-257	238	G38	6420	236
59	C11B	-3215	-257	119	SDI	385	-257	179	VDDD	4535	-257	239	G40	6404	116
60	C11B	-3155	-257	120	NRD	445	-257	180	VDDD	4595	-257	240	G42	6388	236

No.	Pad name	X	Y
241	G44	6372	116
242	G46	6356	236
243	G48	6340	116
244	G50	6324	236
245	G52	6308	116
246	G54	6292	236
247	G56	6276	116
248	G58	6260	236
249	G60	6244	116
250	G62	6228	236
251	G64	6212	116
252	G66	6196	236
253	G68	6180	116
254	G70	6164	236
255	G72	6148	116
256	G74	6132	236
257	G76	6116	116
258	G78	6100	236
259	G80	6084	116
260	G82	6068	236
261	G84	6052	116
262	G86	6036	236
263	G88	6020	116
264	G90	6004	236
265	G92	5988	116
266	G94	5972	236
267	G96	5956	116
268	G98	5940	236
269	G100	5924	116
270	G102	5908	236
271	G104	5892	116
272	G106	5876	236
273	G108	5860	116
274	G110	5844	236
275	G112	5828	116
276	G114	5812	236
277	G116	5796	116
278	G118	5780	236
279	G120	5764	116
280	G122	5748	236
281	G124	5732	116
282	G126	5716	236
283	G128	5700	116
284	G130	5684	236
285	G132	5668	116
286	G134	5652	236
287	G136	5636	116
288	G138	5620	236
289	G140	5604	116
290	G142	5588	236
291	G144	5572	116
292	G146	5556	236
293	G148	5540	116
294	G150	5524	236
295	G152	5508	116
296	G154	5492	236
297	G156	5476	116
298	G158	5460	236
299	G160	5444	116
300	G162	5428	236

No.	Pad name	X	Y
301	G164	5412	116
302	G166	5396	236
303	G168	5380	116
304	G170	5364	236
305	G172	5348	116
306	G174	5332	236
307	G176	5316	116
308	G178	5300	236
309	G180	5284	116
310	G182	5268	236
311	G184	5252	116
312	G186	5236	236
313	G188	5220	116
314	G190	5204	236
315	G192	5188	116
316	G194	5172	236
317	G196	5156	116
318	G198	5140	236
319	G200	5124	116
320	G202	5108	236
321	G204	5092	116
322	G206	5076	236
323	G208	5060	116
324	G210	5044	236
325	G212	5028	116
326	G214	5012	236
327	G216	4996	116
328	G218	4980	236
329	G220	4964	116
330	Dummy24	4948	236
331	Dummy25	4932	116
332	Dummy26	4916	236
333	Dummy27	4900	116
334	Dummy28	4884	236
335	Dummy29	4868	116
336	Dummy30	4852	236
337	Dummy31	4836	116
338	Dummy32	4820	236
339	S528	4804	116
340	S527	4788	236
341	S526	4772	116
342	S525	4756	236
343	S524	4740	116
344	S523	4724	236
345	S522	4708	116
346	S521	4692	236
347	S520	4676	116
348	S519	4660	236
349	S518	4644	116
350	S517	4628	236
351	S516	4612	116
352	S515	4596	236
353	S514	4580	116
354	S513	4564	236
355	S512	4548	116
356	S511	4532	236
357	S510	4516	116
358	S509	4500	236
359	S508	4484	116
360	S507	4468	236

No.	Pad name	X	Y
361	S506	4452	116
362	S505	4436	236
363	S504	4420	116
364	S503	4404	236
365	S502	4388	116
366	S501	4372	236
367	S500	4356	116
368	S499	4340	236
369	S498	4324	116
370	S497	4308	236
371	S496	4292	116
372	S495	4276	236
373	S494	4260	116
374	S493	4244	236
375	S492	4228	116
376	S491	4212	236
377	S490	4196	116
378	S489	4180	236
379	S488	4164	116
380	S487	4148	236
381	S486	4132	116
382	S485	4116	236
383	S484	4100	116
384	S483	4084	236
385	S482	4068	116
386	S481	4052	236
387	S480	4036	116
388	S479	4020	236
389	S478	4004	116
390	S477	3988	236
391	S476	3972	116
392	S475	3956	236
393	S474	3940	116
394	S473	3924	236
395	S472	3908	116
396	S471	3892	236
397	S470	3876	116
398	S469	3860	236
399	S468	3844	116
400	S467	3828	236
401	S466	3812	116
402	S465	3796	236
403	S464	3780	116
404	S463	3764	236
405	S462	3748	116
406	S461	3732	236
407	S460	3716	116
408	S459	3700	236
409	S458	3684	116
410	S457	3668	236
411	S456	3652	116
412	S455	3636	236
413	S454	3620	116
414	S453	3604	236
415	S452	3588	116
416	S451	3572	236
417	S450	3556	116
418	S449	3540	236
419	S448	3524	116
420	S447	3508	236

No.	Pad name	X	Y
421	S446	3492	116
422	S445	3476	236
423	S444	3460	116
424	S443	3444	236
425	S442	3428	116
426	S441	3412	236
427	S440	3396	116
428	S439	3380	236
429	S438	3364	116
430	S437	3348	236
431	S436	3332	116
432	S435	3316	236
433	S434	3300	116
434	S433	3284	236
435	S432	3268	116
436	S431	3252	236
437	S430	3236	116
438	S429	3220	236
439	S428	3204	116
440	S427	3188	236
441	S426	3172	116
442	S425	3156	236
443	S424	3140	116
444	S423	3124	236
445	S422	3108	116
446	S421	3092	236
447	S420	3076	116
448	S419	3060	236
449	S418	3044	116
450	S417	3028	236
451	S416	3012	116
452	S415	2996	236
453	S414	2980	116
454	S413	2964	236
455	S412	2948	116
456	S411	2932	236
457	S410	2916	116
458	S409	2900	236
459	S408	2884	116
460	S407	2868	236
461	S406	2852	116
462	S405	2836	236
463	S404	2820	116
464	S403	2804	236
465	S402	2788	116
466	S401	2772	236
467	S400	2756	116
468	S399	2740	236
469	S398	2724	116
470	S397	2708	236
471	S396	2642	116
472	S395	2626	236
473	S394	2610	116
474	S393	2594	236
475	S392	2578	116
476	S391	2562	236
477	S390	2546	116
478	S389	2530	236
479	S388	2514	116
480	S387	2498	236

No.	Pad name	X	Y
481	S386	2482	116
482	S385	2466	236
483	S384	2450	116
484	S383	2434	236
485	S382	2418	116
486	S381	2402	236
487	S380	2386	116
488	S379	2370	236
489	S378	2354	116
490	S377	2338	236
491	S376	2322	116
492	S375	2306	236
493	S374	2290	116
494	S373	2274	236
495	S372	2258	116
496	S371	2242	236
497	S370	2226	116
498	S369	2210	236
499	S368	2194	116
500	S367	2178	236
501	S366	2162	116
502	S365	2146	236
503	S364	2130	116
504	S363	2114	236
505	S362	2098	116
506	S361	2082	236
507	S360	2066	116
508	S359	2050	236
509	S358	2034	116
510	S357	2018	236
511	S356	2002	116
512	S355	1986	236
513	S354	1970	116
514	S353	1954	236
515	S352	1938	116
516	S351	1922	236
517	S350	1906	116
518	S349	1890	236
519	S348	1874	116
520	S347	1858	236
521	S346	1842	116
522	S345	1826	236
523	S344	1810	116
524	S343	1794	236
525	S342	1778	116
526	S341	1762	236
527	S340	1746	116
528	S339	1730	236
529	S338	1714	116
530	S337	1698	236
531	S336	1682	116
532	S335	1666	236
533	S334	1650	116
534	S333	1634	236
535	S332	1618	116
536	S331	1602	236
537	S330	1586	116
538	S329	1570	236
539	S328	1554	116
540	S327	1538	236

No.	Pad name	X	Y
541	S326	1522	116
542	S325	1506	236
543	S324	1490	116
544	S323	1474	236
545	S322	1458	116
546	S321	1442	236
547	S320	1426	116
548	S319	1410	236
549	S318	1394	116
550	S317	1378	236
551	S316	1362	116
552	S315	1346	236
553	S314	1330	116
554	S313	1314	236
555	S312	1298	116
556	S311	1282	236
557	S310	1266	116
558	S309	1250	236
559	S308	1234	116
560	S307	1218	236
561	S306	1202	116
562	S305	1186	236
563	S304	1170	116
564	S303	1154	236
565	S302	1138	116
566	S301	1122	236
567	S300	1106	116
568	S299	1090	236
569	S298	1074	116
570	S297	1058	236
571	S296	1042	116
572	S295	1026	236
573	S294	1010	116
574	S293	994	236
575	S292	978	116
576	S291	962	236
577	S290	946	116
578	S289	930	236
579	S288	914	116
580	S287	898	236
581	S286	882	116
582	S285	866	236
583	S284	850	116
584	S283	834	236
585	S282	818	116
586	S281	802	236
587	S280	786	116
588	S279	770	236
589	S278	754	116
590	S277	738	236
591	S276	722	116
592	S275	706	236
593	S274	690	116
594	S273	674	236
595	S272	658	116
596	S271	642	236
597	S270	626	116
598	S269	610	236
599	S268	594	116
600	S267	578	236

No.	Pad name	X	Y
601	S266	562	116
602	S265	546	236
603	S264	-554	116
604	S263	-570	236
605	S262	-586	116
606	S261	-602	236
607	S260	-618	116
608	S259	-634	236
609	S258	-650	116
610	S257	-666	236
611	S256	-682	116
612	S255	-698	236
613	S254	-714	116
614	S253	-730	236
615	S252	-746	116
616	S251	-762	236
617	S250	-778	116
618	S249	-794	236
619	S248	-810	116
620	S247	-826	236
621	S246	-842	116
622	S245	-858	236
623	S244	-874	116
624	S243	-890	236
625	S242	-906	116
626	S241	-922	236
627	S240	-938	116
628	S239	-954	236
629	S238	-970	116
630	S237	-986	236
631	S236	-1002	116
632	S235	-1018	236
633	S234	-1034	116
634	S233	-1050	236
635	S232	-1066	116
636	S231	-1082	236
637	S230	-1098	116
638	S229	-1114	236
639	S228	-1130	116
640	S227	-1146	236
641	S226	-1162	116
642	S225	-1178	236
643	S224	-1194	116
644	S223	-1210	236
645	S222	-1226	116
646	S221	-1242	236
647	S220	-1258	116
648	S219	-1274	236
649	S218	-1290	116
650	S217	-1306	236
651	S216	-1322	116
652	S215	-1338	236
653	S214	-1354	116
654	S213	-1370	236
655	S212	-1386	116
656	S211	-1402	236
657	S210	-1418	116
658	S209	-1434	236
659	S208	-1450	116
660	S207	-1466	236

No.	Pad name	X	Y
661	S206	-1482	116
662	S205	-1498	236
663	S204	-1514	116
664	S203	-1530	236
665	S202	-1546	116
666	S201	-1562	236
667	S200	-1578	116
668	S199	-1594	236
669	S198	-1610	116
670	S197	-1626	236
671	S196	-1642	116
672	S195	-1658	236
673	S194	-1674	116
674	S193	-1690	236
675	S192	-1706	116
676	S191	-1722	236
677	S190	-1738	116
678	S189	-1754	236
679	S188	-1770	116
680	S187	-1786	236
681	S186	-1802	116
682	S185	-1818	236
683	S184	-1834	116
684	S183	-1850	236
685	S182	-1866	116
686	S181	-1882	236
687	S180	-1898	116
688	S179	-1914	236
689	S178	-1930	116
690	S177	-1946	236
691	S176	-1962	116
692	S175	-1978	236
693	S174	-1994	116
694	S173	-2010	236
695	S172	-2026	116
696	S171	-2042	236
697	S170	-2058	116
698	S169	-2074	236
699	S168	-2090	116
700	S167	-2106	236
701	S166	-2122	116
702	S165	-2138	236
703	S164	-2154	116
704	S163	-2170	236
705	S162	-2186	116
706	S161	-2202	236
707	S160	-2218	116
708	S159	-2234	236
709	S158	-2250	116
710	S157	-2266	236
711	S156	-2282	116
712	S155	-2298	236
713	S154	-2314	116
714	S153	-2330	236
715	S152	-2346	116
716	S151	-2362	236
717	S150	-2378	116
718	S149	-2394	236
719	S148	-2410	116
720	S147	-2426	236

No.	Pad name	X	Y
721	S146	-2442	116
722	S145	-2458	236
723	S144	-2474	116
724	S143	-2490	236
725	S142	-2506	116
726	S141	-2522	236
727	S140	-2538	116
728	S139	-2554	236
729	S138	-2570	116
730	S137	-2586	236
731	S136	-2602	116
732	S135	-2618	236
733	S134	-2634	116
734	S133	-2650	236
735	S132	-2716	116
736	S116	-2732	236
737	S130	-2748	116
738	S129	-2764	236
739	S128	-2780	116
740	S127	-2796	236
741	S126	-2812	116
742	S125	-2828	236
743	S124	-2844	116
744	S123	-2860	236
745	S122	-2876	116
746	S121	-2892	236
747	S120	-2908	116
748	S119	-2924	236
749	S118	-2940	116
750	S117	-2956	236
751	S116	-2972	116
752	S115	-2988	236
753	S114	-3004	116
754	S113	-3020	236
755	S112	-3036	116
756	S111	-3052	236
757	S110	-3068	116
758	S109	-3084	236
759	S108	-3100	116
760	S107	-3116	236
761	S106	-3132	116
762	S105	-3148	236
763	S104	-3164	116
764	S103	-3180	236
765	S102	-3196	116
766	S101	-3212	236
767	S100	-3228	116
768	S99	-3244	236
769	S98	-3260	116
770	S97	-3276	236
771	S96	-3292	116
772	S95	-3308	236
773	S94	-3324	116
774	S93	-3340	236
775	S92	-3356	116
776	S91	-3372	236
777	S90	-3388	116
778	S89	-3404	236
779	S88	-3420	116
780	S87	-3436	236

No.	Pad name	X	Y
781	S86	-3452	116
782	S85	-3468	236
783	S84	-3484	116
784	S83	-3500	236
785	S82	-3516	116
786	S81	-3532	236
787	S80	-3548	116
788	S79	-3564	236
789	S78	-3580	116
790	S77	-3596	236
791	S76	-3612	116
792	S75	-3628	236
793	S74	-3644	116
794	S73	-3660	236
795	S72	-3676	116
796	S71	-3692	236
797	S70	-3708	116
798	S69	-3724	236
799	S68	-3740	116
800	S67	-3756	236
801	S66	-3772	116
802	S65	-3788	236
803	S64	-3804	116
804	S63	-3820	236
805	S62	-3836	116
806	S61	-3852	236
807	S60	-3868	116
808	S59	-3884	236
809	S58	-3900	116
810	S57	-3916	236
811	S56	-3932	116
812	S55	-3948	236
813	S54	-3964	116
814	S53	-3980	236
815	S52	-3996	116
816	S51	-4012	236
817	S50	-4028	116
818	S49	-4044	236
819	S48	-4060	116
820	S47	-4076	236
821	S46	-4092	116
822	S45	-4108	236
823	S44	-4124	116
824	S43	-4140	236
825	S42	-4156	116
826	S41	-4172	236
827	S40	-4188	116
828	S39	-4204	236
829	S38	-4220	116
830	S37	-4236	236
831	S36	-4252	116
832	S35	-4268	236
833	S34	-4284	116
834	S33	-4300	236
835	S32	-4316	116
836	S31	-4332	236
837	S30	-4348	116
838	S29	-4364	236
839	S28	-4380	116
840	S27	-4396	236

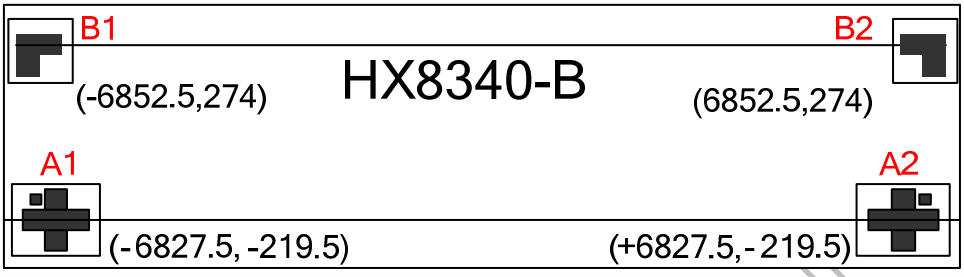
No.	Pad name	X	Y
841	S26	-4412	116
842	S25	-4428	236
843	S24	-4444	116
844	S23	-4460	236
845	S22	-4476	116
846	S21	-4492	236
847	S20	-4508	116
848	S19	-4524	236
849	S18	-4540	116
850	S17	-4556	236
851	S16	-4572	116
852	S15	-4588	236
853	S14	-4604	116
854	S13	-4620	236
855	S12	-4636	116
856	S11	-4652	236
857	S10	-4668	116
858	S9	-4684	236
859	S8	-4700	116
860	S7	-4716	236
861	S6	-4732	116
862	S5	-4748	236
863	S4	-4764	116
864	S3	-4780	236
865	S2	-4796	116
866	S1	-4812	236
867	Dummy33	-4828	116
868	Dummy34	-4844	236
869	Dummy35	-4860	116
870	Dummy36	-4876	236
871	Dummy37	-4892	116
872	Dummy38	-4908	236
873	Dummy39	-4924	116
874	Dummy40	-4940	236
875	G219	-4956	116
876	G217	-4972	236
877	G215	-4988	116
878	G213	-5004	236
879	G211	-5020	116
880	G209	-5036	236
881	G207	-5052	116
882	G205	-5068	236
883	G203	-5084	116
884	G201	-5100	236
885	G199	-5116	116
886	G197	-5132	236
887	G195	-5148	116
888	G193	-5164	236
889	G191	-5180	116
890	G189	-5196	236
891	G187	-5212	116
892	G185	-5228	236
893	G183	-5244	116
894	G181	-5260	236
895	G179	-5276	116
896	G177	-5292	236
897	G175	-5308	116
898	G173	-5324	236
899	G171	-5340	116
900	G169	-5356	236

No.	Pad name	X	Y
901	G167	-5372	116
902	G165	-5388	236
903	G163	-5404	116
904	G161	-5420	236
905	G159	-5436	116
906	G157	-5452	236
907	G155	-5468	116
908	G153	-5484	236
909	G151	-5500	116
910	G149	-5516	236
911	G147	-5532	116
912	G145	-5548	236
913	G143	-5564	116
914	G141	-5580	236
915	G139	-5596	116
916	G137	-5612	236
917	G135	-5628	116
918	G133	-5644	236
919	G116	-5660	116
920	G129	-5676	236
921	G127	-5692	116
922	G125	-5708	236
923	G123	-5724	116
924	G121	-5740	236
925	G119	-5756	116
926	G117	-5772	236
927	G115	-5788	116
928	G113	-5804	236
929	G111	-5820	116
930	G109	-5836	236
931	G107	-5852	116
932	G105	-5868	236
933	G103	-5884	116
934	G101	-5900	236
935	G99	-5916	116
936	G97	-5932	236
937	G95	-5948	116
938	G93	-5964	236
939	G91	-5980	116
940	G89	-5996	236
941	G87	-6012	116
942	G85	-6028	236
943	G83	-6044	116
944	G81	-6060	236
945	G79	-6076	116
946	G77	-6092	236
947	G75	-6108	116
948	G73	-6124	236
949	G71	-6140	116
950	G69	-6156	236
951	G67	-6172	116
952	G65	-6188	236
953	G63	-6204	116
954	G61	-6220	236
955	G59	-6236	116
956	G57	-6252	236
957	G55	-6268	116
958	G53	-6284	236
959	G51	-6300	116
960	G49	-6316	236

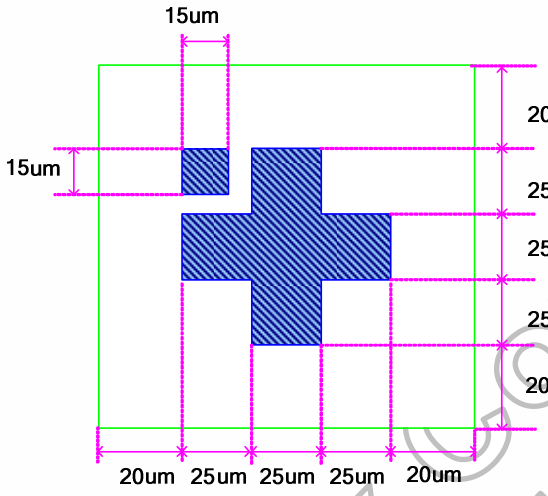
No.	Pad name	X	Y
961	G47	-6332	116
962	G45	-6348	236
963	G43	-6364	116
964	G41	-6380	236
965	G39	-6396	116
966	G37	-6412	236
967	G35	-6428	116
968	G33	-6444	236
969	G31	-6460	116
970	G29	-6476	236
971	G27	-6492	116
972	G25	-6508	236
973	G23	-6524	116
974	G21	-6540	236
975	G19	-6556	116
976	G17	-6572	236
977	G15	-6588	116
978	G13	-6604	236
979	G11	-6620	116
980	G9	-6636	236
981	G7	-6652	116
982	G5	-6668	236
983	G3	-6684	116
984	G1	-6700	236
985	Dummy41	-6716	116
986	Dummy42	-6732	236
987	Dummy43	-6748	116
988	Dummy44	-6764	236

Alignment Mark	X	Y
A1	-6827.5	-219.5
A2	+6827.5	-219.5
B1	-6852.5	274
B2	6852.5	274

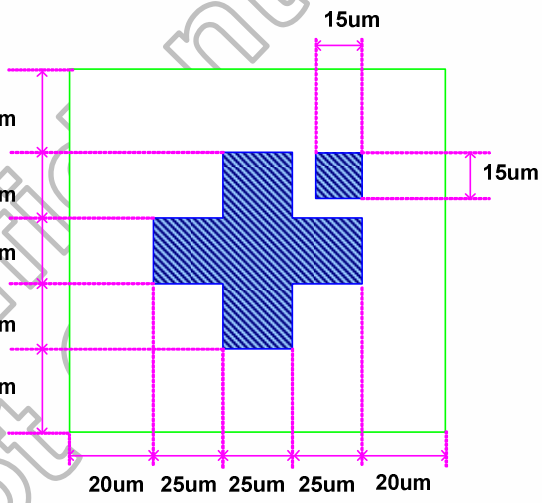
4.4 Alignment Mark



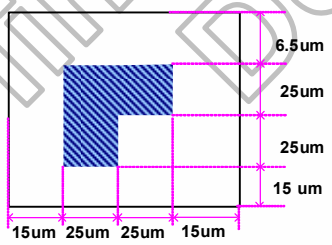
A_MARK (A1)



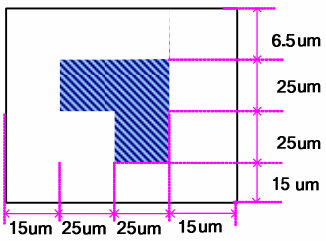
A_MARK (A2)



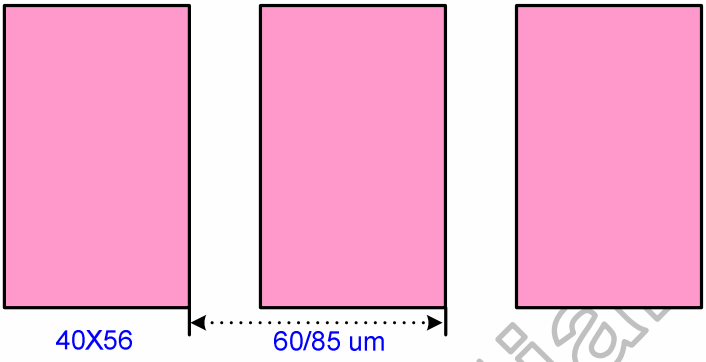
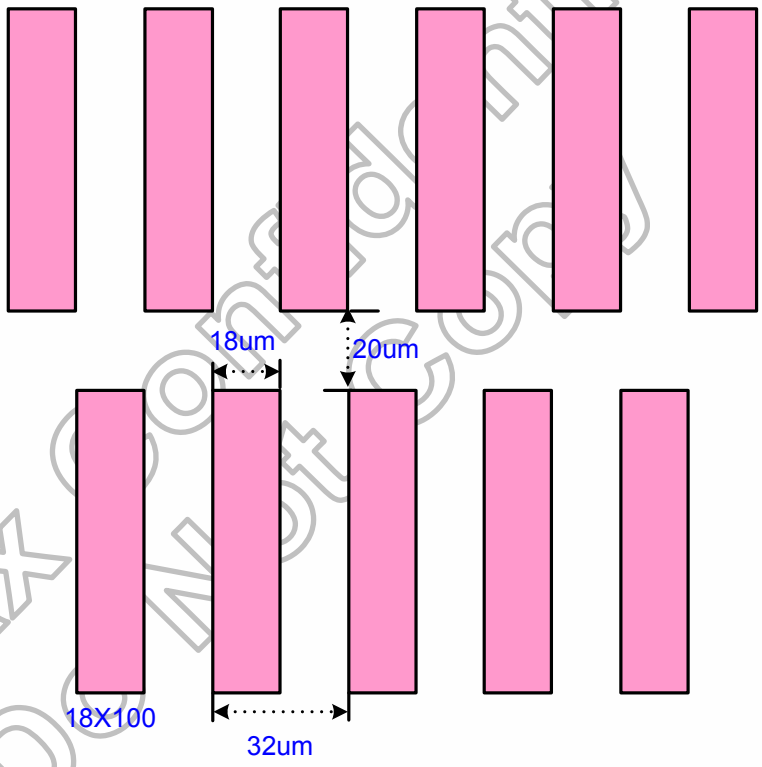
A_MARK (B1)



A_MARK (B2)



4.5 Bump Size

Input PAD	
Output PAD	

5. Interface

The HX8340-B supports two-type interface group: Command-Parameter interface mode, Register-Content interface mode.

This manual description focuses on Register-Content interface mode. About the Command-Parameter interface mode, please refer to the HX8340-B (N) datasheet for detail.

In Register-Content interface mode (IFSEL0='L'), the HX8340-B has a system interface circuit for command/parameter (include display data) transferring, and a RGB interface circuit for data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8340-B shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

5.1 System Interface Circuit

The register-content interface circuit in HX8340-B supports 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and a serial bus system interface for serial data input. When NCS = 'L', the parallel and serial bus system interface of the HX8340-B become active and data transfer through the interface circuit is available. The input bus width format of system interface circuit is selected by external pins IM3-0 setting. For selecting the input bus format, please refer to Table 5.1.

In register-content interface, it includes command code and the following parameter and GRAM data. The command code can be written through data bus by setting DNC ='0'. Then the parameter or GRAM data can be written to register at which that index pointer pointed by setting DNC='1'.

IM3	IM2	IM1	IM0	Interface	NRD_E	NWR_RNW_SCL	DNC	Data Bus use
0	0	0	0	6800 MCU 16-bits Parallel	E	RNW	DNC	DB0, DB9: Unused, DB17-B10, DB8-DB1: 16-bit data
0	0	0	1	6800 MCU 8-bits Parallel	E	RNW	DNC	DB9- DB0 Unused, DB17-DB10: 8-bits Data
0	0	1	0	8080 MCU 16-bits Parallel	NRD_E	NWR	DNC	DB0, DB9: Unused, DB17-10, DB8-DB1: 16-bit data
0	0	1	1	8080 MCU 8-bits Parallel	NRD_E	NWR	DNC	DB9- DB0: Unused, DB17-DB10: 8-bits Data
-	1	-	ID	Serial interface	Note(1)	SCL	Note(1)	SDI, SDO
1	0	0	0	6800 MCU 18-bits Parallel	E	RNW	DNC	DB17-DB0: 18-bits Data
1	0	0	1	6800 MCU 9-bits Parallel	E	RNW	DNC	DB8-DB0: Unused, DB17-DB9: 9-bits Data
1	0	1	0	8080 MCU 18-bits Parallel	NRD_E	NWR	DNC	DB17-DB0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel	NRD_E	NWR	DNC	DB8-DB0: Unused, DB17-DB9: 9-bits Data
Other Setting				Setting Invalid				

Note: (1) Can be connected to GND or IOVCC level.
(2) SDI and SDO can be tie together as SDA

Table 5. 1 Pin connection According to MCU Interface Type Selection

5.1.1 Parallel Bus System Interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface are listed in Table 5.2 and Table 5.3.

IM3	IM2	IM1	IM0	Interface	DNC	NRD_E	NWR_RNW_SCL	Function
0	0	1	0	16-bits Parallel	0	1	↑	Write 8-bits command (DB8 to DB1)
					1	1	↑	Write 8-bits parameter (DB8 to DB1)
					1	1	↑	Write 16-bits display data (DB17 to DB10, DB8 to DB1)
					1	↑	1	Read 8-bits command (DB8 to DB1)
					1	↑	1	Read 16-bits display data (DB17 to DB10, DB8 to DB1)
0	0	1	1	8-bits Parallel	0	1	↑	Write 8-bits command (DB17 to DB10)
					1	1	↑	Write 8-bits parameter (DB17 to DB10)
					1	1	↑	Write 8-bits display data (DB17 to DB10)
					1	↑	1	Read 8-bits parameter or status (DB17 to DB10)
					1	↑	1	Read 8-bits display data (DB17 to DB10)
1	0	1	0	18-bits Parallel	0	1	↑	Write 8-bits command (DB8 to DB1)
					1	1	↑	Write 8-bits parameter (DB8 to DB1)
					1	1	↑	Write 18-bits display data (DB17 to DB0)
					1	↑	1	Read 8-bits parameter or status (DB8 to DB1)
					1	↑	1	Read 18-bits display data (DB17 to DB0)
1	0	1	1	9-bits Parallel	0	1	↑	Write 8-bits command (DB17 to DB10)
					1	1	↑	Write 8-bits parameter (DB17 to DB10)
					1	1	↑	Write 9-bits display data (DB17 to DB9)
					1	↑	1	Read 8-bits command (DB17 to DB10)
					1	↑	1	Read 9-bits display data (DB17 to DB9)

Table 5. 2 Data Pin Function for I80 Series CPU

IM3	IM2	IM1	IM0	Interface	DNC	NWR_RNW_SCL	NRD_E	Function
0	0	0	0	16-bits Parallel	0	0	↓	Write 8-bits command (DB8 to DB1)
					1	0	↓	Write 8-bits parameter (DB8 to DB1)
					1	0	↓	Write 16-bits display data (DB17 to DB10, DB8 to DB1)
					1	1	↓	Read 8-bits command (DB8 to DB1)
					1	1	↓	Read 16-bits display data (DB17 to DB10, DB8 to DB1)
0	0	0	1	8-bits Parallel	0	0	↓	Write 8-bits command (DB17 to DB10)
					1	0	↓	Write 8-bits parameter (DB17 to DB10)
					1	0	↓	Write 8-bits display data (DB17 to DB10)
					1	1	↓	Read 8-bits parameter or status (DB17 to DB10)
					1	1	↓	Read 8-bits display data (DB17 to DB10)
1	0	0	0	18-bits Parallel	0	0	↓	Write 8-bits command (DB8 to DB1)
					1	0	↓	Write 8-bits parameter (DB8 to DB1)
					1	0	↓	Write 18-bits display data (DB17 to DB0)
					1	1	↓	Read 8-bits parameter or status (DB8 to DB1)
					1	1	↓	Read 18-bits display data (DB17 to DB0)
1	0	0	1	9-bits Parallel	0	0	↓	Write 8-bits command (DB17 to DB10)
					1	0	↓	Write 8-bits parameter (DB17 to DB10)
					1	0	↓	Write 9-bits display data (DB17 to DB9)
					1	1	↓	Read 8-bits command (DB17 to DB10)
					1	1	↓	Read 9-bits display data (DB17 to DB9)

Table 5. 3 Data Pin Function for M68 Series CPU

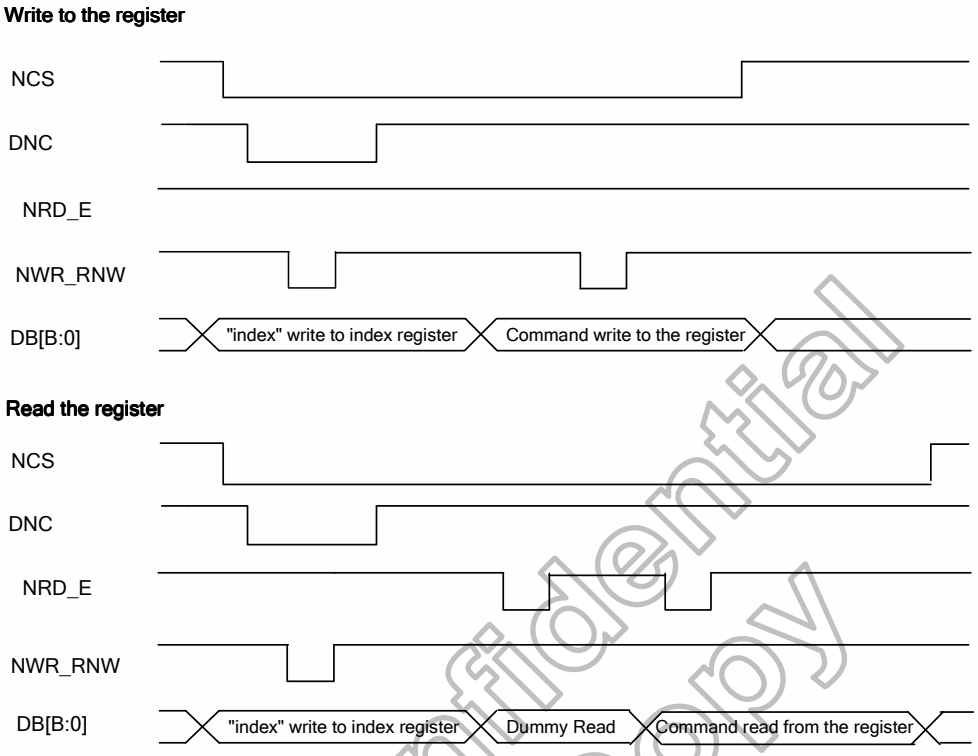


Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

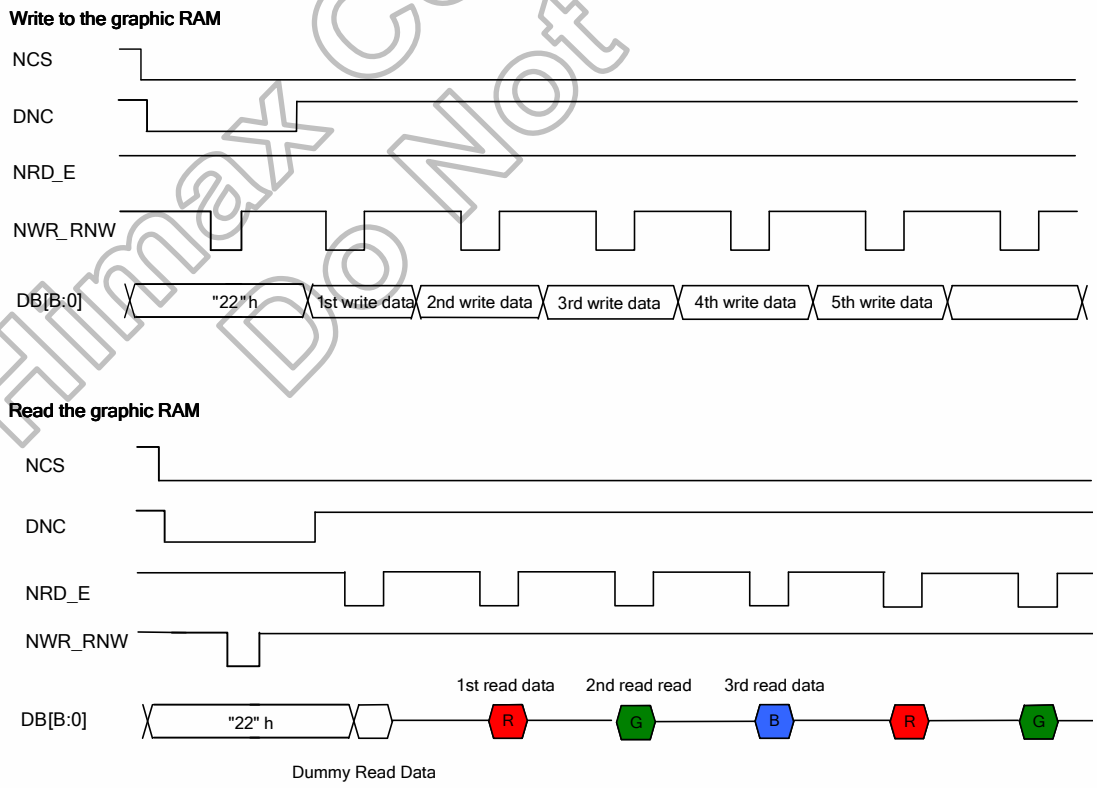


Figure 5. 2 GRAM Read/Write Timing in Bit Parallel Bus System Interface (for I80 Series MPU)

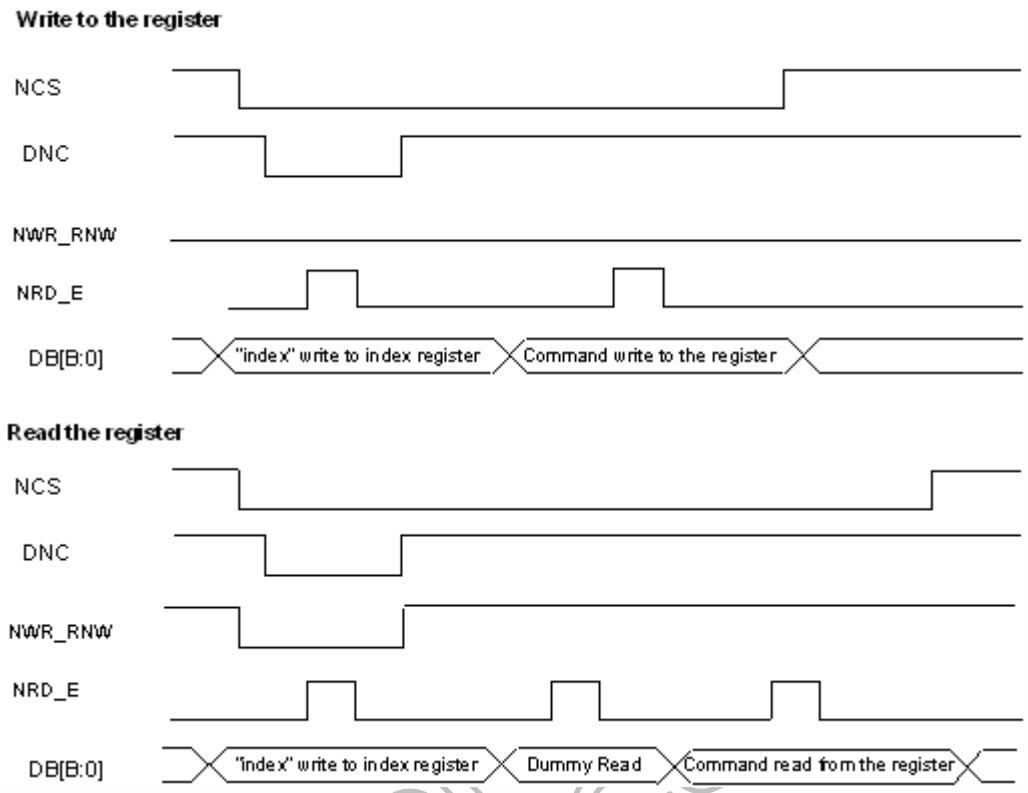


Figure 5. 3 Register Read/Write Timing in Parallel Bus System Interface (for M68 Series MPU)

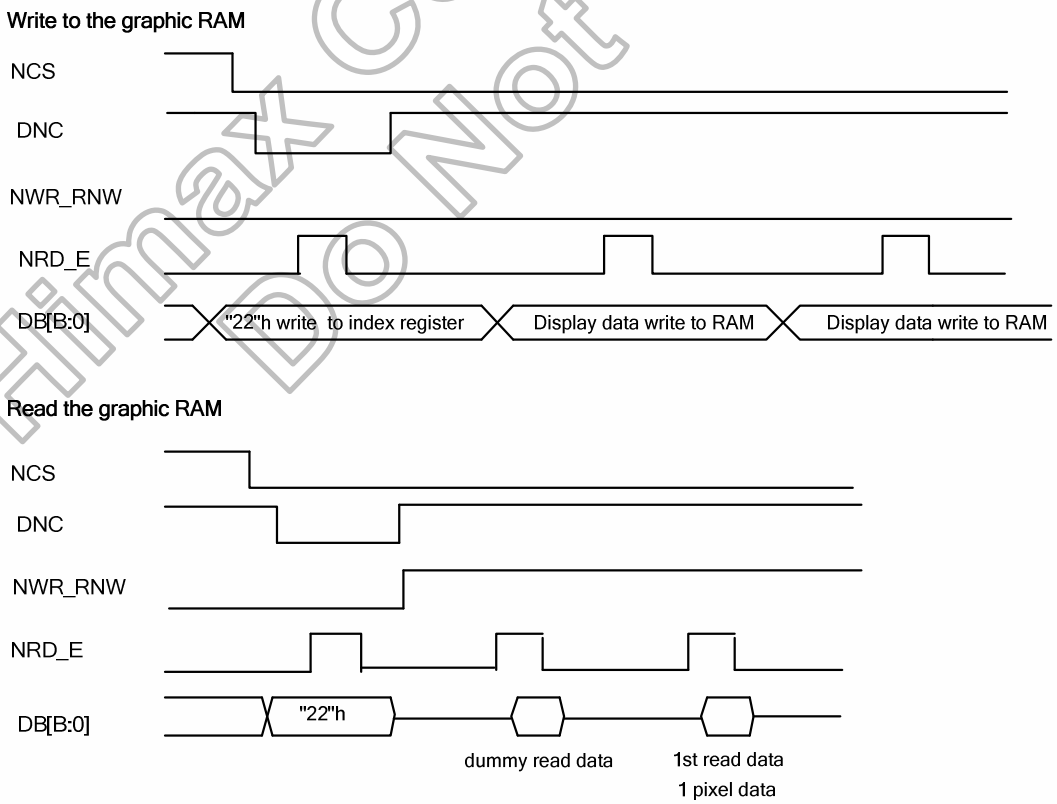


Figure 5. 4 GRAM Read/Write Timing in Bit Parallel Bus System Interface (for M68 Series MPU)

5.1.2 MCU Data Color Coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixels/ 3-byyes)
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixels/ 2-byyes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 3byyes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5. 4 8-Bits Parallel Interface Set Table

- Parallel 16-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
									x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4K-Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3byyes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5. 5 16-Bits Parallel Interface Set Table

- Parallel 9-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5. 6 9-Bits Parallel Interface Set Table

- Parallel 18-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	**4K-Color**
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	**65K-Color**
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 5. 7 18-Bits Parallel Interface Set Table

Parallel 8-Bits Bus Interface for RAM Data Write

Different display data formats are available for three colors depth supported by listed below.
- 4K-Colors, RGB 4, 4, 4-bits input data. (17H="03h")
- 65K-Colors, RGB 5, 6, 5-bits input data. (17H="05h")
- 262K-Colors, RGB 6, 6, 6-bits input data. (17H="06h")

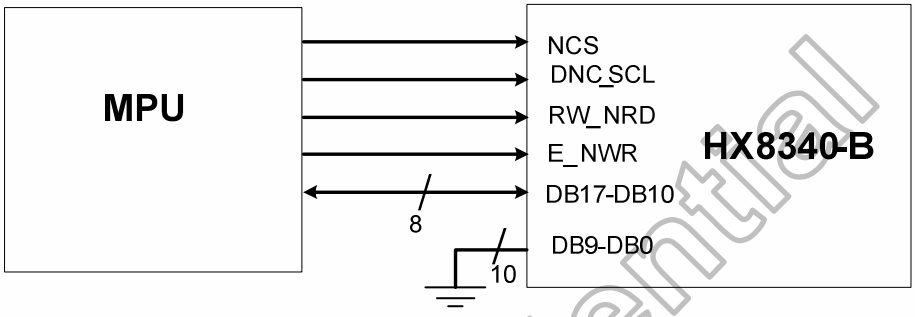
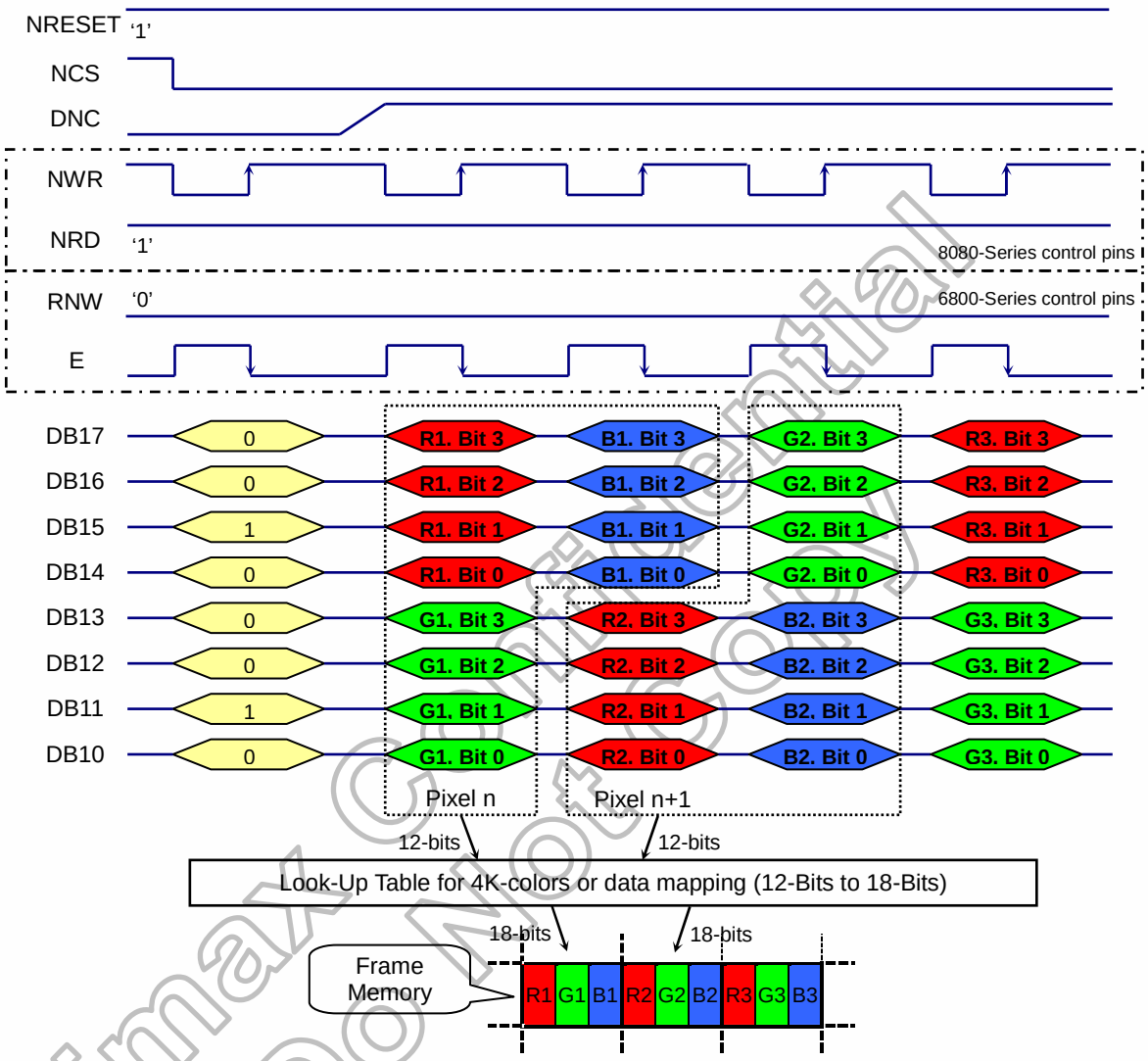


Figure 5. 5 Example of I80- / M68- System 8-Bit Parallel Bus Interface

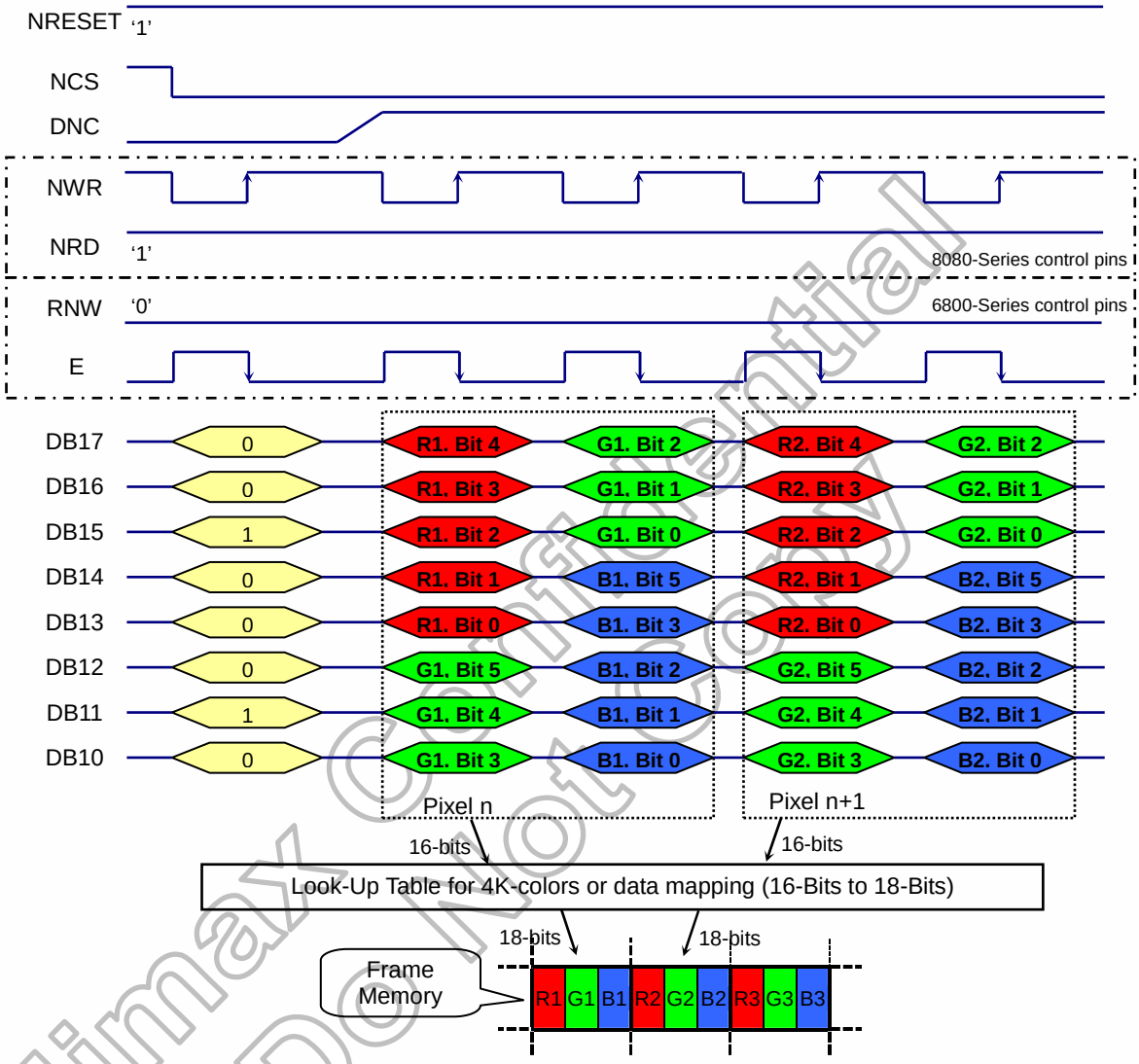
8-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colors, 17H="03h"
There are 2-pixels (6 sub-pixels) per 3-bytes.



Note: (1) The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 6 8-bit data bus for 12-bits/pixel

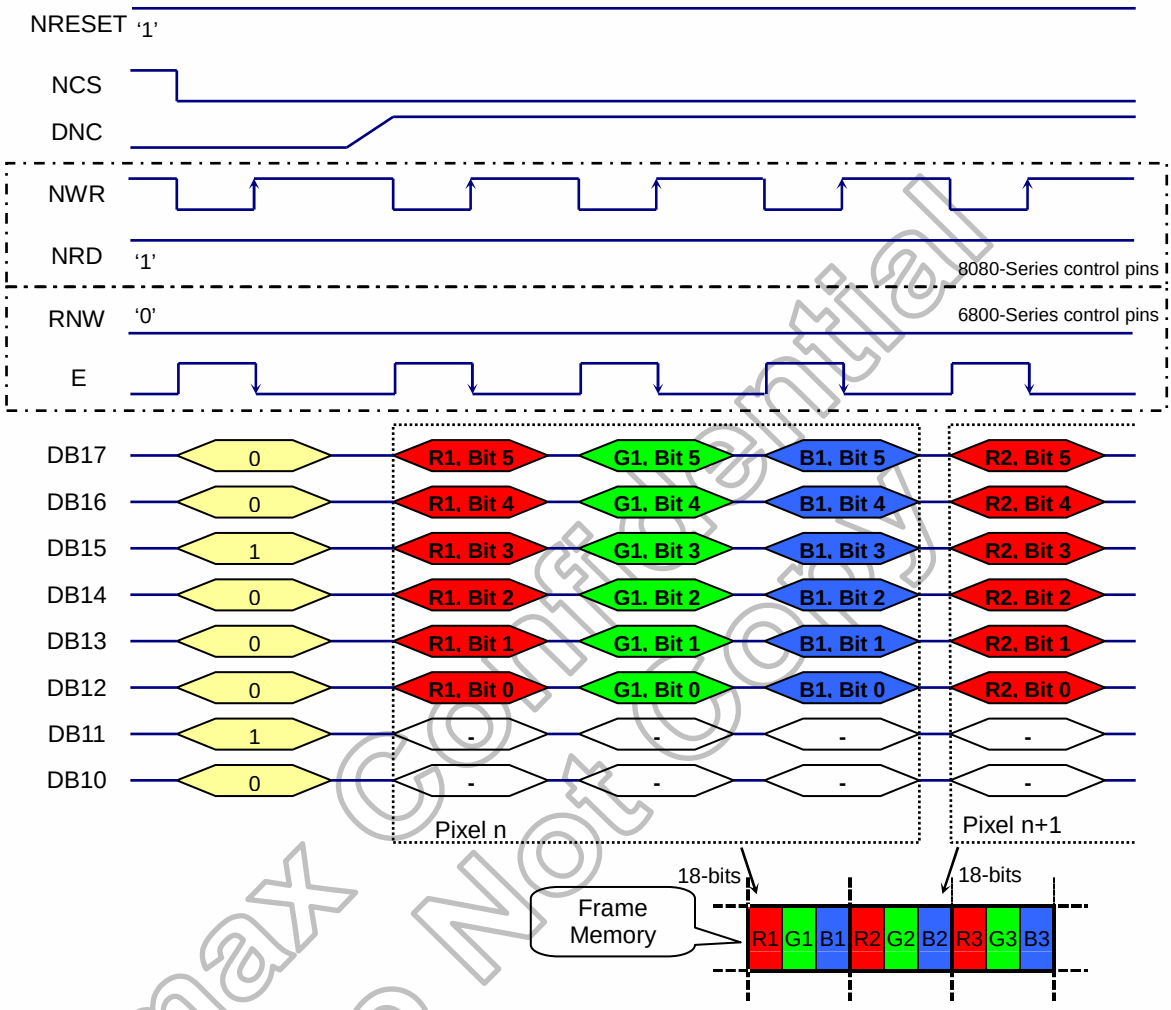
8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 17H="05h"
There is 1-pixel (3 sub-pixels) per 2-bytes.



Note: (1) The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
(2) 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 7 8-bit data bus for 16-bits/pixel

8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h"
There is 1-pixel (3 sub-pixels) per 3-bytes.



Note: (1) The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 8 8-bit data bus for 18-bits/pixel

Parallel 16-Bits Bus Interface for RAM Data Write

Different display data formats are available for three colors depth supported by listed below.
- 4K-Colors, RGB 4, 4, 4-bits input data. (17H="03h")
- 65K-Colors, RGB 5, 6, 5-bits input data. (17H="05h")
- 262K-Colors, RGB 6, 6, 6-bits input data. (17H="06h")

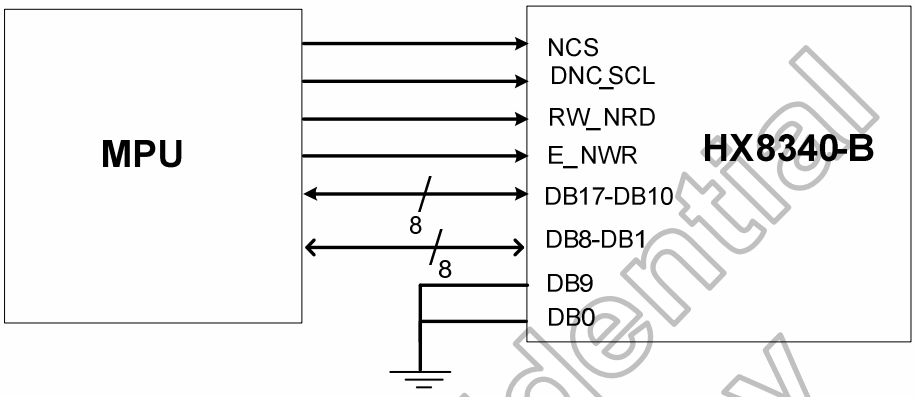
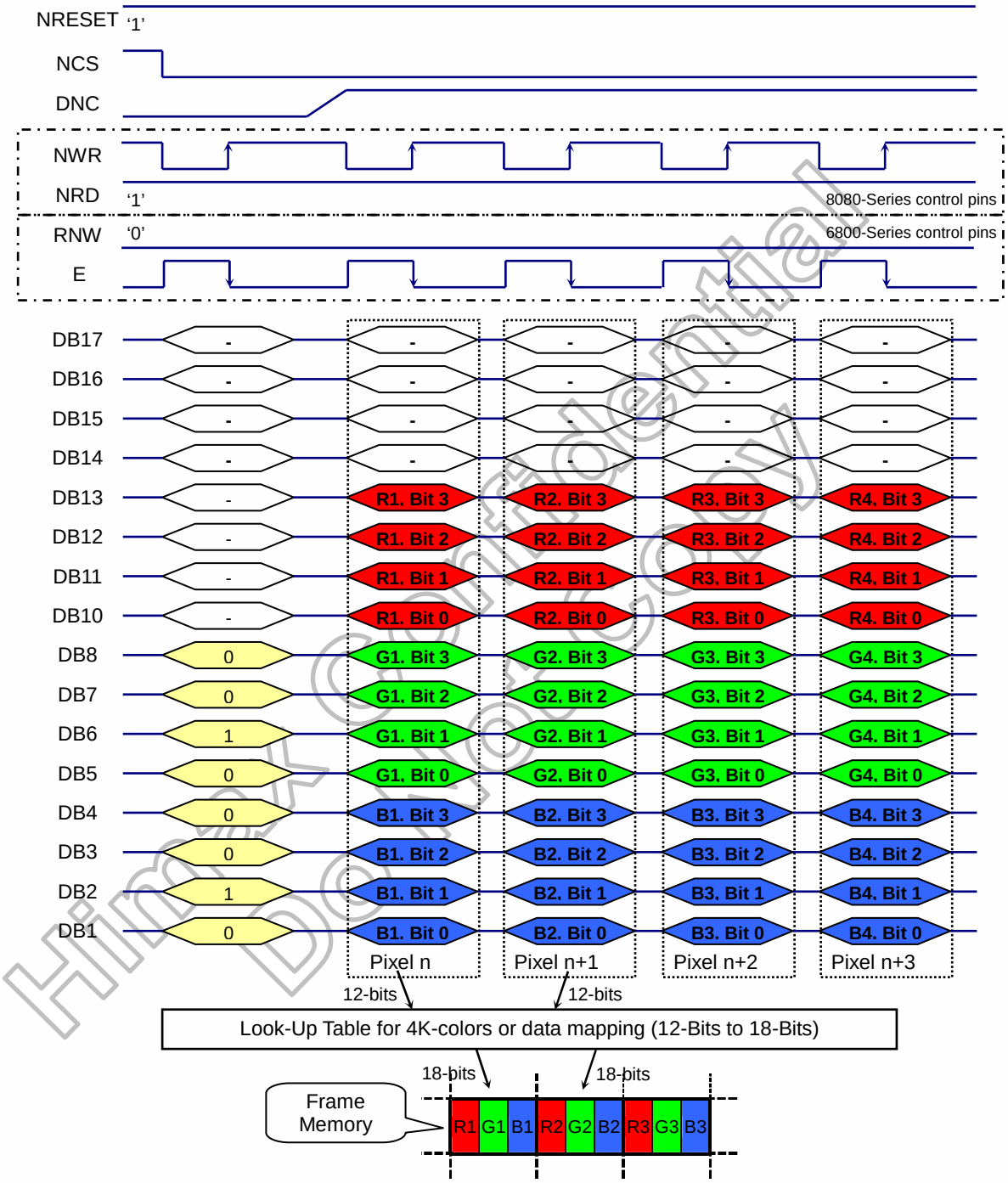


Figure 5. 9 Example of I80- / M68- System 16-Bit Parallel Bus Interface

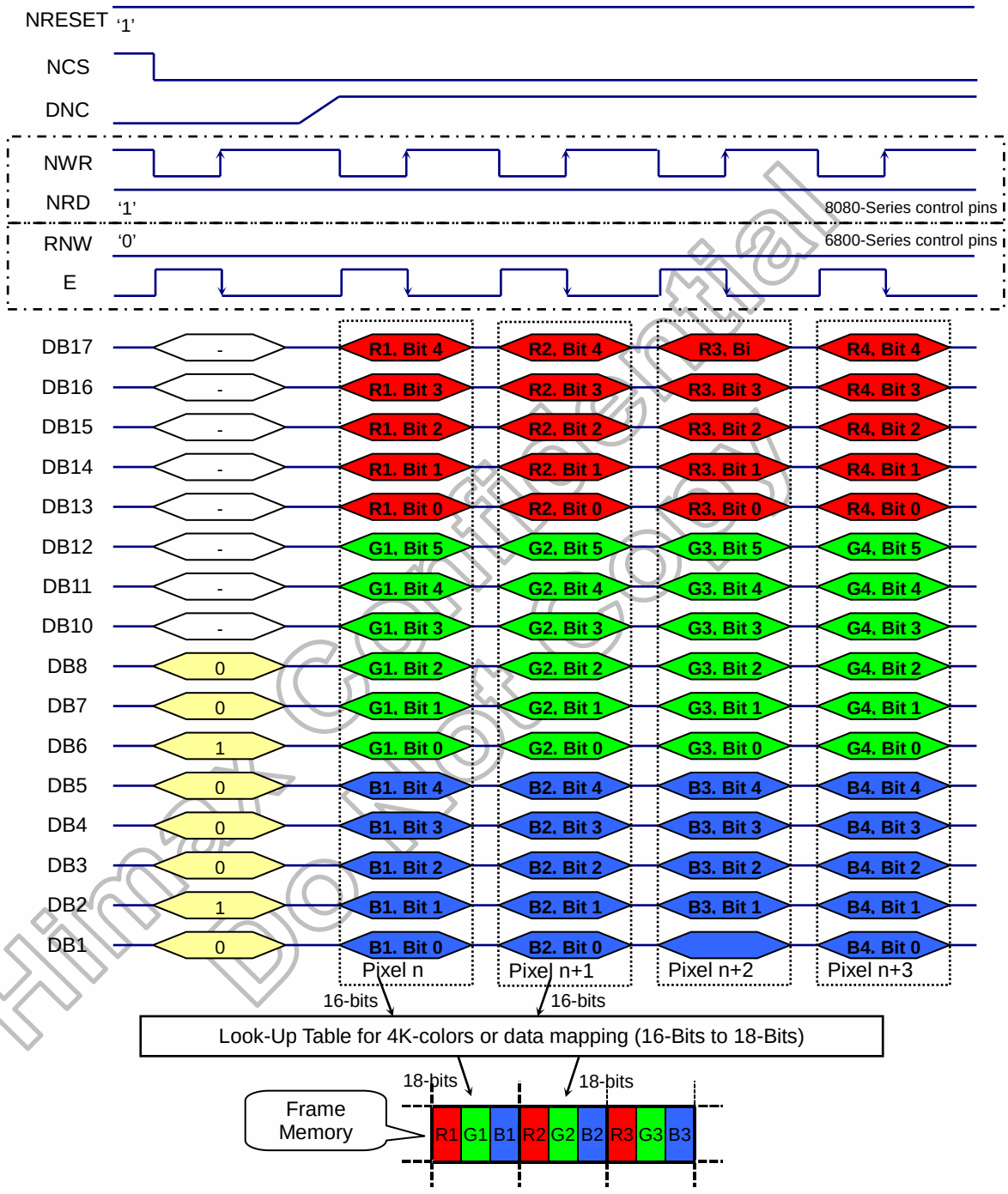
16-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colors, 17H="03h"
There is 1-pixel (3 sub-pixels) per 1-byte



Note: (1) The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
(2)1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 10 16-bit data bus for 12-bits/pixel

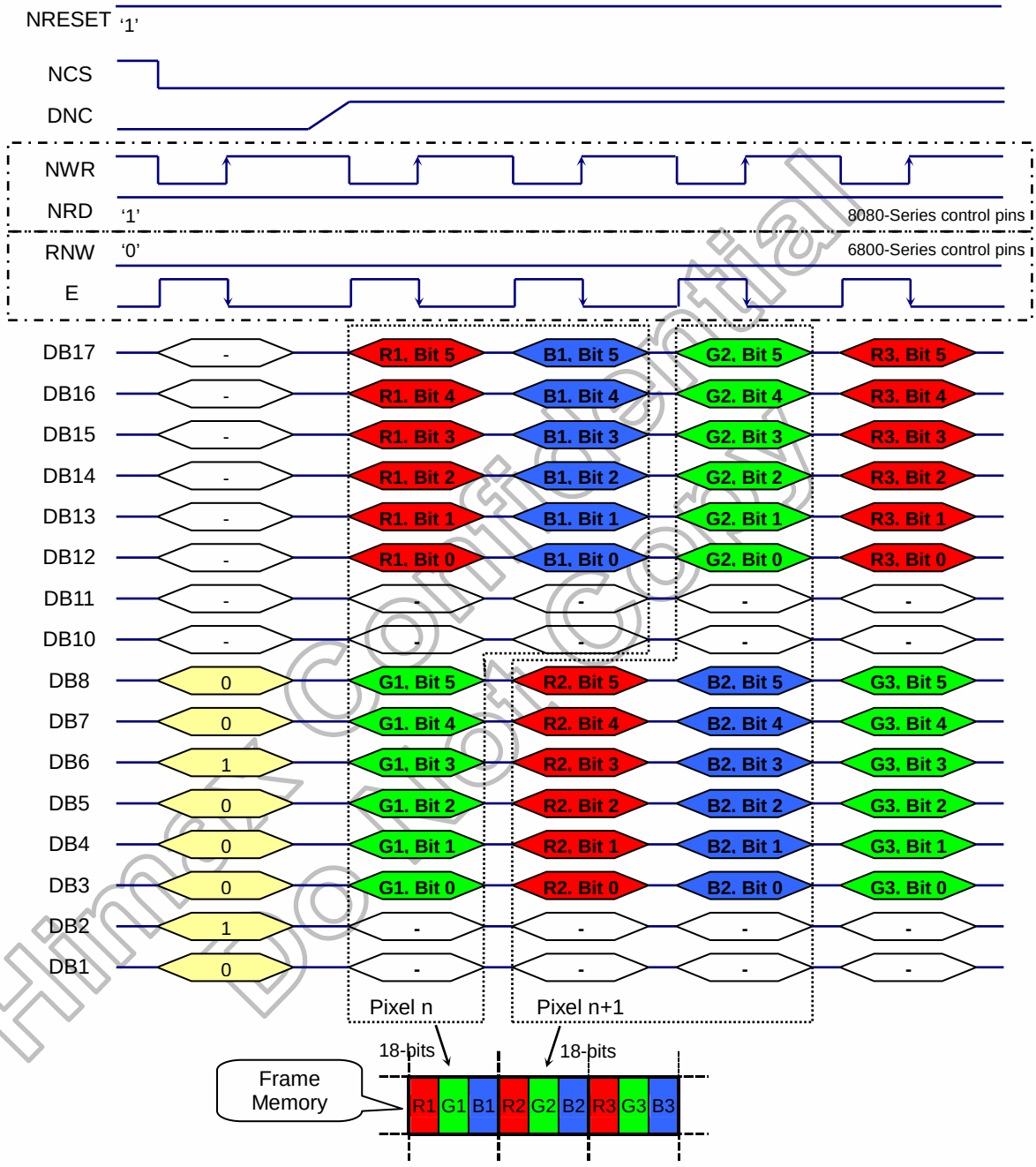
16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 17H="05h"
There is 1-pixel (3 sub-pixels) per 1-byte



Note: (1) The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
(2) 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 11 16-bit data bus for 16-bits/pixel

16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h"
There are 2-pixels (6 sub-pixels) per 3-bytes



Note: (1) The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 12 16-bit data bus for 18-bits/pixel

Parallel 9-Bits Bus Interface for RAM Data Write

Different display data formats are available for three colors depth supported by listed below.
- 262K-Colors, RGB 6, 6, 6-bits input data. (17H="06h")

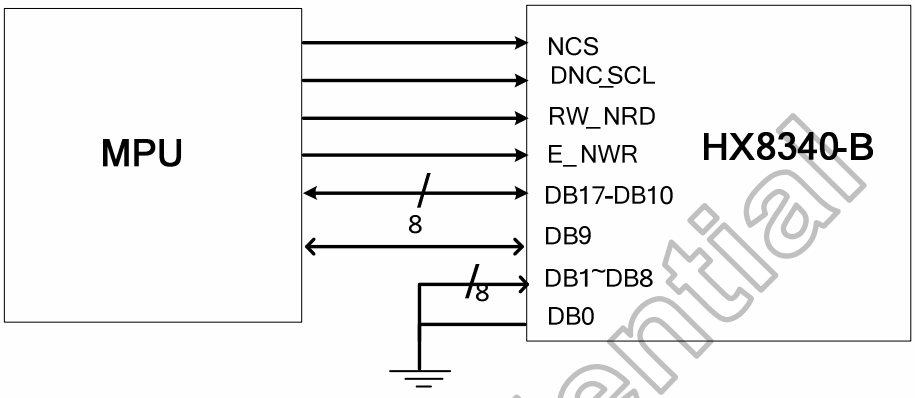
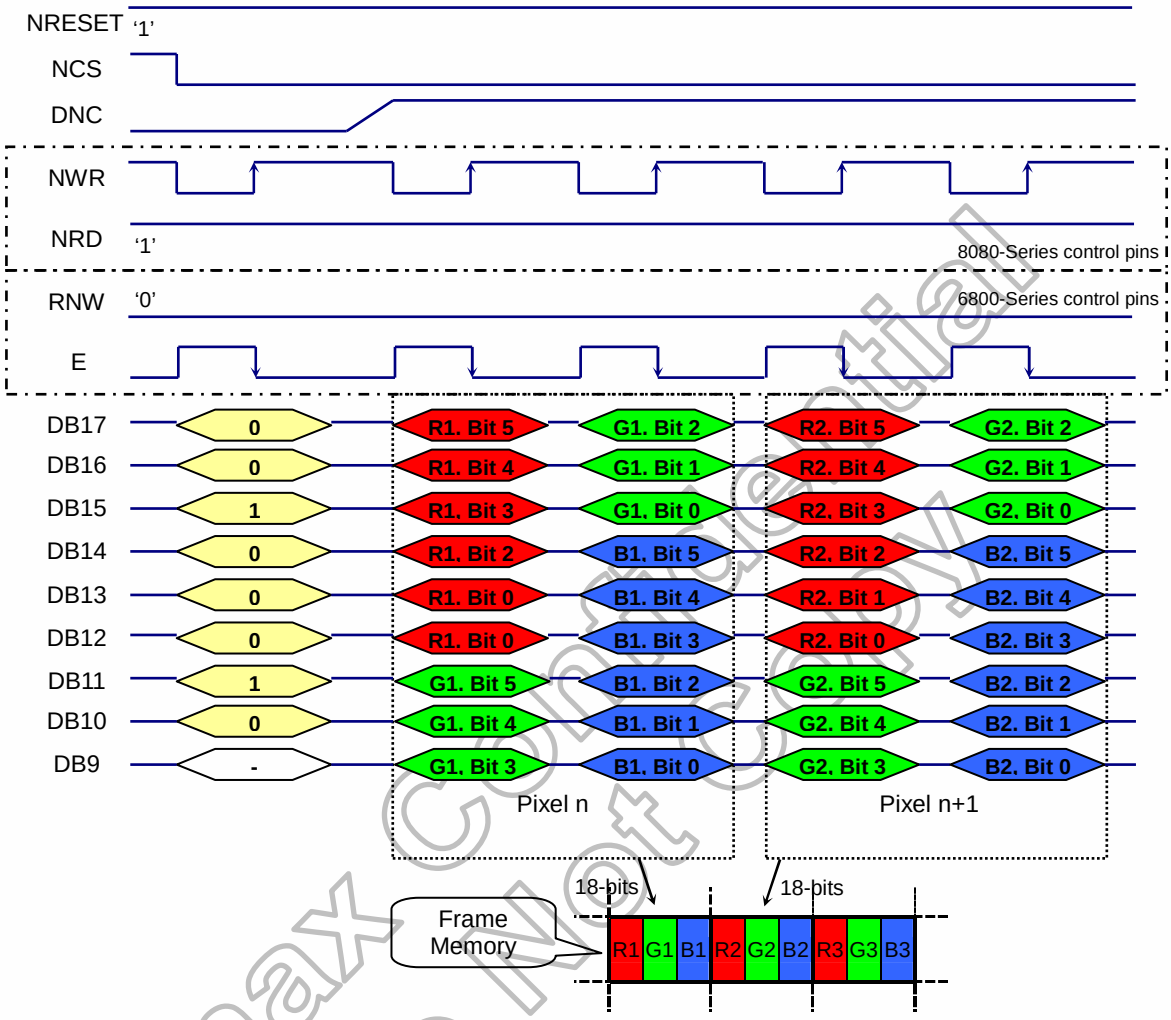


Figure 5. 13 Example of I80- / M68- System 9-Bit Parallel Bus Interface

9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h"
There is 1-pixel (3 sub-pixels) per 2-bytes



Note: (1) The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 14 9-bit data bus for 18-bits/pixel

Parallel 18-Bits Bus Interface for RAM Data Write

Different display data formats are available for three colors depth supported by listed below.
- 4K-Colors, RGB 4, 4, 4-bits input data. (17H="03h")
- 65K-Colors, RGB 5, 6, 5-bits input data. (17H="05h")
- 262K-Colors, RGB 6, 6, 6-bits input data. (17H="06h")

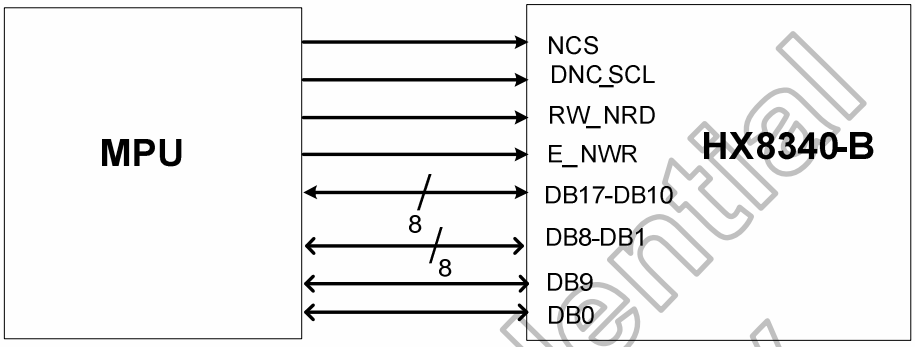
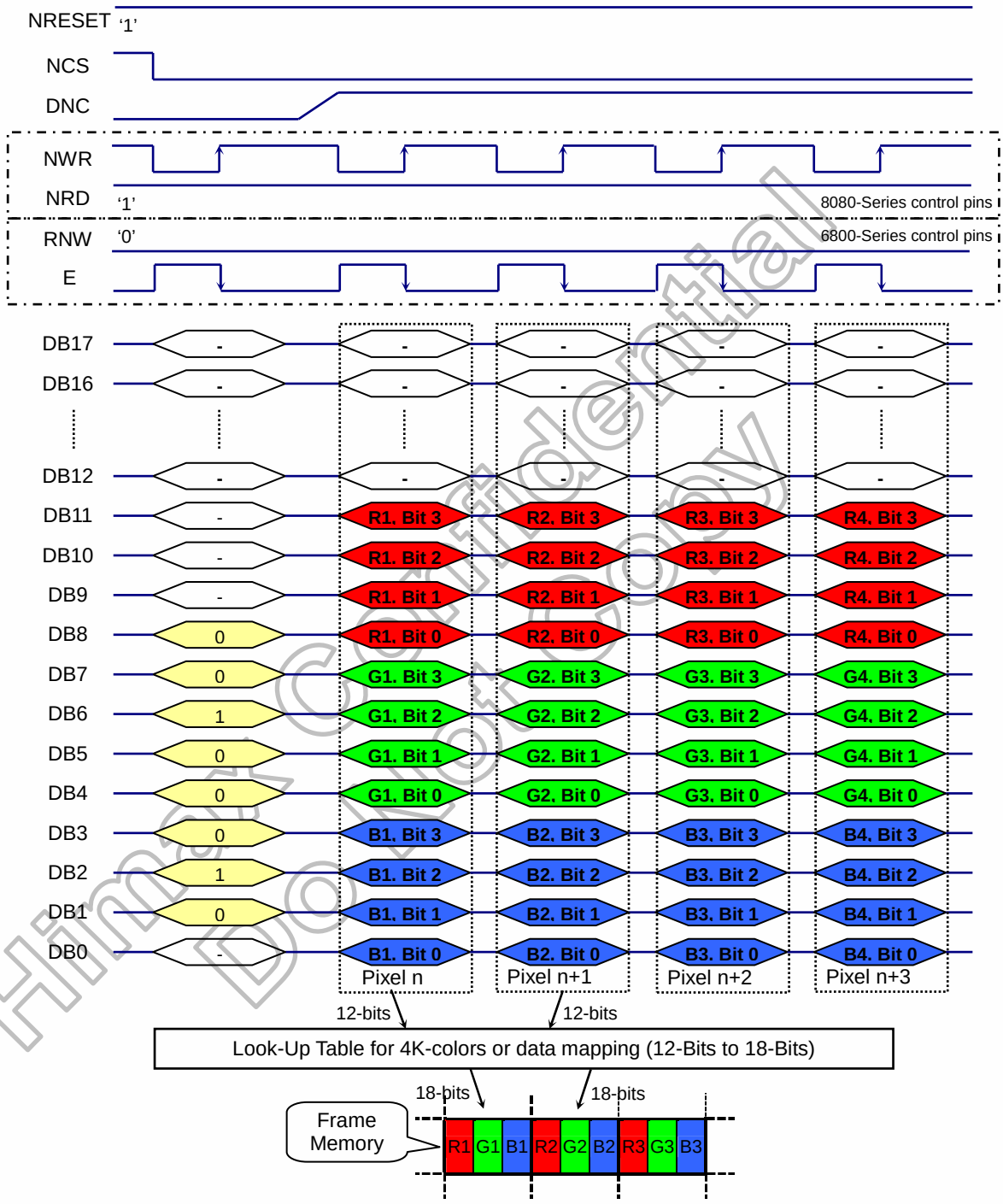


Figure 5. 15 Example of I80- / M68- System 18-Bit Parallel Bus Interface

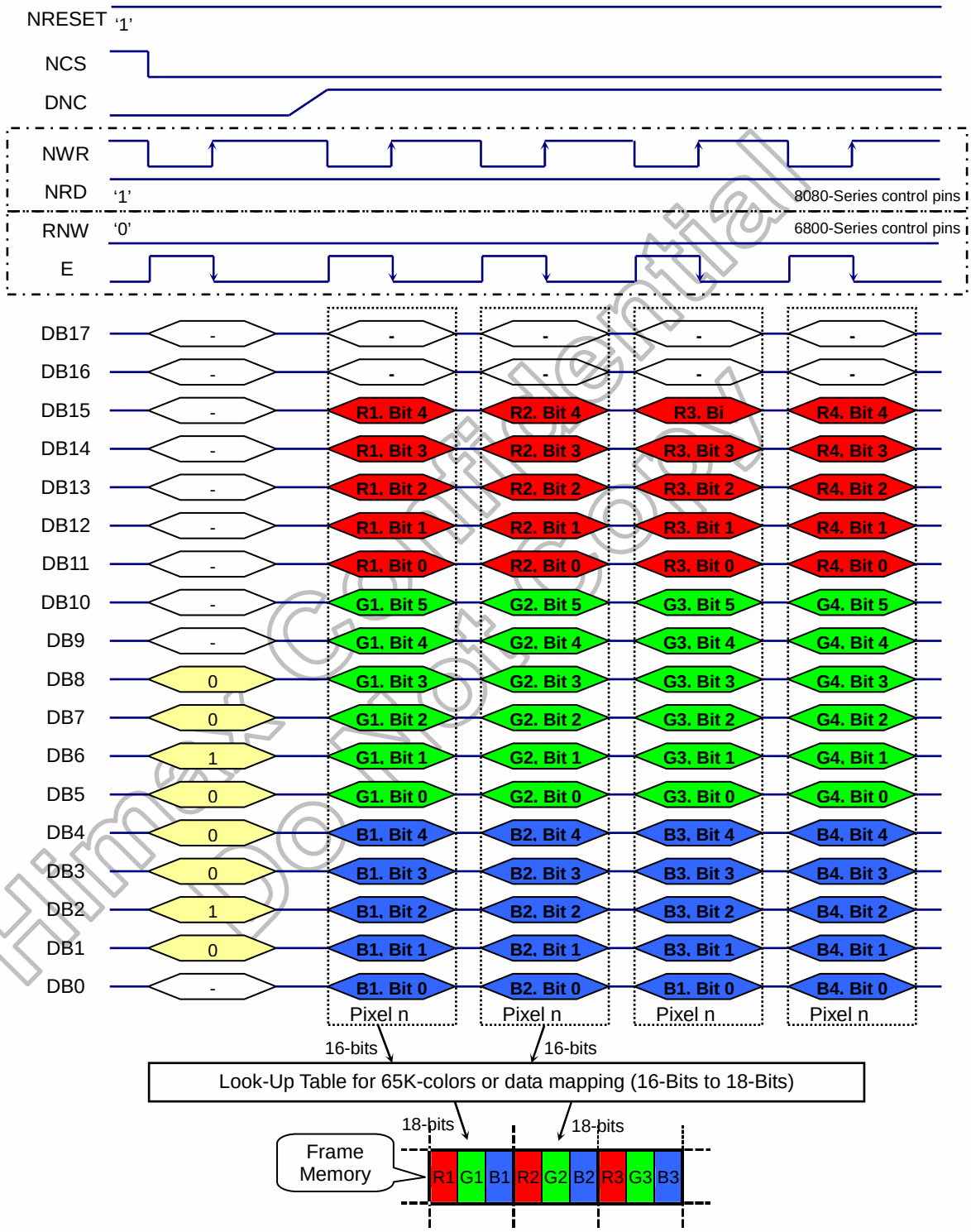
18-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colors, 17H="03h"
There is 1-pixel (3 sub-pixels) per 1-byte



Note: (1) The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
(2) 1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 16 18-bit data bus for 12-bits/pixel

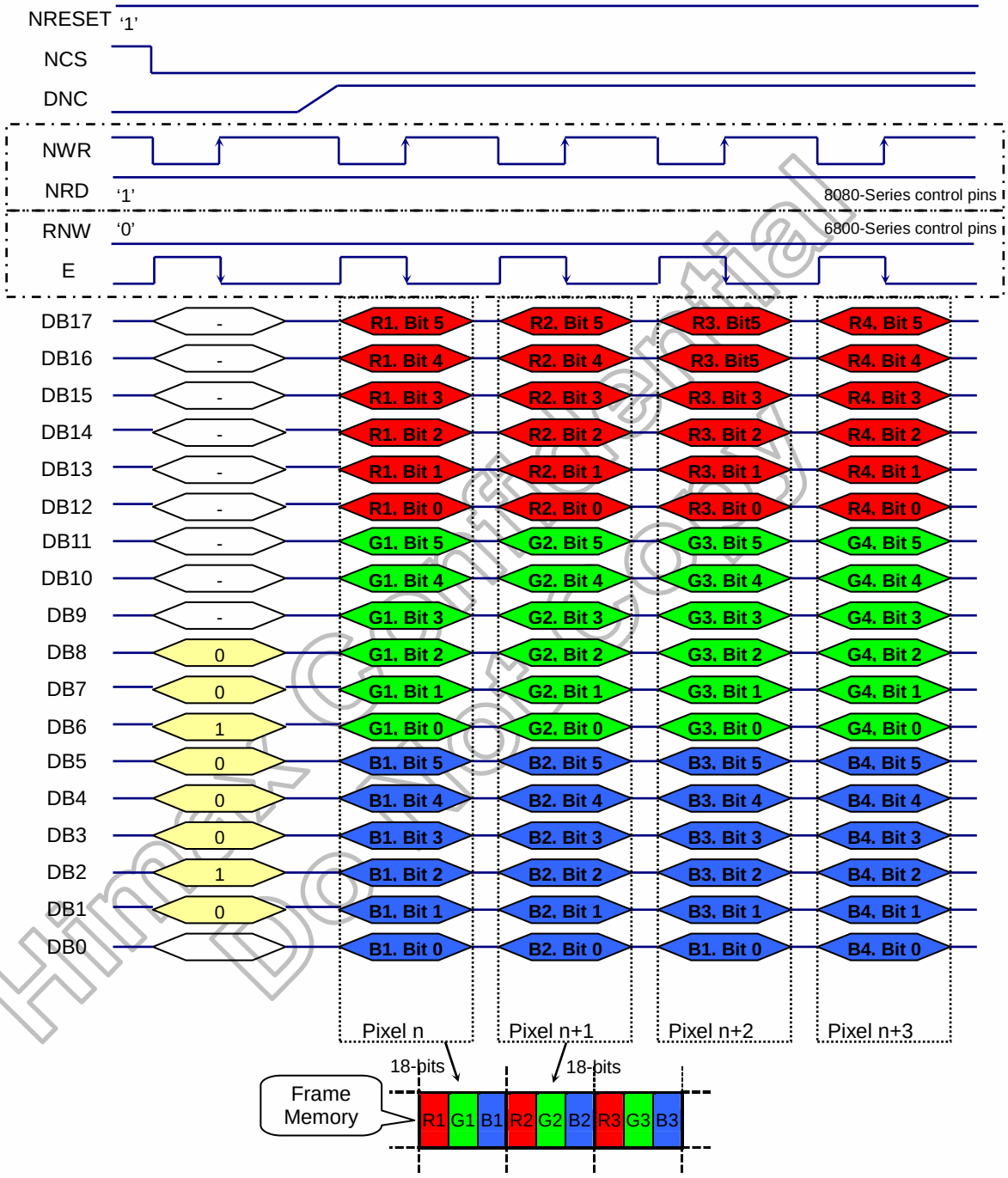
18-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 17H="05h"
There is 1-pixel (3 sub-pixels) per 1-bytes



Note: (1) The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
(2) 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 17 18-bit data bus for 16-bits/pixel

18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h"
There is 1-pixel (6 sub-pixels) per 1-byte



Note: (1) The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 18 18-bit data bus for 18-bits/pixel

5.1.3 MCU Data Color Coding for RAM Data Read

- Parallel 8-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x											262K-Color (1-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5. 8 8-Bits Parallel Interface Set Table

- Parallel 16-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
		x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5. 9 16-Bits Parallel Interface Set Table

- Parallel 9-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3										262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5. 10 9-Bits Parallel Interface Set Table

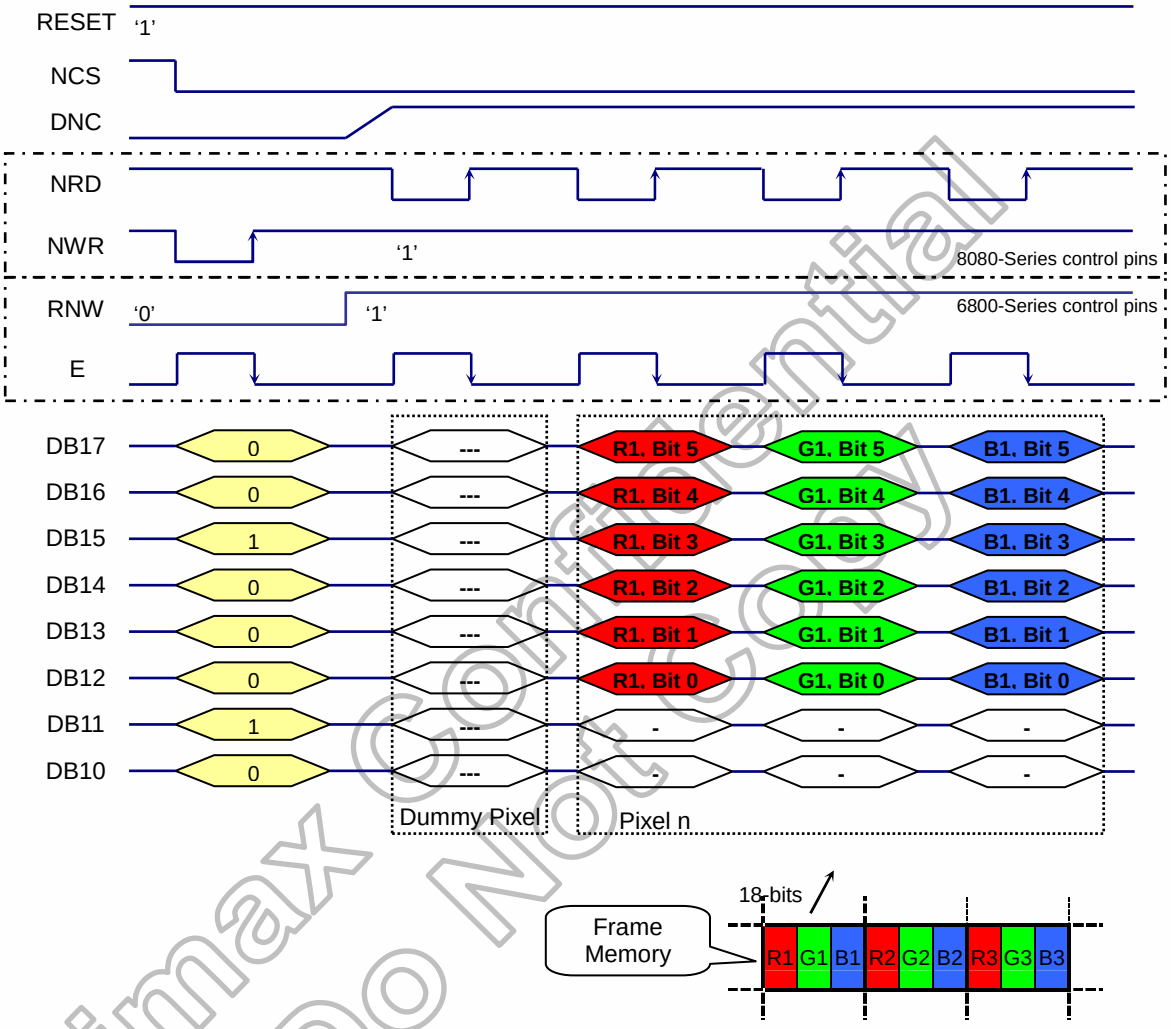
- Parallel 18-Bits Bus Interface

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
									x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1-pixels/ 2bytes)

Table 5. 11 18-Bits Parallel Interface Set Table

Parallel 8-Bits Bus Interface for RAM Data Read

There is 1-pixel (3 sub-pixels) per 3-bytes. (RGB 6-6-6-bits output)

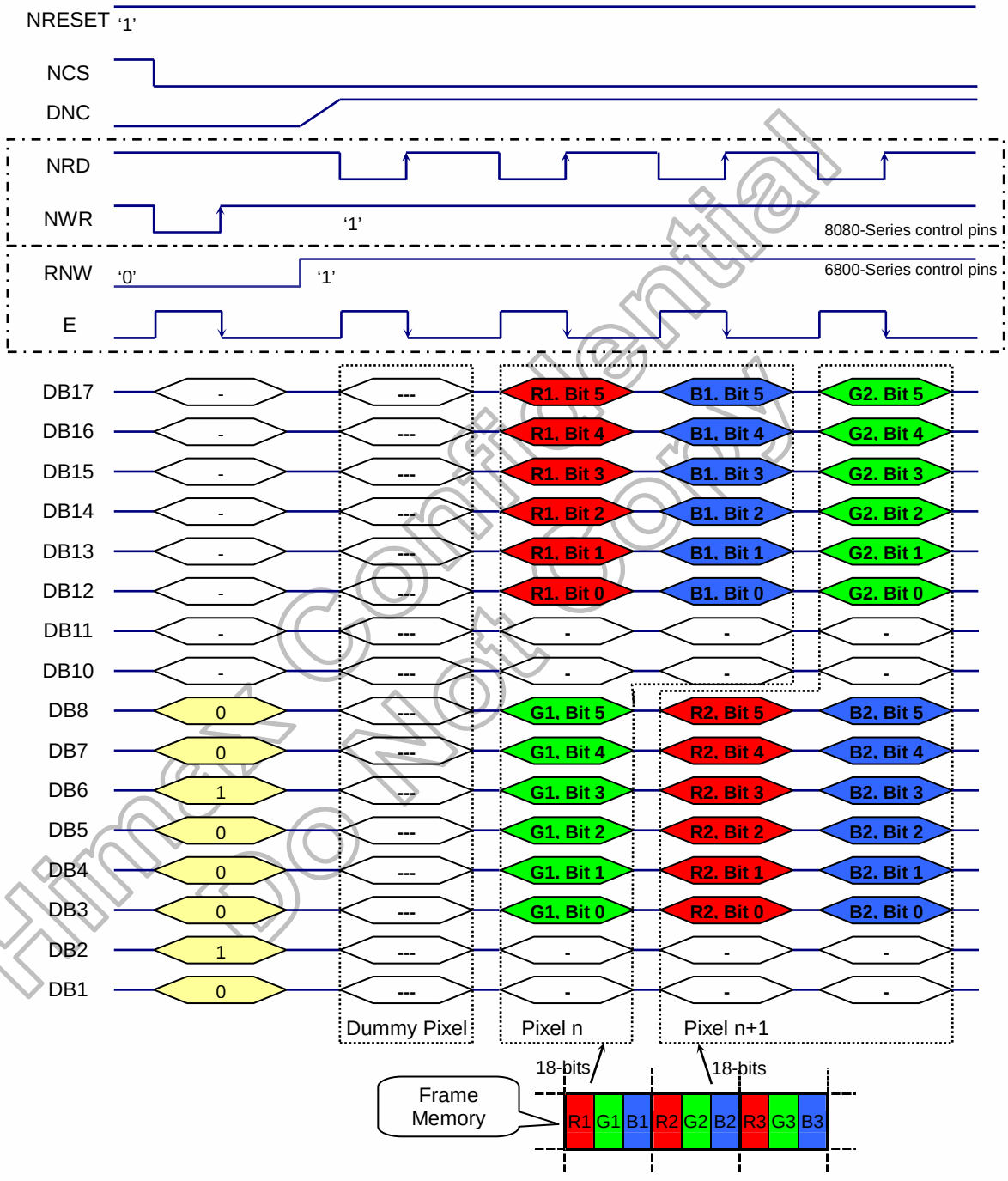


Note: (1) The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 19 8-bit data bus for RAM data read

Parallel 16-Bits Bus Interface for RAM Data Read

There are 2 pixel (6 sub-pixels) per 3 bytes (RGB 6-6-6-bits output)

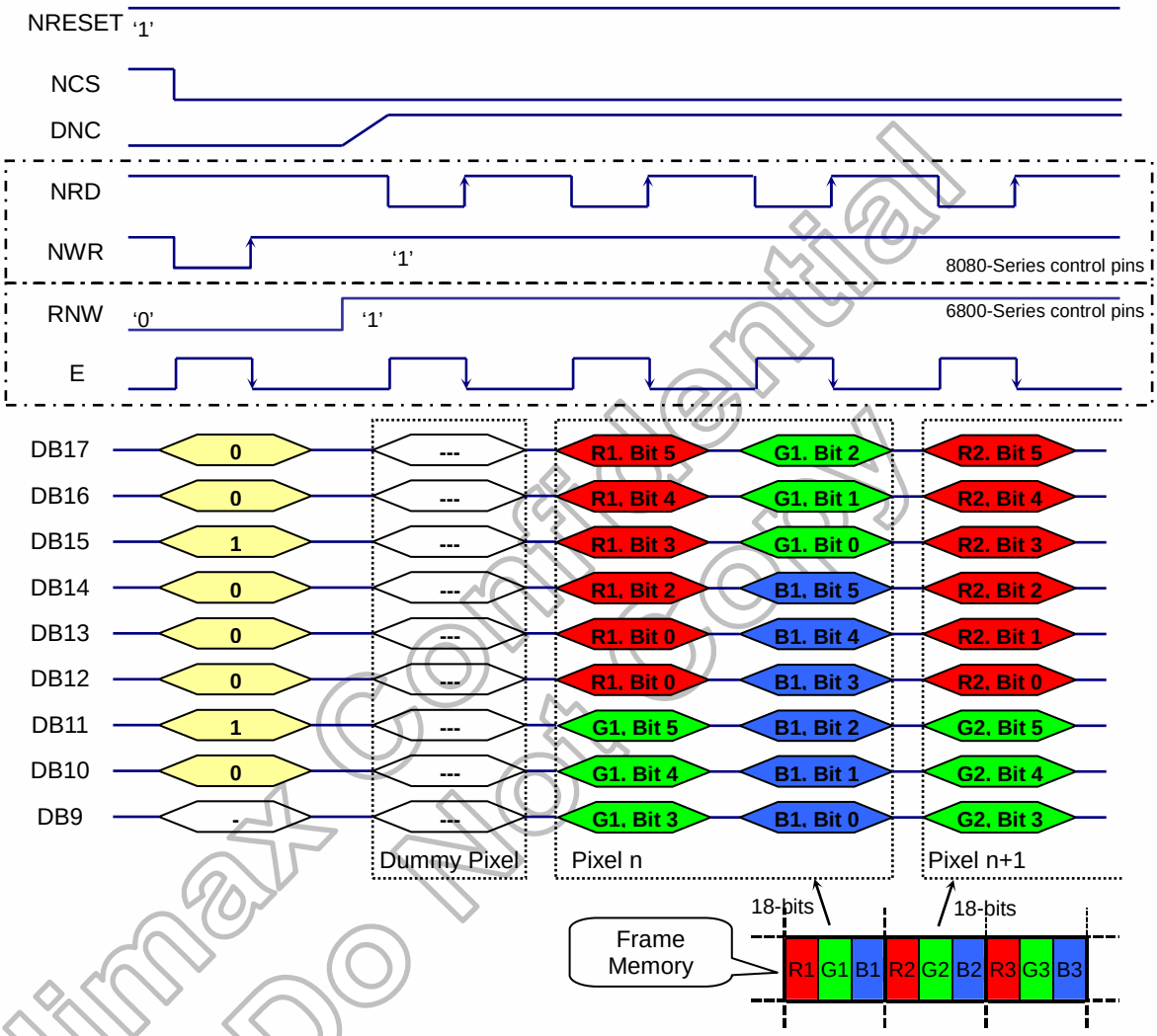


Note: (1) The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 20 16-bit data bus for RAM data read

Parallel 9-Bits Bus Interface for RAM Data Read

There are 1 pixel (3 sub-pixels) per 2 bytes (RGB 6-6-6-bits output)

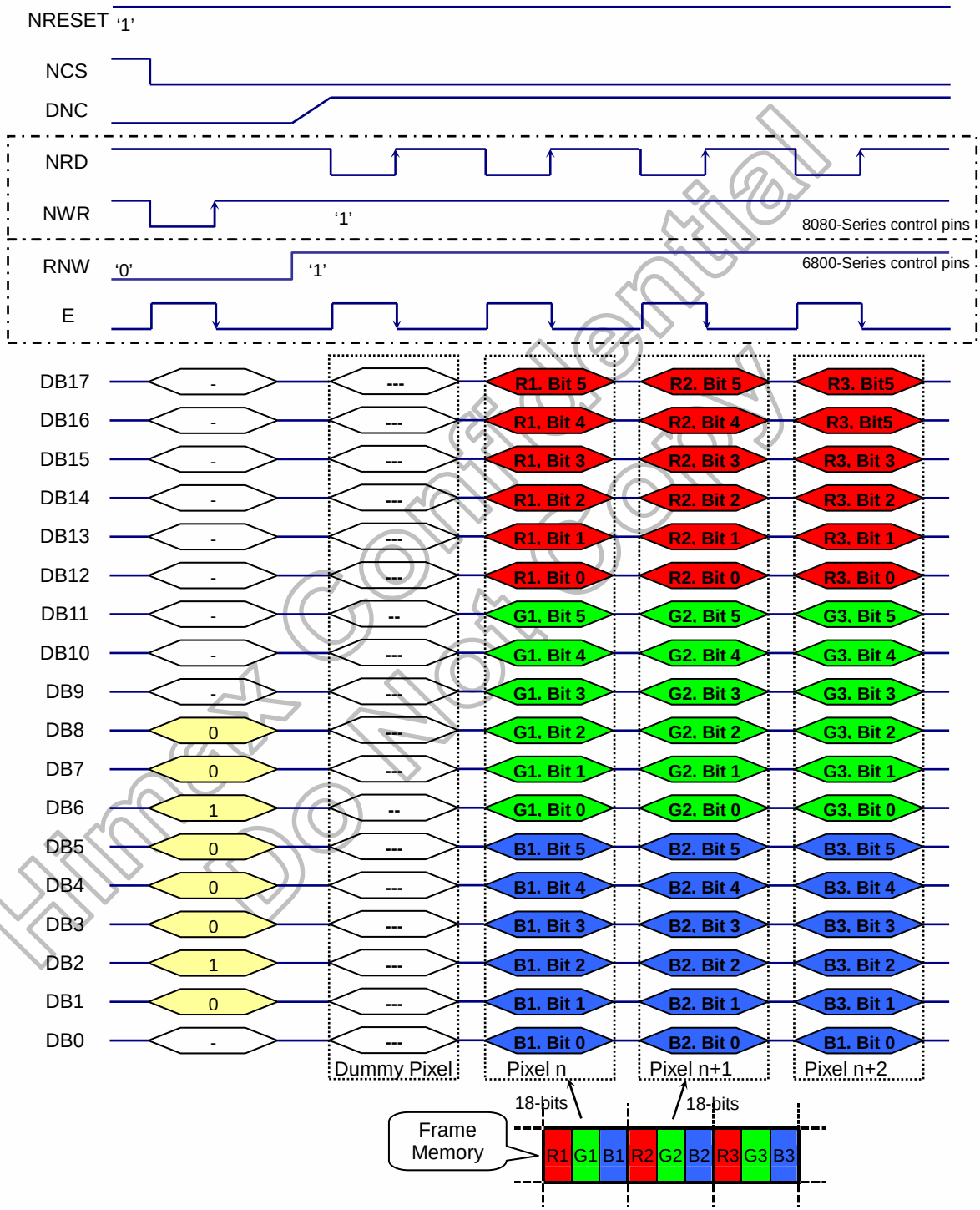


Note: (1) The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
(3)'-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 21 9-bit data bus for RAM data read

Parallel 18-Bits Bus Interface for RAM Data Read

There are 1 pixel (3 sub-pixels) per 1 bytes (RGB 6-6-6-bits output)



Note: (1) The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
(2) 1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(3) '-' = Don't care - Can be set to IOVCC or VSSD level.

Figure 5. 22 18-bit data bus for RAM data read

5.1.4 Serial Bus System Interface

The HX8340-B supports the serial bus interface in register-content mode by setting external pins “IM2” pins to “1”. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), serial output data (SDO) and the serial transfer clock signal (NWR_RNW_SCL).

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin IM0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

Table 5. 12 The Function of RS and R/W Bit

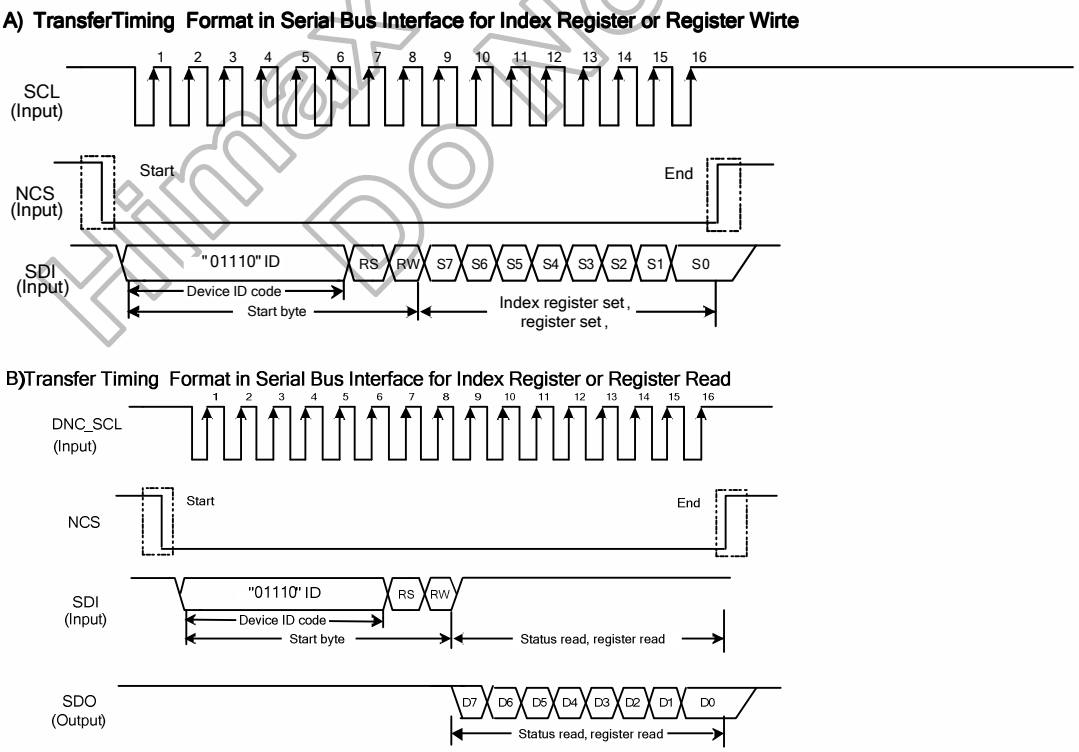


Figure 5. 23 Index Register Read/Write Timing in Serial Bus System Interface

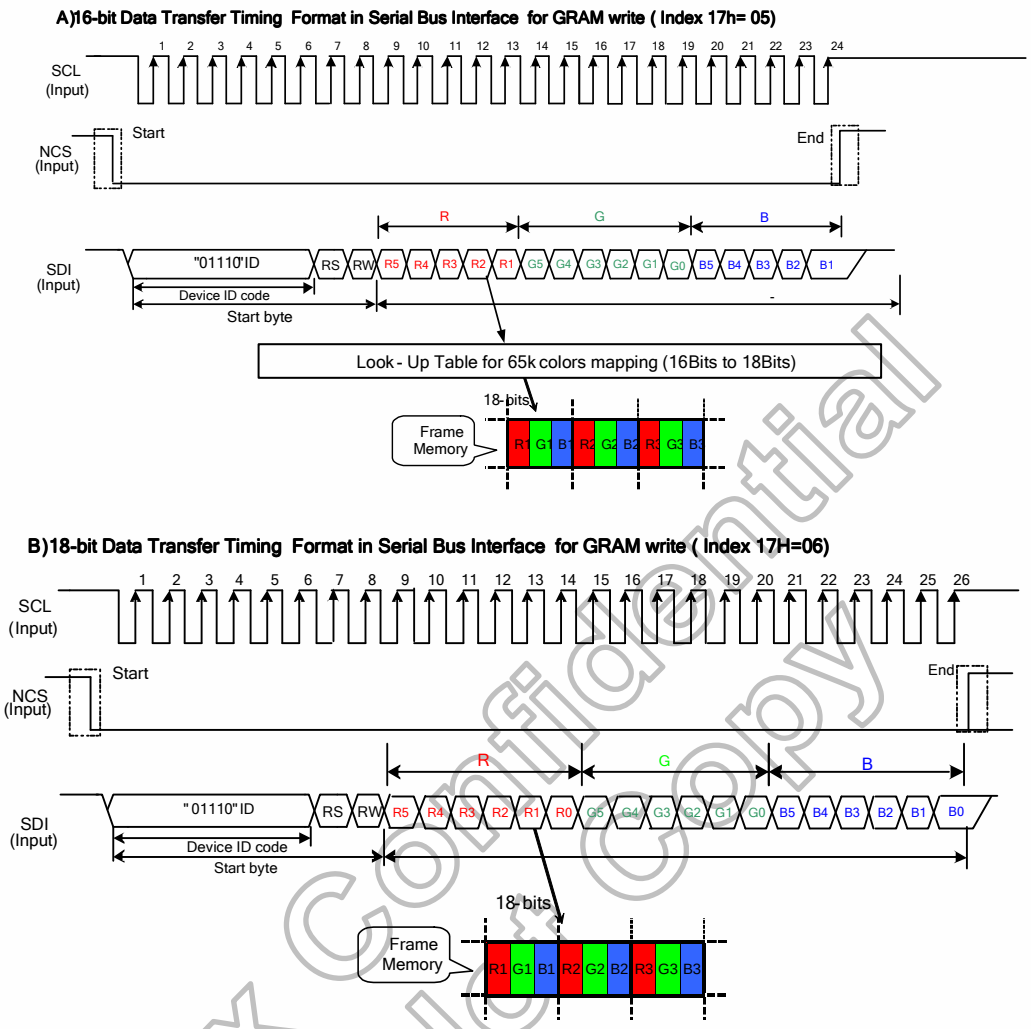


Figure 5. 24 Data Write Timing in Serial Bus System Interface

5.1.5 Color Depth Conversion Look-up Tables

Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data 4k Color
$R_{005}R_{004}$ R_{003} R_{002} R_{001} R_{000} $G_{005}G_{004}$ G_{003} G_{002} G_{001} G_{000} $B_{005}B_{004}$ B_{003} B_{002} B_{001} B_{000}	000000	1	0000
$R_{105}R_{104}$ R_{103} R_{102} R_{101} R_{100} $G_{105}G_{104}$ G_{103} G_{102} G_{101} G_{100} $B_{105}B_{104}$ B_{103} B_{102} B_{101} B_{100}	000100	2	0001
$R_{205}R_{204}$ R_{203} R_{202} R_{201} R_{200} $G_{205}G_{204}$ G_{203} G_{202} G_{201} G_{200} $B_{205}B_{204}$ B_{203} B_{202} B_{201} B_{200}	001000	3	0010
$R_{305}R_{304}$ R_{303} R_{302} R_{301} R_{300} $G_{305}G_{304}$ G_{303} G_{302} G_{301} G_{300} $B_{305}B_{304}$ B_{303} B_{302} B_{301} B_{300}	001100	4	0011
$R_{405}R_{404}$ R_{403} R_{402} R_{401} R_{400} $G_{405}G_{404}$ G_{403} G_{402} G_{401} G_{400} $B_{405}B_{404}$ B_{403} B_{402} B_{401} B_{400}	010001	5	0100
$R_{505}R_{504}$ R_{503} R_{502} R_{501} R_{500} $G_{505}G_{504}$ G_{503} G_{502} G_{501} G_{500} $B_{505}B_{504}$ B_{503} B_{502} B_{501} B_{500}	010101	6	0101
$R_{605}R_{604}$ R_{603} R_{602} R_{601} R_{600} $G_{605}G_{604}$ G_{603} G_{602} G_{601} G_{600} $B_{605}B_{604}$ B_{603} B_{602} B_{601} B_{600}	011001	7	0110
$R_{705}R_{704}$ R_{703} R_{702} R_{701} R_{700} $G_{705}G_{704}$ G_{703} G_{702} G_{701} G_{700} $B_{705}B_{704}$ B_{703} B_{702} B_{701} B_{700}	011101	8	0111
$R_{805}R_{804}$ R_{803} R_{802} R_{801} R_{800} $G_{805}G_{804}$ G_{803} G_{802} G_{801} G_{800} $B_{805}B_{804}$ B_{803} B_{802} B_{801} B_{800}	100010	9	1000
$R_{905}R_{904}$ R_{903} R_{902} R_{901} R_{900} $G_{905}G_{904}$ G_{903} G_{902} G_{901} G_{900} $B_{905}B_{904}$ B_{903} B_{902} B_{901} B_{900}	100110	10	1001
$R_{105}R_{104}$ R_{103} R_{102} R_{101} R_{100} $G_{105}G_{104}$ G_{103} G_{102} G_{101} G_{100} $B_{105}B_{104}$ B_{103} B_{102} B_{101} B_{100}	101010	11	1010
$R_{115}R_{114}$ R_{113} R_{112} R_{111} R_{110} $G_{115}G_{114}$ G_{113} G_{112} G_{111} G_{110} $B_{115}B_{114}$ B_{113} B_{112} B_{111} B_{110}	101110	12	1011
$R_{125}R_{124}$ R_{123} R_{122} R_{121} R_{120} $G_{125}G_{124}$ G_{123} G_{122} G_{121} G_{120} $B_{125}B_{124}$ B_{123} B_{122} B_{121} B_{120}	110011	13	1100
$R_{135}R_{134}$ R_{133} R_{132} R_{131} R_{130} $G_{135}G_{134}$ G_{133} G_{132} G_{131} G_{130} $B_{135}B_{134}$ B_{133} B_{132} B_{131} B_{130}	110111	14	1101
$R_{145}R_{144}$ R_{143} R_{142} R_{141} R_{140} $G_{145}G_{144}$ G_{143} G_{142} G_{141} G_{140} $B_{145}B_{144}$ B_{143} B_{142} B_{141} B_{140}	111011	15	1110
$R_{155}R_{154}$ R_{153} R_{152} R_{151} R_{150} $G_{155}G_{154}$ G_{153} G_{152} G_{151} G_{150} $B_{155}B_{154}$ B_{153} B_{152} B_{151} B_{150}	111111	16	1111

Table 5. 13 Look-up Tables for 4k Color Mode

Look Up Table Outputs Frame Memory Data (6-bit)	Default value after H/W Reset	RGBSET parameter	Look Up Table Input Data 65k Color
R005 R004 R003 R002 R001 R000 B005 B004 B003 B002 B001 B000	000000	1	00000
R105 R104 R103 R102 R101 R100 B105 B104 B103 B102 B101 B100	000010	2	00001
R205 R204 R203 R202 R201 R200 B205 B204 B203 B202 B201 B200	000100	3	00010
R305 R304 R303 R302 R301 R300 B305 B304 B303 B302 B301 B300	000110	4	00011
R405 R404 R403 R402 R401 R400 B405 B404 B403 B402 B401 B400	001000	5	00100
R505 R504 R503 R502 R501 R500 B505 B504 B503 B502 B501 B500	001010	6	00101
R605 R604 R603 R602 R601 R600 B605 B604 B603 B602 B601 B600	001100	7	00110
R705 R704 R703 R702 R701 R700 B705 B704 B703 B702 B701 B700	001110	8	00111
R805 R804 R803 R802 R801 R800 B805 B804 B803 B802 B801 B800	010000	9	01000
R905 R904 R903 R902 R901 R900 B905 B904 B903 B902 B901 B900	010010	10	01001
R105 R104 R103 R102 R101 R100 B105 B104 B103 B102 B101 B100	010100	11	01010
R115 R114 R113 R112 R111 R110 B115 B114 B113 B112 B111 B110	010110	12	01011
R125 R124 R123 R122 R121 R120 B125 B124 B123 B122 B121 B120	011000	13	01100
R135 R134 R133 R132 R131 R130 B135 B134 B133 B132 B131 B130	011010	14	01101
R145 R144 R143 R142 R141 R140 B145 B144 B143 B142 B141 B140	011100	15	01110
R155 R154 R153 R152 R151 R150 B155 B154 B153 B152 B151 B150	011110	16	01111
R165 R164 R163 R162 R161 R160 B165 B164 B163 B162 B161 B160	100001	17	10000
R175 R174 R173 R172 R171 R170 B175 B174 B173 B172 B171 B170	100011	18	10001
R185 R184 R183 R182 R181 R180 B185 B184 B183 B182 B181 B180	100101	19	10010
R195 R194 R193 R192 R191 R190 B195 B194 B193 B192 B191 B190	100111	20	10011
R205 R204 R203 R202 R201 R200 B205 B204 B203 B202 B201 B200	101001	21	10100
R215 R214 R213 R212 R211 R210 B215 B214 B213 B212 B211 B210	101011	22	10101
R225 R224 R223 R222 R221 R220 B225 B224 B223 B222 B221 B220	101101	23	10110
R235 R234 R233 R232 R231 R230 B235 B234 B233 B232 B231 B230	101111	24	10111
R245 R244 R243 R242 R241 R240 B245 B244 B243 B242 B241 B240	110001	25	11000
R255 R254 R253 R252 R251 R250 B255 B254 B253 B252 B251 B250	110011	26	11001
R265 R264 R263 R262 R261 R260 B265 B264 B263 B262 B261 B260	110101	27	11010
R275 R274 R273 R272 R271 R270 B275 B274 B273 B272 B271 B270	110111	28	11011
R285 R284 R283 R282 R281 R280 B285 B284 B283 B282 B281 B280	111001	29	11100
R295 R294 R293 R292 R291 R290 B295 B294 B293 B292 B291 B290	111011	30	11101
R305 R304 R303 R302 R301 R300 B305 B304 B303 B302 B301 B300	111101	31	11110
R315 R314 R313 R312 R311 R310 B315 B314 B313 B312 B311 B310	111111	32	11111

Note: Green color in 65k color mode is mapping directly.

Table 5. 14 Look-up Tables for 65k Color Mode

5.2 RGB Interface

The HX8340-B uses **RCM[1:0]='10' or '11' hardware setting to select RGB interface.** When after Power on Sequence, the RGB interface is activated. When RCM[1:0]='10' use VS, HS, DE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM[1:0]='11' use VS, HS, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VS, HS, DE and DB17-0 lines states when there is a rising edge of the DOTCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level('H') of DE signal, and display operations are executed in synchronization with the frame synchronizing signal (VS), line synchronizing signal (HS) and pixel clock (DOTCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HS signal, and the VBP setting of VS. In these two RGB interface mode, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VS) signal is used to tell when there is received a new frame of the display, and this is negative ('-', '0', low) active. Horizontal synchronization signal (HS) is used to tell when there is received a new line of the frame, and this is negative ('-', '0', low) active. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display, and this is positive ('+', '1', high) active. DB17-0 are used to tell what is the information of the image that is transferred on the display when DE='H'.

The pixel clock cycle is described in the following figure.

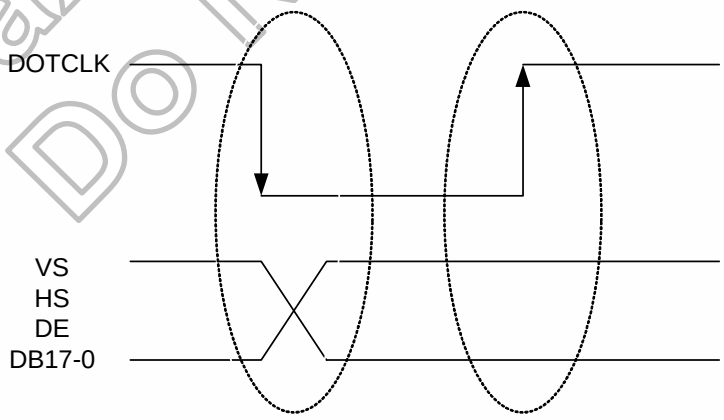


Figure 5. 25 DOTCLK Cycle

General timing diagram in RGB interface is as follow

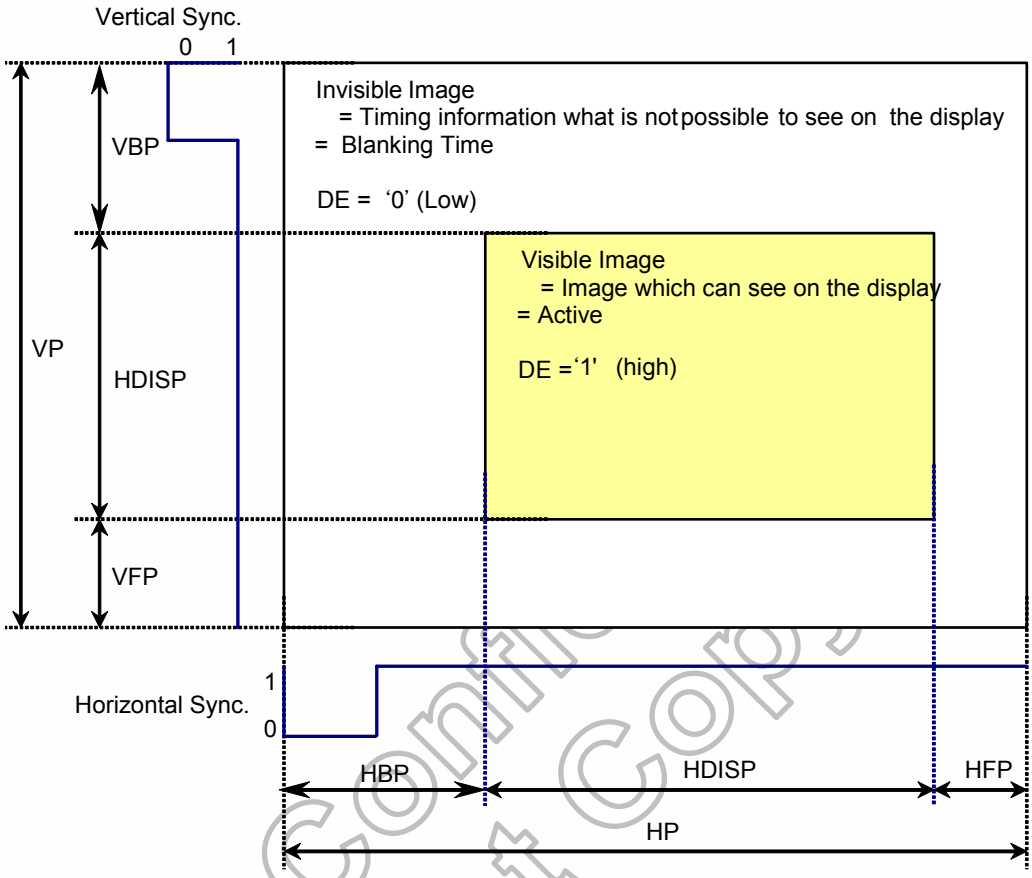
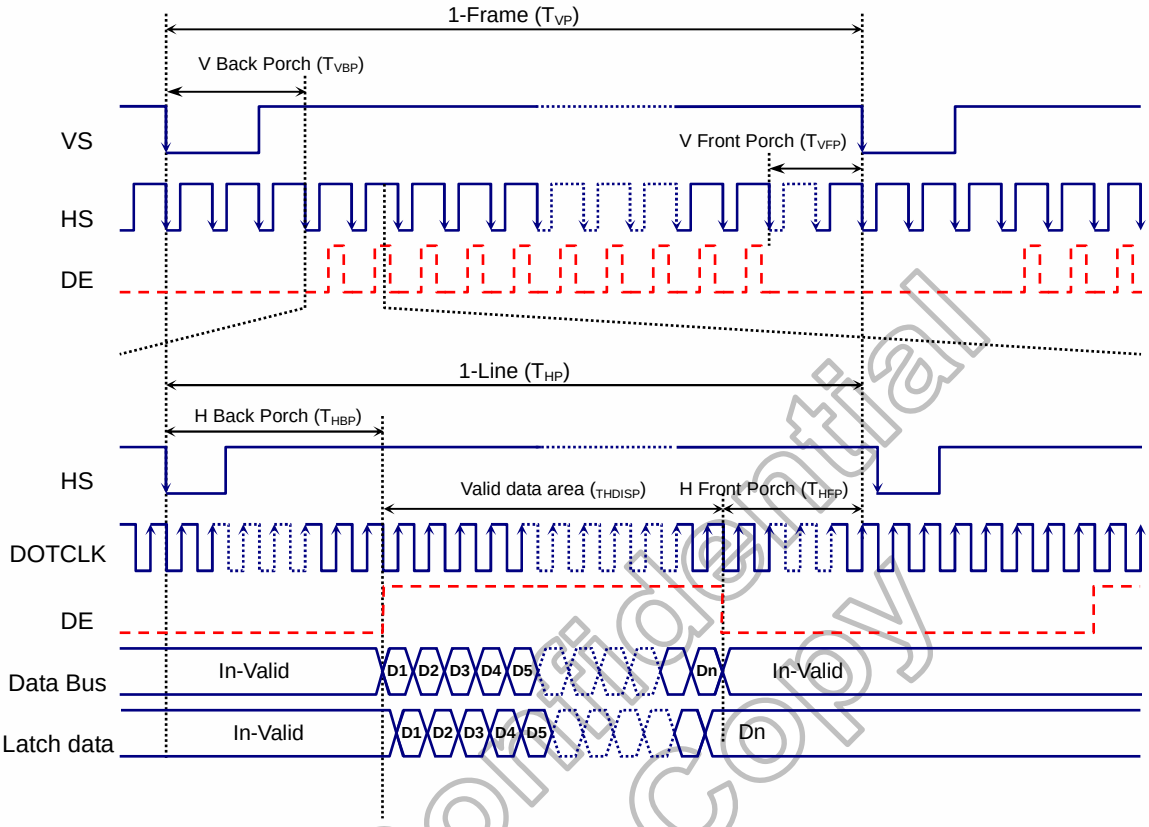


Figure 5. 26 RGB Interface Circuit Input Timing Diagram

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.



Note: (1) RGB mode 2 doesn't need DE signal
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (33H) command.

Figure 5. 27 RGB Mode timing Diagram

All 3-kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bits, 16-bits and 18-bits data width)

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
E0h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note: (1) When 17H="E0h", 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(2) Only 17H= "50h","60h", "E0h" are valid on RGB I/F, Others are invalid.
(3) 'x' don't care, but need to set IOVCC or VSSD level.

Table 5. 15 RGB interface Bus Width Set Table

RGB Interface Mode

RGB I/F Mode	DOTCLK	DE	VS	HS	Video Data bus DB[B:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = "10"), writing data to display is done by DOTCLK and Video Data Bus (DB[B:0]), when DE is high state. The external synchronization signals (DOTCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VS, HS and DE signals to driver.

In RGB Mode 2 (RCM1, RCM0 = "11"), blanking porch setting of VS and HS signals are defined by RGBBPCTR command. DE pin is not used.

5.2.1 Color Order on RGB Interface

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on RGB interface, is describing on the following table:

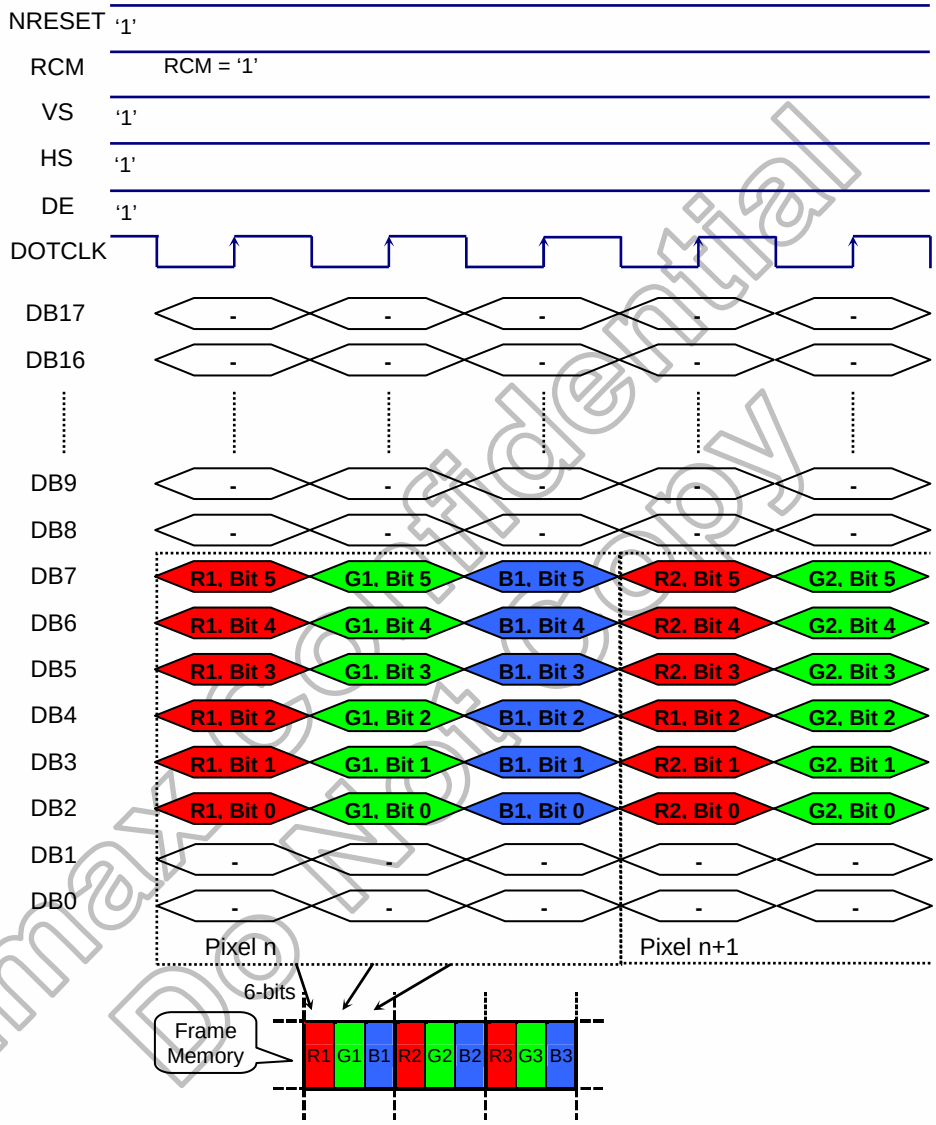
Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colors on this table - Not all gray levels of colors.

Table 5. 16 Meaning of the Pixel Information for Main Colors on RGB Interface

5.2.2 RGB Data Color Coding

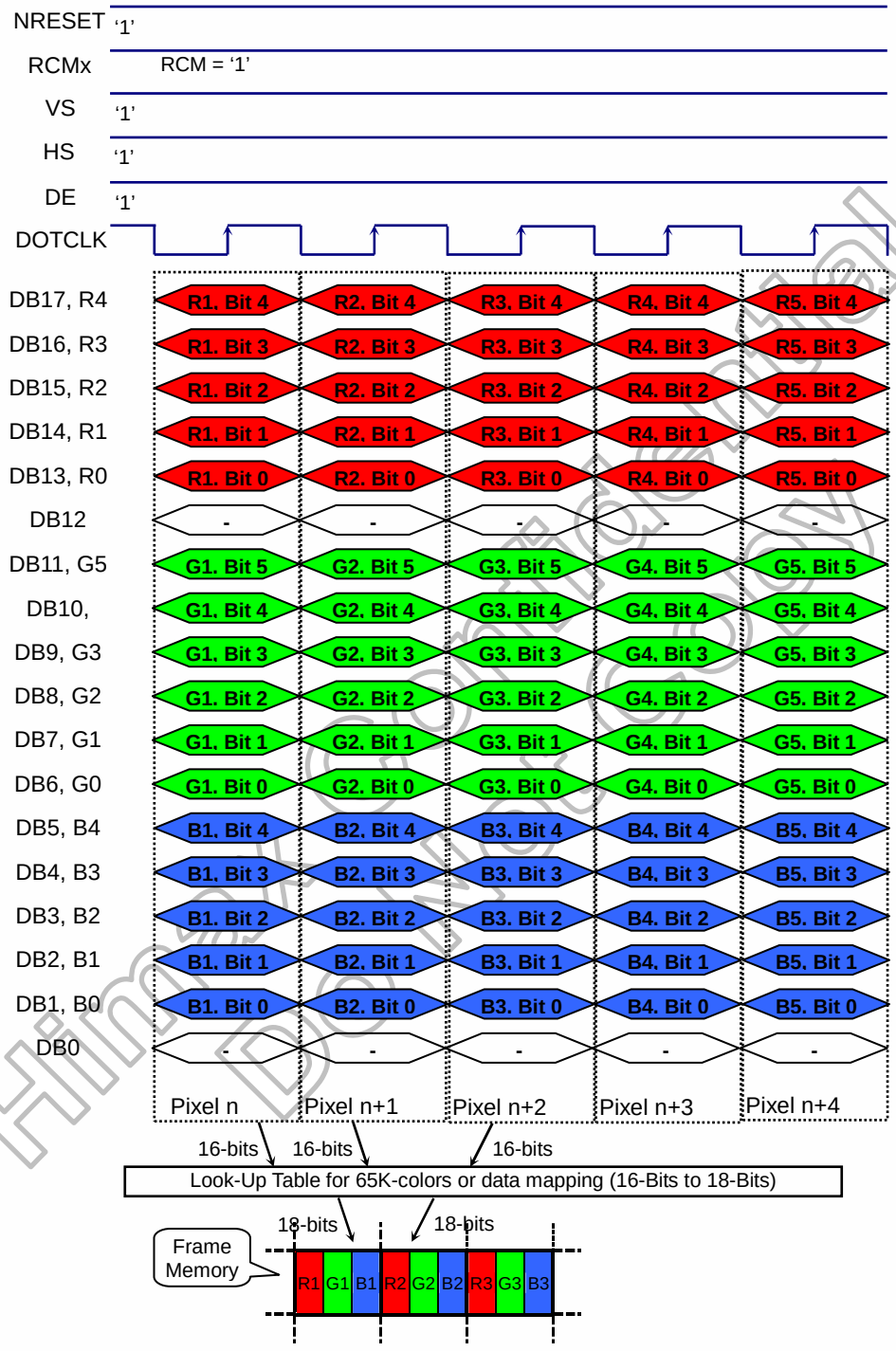
18-bits/pixel Colors Order on 6-bits Data width RGB Interface (RGB 6-6-6-bits input).
There are 1 pixel (3 sub-pixels) per 3 bytes, 262K-colors, 17H="E0h"



Note: (1) The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-trandfer data one pixel)
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 28 RGB 18-bits/pixel on 6-bits Data width

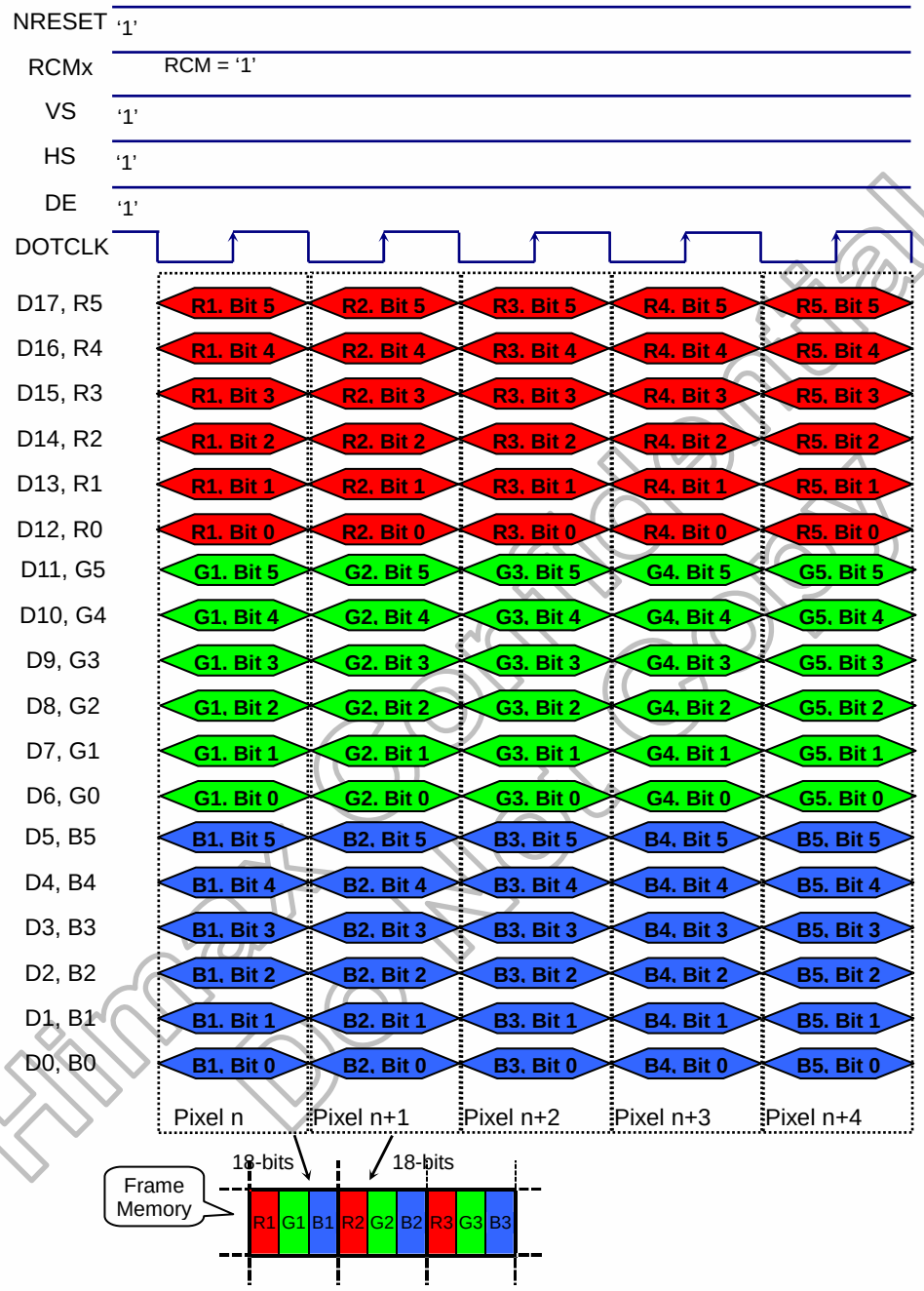
16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input).
There are 1 pixel (3 sub-pixels) per 1 bytes, 65K-colors, 17H="50h"



Note: (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 29 RGB 16-bits/pixel on 16-bits Data width

18-bits/pixel Colors Order on the 18-bits Data width RGB Interface (RGB 6-6-6-bits input). There are 1 pixel (3 sub-pixels) per 1 bytes, 262K-colors, 17H="60h"



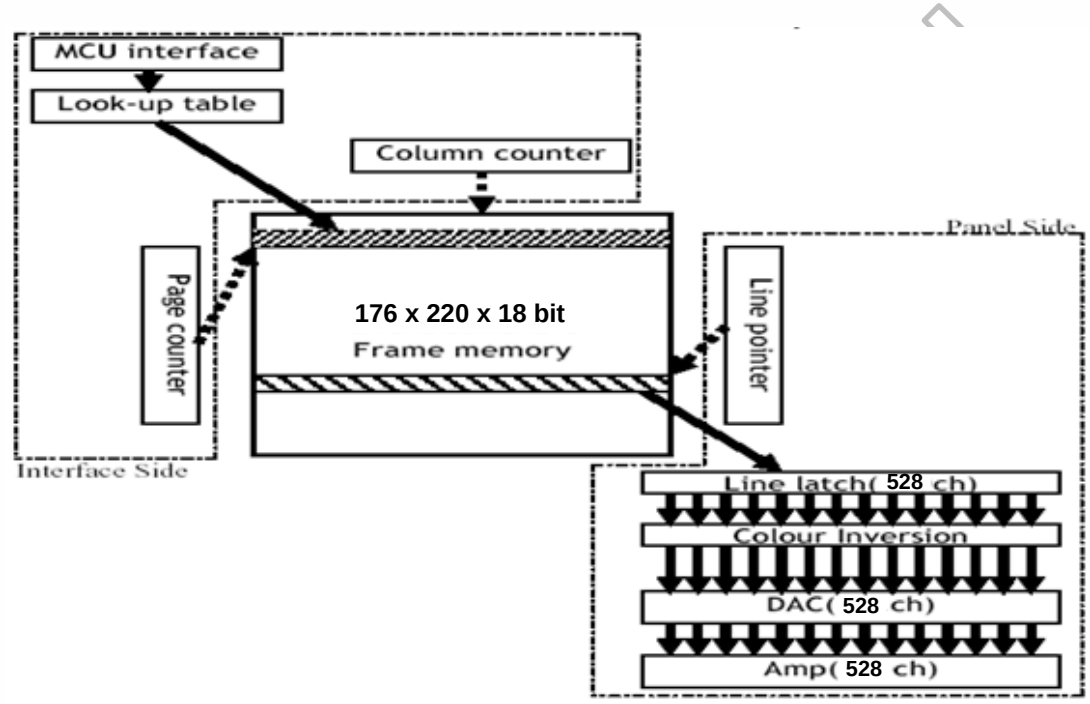
Note: (1) The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 30 RGB 18-bits/pixel on 18-bits Data width

6. Display Data GRAM

The display data RAM stores display dots and consists of 696960 bits (176x18x220 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



6.1 Display Data GRAM Mapping

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

(00,00)H	(00,01)H	(00,02)H	---------	(00,AC)H	(00,AD)H	(00,AE)H	(00,AF)H
(01,00)H	(01,01)H	(01,02)H	---------	(01,AC)H	(01,AD)H	(01,AE)H	(01,AF)H
(02,00)H	(02,01)H	(02,02)H	---------	(02,AC)H	(02,AD)H	(02,AE)H	(02,AF)H
(03,00)H	(03,01)H	(03,02)H	---------	(03,AC)H	(03,AD)H	(03,AE)H	(03,AF)H
(04,00)H	(04,01)H	(04,02)H	---------	(04,AC)H	(04,AD)H	(04,AE)H	(04,AF)H
(05,00)H	(05,01)H	(05,02)H	---------	(05,AC)H	(05,AD)H	(05,AE)H	(05,AF)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(D6,00)H	(D6,01)H	(D6,02)H	---------	(D6,AC)H	(D6,AD)H	(D6,AE)H	(D6,AF)H
(D7,00)H	(D7,01)H	(D7,02)H	---------	(D7,AC)H	(D7,AD)H	(D7,AE)H	(D7,AF)H
(D8,00)H	(D8,01)H	(D8,02)H	---------	(D8,AC)H	(D8,AD)H	(D8,AE)H	(D8,AF)H
(D9,00)H	(D9,01)H	(D9,02)H	---------	(D9,AC)H	(D9,AD)H	(D9,AE)H	(D9,AF)H
(DA,00)H	(DA,01)H	(DA,02)H	---------	(DA,AC)H	(DA,AD)H	(DA,AE)H	(DA,AF)H
(DB,00)H	(DB,01)H	(DB,02)H	---------	(DB,AC)H	(DB,AD)H	(DB,AE)H	(DB,AF)H

Table 6. 1 GRAM Address for Display Panel Position

6.2 Address Counter (AC) of GRAM

The HX8340-B contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the **CASET** (start: **SC**, end: **EC**) and the PASET (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

6.2.1 System Interface to GRAM Write Direction

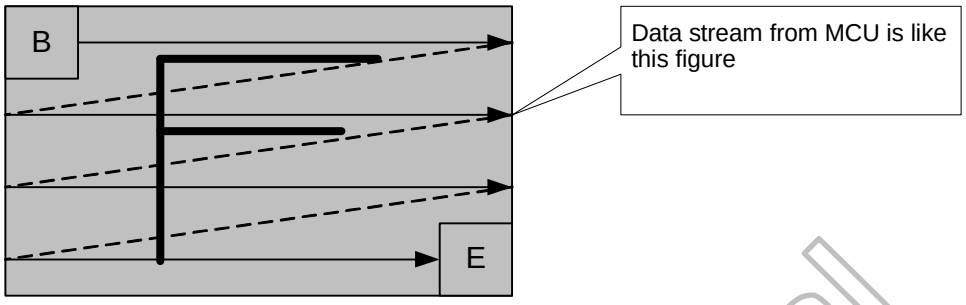


Figure 6. 1 Image Data Sending Order from the Host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits setting

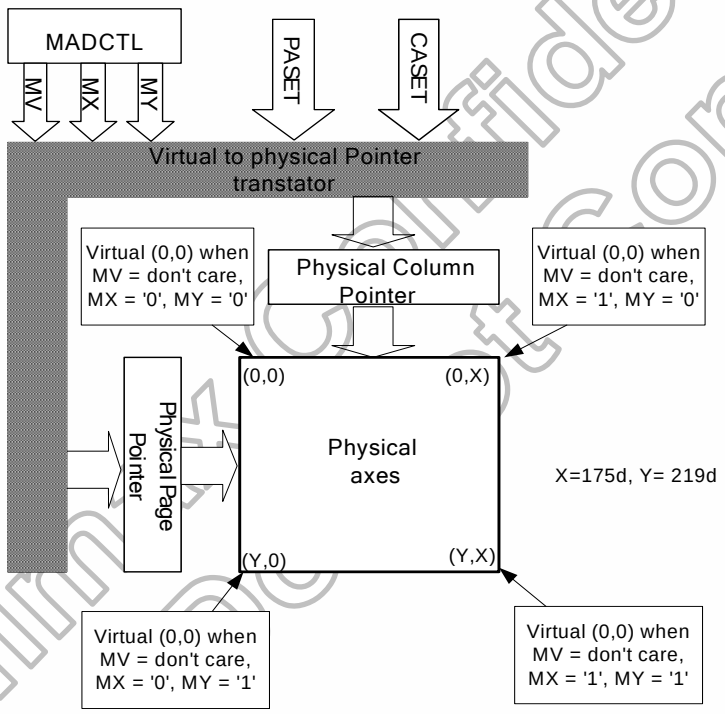


Figure 6. 2 Image Data Writing Control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6. 2 CASET and PASET Control for Physical Column/Page Pointers

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

Table 6. 3 Rules for Updating GRAM Order

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

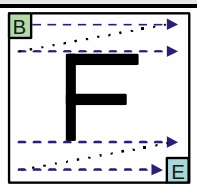
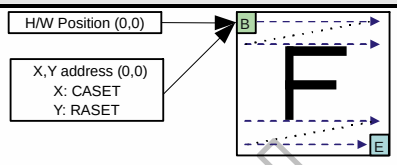
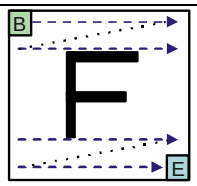
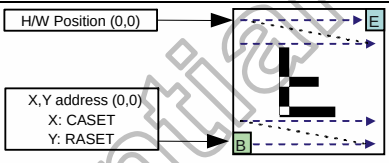
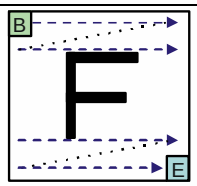
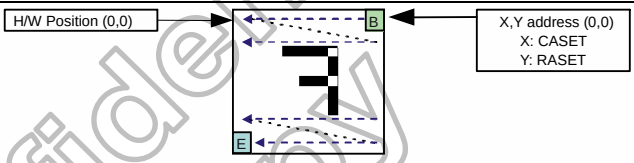
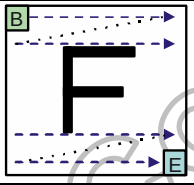
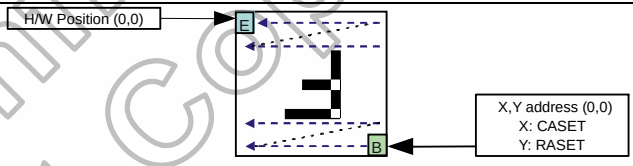
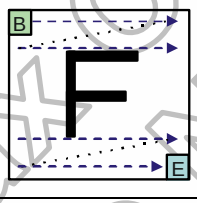
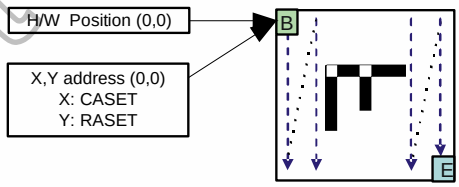
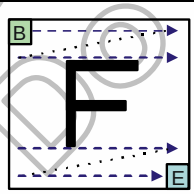
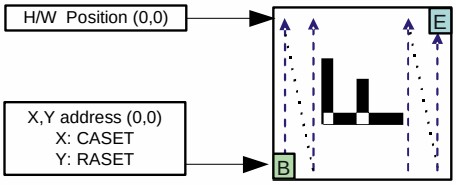
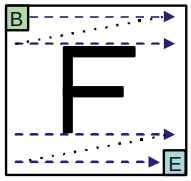
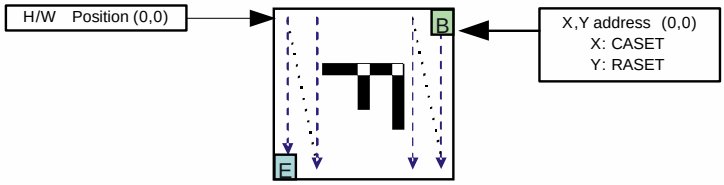
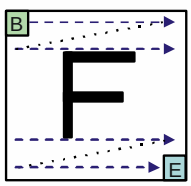
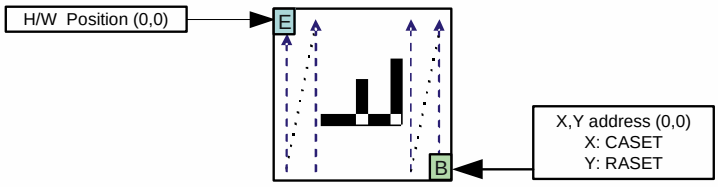
Display Data Direction	MADCTR parameter			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6. 4 Address Direction Settings

Example for rotation with MY, MX and MV

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20 => commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.

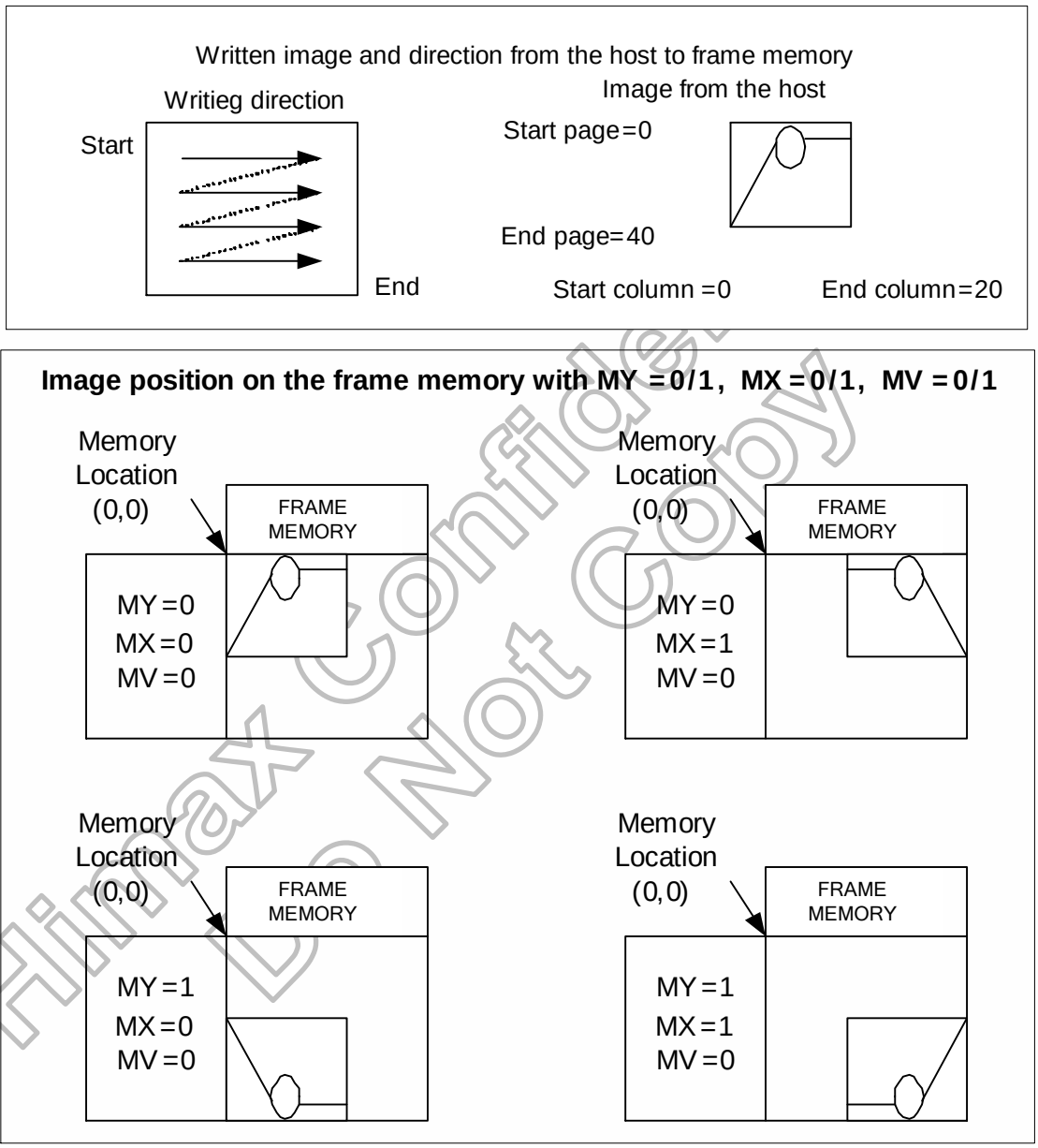
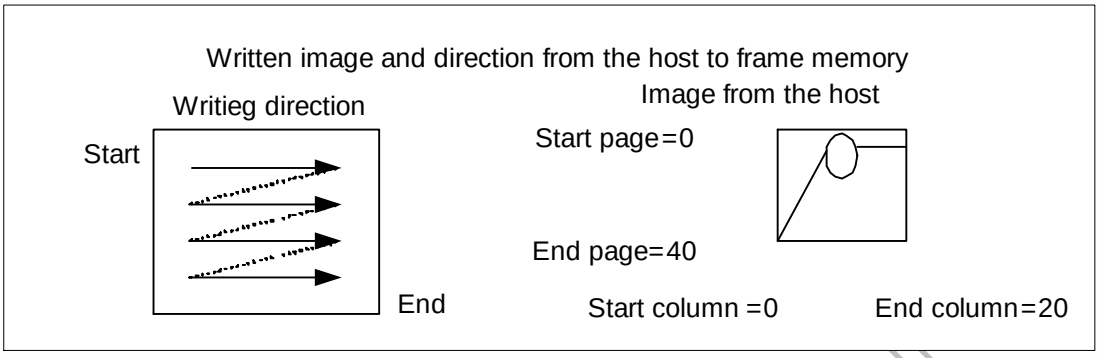


Figure 6. 3 Example for Rotation with MY, MX and MV – 1



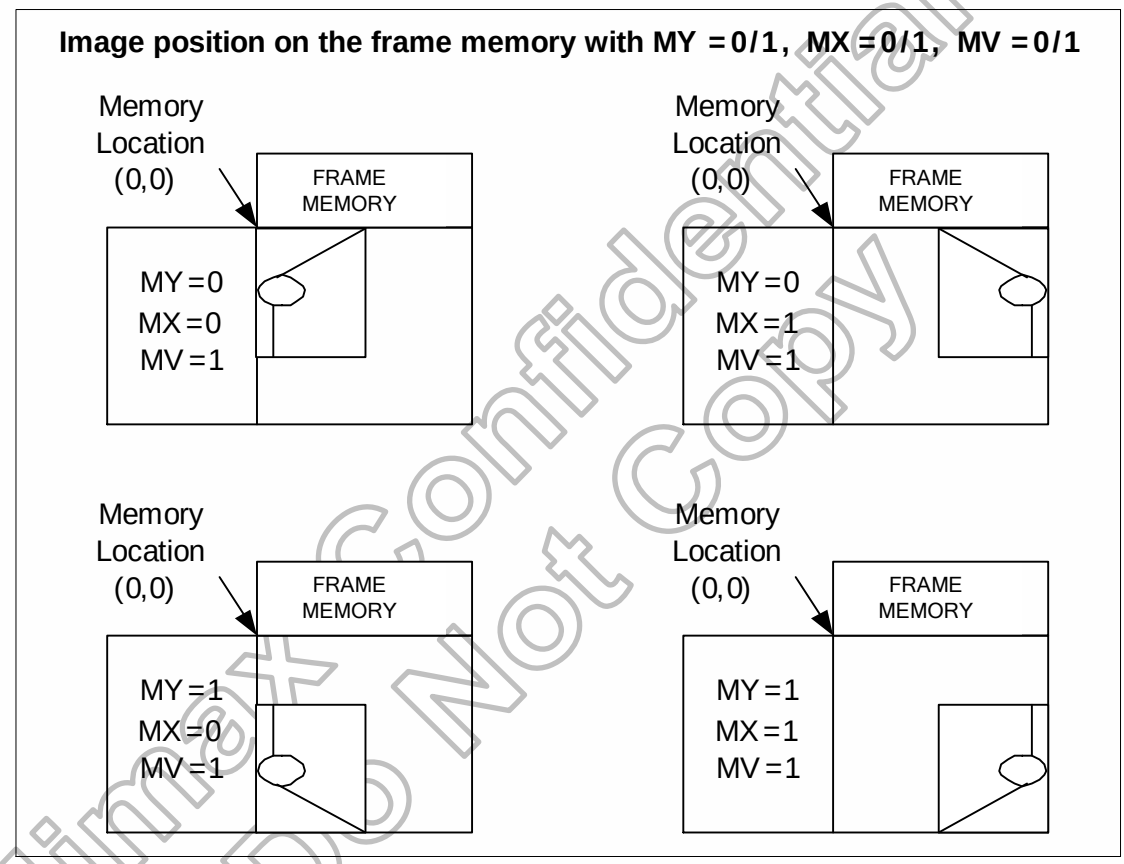


Figure 6. 4 Example for Rotation with MY, MX and MV - 2

6.3 GRAM to Display Address Mapping

By setting the external **SMX** pin, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the external **SMY** pin, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the external **SRGB** pin, the relation between the source output channel and the <
R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 6.5, Table 6.6 and Table 6.7 show the relationship among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

SRGB = 'H'														
Source	**SMX = 'H'**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**-------**	**S523**	**S524**	**S525**	**S526**	**S527**	**S528**
Output	**SMX = 'L'**	**S526**	**S527**	**S528**	**S523**	**S524**	**S525**	**-------**	**S4**	**S5**	**S6**	**S1**	**S2**	**S3**
X Address		"00"h			"01"h			-------	"AE"h			"AF"h		
RGB data		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			------	Pixel 175			Pixel 176		

SRGB = 'L'														
Source	**SMX = 'H'**	**S3**	**S2**	**S1**	**S6**	**S5**	**S4**	**-------**	**S523**	**S524**	**S525**	**S526**	**S527**	**S528**
Output	**SMX = 'L'**	**S528**	**S527**	**S526**	**S525**	**S524**	**S523**	**-------**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		"00"h			"01"h			-------	"AE"h			"AF"h		
Bit Allocation		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 175			Pixel 176		

Note: (1) RGB direction default setting is defined by the hardware pin SRGB.
(2) Register R16h[4](BGR) bit will override the hardware SRGB setting once software was sent to R16h[4](BGR) bit. Hardware pin SRGB control is invalid, and RGB filter order is controlled by R16h[4](BGR) bit.

Table 6. 5 GRAM X Address and Display Panel Position

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
G1	0000h			0001h			0002h			---	00ACh			00ADh			00AEh			00AFh		
G2	0100h			0101h			0102h			---	01ACh			01ADh			01AEh			01AFh		
G3	0200h			0201h			0202h			---	02ACh			02ADh			02AEh			02AFh		
G4	0300h			0301h			0302h			---	03ACh			03ADh			03AEh			03AFh		
G5	0400h			0401h			0402h			---	04ACh			04ADh			04AEh			04AFh		
G6	0500h			0501h			0502h			---	05ACh			05ADh			05AEh			05AFh		
G7	0600h			0601h			0602h			---	06ACh			06ADh			06AEh			06AFh		
G8	0700h			0701h			0702h			---	07ACh			07ADh			07AEh			07AFh		
G9	0800h			0801h			0802h			---	08ACh			08ADh			08AEh			08AFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G211	D200h			D201h			D202h			---	D2ACh			D2ADh			D2AEh			D2AFh		
G212	D300h			D301h			D302h			---	D3ACh			D3ADh			D3AEh			D3AFh		
G213	D400h			D401h			D402h			---	D4ACh			D4ADh			D4AEh			D4AFh		
G214	D500h			D501h			D502h			---	D5ACh			D5ADh			D5AEh			D5AFh		
G215	D600h			D601h			D602h			---	D6ACh			D6ADh			D6AEh			D6AFh		
G216	D700h			D701h			D702h			---	D7ACh			D7ADh			D7AEh			D7AFh		
G217	D800h			D801h			D802h			---	D8ACh			D8ADh			D8AEh			D8AFh		
G218	D900h			D901h			D902h			---	D9ACh			D9ADh			D9AEh			D9AFh		
G219	DA00h			DA01h			DA02h			---	DAACh			DAADh			DAAEh			DAAFh		
G220	DB00h			DB01h			DB02h			---	DBACh			DBADh			DBAEh			DBAFh		

Table 6. 6 GRAM Address and Display Panel Position (SMY ='L')

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
G220	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G219	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G218	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G217	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G216	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G215	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G214	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G213	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G212	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	D200h			D201h			D202h			---	D2ACh			D2ADh			D2AEh			D2AFh		
G9	D300h			D301h			D302h			---	D3ACh			D3ADh			D3AEh			D3AFh		
G8	D400h			D401h			D402h			---	D4ACh			D4ADh			D4AEh			D4AFh		
G7	D500h			D501h			D502h			---	D5ACh			D5ADh			D5AEh			D5AFh		
G6	D600h			D601h			D602h			---	D6ACh			D6ADh			D6AEh			D6AFh		
G5	D700h			D701h			D702h			---	D7ACh			D7ADh			D7AEh			D7AFh		
G4	D800h			D801h			D802h			---	D8ACh			D8ADh			D8AEh			D8AFh		
G3	D900h			D901h			D902h			---	D9ACh			D9ADh			D9AEh			D9AFh		
G2	DA00h			DA01h			DA02h			---	DAACh			DAADh			DAAEh			DAAFh		
G1	DB00h			DB01h			DB02h			---	DBACh			DBADh			DBAEh			DBAFh		

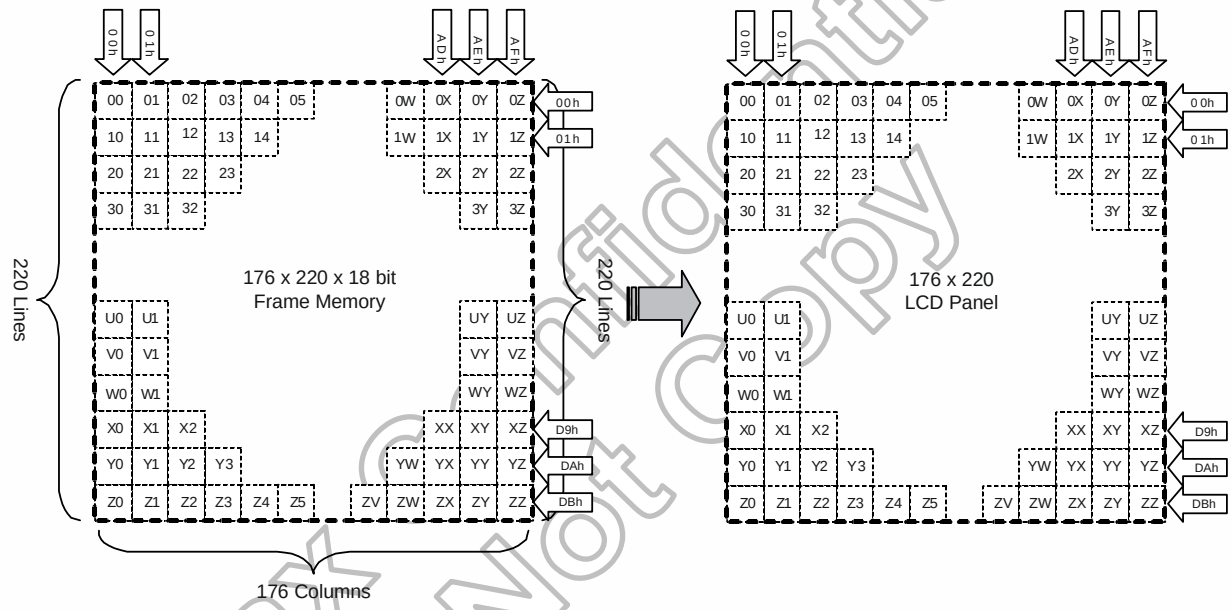
Table 6. 7 GRAM Address and Display Panel Position (SMY ='H')

HX8340-B supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

When the **PLTON** is set '0', HX8340-B will be into Normal Display Mode. When the **PLTON** is set '1', HX8340-B will be into Partial Display Mode.

6.3.1 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00AFh and page pointer is 0000h to 00DBh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0) (**SMX** = 'L', **SMY** = 'L').



Example:

(1) **PLTON** ='1',

(2) R30h's SR=11_{DEC}, ER=130_{DEC}, MADCTL's B4(ML)='0' (**SMY** = 'L').

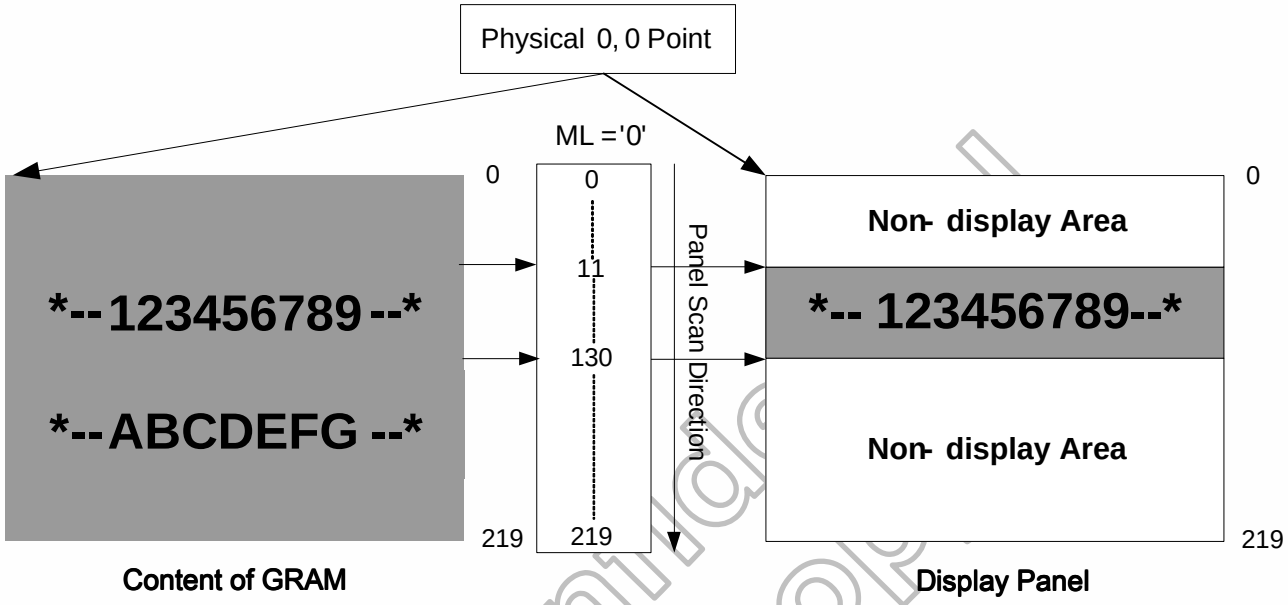


Figure 6. 5 Example of Partial Mode on (ML='0')

Example:

(1) **PLTON** ='1',

(2) R30h's SR= 11_{DEC}, ER=130_{DEC}, MADCTL's B4(ML)='1' (**SMY** = 'L').

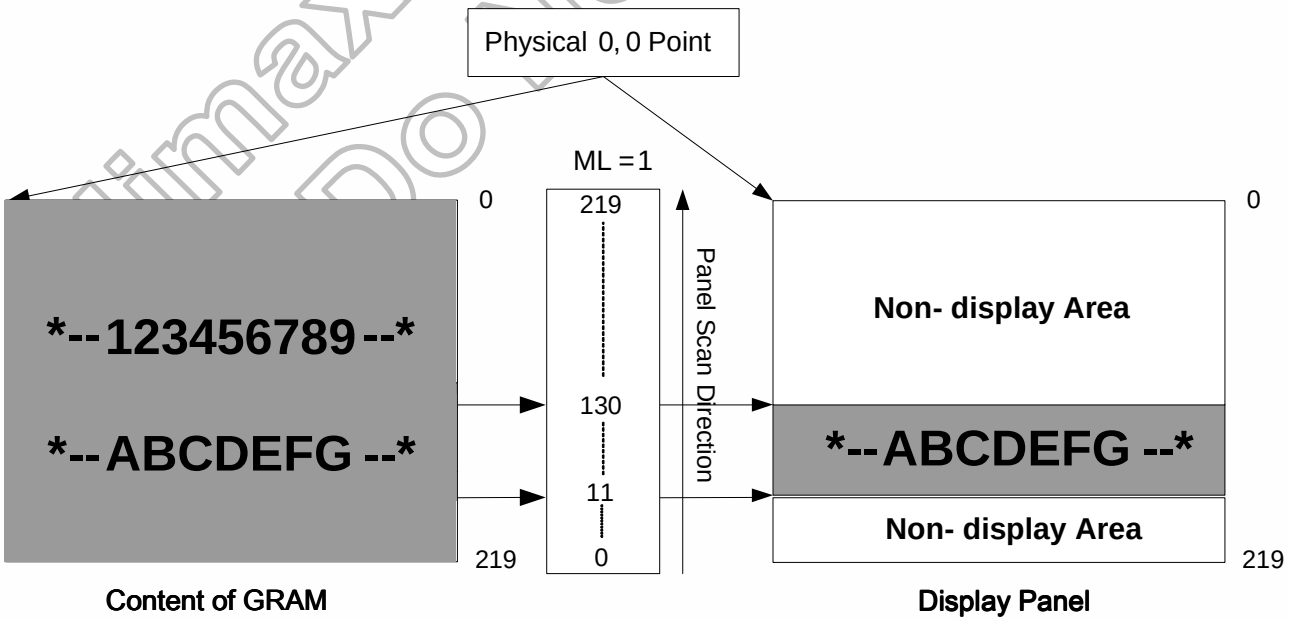


Figure 6. 6 Example of Partial Mode on (ML='1')

The refresh gate scan cycle in the rest display area of the screen (non-display area) can be specified by **ISC[3:0]** bits. The scan cycle is set to an odd number from 0~13.The polarity is inverted every scan cycle. Refresh gate scan cycle is related to the power consumption. Lower power for higher scan rate.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

Table 6. 8 ISC[3:0] Bits Definition

The rest display area (non-display area) will be the white display if the type of LCD is normally white (**NWB** = “1”) and will be the black display if the type of LCD is normally black (**NWB** = “0”) in refresh gate scan cycle.

6.3.2 Vertical Scroll Display Mode

The vertical scrolling display is specified by VSCRDEF instruction (R0Eh~R13h) and VSCRSADD instruction (R14h~R15h).

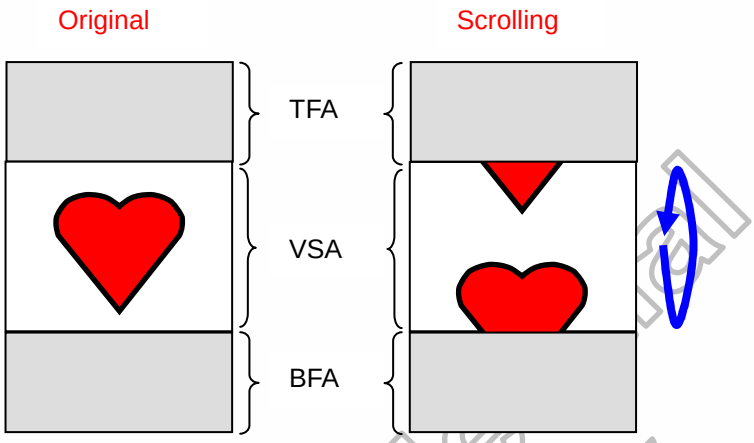


Figure 6. 7 Vertical Scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=220. In this case, scrolling is applied as shown below.

Example (1) TFA='2d', VSA='218d', BFA='0d', VSP='3d' when MADCTL B4 (**ML**)=0
(**SMX** = 'L', **SMY** = 'L').

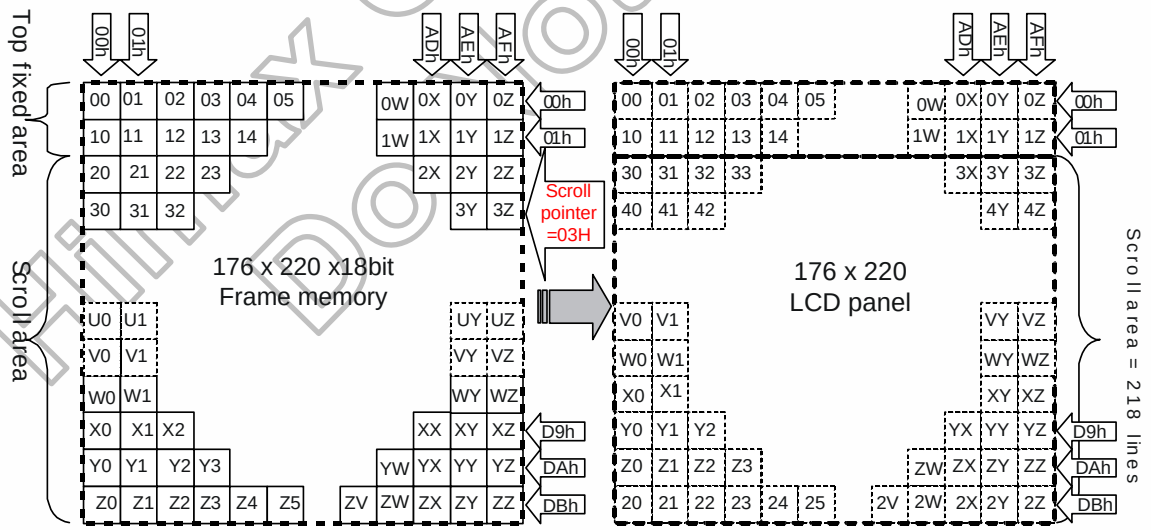


Figure 6. 8 Memory Map of Vertical Scrolling I

Example (2) TFA=’2d’, VSA=’216d’, BFA=’2d’, VSP=’3d’ when MADCTL B4 (**ML**)=0 (**SMX** = ‘L’, **SMY** = ‘L’).

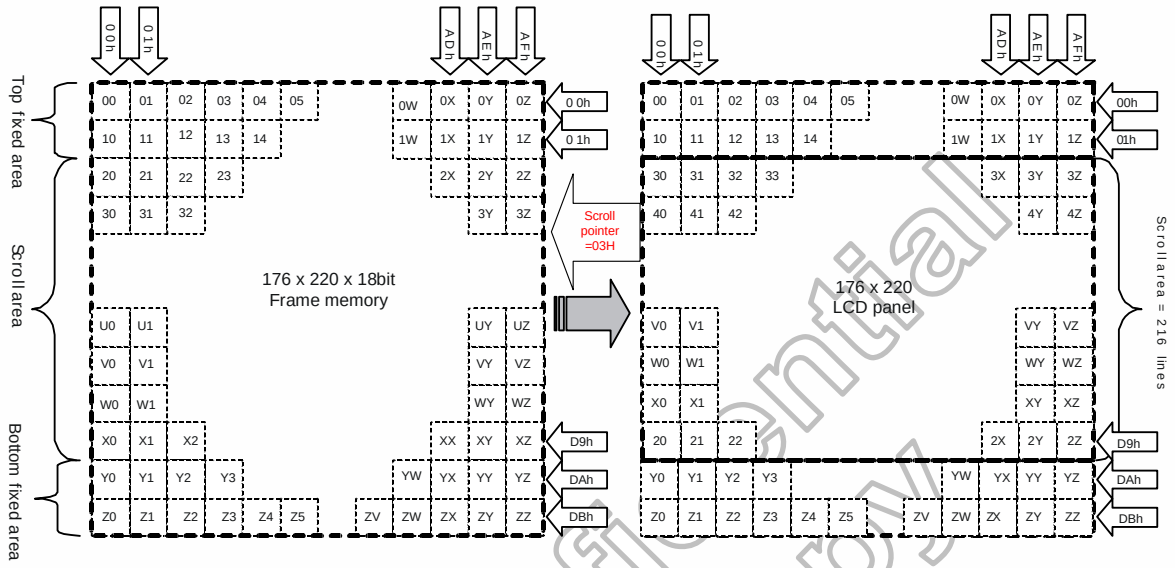


Figure 6. 9 Memory Map of Vertical Scrolling II

Example (3) TFA=’2d’, VSA=’216d’, BFA=’2d’, VSP=’5d’ when MADCTL B4 (**ML**)=0 (**SMX** = ‘L’, **SMY** = ‘L’).

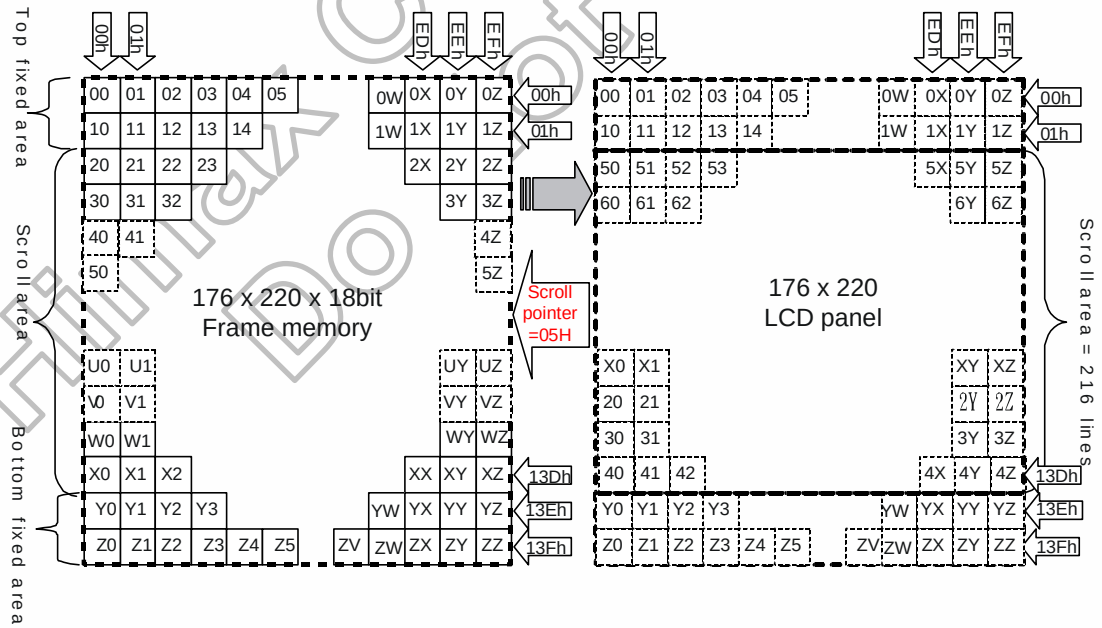


Figure 6. 10 Memory Map of Vertical Scrolling III

Vertical Scroll Example

There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA ≠ ‘220d’
N/A. Do not set TFA + VSA + BFA ≠‘220d’. In that case, unexpected picture will be shown.
Case 2: TFA + VSA + BFA= ‘20d’ (Scrolling)
Example (1) When TFA=’0d’, VSA=’220d’, BFA=’0d’ and VSP=’40d’, MADCTL parameter B4(**ML**)=’0’

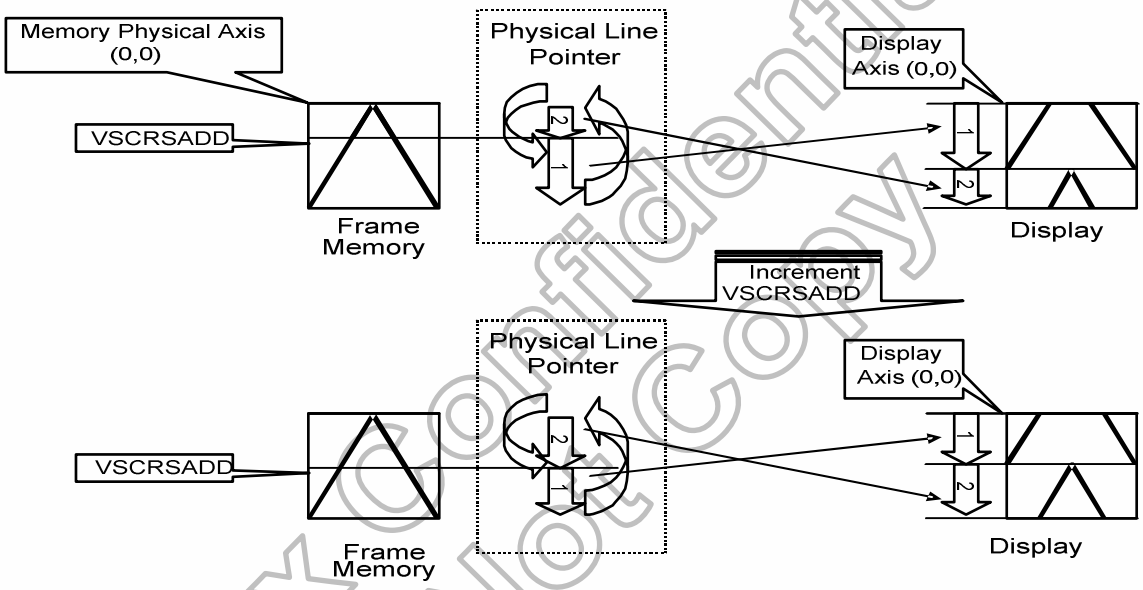


Figure 6. 11 Vertical Scroll Example when ML=’0’

Example (2) TFA=’30d’, VSA=’190d’, BFA=’0d’ and VSP=’80d’, MADCTRL parameter B4(**ML**) = ’**1’**

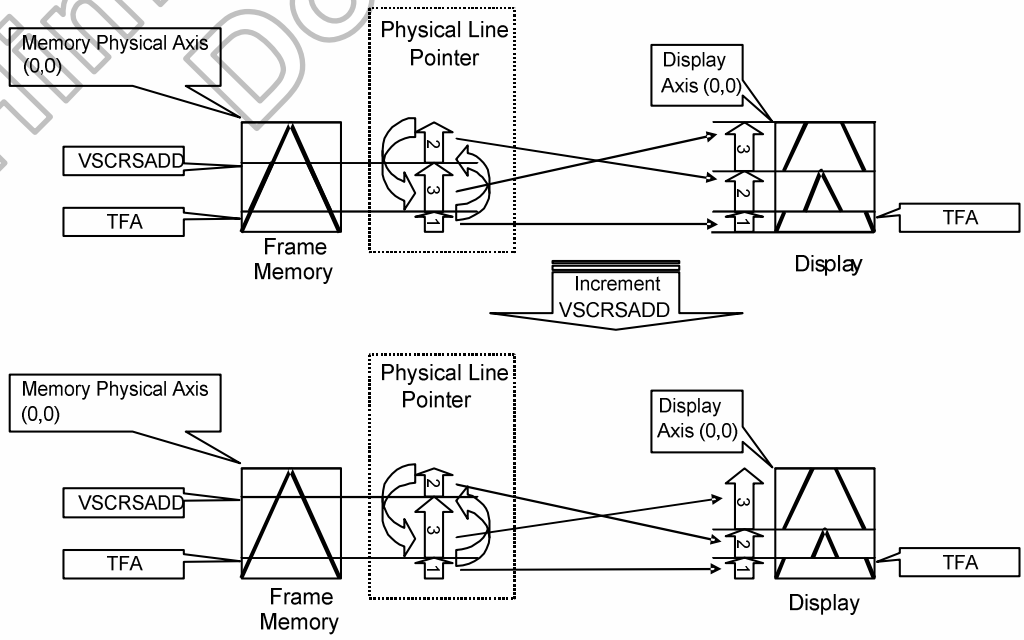


Figure 6. 12 Vertical Scroll Example when ML=’1’

6.3.3 Updating Order on Display Active Area in RGB Interface Mode (Normal Mode On + Sleep Out)

There is defined different kind of updating orders for display in RGB interface mode (**RCM[1:0] = '10' or '11'**). These updating are controlled by external RL pin internal CRL bit based on external SMX pin setting and external TB pin/ internal CTB bit based on external SMY pin setting.

Please note that as internal CRL bit be written in RGB interface, the external pin RL control is invalid, and CRL is operated based on external pin SMX setting. As internal CTB bit be written in RGB interface, the external pin TB control is invalid, and CRL is operated based on external pin SMY setting.

Data streaming direction from the host to the display is described in the following figure.

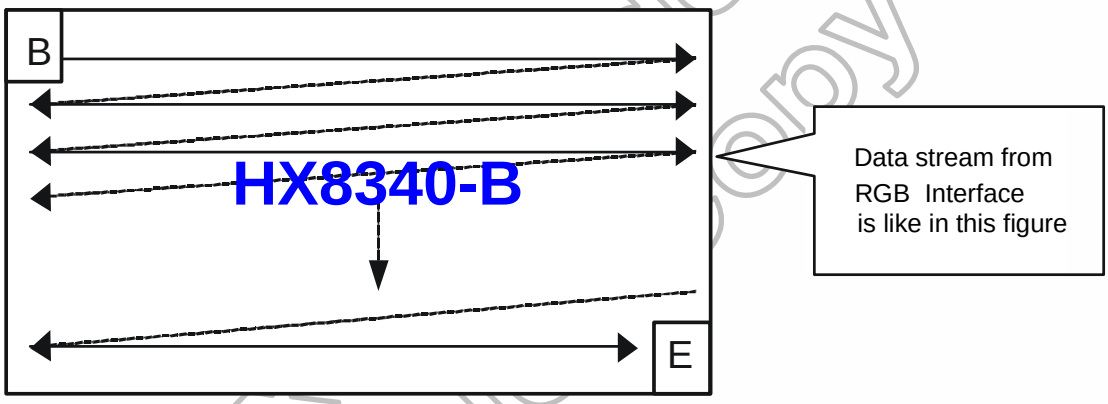


Figure 6. 13 Data Streaming Order in RGB I/F

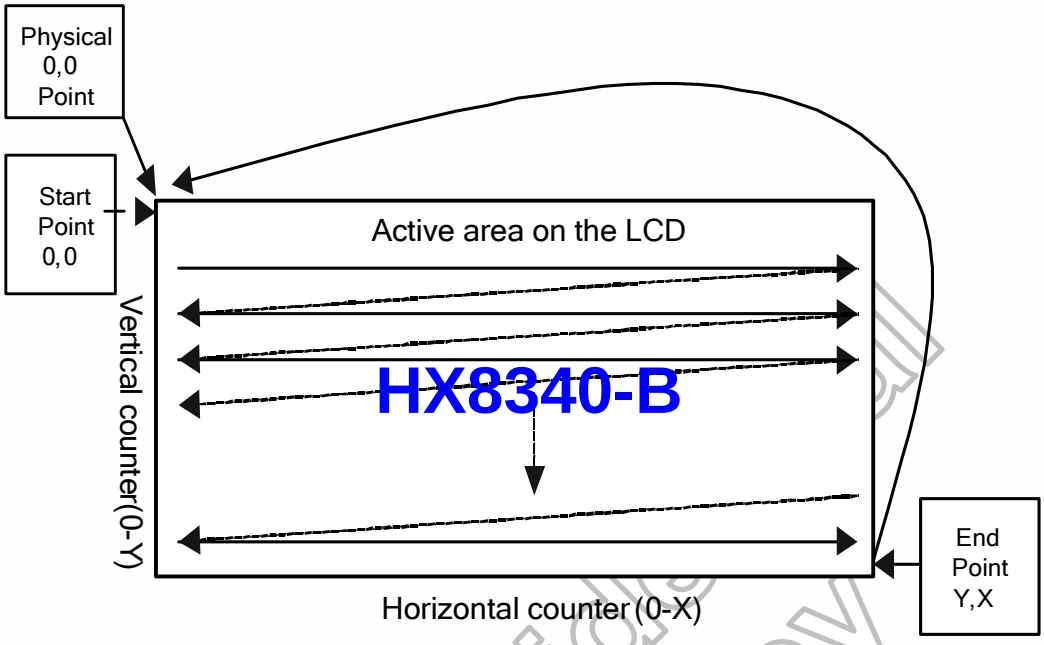


Figure 6. 14 Updating Order when TB = 'L' and RL = 'L'

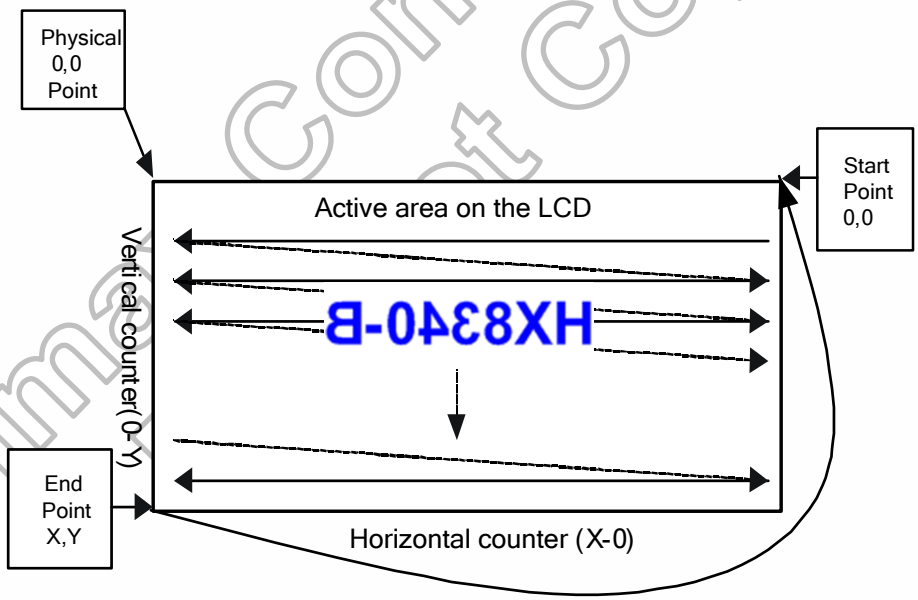


Figure 6. 15 Updating Order when TB = 'L' and RL = 'H'

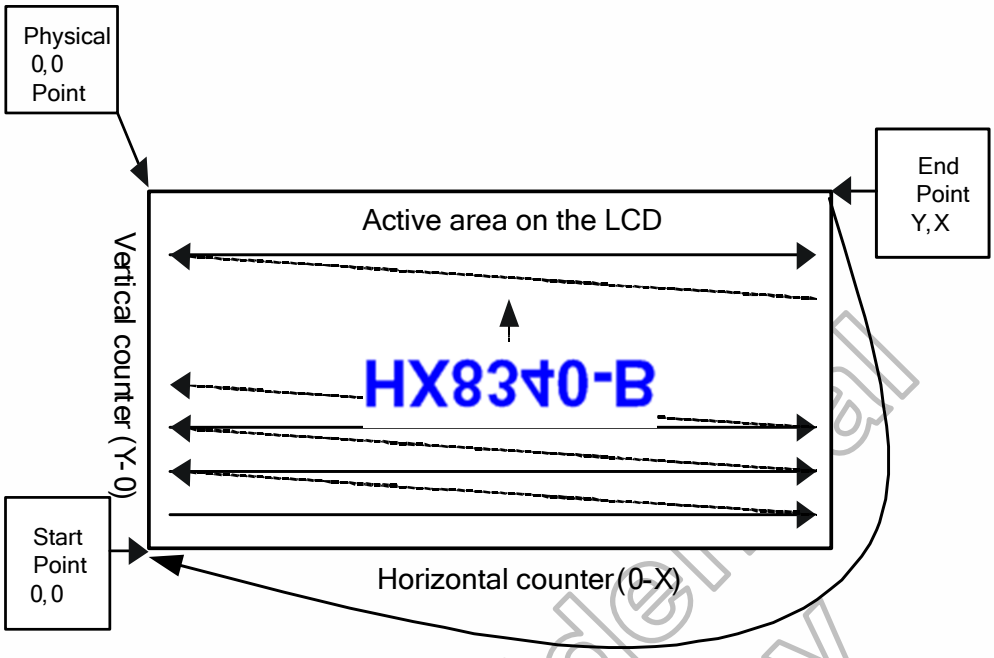


Figure 6. 16 Updating Order when TB = 'H' and RL = 'L'

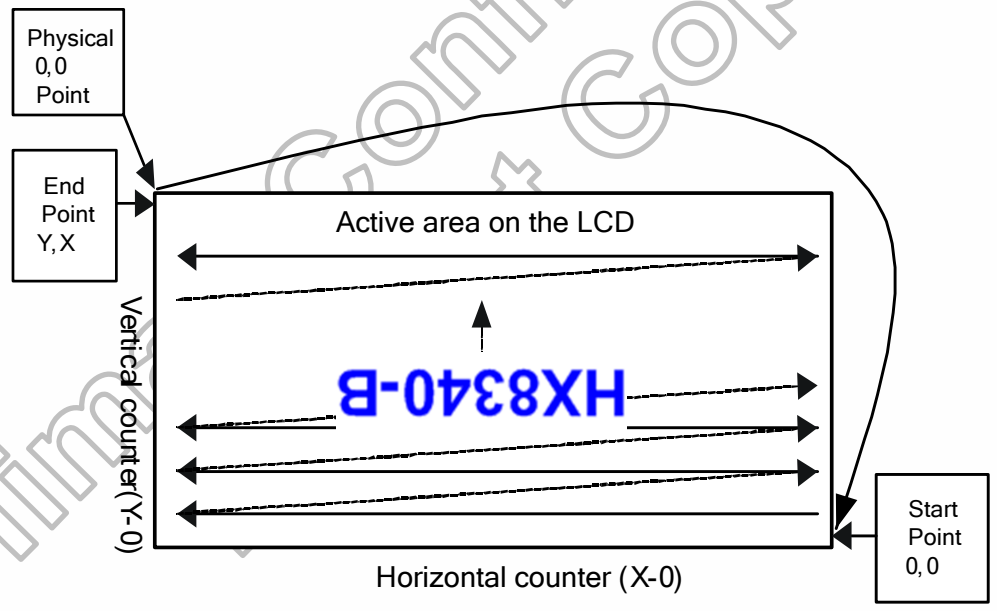


Figure 6. 17 Updating Order when TB = 'H' and RL = 'H'

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

Table 6. 9 Rules for Updating Order on Display Active Area in RGB Interface Display Mode

7. Functional Description

7.1 Internal Oscillator

The HX8340-B can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, it can be adjusted for initial 2.52MHz internal clock generation. With other dividers setting, the 2.52MHz internal clock can be used to generate clock for other part of the chip using.

In RGB interface mode (RCM[1:0] = '10' or '11'), external DOTCLK will be replace the internal clock for other part of the chip using.

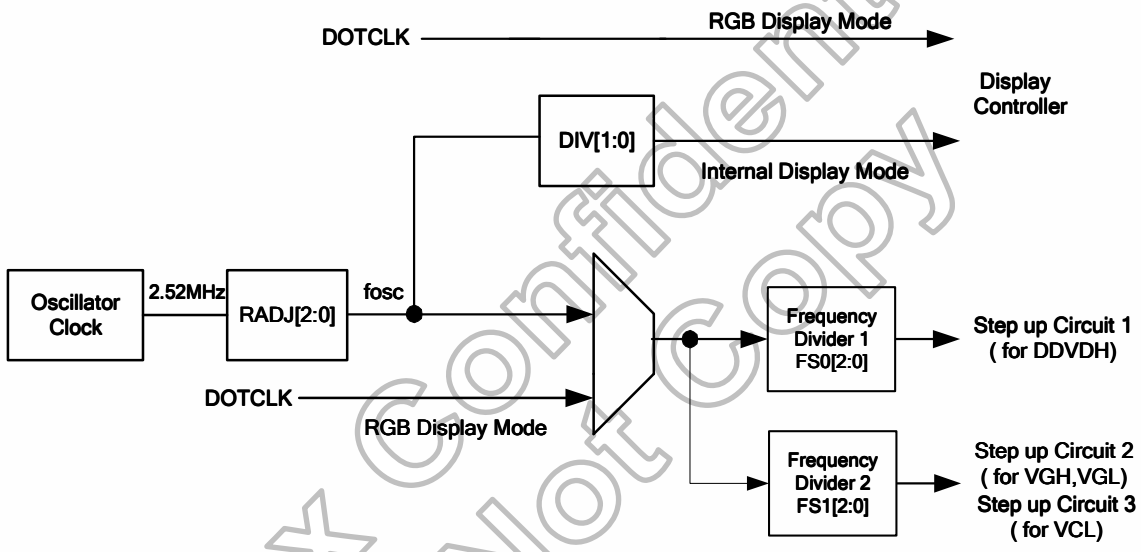


Figure 7. 1 HX8340-B Internal Clock Circuit

7.2 Gamma Characteristic Correction Function

The HX8340-B incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

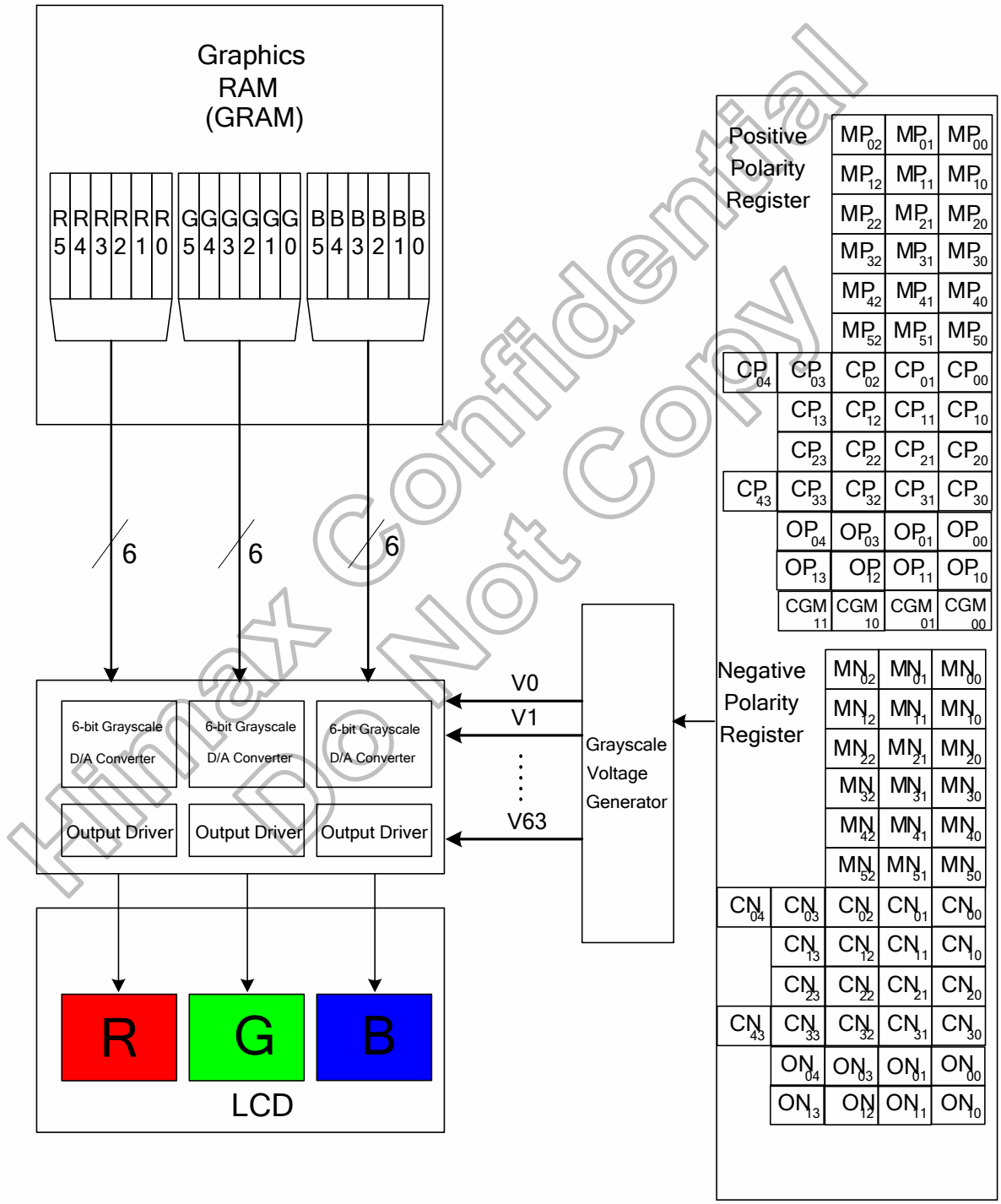


Figure 7. 2 Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages (RVP 0, 1, 8, 20, 43, 55, 62 and 63). For positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

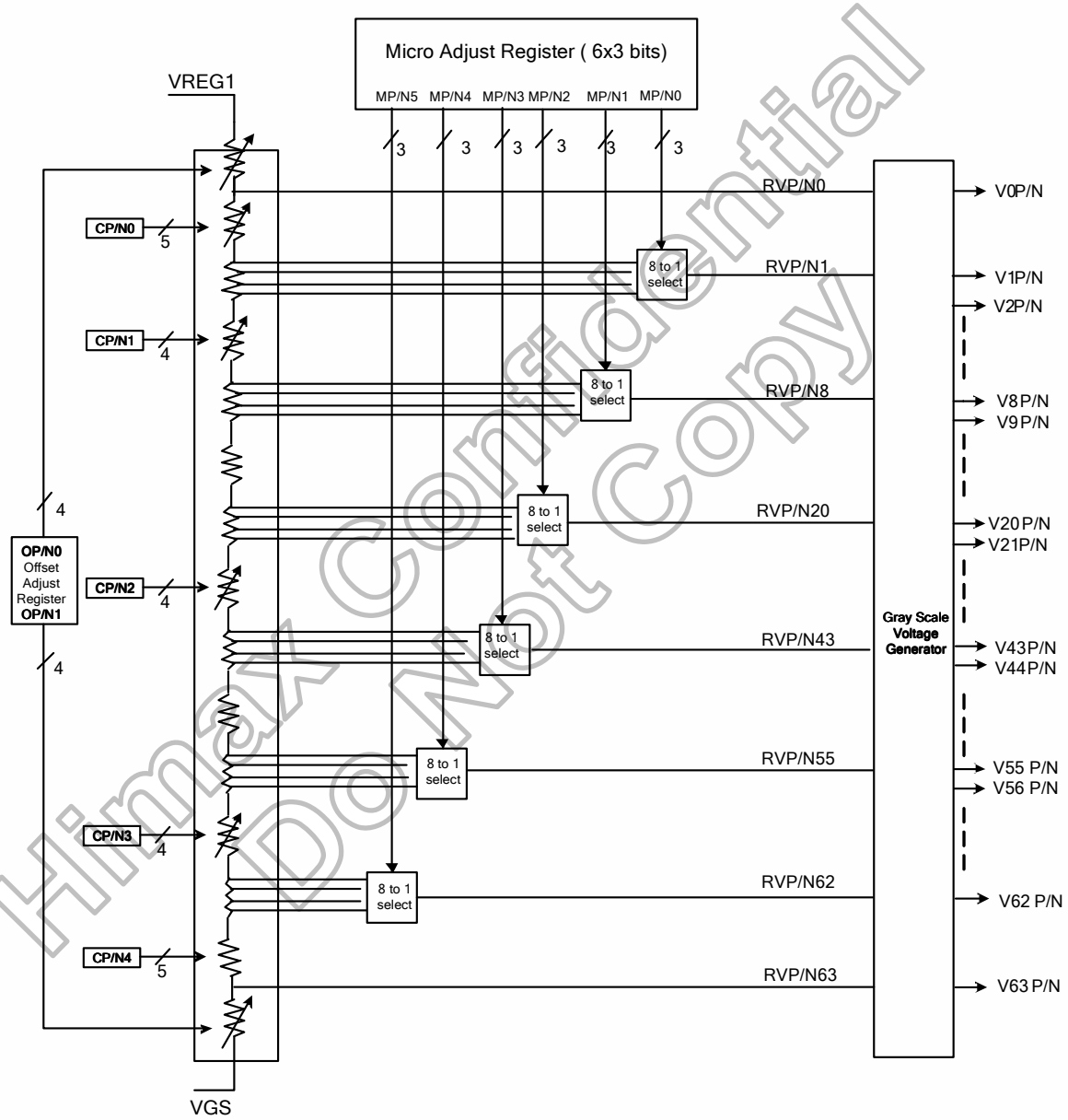


Figure 7. 3 Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This HX8343-B has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics.

(A) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

(B) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(C) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (RVP/N 0, 1, 8, 20, 44, 56, 63, 64). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Description
Center Adjustment	CP/N0 4-0	Variable resistor (VRTP/N) for center adjustment
	CP/N1 3-0	Variable resistor (VRCP/N0)for center adjustment
	CP/N2 3-0	Variable resistor (VRMP/N) for center adjustment
	CP/N3 3-0	Variable resistor (VRCP/N1)for center adjustment
	CP/N4 4-0	Variable resistor (VRBP/N)for center adjustment
Macro Adjustment	MP/N0 2-0	8-to-1 selector (reference voltage level of grayscale 1)
	MP/N1 2-0	8-to-1 selector (reference voltage level of grayscale 8)
	MP/N2 2-0	8-to-1 selector (reference voltage level of grayscale 20)
	MP/N3 2-0	8-to-1 selector (reference voltage level of grayscale 43)
	MP/N4 2-0	8-to-1 selector (reference voltage level of grayscale 55)
	MP/N5 2-0	8-to-1 selector (reference voltage level of grayscale 62)
Offset Adjustment	OP/N0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP/N1 3-0	Variable resistor (VROP/N1)for offset adjustment

Table 7. 1 Gamma-Adjustment Registers

Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (RVP/N 0, 1, 8, 20, 43, 55, 62 63)

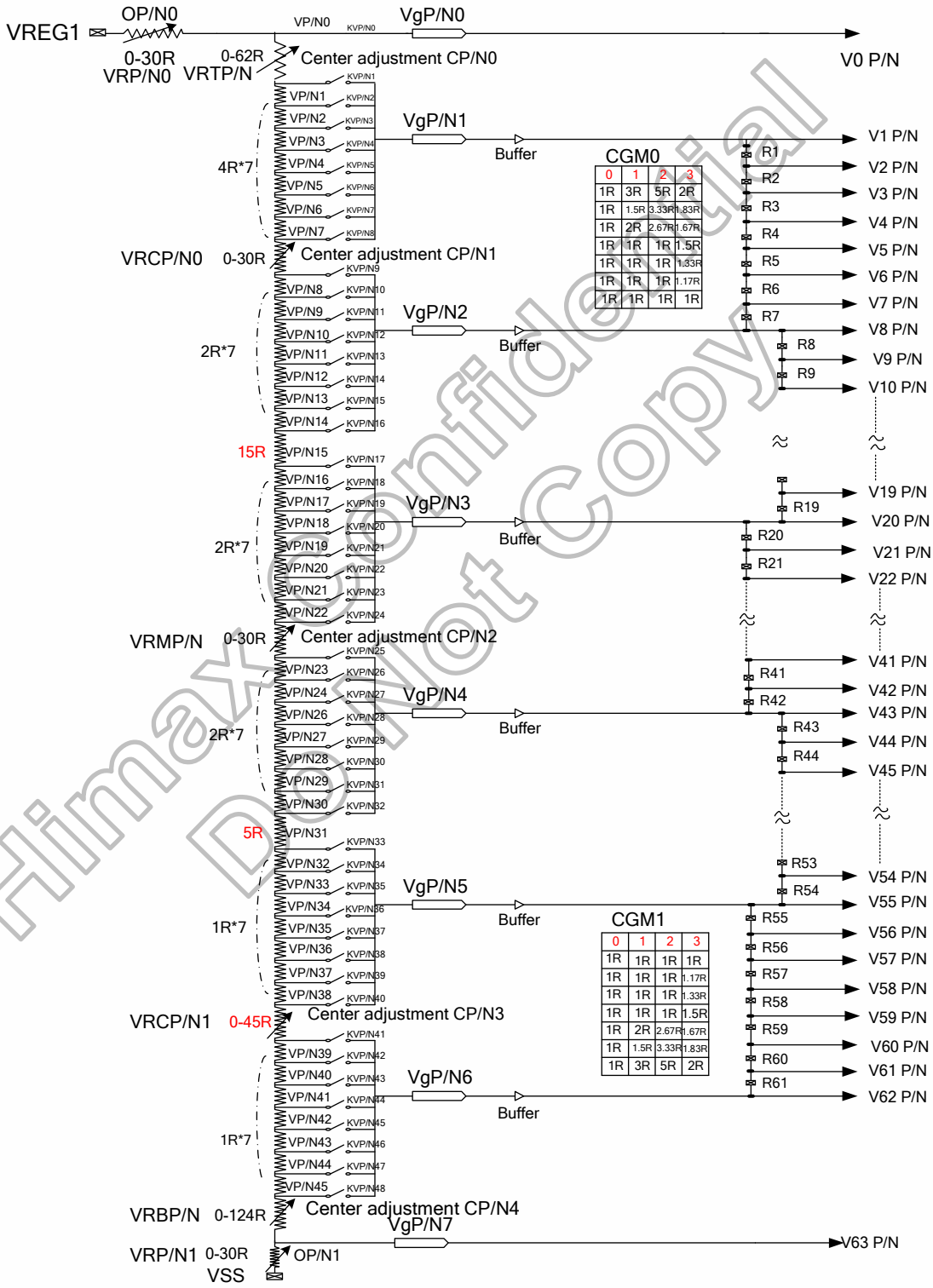


Figure 7. 4 Gamma Resister Stream and Gamma Reference Voltage

Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register OP/N0 3-0	Resistance VRP/N0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 7. 2 Offset Adjustment 0

Value in Register OP/N1 3-0	Resistance VRP/N1
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 7. 3 Offset Adjustment 1

Value in Register CP/N0 4-0	Resistance VRTP/N0	Value in Register CP/N4 4-0	Resistance VRBP/N	Value in Register CP/N1(2) 3-0	Resistance VRCP/N0 VRMP/N
00000	0R	00000	0R	0000	0R
00001	2R	00001	4R	0001	2R
00010	4R	00010	8R	0010	4R
•	•	•	•	•	•
•	•	•	•	•	•
11100	56R	11100	112R	1100	24R
11101	58R	11101	116R	1101	26R
11110	60R	11110	120R	1110	28R
11111	62R	11111	124R	1111	30R

Value in Register CP/N3 3-0	Resistance VRCP/N1
0000	0R
0001	3R
0010	6R
•	•
•	•
1100	36R
1101	39R
1110	42R
1111	45R

Table 7. 4 Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationships are shown below.

Value in Register	Voltage level					
MP/N 2-0	VgP/N 1	VgP/N 2	VgP/N 3	VgP/N 4	VP/N 5	VP/N 6
000	KVP/N1	KVP/N9	KVP/N17	KVP/N25	KVP/N33	KVP/N41
001	KVP/N 2	KVP/N10	KVP/N18	KVP/N26	KVP/N34	KVP/N42
010	KVP/N3	KVP/N11	KVP/N19	KVP/N27	KVP/N35	KVP/N43
011	KVP/N 4	KVP/N12	KVP/N20	KVP/N28	KVP/N36	KVP/N44
100	KVP/N 5	KVP/N13	KVP/N21	KVP/N29	KVP/N37	KVP/N45
101	KVP/N 6	KVP/N14	KVP/N22	KVP/N30	KVP/N38	KVP/N46
110	KVP/N 7	KVP/N15	KVP/N23	KVP/N31	KVP/N39	KVP/N47
111	KVP/N 8	KVP/N16	KVP/N24	KVP/N32	KVP/N40	KVP/N48

Table 7. 5 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas.

Reference Voltage	Formula		Pin
VgP/N0	----	VREG1-VD*VRP/N0 /sumRP/N	KVP/N0
VgP/N1	MP/N0 2-0=000	VREG1 –VD((VRP/N0+VRTP/N) /sumRP/N	KVP/N1
	MP/N0 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N +4R) /sumRP/N	KVP/N2
	MP/N0 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N +8R) /sumRP/N	KVP/N3
	MP/N0 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N +12R) /sumRP/N	KVP/N4
	MP/N0 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N +16R) /sumRP/N	KVP/N5
	MP/N0 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N +20R) /sumRP/N	KVP/N6
	MP/N0 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N +24R) /sumRP/N	KVP/N7
	MP/N0 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N +28R) /sumRP/N	KVP/N8
VgP/N2	MP/N1 2-0=000	VREG1 –VD((VRP/N0+ VRTP/N +28R+VRCP/N0) /sumRP/N	KVP/N9
	MP/N1 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N +30R+VRCP/N0) /sumRP/N	KVP/N10
	MP/N1 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N +32R+VRCP/N0) /sumRP/N	KVP/N11
	MP/N1 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N +34R+VRCP/N0) /sumRP/N	KVP/N12
	MP/N1 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N +36R+VRCP/N0) /sumRP/N	KVP/N13
	MP/N1 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N +38R+VRCP/N0) /sumRP/N	KVP/N14
	MP/N1 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N +40R+VRCP/N0) /sumRP/N	KVP/N15
	MP/N1 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N +42R+VRCP/N0) /sumRP/N	KVP/N16
VgP/N3	MP/N2 2-0=000	VREG1 –VD((VRP/N0+ VRTP/N+57R+VRCP/N0) /sumRP/N	KVP/N17
	MP/N2 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N+59R+VRCP/N0) /sumRP/N	KVP/N18
	MP/N2 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N+61R+VRCP/N0) /sumRP/N	KVP/N19
	MP/N2 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N+63R+VRCP/N0) /sumRP/N	KVP/N20
	MP/N2 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N+65R+VRCP/N0) /sumRP/N	KVP/N21
	MP/N2 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N+67R+VRCP/N0) /sumRP/N	KVP/N22
	MP/N2 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N+69R+VRCP/N0) /sumRP/N	KVP/N23
	MP/N2 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N+71R+VRCP/N0) /sumRP/N	KVP/N24
VgP/N4	MP/N3 2-0=000	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +71R+VRCP/N0) /sumRP/N	KVP/N25
	MP/N3 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +73R+VRCP/N0) /sumRP/N	KVP/N26
	MP/N3 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +75R+VRCP/N0) /sumRP/N	KVP/N27
	MP/N3 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +77R+VRCP/N0) /sumRP/N	KVP/N28
	MP/N3 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +89R+VRCP/N0) /sumRP/N	KVP/N29
	MP/N3 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +81R+VRCP/N0) /sumRP/N	KVP/N30
	MP/N3 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +83R+VRCP/N0) /sumRP/N	KVP/N31
	MP/N3 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +85R+VRCP/N0) /sumRP/N	KVP/N32
VgP/N5	MP/N4 2-0=000	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +90R+VRCP/N0) /sumRP/N	KVP/N33
	MP/N4 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +91R+VRCP/N0) /sumRP/N	KVP/N34
	MP/N4 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +92R+VRCP/N0) /sumRP/N	KVP/N35
	MP/N4 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +93R+VRCP/N0) /sumRP/N	KVP/N36
	MP/N4 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +94R+VRCP/N0) /sumRP/N	KVP/N37
	MP/N4 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +95R+VRCP/N0) /sumRP/N	KVP/N38
	MP/N4 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +96R+VRCP/N0) /sumRP/N	KVP/N39
	MP/N4 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +97R+VRCP/N0) /sumRP/N	KVP/N40
VgP/N6	MP/N5 2-0=000	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N+97R+VRCP/N0 +VRCP/N1) /sumRP/N	KVP/N41
	MP/N5 2-0=001	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +98R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N42
	MP/N5 2-0=010	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +99R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N43
	MP/N5 2-0=011	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +100R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N44
	MP/N5 2-0=100	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +101R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N45
	MP/N5 2-0=101	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +102R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N46
	MP/N5 2-0=110	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +103R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N47
	MP/N5 2-0=111	VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +104R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N48
VgP/N7	----	VREG1 –VD((VRP/N0+ VRBP/N+ VRTP/N+ VRMP/N +104R+VRCP/N0+VRCP/N1) /sumRP/N	KVP/N49

SumRP=104R+VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
SumRN=104R+ VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
VD=(VREG1–VSS)

Table 7. 6 Voltage Calculation Formula

Grayscale Voltage	Formula
V0P/N	VgP/N0
V1 P/N	VgP/N1
V2 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT1
V3 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT2
V4 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT3
V5 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT4
V6 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT5
V7 P/N	VgP/N2+(VgP/N1-VgP/N2)*CT6
V8 P/N	VgP/N2
V9 P/N	VgP/N3+(VgP/N2-VgP/N3)*(22/24)
V10 P/N	VgP/N3+(VgP/N2-VgP/N3)*(20/24)
V11 P/N	VgP/N3+(VgP/N2-VgP/N3)*(18/24)
V12 P/N	VgP/N3+(VgP/N2-VgP/N3)*(16/24)
V13 P/N	VgP/N3+(VgP/N2-VgP/N3)*(14/24)
V14 P/N	VgP/N3+(VgP/N2-VgP/N3)*(12/24)
V15 P/N	VgP/N3+(VgP/N2-VgP/N3)*(10/24)
V16 P/N	VgP/N3+(VgP/N2-VgP/N3)*(8/24)
V17 P/N	VgP/N3+(VgP/N2-VgP/N3)*(6/24)
V18 P/N	VgP/N3+(VgP/N2-VgP/N3)*(4/24)
V19 P/N	VgP/N3+(VgP/N2-VgP/N3)*(2/24)
V20 P/N	VgP/N3
V21 P/N	VgP/N4+(VgP/N3-VgP/N4)*(22/23)
V22 P/N	VgP/N4+(VgP/N3-VgP/N4)*(21/23)
V23 P/N	VgP/N4+(VgP/N3-VgP/N4)*(20/23)
V24 P/N	VgP/N4+(VgP/N3-VgP/N4)*(19/23)
V25 P/N	VgP/N4+(VgP/N3-VgP/N4)*(18/23)
V26 P/N	VgP/N4+(VgP/N3-VgP/N4)*(17/23)
V27 P/N	VgP/N4+(VgP/N3-VgP/N4)*(16/23)
V28 P/N	VgP/N4+(VgP/N3-VgP/N4)*(15/23)
V29 P/N	VgP/N4+(VgP/N3-VgP/N4)*(14/23)
V30 P/N	VgP/N4+(VgP/N3-VgP/N4)*(13/23)
V31 P/N	VgP/N4+(VgP/N3-VgP/N4)*(12/23)

Grayscale Voltage	Formula
V32 P/N	VgP/N4+(VgP/N3-VgP/N4)*(11/23)
V33 P/N	VgP/N4+(VgP/N3-VgP/N4)*(10/23)
V34 P/N	VgP/N4+(VgP/N3-VgP/N4)*(9/23)
V35 P/N	VgP/N4+(VgP/N3-VgP/N4)*(8/23)
V36 P/N	VgP/N4+(VgP/N3-VgP/N4)*(7/23)
V37 P/N	VgP/N4+(VgP/N3-VgP/N4)*(6/23)
V38 P/N	VgP/N4+(VgP/N3-VgP/N4)*(5/23)
V39 P/N	VgP/N4+(VgP/N3-VgP/N4)*(4/23)
V40 P/N	VgP/N4+(VgP/N3-VgP/N4)*(3/23)
V41 P/N	VgP/N4+(VgP/N3-VgP/N4)*(2/23)
V42 P/N	VgP/N4+(VgP/N3-VgP/N4)*(1/23)
V43 P/N	VgP/N4
V44 P/N	VgP/N5+(VgP/N4-VgP/N5)*(22/24)
V45 P/N	VgP/N5+(VgP/N4-VgP/N5)*(20/24)
V46 P/N	VgP/N5+(VgP/N4-VgP/N5)*(18/24)
V47 P/N	VgP/N5+(VgP/N4-VgP/N5)*(16/24)
V48 P/N	VgP/N5+(VgP/N4-VgP/N5)*(14/24)
V49 P/N	VgP/N5+(VgP/N4-VgP/N5)*(12/24)
V50 P/N	VgP/N5+(VgP/N4-VgP/N5)*(10/24)
V51 P/N	VgP/N5+(VgP/N4-VgP/N5)*(8/24)
V52 P/N	VgP/N5+(VgP/N4-VgP/N5)*(6/24)
V53 P/N	VgP/N5+(VgP/N4-VgP/N5)*(4/24)
V54 P/N	VgP/N5+(VgP/N4-VgP/N5)*(2/24)
V55 P/N	VgP/N5
V56 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB1
V57 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB2
V58 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB3
V59 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB4
V60 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB5
V61 P/N	VgP/N6+(VgP/N5-VgP/N6)*CB6
V62 P/N	VgP/N6
V63 P/N	VgP/N7

Table 7. 7 Voltage Calculation Formula of Grayscale Voltage

CGM0[1:0]	"00"	"01"	"10"	"11"
CT1	6/7	7.5/10.5	10/15	8.5/10.5
CT2	5/7	6/10.5	6.67/15	6.67/10.5
CT3	4/7	4/10.5	4/15	5.0/10.5
CT4	3/7	3/10.5	3/15	3.5/10.5
CT5	2/7	2/10.5	2/15	2.17/10.5
CT6	1/7	1/10.5	1/15	1/10.5

CGM1[1:0]	"00"	"01"	"10"	"11"
CB1	6/7	9.5/10.5	14/15	9.5/10.5
CB2	5/7	8.5/10.5	13/15	8.33/10.5
CB3	4/7	7.5/10.5	12/15	7.0/10.5
CB4	3/7	6.5/10.5	11/15	5.5/10.5
CB5	2/7	4.5/10.5	8.33/15	3.83/10.5
CB6	1/7	3.0/10.5	5/15	2.0/10.5

Note: Negative gamma don't have CGM0/CGM1 setting, the ratio V2~V7 and V56~V61 is automatically mapping from positive side.

Table 7. 8 Voltage Calculation Formula of Grayscale Voltage V2~V7 and V56~V61

Relationship between GRAM Data and Output Level

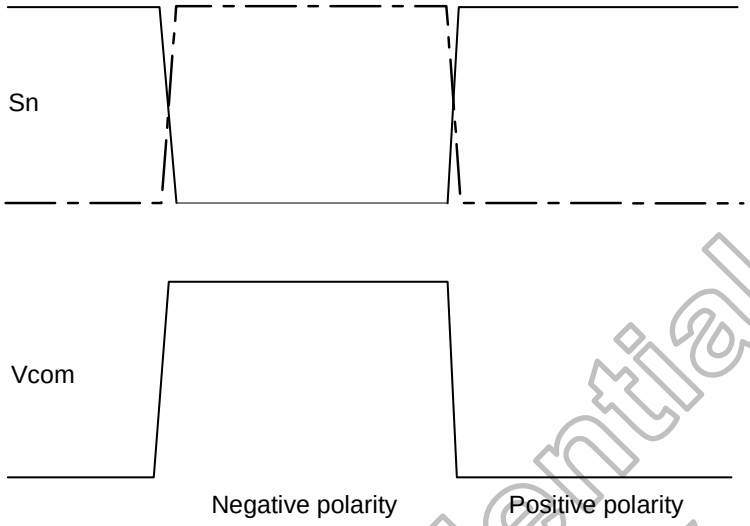
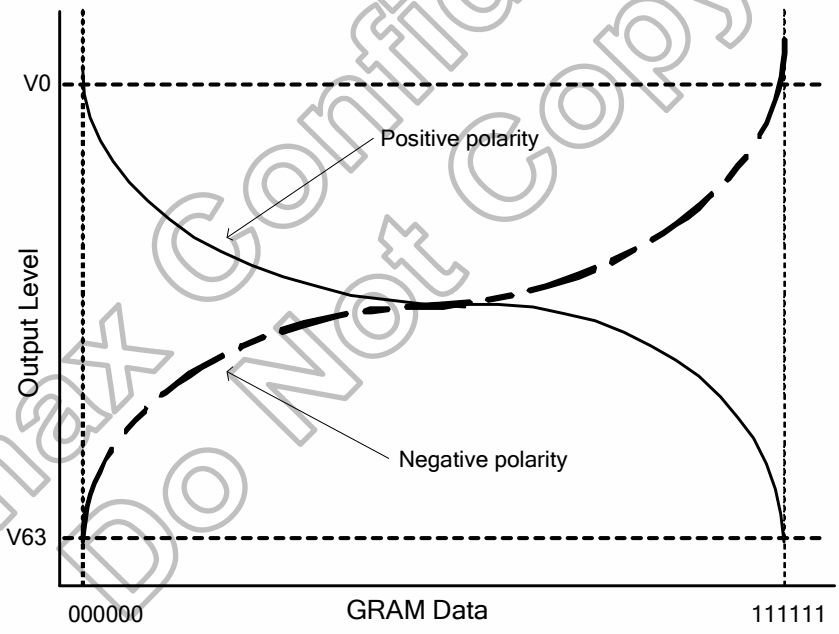


Figure 7. 5 Relationship between Source Output and VCOM



(Same characteristic for each RGB)

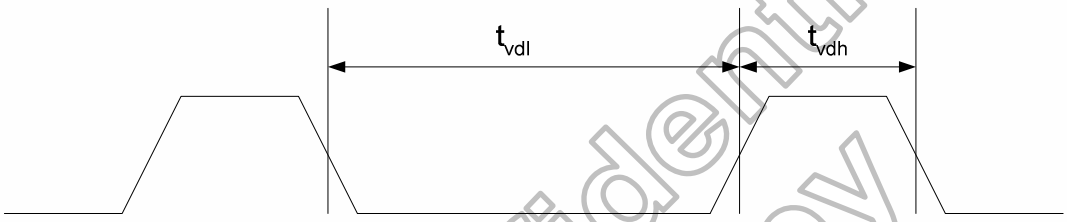
Figure 7. 6 Relationship between GRAM Data and Output Level (Normal White Panel and INVON="0")

7.3 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.3.1 Tearing Effect Line Modes

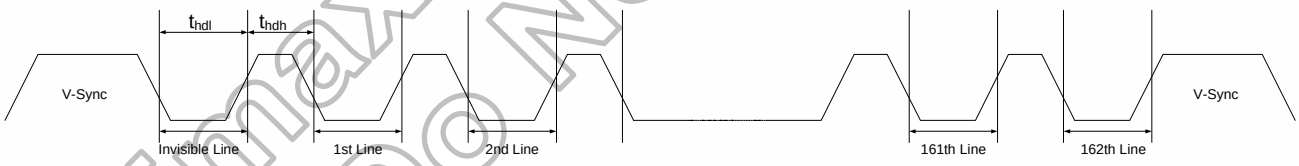
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh} = The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

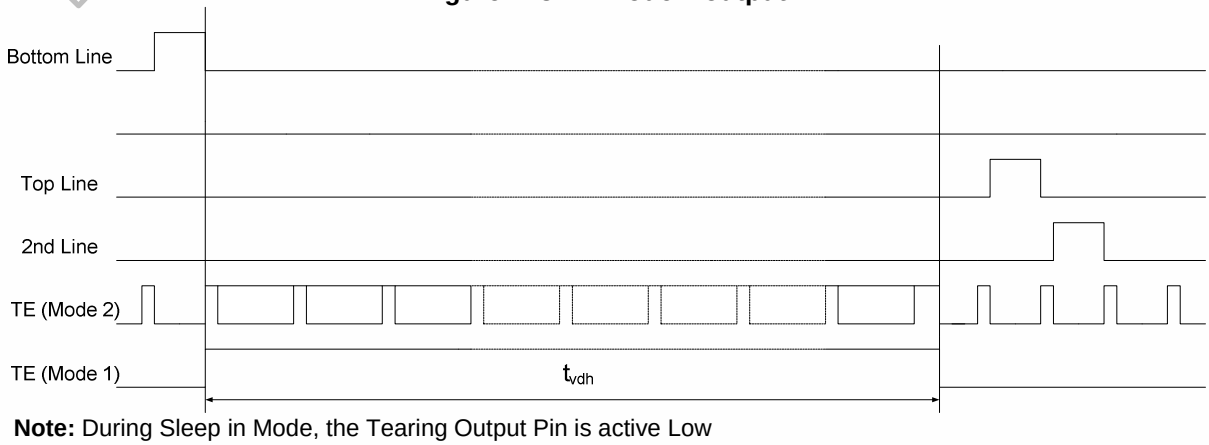
Figure 7. 7 TE mode 1 output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 220 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 7. 8 TE mode 2 output



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 7. 9 TE output waveform

7.3.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.

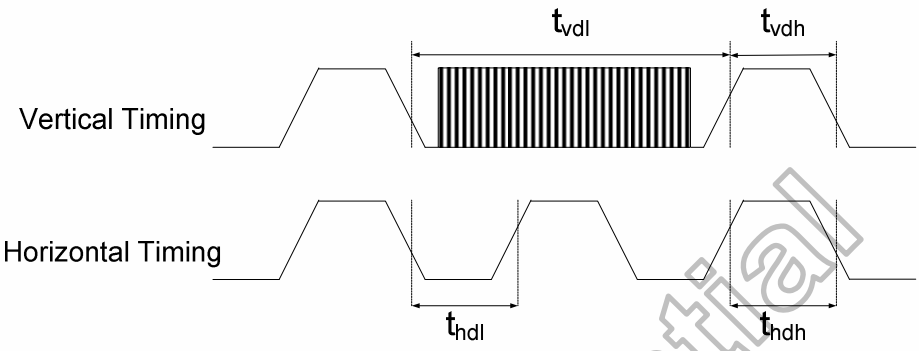


Figure 7. 10 Waveform of Tearing Effect Signal

Idle Mode Off (Frame Rate = TBD Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	BP+FP	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Table 7. 9 AC characteristics of Tearing Effect Signal

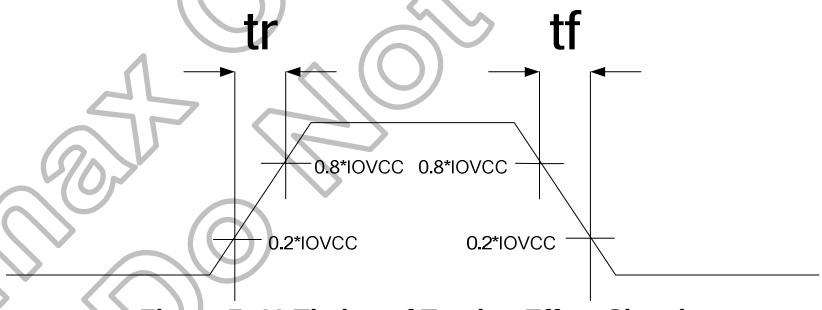
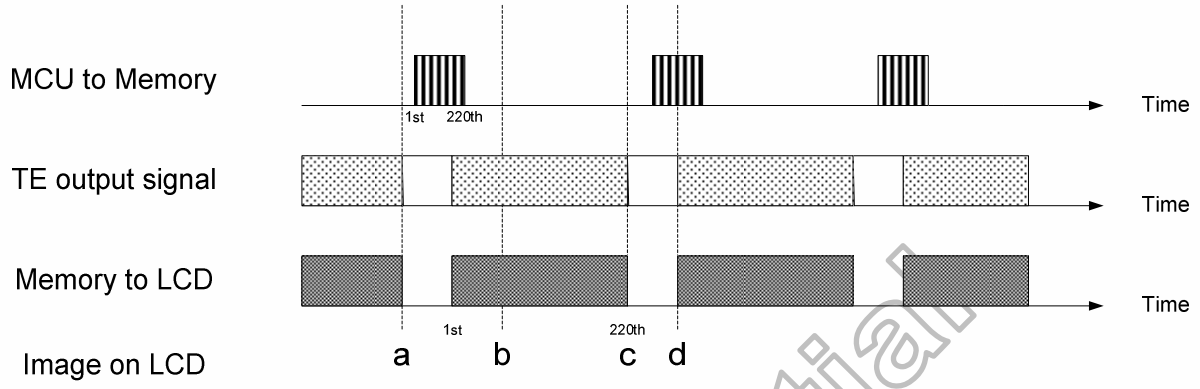


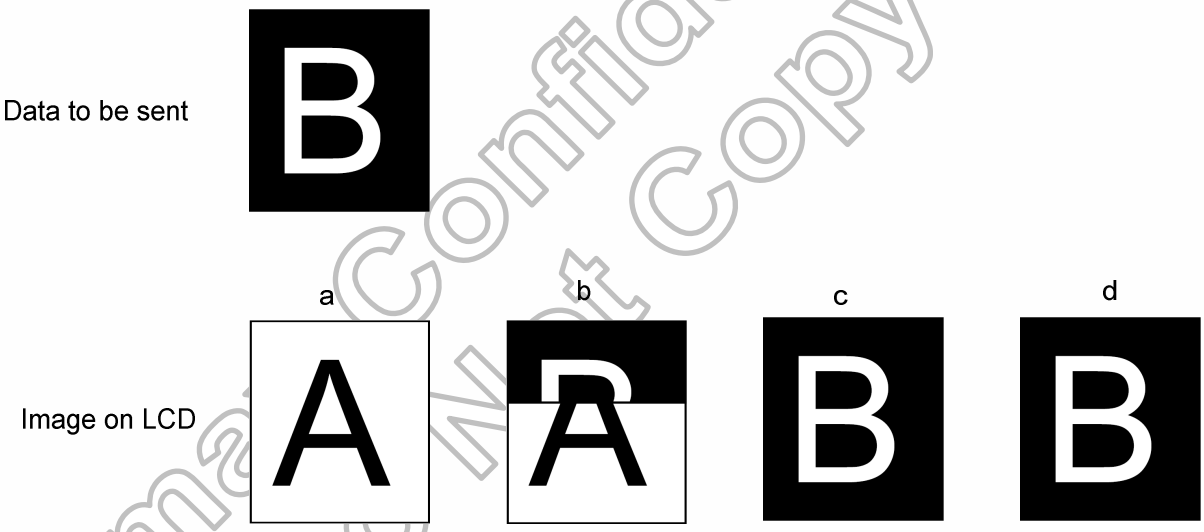
Figure 7. 11 Timing of Tearing Effect Signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

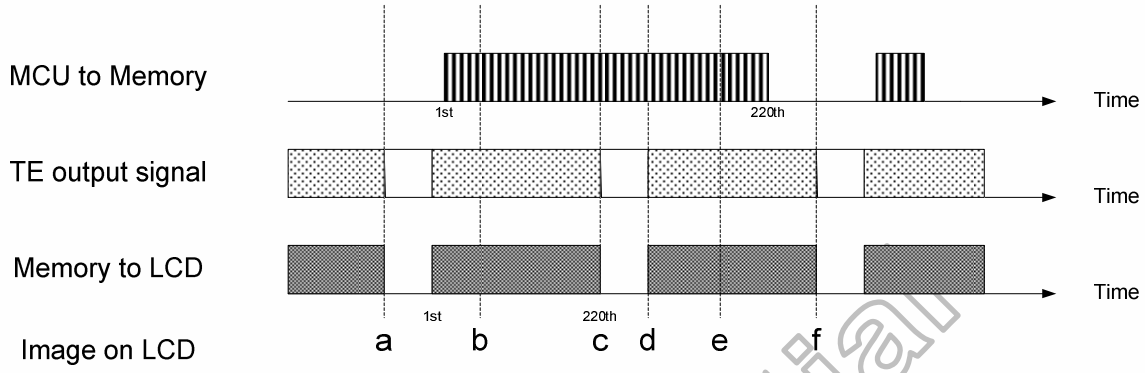
7.3.3 Example 1: MPU Write is faster than Panel Read



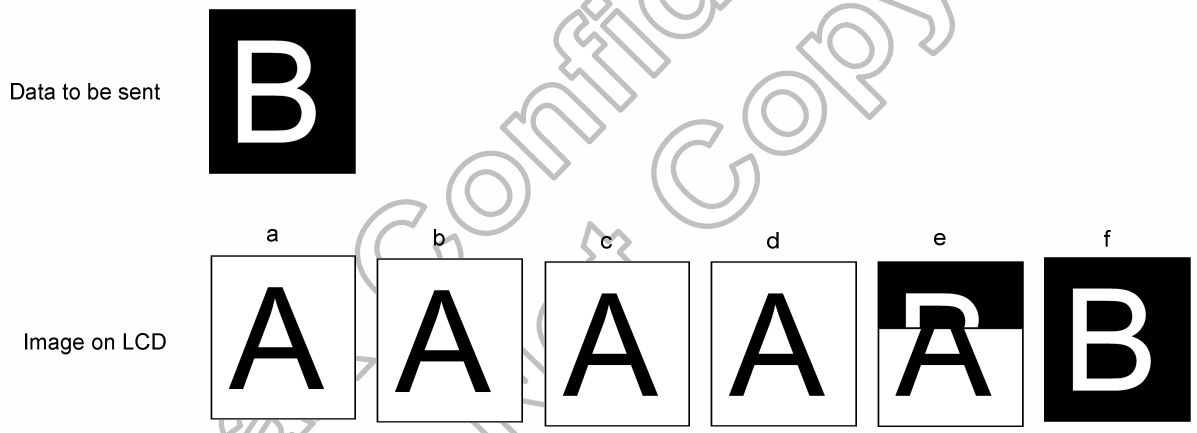
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.3.4 Example 2: MPU Write is slower than Panel Read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.4 LCD Power Generation Circuit

7.4.1 Power Supply Circuit

The power circuit of HX8340-B is used to generate supply voltages for LCD panel driving.

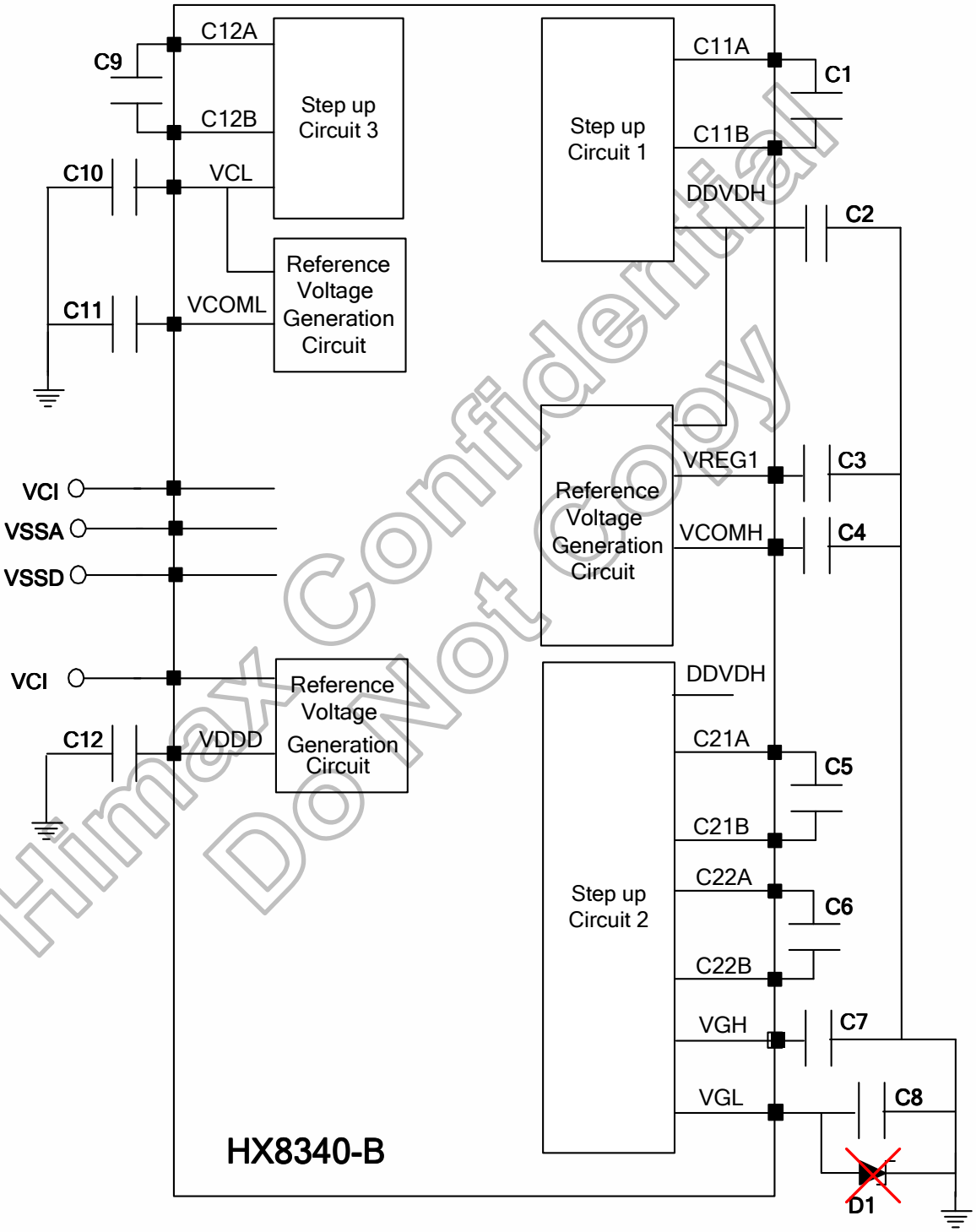


Figure 7. 12 The Block Diagram of HX8340-B Power Circuit

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity
C1 (C11A/B)	6V	1 µF (B characteristics)
C2 (DDVDH)	10V	1 µF (B characteristics)
C3 (VREG1)	10V	1 µF (B characteristics)
C4(VCOMH)	10V	1 µF (B characteristics)
C5 (C21A/B)	10V	1 µF (B characteristics)
C6 (C22A/B)	10V	1 µF (B characteristics)
C7 (VGH)	25V	1 µF (B characteristics)
C8 (VGL)	16V	1 µF (B characteristics)
C9 (C12A/B)	6V	1 µF (B characteristics)
C10 (VCL)	6V	1 µF (B characteristics)
C11 (VCOML)	6V	1 µF (B characteristics)
C12 (VDDD)	6V	1 µF (B characteristics)

Table 7. 10 The adoptability of Capacitor and Diode

7.4.2 LCD Power Generation Scheme

The boost voltage generated is shown as below.

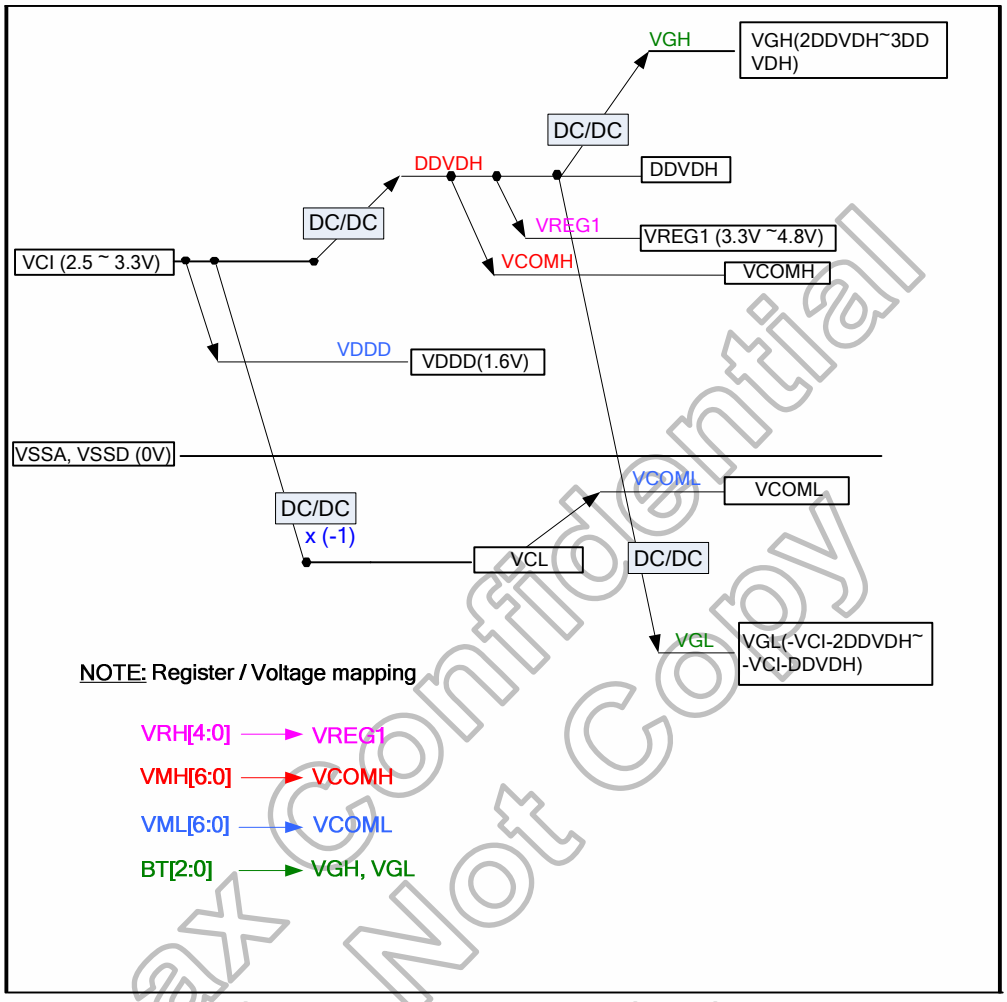


Figure 7. 13 LCD Power Generation Scheme

7.5 Power Function

7.5.1 System Interface Power On/Off Sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display On/Off Set flow

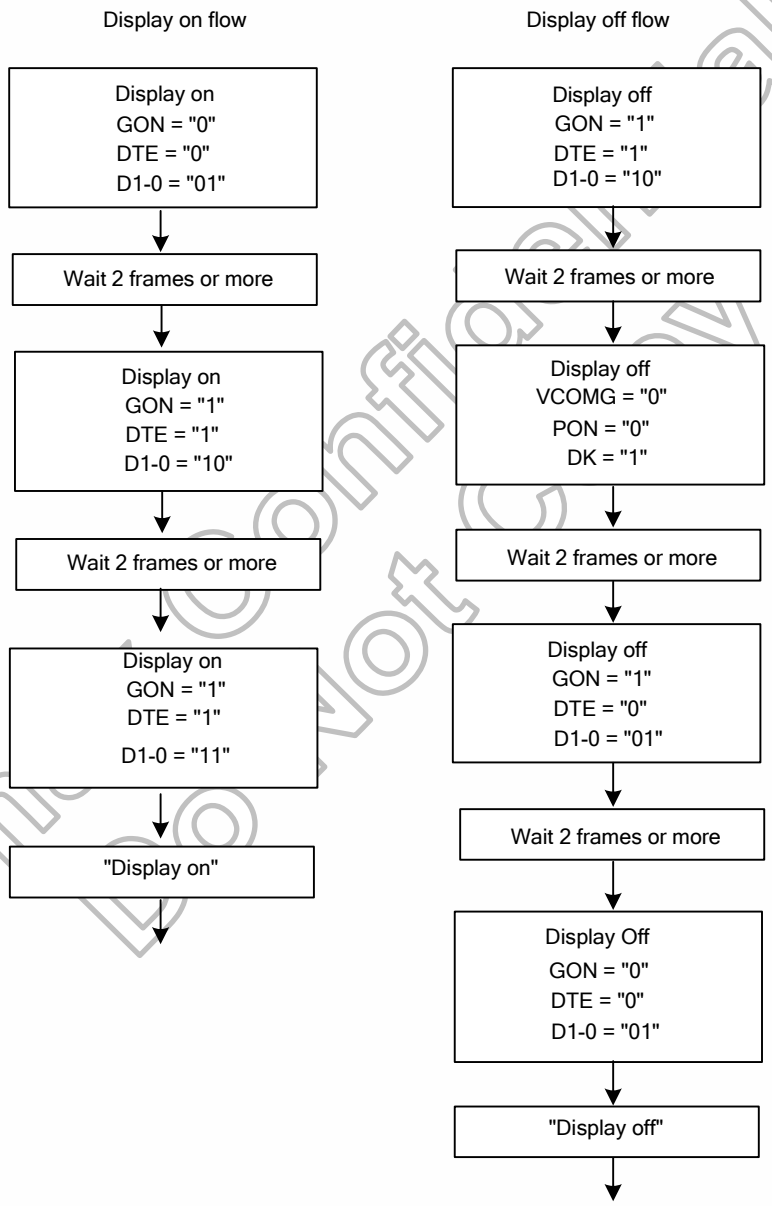


Figure 7. 14 Display On/Off Set flow

Sleep Mode Set up Flow

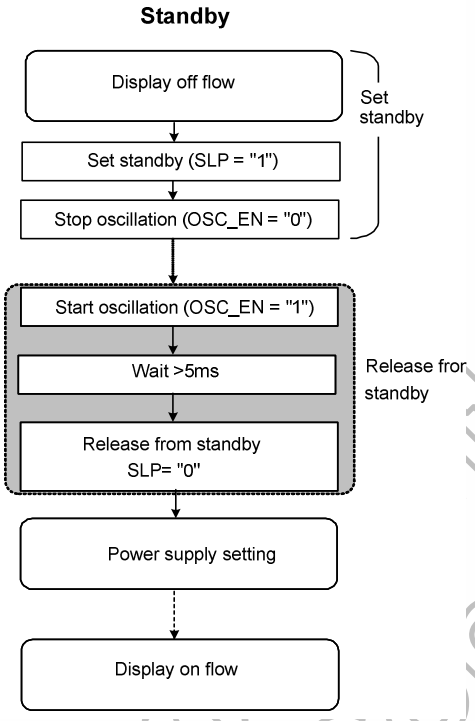


Figure 7. 15 Standby Mode Setting flow

Power On/Off Setting up Flow

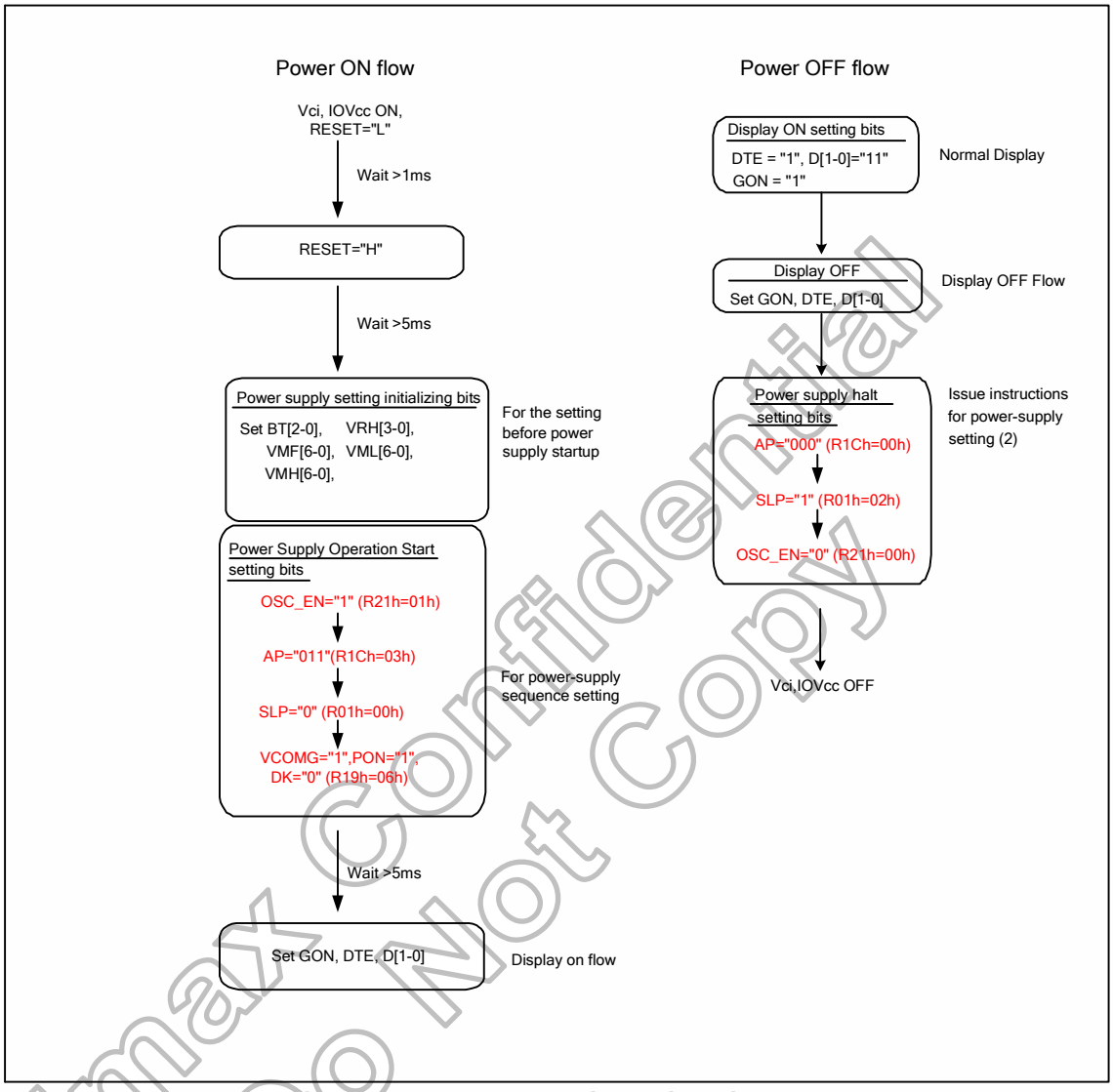


Figure 7. 16 Power Supply Setting Flow

7.5.2 RGB Interface Power On/Off

RGB mode Power on/off can be controlled by external pin SHUT or by internal CSHUT bit. As the internal CSHUT bit be written in RGB interface, the external pin SHUT control will be invalid

Power on Sequence

The Driver operates power up and display ON by IOVCC, VCII, SHUT, VS, HS, DE, DOTCLK on RGB mode as show as following figure.

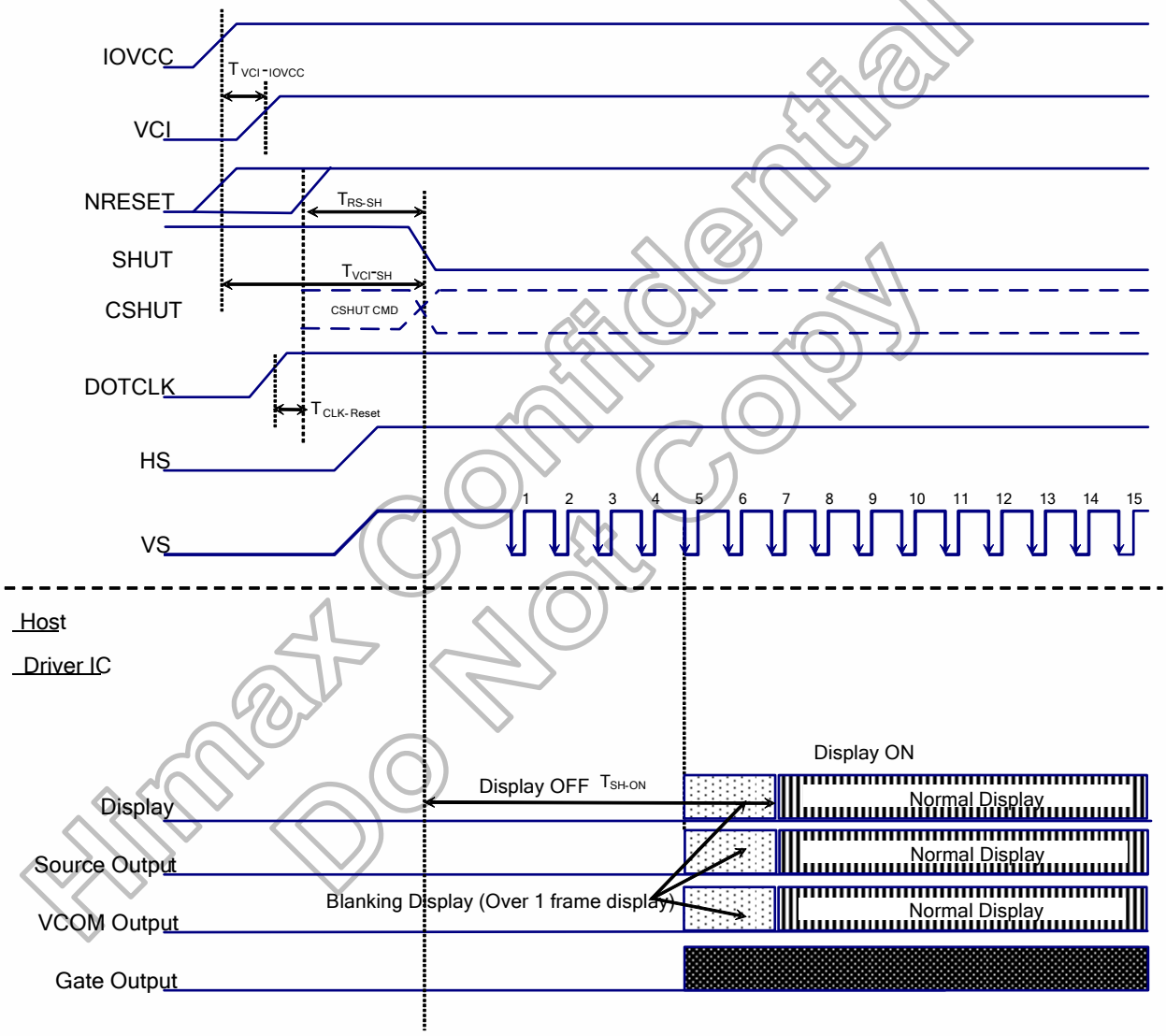


Figure 7. 17 Power On Sequence on RGB

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
IOVCC On to VCI On	$T_{IOVCC-VCI}$	0		-	ns	Note(1)
IOVCC/VCI on to falling edge of SHUT	T_{VCI-SH}	2	10	-	ms	-
RESX to falling of SHUT	T_{RS-SH}	1	2	-	ms	-
DOTCLK to NRESET	$T_{CLK-Nreset}$	20	20	-	DOTCLK	-
Falling edge of SHUT to Display start	T_{SH-ON}	-	6	-	VS	-

Note: (1) $T_{IOVCC-VCI}$ can be <=0ns, >0ns. In any case, IOVCC and VCI power up sequence should not have any impact on the driver / display functionalities / performance.
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (33H) command.

Table 7. 11 Power ON AC Characteristics

Power off Sequence Operate

The Driver operates power off and display OFF by VCI, IOVCC, SHUT, VS, HS and DE on RGB mode 2 as show as following figure.

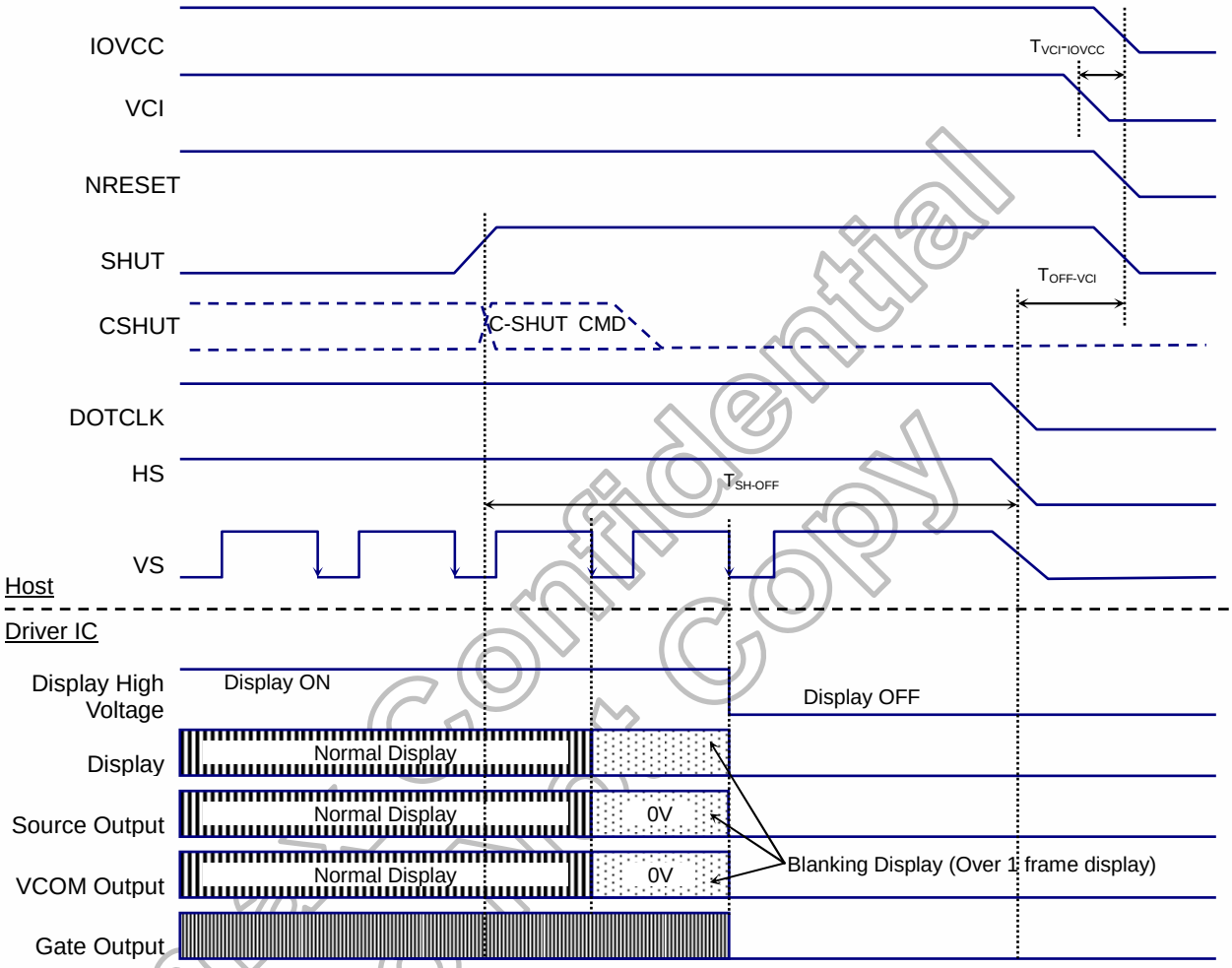


Figure 7. 18 Power off Sequence on RGB Mode

Characteristics	Symbol	Spec.			Unit	Remark
		Min.	Typ.	Max.		
IOVCC On to VCI On	$T_{iovcc-vci}$	0	-	-	ns	Note(1)
Signals Input to IOVCC/VCI Off	T_{SH-OFF}	1	-	-	us	Note(2)
Rising Edge of SHUT to Display Off	T_{SH-OFF}	2	-	-	VS	-

Note: (1) $T_{IOVCC-VCI}$ can be <=0ns, >0ns. In any case, IOVCC and VCI power up sequence should not have any impact on the driver / display functionalities / performance.
(2) Signals mean VS, HS, and DOTCLK signal.
(3) EPL='0', VSPL='0', HSPL='0' and DPL='0' of SETRGBIF (33H) command.

Table 7. 12 Power off AC Characteristics

7.6 Input / Output Pin State

7.6.1 Output Pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low

Table 7. 13 Characteristics of Output Pins

7.6.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
NRESET	Section 7.5.1	Input valid	Input valid	Section 7.5.1
NCS	Input invalid	Input valid	Input valid	Input invalid
NWR_RNW	Input invalid	Input valid	Input valid	Input invalid
NRD_E	Input invalid	Input valid	Input valid	Input invalid
DNC	Input invalid	Input valid	Input valid	Input invalid
SDI	Input invalid	Input valid	Input valid	Input invalid
VS	Input invalid	Input valid	Input valid	Input invalid
HS	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
DB[17:0]	Input invalid	Input valid	Input valid	Input invalid
OSC, M3, IM2, IM1,IM0,	Input invalid	Input valid	Input valid	Input invalid
EXTC	Input invalid	Input valid	Input valid	Input invalid

Table 7. 14 Characteristics of Input Pins

8. Command Set

8.1 Command Description

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R01h	Display Mode control	W/R	*	*	*	SCROL(0)		IDMON (0)	INVON (0)	SLP (1)	PTLON (0)	
R02h	Column address start 2	W/R	*	SC[15:8] (8'b0000_0000)								
R03h	Column address start 1	W/R	*	SC[7:0] (8'b0000_0000)								
R04h	Column address end 2	W/R	*	EC[15:8] (8'b0000_0000)								
R05h	Column address end 1	W/R	*	EC[7:0] (8'b1010_1111)								
R06h	Row address start 2	W/R	*	SP[15:8] (8'b0000_0000)								
R07h	Row address start 1	W/R	*	SP[7:0] (8'b0000_0000)								
R08h	Row address end 2	W/R	*	EP[15:8] (8'b0000_0000)								
R09h	Row address end 1	W/R	*	EP[7:0] (8'b1101_1011)								
R0Ah	Partial area start row 2	W/R	*	PSL[15:8] (8'b0000_0000)								
R0Bh	Partial area start row 1	W/R	*	PSL[7:0] (8'b0000_0000)								
R0Ch	Partial area end row 2	W/R	*	PEL[15:8] (8'b0000_0000)								
R0Dh	Partial area end row 1	W/R	*	PEL[7:0] (8'b1101_1011)								
R0Eh	Vertical Scroll Top fixed area 2	W/R	*	TFA[15:8] (8'b0000_0000)								
R0Fh	Vertical Scroll Top fixed area 1	W/R	*	TFA[7:0] (8'b0000_0000)								
R10h	Vertical Scroll height area 2	W/R	*	VSA[15:8] (8'b0000_0000)								
R11h	Vertical Scroll height area 1	W/R	*	VSA[7:0] (8'b1101_1100)								
R12h	Vertical Scroll Button area 2	W/R	*	BFA[15:8] (8'b0000_0000)								
R13h	Vertical Scroll Button area 1	W/R	*	BFA [7:0] (8'b0000_0000)								
R14h	Vertical Scroll Start address 2	W/R	*	VSP [15:8] (8b' 0000_0000)								
R15h	Vertical Scroll Start address 1	W/R	*	VSP [7:0] (8b' 0000_0000)								
R16h	Memory Access control	W/R	*	MY(0)	MX(0)	MV(0)	ML(0)	BGR(0)	*	*	*	
R17h	COLMOD	W/R	*	CSEL[3:0] (4b'0110)				*	IFPF[2:0] (3b'110)			
R18h	OSC Control	W/R	*	*	RADJ1[2:0] (3b'101)			*	RADJ0[2:0](3b'100)			
R19h	Power Control 1	W/R	*	*		*	*	*	VCOMG(0)	PON(0)	DK(1)	
R1Ah	Power Control 3	W/R	*	*`	I/PI FS0[2:0] (100)			*	N/P FS0[2:0] (100)			
R1Bh	Power Control 4	W/R	*	*	I/PI FS1[2:0] (010)			*	N/P FS1[2:0] (010)			
R1Ch	Power Control 5	W/R	*	*	*	*	*	*	AP[2:0] (000)			
R1Dh	Power Control 6	W/R	*	N/P_SAP[7:0(8b'0011_0010)								
R1Eh	Power Control 7	W/R	*	I/PI_SAP[7:0](8b'0011_0010)								
R1Fh	Power Control 8	W/R	*	*	*	*	*	VRH[4:0] (5b'00011)				
R20h	Power Control 9	W/R	*					*	BT[2:0] (000)*			
R21h	OSC Control	W/R	*	*	*			*			OSC_EN (0)	
R22h	SRAM Write Control	W/R	SRAM Write									
R23h	VCOM Control 1	W/R	*	*	VMF[6:0] (7b'100_0000)							
R24h	VCOM Control 2	W/R	*	*	VMH[6:0] (7b'001_1100)							
R25h	VCOM Control 3	W/R	*	*	VML[6:0] (7b'011_0100)							

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R26h	Display Control 1	W/R	*	PT[1:0] (10)		GON(1)	DTE(0)	D[1:0] (00)		*	*	
R27h	Display Control 2	W/R	*	REF (1)	PTV[1:0](01)		PTG (1)	ISC[3:0] (0011)				
R28h	Frame Rate Control 1	W/R	*	*	*	IP/DIV[1:0] (00)		*		N/P_DIV[1:0] (00)		
R29h	Frame Rate control 2	W/R	*	I/PI_RTN[3:0] (4b'1000)				N/P_RTN[3:0] (4'b1000)				
R2Ah	Frame Rate Control 3	W/R	*	N/P_DUM[7:0] (8b'0000_1000)								
R2Bh	Frame Rate Control 4	W/R	*	I/PI_DUM[7:0] (8b'0000_1000)								
R2Ch	Cycle Control 1	W/R	*	SON[7:0] (8'b0011_1000)								
R2Dh	Cycle Control 2	W/R	*	GDON[7:0] (8'b0000_1111)								
R2Eh	Cycle Control 3	W/R	*	GDOF[7:0] (8'b1010_1000)								
R2Fh	Display inversion	W/R	*	*	I/PI_NW[2:0](3b'001)			*	N/P_NW[2:0] (3b'001)			
R31h	RGB interface control 1	W/R	*	*	*	HBP[5:0] (6b'00_0110)						
R32h	RGB interface control 2	W/R	*	VBP[7:0] (8b'0000_0110)								
R33h	RGB interface control 3	W/R	*	*	*	*		DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	
R34h	RGB interface control 4	W/R	*	*	*	*		*	*		CSHUT(1)	
R35h	Outputs direction	W/R	*	*	*	*		*	*	CTB(0)	CRL(0)	
R36h	Interface mode	W/R	*	*	*	*		*	*	RCM1(0)	RCM0(0)	
R37h	NW/NB panel set	W/R	*	*	*	*		*	*	*	NWB(0)	
R38h	OTP Control 1	W/R	*	*	*	*	*	OTP_POR	OTP_OTPEN	OTP_PPROG	OTP_PWE	
R39h	OTP Control 2	W/R	*	OTP_YA2	OTP_YA1	OTP_YA0	*	OTP_XA2	OTP_XA1	OTP_XA0	*	
R3Ah	OTP Control 3	W/R	*	*	*	*	OTP_VARDJ1	OTP_VARDJ0	*	OTP_PTM1	OTP_PTM0	
R40h	Positive r1 Control (1)	W/R	*	*	MP12	MP11	MP10	*	MP02	MP01	MP00	
R41h	Positive r1 Control (2)	W/R	*	*	MP32	MP31	MP30	*	MP22	MP21	MP20	
R42h	Positive r1 Control (3)	W/R	*	*	MP52	MP51	MP50	*	MP42	MP41	MP40	
R43h	Positive r1 Control (4)	W/R	*	*	*	*	CP04	CP03	CP02	CP01	CP00	
R44h	Positive r1 Control (5)	W/R	*	CP23	CP22	CP21	CP20	CP13	CP12	CP11	CP10	
R45h	Positive r1 Control (6)	W/R	*	*	*	*	*	CP33	CP32	CP31	CP30	
R46h	Positive r1 Control (7)	W/R	*	*	*	*	CP44	CP43	CP42	CP41	CP40	
R47h	Positive r1 Control (8)	W/R	*	OP13	OP12	OP11	OP10	OP03	OP02	OP01	OP00	
R48h	Positive r1 Control (9)	W/R		*	*	*	*	CGM11	CGM10	CGM01	CGM00	
R50h	Negative r1 Control (1)	W/R	*	*	MN12	MN11	MN10	*	MN02	MN01	MN00	
R51h	Negative r1 Control (2)	W/R	*	*	MN32	MN31	MN30	*	MN22	MN21	MN20	
R52h	Negative r1 Control (3)	W/R	*	*	MN52	MN51	MN50	*	MN42	MN41	MN40	
R53h	Negative r1 Control (4)	W/R	*	*	*	*	CN04	CN03	CN02	CN01	CN00	
R54h	Negative r1 Control (5)	W/R	*	CN23	CN22	CN21	CN20	CN13	CN12	CN11	CN10	
R55h	Negative r1 Control (6)	W/R	*	*	*	*	*	CN33	CN32	CN31	CN30	
R56h	Negative r1 Control (7)	W/R	*	*	*	*	CN44	CN43	CN42	CN41	CN40	
R57h	Negative r1 Control (8)	W/R	*	ON13	ON12	ON11	ON10	ON03	ON02	ON01	ON00	

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R59h	Display control internal use	W/R	*	*	*	*	*	REV_P (0)	BGR_P (0)	SS_P (0)	GS_P (0)	
R60h	Power control internal use (1)	W/R	*	PTBA15 (0)	PTBA14 (0)	PTBA13 (0)	PTBA12 (0)	PTBA11 (0)	PTBA10 (0)	PTBA9 (0)	PTBA8 (0)	
R61h	Power control internal use (2)	W/R	*	PTBA7 (0)	PTBA6 (0)	PTBA5 (0)	PTBA4 (0)	PTBA3 (0)	PTBA2 (0)	PTBA1 (0)	PTBA0 (0)	
R62h	Source control internal use (1)	W/R	*	STBA15 (0)	STBA14 (0)	STBA13 (0)	STBA12 (0)	STBA11 (0)	STBA10 (0)	STBA9 (0)	STBA8 (0)	
R63h	Source control internal use (2)	W/R	*	STBA7 (1)	STBA6 (1)	STBA5 (0)	STBA4 (0)	STBA3 (0)	STBA3 (0)	STBA2 (0)	STBA1 (0)	
R73h	Source OP control	W/R	*	OPON7 (0)	OPON6 (0)	OPON5 (1)	OPON4 (1)	OPON3 (1)	OPON2 (0)	OPON1 (0)	OPON0 (0)	
R93h	Himax ID	R	*	ID (0)	ID (1)	ID(0)	ID (0)	ID (1)	ID (0)	ID (0)	ID0(1)	

8.2 Index Register

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 8. 1 Index Register

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID7-0) in the range from 000000b to 1111111b in binary form.

8.3 Display Mode Control Register (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	SCR OLL	*	IDM ON	INV ON	SLP	PTL ON
R	1	*	*	*	*	*	*	*	*	*	*	0	*	IDM ON	INV ON	SLP	PTL ON

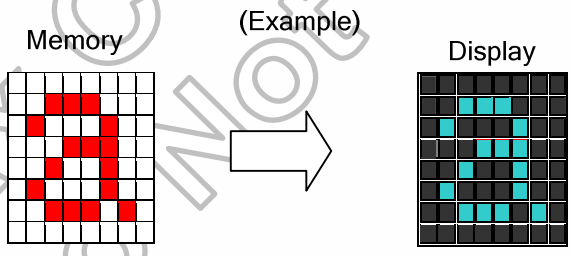
Figure 8. 2 Display Mode Control Register (R01h)

IDMON

This command is used for turning on/off IDLE (8-color display) mode by setting IDMON=1/0.

INVON

This command is used to enter into display inversion mode by setting INVON=1. Vise versa, it recovers from display inversion mode by setting INVON=0. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.



SLP

When SLP = '1', the driver into the sleep mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the sleep mode, only the following process can be executed.

a. Exit the Standby mode (SLP = "0")

b. Start the oscillation

In the Sleep mode, the GRAM data and register content are retained.

PTLON

This command is used for turning on/off PARTIAL mode by setting PTLON=1/0.

SCROLL

This command is used for turning on/off SCROLL mode by setting SCROLL=1/0. This bit can not read.

8.4 Column Address Start Register (R02~03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 8. 3 Column Address Start Register Upper Byte (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 8. 4 Column Address Start Register Low Byte (R03h)

8.5 Column Address End Register (R04~05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 8. 5 Column Address End Register Upper Byte (R04h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 8. 6 Column Address End Register Low Byte (R05h)

8.6 Row Address Start Register (R06~07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 8. 7 Row Address Start Register Upper Byte (R06h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 8. 8 Row Address Start Register Low Byte (R07h)

8.7 Row Address End Register (R08~09h)

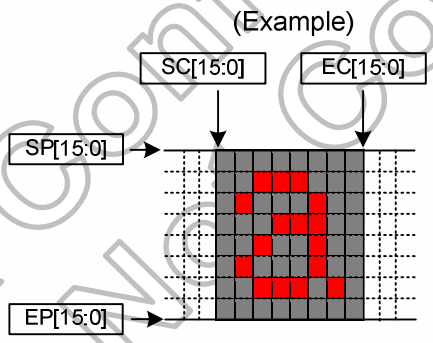
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 8. 9 Row Address End Register Upper Byte (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 8. 10 Row Address End Register Low Byte (R09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. These commands make no change on the other driver status. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



8.8 Partial Area Start Row Register (R0A~0Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 8. 11 Partial Area Start Row Register Upper Byte (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 8. 12 Partial Area Start Row Register Low Byte (R0Bh)

8.9 Partial Area End Row Register (R0C~0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

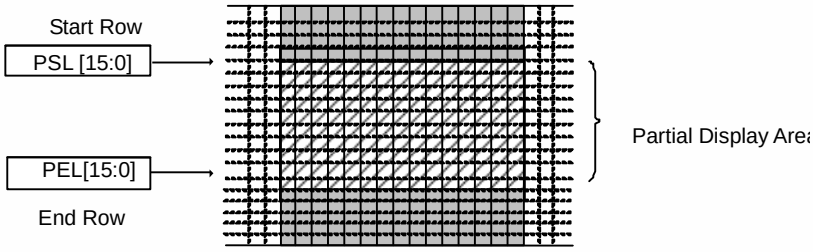
Figure 8. 13 Partial Area End Row Register Upper Byte (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

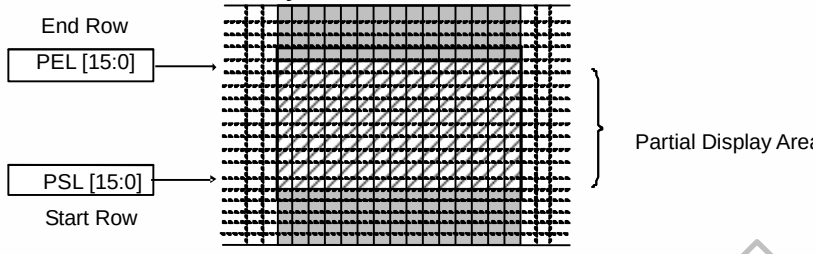
Figure 8. 14 Partial Area End Row Register Low Byte (R0Dh)

These commands (R0Ah~~0Dh) define the partial mode's display area. There are 4 parameters associated with this command, PSL[15:0], PEL[15:0], as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

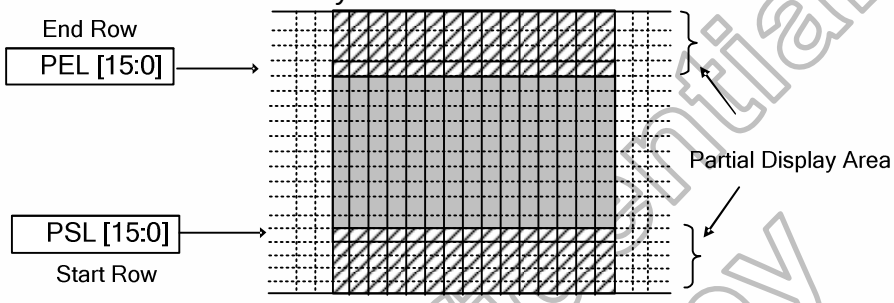
If End Row>Start Row when Memory Access Control ML=0



If End Row>Start Row when Memory Access Control ML=1



If End Row<Start Row when Memory Access Control ML=0



If End Row = Start Row then the Partial Area will be one row deep.

8.10 Vertical Scroll Top Fixed Area Register (R0E~0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 8. 15 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 8. 16 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh)

8.11 Vertical Scroll Height Area Register (R10~11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 8. 17 Vertical Scroll Height Area Register Upper Byte (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 8. 18 Vertical Scroll Height Area Register Low Byte (R11h)

8.12 Vertical Scroll Button Fixed Area Register (R12~13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 8. 19 Vertical Scroll Button Fixed Area Register Upper Byte (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 8. 20 Vertical Scroll Button Fixed Area Register Low Byte (R13h)

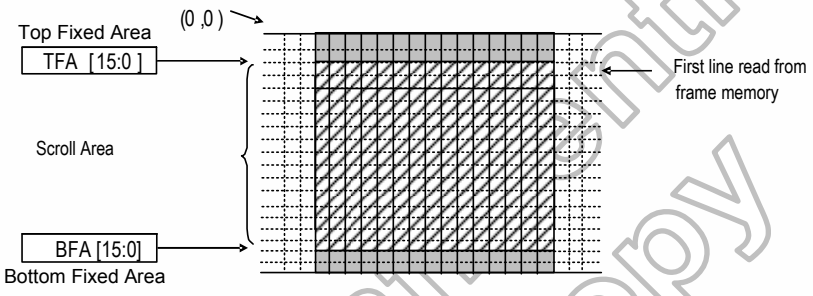
These commands (R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display. When Memory Access Control ML=0,

TFA[15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

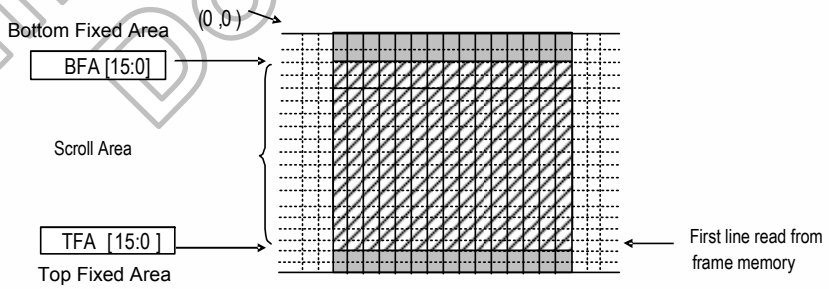


When Memory Access Control ML=1,

TFA[15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



8.13 Vertical Scroll Start Address Register (R14~15h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 8. 21 Vertical Scroll Start Address Register Upper Byte (R14h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

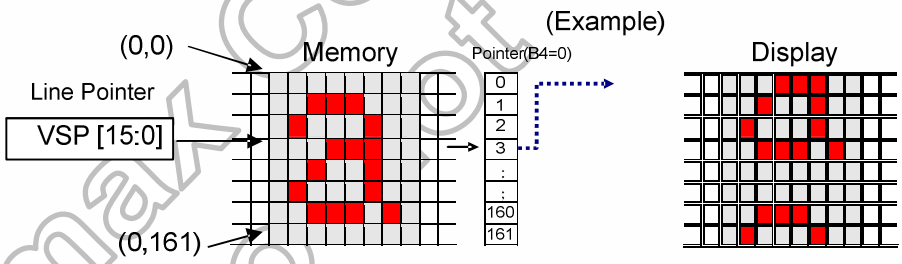
Figure 8. 22 Vertical Scroll Start Address Register Low Byte (R15h)

This command is used together with Vertical Scrolling Definition (18h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When Memory Access Control B4=0

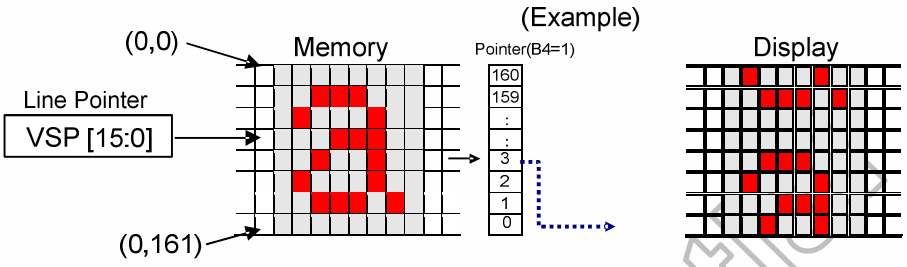
Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3



When Memory Access Control B4=1

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
VSP refers to the Frame Memory line Pointer.

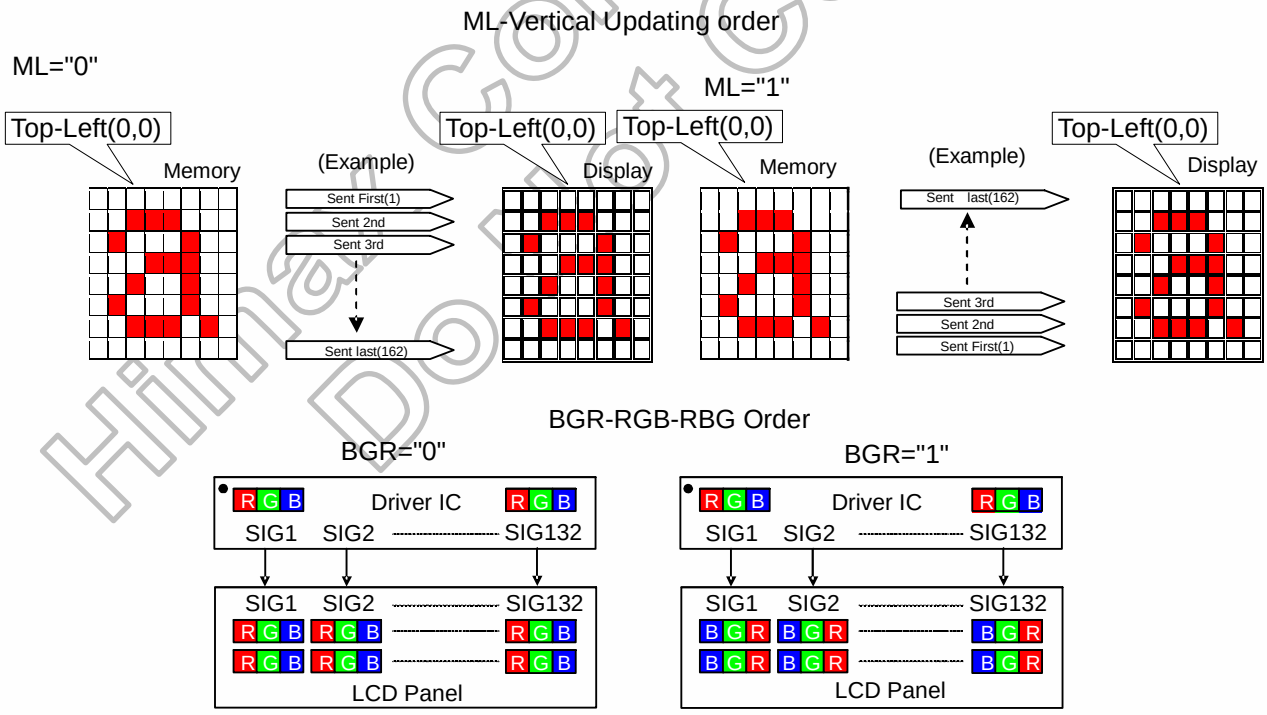
8.14 Memory Access Control Register (R16h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	MY	MX	MV	ML	BGR	*	*	*
R	1	*	*	*	*	*	*	*	*	MY	MX	MV	ML	BGR	*	*	*

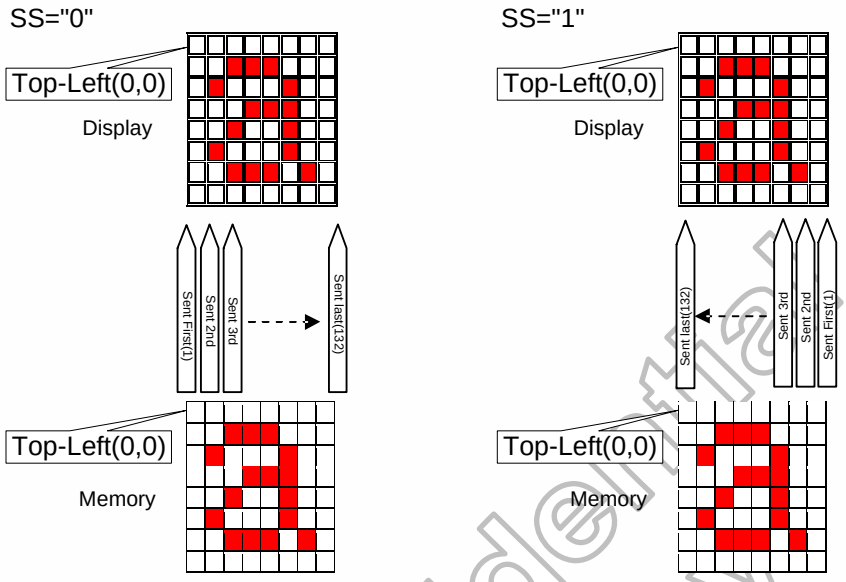
Figure 8. 23 Memory Access Control Register (R16h)

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. "MCU to memory write/read direction"
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) Note : HW pin SRGB=0, BGR color filter SRGB=1, RGB color filter



SS-Horizontal Updating order



Note: Top-Left (0, 0) means a physical memory location.

8.15 COLMOD Control Register (R17h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	CSEL 3 (0)	CSEL 2 (1)	CSEL 1 (1)	CSEL 0 (0)	*	IFPF 2 (1)	IFPF 1 (1)	IFPF0 (0)
R	1	*	*	*	*	*	*	*	*	CSEL 3 (0)	CSEL 2 (1)	CSEL 1 (1)	CSEL 0 (0)	*	IFPF 2 (1)	IFPF 1 (1)	IFPF0 (0)

Figure 8. 24 COLMOD Control Register (R16h)

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface

Interface Format	IFPF2	IFPF1	IFPF0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

RGB interface

Interface Format	CSEL3	CSEL2	CSEL1	CSEL0
16 Bit/Pixel	0	1	0	1
18 Bit/Pixel	0	1	1	0
6 Bit/Pixel	1	1	1	0
Not Defined	The Other Setting			

8.16 OSC Control Register (R18h & R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	RADJ 12	RADJ 11	RADJ 10	*	RADJ 02	RADJ 01	RADJ 00
R	1	*	*	*	*	*	*	*	*	*	RADJ 12	RADJ 11	RADJ 10	*	RADJ 02	RADJ 01	RADJ 00

Figure 8. 25 OSC Control 1 Register (R18h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_ EN
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_ EN

Figure 8. 26 OSC Control 2 Register (R21h)

These commands are used to set internal oscillator related setting

OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. In RGB interface mode (RCM[1:0] = '10' or '11'), internal oscillator will be stop to oscillate and OSC_EN bit control is invalid.

RADJ[2:0]: Internal oscillator frequency adjusts. For details, please refer to "7.1 Internal Oscillator" section. For example, R18h=44h the typical frame rate will be 60Hz.

RADJ 12	RADJ 11	RADJ 10	RADJ 02	RADJ 01	RADJ 00	Internal Oscillator Frequency
0	0	0	0	0	0	133% x 2.52MHz
0	0	1	0	0	1	125% x 2.52MHz
0	1	0	0	1	0	117% x 2.52MHz
0	1	1	0	1	1	108% x 2.52MHz
1	0	0	1	0	0	100% x 2.52MHz
1	0	1	1	0	1	85% x 2.52MHz
1	1	0	1	1	0	75% x 2.52MHz
1	1	1	1	1	1	50% x 2.52MHz
Others						Setting Inhibited

8.17 Power Control 1 Register (R19h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VCOMG	PON	DK
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VCOMG	PON	DK

Figure 8. 27 Power Control 1 Register (R19h)

DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation. For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

VCOMG: Specify on/off control of step-up circuit 3 for VCL voltage generation. For detail, see the Power Supply Setting Sequence. When VCOMG = '0', VCOML = GND.

VCOMG	Operation of step-up circuit 3
0	OFF
1	ON

8.18 Power Control 2 Register (R1Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	I/PI FS02	I/PI FS01	I/PI FS00	*	N/P FS02	N/P FS01	N/P FS00
R	1	*	*	*	*	*	*	*	*	*	I/PI FS02	I/PI FS01	I/PI FS00	*	N/P FS02	N/P FS01	N/P FS00

Figure 8. 28 Power Control 2 Register (R1Ah)

N/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal / Partial mode.

FS02	FS01	FS00	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

8.19 Power Control 3 Register (R1Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	I/PI FS12	I/PI FS11	N/P FS10	*	N/P FS12	N/P FS11	N/P FS10
R	1	*	*	*	*	*	*	*	*	*	I/PI FS12	I/PI FS11	I/PI FS10	*	N/P FS12	N/P FS11	N/P FS10

Figure 8. 29 Power Control 3 Register (R1Bh)

I/PI_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

N/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal / Partial mode.
I/PI_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2, Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

8.20 Power Control 4 Register (R1Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0

Figure 8. 30 Power Control 4 Register (R1Ch)

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Medium Low
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

8.21 Power Control 5 Register (R1Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	N/P_SAP7	N/P_SAP6	N/P_SAP5	N/P_SAP4	N/P_SAP3	N/P_SAP2	N/P_SAP1	N/P_SAP0
R	1	*	*	*	*	*	*	*	*	N/P_SAP7	N/P_SAP6	N/P_SAP5	N/P_SAP4	N/P_SAP3	N/P_SAP2	N/P_SAP1	N/P_SAP0

Figure 8. 31 Power Control 5 Register (R1Dh)

N/P_SAP[7:0]: Internal use, not open.

8.22 Power Control 6 Register (R1Eh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	I/PI_SAP7	I/PI_SAP6	I/PI_SAP5	I/PI_SAP4	I/PI_SAP3	I/PI_SAP2	I/PI_SAP1	I/PI_SAP0
R	1	*	*	*	*	*	*	*	*	I/PI_SAP7	I/PI_SAP6	I/PI_SAP5	I/PI_SAP4	I/PI_SAP3	I/PI_SAP2	I/PI_SAP1	I/PI_SAP0

Figure 8. 32 Power Control 6 Register (R1Eh)

I/PI_SAP[7:0]: Internal use, not open.

8.23 Power Control 7 Register (R1Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0
R	1	*	*	*	*	*	*	*	*	*	*	*	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0

Figure 8. 33 Power Control 7 Register (R1Fh)

VRH[4:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.

VRH4	VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	0	4.80
0	0	0	0	1	4.75
0	0	0	1	0	4.70
0	0	0	1	1	4.65
0	0	1	0	0	4.60
0	0	1	0	1	4.55
0	0	1	1	0	4.50
0	0	1	1	1	4.45
0	1	0	0	0	4.40
0	1	0	0	1	4.35
0	1	0	1	0	4.30
0	1	0	1	1	4.25
0	1	1	0	0	4.20
0	1	1	0	1	4.15
0	1	1	1	0	4.10
0	1	1	1	1	4.05
1	0	0	0	0	4.00
1	0	0	0	1	3.95
1	0	0	1	0	3.90
1	0	0	1	1	3.85
1	0	1	0	0	3.80
1	0	1	0	1	3.75
1	0	1	1	0	3.70
1	0	1	1	1	3.65
1	1	0	0	0	3.60
1	1	0	0	1	3.55
1	1	0	1	0	3.50
1	1	0	1	1	3.45
1	1	1	0	0	3.40
1	1	1	0	1	3.35
1	1	1	1	0	3.30
1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.

8.24 Power Control 8 Register (R20h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	BT2	BT1	BT0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	BT2	BT1	BT0

Figure 8. 34 Power Control 8 Register (R20h)

BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.1V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	1	5.1V	-VCI	3DDVDH	-2DDVDH
0	1	0	5.1V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	5.1V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
1	0	0	5.1V	-VCI	VCI+2DDVDH	-2DDVDH
1	0	1	5.1V	-VCI	VCI+2DDVDH	VCI-2DDVDH
1	1	0	5.1V	-VCI	2DDVDH	-2DDVDH
1	1	1	5.1V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V

8.25 Write/Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 8. 35 Read Data Register (R22h)

WD[17:0] : Transforms the data into 16-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

8.26 VCOM Offset Control Register (R23h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	VMF 6	VMF 5	VMF 4	VMF 3	VM F2	VMF 1	VMF 0
R	1	*	*	*	*	*	*	*	*	*	VMF 6	VMF 5	VMF 4	VMF 3	VM F2	VMF 1	VMF 0

Figure 8. 36 VCOM Offset Control Register (R23h)

VMF[6:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (25mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (25mV)

VMF[6:0]	VCOMH	VCOML
0	“VMH” – 64d	“VML” – 64d
1	“VMH” – 63d	“VML” – 63d
2	“VMH” – 62d	“VML” – 62d
3	“VMH” – 61d	“VML” – 61d
:	:	:
62	“VMH” – 2d	“VML” – 2d
63	“VMH” – 1d	“VML” – 1d
64	“VMH”	“VML”
65	“VMH” + 1d	“VML” + 1d
66	“VMH” + 2d	“VML” + 2d
:	:	:
126	“VMH” + 62d	“VML” + 62d
127	“VMH” + 63d	“VML” + 63d

8.27 VCOMH Control Register (R24h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0
R	1	*	*	*	*	*	*	*	*	*	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0

Figure 8. 37 VCOMH Control Register (R24h)

VMH[6:0]: Set the VCOMH voltage (High level voltage of VCOM).
VCOM High voltage = Decimal(VMH[6:0])x0.025+2.5.
The default value is 1Ch(28x0.025+2.5=3.2V),

VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	VCOMH
0	0	0	0	0	0	0	2.500
0	0	0	0	0	0	1	2.525
0	0	0	0	0	1	0	2.550
0	0	0	0	0	1	1	2.575
0	0	0	0	1	0	0	2.600
0	0	0	0	1	0	1	2.625
:	:	:	:	:	:	:	:
0	1	1	1	0	0	1	3.925
0	1	1	1	0	1	0	3.950
0	1	1	1	0	1	1	3.975
0	1	1	1	1	0	0	4.000
0	1	1	1	1	0	1	4.025
0	1	1	1	1	1	0	4.050
0	1	1	1	1	1	1	4.075
1	0	0	0	0	0	0	4.100
1	0	0	0	0	0	1	4.125
1	0	0	0	0	1	0	4.150
1	0	0	0	0	1	1	4.175
1	0	0	0	1	0	0	4.200
1	0	0	0	1	0	1	
:	:	:	:	:	:	:	:
1	0	1	1	0	0	0	4.700
1	0	1	1	0	0	1	4.725
1	0	1	1	0	1	0	4.750
1	0	1	1	0	1	1	4.775
1	0	1	1	1	0	0	4.800
:	:	:	:	:	:	:	4.800
1	1	1	1	1	1	0	4.800
1	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister)

8.28 VCOML Control Register (R25h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0
R	1	*	*	*	*	*	*	*	*	*	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0

Figure 8. 38 VCOML Control Register (R25h)

VML[6:0]: Set the VCOML voltage (Low level voltage of VCOM).
VCOM Low voltage = Decimal(VML[6:0])x0.025-2.5.
The default value is 34h(52x0.025-2.5=-1.2V)

VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	1	-2.475
0	0	0	0	0	1	0	-2.450
0	0	0	0	0	1	1	-2.425
0	0	0	0	1	0	0	-2.400
0	0	0	0	1	0	1	-2.375
:	:	:	:	:	:	:	:
1	0	1	1	1	1	1	-0.125
1	1	0	0	0	0	0	-0.100
1	1	0	0	0	0	1	-0.075
1	1	0	0	0	1	0	-0.050
1	1	0	0	0	1	1	-0.025
1	1	0	0	1	0	0	0.000
1	1	0	0	1	0	1	Setting inhibit
:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	Setting inhibit

8.29 Display Control 1 Register (R26h)

R/W	RS	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
W	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*
R	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*

Figure 8. 39 Display Control 1 Register (R26h)

D[1:0]: When D1=1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8340-B can control the charging current for the LCD with AC driving. When D1–0 = 01, the internal display of the HX8340-B is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

PT[1:0] : Non-display area source output control see follow table

INVON /REV_PANEL	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 . . 18'h3FFFF	V63 . . V0	V0 . . V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 . . 18'h3FFFF	V0 . . V63	V63 . . V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z

8.30 Display Control 2 Register (R27h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	REF	PTV 1	PTV 0	PTG	ISC3	ISC2	ISC1	ISC0
R	1	*	*	*	*	*	*	*	*	REF	PTV 1	PTV 0	PTG	ISC3	ISC2	ISC1	ISC0

Figure 8. 40 Display Control 2 Register (R27h)

REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enabling.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	--	Black Display (NB = '0') White Display (NB = '1')	Normal Driving	Normal Driving
1	0	0	--	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (NB = '0') White Display (NB = '1')	Normal Driving	Normal Driving
1	1	0	--	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (NB = '0') White Display (NB = '1')	Normal Driving	Normal Driving

8.31 Frame Rate Control Register (R28h~R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0
R	1	*	*	*	*	*	*	*	*	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0

Figure 8. 41 Frame Control 1 Register (R28h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN2	N/P_RTN1	N/P_RTN0
R	1	*	*	*	*	*	*	*	*	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN2	N/P_RTN1	N/P_RTN0

Figure 8. 42 Frame Control 2 Register (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0
R	1	*	*	*	*	*	*	*	*	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0

Figure 8. 43 Frame Control 3 Register (R2Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	I/PI_DUM7	I/PI_DUM6	I/PI_DUM5	I/PI_DUM4	I/PI_DUM3	I/PI_DUM2	I/PI_DUM1	I/PI_DUM0
R	1	*	*	*	*	*	*	*	*	I/PI_DUM7	I/PI_DUM6	I/PI_DUM5	I/PI_DUM4	I/PI_DUM3	I/PI_DUM2	I/PI_DUM1	I/PI_DUM0

Figure 8. 44 Frame Control 4 Register (R2Bh)

N/P_DIV[1:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **N/P_RTN[3:0]** bits (1H period clock cycle), **N/P_DIV[1:0**], and **N/P_DUM[7:0]** bits.

I/PI_DIV[1:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **I/PI_RTN[3:0]** bits(1H period clock cycle), **I/PI_DIV[1:0**], and **I/PI_DUM[7:0]** bits.

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

N/P_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation.
I/PI_ RTN[3:0]: Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[3:0]	Clock number per Line
4'b0000	Setting Inhibited
4'b0001	Setting Inhibited
4'b0010	Setting Inhibited
4'b0011	Setting Inhibited
4'b0100	180
:	:
4'b1110	190
4'b1111	191

N/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
I/PI_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4
:	:
254d	254
255d	255

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (220+DUM)) [Hz]
fosc: RC oscillation frequency

8.32 Display Cycle Control Register (R2Ch~R2Eh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0
R	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0

Figure 8. 45 Display Cycle Control 1 Register (R2Ch)

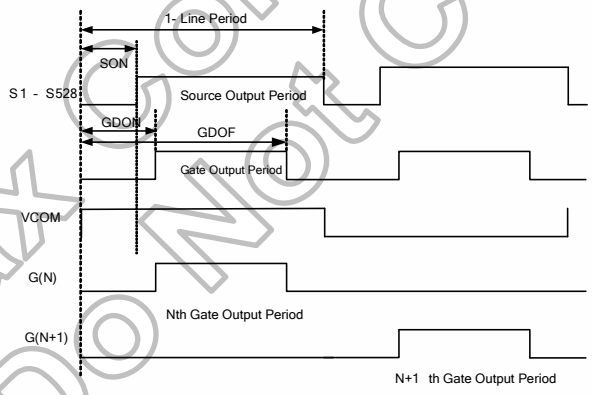
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	GDON N7	GDON N6	GDON N5	GDON N4	GDON N3	GDON N2	GDON N1	GDON N0
R	1	*	*	*	*	*	*	*	*	GDON N7	GDON N6	GDON N5	GDON N4	GDON N3	GDON N2	GDON N1	GDON N0

Figure 8. 46 Display Cycle Control 2 Register (R2Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	GDOF F7	GDOF F6	GDOF F5	GDOF F4	GDOF F3	GDOF F2	GDOF F1	GDOF F0
R	1	*	*	*	*	*	*	*	*	GDOF F7	GDOF F6	GDOF F5	GDOF F4	GDOF F3	GDOF F2	GDOF F1	GDOF F0

Figure 8. 47 Display Cycle Control 1 Register (R2Eh)

The HX8340-B can control the display operation period time for LCD panel driving as follow:



SON[7:0]: Specify the valid source output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h” and “01h” is inhibited).

GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited).

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).

8.33 Display Inversion Control Register (R2Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	I/PI_ NW2	I/PI_ NW1	I/PI_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0
R	1	*	*	*	*	*	*	*	*	*	I/PI_ NW2	I/PI_ NW1	I/PI_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0

Figure 8. 48 Display Inversion Control Register (R2Fh)

This command is used to set display inversion control

N/P_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.

I/PI_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD driving Inversion Type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

8.34 RGB Interface Control Register (R31h~R32h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0
R	1	*	*	*	*	*	*	*	*	*	*	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0

Figure 8. 49 RGB Interface HBP Control Register (R31h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	VBP 7	VBP 6	VBP 5	VBP 4	VBP 3	VBP 2	VBP 1	VBP 0
R	1	*	*	*	*	*	*	*	*	VBP 7	VBP 6	VBP 5	VBP 4	VBP 3	VBP 2	VBP 1	VBP 0

Figure 8. 50 RGB Interface VBP Control Register (R32h)

This command is used to set vertical and horizontal back porch control in RGB I/F mode 2 (RCM[1:0]= '11') (RGB I/F mode 1 is using DE signal as data enable signal)

HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2

HBP[5:0]	No. of clock cycle of DOTCLK
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
61d	61
62d	62
63d	Setting Inhibited

VBP[7:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2

VBP[7:0]	No. of clock cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
253d	253
254d	254
255d	Setting Inhibited

8.35 RGB Interface Signal Control Register (R33h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	DPL	HSPL	VSPL	EPL
R	1	*	*	*	*	*	*	*	*	*	*	*	*	DPL	HSPL	VSPL	EPL

Figure 8. 51 RGB Interface Signal Control Register (R33h)

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	Display image	Operation
0	High	Enable	Write data to DB17-0
0	Low	Disable	Disable
1	High	Disable	Disable
1	Low	Enable	Write data to DB17-0

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

8.36 RGB Interface Power on/off Control Register (R34h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CSHUT
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CSHUT

Figure 8. 52 RGB Interface Power On/Off Control Register (R34h)

This command is used to set chip on/ off control in RGB I/F.

CSHUT	Chip on/off in RGB I/F
0	Chip on
1	Chip off

As CSHUT command bit be written in RGB interface, the external pin SHUT control is invalid, and chip on/off selection is controlled by internal CSHUT command bit.

8.37 RGB Interface Output Direction Register (R35h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CTB	CRL
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	CTB	CRL

Figure 8. 53 RGB Interface Output Direction Control Register (R35h)

This command is used to set driver output direction control in RGB interface.

CRL: Source output direction select register in RGB interface.

CRL	Module Source Output Direction
0	Normal Direction
1	Reverse Direction

CTB: Gate output direction select register in RGB interface.

CTB	Module Gate Output Direction
0	Normal Direction
1	Reverse Direction

Note: (1) As CRL bit be written in RGB interface, the external pin RL control is invalid, CRL is operated based on external pin SMX setting.
(2) As CTB bit be written in RGB interface, the external pin TB control is invalid, CTB is operated based on external pin SMY setting.

8.38 Interface Mode Selection Register (R36h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	RCM 1	RCM 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	RCM 1	RCM 0

Figure 8. 54 Interface Mode Selection Control Register (R36h)

This command is used to set interface mode.

RCM[1:0]: RGB and MCU interface select.

RCM1	RCM0	Interface Select
0	x	System Interface(1)
1	0	RGB Interface(1) (VS+HS+DE)
1	1	RGB Interface(2) (VS+HS)

Note: (1) As RCM[1:0] bit be written, the external pin RCM[1:0] control is invalid.

8.39 Normally White/Black Control Register (R37h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	NWB
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	NWB

Figure 8. 55 Normally White/Black Control Register (R37h)

This command is used to set the characteristic of used panel.

NWB	Panel Type
0	Normally White Panel Used
1	Normally Black Panel Used

8.40 OTP Register (R38h ~ R3Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	OTP_POR	OTP_OTPEN	OTP_PPROG	OTP_PWE
R	1	*	*	*	*	*	*	*	*	*	*	*	*	OTP_POR	OTP_OTPEN	OTP_PPROG	OTP_PWE

Figure 8. 56 OTP Command 1 (R38h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	OTP_YA2	OTP_YA1	OTP_YA0	*	OTP_XA2	OTP_XA1	OTP_XA0	*
R	1	*	*	*	*	*	*	*	*	OTP_YA2	OTP_YA1	OTP_YA0	*	OTP_XA2	OTP_XA2	OTP_XA0	*

Figure 8. 57 OTP Command 2 (R39h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	OTP_VR ADJ1	OTP_VR ADJ0	*	*	OTP_PT M1	OTP_PT M0	*	*
R	1	*	*	*	*	*	*	*	*	OTP_VR ADJ1	OTP_VR ADJ0	*	*	OTP_PT M1	OTP_PT M0	*	*

Figure 8. 58 OTP Command 3 (R3Ah)

This command is used to set the OTP related setting. Please see OTP flow for detail use.

OTP_POR: for OTP read/write timing control

OTP_OTPEN: 1'b1 to select 6.5V for OTP write operation.

OTP_PPROG: 1'b1 to turn on OTP write mode.

OTP_PWE: 1'b1 to write OTP.

OTP_XA[2:0]: OTP_YA[2:0]: Select OTP writes address

OTP_TM[1:0]: OTP Test mode register, In-house use.

OTP_VRADJ[1:0]: OTP VPP2 adjusts register, In-house use.

8.41 Positive Gamma Control (R40h~R48h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MP 12	MP 11	MP 10	*	MP 02	MP 01	MP 00
R	1	*	*	*	*	*	*	*	*	*	MP 12	MP 11	MP 10	*	MP 02	MP 01	MP 00

Figure 8. 59 Positive Gamma Control 1 Register (R40h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MP 32	MP 31	MP 30	*	MP 22	MP 21	MP 20
R	1	*	*	*	*	*	*	*	*	*	MP 32	MP 31	MP 30	*	MP 22	MP 21	MP 20

Figure 8. 60 Positive Gamma Control 2 Register (R41h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MP 52	MP 51	MP 50	*	MP 42	MP 41	MP 40
R	1	*	*	*	*	*	*	*	*	*	MP 52	MP 51	MP 50	*	MP 42	MP 41	MP 40

Figure 8. 61 Positive Gamma Control 3 Register (R42h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	CP 04	CP 03	CP 02	CP 01	CP 00
R	1	*	*	*	*	*	*	*	*	*	*	*	CP 04	CP 03	CP 02	CP 01	CP 00

Figure 8. 62 Positive Gamma Control 4 Register (R43h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	CP 23	CP 22	CP 21	CP 20	CP 13	CP 12	CP 11	CP 10
R	1	*	*	*	*	*	*	*	*	CP 23	CP 22	CP 21	CP 20	CP 13	CP 12	CP 11	CP 10

Figure 8. 63 Positive Gamma Control 5 Register (R44h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	CP 33	CP 32	CP 31	CP 30
R	1	*	*	*	*	*	*	*	*	*	*	*	*	CP 33	CP 32	CP 31	CP 30

Figure 8. 64 Positive Gamma Control 6 Register (R45h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	CP 44	CP 43	CP 42	CP 41	CP 40
R	1	*	*	*	*	*	*	*	*	*	*	*	CP 44	CP 43	CP 42	CP 41	CP 40

Figure 8. 65 Positive Gamma Control 7 Register (R46h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	OP 23	OP 22	OP 21	OP 20	OP 13	OP 12	OP 11	OP 10
R	1	*	*	*	*	*	*	*	*	OP 23	OP 22	OP 21	OP 20	OP 13	OP 12	OP 11	OP 10

Figure 8. 66 Positive Gamma Control 8 Register (R47h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	CGM 11	CGM 10	CGM 01	CGM 00
R	1	*	*	*	*	*	*	*	*	*	*	*	*	CGM 11	CGM 10	CGM 01	CGM 00

Figure 8. 67 Positive Gamma Control 9 Register (R48h)

8.42 Negative Gamma Control (R50h~R57h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MN 12	MN 11	MN 10	*	MN 02	MN 01	MN 00
R	1	*	*	*	*	*	*	*	*	*	MN 12	MN 11	MN 10	*	MN 02	MN 01	MN 00

Figure 8. 68 Negative Gamma Control 1 Register (R50h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MN 32	MN 31	MN 30	*	MN 22	MN 21	MN 20
R	1	*	*	*	*	*	*	*	*	*	MN 32	MN 31	MN 30	*	MN 22	MN 21	MN 20

Figure 8. 69 Negative Gamma Control 2 Register (R51h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	MN 52	MN 51	MN 50	*	MN 42	MN 41	MN 40
R	1	*	*	*	*	*	*	*	*	*	MN 52	MN 51	MN 50	*	MN 42	MN 41	MN 40

Figure 8. 70 Negative Gamma Control 3 Register (R52h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	CN 04	CN 03	CN 02	CN 01	CN 00
R	1	*	*	*	*	*	*	*	*	*	*	*	CN 04	CN 03	CN 02	CN 01	CN 00

Figure 8. 71 Negative Gamma Control 4 Register (R53h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	CN 23	CN 22	CN 21	CN 20	CN 13	CN 12	CN 11	CN 10
R	1	*	*	*	*	*	*	*	*	CN 23	CN 22	CN 21	CN 20	CN 13	CN 12	CN 11	CN 10

Figure 8. 72 Negative Gamma Control 5 Register (R54h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	CN 33	CN 32	CN 31	CN 30
R	1	*	*	*	*	*	*	*	*	*	*	*	*	CN 33	CN 32	CN 31	CN 30

Figure 8. 73 Negative Gamma Control 6 Register (R55h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	CN 44	CN 43	CN 42	CN 41	CN 40
R	1	*	*	*	*	*	*	*	*	*	*	*	CN 44	CN 43	CN 42	CN 41	CN 40

Figure 8. 74 Negative Gamma Control 7 Register (R56h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	ON 23	ON 22	ON 21	ON 20	ON 13	ON 12	ON 11	ON 10
R	1	*	*	*	*	*	*	*	*	ON 23	ON 22	ON 21	ON 20	ON 13	ON 12	ON 11	ON 10

Figure 8. 75 Negative Gamma Control 8 Register (R57h)

Register Groups	Positive Polarity	Description
Center Adjustment	CP/N0 4-0	Variable resistor (VRTP/N) for center adjustment
	CP/N1 3-0	Variable resistor (VRCP/N0)for center adjustment
	CP/N2 3-0	Variable resistor (VRMP/N) for center adjustment
	CP/N3 3-0	Variable resistor (VRCP/N1)for center adjustment
	CP/N4 4-0	Variable resistor (VRBP/N)for center adjustment
Macro Adjustment	MP/N0 2-0	8-to-1 selector (reference voltage level of grayscale 1)
	MP/N1 2-0	8-to-1 selector (reference voltage level of grayscale 8)
	MP/N2 2-0	8-to-1 selector (reference voltage level of grayscale 20)
	MP/N3 2-0	8-to-1 selector (reference voltage level of grayscale 43)
	MP/N4 2-0	8-to-1 selector (reference voltage level of grayscale 55)
	MP/N5 2-0	8-to-1 selector (reference voltage level of grayscale 62)
Offset Adjustment	OP/N0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP/N1 3-0	Variable resistor (VROP/N1)for offset adjustment

For details, please refer to 7.2 Gamma resister stream and 8 to 1 Selector.

8.43 Display Control Internal Used (R59h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	REV_P	BGR_P	GS_P	SS_P
R	1	*	*	*	*	*	*	*	*	*	*	*	*	REV_P	BGR_P	GS_P	SS_P

Figure 8. 76 Display Control Internal used Register (R59h)

This command is internal use for display panel setting. As this command be written, the external pin REV, SRGB, SMX and SMY hardware control pins are invalid.

REV_P: The source output dat ploarity selected. When REV_P=0, data will not reverse. When REV_P = 1, the data will reverse.

BGR_P: The color filter order direction selected. When BGR_P=0, S1,S2,S3 filter order= “BGR”. When BGR_P = 1, S1,S2,S3 filter order=”RGB”..

GS_P: The gate driver output shift direction selected. When GS_P=0, the shift direction from G1 to G220. When GS_P = 1, the shift direction from G220 to G1.

SS_P: The source driver output shift direction selected. When SS_P=0, the shift direction from S528 to S1. When SS_P = 1, the shift direction from S1 to S28.

8.43 Power Control Internal Used (R60h~R63h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PTBA15	PTBA14	PTBA13	PTBA12	PTBA11	PTBA10	PTAB9	PTBA8
R	1	*	*	*	*	*	*	*	*	PTBA15	PTBA14	PTBA13	PTBA12	PTBA11	PTBA10	PTAB9	PTBA8

Figure 8. 77 Power Control Internal used (1) Register (R60h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	PTBA7	PTBA6	PTBA5	PTBA4	PTBA3	PTBA2	PTBA1	PTBA0
R	1	*	*	*	*	*	*	*	*	PTBA7	PTBA6	PTBA5	PTBA4	PTBA3	PTBA2	PTBA1	PTBA0

Figure 8. 78 Power Control Internal used (2) Register (R61h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	STBA15	STBA14	STBA13	STBA12	STBA11	STBA10	STAB9	STBA8
R	1	*	*	*	*	*	*	*	*	STBA15	STBA14	STBA13	STBA12	STBA11	STBA10	STAB9	STBA8

Figure 8. 79 Source Control Internal used (1) Register (R62h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	STBA7	STBA6	STBA5	STBA4	STBA3	STBA2	STBA1	STBA0
R	1	*	*	*	*	*	*	*	*	STBA7	STBA6	STBA5	STBA4	STBA3	STBA2	STBA1	STBA0

Figure 8. 80 Source Control Internal used (2) Register (R63h)

These commands are internal used.

PTBA[15:0]: Power control internal used.

STBA[15:0]: Source Power control internal used.

8.44 Source OP Control (R73h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	*	*	*	*	*	*	*	OPNO7	OPON6	OPON5	OPON4	OPON3	OPON2	OPNO1	OPON0
R	1	*	*	*	*	*	*	*	*	OPNO7	OPON6	OPON5	OPON4	OPON3	OPON2	OPNO1	OPON0

Figure 8. 81 Source OP Control Register (R73h)

This command is used to set the Source OP output period. It will increase the driving ability of the source driver. For example, if the user has crosstalk issue, user can adjust this command for more driving ability, the ability is more when the setting is bigger.

OPON[7:0]: Specify the valid source OP output period in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode.

8.45 Himax ID (R93h)

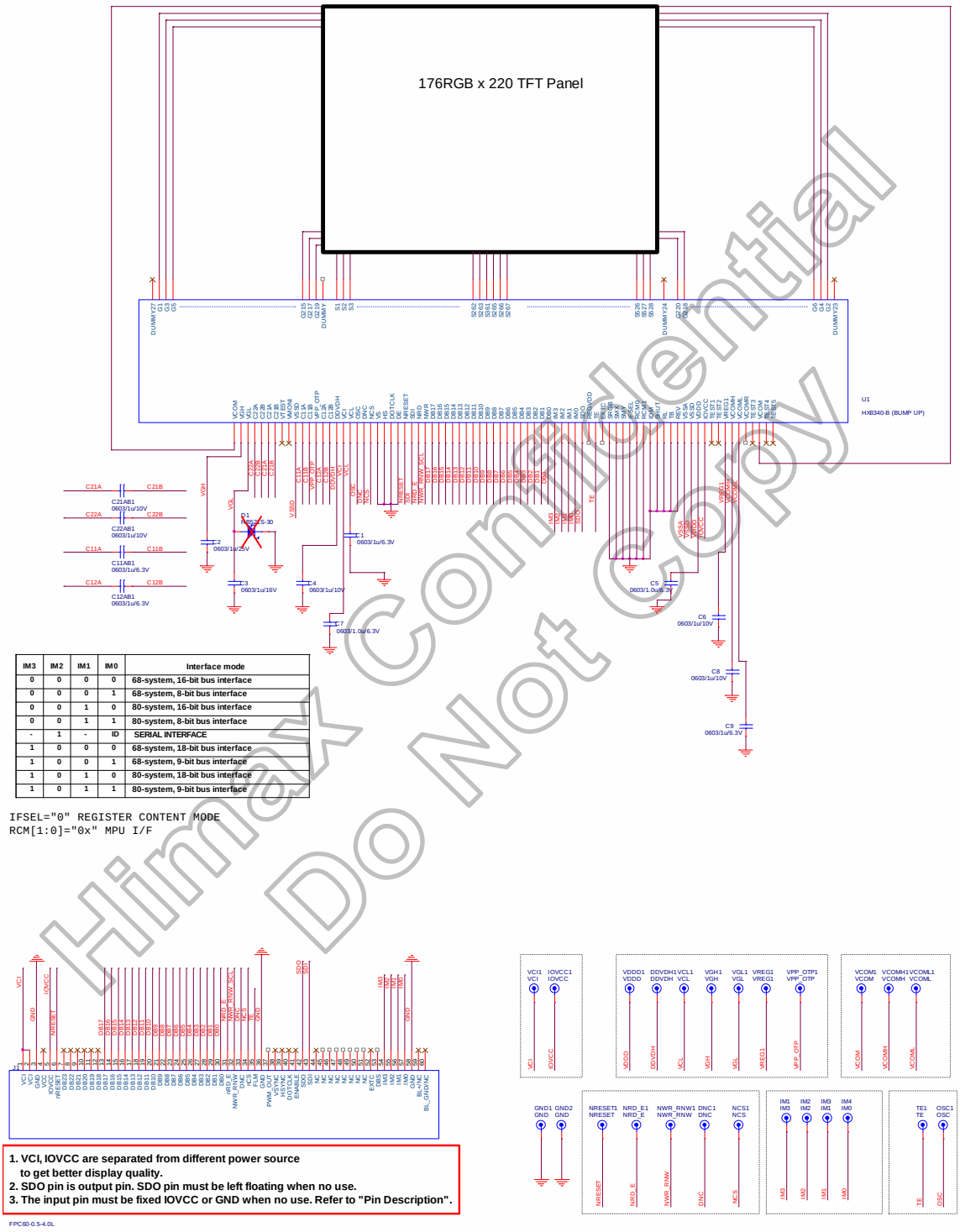
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 8. 82 Himax ID Register (R93h)

This command is used to read this IC's ID code. The ID code of this IC is 49h.

9. Layout Recommendation

9.1 Parallel Interface of Register-Content Mode



IM3	IM2	IM1	IM0	Interface mode
0	0	0	0	68-system, 16-bit bus interface
0	0	0	1	68-system, 8-bit bus interface
0	0	1	0	80-system, 16-bit bus interface
0	0	1	1	80-system, 8-bit bus interface
-	1	-	ID	SERIAL INTERFACE
1	0	0	0	68-system, 18-bit bus interface
1	0	0	1	68-system, 9-bit bus interface
1	0	1	0	80-system, 18-bit bus interface
1	0	1	1	80-system, 9-bit bus interface

IFSEL="0" REGISTER CONTENT MODE
RCM[1:0]="0x" MPU I/F

1. VCI, IOVCC are separated from different power source to get better display quality.
2. SDO pin is output pin. SDO pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

FPC60-0.5-4.0L

Figure 9. 1 Layout Recommendation of System Interface

9.2 RGB + SPI Interface of Register-Content

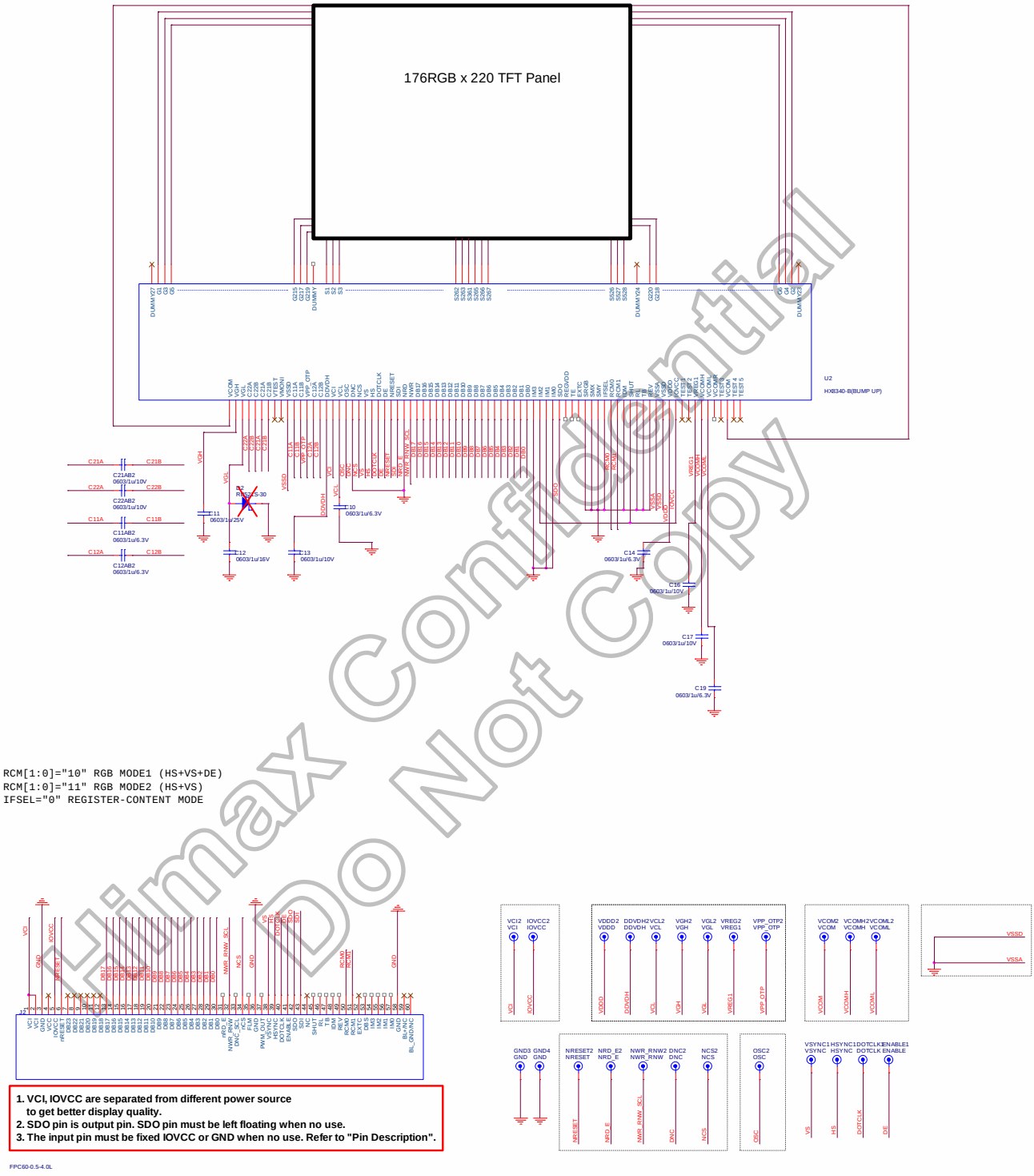


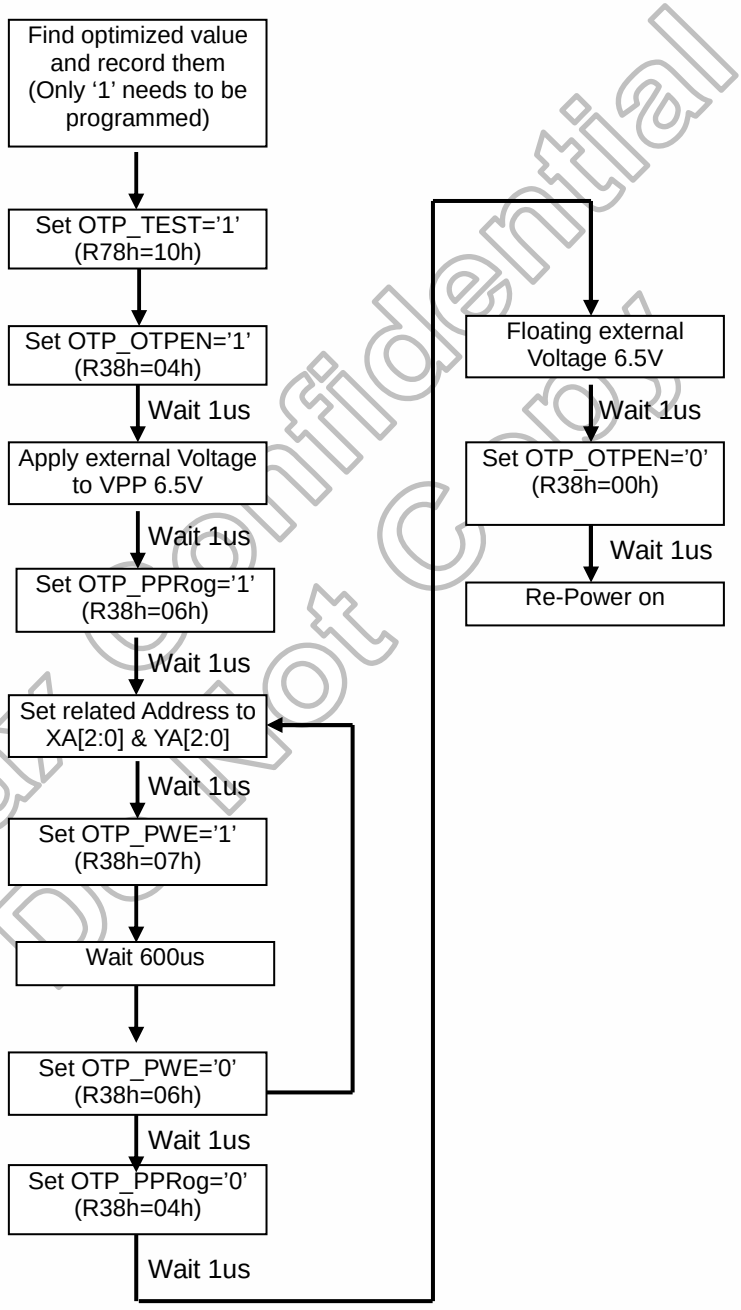
Figure 9. 2 Layout Recommendation of RGB Interface

10. OTP

	YA[2:0]=111	YA[2:0]=110	YA[2:0]=101	YA[2:0]=100	YA[2:0]=011	YA[2:0]=010	YA[2:0]=001	YA[2:0]=000	Non-Program
XA[2:0]=011	Invalid	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	00h

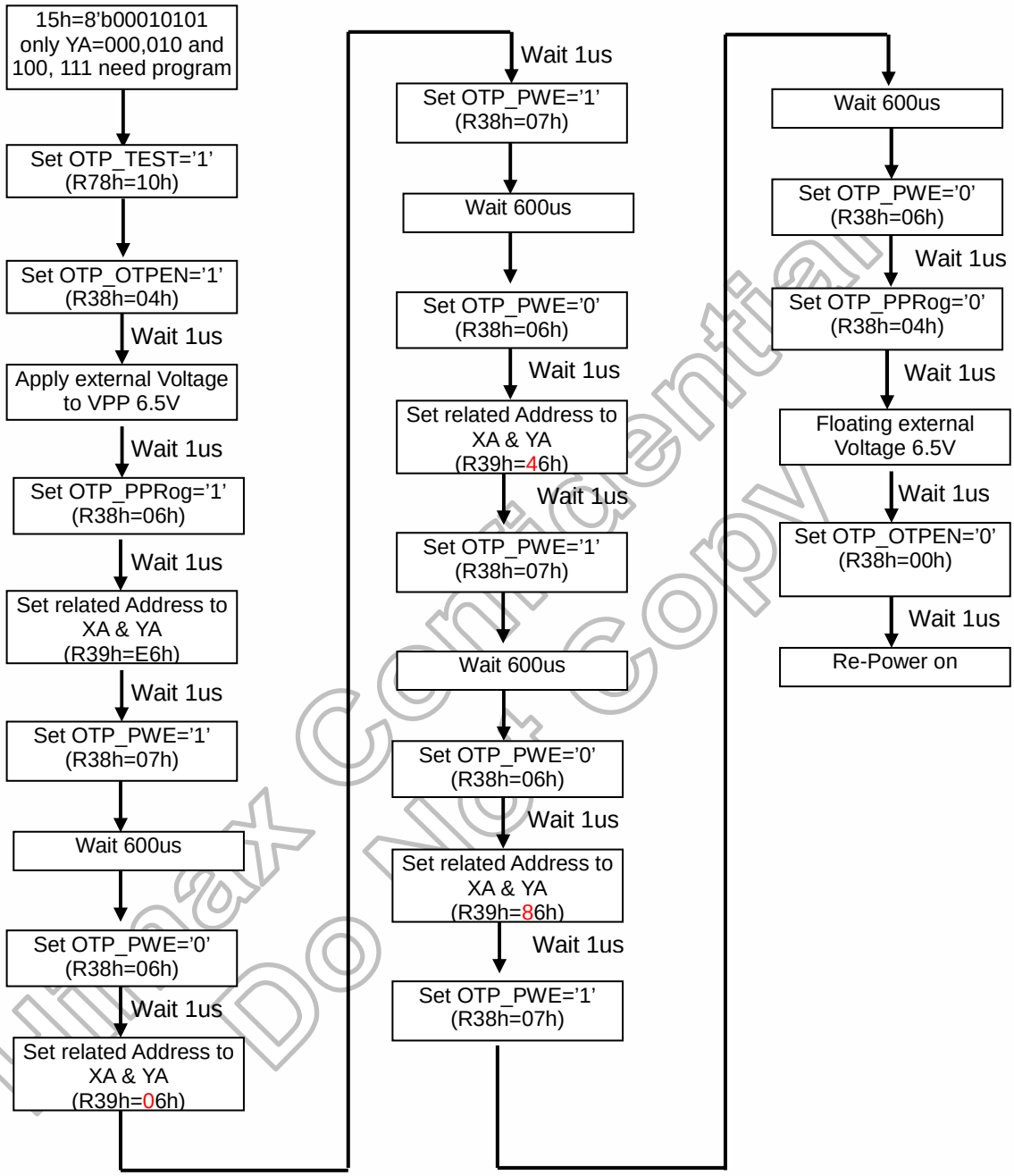
Table 10. 1 OTP ADDRESS MAPPING

OTP Programming Flow



Note: Invalid bit must program if user want use this OTP function

OTP Programming Example (VMF=15h)



11. Electrical Characteristic

11.1 Absolute Maximum Ratings

(VSS = 0V)

Item	Symbol	Value	Unit
Logic Supply voltage	IOVCC	-0.3~+3.6	V
Power Supply voltage	VCI	-0.3~+4.2	V
Logic input voltage range	Vin	-0.3~IOVCC+0.5	V
Logic Output voltage range	Vo	-0.3~IOVCC+0.5	V
Operating Temperature Range	TOPR	-20~+70	℃
Storage Temperature Range	TSTG	-40~+125	℃

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.

Table 11. 1 Absolute Maximum Ratings

11.2 ESD Protection Level

Item	Test Condition	Protection Level	Unit
Human Body Model	C=100 pF, R=1.5 kΩ	±2.0K	V
Machine Model	C=200 pF, R=0.0 Ω	±200	V

11.3 Latch-Up Protection Level

>±100 mA

11.4 Light Sensitivity

T.B.D

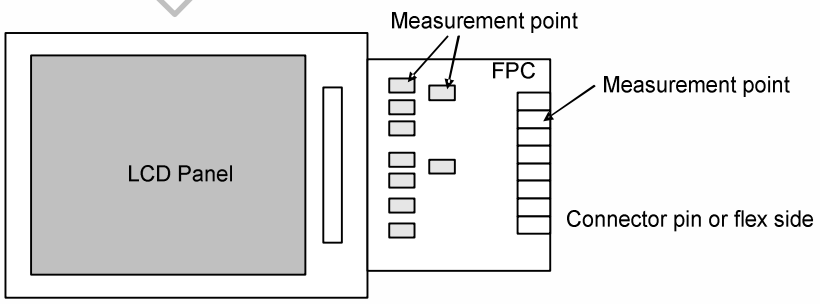
11.5 Maximum Layout Resistance

Name	Type	Maximum Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VPP_OTP	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
DBS,IM[3:0], EXTC, IFSEL0,RCM[1:0]	Input	100	Ω
NRD_E, NWR_RNW, DNC_SCL, NCS, SDI	Input	100	Ω
NRESET,SMX,SMY,SRGB,	Input	100	Ω
IDM,SHUT,RL,TB,REV	Input	100	Ω
DB[17:0], DOTCLK, DE, VS, HS	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	30	Ω
VCOMH, VCOML	Capacitor connection	30	Ω
C11A, C11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
VCOMR	Input	100	Ω
SDO, TE	Output	100	Ω

11.6 DC Characteristics

(Ta = 25° C)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Source Drive Voltage	VREG1	-	3.00	4.65	4.80	
Gate Drive High Voltage	VGH	VCI=2.8V	10.0	-	15.3	
Gate Drive Low Voltage	VGL	VCI=2.8V	-13.5	-	-7.5	
Drive Supply Voltage	|VGH-VGL|	VCI=2.8V	17.5	-	28.8	
Input / Output						
High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1.0	-	1.0	µA
Oscillator frequency	fOSC	VCI=2.8V	2.40	2.52	2.60	MHz
Booster						
AVDD boost voltage1	DDVDH	IAVDD=1mA VCI=2.8V	4.9	-	5.3	V
VCL boost voltage	VCL	ICL=-300uA VCI=2.8V	-2.6	-	-2.8	
VCOM Generator						
VCOM amplitude	VCOM	No load	3.0	-	7.3	V
VCOM high level	VCOMH	No load	3.0	-	4.8	V
VCOM low level	VCOML	No load	-2.5	-	0.0	V
Source Driver						
Output voltage deviation	DVOS	VSSD+1.0 ~ VREG1-1.0	-	-	20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	-	30	mV
Others						
OTP Programming Voltage	VPP_OTP	Programming mode	6.3	6.5	6.7	V



11.6.1 Current Consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption	
						Typical	Worst case
						VCI (mA)	VCI (mA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	Line	Note(1)	X;X;X	2.30	4.35
			Line	Note(2)	X;X;X	2.10	4.10
			Line	Note(3)	X;X;X	2.20	4.30
			Line	Note(4)	X;X;X	2.00	4.15
			Line	Note(5)	X;X;X	2.00	4.15
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	60Hz	Line	Note(5)	X;X;X	1.70	3.50
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	60Hz	Line	Grey Levels	X;X;X	1.20	2.70
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode On - Sleep Out Mode	60Hz	Line	Note(6)	X;X;X	0.80	2.45
			Line	Note(7)	X;X;X	0.99	2.55
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	0.005	0.080
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	Line	262k Colors Note(8) CPU Access @ 25fps	0;0;0	3.50	6.4
					0;0;1	3.50	6.4
					0;1;0	3.50	6.4
					0;1;1	3.50	6.4
					1;0;0	3.50	6.4
					1;0;1	3.50	6.4
					1;1;0	3.50	6.4
					1;1;1	3.50	6.4

Typical Case:
T_A = 25oC
IOVCC=1.8V
VCI = 2.8V

Worst Case:
T_A = -30 to70oC
IOVCC = 1.65V to 3.3V
VCI = 2.5V to 3.3V
Includes Process Variance.

Note: X Do not care
(1) All pixels black
(2) Checker board one by one
(3) Checker board 4 by 4
(4) Grey-scale from top to bottom
(5) 20% Black, 80%White
(6) Black & White Checker board 8 by 8.
(7) Absolute Worst Case Patterns: Defined by Display Supplier
(8) Absolute Worst Case Patterns and Sequences: Defined by Display Supplier
(9) Absolute worst case VCI current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.
(10) Absolute worst case IOVCC current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.
(11) Inrush currents are not included in current consumption values

11.7 AC Characteristics

11.7.1 Parallel Interface Characteristics (8080-Series MPU)

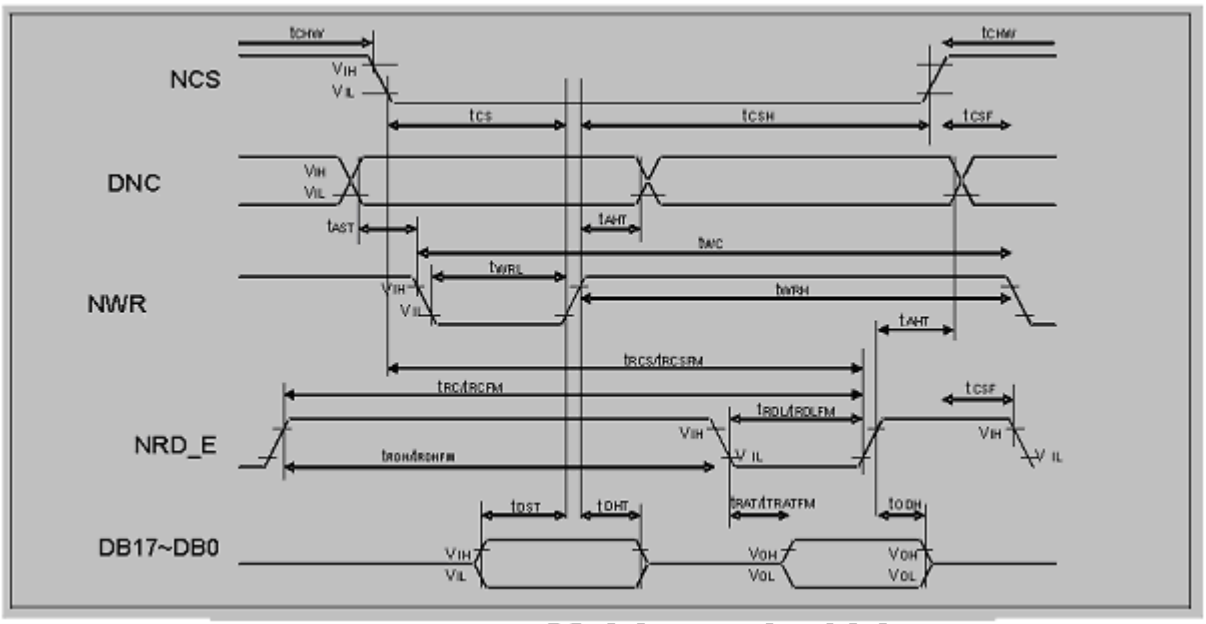


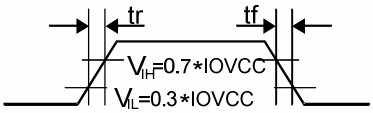
Figure 11. 1 Parallel Interface Characteristics (8080-Series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70° C)

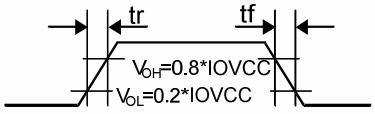
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	15	-		
	t_{RCS}	Chip select setup time (Read ID)	45	-		
	t_{RCSFM}	Chip select setup time (Read FM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
	t_{CSH}	Chip select hold time	10	-		
NWR_RNW	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	15	-		
NRD_E (ID)	t_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	90	-		
	t_{RDL}	Control pulse "L" duration (ID)	45	-		
NRD_E (FM)	t_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	90	-		
	t_{RDLFM}	Control pulse "L" duration (FM)	355	-		
D15 to D0	t_{DST}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RAT}	Read access time (ID)	-	40		
	t_{RATFM}	Read access time (FM)	-	340		
	t_{ODH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



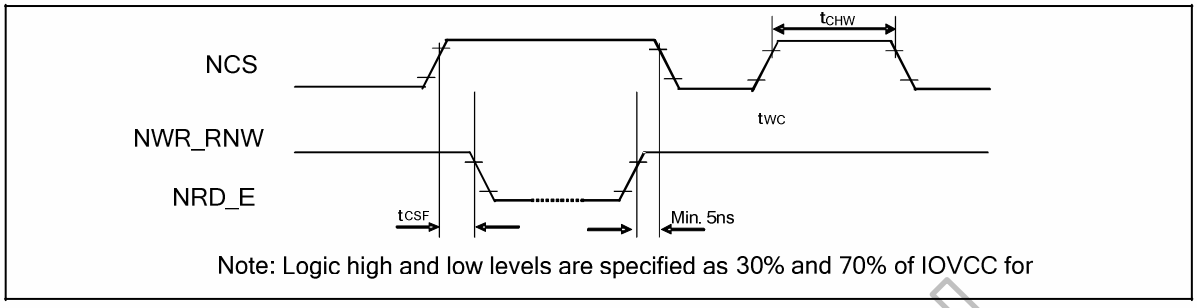


Figure 11. 2 Chip Select Timing

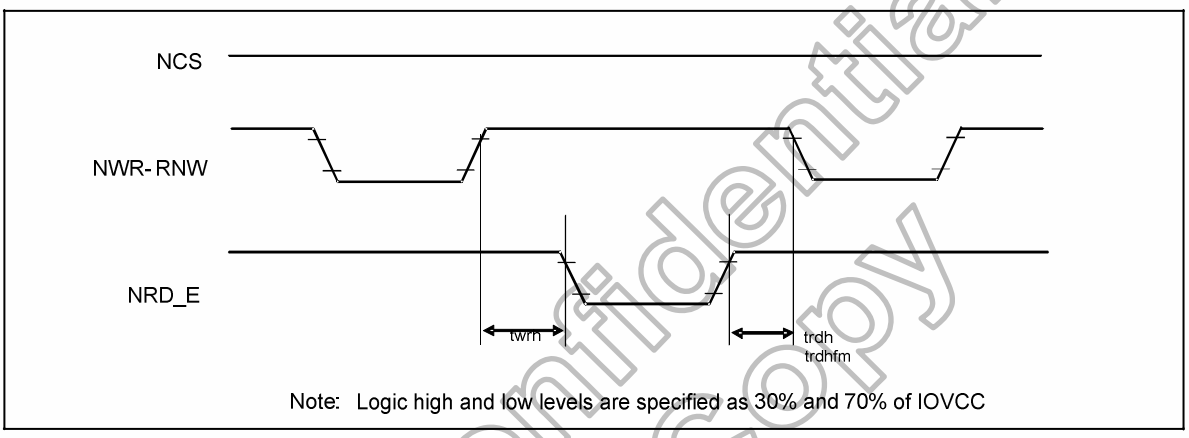


Figure 11. 3 Write to Read and Read to Write Timing

11.7.2 Parallel Interface Characteristics (6800-Series MPU)

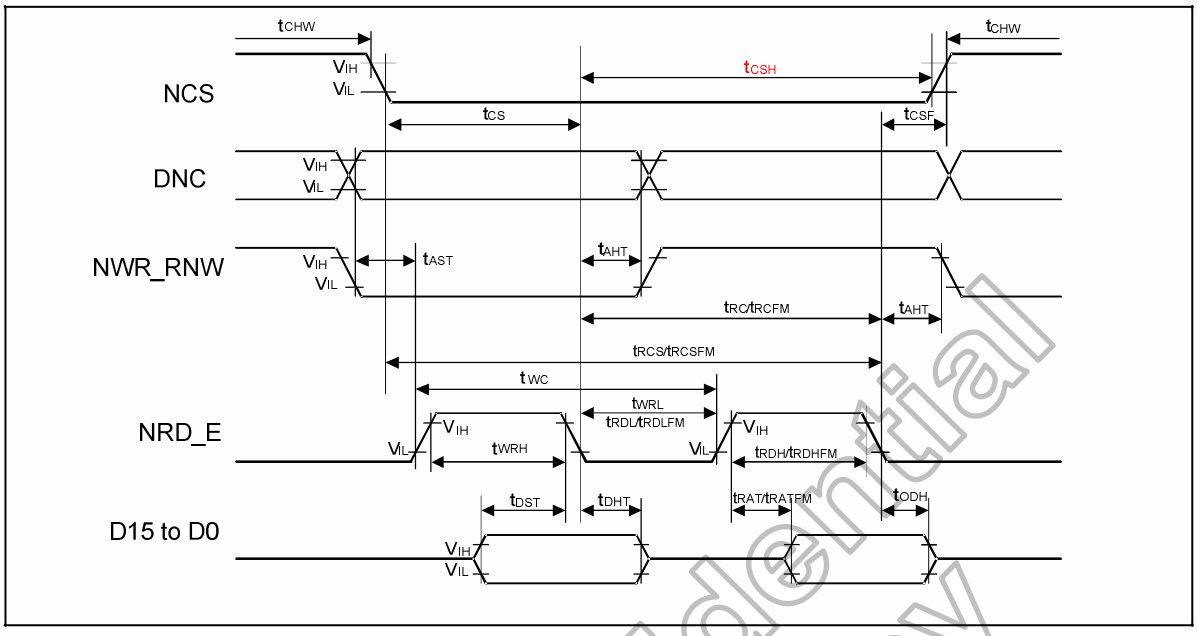


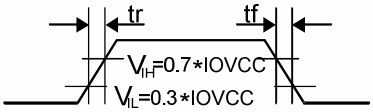
Figure 11. 4 Parallel Interface Characteristics (6800-Series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70° C)

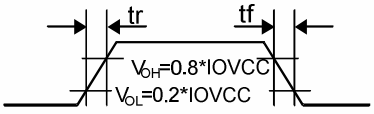
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	15	-		
	t_{RCS}	Chip select setup time (Read ID)	45	-		
	t_{RCSFM}	Chip select setup time (Read FM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
	t_{CSH}	Chip select hold time	10	-		
NWR_RNW	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	15	-		
NRD_E (ID)	t_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	90	-		
	t_{RDL}	Control pulse "L" duration (ID)	45	-		
NRD_E (FM)	t_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	90	-		
	t_{RDLFM}	Control pulse "L" duration (FM)	355	-		
D17 to D0	t_{dst}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RAT}	Read access time (ID)	-	40		
	t_{RATFM}	Read access time (FM)	-	340		
	t_{ODH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



11.7.3 Serial Interface Characteristics

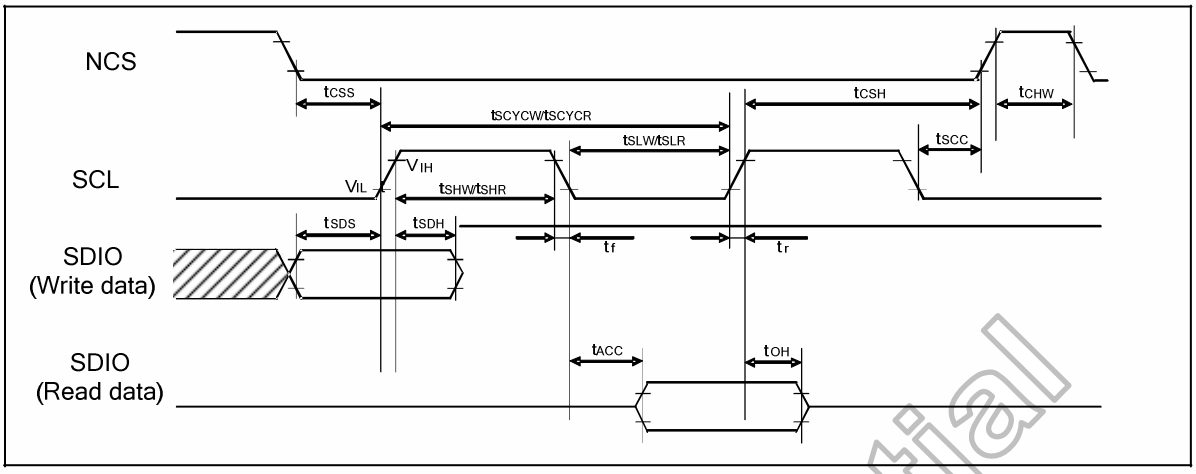


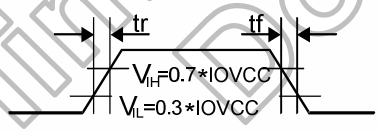
Figure 11. 5 Serial Interface Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70° C)

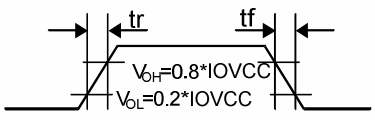
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	20 8 8	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDIO	8 8	- -	- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDI for maximum C_L=30pF For minimum C_L=8pF	10	-	50	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	50	ns
SCL to Chip select	t_{SCC}	SCL, NCS	20	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	40	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	15 15	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

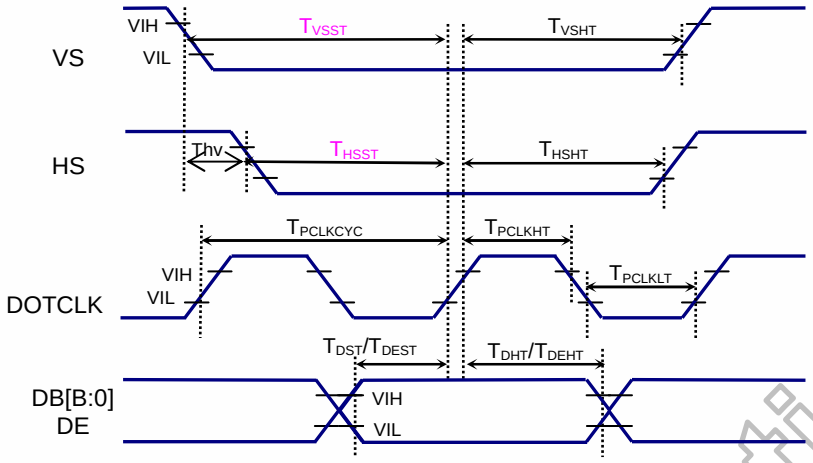
Input Signal Slope



Output Signal Slope



11.7.4 RGB Interface Characteristics

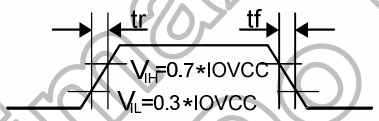


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,Ta = -30 to 70° C)

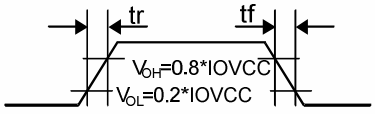
Item	Symbol	Condition	Spec.			Unit
			Min	Type.	Max	
Pixel low pulse width	T_{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T_{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T_{VSST}	-	15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Data Enable set-up time	T_{DEST}	-	15	-	-	ns
Data Enable hold time	T_{DEHT}	-	15	-	-	ns
Data set-up time	T_{DST}	-	15	-	-	ns
Data hold time	T_{DHT}	-	15	-	-	ns
Phase difference of sync signal falling edge	Thv	-	0	-	176	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

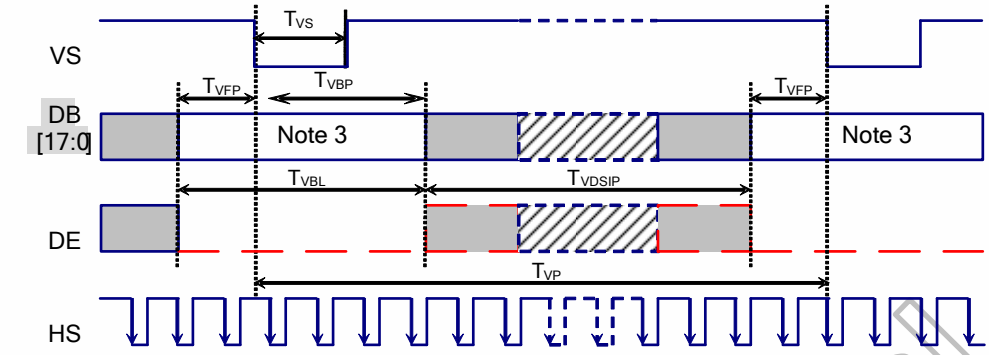
Input Signal Slope



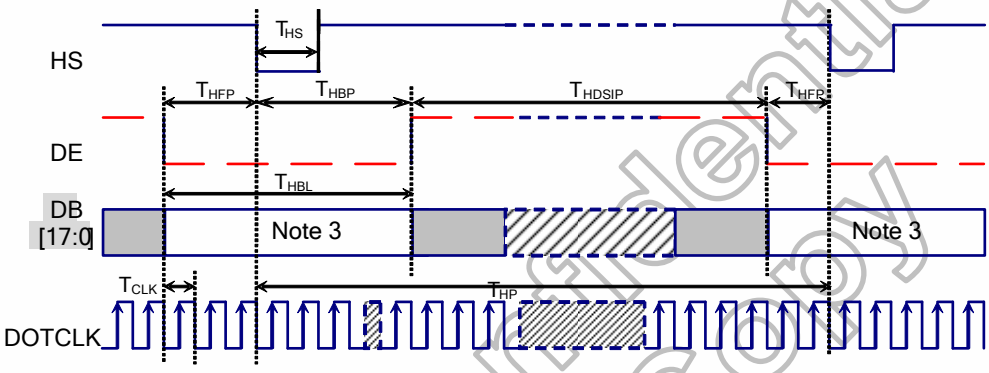
Output Signal Slope



Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



Item	Symbol	Condition	Spec.			Unit
			Min.	Type.	Max.	
Vertical Timing						
Vertical cycle period	T_{VP}	-	224	228	511	HS
Vertical low pulse width	T_{VS}	-	2	2	-	HS
Vertical front porch	T_{VFP}	-	2	2	-	HS
Vertical back porch	T_{VBP}	-	2	6	254	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	8		HS
Vertical active area	T_{VDISP}	-	-	220	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	180	184	255	DOTCLK
Horizontal low pulse width	T_{HS}	-	2	2	-	DOTCLK
Horizontal front porch	T_{HFP}	-	2	2	-	DOTCLK
Horizontal back porch	T_{HBP}	-	2	6	62	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	4	8	-	DOTCLK
Horizontal active area	T_{HDISP}	-	-	176	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	2.0	2.52	10.0	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of DOTCLK.

11.7.5 Reset Input Timing

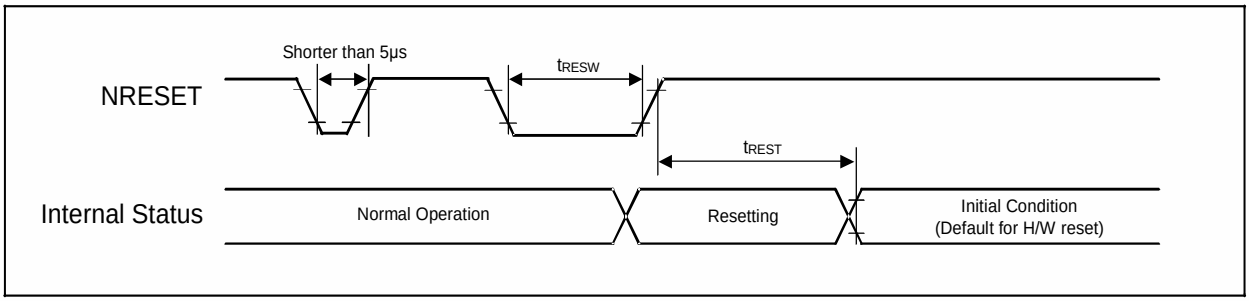


Figure 11. 6 Reset Input Timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	NRESET	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	-	-	5	When reset applied during Sleep In mode	ms
		-		-	120	When reset applied during Sleep Out mode	ms

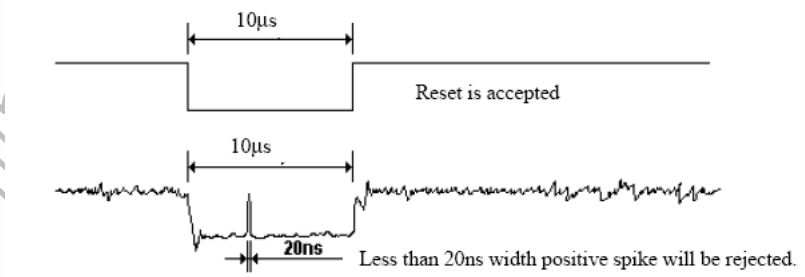
Note: (1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:

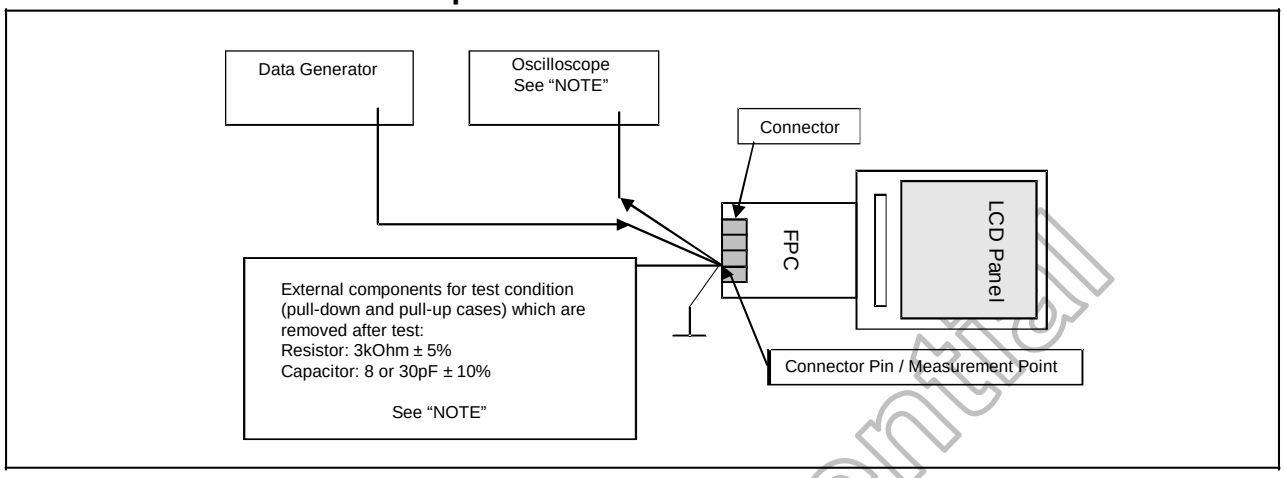


(5) It is necessary to wait 5msec after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120ms.

11.7.6 Measurement Conditions

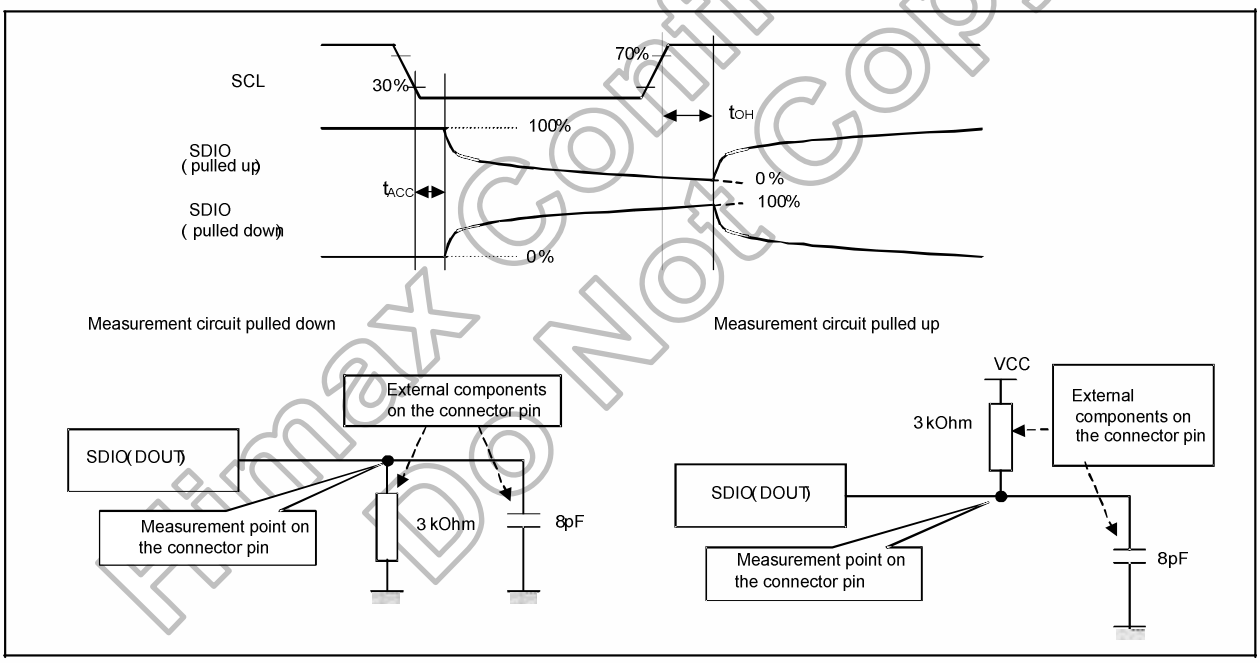
11.7.6.1 tACC, tOH Measurement Condition

Measurement Condition Set-up

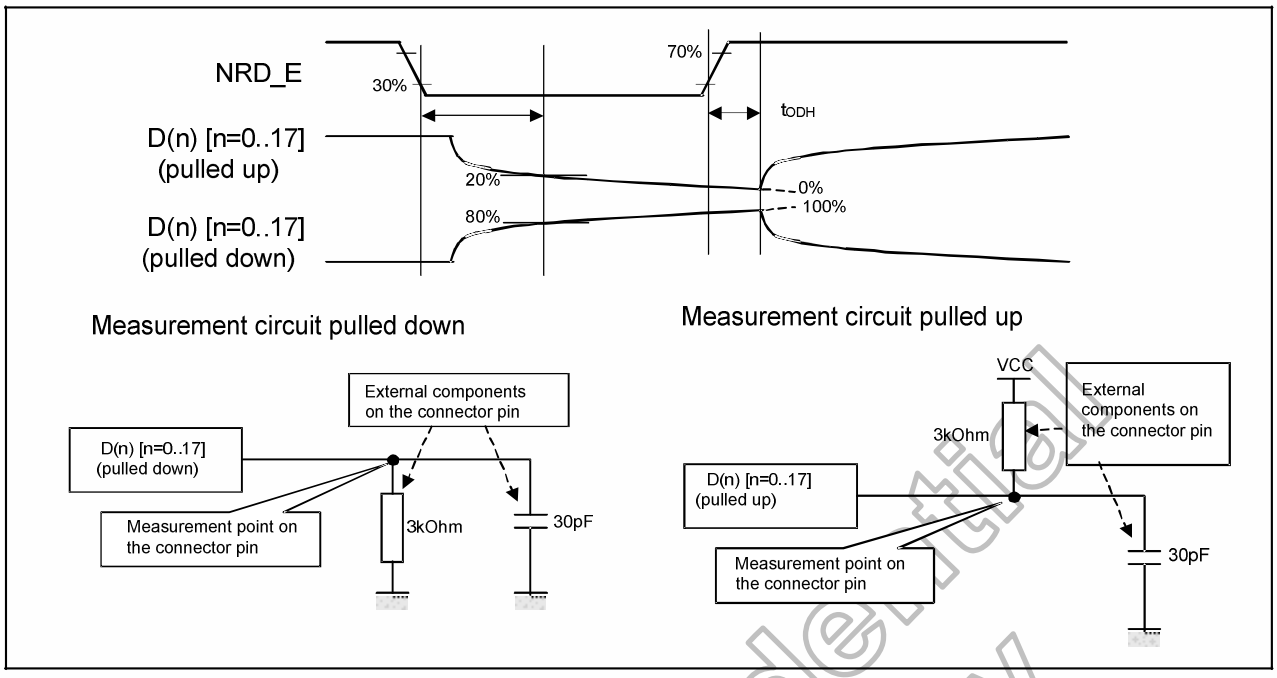


Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Minimum Value Measurement



Maximum Value Measurement



12. Ordering Information

Part No.	Package
HX8340-B000 PDxxx	PD : mean COG xxx : mean chip thickness (µm), (default: 300µm)

13. Revision History

Version	Date	Description of Changes
01	2007/10/05	New setup
	2007/11/01	1. P9, modify IFSEL= 'L' for Register-Content interface. 2. P10, modify IOVCC =1.65~3.3V, VGH=+9.0~+15.6V 3. P11, modify Block Diagram add RL, TB, SHUT, REV, IDM pins 4. P12, modify DNC and NWR pin description. 5. P15, modify VGH max voltage =15.6V 6. P29, modify M68 read/write timing. 7. P84. modify Figure 7.19 Gamma Resister Stream and Gamma Reference Voltage 8. P85, modify Table 7.4 Center Adjustment 9. P87, modify Table 7.6 Voltage Calculation Formula 10. P97~P99, modify System interface power on flow. 11. P103, update command R1Fh default to 03h. 12. P104, update command R38h~R3Ah OTP related register. 13. P105, update R01h command, remove DISP bit and modify SLP definition. 14. P136, update command R38h~R3Ah OTP related register. 15. P140~P141, modify Layout Recommendation 16. P142, update OTP table and OTP programming flow.
	2007/11/12	1. P85, modify Gamma Table 7.4 Center Adjustment 2. P85, modify Gamma Table 7. 6 Voltage Calculation Formula
	2007/11/14	1. P27, Table 5. 2 Data Pin Function for I80 Series CPU 2. P27, Table 5. 3 Data Pin Function for M68 Series CPU 3. P50, Figure 5. 9 Index Register Read/Write Timing in Serial Bus System Interface 4. P87, Table 7. 6 Voltage Calculation Formula 5. P97~P99, 7.5.1 System Interface Power On/Off Sequence 6. P103, 8.1 Command Table 7. P105, 8.3 Display Mode Control Register (R01h)
	2007/12/03	1. P13, modify SHUT Pin description. 2. P97~P99, 7.5.1 System Interface Power On/Off Sequence 3. P100, modify RGB mode Power on AC timing 4. P103, modify Command Table. 5. P105, modify Display mode control Register R01h 6. P139, modify OTP command 2 R39h 7. P142, update Chapter 10. OTP programming

Version	Date	Description of Changes
	2008/01/18	1. P10, modify DDVDH voltage to typical 5.1V 2. P12, modify Pin description of TE and SRGB 3. P50, modify Table 5. 12 The Function of RS and R/W Bit 4. P97~P99, modify 7.5.1 System Interface Power On/Off Sequence 5. P105, add register R60h~R63h and R73h to register table 6. P106, modify R01h scroll bit, this bit can not be read 7. P123, modify R20h power control 8 register, change DDVDH voltage to typical 5.1V 8. P134, modify register R31h HBP and R32h VBP 9. P141, add 8.43 Power Control Internal Used register R60h~R63h and Source OP Control R73h 10.P142, modify Figure 9. 1 Layout Recommendation of System Interface 11.P142, modify Figure 9. 2 Layout Recommendation of RGB Interface 12.P143~P145, modify chapter 10 OTP function 13.P145 modify 11.2 ESD protection level
	2008/02/19	1. P12 modify Pin description of HS and VS 2. P16 modify Pin description of dummy 18 and dummy19 3. P117 modify R18h OSC control register 4. P123 modify VCL mapping voltage 5. P142 add 8.45 Himax ID register 6. P147 update latch-up protection level 7. P149 update 11.6 DC Characteristics 8. P150 update 11.6.1 current consumption 9. P154 update serial interface AC timing
	2008/03/07	1. P22~P23 add alignment mark B1 and B2 2. P52~P53 modify look-up table 3. P141 add register R59h display control internal use