DATA SHEET

(DOC No. HX8345-A-DS)

HX8345-A

128RGB x 160dot, 262k color, with internal RAM, TFT controller driver

Preliminary Version 01 Sep., 2006

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This manual is described the Himax's HX8345-A 128RGB*160 dots resolution driving controller. The HX8345-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 128RGB*160 dots at maximum.

The HX8345-A has five system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, an 68-system 18-/16-/9-/8-bit bus interface, VSYNC interface (internal clock, DB17-0) , serial data transfer interface and RGB18-/16-/6-bit bus interface (DOTCLOCK, VSYNC, HSYNC, ENABLE, PD17-0). In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers. The HX8345-A also supports various functions to reduce the power consumption of a LCD system via software control, such as an standby mode, sleep mode and 8-color display mode,

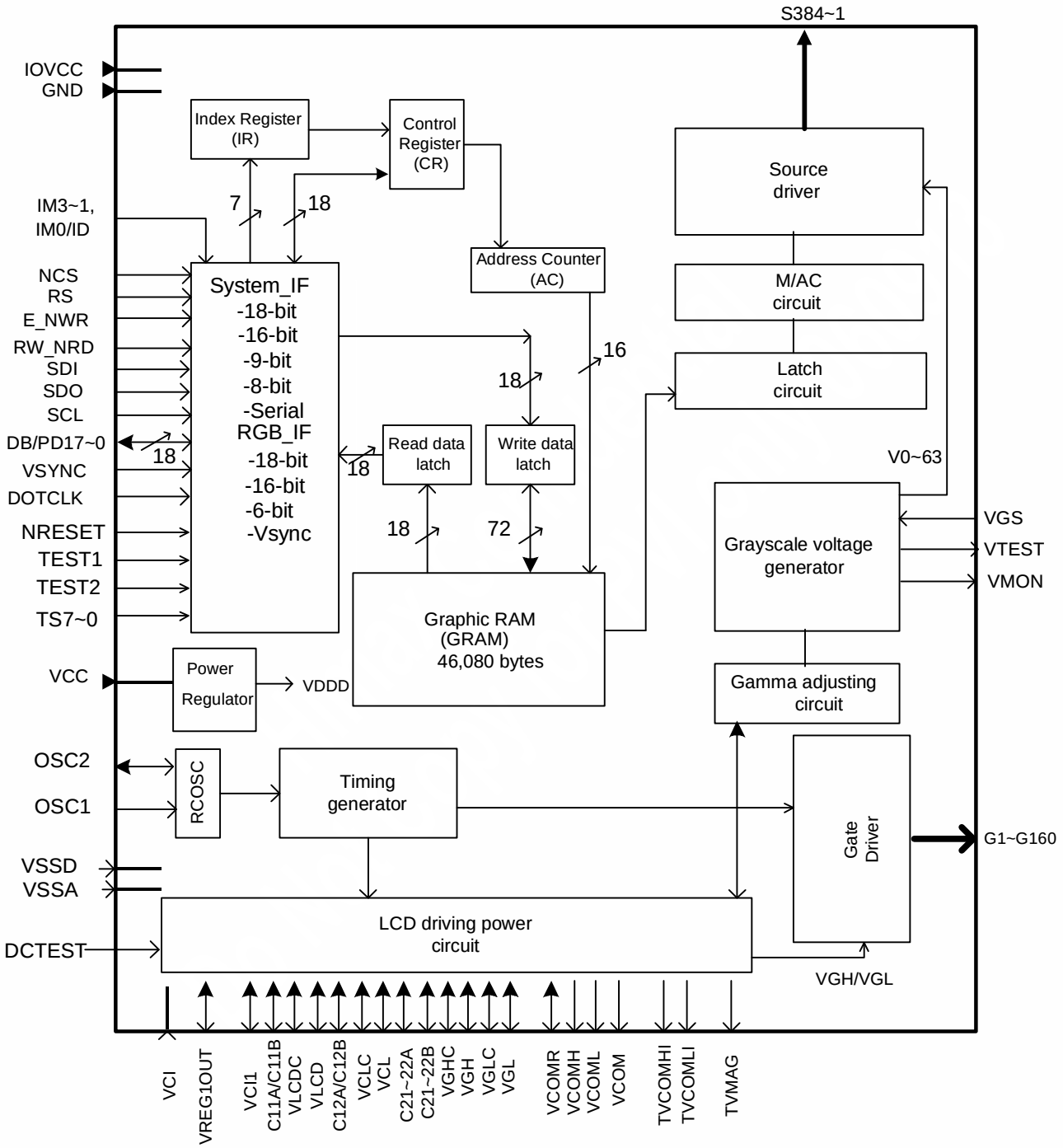
The HX8345-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

- Single chip solution to drive a TFT panel
- 128RGB x 160-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support interface:
  - 80 system interface (8-/9-/16-/18-bit bus)
  - 68 system interface (8-/9-/16-/18-bit bus)
  - Serial Data Transfer Interface
  - RGB interface (6-/16-/18-bit bus)
  - VSYNC data transfer interface
- Internal graphics RAM capacity: 46,080 bytes
- The 262,144 colors can be displayed at the same time with gamma correction
- The vertical scroll display function in line units
- Internal operation circuit of liquid crystal display:
  - Source channel: 384
  - Gate line: 160
- To write data in a window-RAM address area by using a window-address function
- Bit-operation functions for graphics transaction:
  - The write data mask function in bit unit
  - The logical operation in pixel unit and conditional write function
- Low-power consumption architecture supports:
  - VCI = 2.5 to 3.3 V (internal reference voltage)
  - IOVCC = 1.65 to 3.3 V (Interface IO)
  - VCC = 2.4 to 3.3 V (corresponding low-voltage operation)
  - VLCD = 4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - standby mode
    - sleep mode
- n-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Internal oscillator and hardware reset function
- γ - correction function which makes 262,144 colors available simultaneously
- Vertical scrolling function
- Step–up circuit to step up liquid crystal driving voltages up to 6 times

3. Device Overview

3.1 Block Diagram



3.2 Pin Description

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Descriptions</th></tr>
<tr><td>IM3~0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>Select the MPU interface mode as listed below
<table>
<tr><th>IM0(ID)</th><th>IM1</th><th>IM2</th><th>IM3</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit interface, 68-system</td><td>DB17-10, 8-1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8-bit interface, 68-system</td><td>DB17-10-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit interface, 80-system</td><td>DB17-10, 8-1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit interface, 80-system</td><td>DB17-10</td></tr>
<tr><td>ID</td><td>0</td><td>1</td><td>0</td><td>Serial data transfer interface</td><td>DB1-0</td></tr>
<tr><td>*</td><td>1</td><td>1</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>18-bit interface, 68-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9-bit interface, 68-system</td><td>DB17-9</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit interface, 80-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>9-bit interface, 80-system</td><td>DB17-9</td></tr>
<tr><td>*</td><td>*</td><td>1</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
</table>
Note: If the serial data transfer interface was selected, IM0 pin is used like the ID setting for the device code in transfer data.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>MPU</td><td>The signal for register index or register command select.
Low: Register index or internal status (in read operation);
High: Register command.
Conn ct to IOVCC or VSSD level when serial data transfer interface is selected.</td></tr>
<tr><td>E_NWR</td><td>I</td><td>1</td><td>MPU</td><td>In 80-system bus interface mode, serves as a write strobe signal. Write data at “low” level. In 68-system Interface mode, serves as an ENABLE signal to control data read/write operation.</td></tr>
<tr><td>RW_NRD</td><td>I</td><td>1</td><td>MPU</td><td>Low: Write! High: Read
Serves as a read signal and reads data at the low level in I80 system interface. Fix it to IOVCC or VSSD level when using serial data transfer interface.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVCC level.
Low: Selected (access enabled)
The polarity of the ENABLE signal is inverted by the EPL bit.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>Enable</td><td>Update</td></tr>
<tr><td>0</td><td>1</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>0</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>1</td><td>Enable</td><td>Update</td></tr>
</table></td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td>Serial data transfer input in serial data transfer interface mode. Data would be latched on the rising edge of the SCL signal. Fixed to either IOVCC or VSSD if not in use.</td></tr>
<tr><td>SCL</td><td>I</td><td>1</td><td>MPU</td><td>A synchronizing clock signal in serial data transfer interface mode. Fixed to either IOVCC or VSSD if not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. The polarity of the VSYNC signal is selected by VSPL bit.
0: Start in the low level, 1: Start in the high level
Fix to the IOVcc level when not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. The polarity of the HSYNC signal is selected by HSPL bit.
0: Start in the low level, 1: Start in the high level.
Fix to the IOVcc level when not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal. Fix to the IOVCC level when not used.
If DPL=0: Data are input on the rising edge of DOTCLK.
If DPL=1: Data are input on the falling edge of DOTCLK.</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
NRESET	I	1	MPU or reset circuit	Reset pin. Setting this pin low initializes the LSI. Must be reset after power is supplied.
VCOMR	I	1	Variable Resistor or open	A VCOMH reference voltage input. When adjusting VCOMH externally, set a register to halt the VCOMH internal adjusting circuit. Otherwise, leave this pin open and adjust VCOMH by setting the internal register of the HX8345-A.
VLCD	I	1	Stabilizing capacitor, VLCDC	An output from the step-up circuit1, of twice the VCI1 level. Connect to a stabilizing capacitor 1uF between VLCD and VSSD. Place a Schottky barrier diode between VCI and VLCD. (See “configuration of the power supply”).VLCD=4.0 to 5.5V Connect to VLCDC.
VGH	I	1	Stabilizing capacitor, VGHC	An output from the step-up circuit2.or 4~6 time the VCI1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor 1uF between VGH and VSSD. Place a Schottky barrier diode between VCI and VGH. (See “configuration of the power supply”). Max. VGH=16.5V. Connect to VGHC.
VGL	I	1	Stabilizing capacitor, VGLC	An output from the step-up circuit2.or -3~-5 time the VCI1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor 1uF between VSSD and VGL. Place a Schottky barrier diode between VSSD and VGL. (See “configuration of the power supply”). Min. VGL = -16.5V Connect to VGLC.
VCL	I	1	VCLC	A power supply for the VCOML level. Connect to a stabilizing capacitor 1uF between VSSD and VCL. VCL=0 ~ -3.3V Connect to VCLC.
TEST1	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
TEST2	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel use.
VCI	I	1	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VCILVL	I	1	Power supply	Generates a reference voltage (VCI1OUT, REGP) from the VCILVL level according to the ratio determined by the VC2-0 BITS. Connect to VCI on the FPC.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial data transfer output in serial data transfer interface mode. Data would be output on the falling edge of the SCL signal. When SDO is not used, leave it open.
S1~384	O	384	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0, DATA IN THE ram address "0000" is output from S1.If SS=1, the same data in the ram address "0000" is output from S384. S1,S4,S7,…display red (R),S2,S5,S8,…display green (G),and S3,S6,S9,…display blue(B) (SS=0, BGR=0).
G1~160	O	160	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM	O	2	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel.
VCOMH	O	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	O	1	Stabilizing capacitor or open	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VCOML output stops and a capacitor for stabilization is not needed.
FLM	O	1	MPU or open	A frame start pulse output (amplitude: IOVCC-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it
VLCDC	O	1	VLCD	A power supply for the source driver outputs. A reference voltage for the step-up circuit2. Connect to VLCD.
VGHC	O	1	VGH	A power supply for the TFT LCD's gate driver. Connect to VGH.
VGLC	O	1	VGL	A power supply for the TFT LCD's gate driver. Connect to VGL.
VCLC	O	1	VCL	An output from the step-up circuit of 1-tme the VCI1 level. VCLC=0~-3.3V
TS0~7	O	8	Open	Test pins. Disconnect them.
VMON	O	1	Open	A test pin. Disconnect it.
IOVCCDUM1	O	1	Input pin	Internal IOVCC level outputs. When adjacent input pins are fixed to the IOVCC level, short-circuit them.
IOGNDDUM 1~3	O	3	Input pin	Internal VSSD level outputs. When neighboring input pins are fixed to the VSSD level, short-circuit them.
VTESTOUT	O	1	-	A test pin. Disconnect it.
TVCOMHI	O	1	Stabilizing capacitor	A reference voltage for VCOMH. Must be connected with the capacitor 0.1uF.
TVCOMLI	I/O	1	Open	A test pin. Disconnect it
TVMAG	O	1	Stabilizing capacitor	A reference voltage for VCOML. Must be connected with the capacitor 0.1uF.
VDDD	O	4	Stabilizing capacitor	A stabilizing capacitor for logic power. Connect with the capacitor 1uF.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B C21A, C21B C22A, C22B	I/O	8	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0~17/PD0~17	I/O	18	MPU	When Operates in system interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB17-DB10 9-bit bus: use DB17-DB9 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use PD17-PD12 16-bit bus: use PD17-PD13 and PD11-PD1 18-bit bus: use PD17-PD0 Connected unused pins to the IOVCC or VSSD level.
REGP	I/O	1	Test pin	A test pin for VREG1OUT. Disconnect it.
VCI1OUT	I/O	1	Stabilizing Capacitor	A reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
VREG1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM between VSSD and VGL from the reference voltage between VCI and VSSD that is generated internally. The factor of step-up can be set through an internal register. Connect a capacitor for stabilization. As it is the reference voltage for generating VgoffOUT. Connect to an external power supply lower than VGL, if not using the adjustment circuit 2.
TESTO1, 2	-	2	Open	Dummy pads. Disconnect them.
DUMMY1~28	-	28	Open	Dummy pads. Disconnect them.
DUMMYR1~4	-	4	Open	Dummy pads. Disconnect them.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCC	P	1	Power supply	A power supply for the internal logic. VCC = 2.4 ~ 3.3V
IOVCC	P	1	Power supply	Power supply for interface pin. IOVCC = 1.65 ~3.3 V. Connected to VCC on the FPC if IOVCC = VCC for preventing noise when using the COG method.
VSSD	P	1	Power supply	Ground for the logic side. VSSD = 0V
VSSA	P	1	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.

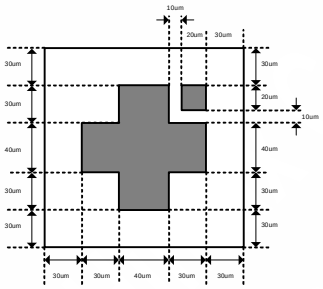
3.3 Pin assignments

. Chip Size : 12312 um x 832 um
(Including Seal ring 16um *2,
Scribe line 40um *2)
. Chip thickness :400um (typ.)
. Pad Location : PAD center
. Coordinate Origin : Chip Center
. Au Bump Size :
1. 50um x 120um
Input/Output

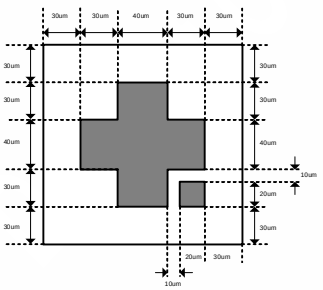
2. 20um x 96um
Staggered LCD output side

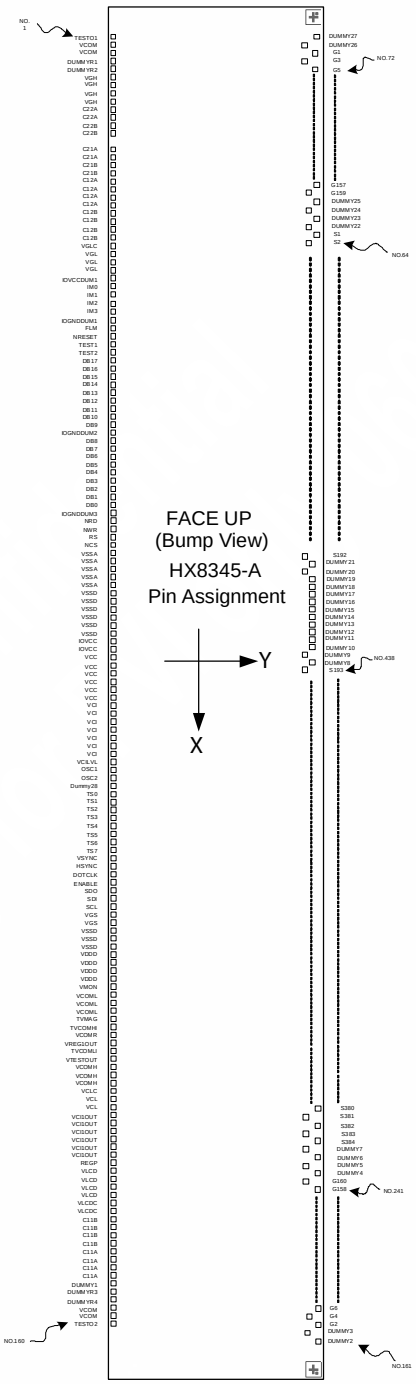
. Alignment Mark

A1: Coordinate (X,Y) = (-6015, +275)



A2: Coordinate (X,Y) = (+6015, +275)





PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	TESTO1	-5795	-295	61	E_NWR	-1595	-295	121	VCOML	2830	-295	181	G38	5410	307
2	VCOM	-5725	-295	62	RS	-1525	-295	122	TVMAG	3015	-295	182	G40	5390	182
3	VCOM	-5655	-295	63	NCS	-1455	-295	123	TVCOMHI	3085	-295	183	G42	5370	307
4	DUMMYR1	-5585	-295	64	VSSA	-1385	-295	124	VCOMR	3155	-295	184	G44	5350	182
5	DUMMYR2	-5515	-295	65	VSSA	-1315	-295	125	VREG1OUT	3225	-295	185	G46	5330	307
6	VGH	-5445	-295	66	VSSA	-1245	-295	126	TVCOMLI	3295	-295	186	G48	5310	182
7	VGH	-5375	-295	67	VSSA	-1175	-295	127	VTESTOUT	3415	-295	187	G50	5290	307
8	VGH	-5305	-295	68	VSSA	-1105	-295	128	VCOMH	3555	-295	188	G52	5270	182
9	VGHC	-5235	-295	69	VSSD	-1035	-295	129	VCOMH	3625	-295	189	G54	5250	307
10	C22A	-5165	-295	70	VSSD	-965	-295	130	VCOMH	3695	-295	190	G56	5230	182
11	C22A	-5095	-295	71	VSSD	-895	-295	131	VCLC	3765	-295	191	G58	5210	307
12	C22B	-5025	-295	72	VSSD	-825	-295	132	VCL	3835	-295	192	G60	5190	182
13	C22B	-4955	-295	73	VSSD	-755	-295	133	VCL	3905	-295	193	G62	5170	307
14	C21A	-4885	-295	74	VSSD	-685	-295	134	VCI1OUT	3975	-295	194	G64	5150	182
15	C21A	-4815	-295	75	IOVCC	-390	-295	135	VCI1OUT	4045	-295	195	G66	5130	307
16	C21B	-4745	-295	76	IOVCC	-320	-295	136	VCI1OUT	4115	-295	196	G68	5110	182
17	C21B	-4675	-295	77	VCC	-250	-295	137	VCI1OUT	4185	-295	197	G70	5090	307
18	C12A	-4605	-295	78	VCC	-180	-295	138	VCI1OUT	4255	-295	198	G72	5070	182
19	C12A	-4535	-295	79	VCC	-110	-295	139	VCI1OUT	4325	-295	199	G74	5050	307
20	C12A	-4465	-295	80	VCC	-40	-295	140	REGP	4395	-295	200	G76	5030	182
21	C12A	-4395	-295	81	VCC	30	-295	141	VLCD	4465	-295	201	G78	5010	307
22	C12B	-4325	-295	82	VCC	100	-295	142	VLCD	4535	-295	202	G80	4990	182
23	C12B	-4255	-295	83	VCI	170	-295	143	VLCD	4605	-295	203	G82	4970	307
24	C12B	-4185	-295	84	VCI	240	-295	144	VLCD	4675	-295	204	G84	4950	182
25	C12B	-4115	-295	85	VCI	310	-295	145	VLCDC	4745	-295	205	G86	4930	307
26	VGLC	-4045	-295	86	VCI	380	-295	146	VLCDC	4815	-295	206	G88	4910	182
27	VGL	-3975	-295	87	VCI	450	-295	147	C11B	4885	-295	207	G90	4890	307
28	VGL	-3905	-295	88	VCI	520	-295	148	C11B	4955	-295	208	G92	4870	182
29	VGL	-3835	-295	89	VCI	590	-295	149	C11B	5025	-295	209	G94	4850	307
30	IOVCCDUM1	-3765	-295	90	VCILVL	660	-295	150	C11B	5095	-295	210	G96	4830	182
31	IM0	-3695	-295	91	OSC1	730	-295	151	C11A	5165	-295	211	G98	4810	307
32	IM1	-3625	-295	92	OSC2	800	-295	152	C11A	5235	-295	212	G100	4790	182
33	IM2	-3555	-295	93	Dummy28	870	-295	153	C11A	5305	-295	213	G102	4770	307
34	IM3	-3485	-295	94	TS0	940	-295	154	C11A	5375	-295	214	G104	4750	182
35	IOGNDDUM1	-3415	-295	95	TS1	1010	-295	155	DUMMY1	5445	-295	215	G106	4730	307
36	FLM	-3345	-295	96	TS2	1080	-295	156	DUMMYR3	5515	-295	216	G108	4710	182
37	NRESET	-3275	-295	97	TS3	1150	-295	157	DUMMYR4	5585	-295	217	G110	4690	307
38	TEST1	-3205	-295	98	TS4	1220	-295	158	VCOM	5655	-295	218	G112	4670	182
39	TEST2	-3135	-295	99	TS5	1290	-295	159	VCOM	5725	-295	219	G114	4650	307
40	DB17	-3065	-295	100	TS6	1360	-295	160	TESTO2	5795	-295	220	G116	4630	182
41	DB16	-2995	-295	101	TS7	1430	-295	161	DUMMY2	5810	307	221	G118	4610	307
42	DB15	-2925	-295	102	VSYNC	1500	-295	162	DUMMY3	5790	182	222	G120	4590	182
43	DB14	-2855	-295	103	HSYNC	1570	-295	163	G2	5770	307	223	G122	4570	307
44	DB13	-2785	-295	104	DOTCLK	1640	-295	164	G4	5750	182	224	G124	4550	182
45	DB12	-2715	-295	105	ENABLE	1710	-295	165	G6	5730	307	225	G126	4530	307
46	DB11	-2645	-295	106	SDO	1780	-295	166	G8	5710	182	226	G128	4510	182
47	DB10	-2575	-295	107	SDI	1850	-295	167	G10	5690	307	227	G130	4490	307
48	DB9	-2505	-295	108	SCL	1920	-295	168	G12	5670	182	228	G132	4470	182
49	IOGNDDUM2	-2435	-295	109	VGS	1990	-295	169	G14	5650	307	229	G134	4450	307
50	DB8	-2365	-295	110	VGS	2060	-295	170	G16	5630	182	230	G136	4430	182
51	DB7	-2295	-295	111	VSSD	2130	-295	171	G18	5610	307	231	G138	4410	307
52	DB6	-2225	-295	112	VSSD	2200	-295	172	G20	5590	182	232	G140	4390	182
53	DB5	-2155	-295	113	VSSD	2270	-295	173	G22	5570	307	233	G142	4370	307
54	DB4	-2085	-295	114	VDDD	2340	-295	174	G24	5550	182	234	G144	4350	182
55	DB3	-2015	-295	115	VDDD	2410	-295	175	G26	5530	307	235	G146	4330	307
56	DB2	-1945	-295	116	VDDD	2480	-295	176	G28	5510	182	236	G148	4310	182
57	DB1	-1875	-295	117	VDDD	2550	-295	177	G30	5490	307	237	G150	4290	307
58	DB0	-1805	-295	118	VMON	2620	-295	178	G32	5470	182	238	G152	4270	182
59	IOGNDDUM3	-1735	-295	119	VCOML	2690	-295	179	G34	5450	307	239	G154	4250	307
60	RW_NRD	-1665	-295	120	VCOML	2760	-295	180	G36	5430	182	240	G156	4230	182

No.	Pad name	X	Y
241	G158	4210	307
242	G160	4190	182
243	DUMMY4	4170	307
244	DUMMY5	4150	182
245	DUMMY6	4130	307
246	DUMMY7	4110	182
247	S384	4090	307
248	S383	4070	182
249	S382	4050	307
250	S381	4030	182
251	S380	4010	307
252	S379	3990	182
253	S378	3970	307
254	S377	3950	182
255	S376	3930	307
256	S375	3910	182
257	S374	3890	307
258	S373	3870	182
259	S372	3850	307
260	S371	3830	182
261	S370	3810	307
262	S369	3790	182
263	S368	3770	307
264	S367	3750	182
265	S366	3730	307
266	S365	3710	182
267	S364	3690	307
268	S363	3670	182
269	S362	3650	307
270	S361	3630	182
271	S360	3610	307
272	S359	3590	182
273	S358	3570	307
274	S357	3550	182
275	S356	3530	307
276	S355	3510	182
277	S354	3490	307
278	S353	3470	182
279	S352	3450	307
280	S351	3430	182
281	S350	3410	307
282	S349	3390	182
283	S348	3370	307
284	S347	3350	182
285	S346	3330	307
286	S345	3310	182
287	S344	3290	307
288	S343	3270	182
289	S342	3250	307
290	S341	3230	182
291	S340	3210	307
292	S339	3190	182
293	S338	3170	307
294	S337	3150	182
295	S336	3130	307
296	S335	3110	182
297	S334	3090	307
298	S333	3070	182
299	S332	3050	307
300	S331	3030	182
301	S330	3010	307
302	S329	2990	182
303	S328	2970	307
304	S327	2950	182
305	S326	2930	307

No.	Pad name	X	Y
306	S325	2910	182
307	S324	2890	307
308	S323	2870	182
309	S322	2850	307
310	S321	2830	182
311	S320	2810	307
312	S319	2790	182
313	S318	2770	307
314	S317	2750	182
315	S316	2730	307
316	S315	2710	182
317	S314	2690	307
318	S313	2670	182
319	S312	2650	307
320	S311	2630	182
321	S310	2610	307
322	S309	2590	182
323	S308	2570	307
324	S307	2550	182
325	S306	2530	307
326	S305	2510	182
327	S304	2490	307
328	S303	2470	182
329	S302	2450	307
330	S301	2430	182
331	S300	2410	307
332	S299	2390	182
333	S298	2370	307
334	S297	2350	182
335	S296	2330	307
336	S295	2310	182
337	S294	2290	307
338	S293	2270	182
339	S292	2250	307
340	S291	2230	182
341	S290	2210	307
342	S289	2190	182
343	S288	2170	307
344	S287	2150	182
345	S286	2130	307
346	S285	2110	182
347	S284	2090	307
348	S283	2070	182
349	S282	2050	307
350	S281	2030	182
351	S280	2010	307
352	S279	1990	182
353	S278	1970	307
354	S277	1950	182
355	S276	1930	307
356	S275	1910	182
357	S274	1890	307
358	S273	1870	182
359	S272	1850	307
360	S271	1830	182
361	S270	1810	307
362	S269	1790	182
363	S268	1770	307
364	S267	1750	182
365	S266	1730	307
366	S265	1710	182
367	S264	1690	307
368	S263	1670	182
369	S262	1650	307
370	S261	1630	182

No.	Pad name	X	Y
371	S260	1610	307
372	S259	1590	182
373	S258	1570	307
374	S257	1550	182
375	S256	1530	307
376	S255	1510	182
377	S254	1490	307
378	S253	1470	182
379	S252	1450	307
380	S251	1430	182
381	S250	1410	307
382	S249	1390	182
383	S248	1370	307
384	S247	1350	182
385	S246	1330	307
386	S245	1310	182
387	S244	1290	307
388	S243	1270	182
389	S242	1250	307
390	S241	1230	182
391	S240	1210	307
392	S239	1190	182
393	S238	1170	307
394	S237	1150	182
395	S236	1130	307
396	S235	1110	182
397	S234	1090	307
398	S233	1070	182
399	S232	1050	307
400	S231	1030	182
401	S230	1010	307
402	S229	990	182
403	S228	970	307
404	S227	950	182
405	S226	930	307
406	S225	910	182
407	S224	890	307
408	S223	870	182
409	S222	850	307
410	S221	830	182
411	S220	810	307
412	S219	790	182
413	S218	770	307
414	S217	750	182
415	S216	730	307
416	S215	710	182
417	S214	690	307
418	S213	670	182
419	S212	650	307
420	S211	630	182
421	S210	610	307
422	S209	590	182
423	S208	570	307
424	S207	550	182
425	S206	530	307
426	S205	510	182
427	S204	490	307
428	S203	470	182
429	S202	450	307
430	S201	430	182
431	S200	410	307
432	S199	390	182
433	S198	370	307
434	S197	350	182
435	S196	330	307

No.	Pad name	X	Y
436	S195	310	182
437	S194	290	307
438	S193	270	182
439	DUMMY8	250	307
440	DUMMY9	230	182
441	DUMMY10	210	307
442	DUMMY11	170	307
443	DUMMY12	130	307
444	DUMMY13	90	307
445	DUMMY14	50	307
446	DUMMY15	-50	307
447	DUMMY16	-90	307
448	DUMMY17	-130	307
449	DUMMY18	-170	307
450	DUMMY19	-210	307
451	DUMMY20	-230	182
452	DUMMY21	-250	307
453	S192	-270	182
454	S191	-290	307
455	S190	-310	182
456	S189	-330	307
457	S188	-350	182
458	S187	-370	307
459	S186	-390	182
460	S185	-410	307
461	S184	-430	182
462	S183	-450	307
463	S182	-470	182
464	S181	-490	307
465	S180	-510	182
466	S179	-530	307
467	S178	-550	182
468	S177	-570	307
469	S176	-590	182
470	S175	-610	307
471	S174	-630	182
472	S173	-650	307
473	S172	-670	182
474	S171	-690	307
475	S170	-710	182
476	S169	-730	307
477	S168	-750	182
478	S167	-770	307
479	S166	-790	182
480	S165	-810	307
481	S164	-830	182
482	S163	-850	307
483	S162	-870	182
484	S161	-890	307
485	S160	-910	182
486	S159	-930	307
487	S158	-950	182
488	S157	-970	307
489	S156	-990	182
490	S155	-1010	307
491	S154	-1030	182
492	S153	-1050	307
493	S152	-1070	182
494	S151	-1090	307
495	S150	-1110	182
496	S149	-1130	307
497	S148	-1150	182
498	S147	-1170	307
499	S146	-1190	182
500	S145	-1210	307

No.	Pad name	X	Y
501	S144	-1230	182
502	S143	-1250	307
503	S142	-1270	182
504	S141	-1290	307
505	S140	-1310	182
506	S139	-1330	307
507	S138	-1350	182
508	S137	-1370	307
509	S136	-1390	182
510	S135	-1410	307
511	S134	-1430	182
512	S133	-1450	307
513	S132	-1470	182
514	S131	-1490	307
515	S130	-1510	182
516	S129	-1530	307
517	S128	-1550	182
518	S127	-1570	307
519	S126	-1590	182
520	S125	-1610	307
521	S124	-1630	182
522	S123	-1650	307
523	S122	-1670	182
524	S121	-1690	307
525	S120	-1710	182
526	S119	-1730	307
527	S118	-1750	182
528	S117	-1770	307
529	S116	-1790	182
530	S115	-1810	307
531	S114	-1830	182
532	S113	-1850	307
533	S112	-1870	182
534	S111	-1890	307
535	S110	-1910	182
536	S109	-1930	307
537	S108	-1950	182
538	S107	-1970	307
539	S106	-1990	182
540	S105	-2010	307
541	S104	-2030	182
542	S103	-2050	307
543	S102	-2070	182
544	S101	-2090	307
545	S100	-2110	182
546	S99	-2130	307
547	S98	-2150	182
548	S97	-2170	307
549	S96	-2190	182
550	S95	-2210	307
551	S94	-2230	182
552	S93	-2250	307
553	S92	-2270	182
554	S91	-2290	307
555	S90	-2310	182
556	S89	-2330	307
557	S88	-2350	182
558	S87	-2370	307
559	S86	-2390	182
560	S85	-2410	307
561	S84	-2430	182
562	S83	-2450	307
563	S82	-2470	182
564	S81	-2490	307
565	S80	-2510	182
566	S79	-2530	307

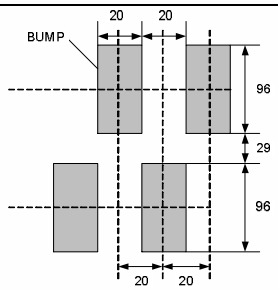
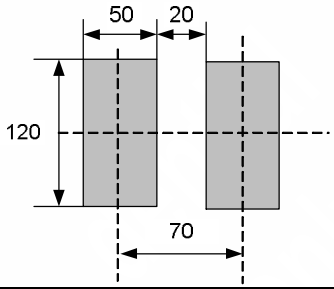
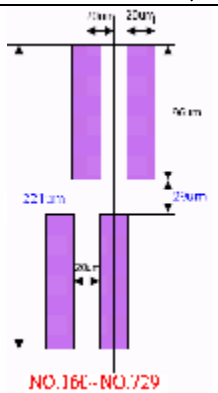
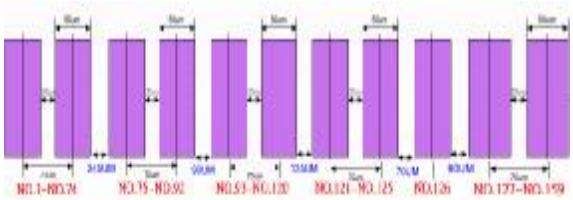
No.	Pad name	X	Y
567	S78	-2550	182
568	S77	-2570	307
569	S76	-2590	182
570	S75	-2610	307
571	S74	-2630	182
572	S73	-2650	307
573	S72	-2670	182
574	S71	-2690	307
575	S70	-2710	182
576	S69	-2730	307
577	S68	-2750	182
578	S67	-2770	307
579	S66	-2790	182
580	S65	-2810	307
581	S64	-2830	182
582	S63	-2850	307
583	S62	-2870	182
584	S61	-2890	307
585	S60	-2910	182
586	S59	-2930	307
587	S58	-2950	182
588	S57	-2970	307
589	S56	-2990	182
590	S55	-3010	307
591	S54	-3030	182
592	S53	-3050	307
593	S52	-3070	182
594	S51	-3090	307
595	S50	-3110	182
596	S49	-3130	307
597	S48	-3150	182
598	S47	-3170	307
599	S46	-3190	182
600	S45	-3210	307
601	S44	-3230	182
602	S43	-3250	307
603	S42	-3270	182
604	S41	-3290	307
605	S40	-3310	182
606	S39	-3330	307
607	S38	-3350	182
608	S37	-3370	307
609	S36	-3390	182
610	S35	-3410	307
611	S34	-3430	182
612	S33	-3450	307
613	S32	-3470	182
614	S31	-3490	307
615	S30	-3510	182
616	S29	-3530	307
617	S28	-3550	182
618	S27	-3570	307
619	S26	-3590	182
620	S25	-3610	307
621	S24	-3630	182
622	S23	-3650	307
623	S22	-3670	182
624	S21	-3690	307
625	S20	-3710	182
626	S19	-3730	307
627	S18	-3750	182
628	S17	-3770	307
629	S16	-3790	182
630	S15	-3810	307
631	S14	-3830	182
632	S13	-3850	307

No.	Pad name	X	Y
633	S12	-3870	182
634	S11	-3890	307
635	S10	-3910	182
636	S9	-3930	307
637	S8	-3950	182
638	S7	-3970	307
639	S6	-3990	182
640	S5	-4010	307
641	S4	-4030	182
642	S3	-4050	307
643	S2	-4070	182
644	S1	-4090	307
645	DUMMY22	-4110	182
646	DUMMY23	-4130	307
647	DUMMY24	-4150	182
648	DUMMY25	-4170	307
649	G159	-4190	182
650	G157	-4210	307
651	G155	-4230	182
652	G153	-4250	307
653	G151	-4270	182
654	G149	-4290	307
655	G147	-4310	182
656	G145	-4330	307
657	G143	-4350	182
658	G141	-4370	307
659	G139	-4390	182
660	G137	-4410	307
661	G135	-4430	182
662	G133	-4450	307
663	G131	-4470	182
664	G129	-4490	307
665	G127	-4510	182
666	G125	-4530	307
667	G123	-4550	182
668	G121	-4570	307
669	G119	-4590	182
670	G117	-4610	307
671	G115	-4630	182
672	G113	-4650	307
673	G111	-4670	182
674	G109	-4690	307
675	G107	-4710	182
676	G105	-4730	307
677	G103	-4750	182
678	G101	-4770	307
679	G99	-4790	182
680	G97	-4810	307
681	G95	-4830	182
682	G93	-4850	307
683	G91	-4870	182
684	G89	-4890	307
685	G87	-4910	182
686	G85	-4930	307
687	G83	-4950	182
688	G81	-4970	307
689	G79	-4990	182
690	G77	-5010	307
691	G75	-5030	182
692	G73	-5050	307
693	G71	-5070	182
694	G69	-5090	307
695	G67	-5110	182
696	G65	-5130	307
697	G63	-5150	182
698	G61	-5170	307

No.	Pad name	X	Y
699	G59	-5190	182
700	G57	-5210	307
701	G55	-5230	182
702	G53	-5250	307
703	G51	-5270	182
704	G49	-5290	307
705	G47	-5310	182
706	G45	-5330	307
707	G43	-5350	182
708	G41	-5370	307
709	G39	-5390	182
710	G37	-5410	307
711	G35	-5430	182
712	G33	-5450	307
713	G31	-5470	182
714	G29	-5490	307
715	G27	-5510	182
716	G25	-5530	307
717	G23	-5550	182
718	G21	-5570	307
719	G19	-5590	182
720	G17	-5610	307
721	G15	-5630	182
722	G13	-5650	307
723	G11	-5670	182
724	G9	-5690	307
725	G7	-5710	182
726	G5	-5730	307
727	G3	-5750	182
728	G1	-5770	307
729	DUMMY26	-5790	182
730	DUMMY27	-5810	307

Alignment mark	X	Y
A1	-6015	275
A2	6015	275

BUMP Arrangement

Source Gate	
I/O pins	
Arrangement	 

4. Interface

4.1 System Interface

The HX8345-A supports three system interfaces: an 80-system 18-/16-/9-/8-bit bus interface, a 68-system 18-/16-/9-/8-bit bus interface and a serial data transfer bus interface. The interface mode is selected by the IM3-0 pins setting.
The HX8345-A includes an index register (IR), which is stored the index data of internal control register and RAM. There are two 18-bit bus control registers, which are used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the second read data operations is valid.

80- / 68-system Bus

Operations	RS	80-system		68-system	
		NWR	NRD	E	RW
Writes Indexes into IR	0	0	1	1	0
Reads internal status	0	1	0	1	1
Writes data into control register or GRAM	1	0	1	1	0
Reads control register or GRAM data	1	1	0	1	1

Table 4. 1 Register Selection (18-/16-/9-/8- Bit System Interface)

Start Bytes

Operations	RW	RS
Writes Indexes into IR	0	0
Reads internal status	1	0
Writes data into control register or GRAM	0	1
Reads data from control register or GRAM	1	1

Table 4. 2 Register Selection (Serial Data Transfer Interface)

4.1.1 80-/ 68-System Interface

18-bit bus Interface

The 80-system 18-bit parallel data transfer can be used by setting IM3-0 pins to "1010". And the 68-system 18-bit parallel data transfer can be used by setting IM3-0 pins to "1000". The Figure 4.1 is the example of interface with i80/m68 microcomputer and the Figure 4.2 is the data format of 18-bit system interface.

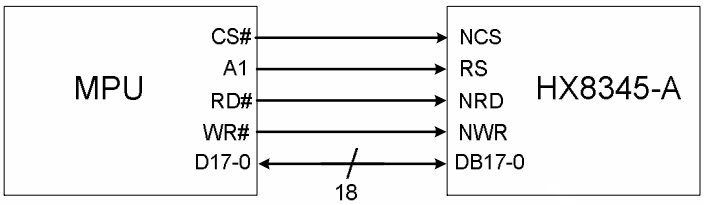


Figure 4. 1 Example of 80- / 68- System 18-bit bus Interface

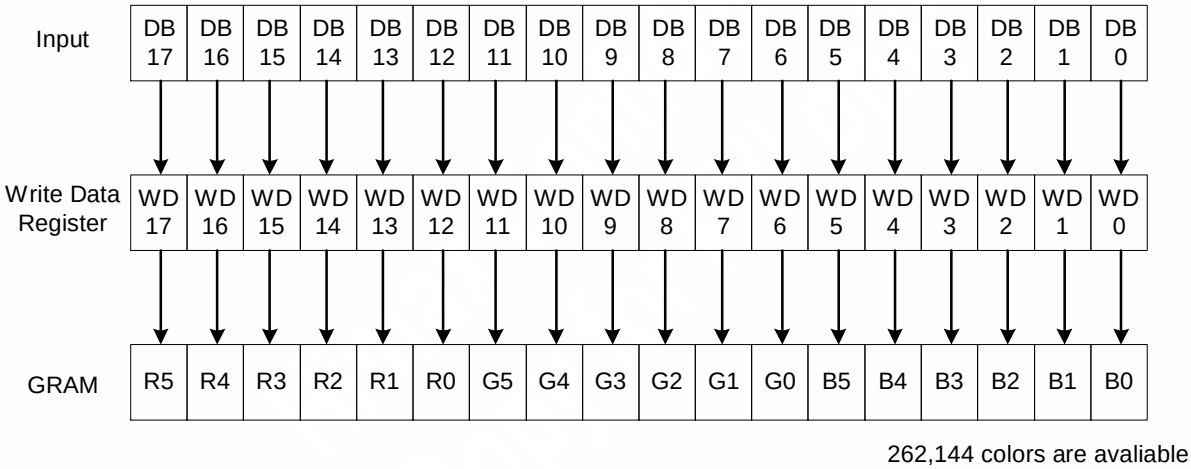


Figure 4. 2 Data Format of 18-bit bus System Interface

16-bit bus Interface

The 80-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to "0010". And the 68-system 16-bit bus parallel data transfer can be used by setting IM3-0 pins to "0000". The data written to GRAM is expanded to 18-bit bus data automatically in the LSI. Unused pins (DB9, DB0) must be fixed to the VCC or VSSD level. The Figure 4.3 is the example of interface with 16-bit i80/m68 microcomputer bus and the Figure 4.4 is the data format of 16-bit bus system interface.

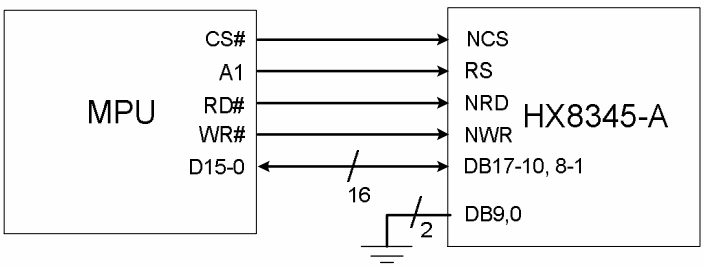
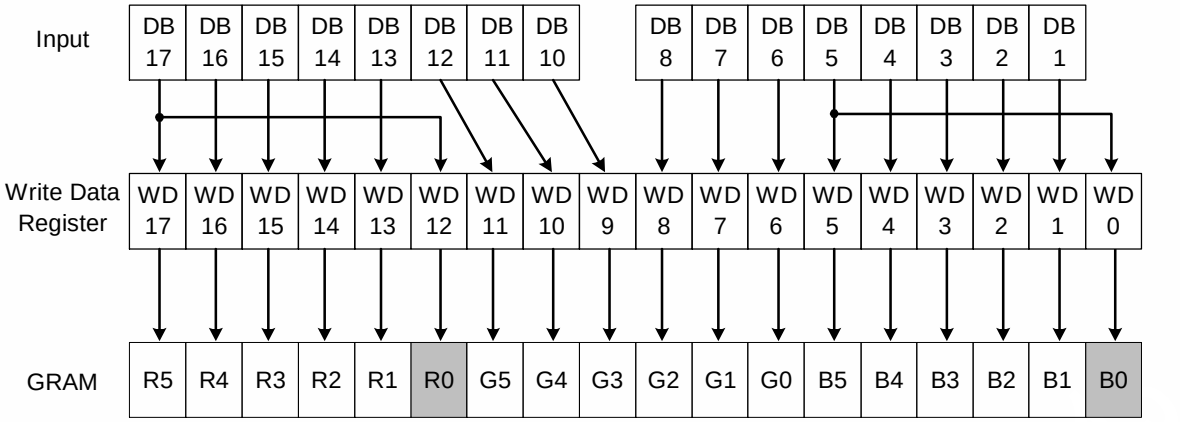


Figure 4. 3 Example of 80- / 68- System 16-bit bus Interface



65,536 colors are avaliable

Figure 4. 4 Data Format of 16-bit bus System Interface

9-bit bus Interface

The 80-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to “1011”. And the 68-system 9-bit bus parallel data transfer can be used by setting IM3-0 pins to “1001”. In 80-/68- system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and the 18-bit GRAM write data are divided into lower and upper bits, and then the upper bits are transferred first. Unused pins (DB8-0) must be fixed to the VCC or VSSD level. Ensure that upper bytes have to be written when writing the index register.

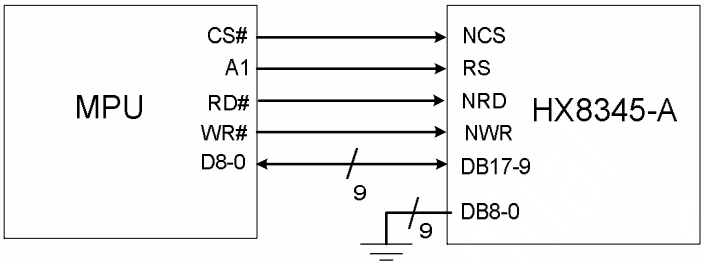


Figure 4. 5 Example of 80- / 68- System 9-bit bus Interface

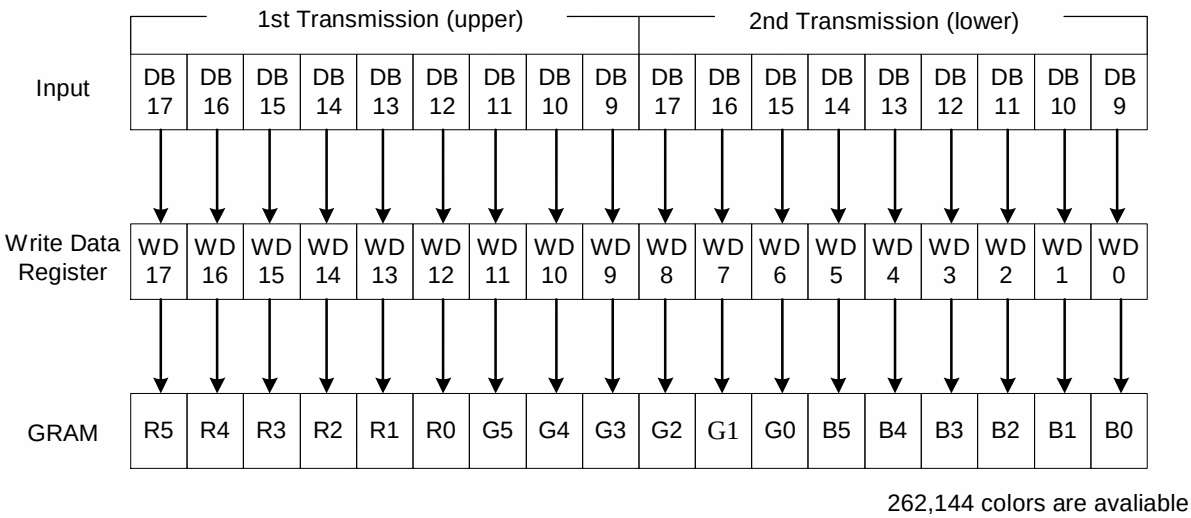


Figure 4. 6 Data Format of 9-bit bus System Interface

8-bit bus Interface

The 80-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0011”. And the 68-system 8-bit bus parallel data transfer can be used by setting IM3-0 pins to “0001”. In 80-/68- system 8-bit bus parallel data transfer mode, the 16-bit bus instruction and the 18-bit GRAM write data are divided into lower and upper bits, and then the upper bits are transferred first.

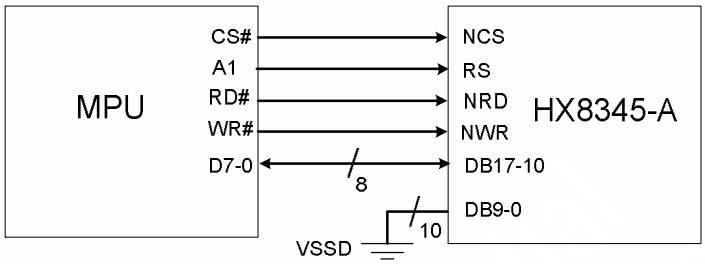


Figure 4. 7 Example of 80- / 68- System 8-bit bus Interface

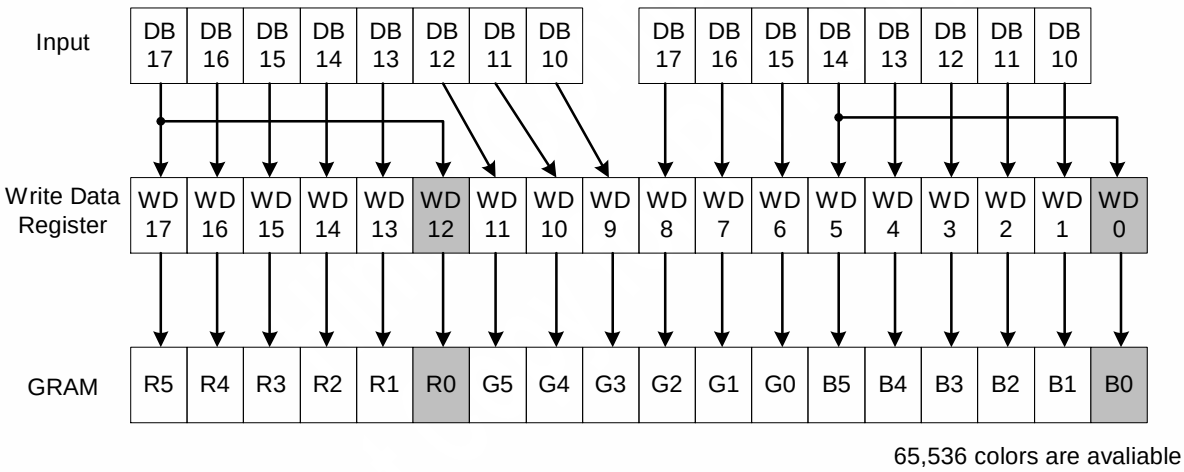
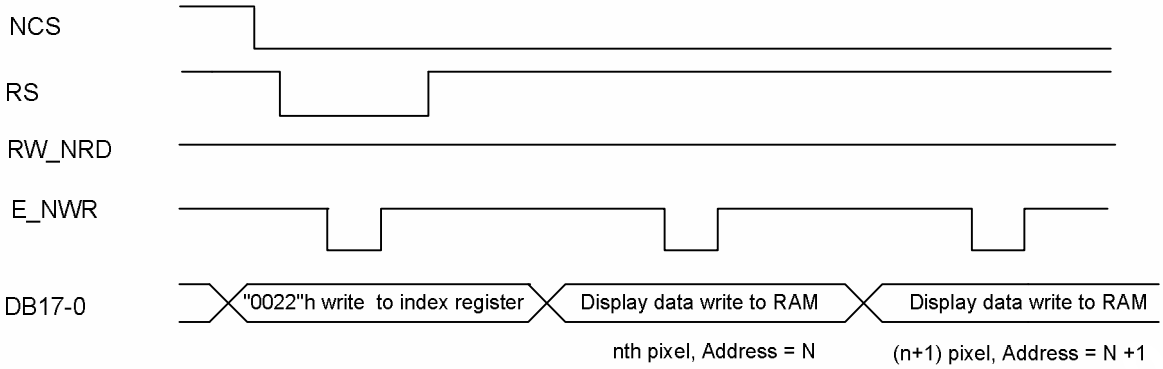
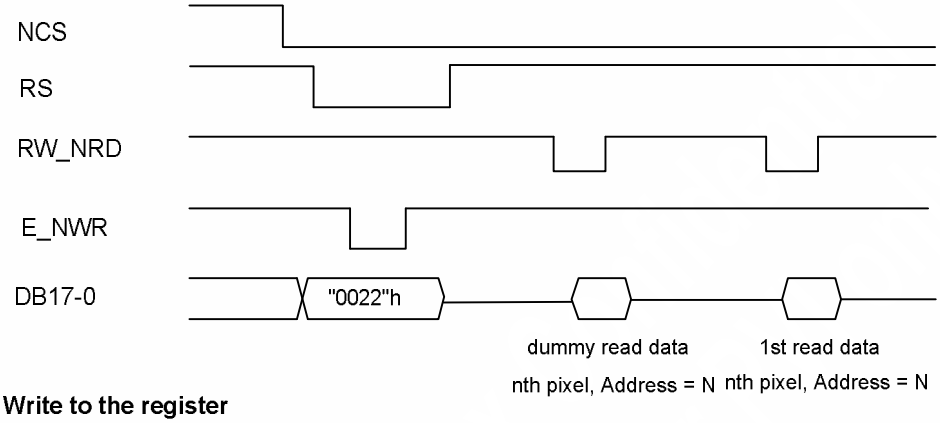


Figure 4. 8 Data Format of 8-bit bus System Interface

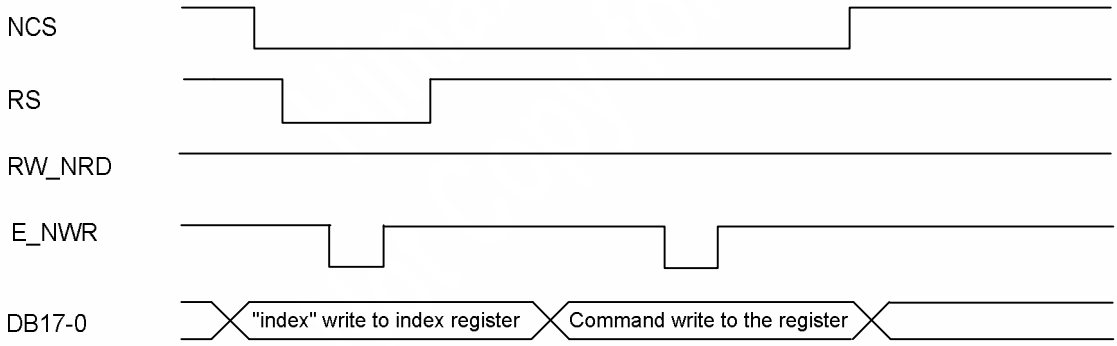
Write to the graphic RAM



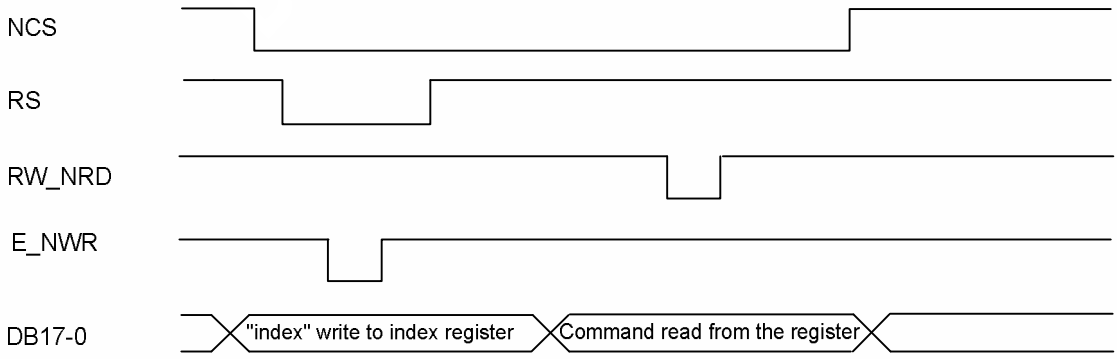
Read the graphic RAM



Write to the register



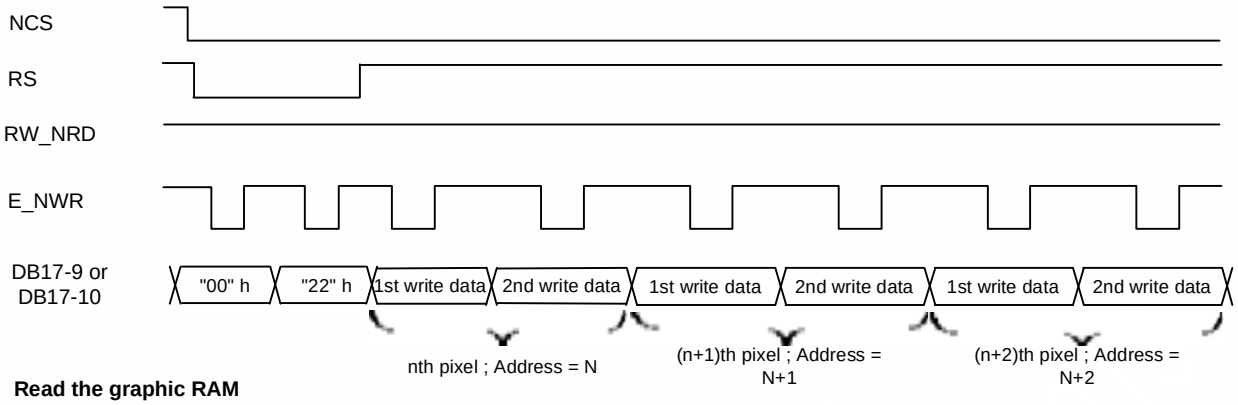
Read the register



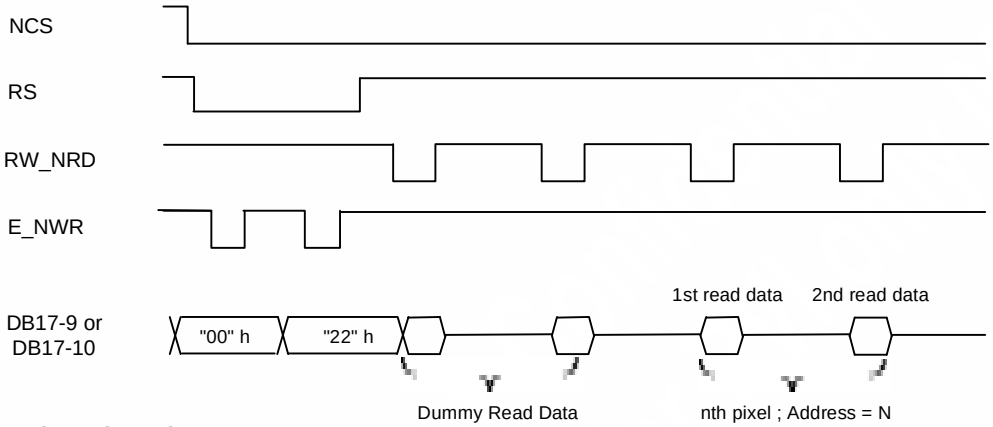
I80 - 18/16 bit interface : D17~D10 = 00h, D8~D1 = Index value

Figure 4. 9 18 / 16-bit Parallel Bus Interface Timing (for i80 series MPU)

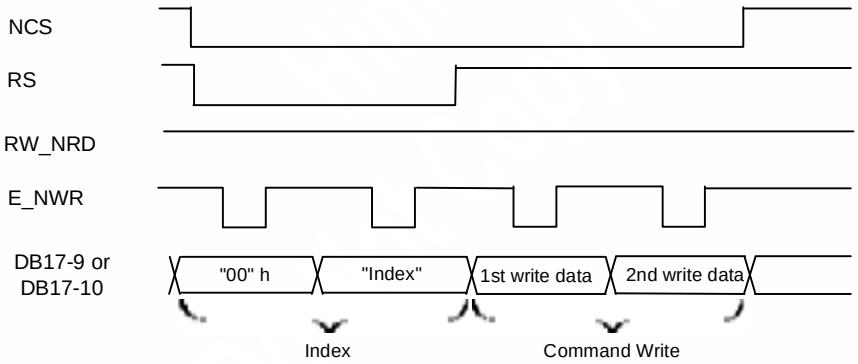
Write to the graphic RAM



Read the graphic RAM



Write to the register



Read the register

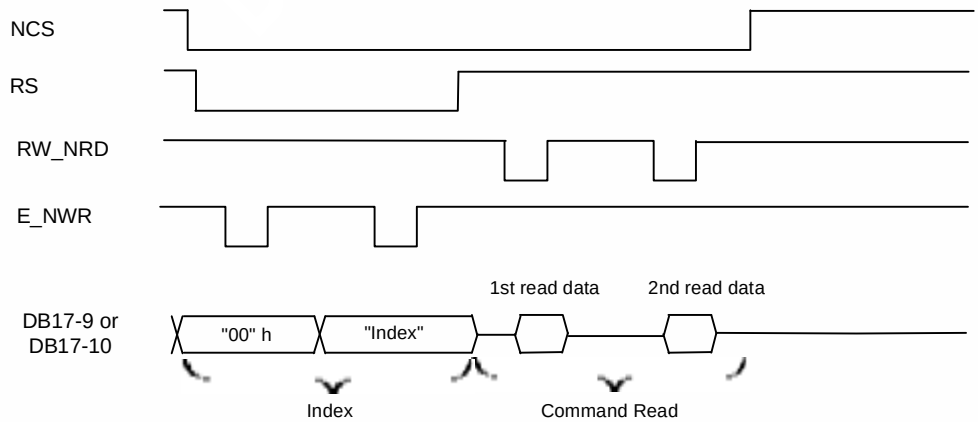
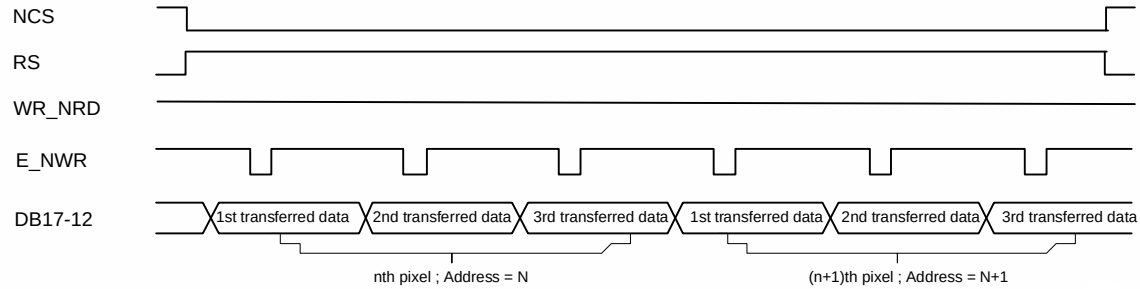


Figure 4. 10 9 / 8-bit Parallel Bus Interface Timing (for i80 series MPU)

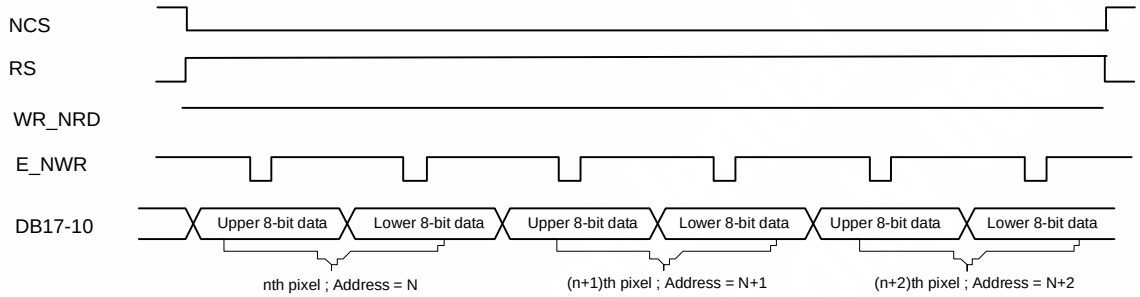
Write to the display data RAM

18/16-bit display data (6-bit x 3 transfers transfers)



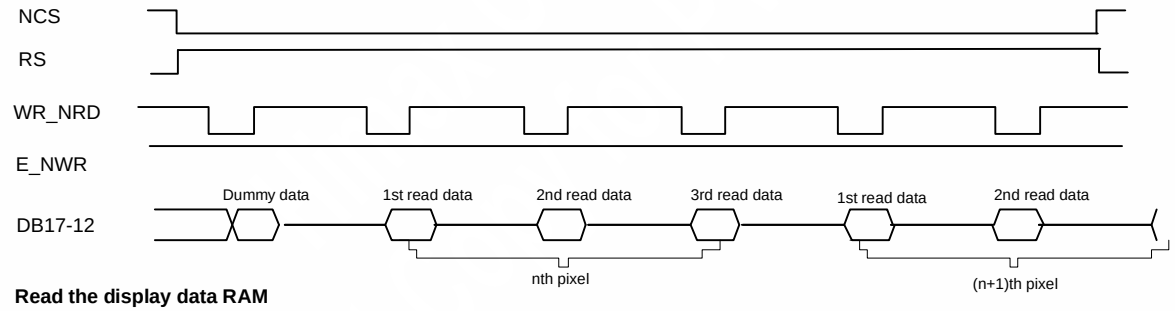
Write to the display data RAM

16-bit display data (8-bit x 2 transfers, TRI=0)



Read the display data RAM

18/16-bit display data (6-bit x 3 transfers, TRI=1)



Read the display data RAM

16-bit display data (8-bit x 2 transfers, TRI=0)

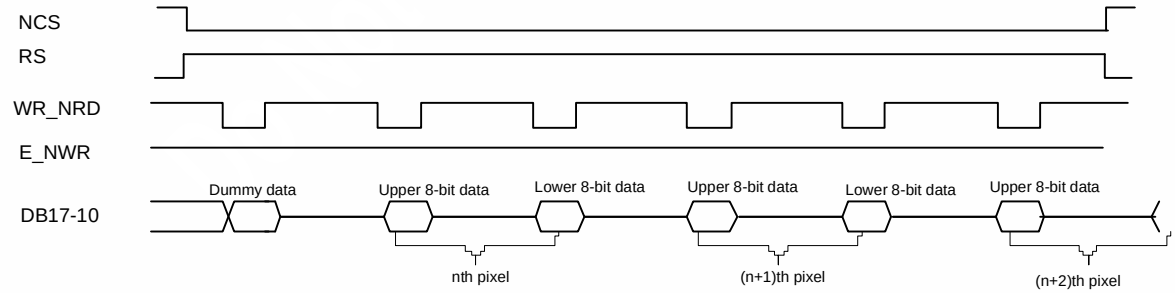


Figure 4. 11 8/6-bit Parallel Bus Interface Timing (for i80 series MPU)

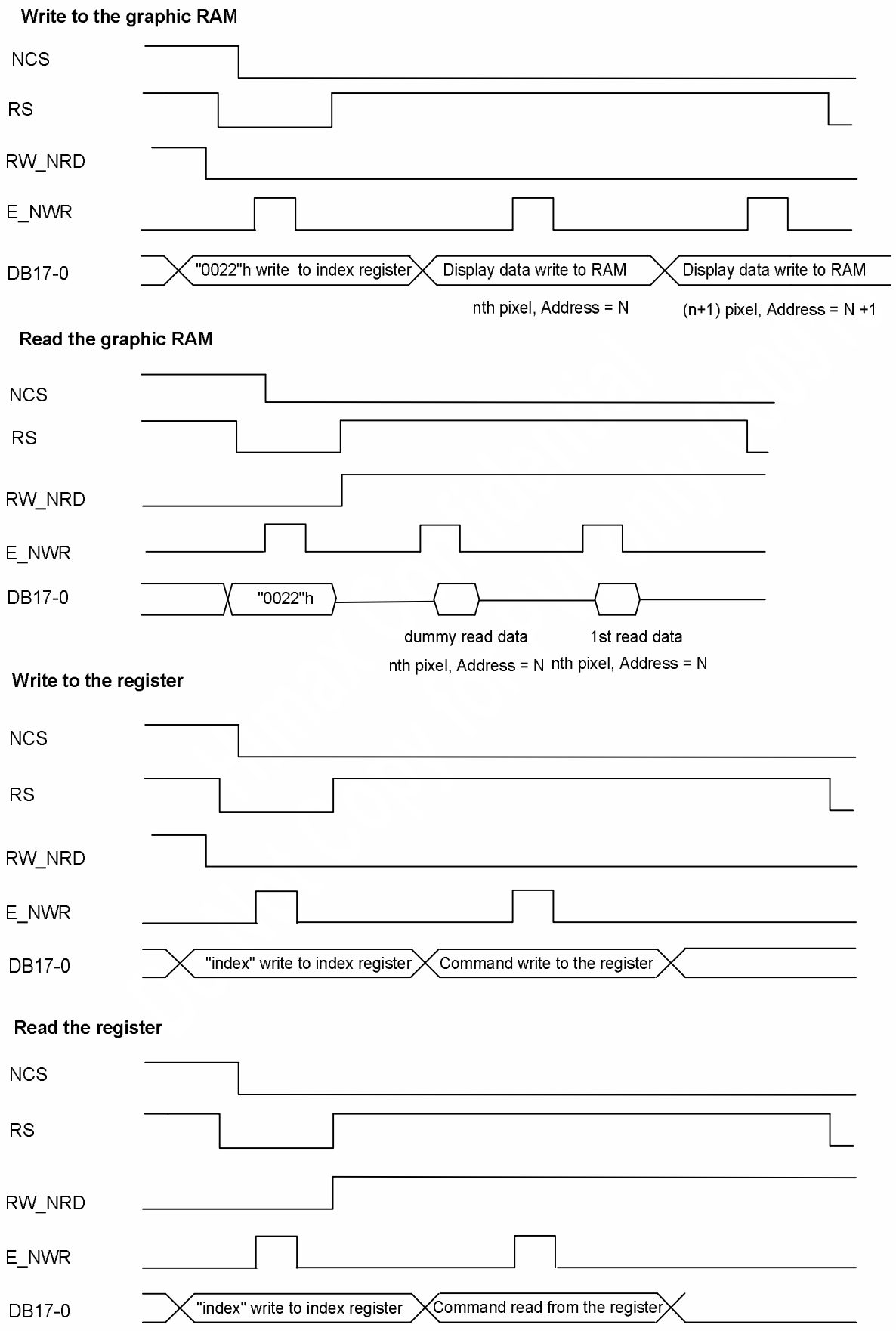


Figure 4. 12 18 / 16-bit Parallel Bus Interface Timing (for M68 series MPU)

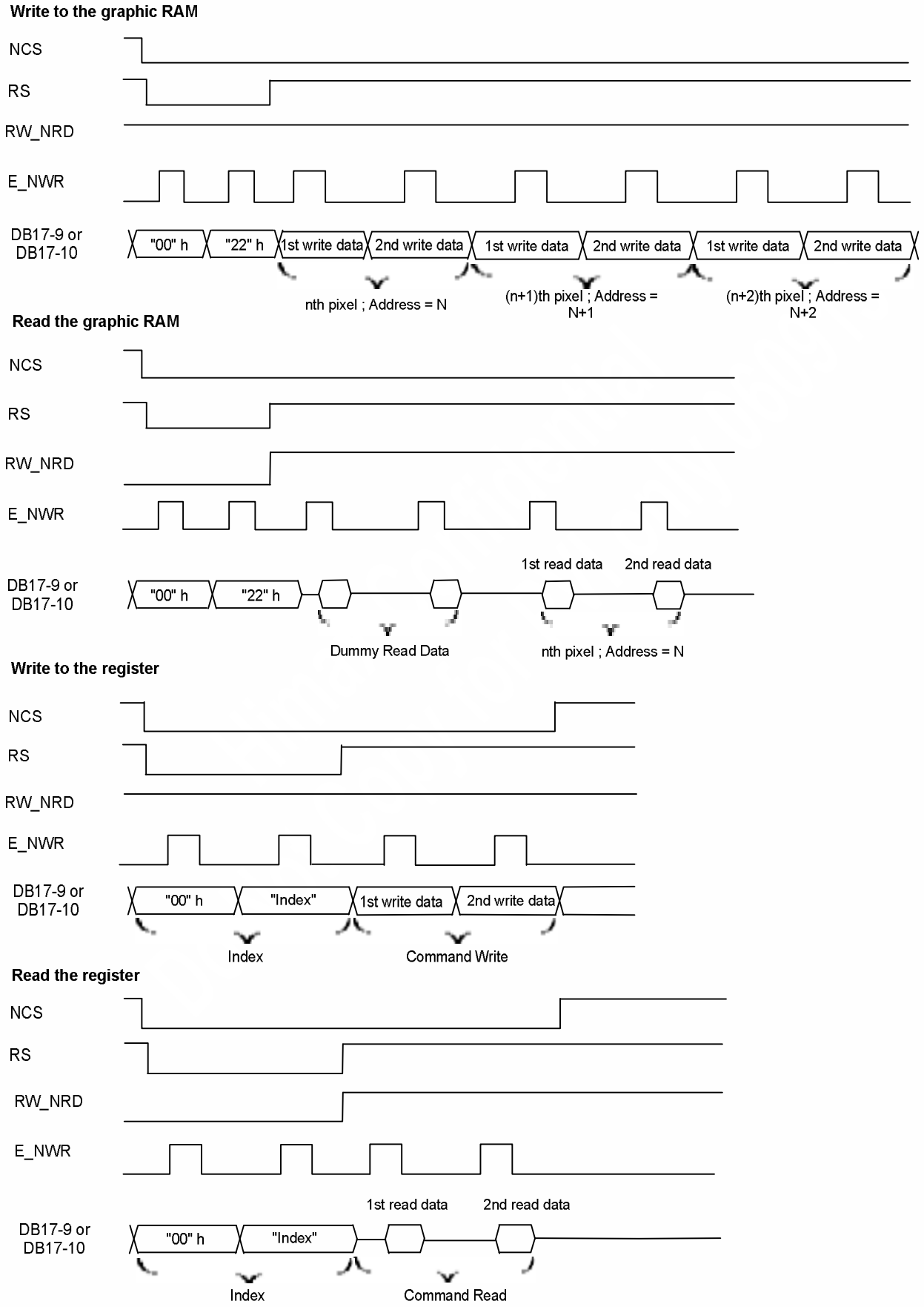
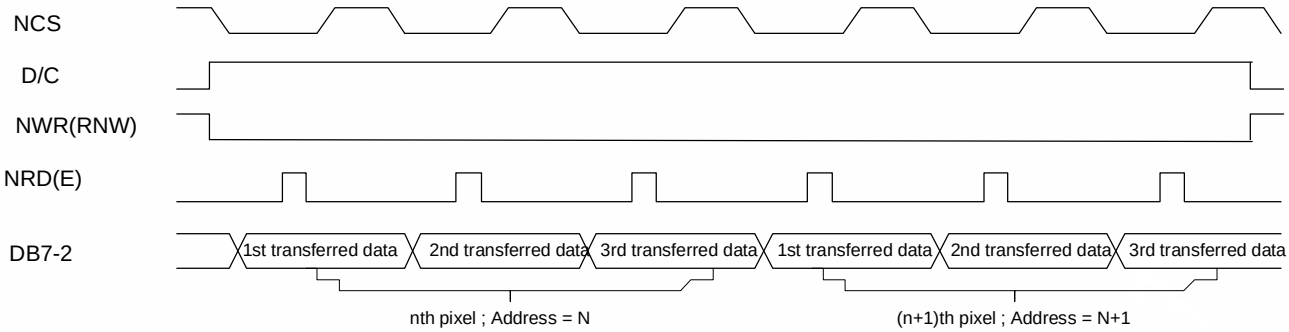


Figure 4. 13 9 / 8-bit Parallel Bus Interface Timing (for M68 series MPU)

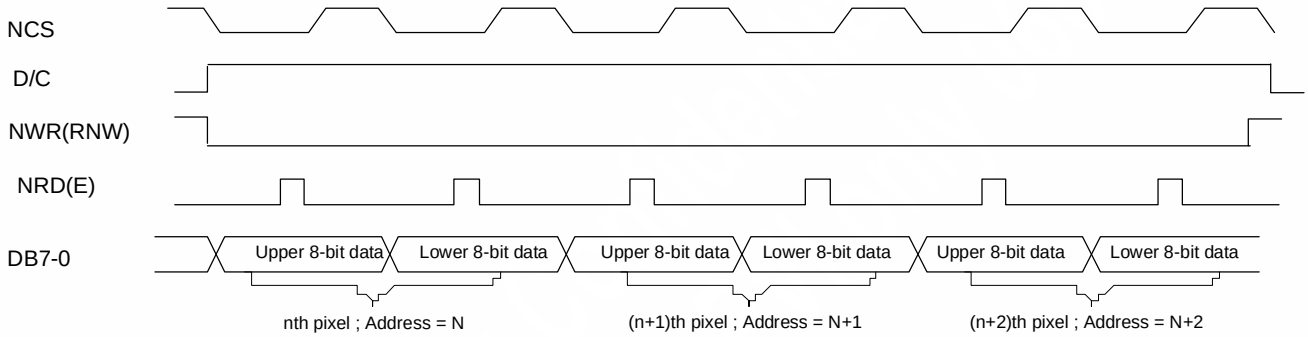
Write to the display data RAM

18/16-bit display data (6-bit x 3 transfers transfers)



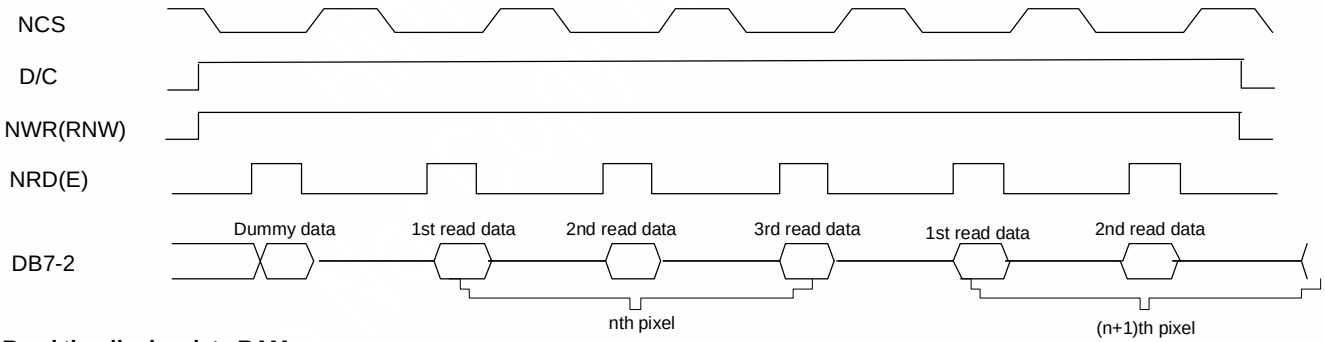
Write to the display data RAM

16/12-bit display data (8-bit x 2 transfers)



Read the display data RAM

18/16-bit display data (6-bit x 3 transfers)



Read the display data RAM

16-bit display data (8-bit x 2 transfers)

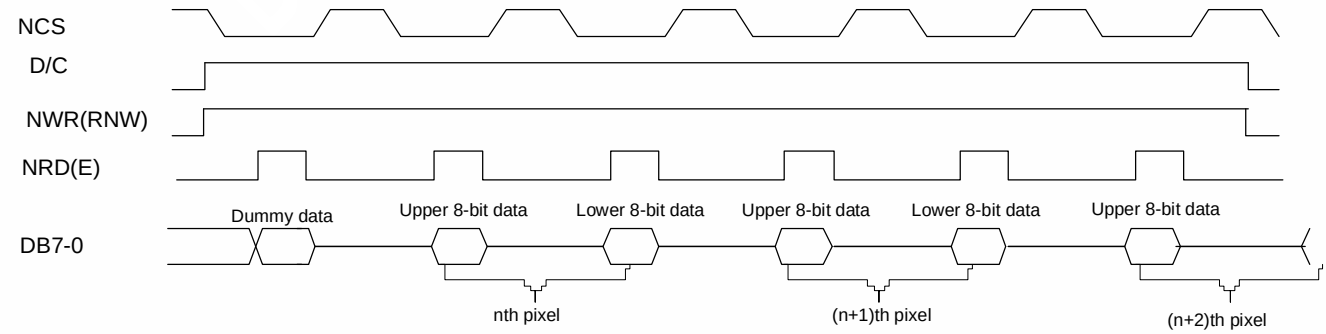


Figure 4. 14 8/6-bit Parallel Bus Interface Timing (for m68 series MPU)

4.1.2 Serial Data Transfer Interface

The HX8345-A supports the serial data transfer interface by setting IM3-1 pins to “010”. The serial data transfer interface mode is enabled through the chip select line (NCS), and accessed via a three-wire control consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock line (SCL). When HX8345-A is set up for serial data transfer interface mode, the IM0(ID) pin is used as an ID pin and then the DB17-0 pins, which are not used, must be fixed at VCC or VSSD.

In serial data transfer interface mode, the HX8345-A can transfer initially with the start byte at the falling edge of NCS input and finish the transfer at the rising edge of a NCS input.

When the chip select line (NCS) of HX8345-A set active low, the start byte will be transferred first. The start byte is making up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of the 6-bit bus device identification code must be set 01110 and the least significant bit of the identification code can be determined by the IM0/ID pin. The register select bit (RS) is the seventh bit of the start byte. The cases of write data to the index register or read the status must be setting RS = 0, and the cases of write or read an instruction or GRAM data must be setting RS = 1. The read or write function is selected according to the eighth bit of the start byte (RW bit). The data is received when RW = 0, and is transmitted when RW = 1. Table4.3 list different conditions when change the RS and RW bit.

When the serial data transfer interface is enabled, the HX8345-A starts taking in start byte and subsequent data that is transferred with the MSB first. Further, the registers of 16-bit bus format can be dividing to the upper eight bits as the first byte and lower eight bits as the second byte. The HX8345-A executed the write data operation to the GRAM after two-byte and then automatically expanded to the 18-bit bus format (Figure 4.9). When the read status/register operations are executed, the prior byte after start byte is invalid, and then the HX8345-A starts to read correct status/register data from second byte. As well as, when the read GRAM data operation, the prior five bytes of GRAM read data after the start byte are invalid. The HX8345-A starts to read correct GRAM data from the sixth byte.

RS	RW	Function
0	0	Index register set
0	1	Status read
1	0	Register or GRAM data write
1	1	Register or GRAM data read

Table 4. 3 The Function of RS and RW Bit

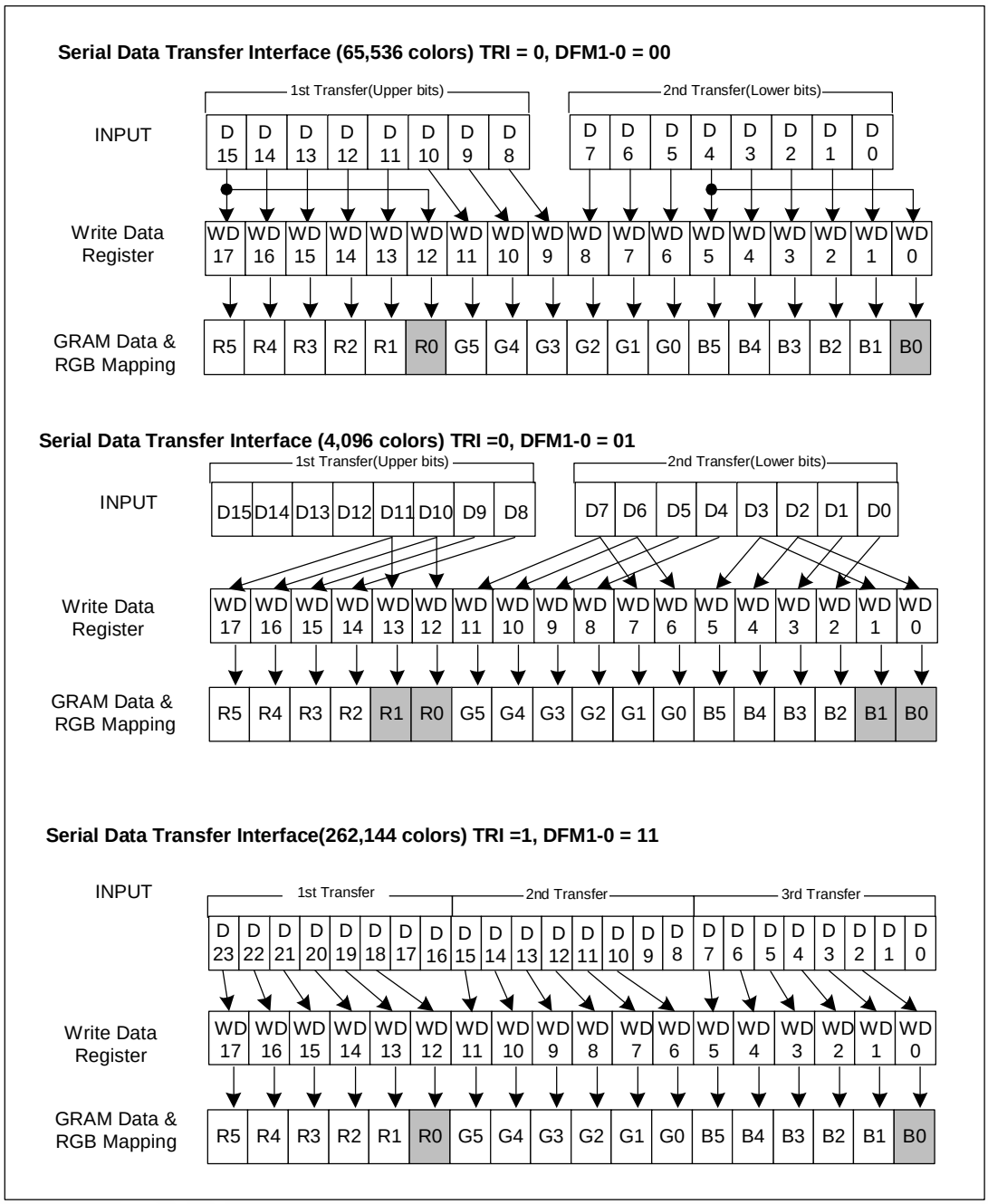


Figure 4. 15 Data Format of Serial Data Transfer Interface GRAM

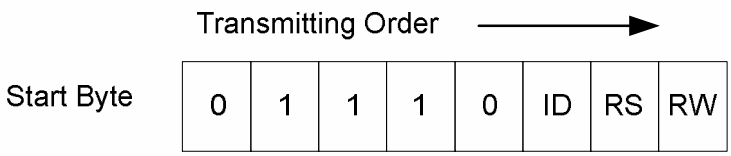


Figure 4. 16 Start Byte Format of Serial Interface

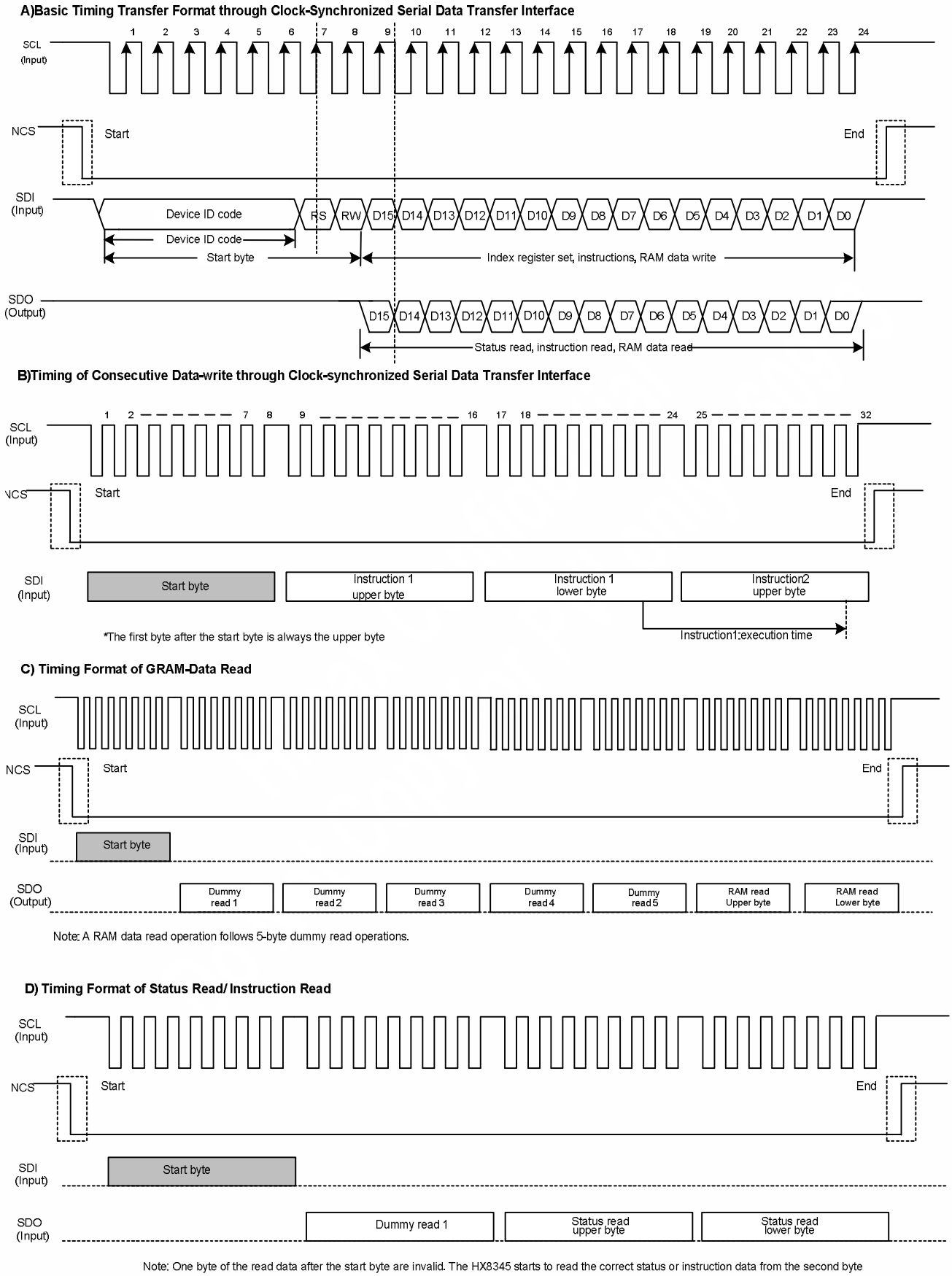


Figure 4. 17 Data transfer through Serial Data Transfer Interface

4.2 VSYNC Interface

The HX8345-A supports the VSYNC interface mode that executed the display operation by the internal clocks generated from internal oscillators and synchronized with the frame synchronization signal VSYNC. When the VSYNC interface mode is selected, the interface display a moving picture through system interface with minimum modification those re-write display data to the internal GRAM in a high speed RAM function. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

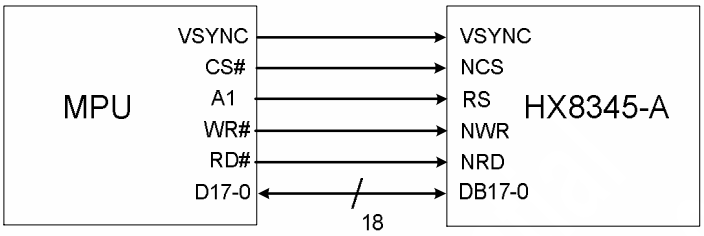


Figure 4. 18 VSYNC Interface to MPU

The VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It requires GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP, BP and display lines duration(NL):

$$Internal\ ocillator\ clock\ (f_{osc})[Hz] = Frame\ Frequency \times [Display\ Lines(NL) + FP + BP] \times Clock\ Cycle\ Per\ Line(RTN) \times\ frequency\ \ fluctuation$$

The parameter of frequency fluctuation is ascribing to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

The minimum speed for RAM can be computed by the following formula:

$$Min\ RAM\ Write\ Speed\ [Hz]" \frac{128 \times DisplayLines(NL) \times f_{osc}}{[BackPorch(BP) + DisplyLines(NL) - MARGIN\ lines] \times ClockCyclePerLine(RTN)}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the HX8345-A start the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting an internal oscillator clock (fosc) first.
An example of internal oscillator clock (fosc) and minimum speed for RAM writing set up in VSYNC interface mode is as follows.

Example
Display size: 128RGB*160 lines
Lines of be used: 160 lines (NL[4:0]=10011)
FP: 2 lines (FP[3:0]=0010)
BP:14 lines (BP[3:0]=1110)

Frequency fluctuation: 5#
Frame frequency: 60Hz

Internal oscillator clock (fosc) [Hz] = 60 × [160 + 2 +14] × 16 × (1.05/0.95) 187 kHz

The Min. RAM Write Speed [Hz] ! 128 × 160 × 187k / {[14 + 160-2] × 16} 1.39MHz

In this example, the minimum RAM write speed of VSYNC interface is 1.39MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the HX8345-A initiate the display operation and make it possible to re-write the display area set previously. Further, if the display area is different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.

When the HX8345-A make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 4.19 illustrates the process of VSNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.

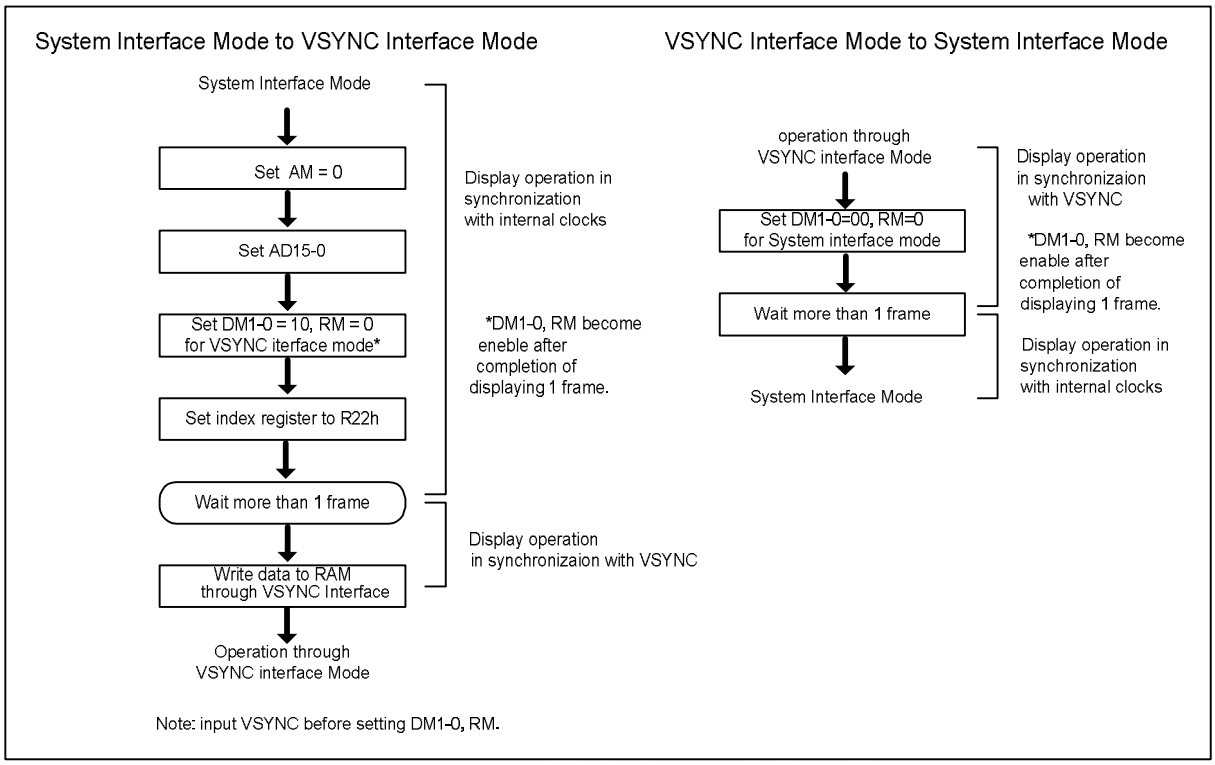


Figure 4. 19 VSYNC interface with internal clock and system interface with internal clock mode transition

The partial display function, vertical scroll function and interlaced scan function are invalidity function in VSYNC interface mode.

4.3 RGB Interface

The HX8345-A supports the RGB interface that display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE) be described on Table 4.5. The RGB interface can be used by setting DM1-0=01 and RM=1. In RGB interface mode, with use a window address function , enables to display data in a moving picture area and makes it possible to transfer the display only by re-writing a screen with minimum data transfers.

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit bus RGB interface	PD17-0
0	1	16-bit bus RGB interface	PD17-13, 11-1
1	0	6-bit bus RGB interface	PD17-12
1	1	Ignore	-

Table 4. 4 RIM Bit Set

EPL	ENABLE	RAM Write	RAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

Table 4. 5 EPL and ENABLE Set

When the HX8345-A set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continues until the next input of the VSYNC signal.

The HX8345-A supports two types of RGB interface mode, the difference between them is the RAM access using the RGB interface (PD17-0) or system interface (DB17-0). The data is written to the internal GRAM synchronized with DOTCLK inputs when ENABLE is setting low. Contrary to set ENABLE high, the data write to the GRAM would be used the system interface. Further, when selected to use system interface, set ENABLE high to stop using the RGB interface for writing data, and then set the RAM access setting bit bus (RM) low to invert RAM access operation by using system interface. After that, set address AD15-0 on falling edges of VSYNC and then set the index field of register (R22h) to access RAM via the system interface. The HX8345-A allows rewriting data in the still picture area by using the system interface when displaying a moving picture in RGB interface mode. When return to use RGB interface to access RAM, set address AD 15-0, RAM access setting bit bus (RM=1) and the index field of register (R22h) before accessing RAM via RGB interface.

The Figure 4.20 are shown the procedure of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

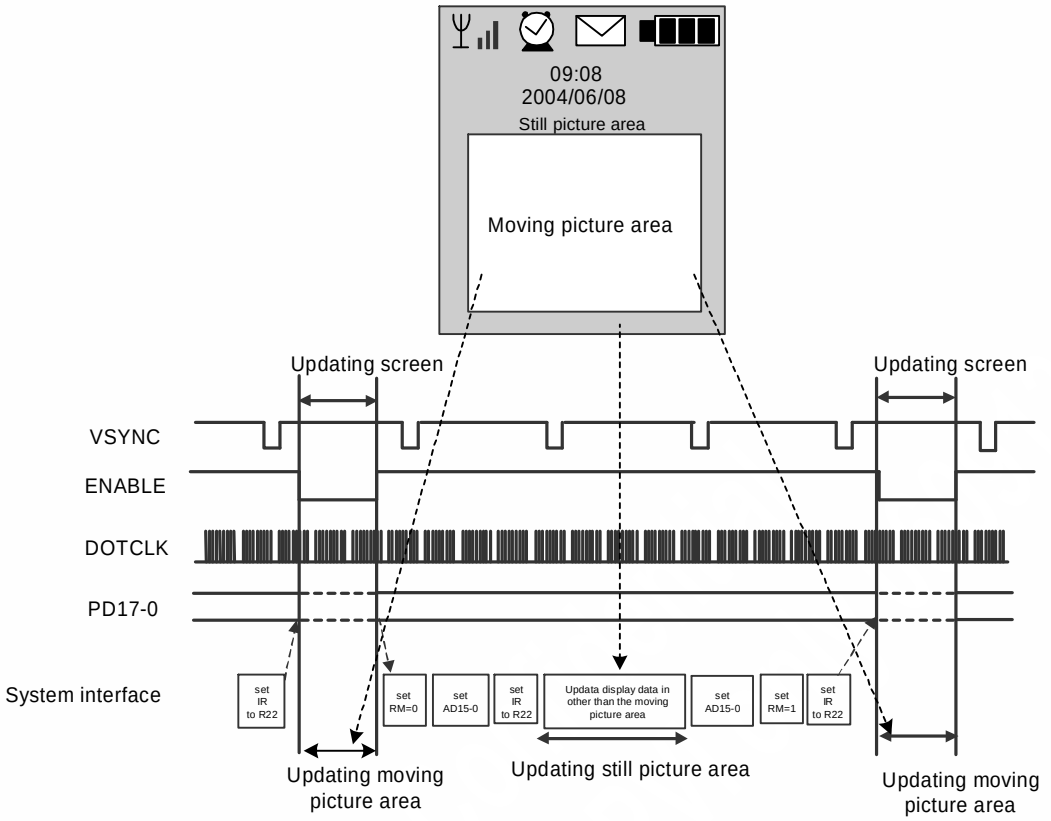


Figure 4. 20 Example of update the still and moving picture

When set up in RGB interface mode, the used of high–speed RAM write mode to write data to the internal GRAM and GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal. It is the same with VSYNC interface mode; partial screen display function, vertical scroll function and interlaced scan function are invalidity function in RGB interface mode.

When the HX8345-A make the transition with system interface mode and RGB interface mode, the sequence of switching process must be follow as Figure 4.21.

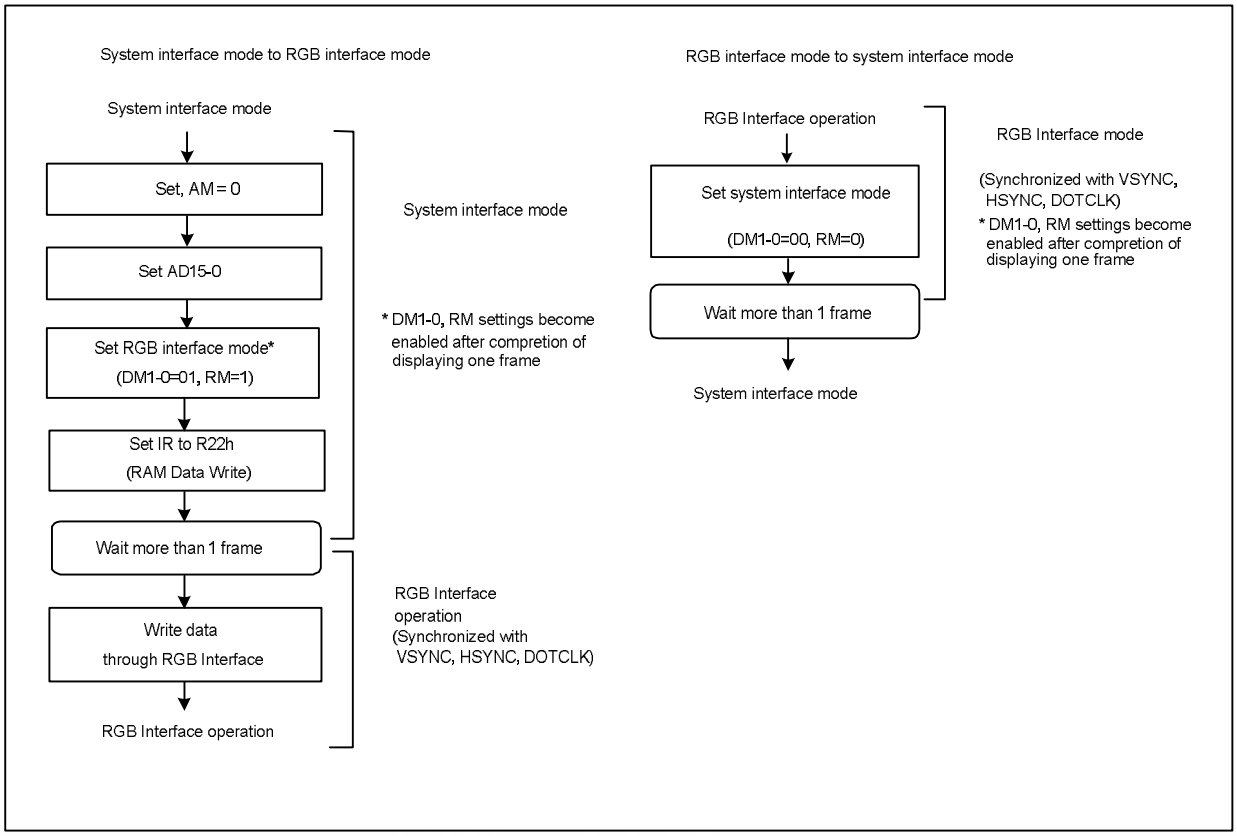


Figure 4. 21 Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure 4.22.

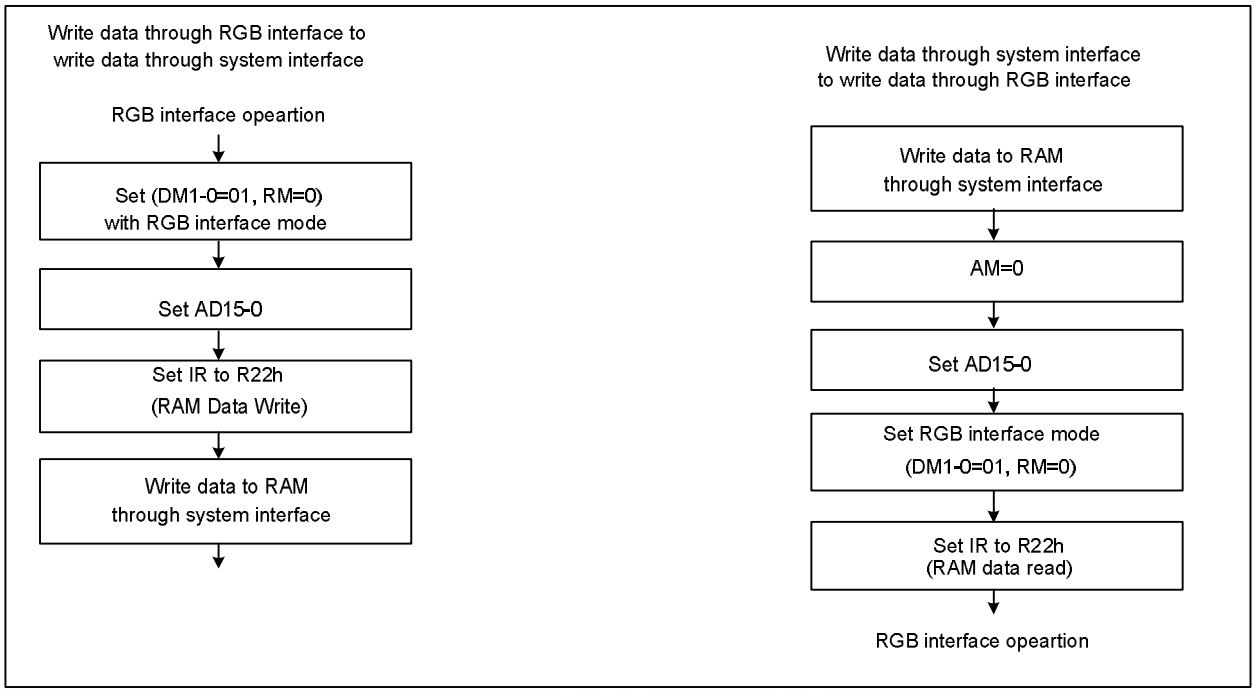


Figure 4. 22 RAM data write sequence through System Interface or RGB Interface during RGB Interface Mode

The HX8345-A supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

18-bit bus RGB interface

The 18-bit interface can be used by setting RIM1-0 bits to “00”. The Figure 4.23 is the example of 18-bit RGB interface with LCD Controller and HX8345-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD17-0 bits and according to the signal of data enable (ENABLE). The Figure2.17 is the data format of 18-bit RGB interface.

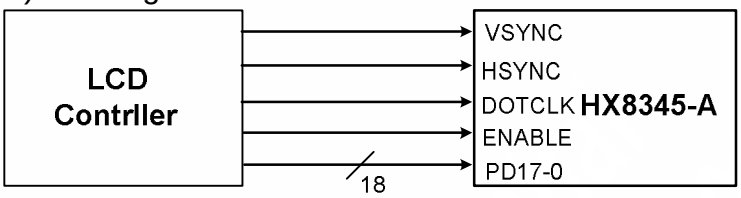


Figure 4. 23 18-bit RGB interface

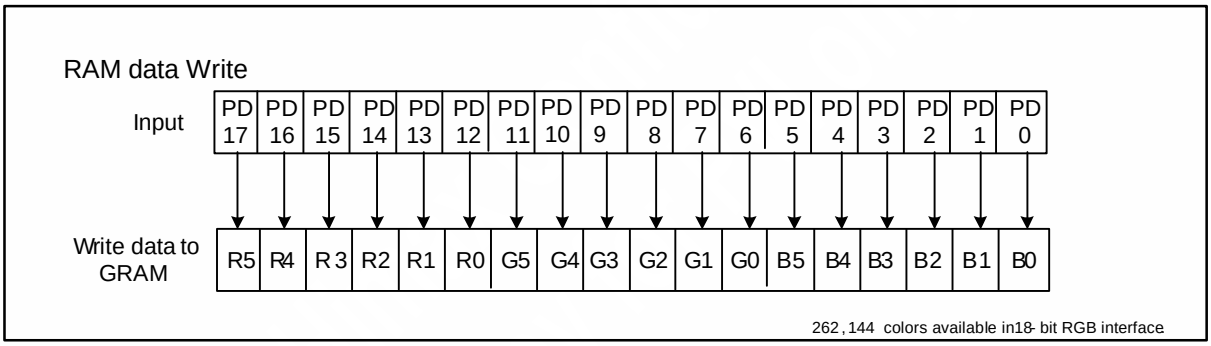


Figure 4. 24 Data format for 18-bit interface

16-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “01”. The Fig 2.18 is the example of 16-bit bus RGB interface with LCD Controller and HX8345-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-13, PD11-1 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins(PD9, PD0) must be fixed to the VCC or VSSD level. The Figure 4.25 is the data format of 16-bit RGB interface.

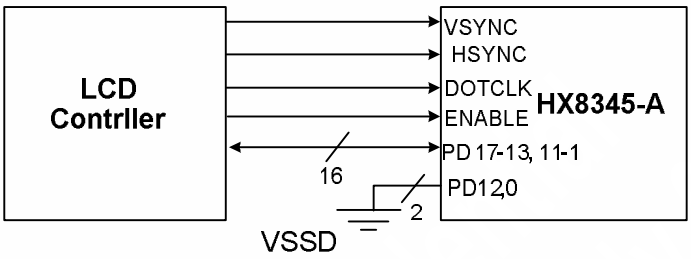


Figure 4. 25 16-bit RGB interface

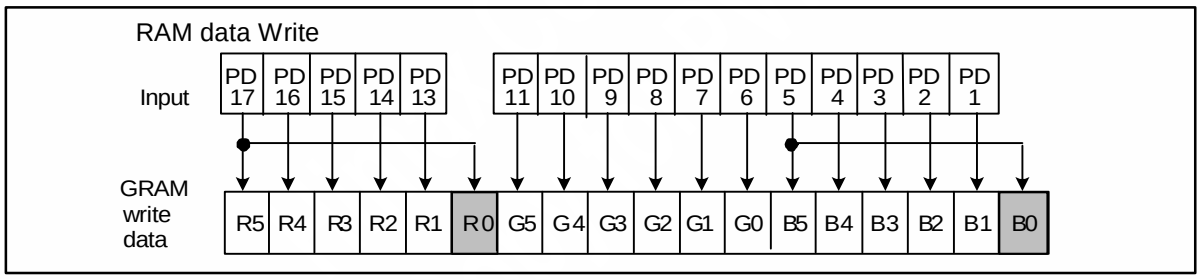


Figure 4. 26 Data format for16-bit interface

6-bit bus RGB interface

The 16-bit bus interface can be used by setting RIM1-0 bits to “10”. The Figure 4.27 is the example of 16-bit bus RGB interface with LCD Controller and HX8345-A. The display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via PD data bus (PD17-12 bits) to the internal GRAM and according to the signal of data enable (ENABLE). The unused pins(PD11-0) must be fixed to the VCC or VSSD level. The Figure 4.28 is the data format of 16-bit bus RGB interface.

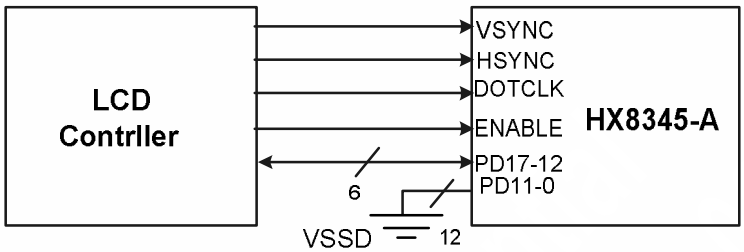


Figure 4. 27 6-bit RGB interface

RAM data write

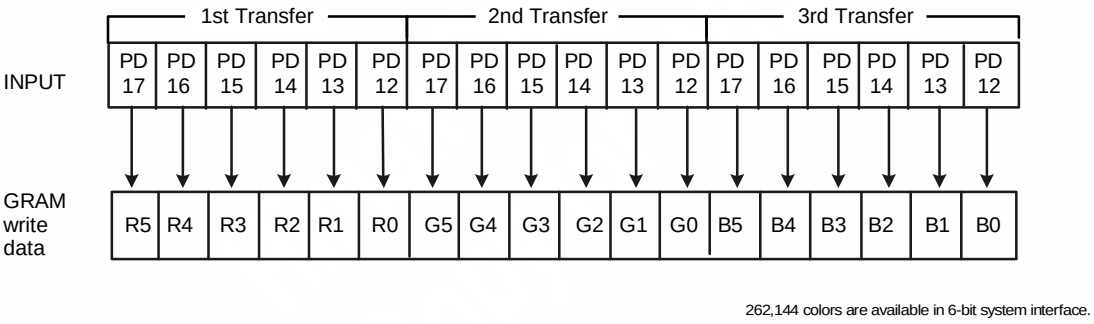


Figure 4. 28 Data format for 6-bit interface

The Figure 4.29 and Figure 4.30 is the timing relationship of system interface and RGB interface.

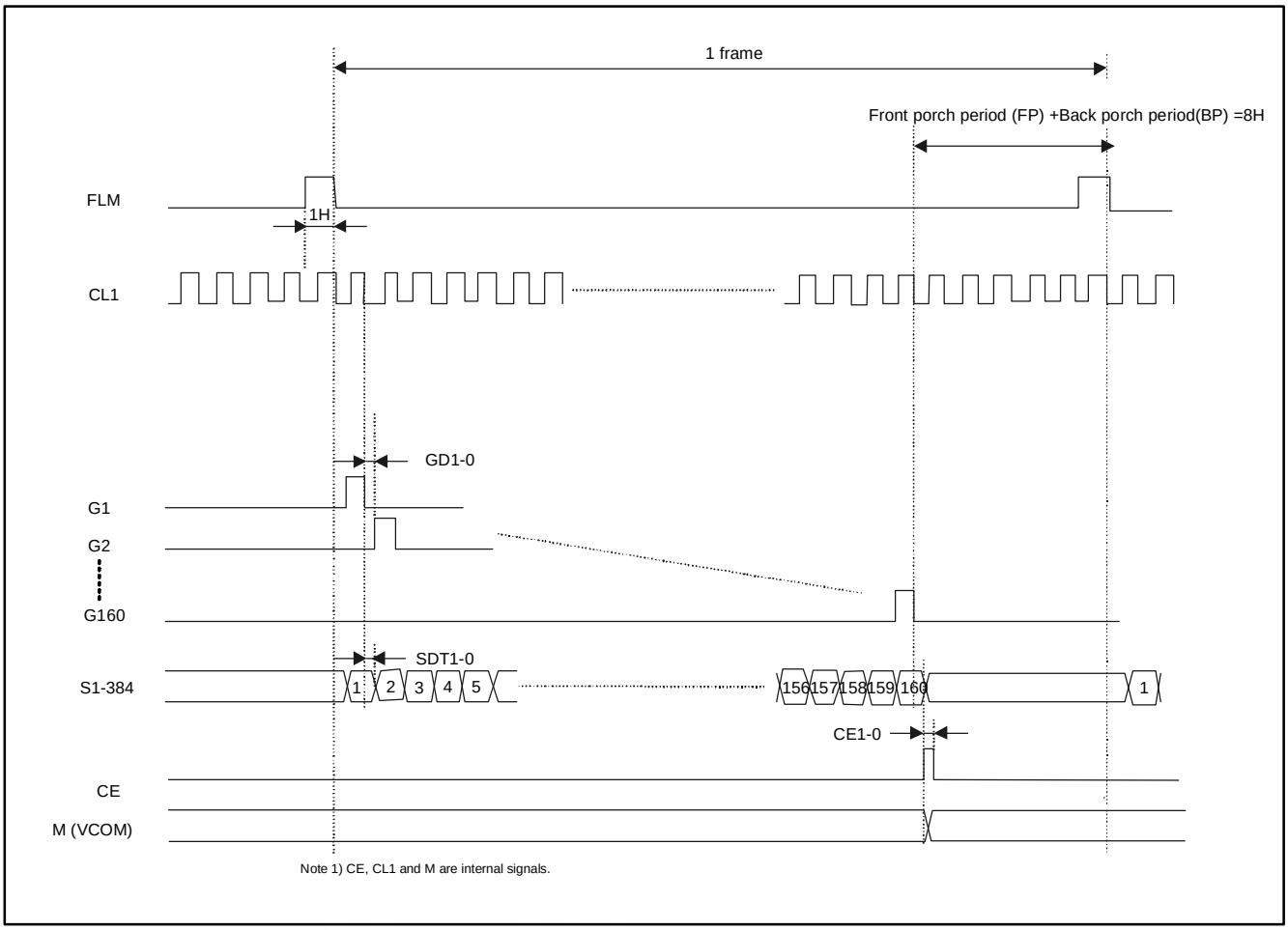


Figure 4. 29 Timing Relationship of System Interface Mode

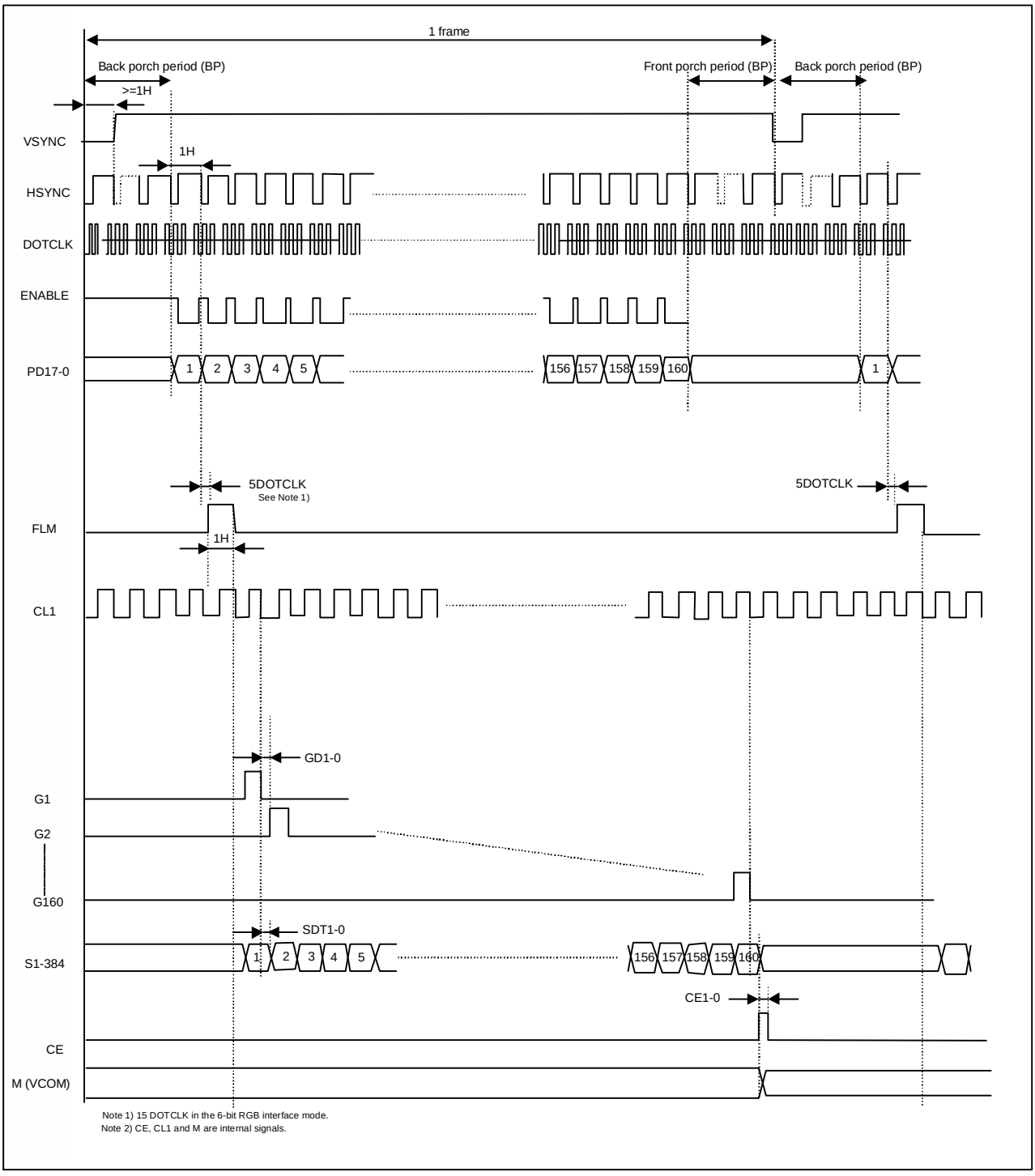


Figure 4. 30 Timing Relationship of RGB Interface Mode

5. Function Description

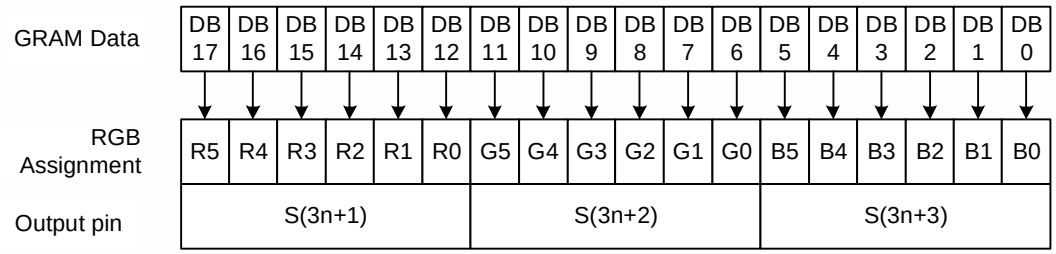
5.1 Graphics RAM

The HX8345-A have an internal graphics RAM that stores 46,080 bytes bit-pattern data, where one pixel is expressed by 18 bits. The GRAM address map is listed as follow:

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S373	S374	S375	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=1	GS=0	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G160	G1	0000H			0001H			0002H			---	007CH			007DH			007EH			007FH		
G159	G2	0100H			0101H			0102H			---	017CH			017DH			017EH			017FH		
G158	G3	0200H			0201H			0202H			---	027CH			027DH			027EH			027FH		
G157	G4	0300H			0301H			0302H			---	037CH			037DH			037EH			037FH		
G156	G5	0400H			0401H			0402H			---	047CH			047DH			047EH			047FH		
G155	G6	0500H			0501H			0502H			---	057CH			057DH			057EH			057FH		
G154	G7	0600H			0601H			0602H			---	067CH			067DH			067EH			067FH		
G153	G8	0700H			0701H			0702H			---	077CH			077DH			077EH			077FH		
G152	G9	0800H			0801H			0802H			---	087CH			087DH			087EH			087FH		
G151	G10	0900H			0901H			0902H			---	097CH			097DH			097EH			097FH		
G150	G11	0A00H			0A01H			0A02H			---	0A7CH			0A7DH			0A7EH			0A7FH		
G149	G12	0B00H			0B01H			0B02H			---	0B7CH			0B7DH			0B7EH			0B7FH		
G148	G13	0C00H			0C01H			0C02H			---	0C7CH			0C7DH			0C7EH			0C7FH		
G147	G14	0D00H			0D01H			0D01H			---	0D7CH			0D7DH			0D7EH			0D7FH		
G146	G15	0E00H			0E01H			0E01H			---	0E7CH			0E7DH			0E7EH			0E7FH		
⋮	⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	G151	9600H			9601H			9602H			---	967CH			967DH			967EH			967FH		
G9	G152	9700H			9701H			9702H			---	977CH			977DH			977EH			977FH		
G8	G153	9800H			9801H			9802H			---	987CH			987DH			987EH			987FH		
G7	G154	9900H			9901H			9902H			---	997CH			997DH			997EH			997FH		
G6	G155	9A00H			9A01H			9A02H			---	9A7CH			9A7DH			9A7EH			9A7FH		
G5	G156	9B00H			9B01H			9B02H			---	9B7CH			9B7DH			9B7EH			9B7FH		
G4	G157	9C00H			9C01H			9C02H			---	9C7CH			9C7DH			9C7EH			9C7FH		
G3	G158	9D00H			9D01H			9D02H			---	9D7CH			9D7DH			9D7EH			9D7FH		
G2	G159	9E00H			9E01H			9E02H			---	9E7CH			9E7DH			9E7EH			9E7FH		
G1	G160	9F00H			9F01H			9F02H			---	9F7CH			9F7DH			9F7EH			9F7FH		

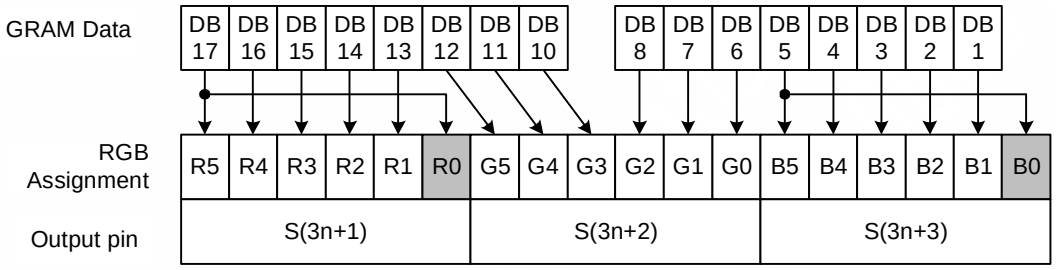
Table 5. 1 GRAM address and display panel position (SS ="0")

80-System/68-System 18-bit bus Interface



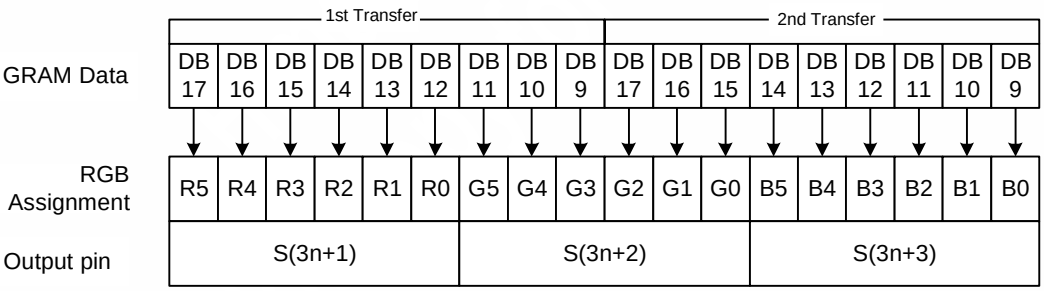
Note: n = lower eight bits of address (0 to 127)

80-System/68-System 16-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

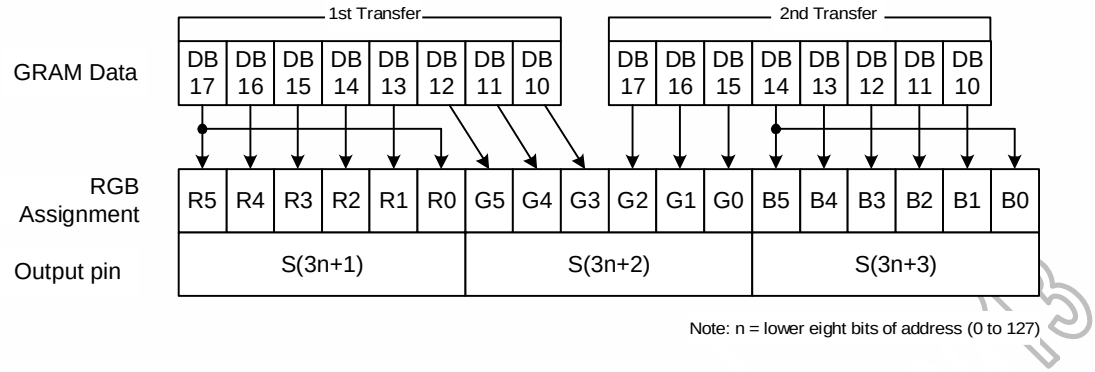
80-System/68-System 9-bit bus Interface



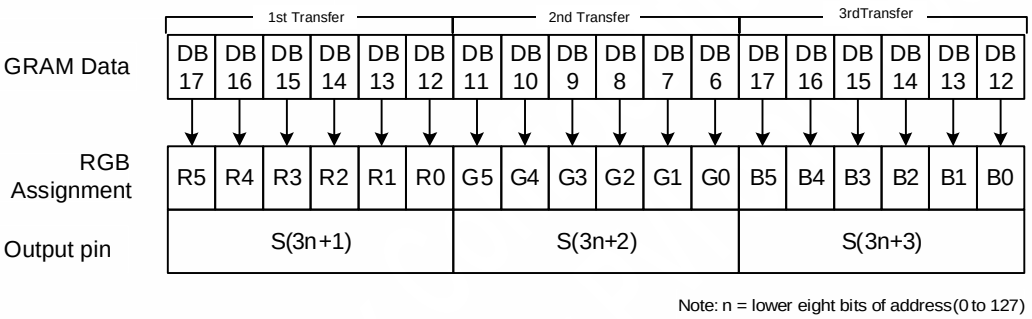
Note: n = lower eight bits of address (0 to 127)

Figure 5. 1 GRAM data and display data of 18-/16-9- bit system interface (SS = "0", BGR = "0")

80-System/68-System 8-bit bus Interface (2 transfers/pixel)



80-System/68-System 8-bi t Interface (3 transfers, 262k colors: TRI=1, DFM1-0=10)



80-System/68-System 8-bi t Interface (3 transfers, 65k colors: TRI=1, DFM1-0=11)

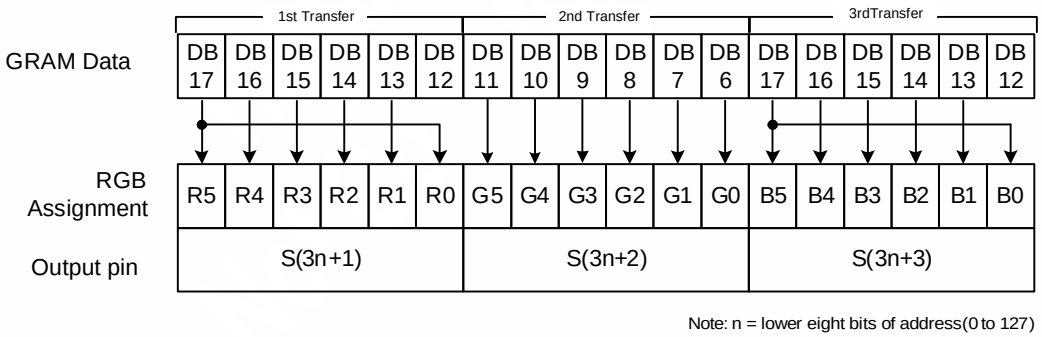
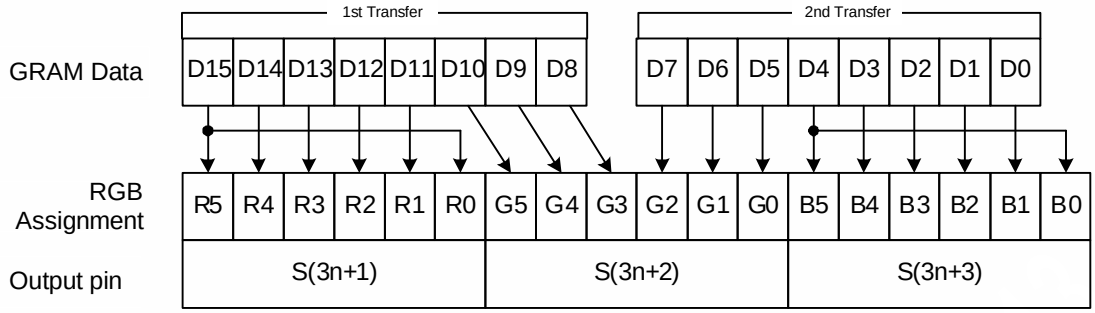


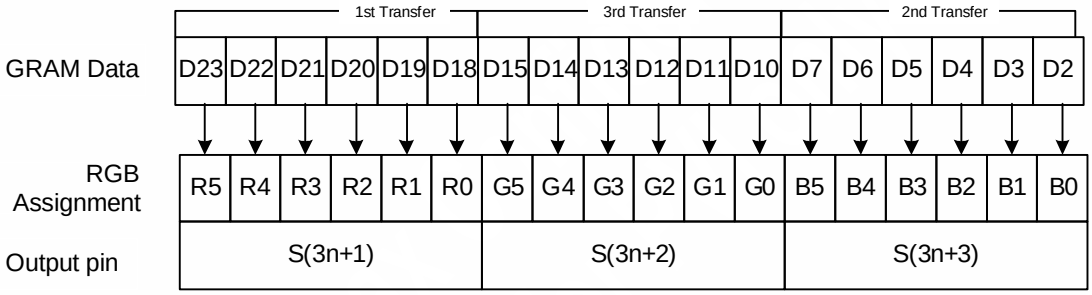
Figure 5. 2 GRAM data and display data of 8-bit system interface (SS = “0”, BGR = “0”)

Serial Data Transfer Interface (2 transfers/65k colors: TRI = 0)



Note: n = lower eight bits of address(0 to 127)

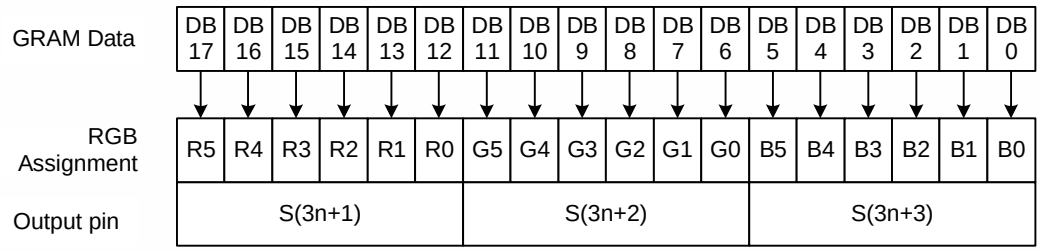
Serial Data Transfer Interface (3 transfers/262k colors: TRI = 1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

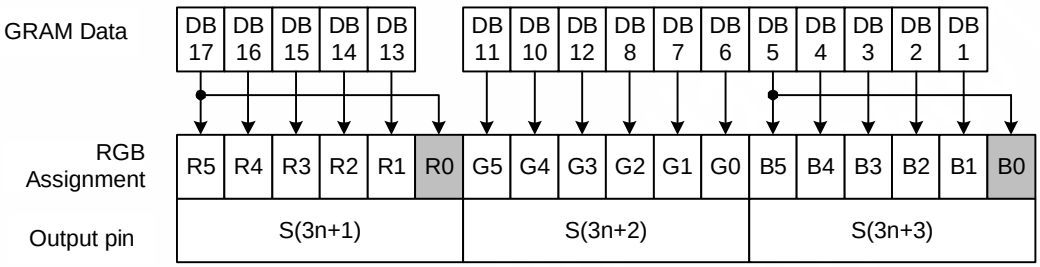
Figure 5. 3 GRAM data and display data of Serial Data Transfer interface (SS = "0", BGR = "0")

18-Bit RGB Interface



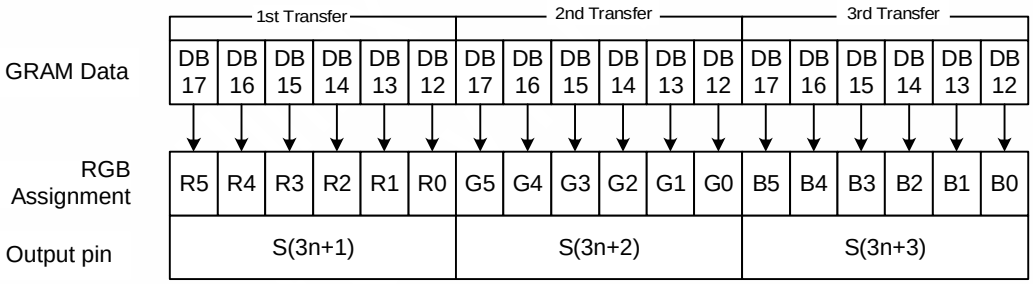
Note: n = lower eight bits of address (0 to 127)

16-Bit RGB Interface



Note: n = lower eight bits of address (0 to 127)

6-Bit RGB Interface



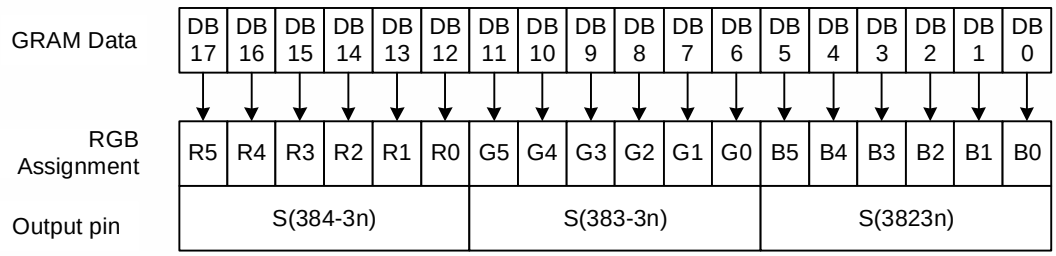
Note: n = lower eight bits of address (0 to 127)

Figure 5. 4 GRAM data and display data: RGB interface (SS = “0”, BGR = “0”)

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	---------	S376	S377	S378	S379	S380	S381	S382	S383	S384
GS=0	GS=1	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0			---------	DB---DB 17 ---0			DB---DB 17 ---0			DB---DB 17 ---0		
G1	G160	007FH			007EH			007DH			007CH			---------	0002H			0001H			0000H		
G2	G159	017FH			017EH			017DH			017CH			---------	0102H			0101H			0100H		
G3	G158	027FH			027EH			027DH			027CH			---------	0202H			0201H			0200H		
G4	G157	037FH			037EH			037DH			037CH			---------	0302H			0301H			0300H		
G5	G156	047FH			047EH			047DH			047CH			---------	0402H			0401H			0400H		
G6	G155	057FH			057EH			057DH			057CH			---------	0502H			0501H			0500H		
G7	G154	067FH			067EH			067DH			067CH			---------	0602H			0601H			0600H		
G8	G153	077FH			077EH			077DH			077CH			---------	0702H			0701H			0700H		
G9	G152	087FH			087EH			087DH			087CH			---------	0802H			0801H			0800H		
G10	G151	097FH			097EH			097DH			097CH			---------	0902H			0901H			0900H		
G11	G150	0A7FH			0A7EH			0A7DH			0A7CH			---------	0A02H			0A01H			0A00H		
G12	G149	0B7FH			0B7EH			0B7DH			0B7CH			---------	0B02H			0B01H			0B00H		
G13	G148	0C7FH			0C7EH			0C7DH			0C7CH			---------	0C02H			0C01H			0C00H		
G14	G147	0D7FH			0D7EH			0D7DH			0D7CH			---------	0D02H			0D01H			0D00H		
⋮	⋮	⋮			⋮			⋮			⋮			---------	⋮			⋮			⋮		
G149	G12	947FH			947EH			947DH			947CH			---------	9402H			9401H			9400H		
G150	G11	957FH			957EH			957DH			957CH			---------	9502H			9501H			9500H		
G151	G10	967FH			967EH			967DH			967CH			---------	9602H			9601H			9600H		
G152	G9	977FH			977EH			977DH			977CH			---------	9702H			9701H			9700H		
G153	G8	987FH			987EH			987DH			987CH			---------	9802H			9801H			9800H		
G154	G7	997FH			997EH			997DH			997CH			---------	9902H			9901H			9900H		
G155	G6	9A7FH			9A7EH			9A7DH			9A7CH			---------	9A02H			9A01H			9A00H		
G156	G5	9B7FH			9B7EH			9B7DH			9B7CH			---------	9B02H			9B01H			9B00H		
G157	G4	9C7FH			9C7EH			9C7DH			9C7CH			---------	9C02H			9C01H			9C00H		
G158	G3	9D7FH			9D7EH			9D7DH			9D7CH			---------	9D02H			9D01H			9D00H		
G159	G2	9E7FH			9E7EH			9E7DH			9E7CH			---------	9E02H			9E01H			9E00H		
G160	G1	9F7FH			9F7EH			9F7DH			9F7CH			---------	9F02H			9F01H			9F00H		

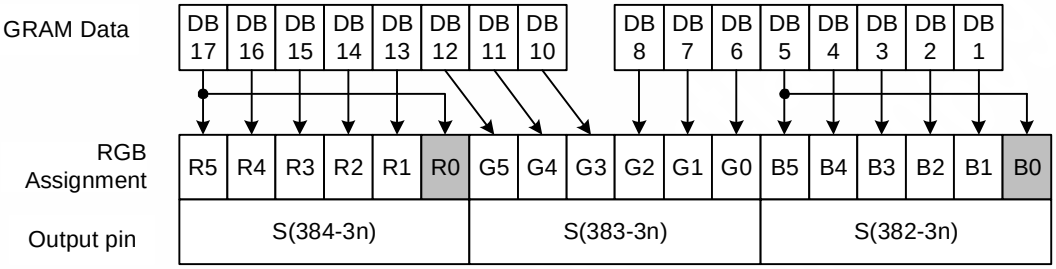
Table 5. 2 GRAM address and display panel position (SS ="1")

80-System 18-bit bus Interface



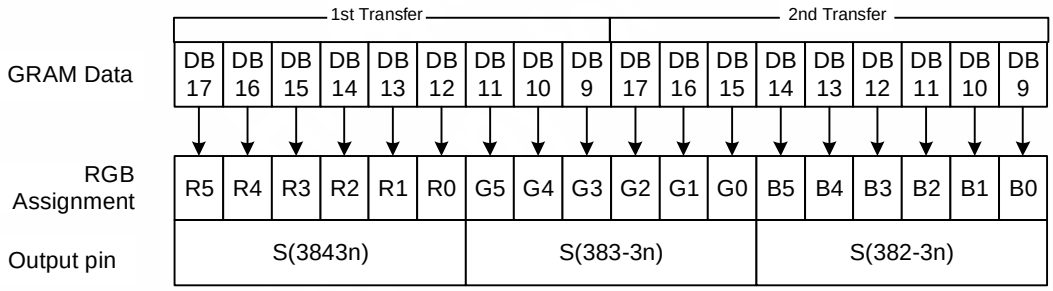
Note: n = lower eight bits of address (0 to 127)

80-System 16-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

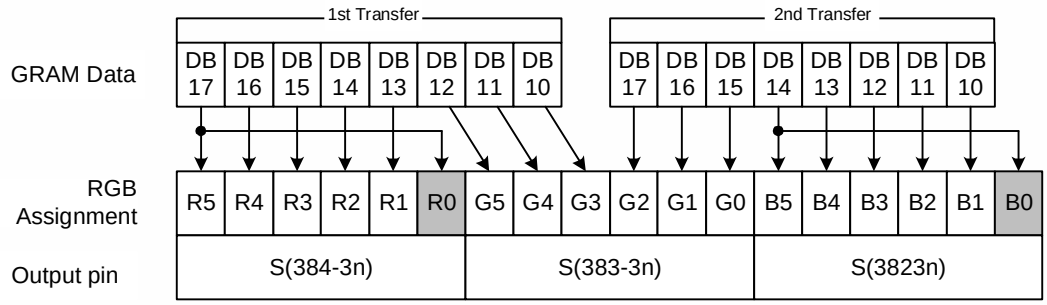
80-System 9-bit bus Interface



Note: n = lower eight bits of address (0 to 127)

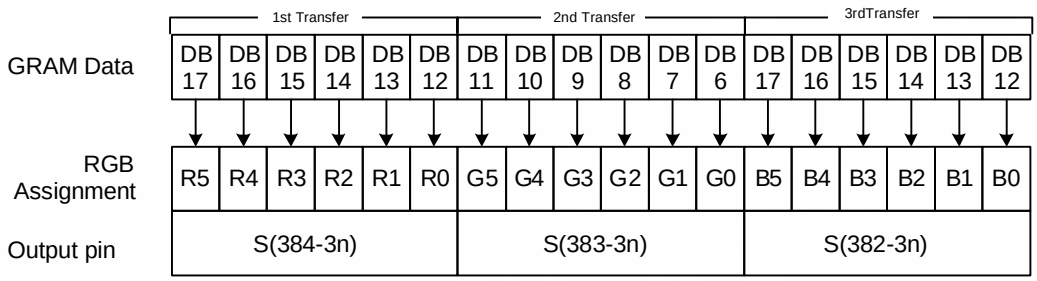
Figure 5. 5 GRAM data and display data of 18-/16-/9- bit system interface (SS = "1", BGR = "1")

80-System 8-bit bus Interface/ Serial Data Transfer Interface (2 transfers/pixel)



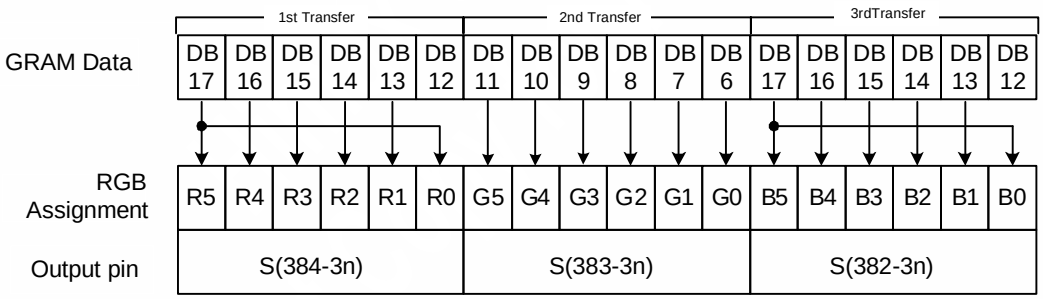
Note: n = lower eight bits of address (0 to 127)

80-System/68-System 8-bi t Interface (3 transfers, 262k colors: TRI=1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

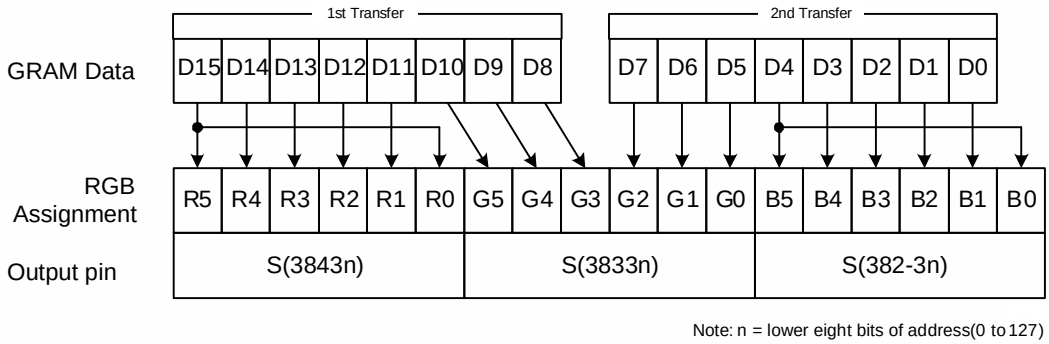
80-System/68-System 8-bi t Interface (3 transfers, 65k colors: TRI=1, DFM1-0=11)



Note: n = lower eight bits of address(0 to 127)

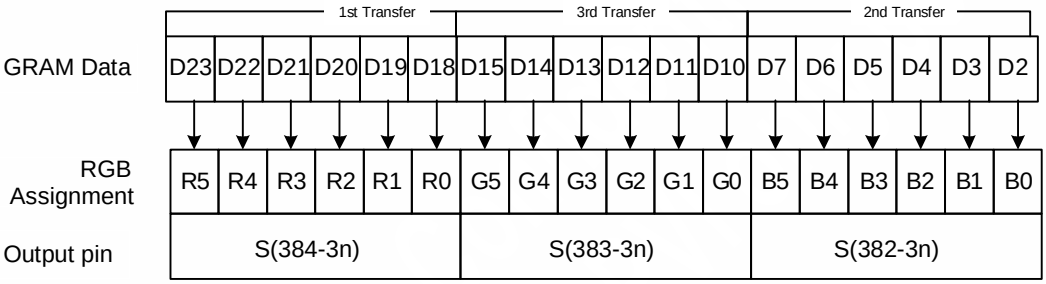
Figure 5. 6 GRAM data and display data of 8-bit system interface (SS = “1”, BGR = “1”)

Serial Data Transfer Interface (2 transfers/65k colors: TRI = 0)



Note: n = lower eight bits of address(0 to 127)

Serial Data Transfer Interface (3 transfers/262k colors: TRI = 1, DFM1-0=10)



Note: n = lower eight bits of address(0 to 127)

Figure 5. 7 GRAM data and display data of Serial Data transfer interface (SS = “1”, BGR = “1”)

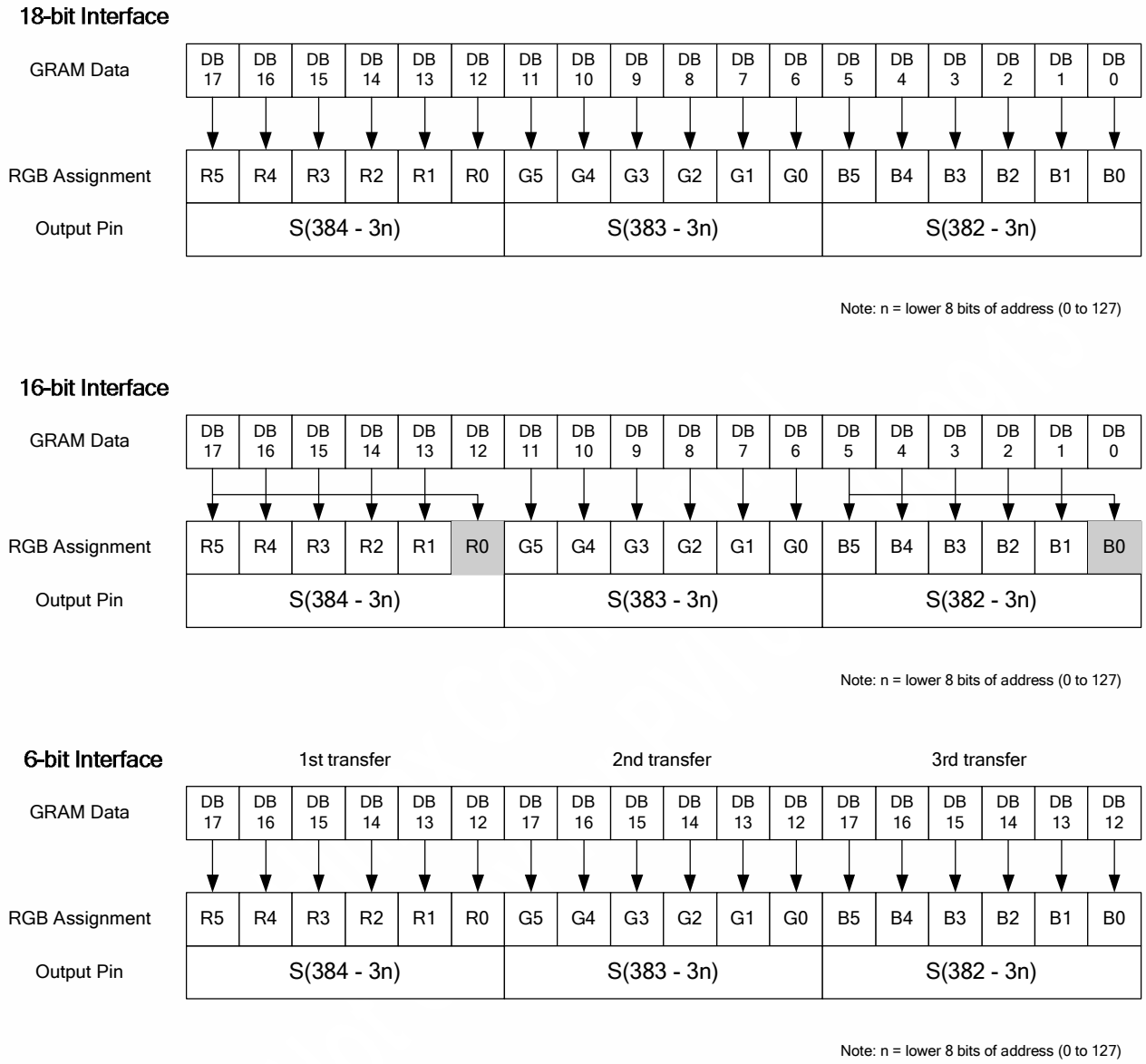


Figure 5. 8 GRAM data and display data: RGB interface (SS = “1”, BGR = “1”)

5.1.1 Window Address Function

The HX8345-A contains a 16-bit bus address counter (AC) which assigns address for writing pixel data to GRAM. The most eight bits of AC are express Y address (line address) and the lower eight bits of AC are express X address (pixel address). Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (AM bit and I/D bits) setting. However, the AC will be not updated after reading from GRAM.

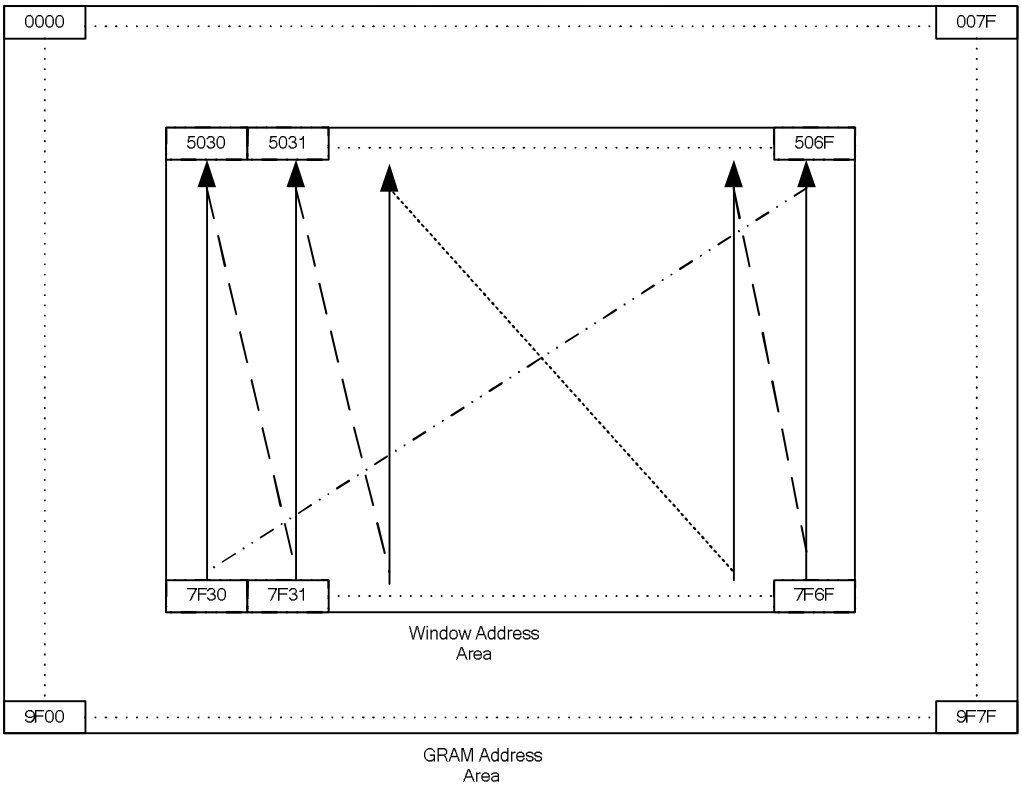
To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0). Therefore, the data can be written consecutively without thinking a data wrap by those bit function. The address setting of window and GRAM are listed as following:

The window addresses setting range:

00H" HSA7-0" HEA7-0" 7FH
00H" VSA7-0" VEA7-0" 9FH

GRAM address setting range:

HSA7-0" AD7-0" HEA7-0
VSA7-0" AD15-8" VEA7-0



Registers setting in this example:
HSA7-0=30, HSE7-0=6F, VSA7-0=50, VEA7-0=7F, AM=1, ID1-0=00

Figure 5. 9 An Example of Window Address Function

5.2 Graphics Operation Function

Write-data Mask function (WM)

The write-data mask function executes the operation of writing the corresponding bits to GRAM when the corresponding bits of the write data mask register (WM17-0) are given “0” and out of writing the corresponding bits of GRAM when the corresponding bits of the write data mask register (WM17-0) are given “1” contrary. Furthermore, the data sent from microcomputer are expanded into 18 bits internally in the 8/16-bit bus system interface, and 16-bit bus RGB interface. But in 18-bit bus system or RGB interface, data are not expanded.
When executes the write-data mask function, the GRAM data not overwritten but retained. This function is usually used when only corresponding bits of one specific pixel are rewritten or a designated display color is changed separately.

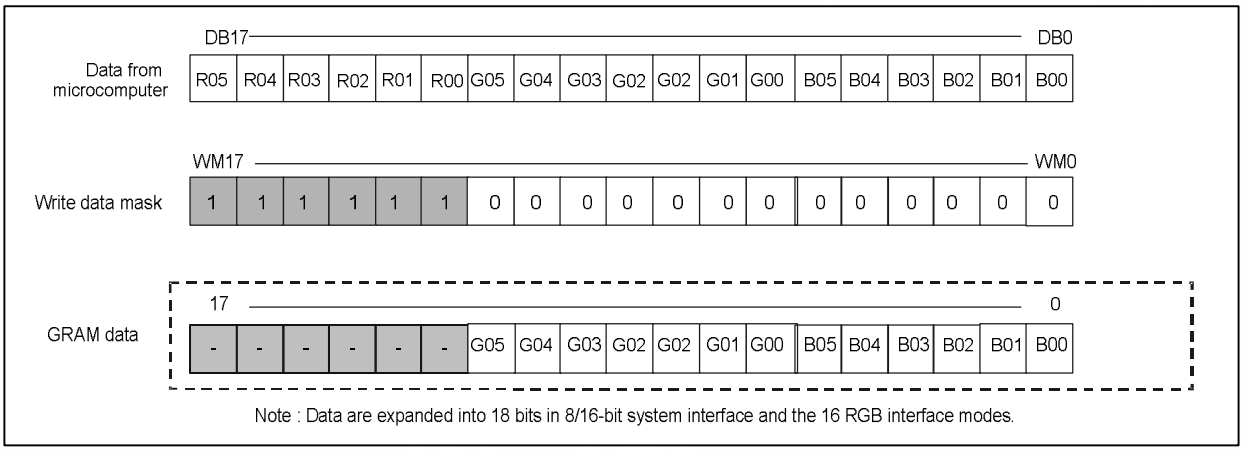


Figure 5. 10 Write data mask function

Logical Operation function (LG)

Logical operation when access the GRAM. The functions of the LG2-0 are:

000: replacement
001: OR operation
010: AND operation
011: XOR operation
100: replacement with matched read
101: replacement with unmatched read
110: replacement with matched write
111: replacement with unmatched write

Compare function (CP)

When LG2-0 is set to 100 or 101, match condition is depending on the CP and GRAM.
When LG2-0 is set to 110 or 111, match condition is depending on the CP and writing data.

5.3 Display Function

5.3.1 Scan Mode Setting

The HX8345-A can set SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8345-A.

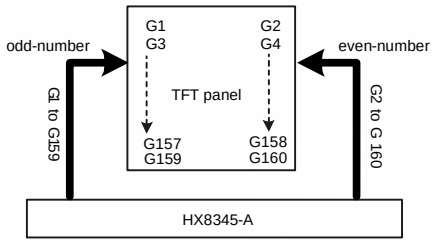
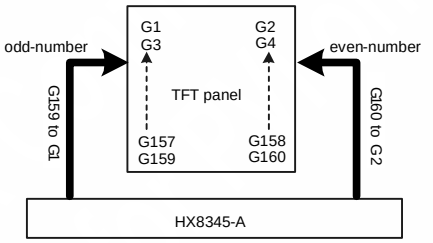
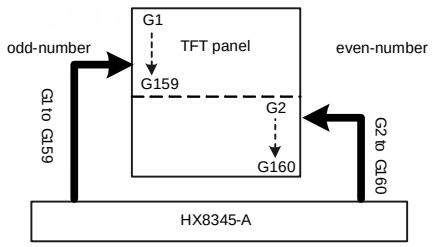
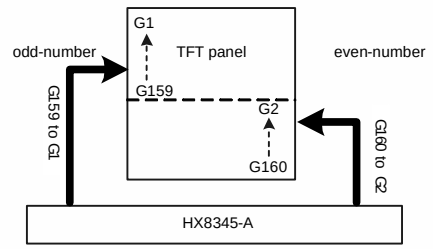
SM	GS	Scan direction
0	0	 G1, G2, G3, G4,.... G157, G158, G159, G160
0	1	 G160, G159, G158, G157,.... G4, G3, G2, G1
1	0	 G1, G3, G5,....G157, G159, G2, G4, G6,....G158, G160
1	1	 G160, G158, G156, ...G4, G2, G159, G157, G155,....G3, G1

Figure 5. 11 SCAN Mode Setting

5.3.2 Partial Screen Display

The HX8345-A has one or two screens driving functions. The position of display screen register (R14h and R15h) can display at any position of the whole screen. The numbers of display lines that display on the first and second windows must be less than total LCD-driving lines setting (NL4…0). The rest display area in the screen should be white display if the type of LCD is normally white and should be black display if the type of LCD is normally black. Therefore, the partial display can reduce the power consumption.

As the below, the first window start line from the SS1(7...0) and end line at SE1(7...0), that are specified by the 1st Display Window Driving Position Register(R14h). The second window start line from SS2(7...0) and end line at SE2(7...0), that are specified by 2nd Display Window Driving Position Register(R15h). And the second display window is availed when the SPT bit is set to 1. The number of the total selection driving lines included the 1st and 2nd display window must be equal to or less than the LCD Drive Line(NL).

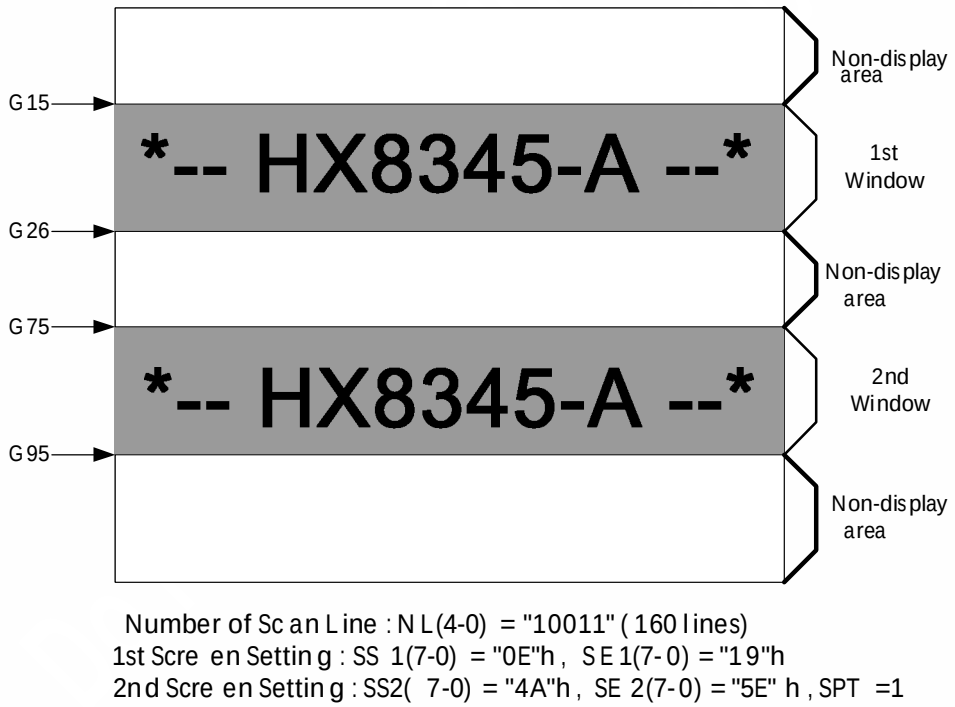


Figure 5. 12 Partial Screen Display Example in 2-Window Driving

The conditions as following must be contented when setting the start line SS1(7..0) and end line SE1(7..0) of the 1st display window at register (R14h) and the start line SS2(7..0) and end line SE2(7..0) of the 2nd display window at register (R15h).

Note: That incorrect display may occur if the conditions setting are not contented.

Condition: 0 ≤ SS1(7-0) ≤ SE1(7-0) ≤ NL

Register Settings	Display Operation
SE1(7..0) - SS1(7..0) +1 = NL	Whole-Screen Display The area of SE1(7..0)-SS1(7..0) is normally displayed
0 < SE1(7..1) - SS1(7..0) +1 < NL	Partial screen display The area of SE1(7…0)-SS1(7...0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Table 5. 3 Conditions on the One Screen Driving (SPT = 0)

Note: The SS2(7-0) and SE2(7-0) settings are ignored.

Condition: 0 ≤ SS1(7-0) ≤ SE1(7-0) < SS2(7-0) ≤ SE2(7-0) ≤ NL

Register Settings	Display Operation
(SE1(7..0) - SS1(7..0) +1) + (SE2(7..0) - SS2(7..0)+1) = NL	Whole-Screen Display The area of (SE27…20) - (SS17…10) is normally displayed
(SE1(7..0) - SS1(7..0) +1) + (SE2(7..0) - SS2(7..0) +1) < NL	Partial Screen Display The area of SE1(7...0) - SS1(7...0) and SE2(7...0) - SS2(7...0) is normally displayed. The rest area is displayed refer to the output level based on the PT (R07h) setting (non-display area).

Table 5. 4 Condition on the Two Screen Driving (SPT = 1)

The driver outputs for non-display area on partial display can be specified. Set the values to match the characteristics for the panel.

PT1	PT0	Source Output in Non-Display Area		VCOM output
		Positive Polarity	Negative Polarity	
0	0	V63	V0	VCOMH VCOML
0	1	V63	V0	VCOMH VCOML
1	0	VSSD	VSSD	VCOMH VCOML
1	1	Hi-Z	Hi-Z	-

Table 5. 5 Source Output in Non-Display Area in Partial Display

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

Table 5. 6 Gate Output in Non-Display Area in Partial Display

Setting of the partial display should follow the flow shown as below

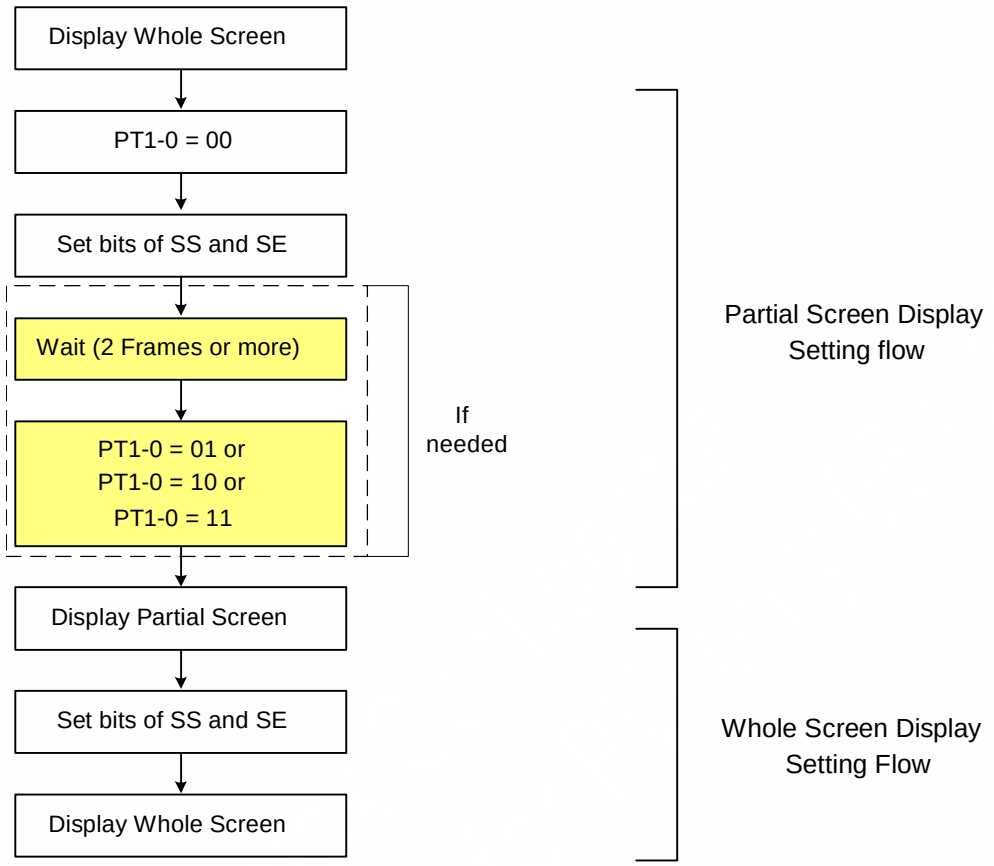


Figure 5. 13 Partial Display Setting Flow

5.3.3 8-Color Display

The HX8345-A supports an 8-color display mode. The grayscale level to be used is V0 and V63 with R5, G5, B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

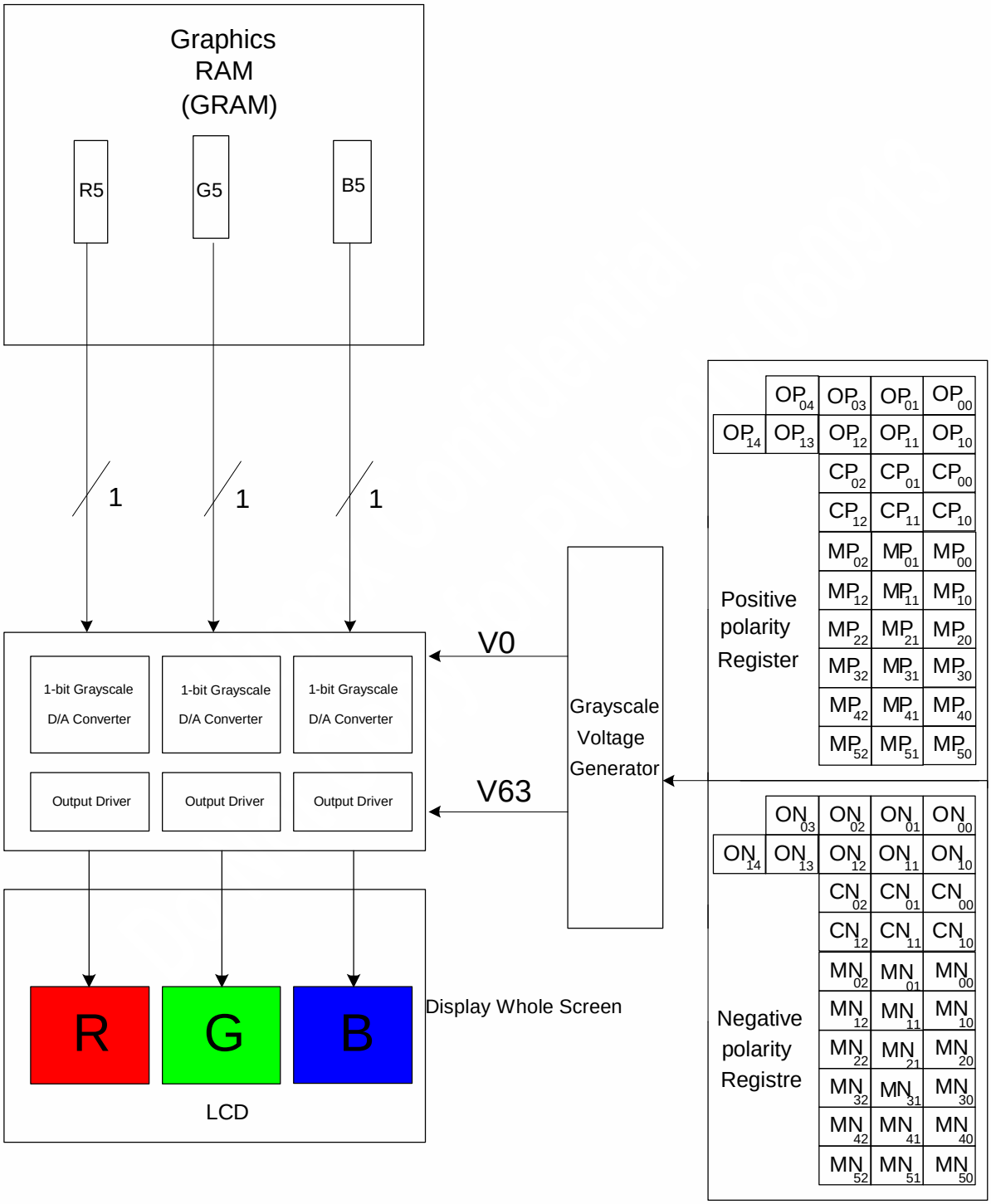


Figure 5. 14 Grayscale Control in 8-Color Mode

The follow figure is the switch sequence between the 262,144-color mode and 8-color mode:

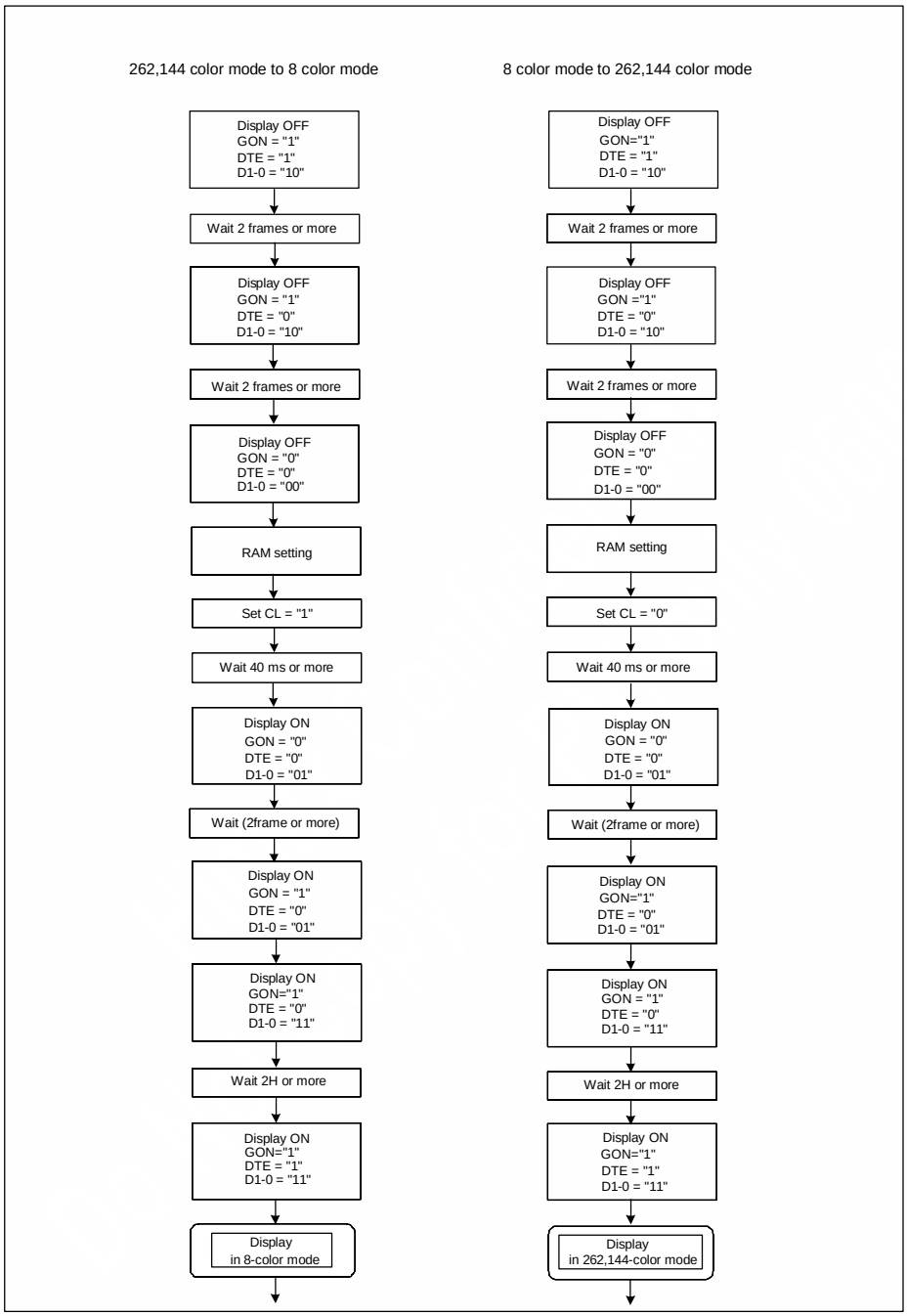


Figure 5. 15 Switch Sequence between 262,144-color Mode and 8-color Mode

5.3.4 N-line Inversion LCD Drive

The HX8345-A supports frame inversion and n-line inversion LCD current driving, which n chooses 1~64. The inversion operation is controlled by POL (Polarity of Liquid Crystal) signal which interval is set by NW5-0 bits in R02h register. The HX8345-A internally transfers POL signal for alternating the VCOM voltage and alternates source output voltage according to gamma register with POL signal, which changes the polarity of LCD driving voltage. When a display quality problem occurs, the n-line inversion LCD drive can improve the quality by setting proper n value.
The value of n also represented by the NW bits+1, which represented LCD alternating frequency becomes high when the number of inversion lines were setting a smaller value, hence ,in the LCD cells, the charge or discharge current is increased.

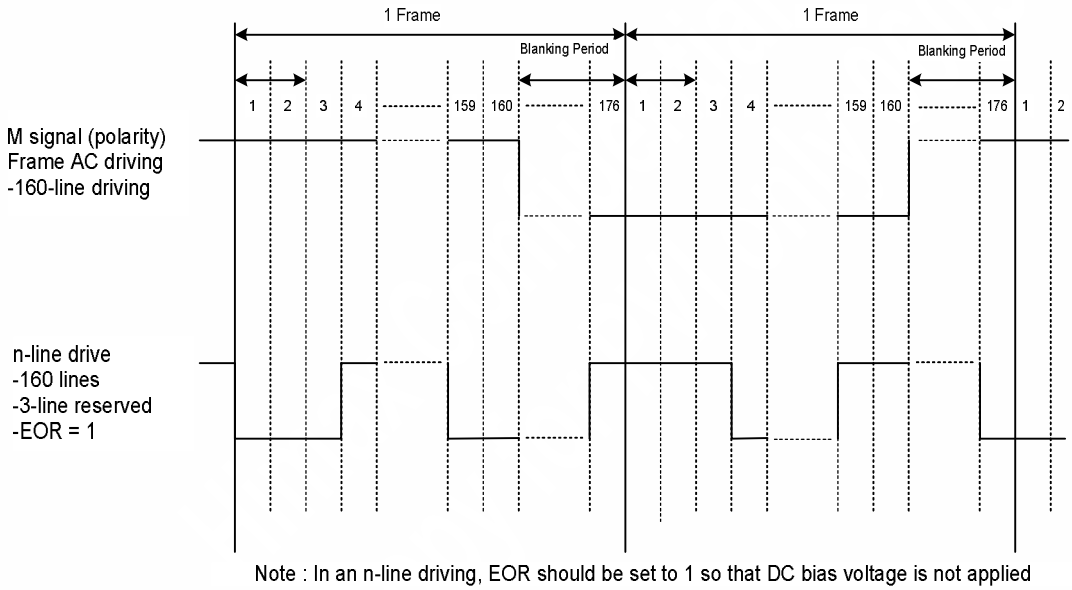


Figure 5. 16 N-line Inversion Driving Diagram

5.3.5 Interlaced Driving Function

The HX8345-A has a interlaced function that divided one frame into 3 fields to drive the LCD to avoid flicker To confirm the display quality with the actual LCD display then determined the number of fields. As following table, the gate selection where the number of field is 3 (setting FLD1-0 = 11) and as following figure the output waveform when 3 field interlaced driving is performed is shown.

GS = 0

FLD1-0	11		
Gate \ Field	1	2	3
G1	*		
G2		*	
G3			*
G4	*		
G5		*	
G6			*
G7	*		
G8		*	
G9			*
:	:	:	:
G157			
G158	*		
G159		*	
G160			*

GS = 1

FLD1-0	11		
Gate \ Field	1	2	3
G160	*		
G159		*	
G158			*
G157	*		
:		*	
G9			*
G8	*		
G7		*	
G6			*
G5	:	:	:
G4			
G3	*		
G2		*	
G1			*

Table 5. 7 Combined with the GS and FLD Setting

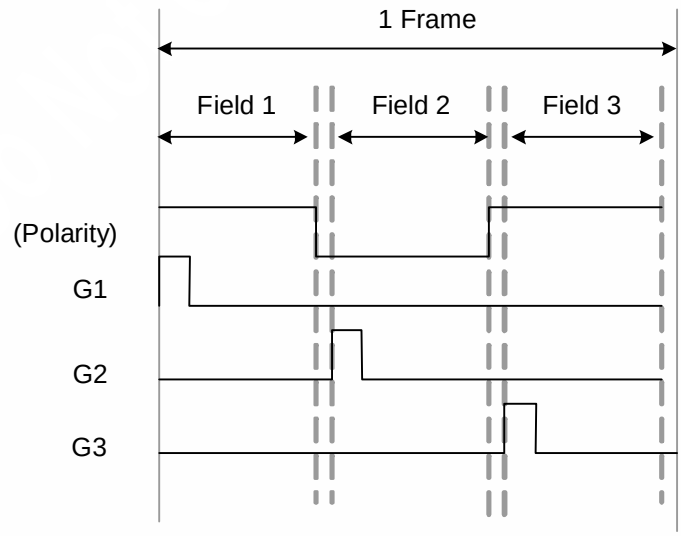


Figure 5. 17 Output Timing for Interlaced Gate Signals (Three-Field is Selected)

5.3.6 AC Driving Alternating Timing

LCD must be driven by alternating voltage polarity between liquid crystal layers. The operation of AC drive timing in each type is shown below. The period of AC drive timing is the same as the period of POL signal which is controlled by the value in register R02h (NW).

In frame-inversion AC drive, LCD-driving signal alternates after one frame finishing display and then a FP or back-porch blanking period are inserted. During the blanking period all gate outputs are remain Vgoff. In interlaced drive, LCD-driving signal alternates after one field finishing display and then a blanking period is inserted. The sum of blanking periods in three fields is equal to the sum of BP and FP blanking period set in a frame. For n-line inversion AC drive, LCD-driving signal alternates before every n-line display starts. Back-porch blanking period is inserted before all display operations starting and front-porch blanking period is inserted after the completion of all display operations.

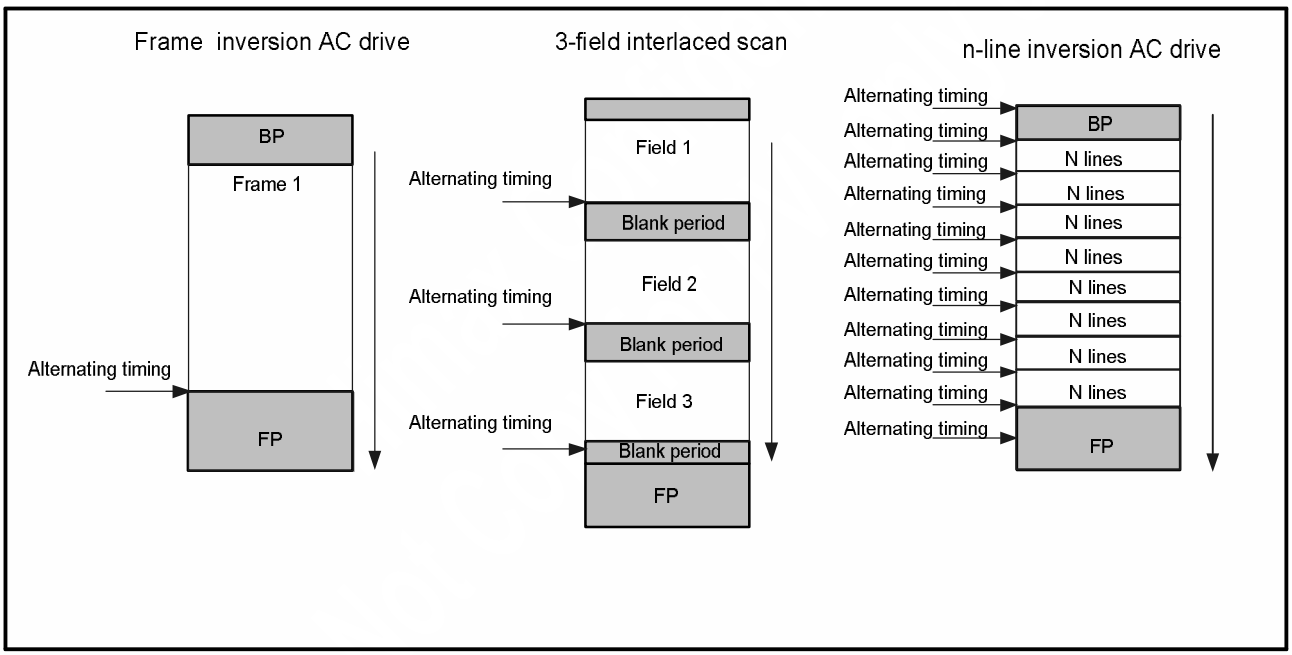


Figure 5. 18 AC Driving Alternating Timing Diagram

5.4 Frame-Frequency Adjustment Function

The HX8345-A supports frequency adjustment function of frame frequency stably that can adjust the frame frequency via the register (DIV, RTN bits) setting in R0Bh during the oscillation frequency.
An animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching (an animated display) is required, the frame frequency can be set higher.

Relationship between LCD Drive Duty and Frame Frequency

The LCD driving duty and the frame frequency is obtained by the following calculation. The frame frequency can be adjusted in the 1-H line period bit (RTN) and in the operation clock division bit (DIV) by write the instruction to the relative register.

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{RTN} \times \text{DIV} \times (\text{NL}+\text{BP}+\text{FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP% 16

Example Calculation: To set the maximum frame frequency to 60 Hz

Number of drive lines: 152 lines (NL=”10010”)

1-line period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1 Division

fosc = 60 Hz × (0 + 16) clock × 1 division × (152+16) lines = 161 (KHz)

In this case, the R-C oscillation frequency becomes 161 KHz. The external resistance value of the R-C oscillator must be adjusted so that the frequency of internal R-C oscillator is equal to 161 KHz. The display duty can be changed by the partial display with the same frequency setting as above.

5.5 γ-Correction Function

The HX8345-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

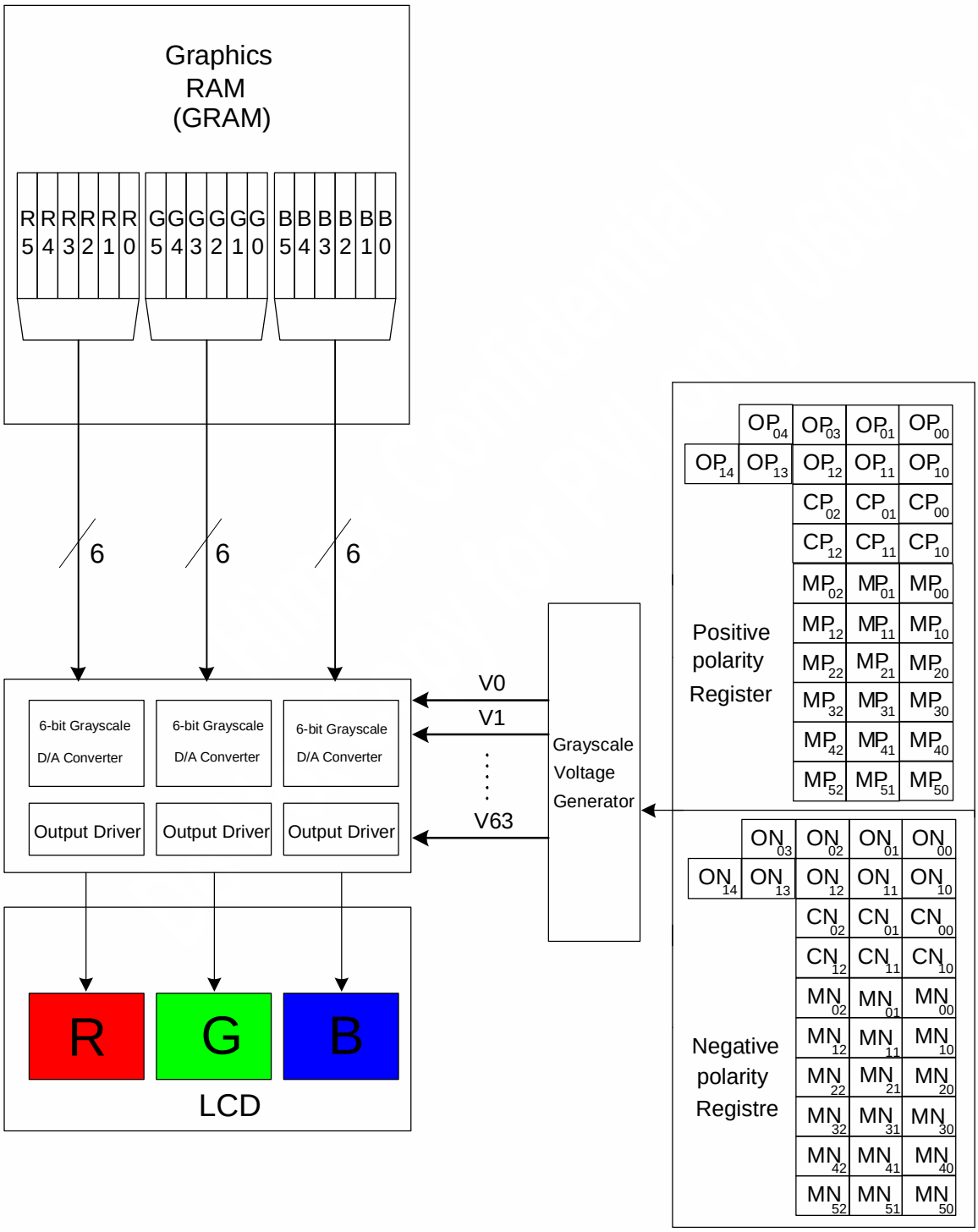


Figure 5. 19 Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

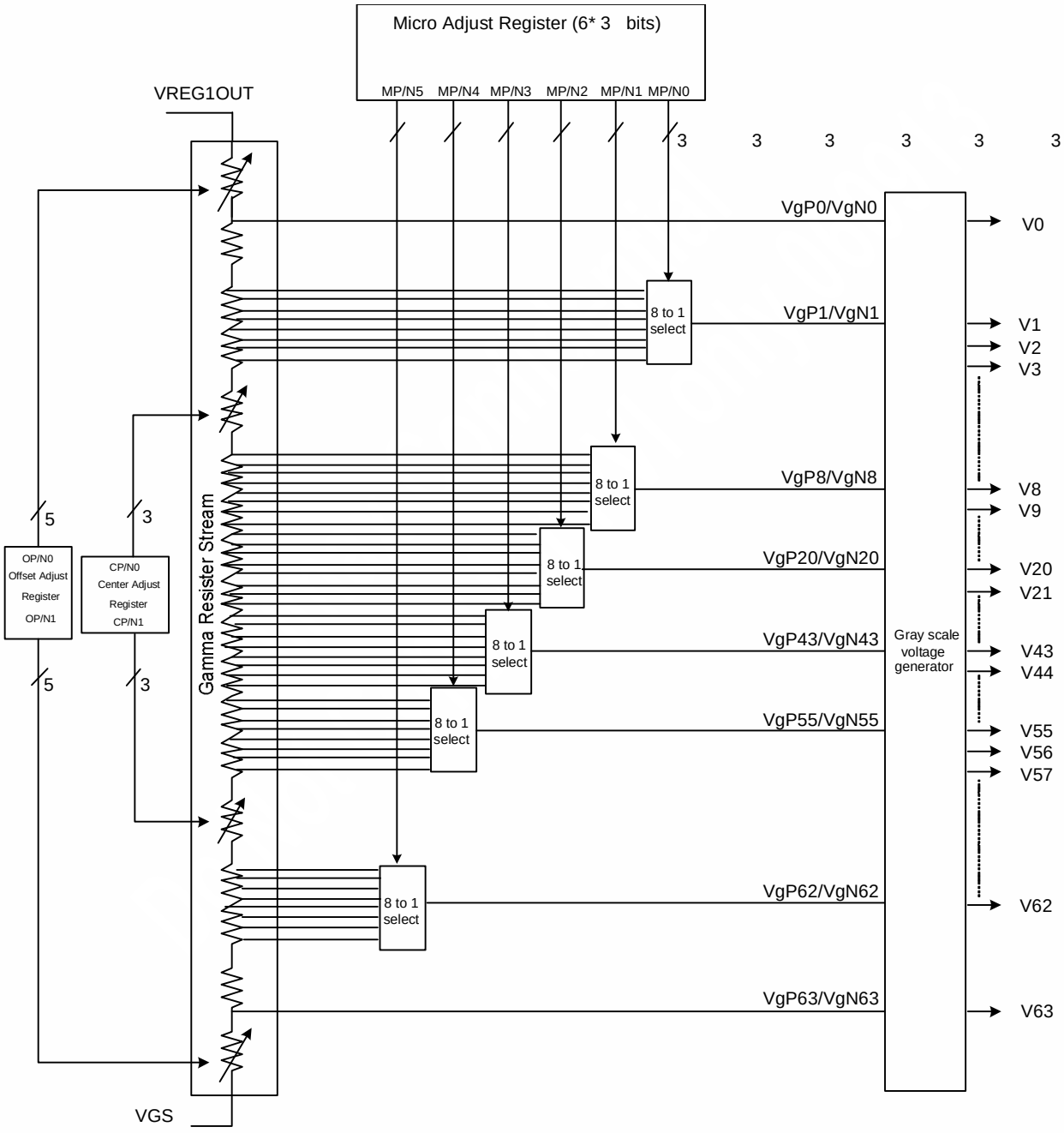


Figure 5. 20 Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This HX8345-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

(1) Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (Vg(P/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Table 5. 8 Gamma-Adjustment Registers

Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (Vg(P/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

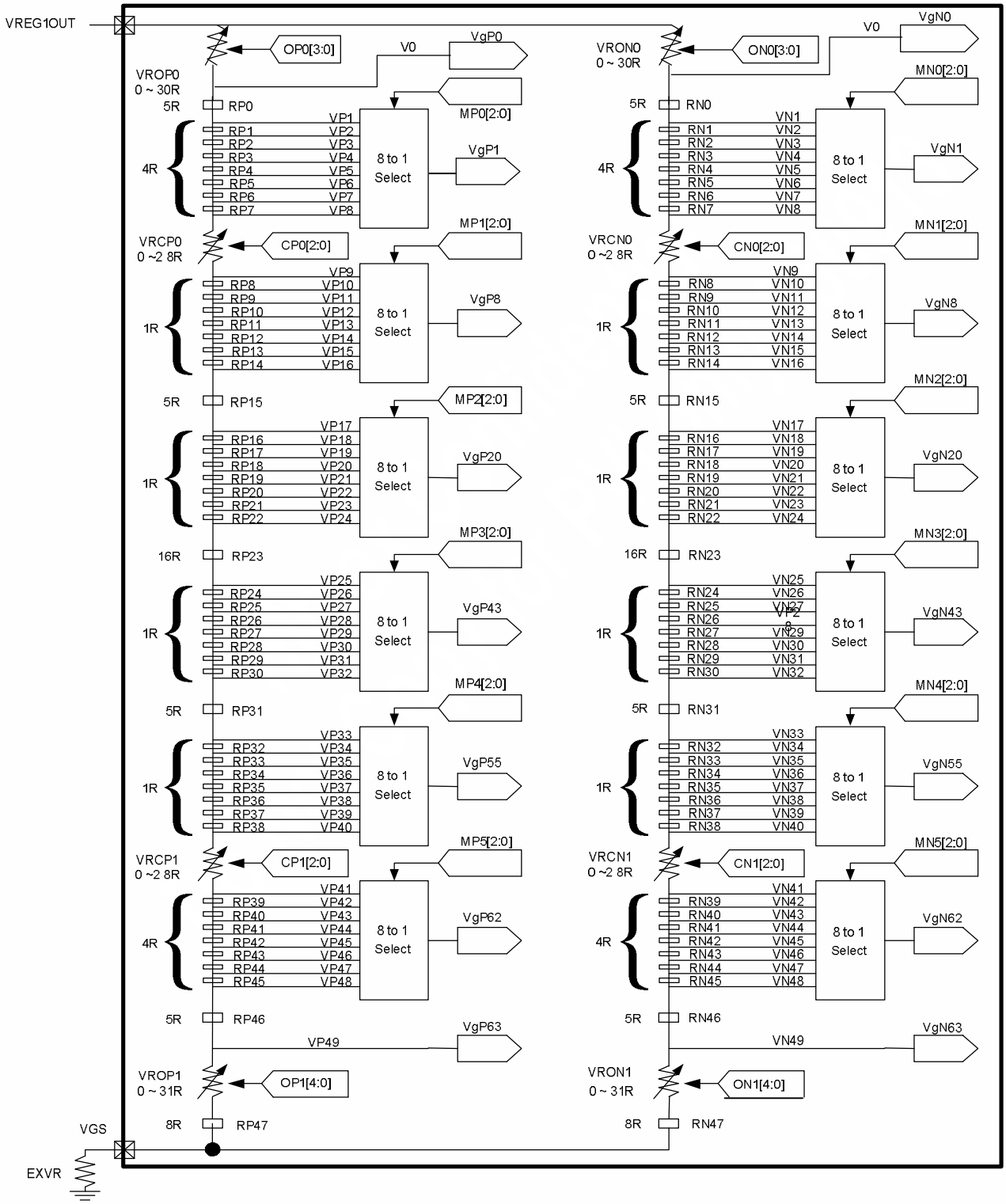


Figure 5. 21 Gamma Resister Stream and Gamma Reference Voltage

Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5. 9 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5. 10 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5. 11 Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationships are shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5. 12 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	----	VREG1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VREG1OUT-VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VREG1OUT-VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VREG1OUT-VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VREG1OUT-VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VREG1OUT-VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VREG1OUT-VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VREG1OUT-VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VREG1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VREG1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VREG1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VREG1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VREG1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VREG1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VREG1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VREG1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VREG1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VREG1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VREG1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VREG1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VREG1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VREG1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VREG1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VREG1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VREG1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VREG1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VREG1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VREG1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VREG1OUT-VD((VROP0+71R+VRCP0) /sumRP	V2P8
	MP3 2-0=100	VREG1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VREG1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VREG1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VREG1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VREG1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VREG1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VREG1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VREG1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VREG1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VREG1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VREG1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VREG1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VREG1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VREG1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VREG1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VREG1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VREG1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VREG1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VREG1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VREG1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	----	VREG1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

Table 5. 13 Voltage Calculation Formula (Positive Polarity)

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD=(VREG1OUT-VGS) ([sumRP(sumRN/(sumRP+sumRN)]/[sumRP×sumRN/(sumRP+sumRN)+EXVR]

Grayscale Voltage	Formula
V0	VgP0
V1	VgP1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VgP8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgP20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgP43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgP55
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VgP62
V63	VgP63

Table 5. 14 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Note: The following relationship should be retained.
VLCD – V0 > 0.5V
VLCD – V8 > 1.1V
V55-VSSD > 1.1V

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VREG1OUT-VD(VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VREG1OUT-VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VREG1OUT-VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VREG1OUT-VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VREG1OUT-VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VREG1OUT-VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VREG1OUT-VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VREG1OUT-VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VREG1OUT-VD((VRON0+33R) /sumRN	VN8
VgN8	MN1 2-0=000	VREG1OUT-VD((VRON0+33R+VRCN0) /sumRN	VN9
	MN1 2-0=001	VREG1OUT-VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VREG1OUT-VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VREG1OUT-VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VREG1OUT-VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VREG1OUT-VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VREG1OUT-VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VREG1OUT-VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	MN2 2-0=000	VREG1OUT-VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VREG1OUT-VD((VRON0+46R+VRCN0) /sumRN	VN18
	MN2 2-0=010	VREG1OUT-VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VREG1OUT-VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VREG1OUT-VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VREG1OUT-VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VREG1OUT-VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VREG1OUT-VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	MN3 2-0=000	VREG1OUT-VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VREG1OUT-VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VREG1OUT-VD((VRON0+70R+VRCN0) /sumRN	VN27
	MN3 2-0=011	VREG1OUT-VD((VRON0+71R+VRCN0) /sumRN	VNP8
	MN3 2-0=100	VREG1OUT-VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VREG1OUT-VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VREG1OUT-VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VREG1OUT-VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	MN4 2-0=000	VREG1OUT-VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VREG1OUT-VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VREG1OUT-VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VREG1OUT-VD((VRON0+83R+VRCN0) /sumRN	VN36
	MN4 2-0=100	VREG1OUT-VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VREG1OUT-VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VREG1OUT-VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VREG1OUT-VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	MN5 2-0=000	VREG1OUT-VD((VRON0+87R+VRCP0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VREG1OUT-VD((VRON0+91R+VRCP0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VREG1OUT-VD((VRON0+95R+VRCP0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VREG1OUT-VD((VRON0+99R+VRCP0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VREG1OUT-VD((VRON0+103R+VRCP0+VRCN1)/sumRN	VN45
	MN5 2-0=101	VREG1OUT-VD((VRON0+107R+VRCP0+VRCN1)/sumRN	VN46
	MN5 2-0=110	VREG1OUT-VD((VRON0+111R+VRCP0+VRCN1)/sumRN	VN47
	MN5 2-0=111	VREG1OUT-VD((VRON0+115R+VRCP0+VRCN1)/sumRN	VN48
VgN63	-	VREG1OUT-VD((VRON0+120R+VRCP0+VRCN1)/sumRN	VN49

Table 5. 15 Voltage Calculation Formula (Negative Polarity)

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD = (VREG1OUT-VGS) ([sumRP(sumRN/(sumRP+sumRN)]/[sumRP(sumRN/(sumRP+sumRN)+EXVR]

Grayscale Voltage	Formula
V0	VgN0
V1	VgN1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VgN8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgN20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgN43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgN55
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VgN62
V63	VgN63

Table 5. 16 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Note: The following relationship should be retained.

VLCD – V0 > 0.5V
VLCD – V8 > 1.1V
V55-VSSD > 1.1V

Relationship between GRAM Data and Output Level (REV = "0")

GRAM Data Set-up	Selected Grayscale	
RGB	N	P
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48

GRAM Data Set-up	Selected Grayscale	
RGB	N	P
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32

GRAM Data Set-up	Selected Grayscale	
RGB	N	P
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16

GRAM Data Set-up	Selected Grayscale	
RGB	N	P
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

Table 5. 17 GRAM Data and Grayscale Level

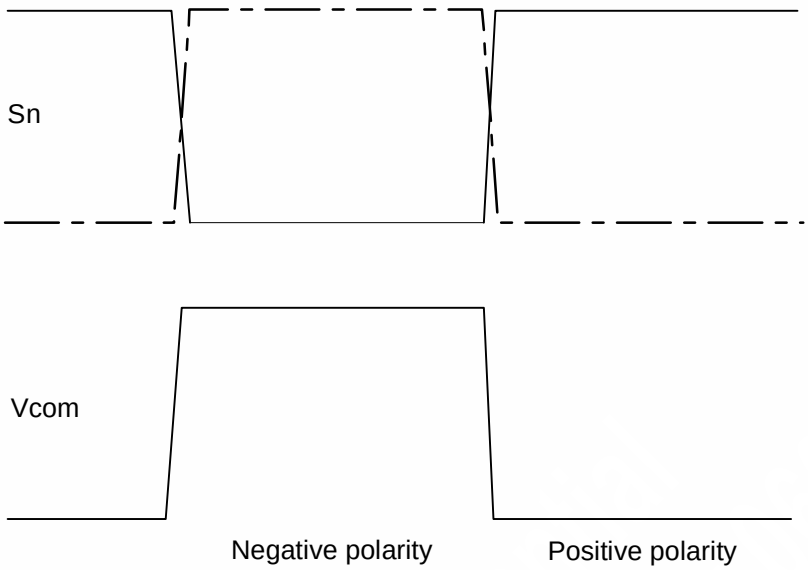


Figure 5. 22 Relationship between Source Output and VCOM

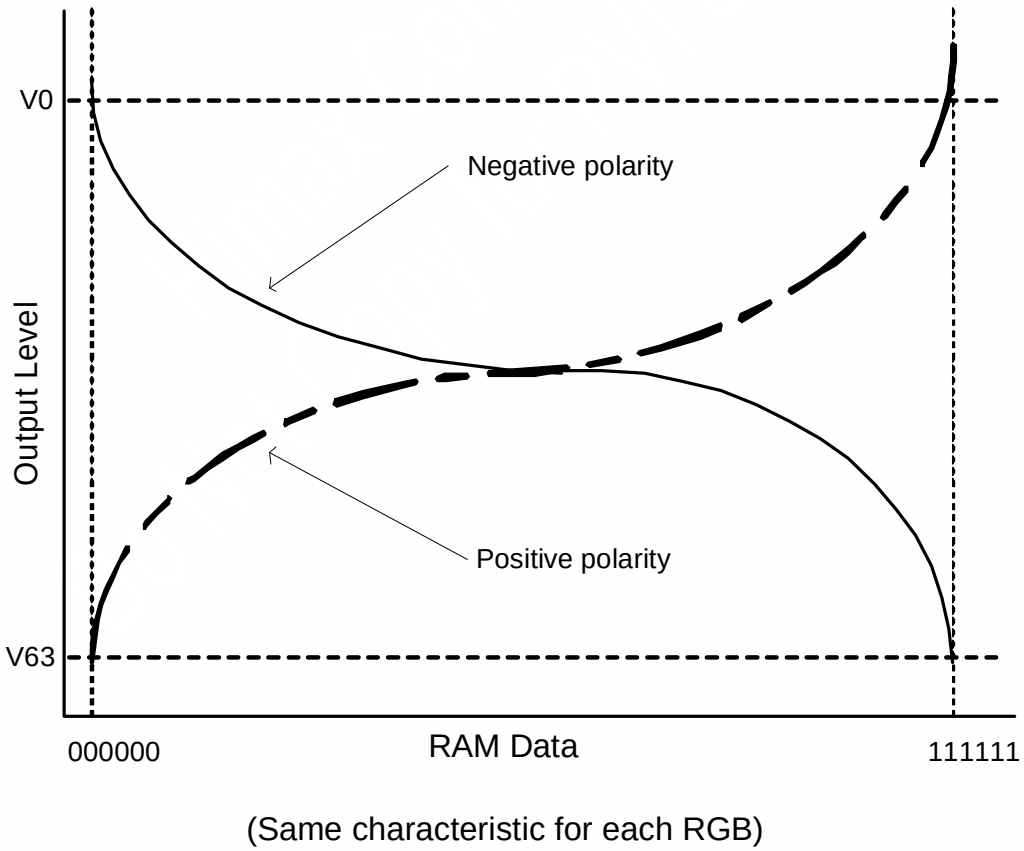


Figure 5. 23 Relationship between GRAM Data and Output Level

5.6 Oscillator

The HX8345-A can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor(Rf). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the DC Electrical Characteristics section.

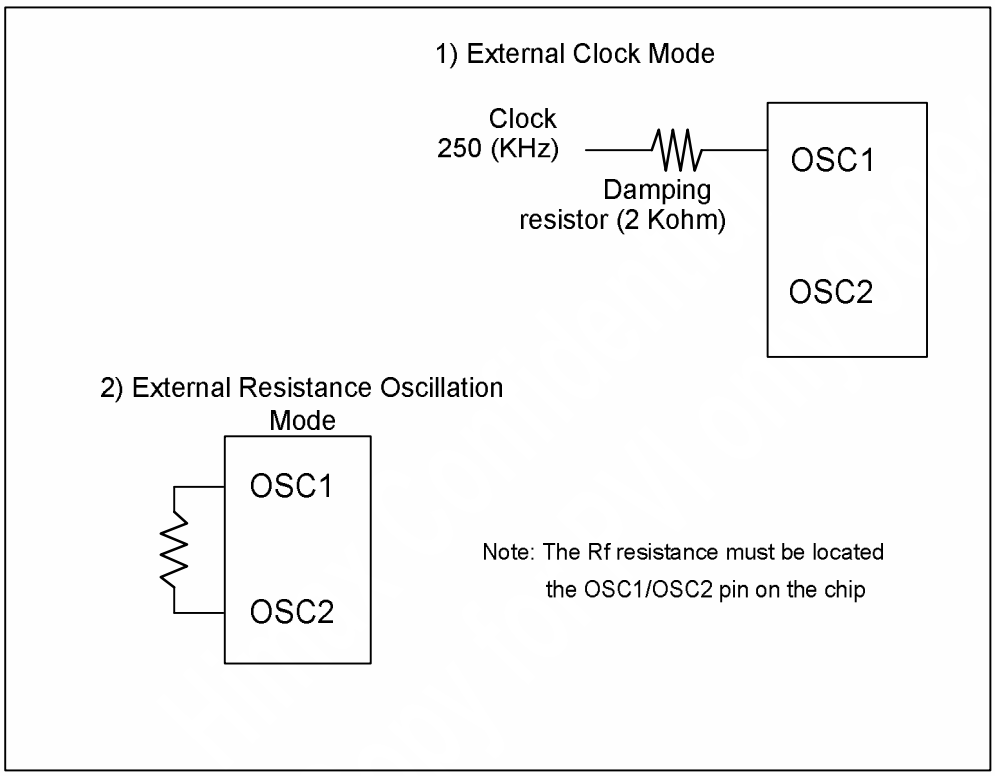


Figure 5. 24 Oscillation Circuit

External Resistance **(Rosc)**	R-C Oscillation Frequency: **Fosc(KHz)**			
	Vcc=2.4V	**Vcc=2.8V**	**Vcc=3.0V**	**Vcc=3.3V**
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD

Table 5. 18 External Resistance Value and R-C Oscillation Frequency (Temporally Defined)

Note: The real frequency has some deviation that dependant on the bumping resistance, glass wring, FPC trace and soldering resistance

6. Registers

The HX8345-A is a single chip with 18-bit bus architecture. The data read from/ write to internal GRAM through the 18-bit data format. When the internal operation of the HX8345-A want to start, first send the control information which is temporarily stored in the registers described as below to allow high-speed interface with a high-performance MPU. The internal operation of the HX8345-A is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (E_NWR), and the data bus signals (DB17-0), control the HX8345-A register.

There are eight categories of registers that is follows:

- Select the index
- Read back the status
- Control the display functions
- Control power management and save power function
- Process or operate the graphics data
- Set internal GRAM addresses for partial data updating
- Transfer data to and from the internal GRAM with High Speed Function
- Set grayscale level for the internal embedded grayscale gamma adjustment

The following specify the explanation of registers such as register format and bit function.

Register No.	Register	E_NWR	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
IR	Index	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
R00h	Start Oscillation	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_EN (1)	
	Device Code Read	R	1	1	0	0	0	0	0	1	1	0	1	0	0	0	1	0	1	
R01h	Driver Output Control(1)	W	1	0	0	0	0	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (0)	NL2 (0)	NL1 (1)	NL0 (1)	
R02h	LCD AC driving Control	W	1	0	0	0	0	FLD1 (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
R03h	Power Control (1)	W	1	0	0	0	0	0	BT2 (0)	BT1 (0)	BT0 (0)	DC02 (0)	DC01 (0)	DC00 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)	
R05h	Entry Mode	W	1	0	0	0	BGR (0)	0	0	0	0	0	0	ID1 (1)	ID0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
R06h	16-bits Compare Register	W	1	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
R07h	Display Control (1)	W	1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
R08h	Display Control (2)	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	FP3 (0)	FP2 (0)	FP1 (1)	FP0 (1)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	BP3 (0)	BP2 (1)	BP1 (0)	BP0 (1)	
R09h	Power Control (2)	W	1	0	0	0	0	0	0	DCM1 (0)	DCM0 (0)	DC12 (0	DC11 (0)	DC10 (0)	0	DK (0)	SAP2 (0)	SAP1 (1)	SAP0 (0)	
R0Ah	External Display Interface Control 1	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	0	0	PTG1 (0)	PTG0 (0)	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
R0Bh	Frame Cycle Control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1 (0)	CE0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
R0Ch	Power Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2 (0)	VC1 (0)	VC0 (0)	
R0Dh	Power Control (4)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
R0Eh	Power Control (5)	W	1	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
R0Fh	Gate Scan Start Position	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
R10h	CPWM 18/16-bit Selection	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F (0)	
R11h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	
R14h	First Screen Driving Position	W	1	SE17 (1)	SE16 (0)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	
R15h	Second Screen Driving Position	W	1	SE27 (1)	SE26 (0)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
R16h	Horizontal RAM Address Position	W	1	HEA7 (0)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
R17h	Vertical RAM Address Position	W	1	VEA7 (1)	VEA6 (0)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	
R20h	16-bits RAM Write Data Mask	W	1	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R21h	RAM Address Set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
R22h	RAM data Write/Read	R	1	RAM			WD17-0 /RAM		(RD17-0)											
R23h	18-bits RAM Write Data Mask (1)	W	1	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
R24h	18-bits RAM Write Data Mask (2)	W	1	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
R25h	18-bits Compare Register (1)	W	1	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
R26h	18-bits Compare Register (2)	W	1	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	

Register No.	Register	E_NWR	RS	Upper Code								Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
R30h	r Control (1)	W	1	0	0	0	0	0	MP 12 (0)	MP 11 (0)	MP 10 (0)	0	0	0	0	0	MP 02 (0)	MP 01 (0)	MP 00 (0)	
R31h	r Control (2)	W	1	0	0	0	0	0	MP 32 (0)	MP P31 (0)	MP 30 (0)	0	0	0	0	0	MP 22 (0)	MP 21 (0)	MP 20 (0)	
R32h	r Control (3)	W	1	0	0	0	0	0	MP52 (0)	MP 51 (0)	MP 50 (0)	0	0	0	0	0	MP 42 (0)	MP 41 (0)	MP 40 (0)	
R33h	r Control (4)	W	1	0	0	0	0	0	CP 12 (0)	CP 11 (0)	CP 10 (0)	0	0	0	0	0	CP 02 (0)	CP 01 (0)	CP00 (0)	
R34h	r Control (5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)	
R35h	r Control (6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)	
R36h	r Control (7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)	
R37h	r Control (8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)	
R3Ah	r Control (9)	W	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)					OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)	
R3Bh	r Control (10)	W	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)					ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)	

Table 6. 1 List Table of Register Set

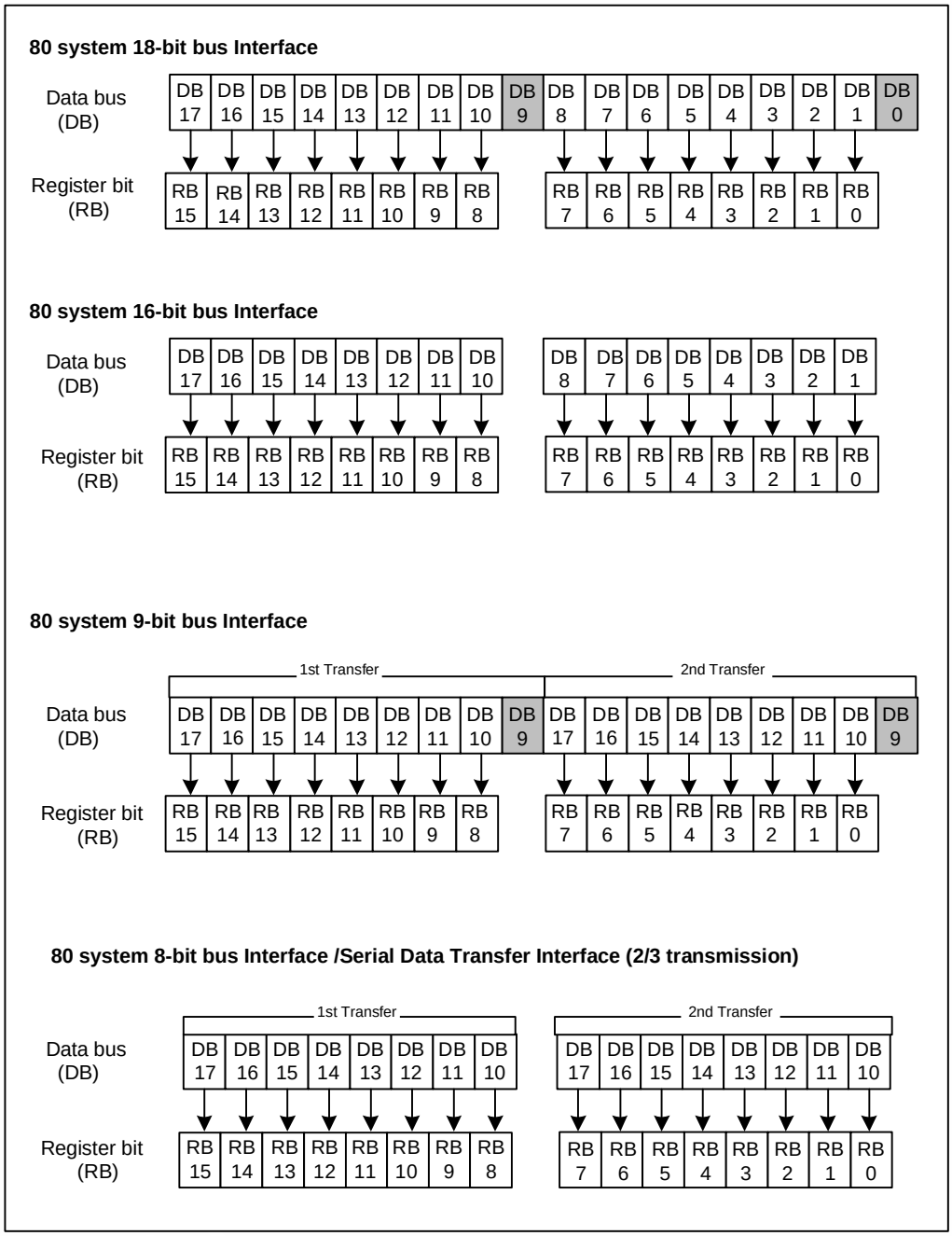


Figure 6. 1 80 System interface mode

6.1 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6. 2 Index Register

Index register (IR) specifies Index of the register from R00h to R4Fh. It sets the register number (ID6-0) in the range from 000000b to 1111111b in binary form.

6.2 Status Read Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 6. 3 Status Read Register

Status Read Register for reading the internal status of the HX8345-A.

L7–0: Indicate the position of driving line, where the liquid crystal display is driven at present.

6.3 Start Oscillation Register (R00h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSD_EN
R	1	1	0	0	0	0	0	1	1	0	1	0	0	0	1	0	1

Figure 6. 4 Start Oscillation Register (R00h)

OSD_EN: When OSD_EN = 1, oscillator is enabled; when OSD_EN = 0, oscillator is disabled. Start Oscillation Register restarts the oscillator from the suspend state at the standby mode. After setting this register, and wait at least 10 ms for oscillation stabilizing before setting the next register.

When the read commend is issued, 8345h is read.

6.4 Driver Output Control Register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 6. 5 Driver Output Control Register (R01h)

NL4–0: Specify the number of scan lines for the LCD driver can be adjusted by every 8 lines. Select the setting value for the panel size or higher.

NL4	NL3	NL2	NL1	NL0	Gate Driver Used	Number of Scan Line	Display Size
0	0	0	0	0	Ignore	Ignore	Ignore
0	0	0	0	1	G1~G16	16	384*16 dots
0	0	0	1	0	G1~G24	24	384 *24dots
0	0	0	1	1	G1~G32	32	384*32 dots
0	0	1	0	0	G1~G40	40	384*40 dots
0	0	1	0	1	G1~G48	48	384 *48dots
0	0	1	1	0	G1~G56	56	384*56 dots
0	0	1	1	1	G1~G64	64	384*64 dots
0	1	0	0	0	G1~G72	72	384*72 dots
:	:	:	:	:	:	:	:
1	0	0	0	0	G1~G136	136	384*136 dots
1	0	0	0	1	G1~G144	144	384*144 dots
1	0	0	1	0	G1~G152	152	384*152 dots
1	0	0	1	1	G1~G160	160	384*160 dots
:	:	:	:	:	:	:	:
1	1	1	1	1	G1~G160	160	384*160 dots

Table 6. 2 NL bits and Scan Line

SS: The source driver output shift direction selected. When SS=0, the shift direction from S1 to S384. When SS = 1, the shift direction from S384 to S1.

GS: Specify the shift direction of gate driver output. When GS = 0, the shift direction from G1 to G160. When GS = 1, the shift direction from G160 to G1.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

6.5 LCD Driving Waveform Control Register (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 6. 6 LCD-Driving-Waveform Control Register (R02h)

NW5–0: Specify the number of n lines that will alternate POL signal when B/C = 1. The inversion is occurred every n + 1 line, and the 1st to the 64th lines can be selected.

EOR: EOR=1 will force POL signal alternate at the beginning of a frame in n-line inversion driving mode (B/C=1), no matter the last interval of POL signal is over or not in last frame. Therefore, EOR bit is used when the POL signal is not completely alternated in some number of drive lines in LCD display area. For details, see the “N-line Inversion LCD Drive” section.

B/C: When B/C = 0, POL signal alternates in every frame for LCD drive. When B/C = 1, POL signal alternates in each n line specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the “N-line Inversion LCD Drive” section.

FLD1-0: Set the number of n field for interlaced driving mode. For details, see the "Interlaced driving function section".

FLD1	FLD0	Number of field
0	0	Ignore
0	1	1 field
1	0	Ignore
1	1	3 fields

Table 6. 3 FLD bits and interlaced field

6.6 Power control Register 1 (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	BT2	BT1	BT0	DC02	DC01	DC00	AP2	AP1	AP0	SLP	STB

Figure 6. 7 Power Control Register 1 (R03h)

STB: When STB = "1", the HX8345-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. Anyway, have not any external clock are supplied. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0")
b. Start the oscillation

Within the standby mode, the GRAM data and register content may be lost. For preventing this, they have to set again after the standby mode is exited.

SLP: When SLP = 1, the HX8345-A into the sleep mode, where the internal display operations are suspend except for the R-C oscillator, thus the current consumption can be reduced. Within the sleep mode, the GRAM data and register content cannot be accessed although they are retained.

AP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP2–0 = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	Ignore
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

Table 6. 4 AP Bits and amount of current in Operational Amplifier

BT2–0: Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced. The different setting values of VLCD, VGH and VGL is got as follow figure that connect with C22 or not.

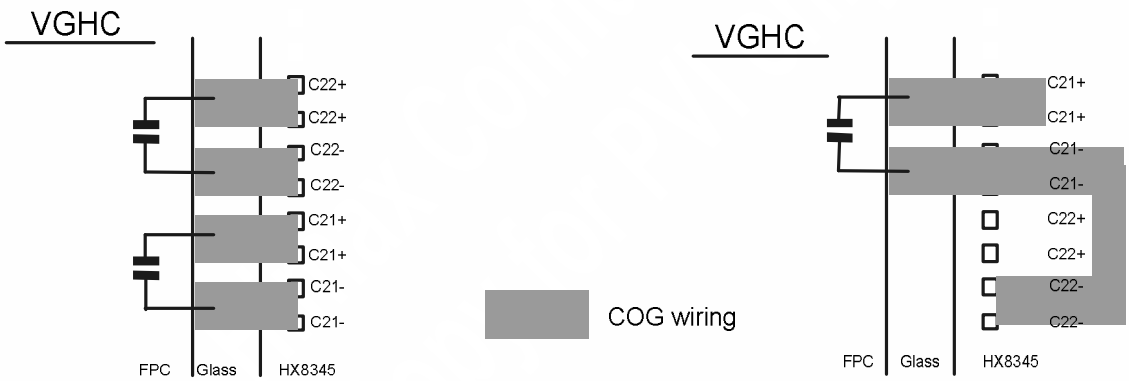


Figure 6. 8 Different Connection of C22 Capacitor

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x VCI1	-1 x VCI1	6 x VCI1	-5 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B, C22 A/B
0	0	1	2 x VCI1	-1 x VCI1	6 x VCI1	-4 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	0	2 x VCI1	-1 x VCI1	6 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
0	1	1	2 x VCI1	-1 x VCI1	5 x VCI1	-5 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	0	2 x VCI1	-1 x VCI1	5 x VCI1	-4 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	0	1	2 x VCI1	-1 x VCI1	5 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	0	2 x VCI1	-1 x VCI1	4x VCI1	-4x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	-	-	-	-	Setting Disable

Table 6. 5 BT Bits and VLCD, VGH and VGL Outputs

BT2	BT1	BT0	VLCD	VCL	VGH	VGL	Capacitor connection pins
0	0	0	2 x VCI1	-1 x VCI1	4 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12 A/B, C21 A/B,
0	0	1	2 x VCI1	-1 x VCI1	4 x VCI1	-2 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
0	1	0	2 x VCI1	-1 x VCI1	4 x VCI1	-1 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
0	1	1	2 x VCI1	-1 x VCI1	3 x VCI1	-3 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	0	0	2 x VCI1	-1 x VCI1	3 x VCI1	-2 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	0	1	2 x VCI1	-1 x VCI1	3 x VCI1	-1 x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B,
1	1	0	2 x VCI1	-1 x VCI1	2x VCI1	-2x VCI1	VLCD, VGH, VGL, VCL, C11A/B, C12A/B, C21A/B, C22A/B
1	1	1	-	-	-	-	Setting Disable

Table 6. 6 BT Bits and VLCD, VGH and VGL Outputs (without CapacitoC22)

Note: The factors of step-up for VGH are derived from VCI1 when VLCD and VCI2 are shorted. The conditions of VLCD ! 5.5V, VCL -3.3V, VGH ! 16.5V, and VGL -16.5V must be satisfied.

DC02–00: Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1
0	0	0	fosc / 4
0	0	1	fosc / 8
0	1	0	fosc / 16
0	1	1	fosc / 32
1	0	0	fosc / 64
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

Table 6. 7 Operation Frequency of Step-up Circuit 1 (fdcdc1)

6.7 Entry Mode Register (R05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0

Figure 6. 9 Entry Mode Register (R05h)

LG2-0: Logical operation of the GRAM read/write.

000: replacement
001: OR operation
010: AND operation
011: XOR operation
100: replacement with matched read
101: replacement with unmatched read
110: replacement with matched write
111: replacement with unmatched write

AM: The updating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D[1...0].

I/D1-0: The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the update method with I/D1-0 & AM bit.

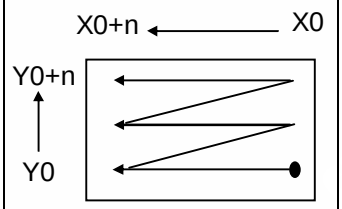
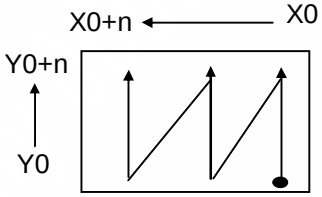
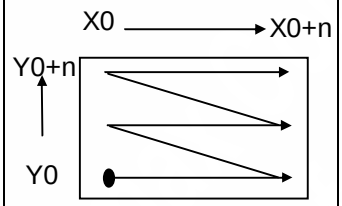
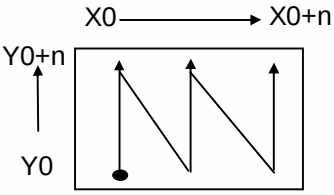
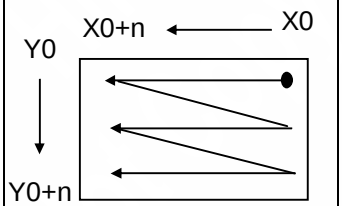
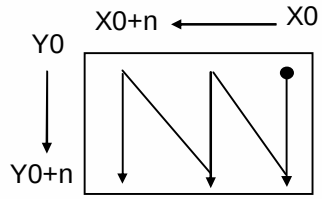
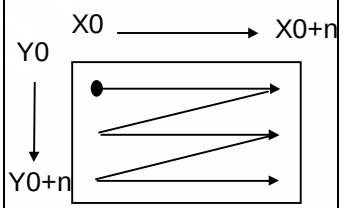
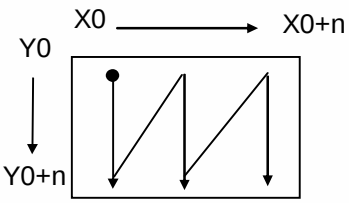
AM	I/D1	I/D0	Description Figure	AM	I/D1	I/D0	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure 6. 10 Address Direction Settings

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BGR: The order of <R><G><B> dot color. When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order. Setting BGR will change the bit order of (WM17-0) in the same way.

6.8 16-bit Compare Register (R06h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CP 15	CP 14	CP 13	CP 12	CP 11	CP 10	CP 9	CP 8	CP 7	CP 6	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

Figure 6. 11 16-bit Compare Register (R06h)

The write date sent from the microcomputer is modified in the HX8345A and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

CP15-0: Set the 16-bits compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

6.9 Display Control Register 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure 6. 12 Display Control Register 1 (R07h)

D1–0: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8345-A can control the charging current for the LCD with AC driving.

Control the display on/off while control GON and DTE. When D1–0 = 01, the internal display of the HX8345-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	Source Output	HX8345-A Internal Display Operations	Gate-Driver Control Signals (CPV, FLM, M) (CPV,STV,POL)
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	Non-lit display	Operate	Operate
1	1	Display	Operate	Operate

Table 6. 8 D Bits and Operation

Notes: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

REV: REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

REV	GRAM data	Source output level							
		Display area		Non-display area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 . . 18'h3FFFF	V63 . . V0	V0 . . V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 . . 18'h3FFFF	V0 . . V63	V63 . . V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z

Table 6. 9 Display Control Instruction

CL: CL = 1, the display mode is set to the 8-color display mode. For details, see the section on the 8-color display mode section.

CL	Number of Display Colors
0	262,144
1	8

Table 6. 10 CL Bit for 8-Color Display

Note: The display 262,144 colors when 18/9 bit bus interface is using, and display 65,536 colors when 16/8 bit bus interface is using.

DTE, GON: Specify the output level of gate line. VCOM level becomes VSSD when GON = 0.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Table 6. 11 GON and DTE bits

Note: GON bit is used in the gate driver. Control according to the bits values is executed by the gate driver. For details, see the data sheet of the gate driver.

SPT: When SPT = 1, the 2-division LCD drive is performed so a LCD can be divided 2 split display windows. For details, see the Partial Screen Display Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st display window. When VLE2 = 1, a vertical scroll is performed in the 2nd display window. Vertical scrolling on the two windows cannot be controlled at the same time.

VLE2	VLE1	1st Display Window	2nd Display Window
0	0	Fixed display	Fixed display
0	1	Scrolled display	Fixed display
1	0	Fixed display	Scrolled display
1	1	Ignore	Ignore

Table 6. 12 VLE Bits

PT1-0: When partial display is in use, these bits determine the source output in the non-display area. For details, see the Partial Screen Display Function section. The output on the source lines during the periods of the front and BP are also determined by PT1-0.

PT1	PT0	Source Output in Non-Display Area		Gate Output in Non-Display Area	VCOM output
		Positive Polarity	Negative Polarity		
0	0	V63	V0	Reference to PTG1-0	VCOMH VCOML
0	1	V63	.V0	Reference to PTG1-0	VCOMH VCOML
1	0	VSSD	VSSD	Reference to PTG1-0	VCOMH VCOML
1	1	Hi-Z	Hi-Z	Reference to PTG1-0	-

Table 6. 13 PT Bits for Source and Gate Output in Non-Display Area of Partial Display

Note: The output on the source lines during the periods of the front and BP and blanking of the partial display is determined by PT1-0.

6.10 Display Control Register 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSPL	HSPL	DPL	EPL	FP3	FP2	FP1	FP0	ISC3	ISC2	ISC1	ISC0	BP3	BP2	BP1	BP0

Figure 6. 13 Display Control Register 2 (R08h)

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to PD17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to PD17-0

Table 6. 14 EPL bit and Enable pin

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

ISC3-0: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

Table 6. 15 ISC bit setting

BP3-0: Specify the amount of scan line for back porch(BP).
FP3-0: Specify the amount of scan line for front porch (FP).

The setting vale, ensure that:
BP + FP " 16 lines
PB ! 2 lines
FP ! 2 lines

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by he display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

FP3	FP2	FP1	FP0	Number of FP Line	Number of BP Line
BP3	BP2	BP1	BP0		
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	3 lines	
0	1	0	0	4 lines	
0	1	0	1	5 lines	
0	1	1	0	6 lines	
0	1	1	1	7 lines	
1	0	0	0	8 lines	
1	0	0	1	9 lines	
1	0	1	0	10 lines	
1	0	1	1	11 lines	
1	1	0	0	12 lines	
1	1	0	1	13 lines	
1	1	1	0	14 lines	
1	1	1	1	Ignore	

Table 6. 16 BP/FP bits

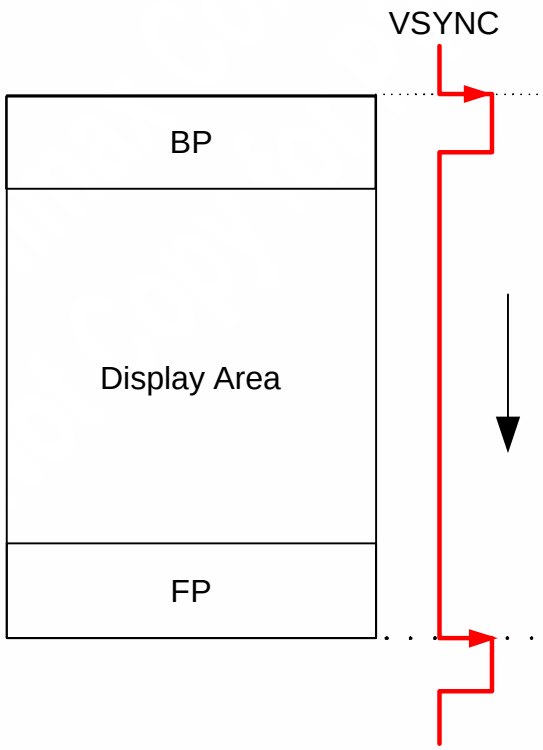


Figure 6. 14 BP/FP

Note: The output signal is delay 2 lines timing from the VSYNC to the LCD

Operation Mode	Number of Interlace Scan Field	BP	FP	BP + FP
System Interface	FLD1-0 = 01	≥2 lines	≥2 lines	≤ 16 lines
	FLD1-0 = 11	3 lines	5 lines	-
RGB Interface	-	≥2 lines	≥2 lines	≤ 16 lines
VSYNC Interface	-	≥2 lines	≥2 lines	16 lines

Table 6. 17 BP3-0, FP3-0 setting dependent on the operation mode

6.11 Power control Register 2 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	DCM 1	DCM 0	DC12	DC11	DC10	0	DK	SAP2	SAP1	SAP0

Figure 6. 15 Power Control Register 2 (R09h)

SAP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP2–0 = 000, the current consumption can be reduced by stopping the operational amplifier.

SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	Stop
0	0	1	Setting Disable
0	1	0	0.62
0	1	1	0.71
1	0	0	1
1	0	1	1.25
1	1	0	1.43
1	1	1	Setting Disable

Table 6. 18 SAP Bits and amount of current in Operational Amplifier

DK: ON/OFF the operation of step-up circuit 1. When power on, the VLCD no output until VGHC is set up completely. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

Table 6. 19 SAP Bits and amount of current in Operational Amplifier

DC12–10: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

fosc = R-C oscillation frequency

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2
0	0	0	fosc / 8
0	0	1	fosc / 16
0	1	0	fosc / 32
0	1	1	fosc / 64
1	0	0	fosc / 128
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	Halted

Table 6. 20 Operation Frequency of Step-up Circuit 2 (fdcdc2)

Note: Ensure that the operation frequency of step-up circuit 1" step-up circuit 2

DCM1-0: Set the set-up frequency in a blank period during 8-color mode (CL=”1”).

DCM1	DCM0	Step-up frequency
0	0	Ignore
0	1	1/2 x fdcdc1,2
1	0	1/4 x fdcdc1,2
1	1	1/8 x fdcdc1,2

Table 6. 21 Step-up frequency setting

6.12 External Display Interface Control Register 1 (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM1	DFM0	0	0	PTG1	PTG0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

Figure 6. 16 External Display Interface Control Register 1 (R0Ah)

RIM1- 0: Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode(1 transfer/pixel)
0	1	16-bit bus RGB interface Mode(1 transfer/pixel)
1	0	6-bit bus RGB interface Mode(3 transfers/pixel)
1	1	Ignore

Table 6. 22 RIM bit for the Transfer Mode of RGB interface

DM1-0: Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 6. 23 DM bit for the Operation Mode of LCD display

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	System interface / VSYNC interface
1	RGB interface

Table 6. 24 RM bit for the access interface of GRAM

Note: the register is set only through the system interface.
Note: A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

PTG1-0: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

Table 6. 25 PTG bit setting

TRI: When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus Interface. When TRI=0, 8-bit bus interface mode is unselected.

DFM1-0: Specify the data format when TRI=1, for 8-bit bus interface or serial data transfer interface. DFM1-0=10, 262K color mode. DFM1-0=11, 65K color mode.

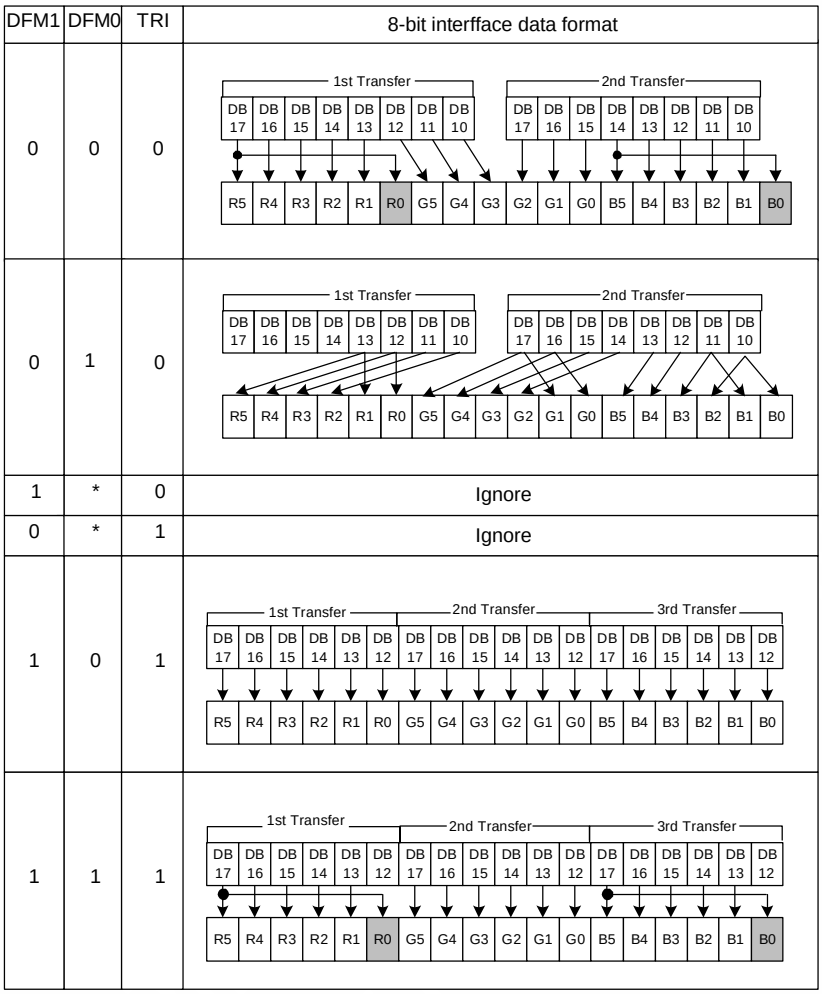


Figure 6. 17 The setting of DFM and TRI (1)

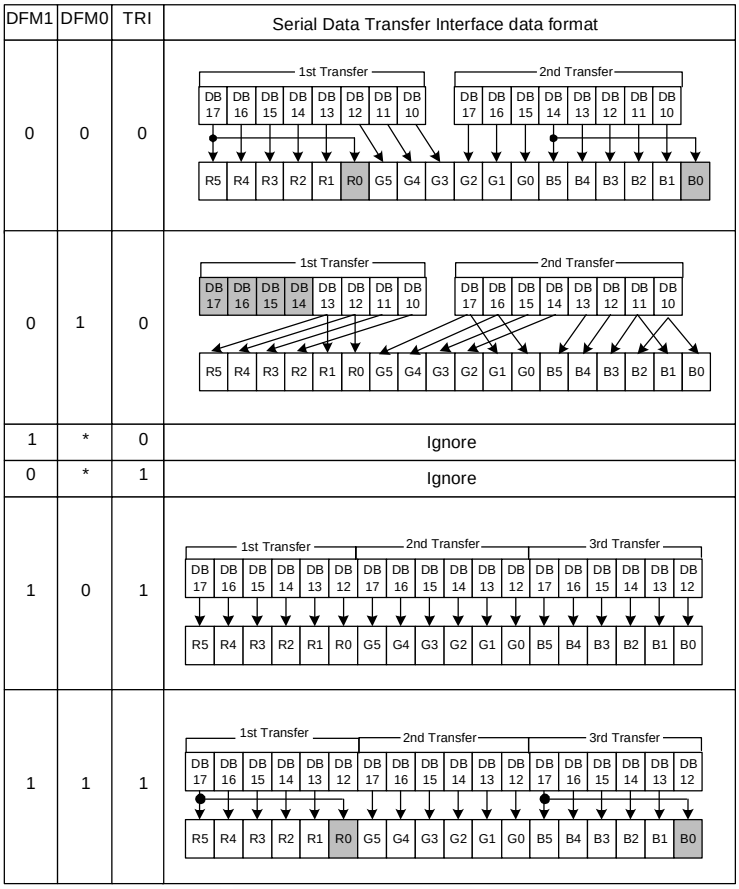


Figure 6. 18 The setting of DFM and TRI (2)

6.13 Frame Cycle Control Register (R0Bh)

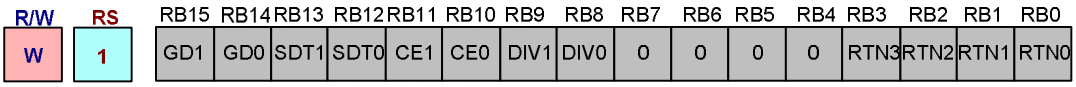


Figure 6. 19 Frame Cycle Control Register (R0Bh)

RTN3-0: Set the 1-line period in a clock unit.

Clock cycles=1/internal operation clock frequency

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Line
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
:	:	:	:	:
1	1	0	1	29
1	1	1	0	30
1	1	1	1	31

Table 6. 26 RTN Bits and Clock Cycles

DIV1-0: The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Table 6. 27 DIV Bits and Clock Frequency

Formula for the Frame Frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{(\text{RTN}*8+16)\ \$\ \text{DIV}\ \$\ (\text{NL}+\text{BP}+\text{FP})}\ [\text{Hz}]$$

fosc: RC oscillation frequency
RTN bit: Clocks per line
DIV bit: Division ratio
NL: The number of lines
FP: Number of lines for front porch
BP: Number of lines for back porch
BP+FP% 16

CE1-0: CE period can be set with CE1-0.

CE1	CE 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	Not CE	Not CE
0	1	1 clock cycle	8 clock cycles
1	0	2 clock cycles	16 clock cycles
1	1	3 clock cycles	24 clock cycles

Table 6. 28 CE Bits for Equalized Period

SDT1-0: Set delay amount from falling edge of the gate output signal for the source outputs.

SDT1	SDT0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (clock: DOTCLK)
0	0	1 clock cycle	8 clock cycles
0	1	2 clock cycles	16 clock cycles
1	0	3 clock cycles	24 clock cycles
1	1	4 clock cycles	32 clock cycles

Table 6. 29 SDT Bits for Source Output Delay

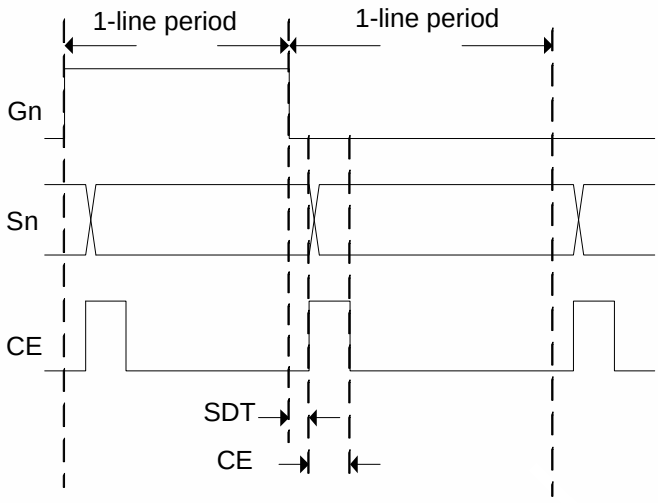


Figure 6. 20 Equalized Period and Source Output Delay

GD1-0: Set amount of non-overlap for the gate output.

GD 1	GD 0	System Interface Operation (source clock: R-C Oscillator)	RGB Interface Operation (source clock: DOTCLK)
0	0	0 clock cycle	0 clock cycle
0	1	4 clock cycles	32 clock cycles
1	0	6 clock cycles	48 clock cycles
1	1	8 clock cycles	64 clock cycles

Table 6. 30 GD Bits for Non-overlap Time between Two Adjacent Gate Output Pulse

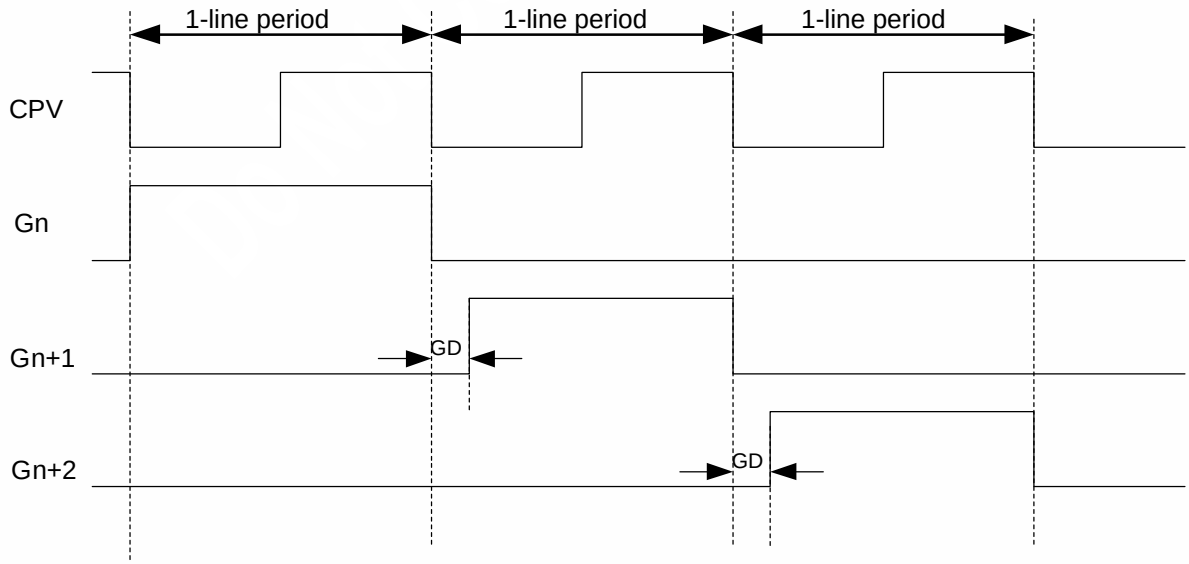


Figure 6. 21 Non-overlap Time between Two Adjacent Gate Output Pulse

Interface mode	Clock Source
System interface mode	R-C oscillator
RGB interface more	DOTCLK
VSYNC interface mode	R-C oscillator

Table 6. 31 Clock Source for Interface Mode

6.14 Power Control Register 3 (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 6. 22 Power Control Register 2 (R0Ch)

VC2-0: Set the reference voltage of VREG1OUT and VCI1 by adjusting the rate of VCI.

VC2	VC1	VC0	Internal reference voltage (REGP) of VGM1OUT and VCI1
0	0	0	VCI
0	0	1	0.92 x VCI
0	1	0	0.87 x VCI
0	1	1	0.83 x VCI
1	0	0	0.76 x VCI
1	0	1	0.73 x VCI
1	1	0	Hi-z
1	1	1	Hi-z

Table 6. 32 VC Settings and Internal Reference Voltage

6.15 Power Control Register 4 (R0Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

Figure 6. 23 Power Control Register 3 (R0Dh)

VRH3-0: Set the magnification of amplification for VREG1OUT voltage. (VCOM, reference voltage for grayscale voltage) It allows magnify the amplification of REGP from 1.38 to 1.83 times.

VRH3	VRH2	VRH1	VRH0	VREG1OUT Voltage
0	0	0	0	REGP x 1.33 times
0	0	0	1	REGP x 1.45 times
0	0	1	0	REGP x 1.55 times
0	0	1	1	REGP x 1.65 times
0	1	0	0	REGP x 1.75 times
0	1	0	1	REGP x 1.80 times
0	1	1	0	REGP x 1.85 times
0	1	1	1	Stopped
1	0	0	0	REGP x 1.900 times
1	0	0	1	REGP x 2.175 times
1	0	1	0	REGP x 2.325 times
1	0	1	1	REGP x 2.475 times
1	1	0	0	REGP x 2.625 times
1	1	0	1	REGP x 2.700 times
1	1	1	0	REGP x 2.775 times
1	1	1	1	Stopped

Table 6. 33 VRH Bits and VREG1OUT Voltage

Notes: Adjust VC2-0 and VRH3-0 so that the VREG1OUT voltage is lower than 5.0 V.
Note: Set the VC and VRH bits so that VREG1OUT is less than (VLCD-0.5)V

PON: ON/OFF the operation of step-up circuit 3. PON = 0 is to stop and PON = 1 to start operation.

6.16 Power Control Register 5 (0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 6. 24 Power Control Register 4 (R0Eh)

VCM4-0: Set the VCOMH voltage (voltage of higher side when VCOM is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VREG1OUT voltage. When VCM4-0 = “11111”, stop the internal volume adjustment and adjust the VCOMH with external resistance from VCOMR.

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VREG1OUT x 0.40
0	0	0	0	1	VREG1OUT x 0.42
0	0	0	1	0	VREG1OUT x 0.44
:	:	:	:	:	:
0	1	1	1	0	VREG1OUT x 0.68
0	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister),
1	0	0	0	0	VREG1OUT x 0.70
1	0	0	0	1	VREG1OUT x 0.72
1	0	0	1	0	VREG1OUT x 0.74
:	:	:	:	:	:
1	1	1	0	0	VREG1OUT x 0.94
1	1	1	0	1	VREG1OUT x 0.96
1	1	1	1	0	VREG1OUT x 0.98
1	1	1	1	1	Stop the internal volume. VCOMH can be adjusted from VCOMR with a external VR (variable resister),

Table 6. 34 VCM4-0 Bits and VCOMH Voltage

Notes: Adjust VREG1OUT and VCM4-0 so that the VCOMH voltage is lower than VREG1OUT.

VDV4-0: Sets the amplification factors for VCOM and Vgoff while VCOM AC drive is being performed. It is possible to setup from 0.6 to 1.23 times of VREG1OUT. When VCOMG = 0, the setup is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VREG1OUT x 0.60
0	0	0	0	1	VREG1OUT x 0.63
0	0	0	1	0	VREG1OUT x 0.66
0	0	0	1	1	VREG1OUT x 0.69
:	:	:	:	:	:
0	1	1	0	0	VREG1OUT x 0.96
0	1	1	0	1	VREG1OUT x 0.99
0	1	1	1	0	VREG1OUT x 1.02
0	1	1	1	1	Inhibition
1	0	0	0	0	VREG1OUT x 1.05
1	0	0	0	1	VREG1OUT x 1.08
1	0	0	1	0	VREG1OUT x 1.11
1	0	0	1	1	VREG1OUT x 1.14
1	0	1	0	0	VREG1OUT x 1.17
1	0	1	0	1	VREG1OUT x 1.20
1	0	1	1	0	VREG1OUT x 1.23
1	0	1	1	1	Inhibition
1	1	-	-	-	

Table 6. 35 VDV4-0 Bits and VCOM Amplitude

Notes: Adjust VREG1OUT and VDV4-0 so that the VCOM and Vgoff amplitudes are lower than 6.0V.

VCOMG: When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ -VCI +0.5V). When VCOMG = 0, VCOML voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, when VCOMG = 0, setting of the VDV4-0 is invalid. In this case, adjustment of VCOM/Vgoff A/C amplitude must be adjusted with VCOMH using VCM4-0.

6.17 Gate Scan Position Register (R0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

Figure 6. 25 Gate Scan Position Register (R0Fh)

SCN4-0: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G160	G1	G160
0	0	0	0	1	G9	G152	G17	G144
0	0	0	1	0	G17	G144	G33	G128
0	0	0	1	1	G25	G136	G49	G112
0	0	1	0	0	G33	G128	G65	G96
0	0	1	0	1	G41	G120	G81	G80
0	0	1	1	0	G49	G112	G97	G64
0	0	1	1	1	G57	G104	G113	G48
0	1	0	0	0	G65	G96	G129	G32
0	1	0	0	1	G73	G88	G145	G16
0	1	0	1	0	G81	G80	G2	G159
0	1	0	1	1	G89	G72	G18	G143
0	1	1	0	0	G97	G64	G34	G127
0	1	1	0	1	G105	G56	G50	G111
0	1	1	1	0	G113	G48	G66	G95
0	1	1	1	1	G121	G40	G82	G79
1	0	0	0	0	G129	G32	G98	G63
1	0	0	0	1	G137	G24	G114	G47
1	0	0	1	0	G145	G16	G130	G31
1	0	0	1	1	G153	G8	G146	G15

Table 6. 36 SCN bits and Scanning Start Position for Gate Driver

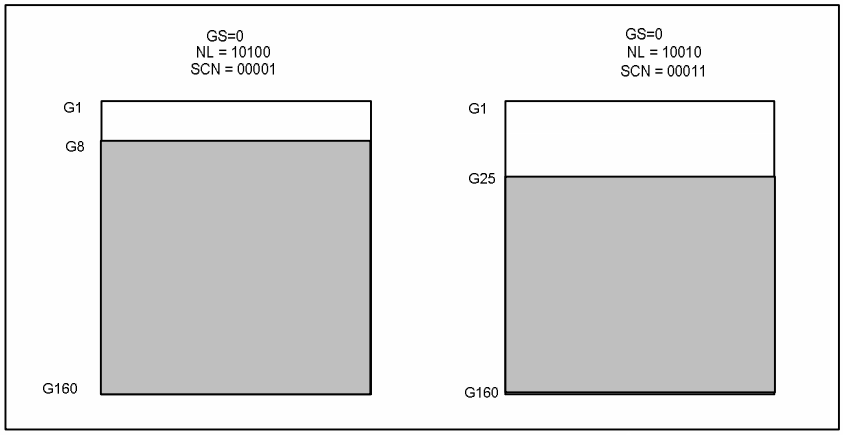


Figure 6. 26 SCN bits and Scanning Start Position for Gate Driver

Note: Don't set NL, SCN over the end position of gate line (G160)
Note: Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 160.

6.18 CP/WM 18/16-bit Selection Register (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F

Figure 6. 27 CP/WM 18/16-bit Selection Register (R10h)

F: Set the CP/WM to 18/16-bit mode.

F	CP/WM
0	Set the CP/WM to 16 bit mode
1	Set the CP/WM to 18 bit mode

Table 6. 37 F bit

6.19 Vertical Scroll Control Register (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 6. 28 Vertical Scroll Control Register (R11h)

VL7–0: Specify the amount of scrolling line from 0 to 160 in the display to enable smooth vertical scrolling. If GRAM address mapping would exceed “9Fxx”H, GRAM address mapping would restart from “00xx”H after the data in “9Fxx”H of GRAM being displayed. The display-start line (VL7–0) is valid only when VLE1 = 1 or VLE2 = 1. The display-start line is fixed to zero when VLE2-1 = 00. (VLE1 is the 1st display window vertical-scroll enable bit, and VLE2 is the 2nd display window vertical-scroll enable bit.)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Length
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
:	:	:	:	:		:	:	:
1	0	0	1	1	1	0	1	157 lines
1	0	0	1	1	1	1	0	158 lines
1	0	0	1	1	1	1	1	159 lines

Table 6. 38 VL bits and scrolling Length

6.20 First Display Window Driving Position Register (R14h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	SS 17	SS 16	SS 15	SS 14	SS 13	SS 12	SS 11	SS 10

Figure 6. 29 First Screen Driving Position Register (R14h)

SS17–0: Specify the driving start position for the first display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver.

SE17–0: Specify the driving end position for the first display window in a line unit. The LCD driving is performed to the 'setting value + 1' gate driver. See the Partial-Screen Display Function section for details.

6.21 Second Display Window Driving Position Register (R15h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	SS 27	SS 26	SS 25	SS 24	SS 23	SS 22	SS 21	SS 20

Figure 6. 30 Second Screen Driving Position Register (R15h)

SS27–0: Specify the driving start position for the second display window in a line unit. The LCD driving starts from the 'setting value + 1' scan line of gate driver. The second display window is driven when SPT = 1.

SE27–0: Specify the driving end position for the second display window in a line unit. The LCD driving is performed to the ' setting value + 1' gate driver.

Note: Ensure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤9Fh. For details, see the Partial Screen Display Function section.

6.22 Horizontal RAM Address Position Register (R16h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HAE 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0

Figure 6. 31 Horizontal RAM Address Position Register (R44h)

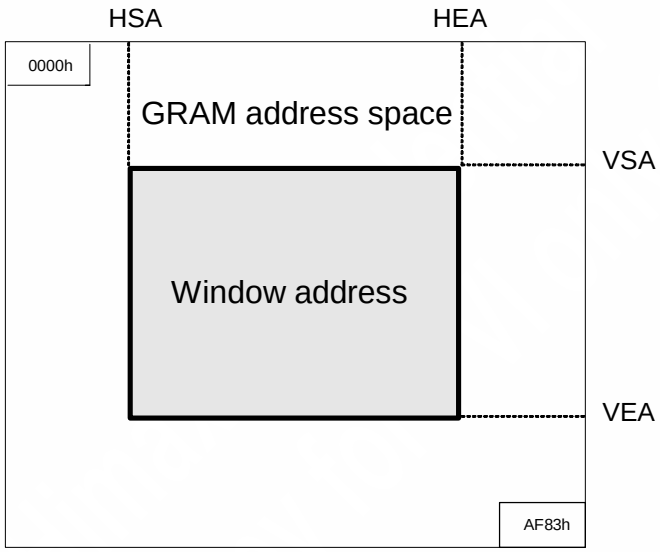
HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA7-0.Ensure that “00”h ≤HSA7-0 ≤HEA7-0 ≤”7F”h.

6.23 Vertical RAM Address Position Register (R17h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 6. 32 Vertical RAM Address Position Register (R45h)

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA7-0 to the address specified by VEA7-0. Ensure that “00”h ≤VSA7-0 ≤VEA7-0 ≤”9F”h



Window address setting range
“00”h ≤HSA7-0 ≤HEA7-0 ≤”7F”h
“00”h ≤VSA7-0 ≤VEA7-0 ≤”9F”h

Figure 6. 33 Window Address Setting Range

Note1. The window address range must be within the GRAM address space.
Note2. Data are written to GRAM in four-words when operating in high speed mode so dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

6.24 16-bit RAM Write Data Mask Register (R20h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure 6. 34 16-bit RAM Write Data Mask Register (R20h)

WM15–0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. The GRAM cannot be accessed in standby mode. When 16-/8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

6.25 RAM Address Register (R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 6. 35 RAM Address Register (R21h)

AD15–0: Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

AD15-AD0	GRAM Setting
“0000” h – “007F” h	Bitmap data for G1
“0100” h – “017F” h	Bitmap data for G2
“0200” h – “027F” h	Bitmap data for G3
:	:
“9D00” h – “9D7F” h	Bitmap data for G158
“9E00” h – “9E7F” h	Bitmap data for G159
“9F00” h – “9F7F” h	Bitmap data for G160

Table 6. 39 GRAM address mapping

6.26 Write Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
		PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
RGB-I/F mode:		WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 6. 36 Write Data Register (R22h)

WD17–0: Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

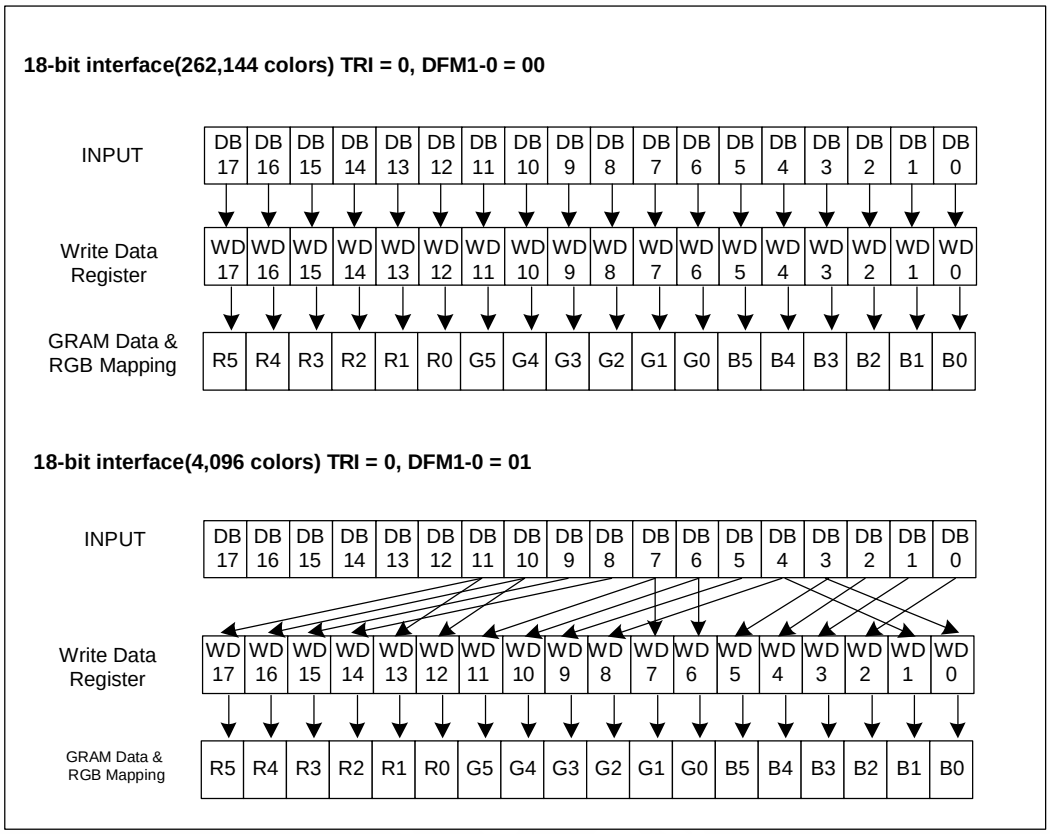


Figure 6. 37 Bit Mapping of One Pixel Data: Input Data (18-bit Interface) Written to GRAM through Write Data Register

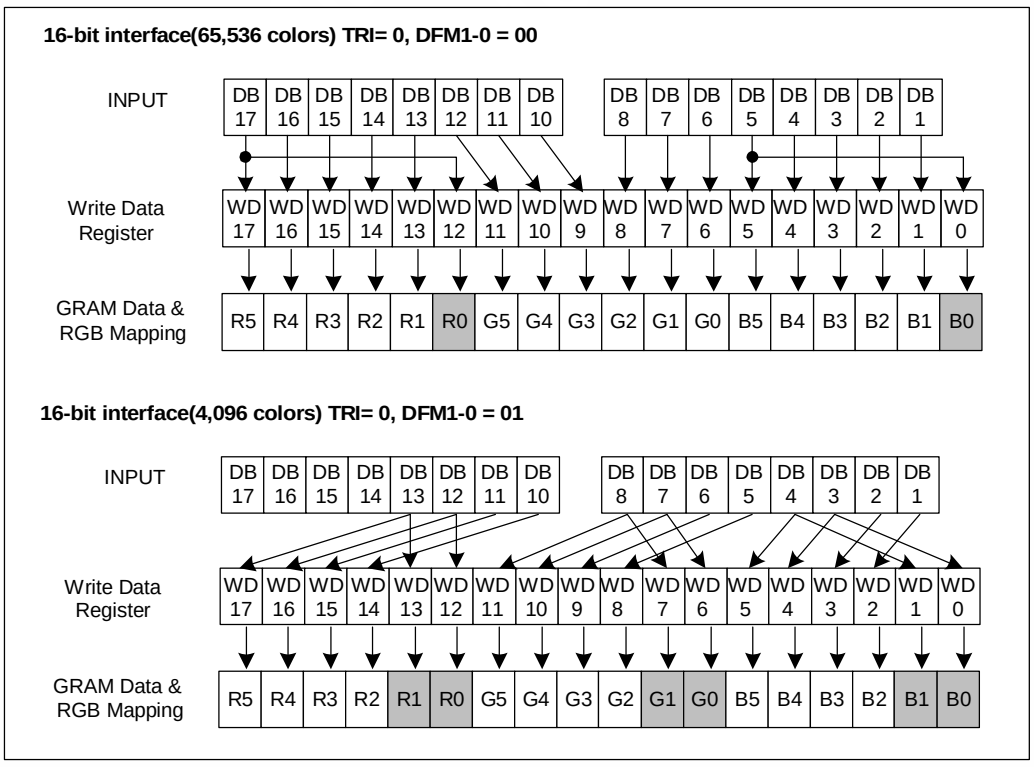


Figure 6. 38 Bit Mapping of One Pixel Data: Input Data (16-bit Interface) Written to GRAM through Write Data Register

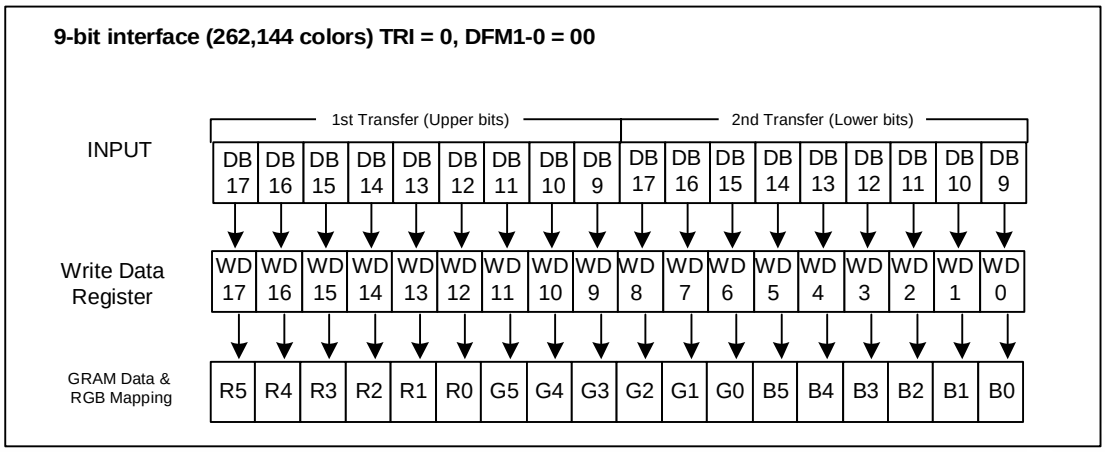


Figure 6. 39 Bit Mapping of One Pixel Data: Input Data (9-bit Interface) Written to GRAM through Write Data Register

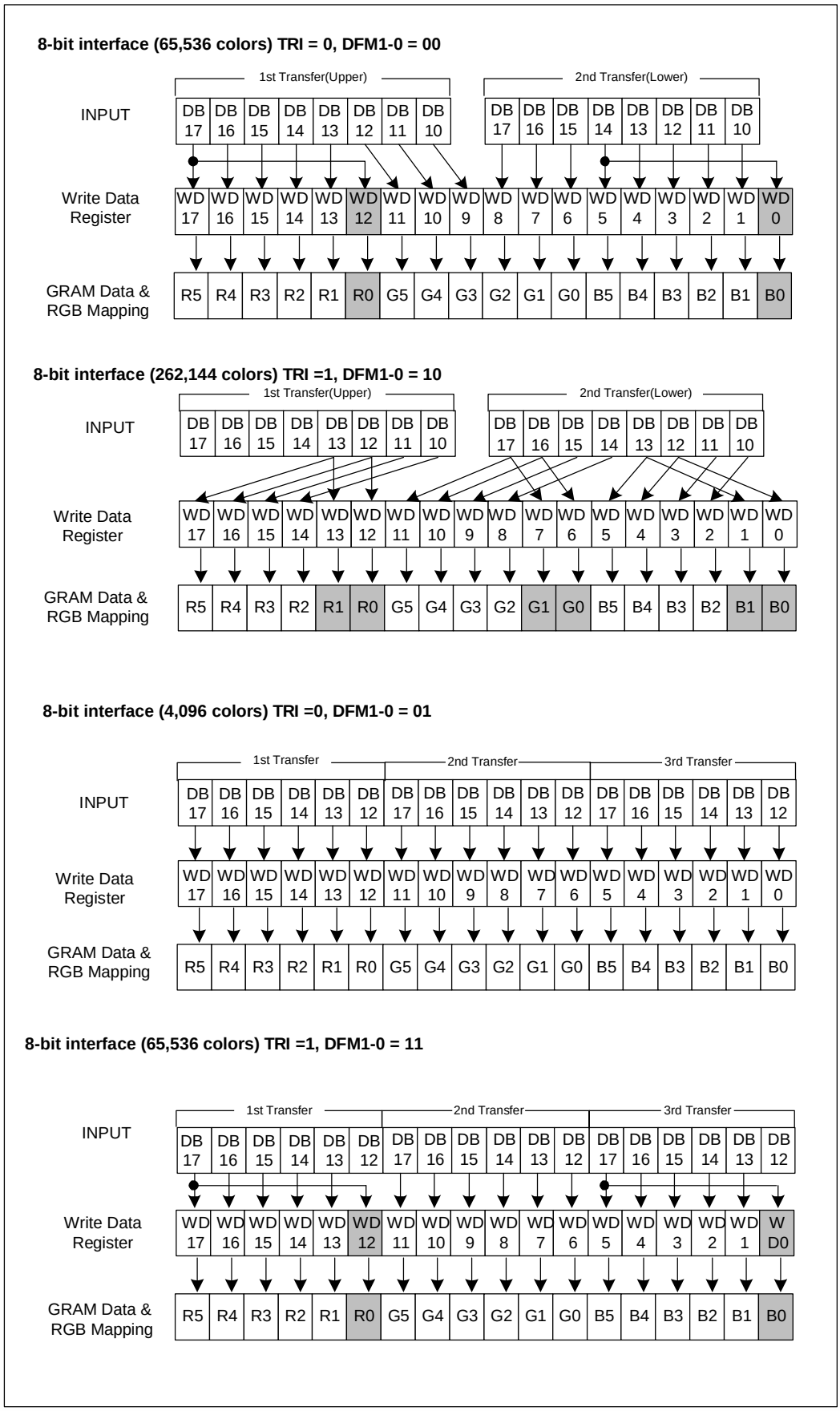


Figure 6. 40 Bit Mapping of One Pixel Data: Input Data (8-bit Interface) Written to GRAM through Write Data Register

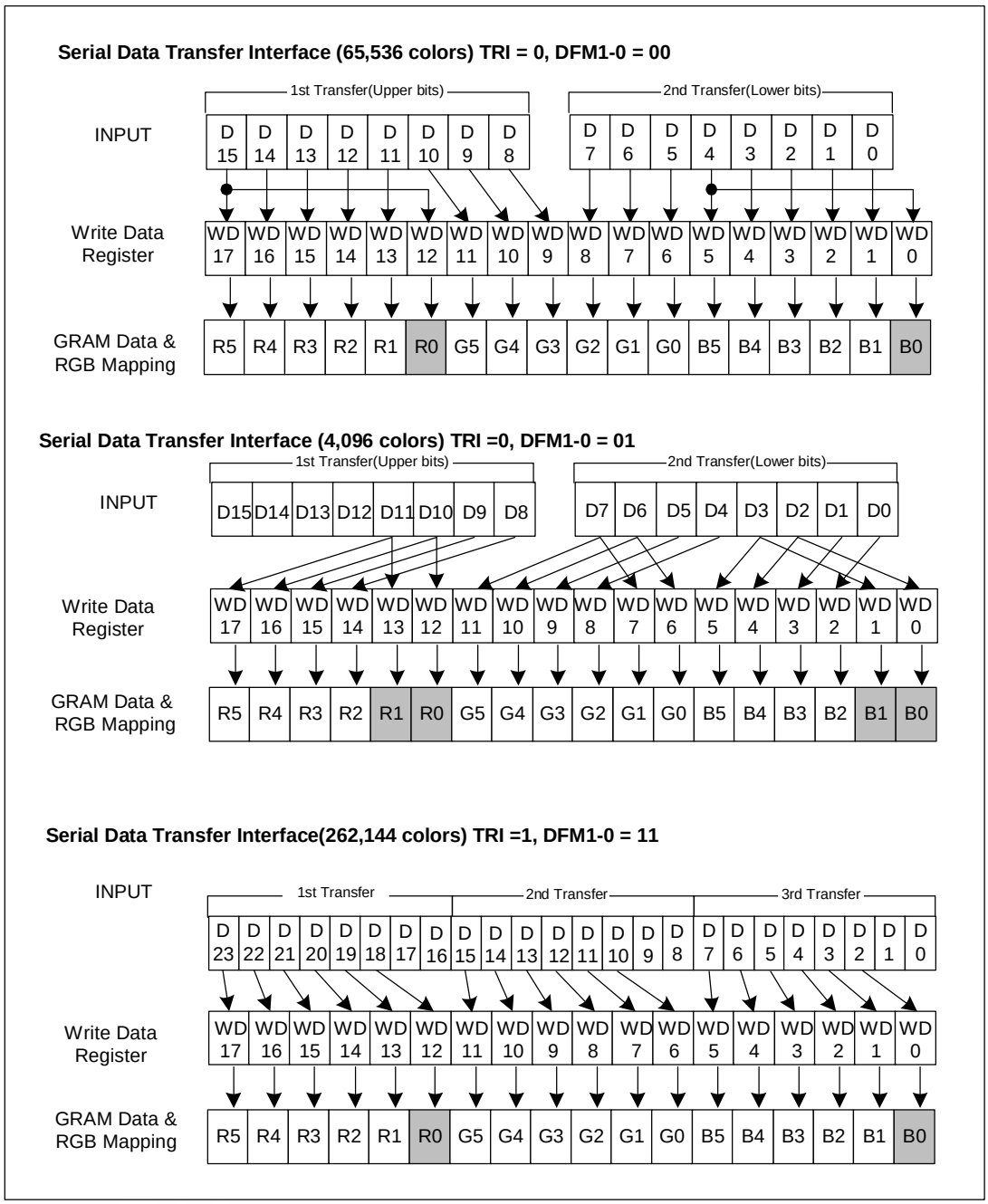
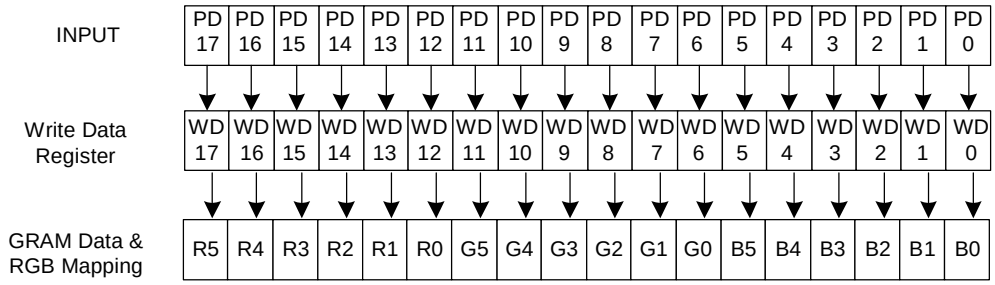


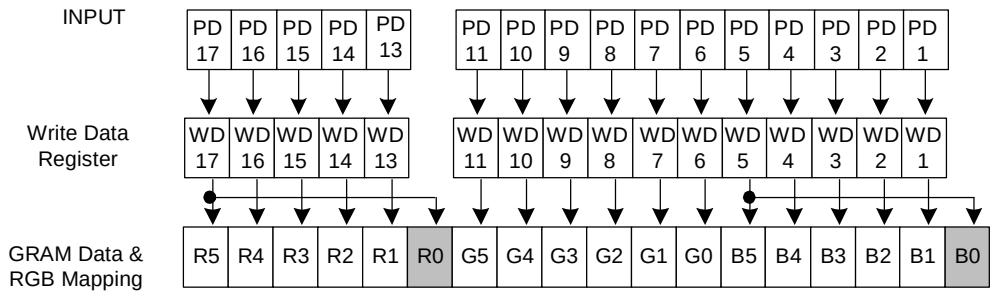
Figure 6. 41 Bit Mapping of One Pixel Data: Input Data (Serial Data Transfer interface) Written to GRAM through Write Data Register

18-bit RGB interface (262,144 colors)



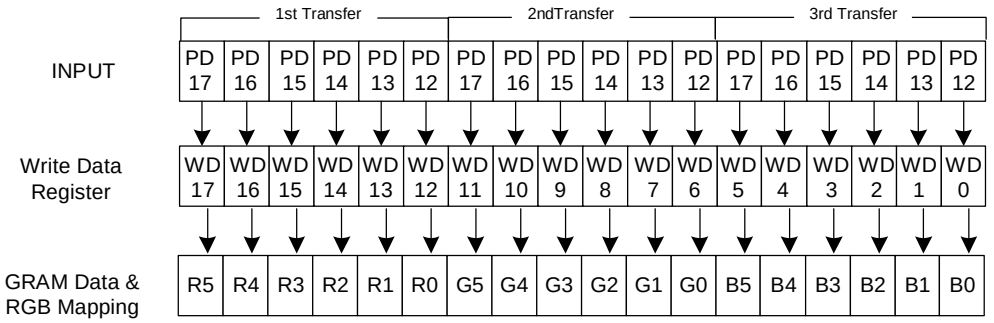
Set the index register when writing data through an RGB interface.

16-bit RGB interface (65,563 colors)



Set the index register when writing data through an RGB interface.

6-bit RGB interface (262,144 colors)



Set the index register when writing data through an RGB interface.

Figure 6. 42 Bit Mapping of One Pixel Data: Input Data (18/16/6-bit RGB Interface) Written to GRAM through Write Data Register

6.27 Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 6. 43 Read Data Register (R22h)

RD17–0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

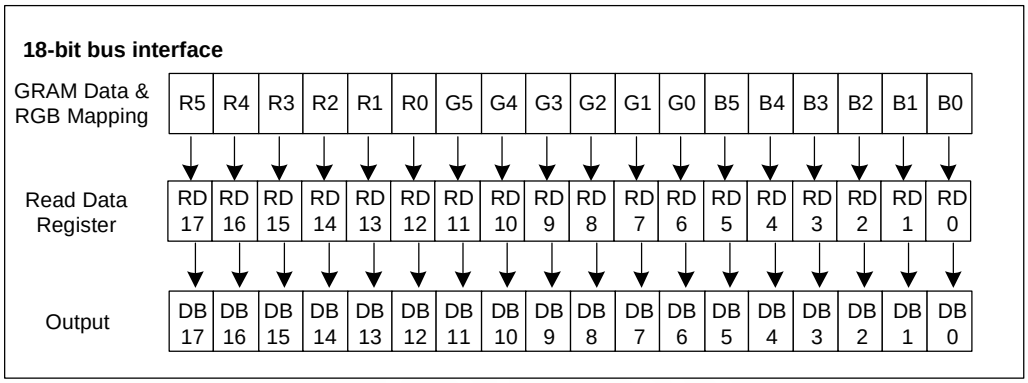


Figure 6. 44 Output Data Read from GRAM through Read Data Register in 18-bit Interface Mode

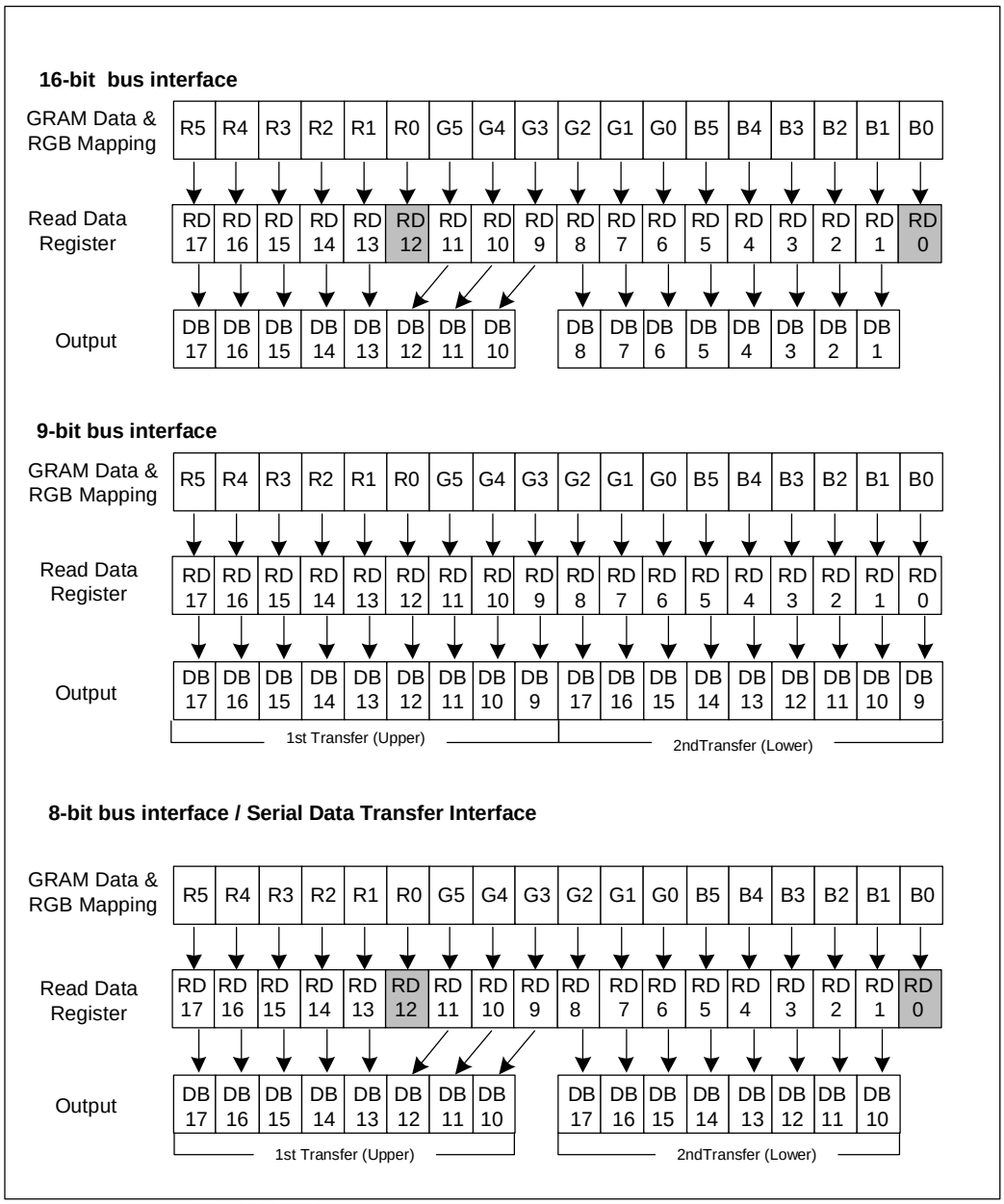


Figure 6. 45 Output Data Read from GRAM through Read Data Register in 16- /9- /8-bit Interface Mode

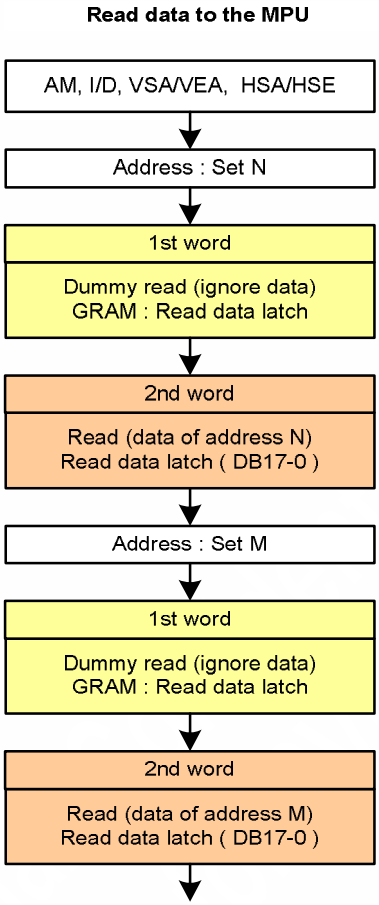


Figure 6. 46 Flow Chart of GRAM Read Data

6.28 18-bit RAM Write Data Mask Register 1 (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	0	0	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure 6. 47 18-bit RAM Write Data Mask Register 1 (R23h)

6.29 18-bit RAM Write Data Mask Register 2 (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	WM 17	WM 16	WM 15	WM 14	WM 13	WM 12

Figure 6. 48 18-bit RAM Write Data Mask Register 2 (R24h)

WM17–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM17 = 1, this bit mask the write data of RB17 and does not write to the GRAM. Similarly, the WM16~WM0 bit masks the write data of RB16~RB0 in a bit unit. For details, see the Graphics Operation Function section.

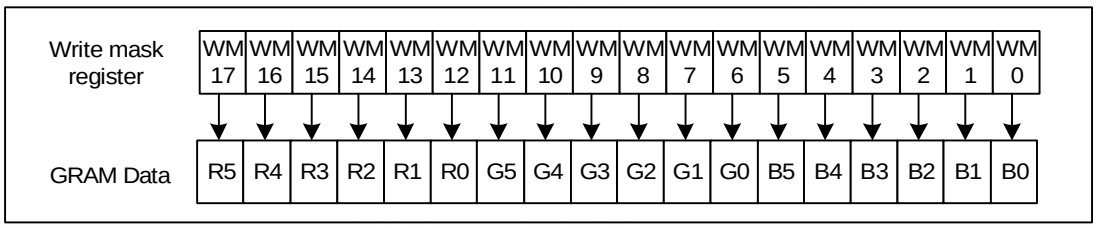


Figure 6. 49 GRAM Write Data Mask

Note: Please set R10h to 0001h, when WM17~0 in using.

6.30 18-bit Compare Register 1 (R25h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	CP 11	CP 10	CP 9	CP 8	CP 7	CP 6	0	0	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

Figure 6. 50 18-bit Compare Register 1(R25h)

6.31 18-bit Compare Register 2 (R26h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	CP 17	CP 16	CP 15	CP 14	CP 13	CP 12

Figure 6. 51 18-bit Compare Register 2 (R26h)

CP17–0: Set the 18-bits compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

Note: Please set R10h to 0001h, when CP17~0 in using.

6.32 Gamma Control Register Set

Gamma Control Register 1~10 (R30h~R3Bh)

	R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R30	W	1	0	0	0	0	0	MP1 (2)	MP1 (1)	MP1 (0)	0	0	0	0	0	MP0 (2)	MP0 (1)	MP0 (0)
R31	W	1	0	0	0	0	0	MP3 (2)	MP3 (1)	MP3 (0)	0	0	0	0	0	MP2 (2)	MP2 (1)	MP2 (0)
R32	W	1	0	0	0	0	0	MP5 (2)	MP3 (1)	MP5 (0)	0	0	0	0	0	MP4 (2)	MP4 (1)	MP4 (0)
R33	W	1	0	0	0	0	0	CP1 (2)	CP1 (1)	CP1 (0)	0	0	0	0	0	CP0 (2)	CP0 (1)	CP0 (0)
R34	W	1	0	0	0	0	0	MN1 (2)	MN1 (1)	MN1 (0)	0	0	0	0	0	MN0 (2)	MN0 (1)	MN0 (0)
R35	W	1	0	0	0	0	0	MN3 (2)	MN3 (1)	MN3 (0)	0	0	0	0	0	MN2 (2)	MN2 (1)	MN2 (0)
R36	W	1	0	0	0	0	0	MN5 (2)	MN5 (1)	MN5 (0)	0	0	0	0	0	MN4 (2)	MN4 (1)	MN4 (0)
R37	W	1	0	0	0	0	0	CN1 (2)	CN1 (1)	CN1 (0)	0	0	0	0	0	CN0 (2)	CN0 (1)	CN0 (0)
R3A	W	1	0	0	0	OP1 (4)	OP1 (3)	OP1 (2)	OP1 (1)	OP1 (0)	0	0	0	0	OP0 (3)	OP0 (2)	OP0 (1)	OP0 (0)
R3B	W	1	0	0	0	ON1 (4)	ON1 (3)	ON1 (2)	ON1 (1)	ON1 (0)	0	0	0	0	ON0 (3)	ON0 (2)	ON0 (1)	ON0 (0)

MP5-0 (2:0): Gamma adjustment registers for positive polarity output
CP1-0 (2:0): Gamma gradient adjustment registers for positive polarity output
MN5-0 (2:0): Gamma adjustment registers for negative polarity output
CN1-0 (2:0: Gamma gradient adjustment register for negative polarity output
OP0 (3:0)/OP1 (4:0): Amplification adjustment resistor for positive polarity output
ON0 (3:0)/ON1 (4:0): Amplification average adjustment resistor for negative polarity output

Figure 6. 52 Gamma Control Register 1~10 (R30h~R3Bh)

6.33 Initialization

Output Pin Initialization

1. Driver output pins (Source outputs): Output VSSD level
2. Driver output pins (Gate outputs): Output VGH level
3. Oscillator output pin (OSC2): Output oscillation signal

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10011, SS = 0, GS = 0, SM = 0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Power control 1 (BT2-0 = 000, DC02-10 = 000, AP2–0 = 000: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. Entry mode set (BGR = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move)
6. Display control 1 (PT1-0 = 00, VLE2-1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL =0: 262144-color mode, REV = 0, D1–0 = 00: Display off)
7. Display control 2 (VSPL = 0, HSPL = 0, DPL = 0, EPL = 0, FP3-0 = 0011, ISC3-0 = 0000, BP3-0 = 0101)
8. Power control 2 (DCM1-0 = 00, DC12-10 = 000, DK = 0, SAP2–0 = 100)
9. External display interface control 1 (TRI = 0, DFM1-0 = 00, PTG1-0 = 00, RM = 0: System interface, DM1-0 = 00: internal clock operation, RIM1-0 = 00: 18-bit RGB interface)
10. Frame cycle control (GD1-0 = 00, SDT1-0 = 00, CE1-0 = 00: No equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clocks in 1-line period)
11. Power control 3 (VC2-0 = 000)
12. Power control 4 (PON=0,VRH3-0 = 0000)
13. Power control 5 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
14. Gate scan starting position (SCN4-0 = 00000)
15. Vertical scroll (VL7–0 = 00000000)
16. 1st screen division (SE17-10 = 10011111, SS17-10 = 00000000)
17. 2nd screen division (SE27-20 = 10011111, SS27-20 = 00000000)
18. Horizontal RAM address position (HEA7-0 = 01111111, HSA7-0 = 00000000)
19. Vertical RAM address position (VEA7-0 = 10011111, VSA7-0 = 00000000)
20. RAM write data mask (WM15–0 = 0000000000000000h: No mask)
21. RAM address set (AD15–0 = 0000h)
22. RAM write data mask (WM17–0 = 00000000000000000h: No mask)
23. Gamma control
    (MP02-00 = 000, MP12-10 = 000, MP22-20 = 000, MP32-30 = 000, MP42-40 = 000, MP52-50 = 000, CP02-00 = 000, CP12-10 = 000)
    (MN02-00 = 000, MN12-10 = 000, MN22-20 = 000, MN32-30 = 000, MN42-40 = 000, MN52-50 = 000, CN02-00 = 000, CN12-10 = 000)
    (OP03-00 =0000, OP14-10=00000, ON03-00=0000, ON14-10=0000)

6.34 Reset Function

The HX8345-A is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from the MPU can be accepted. The reset input must be held for at least 1 ms. do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

GRAM Data Initialization:

It must be initialized by software while display is off (D1-0=00)

7. Power Generation

7.1 Specification

The specification of power supply circuit and pins connection are shown as following table:

Pins connection	Recommended voltage	Capacity
TVCOMHI, TVCOMLI, TVMAG	6V	0.1 µF (B characteristics)
VDDD, VCIOUT, VCLC, VCOMH, VCOML, C12A/B	6V	1 µF (B characteristics)
VLCD, C21A/B, C22A/B VREG1OUT, C11A/B,	10V	1 µF (B characteristics)
VGHC, VGLC	25V	1 µF (B characteristics)

Table 7. 1 The adoptability of Capacitor

Pins connection	Feature
VSSD – VGL (VCI – VGH)	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

Table 7. 2 The adoptability of Schottky diode

Pins to connect	Resistance
VCOMR	> 200 kΩ

Table 7. 3 The adoptability of Variable resistor

7.2 Power supply Circuit

The power supply circuit of HA8345-A preside over generating supply voltages to drive a LCD panel.

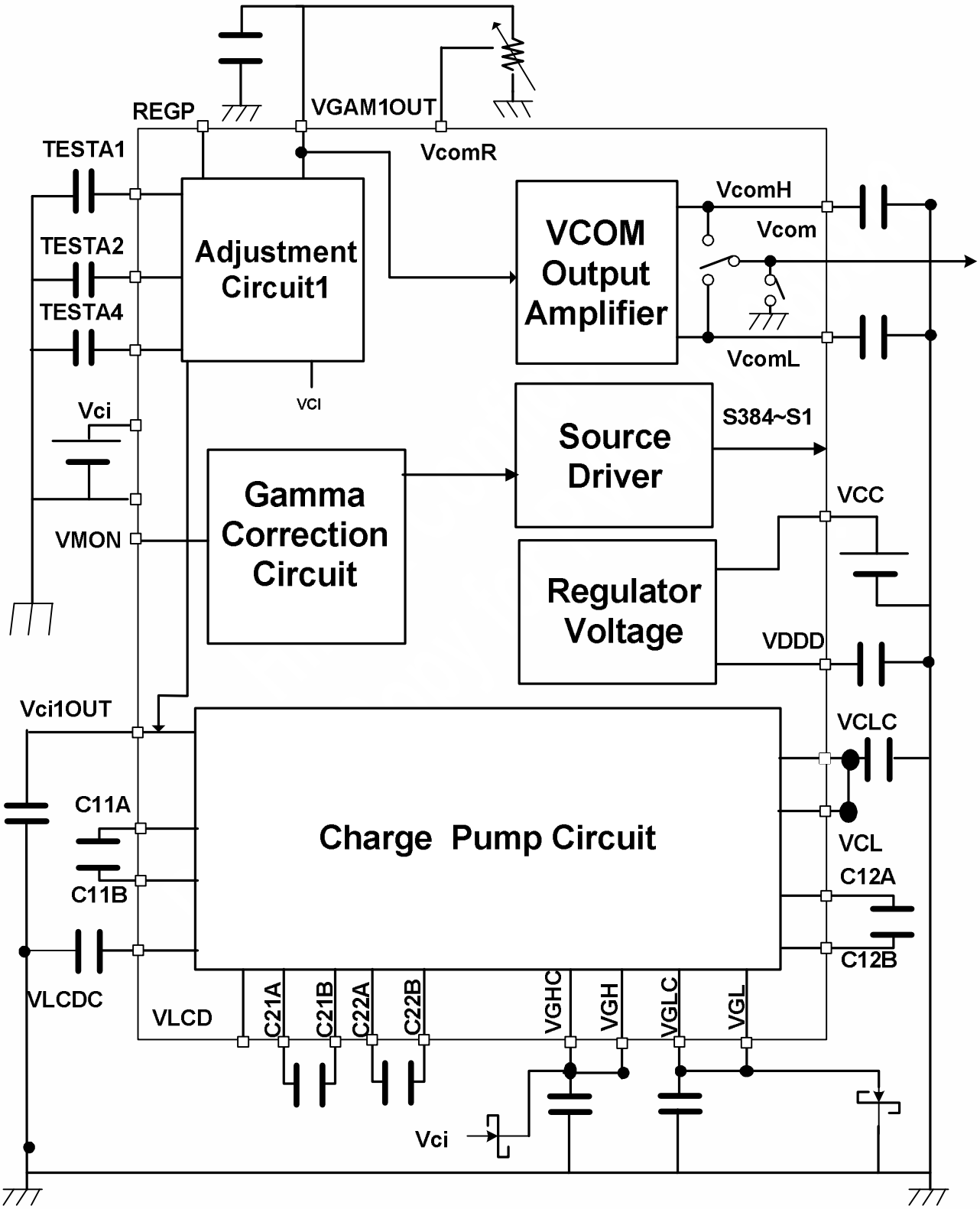


Figure 7. 1 Block Diagram of Power Supply Circuit

7.3 Voltage Setting

The voltage setting pattern diagram of the HX8345-A illustrates as following figure. The outputs of VLCDC, VGH, VGL and VCL are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption. When the VCOM voltage alternating cycle is high, the large current will be consumed.

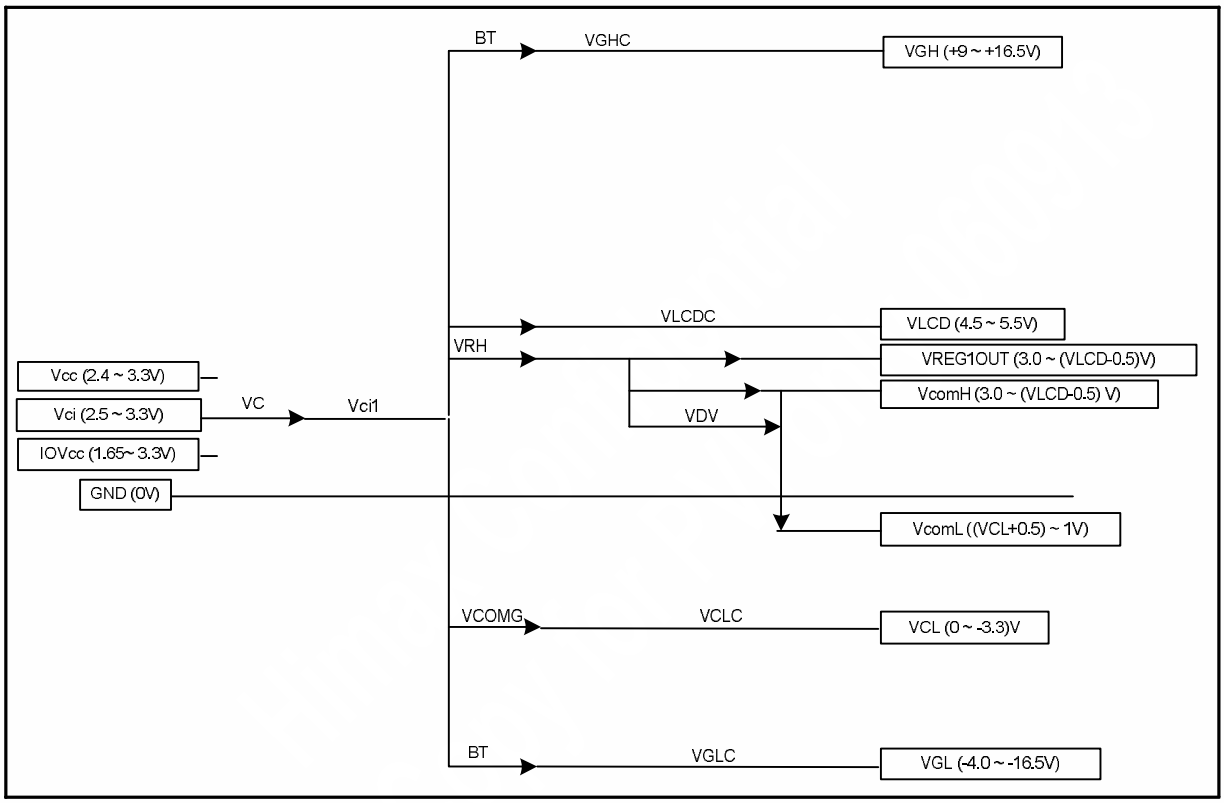


Figure 7. 2 Voltage setting diagram

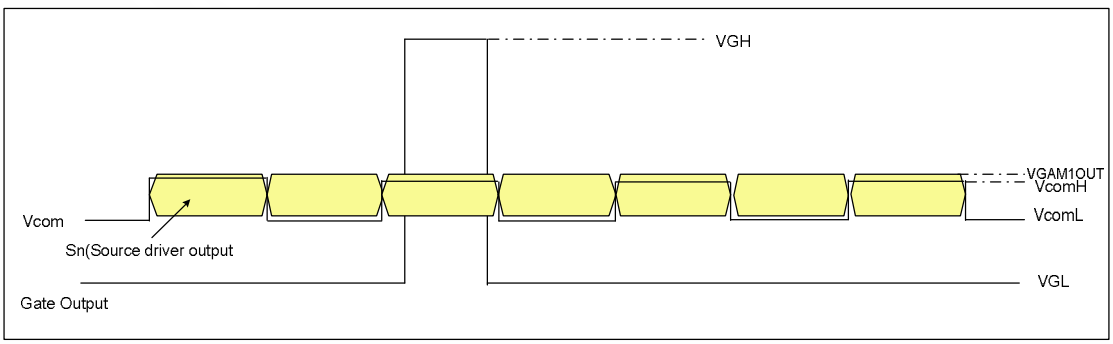


Figure 7. 3 The applied voltage of the TFT display

7.4 Register Setting

The following are the sequences of register setting flow that applied to the HA8345-A driving the TFT display.

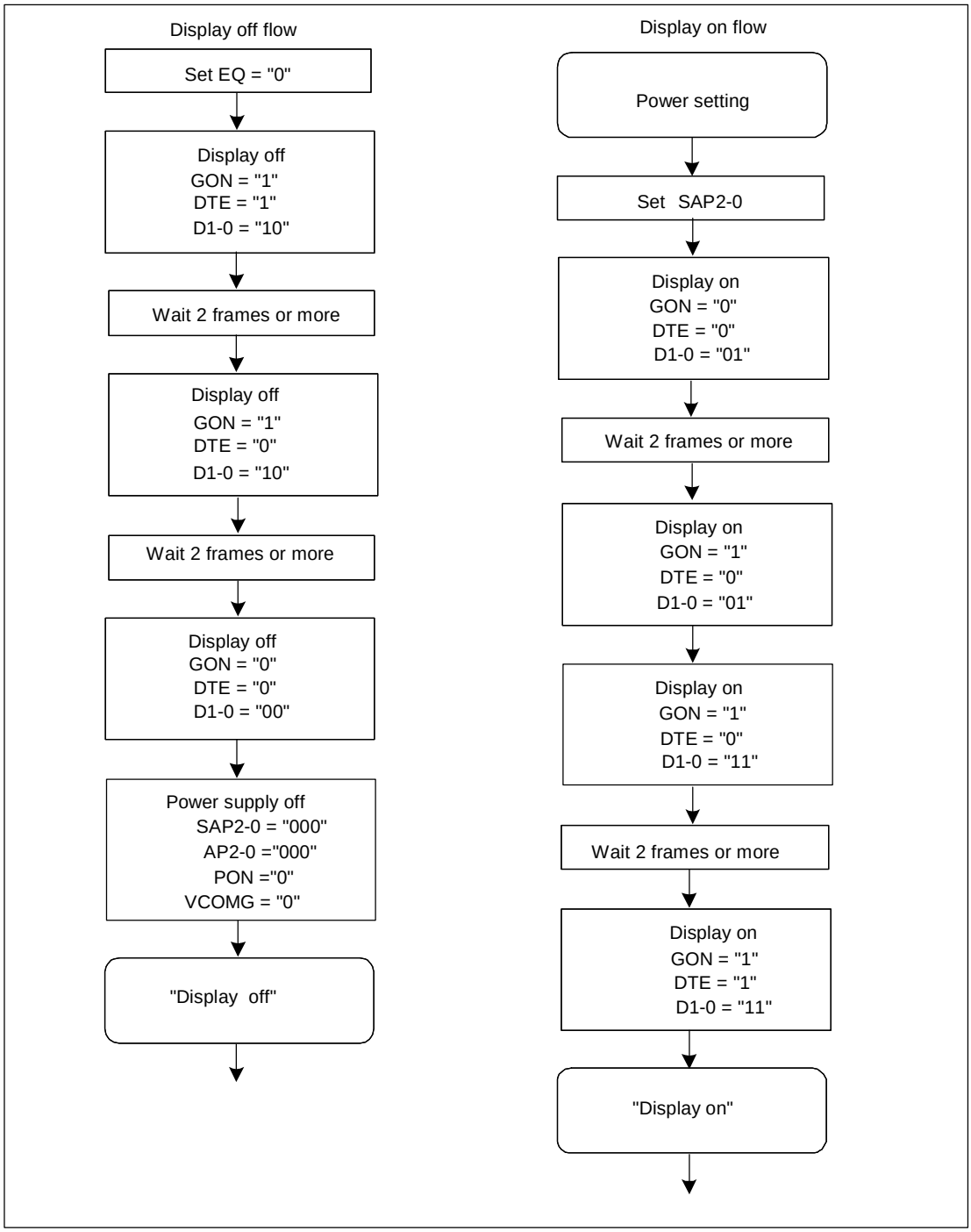


Figure 7. 4 Register setting sequence

Standby mode and Sleep Mode setting flow:

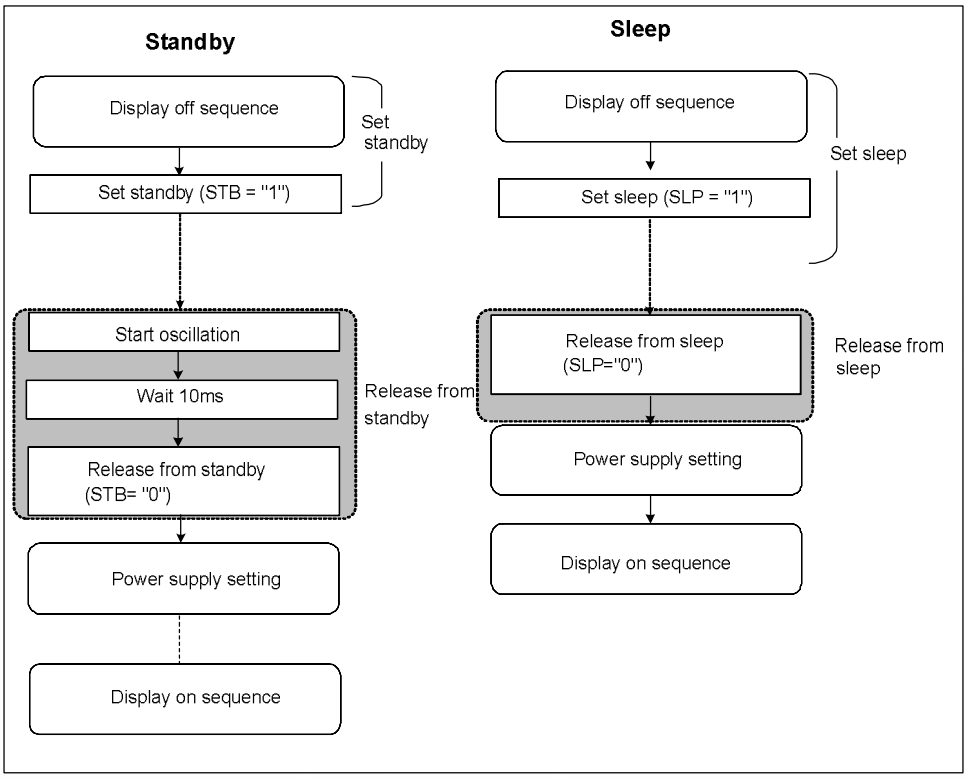


Figure 7. 5 Standby Mode and Sleep Mode Setting Sequence

7.5 Power Supply Setting

The power supply setting sequence of the HX8345-A is as below.

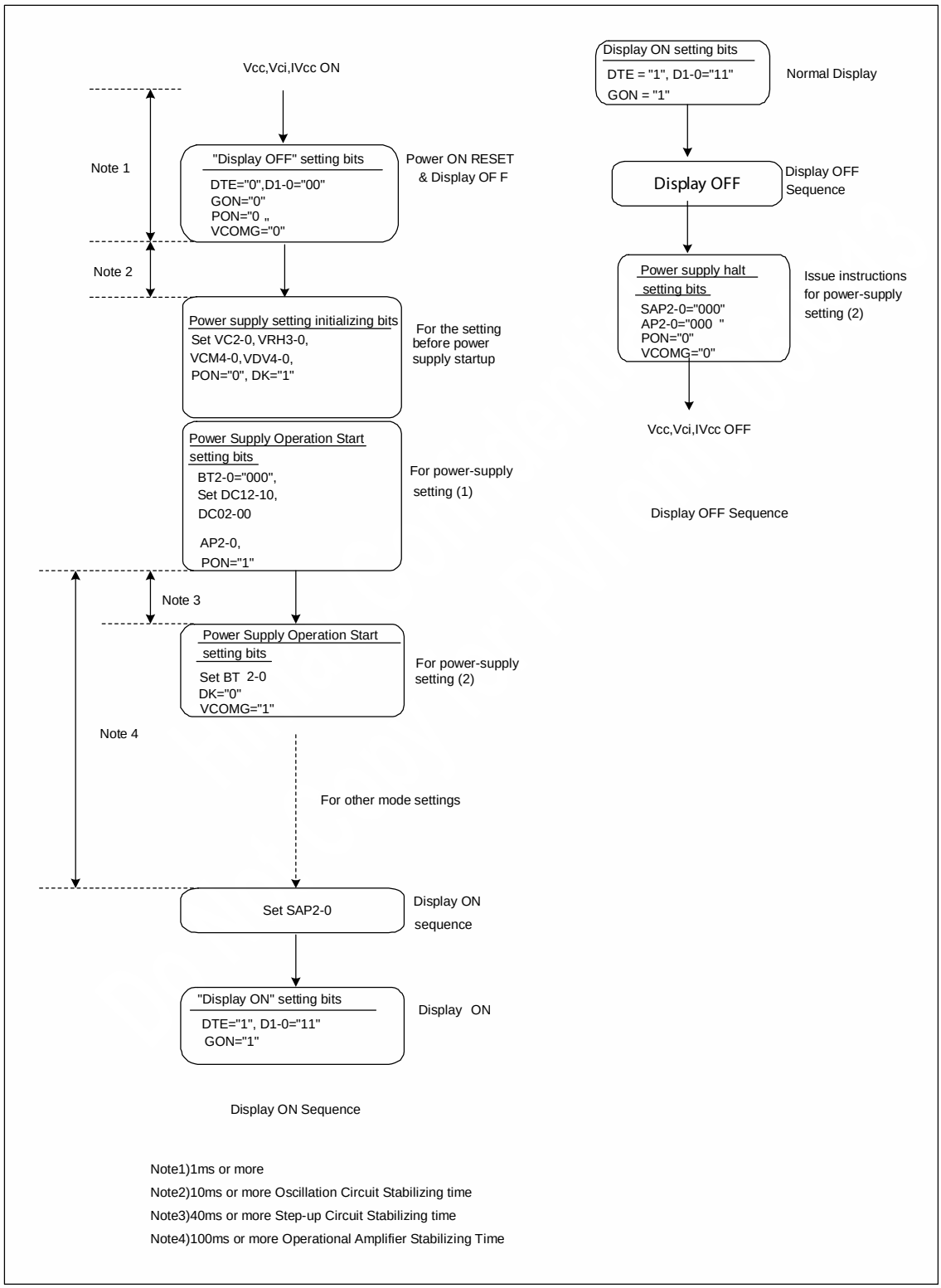


Figure 7. 6 Power Supply Setting Flow

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage 1	VCC, IOVCC	V	-0.3 ~ + 4.6	Note(1),(2)
Power supply voltage 2	VCI - VSSA	V	-0.3 ~ + 4.6	Note(1),(3)
Power supply voltage 3	VLCD - VSSA	V	-0.3 ~ + 6.0	Note(1),(4)
Power supply voltage 4	VSSA -VCL	V	-0.3 ~ + 4.6	Note(1),(5)
Power supply voltage 5	VLCD - VCL	V	-0.3 ~ + 9.0	Note(1),(6)
Power supply voltage 6	VGH - VSSA	V	-0.3 ~ + 18.5	Note(1),(7)
Power supply voltage 7	VSSA - VGL	V	-0.3 ~ + 16.5	Note(1),(8)
Input voltage	Vt	V	-0.3 ~ VCC + 0.3	Note(1)
Operating temperature	Topr	&C	-40 ~ + 85	Note(9),(10)
Storage temperature	Tstg	&C	-55 ~ + 110	Note(9),(10)

Notes:
(1) VCC, VSSD must be maintained
(2) (High) VCC ≥ VSSD (Low), (High) IOVCC ≥ VSSD (Low).
(3) Make sure (High) VCI ≥ VSSA (Low).
(4) Make sure (High) VLCD ≥ VSSA (Low).
(5) Make sure (High) VSSA ≥VCL (Low)
(6) Make sure (High) VLCD ≥ VCL (Low).
(7) Make sure (High) VGH ≥ VSSA (Low).
(8) Make sure (High) VSSA ≥ VGL (Low).
(9) For die and wafer products, specified up to 85# .

10. This temperature specifications apply to the COG package.

Table 8. 1 Absolute Maximum Rating

8.2 AC Characteristic

AC Characteristics (IOVCC = 1.65 ~ 3.3V, VCC = 2.4 ~ 3.3V, Ta = -40 ~ 85 °C)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	f_{cp}	KHz	100	176	600	IOVCC=1.65 ~ 3.3V, VCC= 2.4 ~ 3.3V
External clock duty ratio	Duty	%	45	50	55	IOVCC=1.65 ~ 3.3V, VCC= 2.4 ~ 3.3V
External clock rise time	trcp	µs	-	-	0.2	IOVCC=1.65 ~ 3.3V, VCC= 2.4 ~ 3.3V
External clock fall time	tfcp	µs	-	-	0.2	IOVCC=1.65 ~ 3.3V, VCC= 2.4 ~ 3.3V
R-C oscillation clock	f_{OSC}	KHz	TBD	TBD	TBD	Rf = 200K ohm , VCC=3V

Table 8. 2 Clock Characteristics (IOVCC = 1.65 ~ 3.3V, VCC = 2.4 ~ 3.3V)

80/68-system Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	200	-	-	Figure 8.1
	Read	t_{CYCR}	ns	500	-	-	Figure 8.1
Write low-level pulse width		PW_{LW}	ns	50	-	-	Figure 8.1
Read low-level pulse width		PW_{LR}	ns	200	-	-	Figure 8.1
Write high-level pulse width		PW_{HW}	ns	100	-	-	Figure 8.1
Read high-level pulse width		PW_{HR}	ns	200	-	-	Figure 8.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.1
Setup time	Write (RS to NCS, E_NWR)	t_{AS}	ns	10	-	-	Figure 8.1
	Read (RS to NCS , RW_NRD)			10	-	-	Figure 8.1
Address hold time		t_{AH}	ns	5		-	Figure 8.1
Write data set up time		t_{DSW}	ns	60		-	Figure 8.1
Write data hold time		t_{H}	ns	15		-	Figure 8.1
Read data delay time		t_{DDR}	ns	-	-	200	Figure 8.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.1

Table 8. 3 80-System Normal Write Mode / (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCEW}	ns	200	-	-	Figure 8.2
	Read	t_{CYCER}	ns	500	-	-	Figure 8.2
Write low-level pulse width		PWE_{LW}	ns	50	-	-	Figure 8.2
Read low-level pulse width		PWE_{LR}	ns	200	-	-	Figure 8.2
Write high-level pulse width		PWE_{HW}	ns	100	-	-	Figure 8.2
Read high-level pulse width		PWE_{HR}	ns	200	-	-	Figure 8.2
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 8.2
Setup time	Write (RS to NCS, E_NWR)	t_{ASE}	ns	10	-	-	Figure 8.2
	Read (RS to NCS , RW_NRD)			10	-	-	Figure 8.2
Address hold time		t_{AHE}	ns	5	-	-	Figure 8.2
Write data set up time		t_{DSWE}	ns	60	-	-	Figure 8.2
Write data hold time		t_{HE}	ns	15	-	-	Figure 8.2
Read data delay time		t_{DDR}	ns	-	-	200	Figure 8.2
Read data hold time		t_{DHR}	ns	5	-	-	Figure 8.2

Table 8. 4 68-System Normal Write Mode (HWM = 0) / (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	70	-	-	Figure 8.3
	Read (transmitted)	t_{SCYC}	ns	150	-	-	Figure 8.3
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	30	-	-	Figure 8.3
	Read (transmitted)	t_{SCH}	ns	70	-	-	Figure 8.3
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	30	-	-	Figure 8.3
	Read (transmitted)	t_{SCL}	ns	70	-	-	Figure 8.3
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	20	Figure 8.3
Chip select set up time		t_{CSU}	ns	20	-	-	Figure 8.3
Chip select hold time		t_{CH}	ns	60	-	-	Figure 8.3
Serial input data set up time		t_{SISU}	ns	30	-	-	Figure 8.3
Serial input data hold time		t_{SIH}	ns	30	-	-	Figure 8.3
Serial output data set up time		t_{SOD}	ns	-	-	100	Figure 8.3
Serial output data hold time		t_{SOH}	ns	10	-	-	Figure 8.3

Table 8. 5 (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

RGB Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	Figure 8.4
ENABLE setup time	t_{ENS}	ns	10	-	-	Figure 8.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 8.4
PD data setup time	t_{PDS}	ns	10	-	-	Figure 8.4
PD data hold time	t_{PDH}	ns	40	-	-	Figure 8.4
DOTCLK high-level pulse width	PWDH	ns	40	-	-	Figure 8.4
DOTCLK low-level pulse width	PWDL	ns	40	-	-	Figure 8.4
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Figure 8.4
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	25	Figure 8.4

Table 8. 6 18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	Figure 8.4
ENABLE setup time	t_{ENS}	ns	10	-	-	Figure 8.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 8.4
PD data setup time	t_{PDS}	ns	10	-	-	Figure 8.4
PD data hold time	t_{PDH}	ns	30	-	-	Figure 8.4
DOTCLK high-level pulse width	PWDH	ns	30	-	-	Figure 8.4
DOTCLK low-level pulse width	PWDL	ns	30	-	-	Figure 8.4
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	Figure 8.4
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	25	Figure 8.4

Table 8. 7 6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

8.3 DC Characteristic

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVCC=1.65~3.3V, VCC= 2.4 ~ 3.3V	0.8*IOVCC	-	-	-
Input low voltage	V_{IL}	V	IOVCC=1.65~3.3V, VCC= 2.4 ~ 3.3V	-	-	0.18*IOVCC	-
Output high voltage(1) (DB0-15 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.9*IOVCC	-	-	-
Output low voltage (DB0-15 Pins)	V_{OL1}	V	IOVCC=1.65~3.3V, VCC= 2.4 ~ 3.3V I_{OL} = 0.1mA	-	-	0.1*IOVCC	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ IOVCC	-0.1	-	0.1	IOVCC=2.8V
Current consumption during normal operation (VCC – VSSD)	I_{OP}	µA	IOVCC=3.0V, VCC=3.0V , VREG1OUT=4.93V VLCDC=5.5V (VC=3'b001, 0.92*VCI), f_{OSC} = 236KHz (160 line) , Ta=25°C, GRAM data = 0000h, REV="1", SAP="100", ON4-0="0", OP4-0="0", MP52-00="0", MN52-00="0", CP12-00="0" CN12-00="0	-	80uA (VCC)	200uA (VCC)	-
Current consumption during standby mode (VCC – VSSD)	I_{ST}	µA	IOVCC=3.0V, VCC=3.0V , Ta=25°C	-	1 (IOVCC, VCC)	10 (IOVCC, VCC)	-
Output voltage deviation		mV	-	-	5mV	-	-
Dispersion of the Average Output Voltage	V	mV	-	-10mV	-	10mV	-

Table 8. 8 (IOVCC = 1.65 ~ 3.3V, VCC = 2.4 ~ 3.3V, Ta = -40 ~ 85 °C)

8.4 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fOSC	kHz	Rf = 200kΩ, VCC = 3.0V	200	250	300

Table 8. 9 Clock Characteristics (VCC = 2.4 ~ 3.3V, IOVCC = 1.65 ~ 3.3V)

8.5 Reset Timing Characteristics

Item	Symbol	Unit	Timing diagram	Min.	Typ.	Max.
Reset low-level width	tRES	ms	Figure 8.6	1	-	-
Reset rise time	trRES	µs	Figure 8.6	-	-	10

Table 8. 10 Reset Timing Characteristics (VCC = 2.4 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

8.6 LCD driver output Characteristics

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Driver output delay time	tdd	µs	IOVCC=3V, VCC=3V, VLCD=5.5V, VREG1OUT=5.0V, RC oscillation: fosc =315kHz (160 lines), Ta=25&C REV=0, SAP=010, AP=010, 0N14-00=0, 0P14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF ' when the level changes from a same grayscale level on all pins ' Time to reach +/-35mV when VCOM polarity inverts	-	35	-

Table 8. 11 LCD Driver Output Characteristics

8.7 Timing Characteristic

80-system Bus Operation

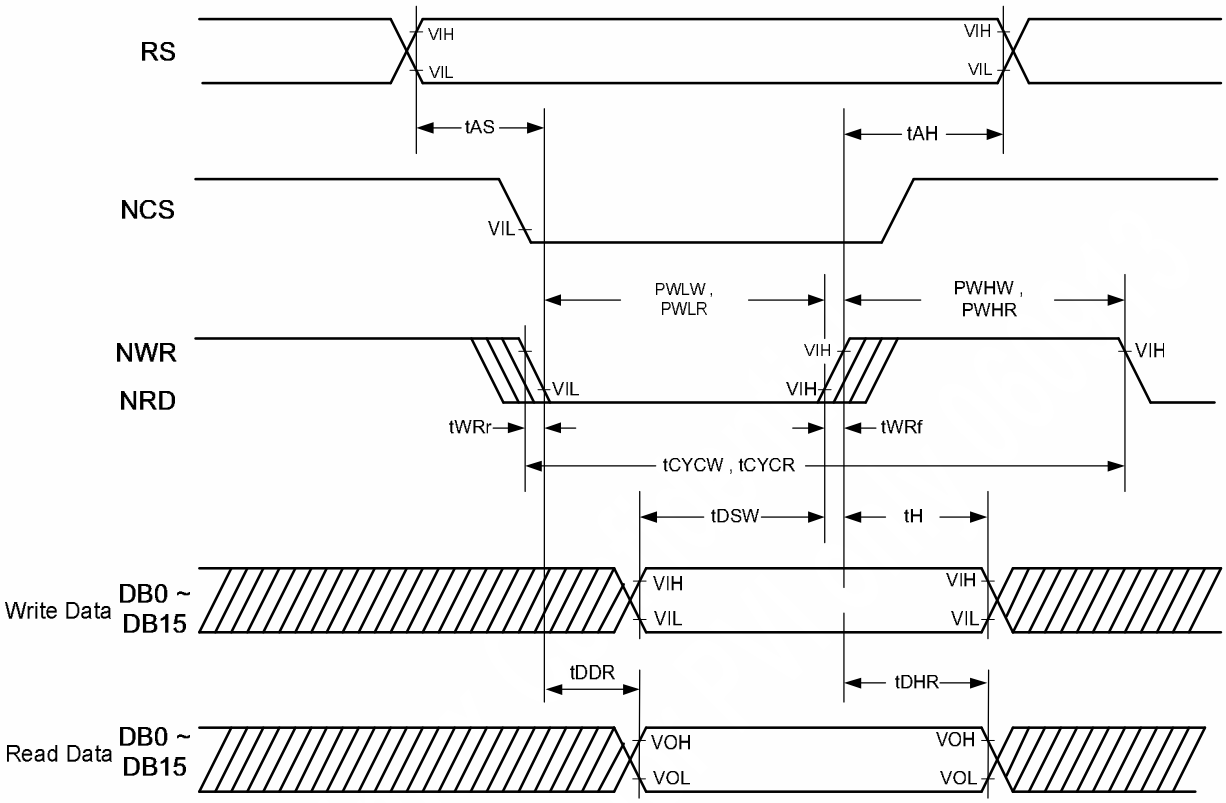


Figure 8. 1 80-system Bus Timing

68-system Bus Operation

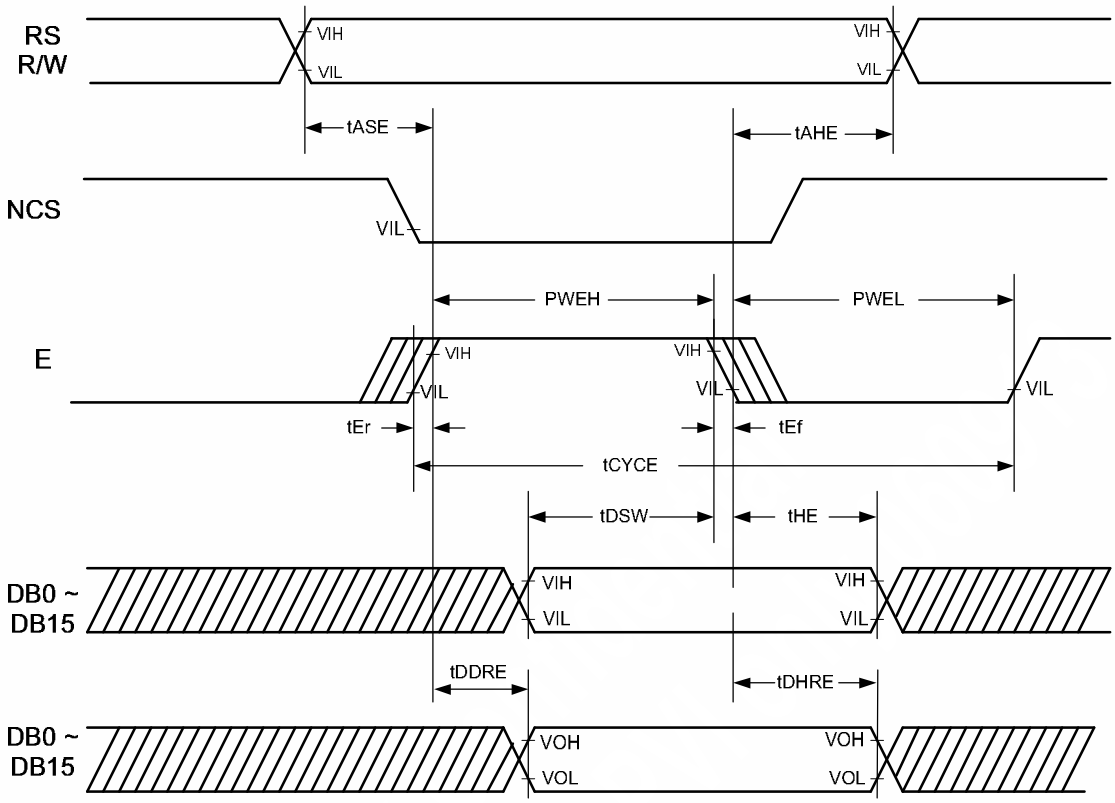


Figure 8. 2 68-system Bus Operation

Clock Synchronized Serial Data Transfer Interface Operation

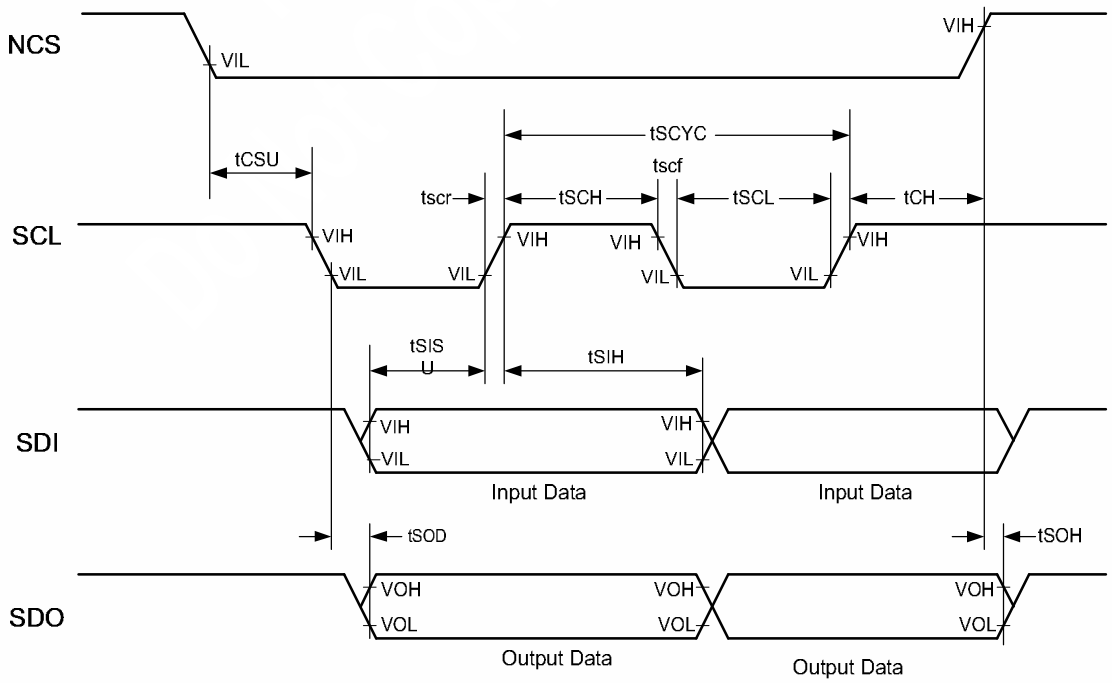


Figure 8. 3 Clock Synchronized Serial Data Transfer Interface Timing

RGB Interface Operation

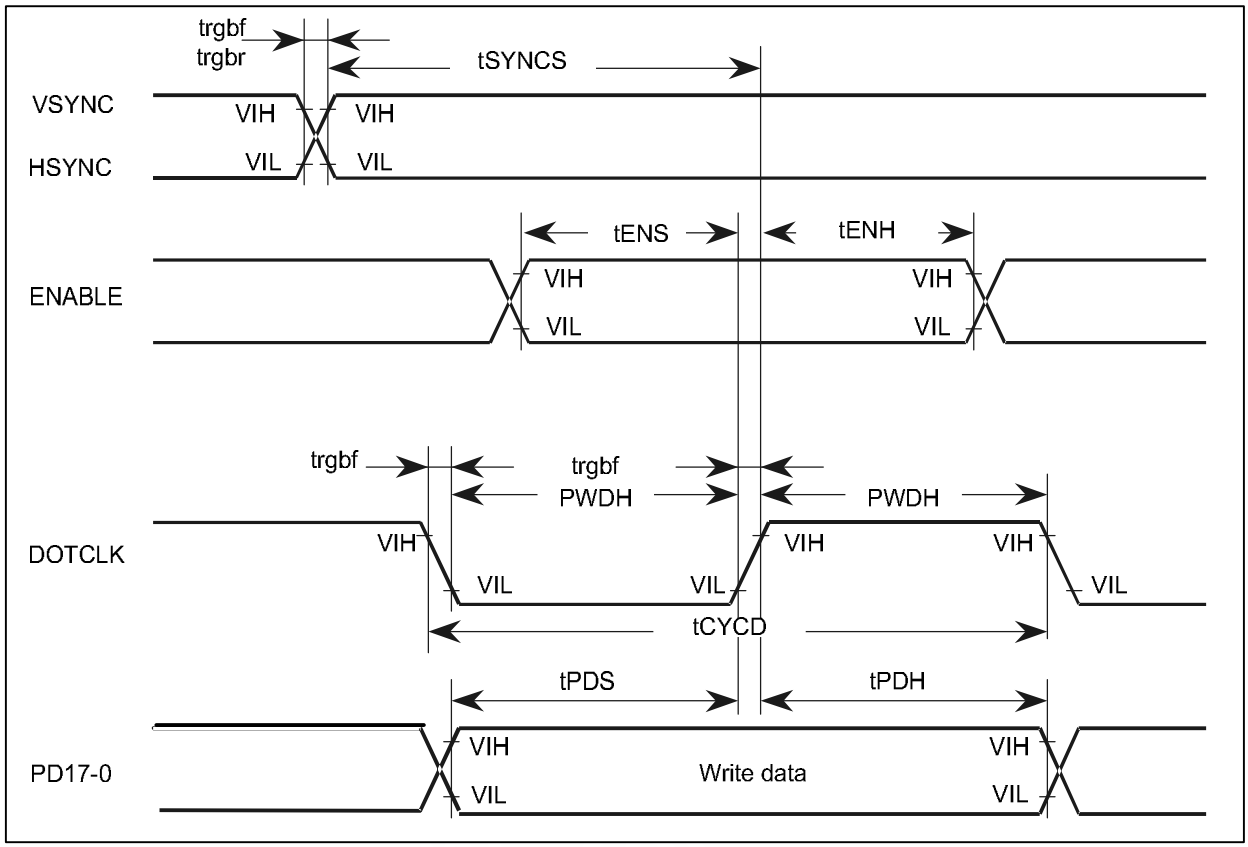


Figure 8. 4 RGB Interface Operation

LCD Driving Output

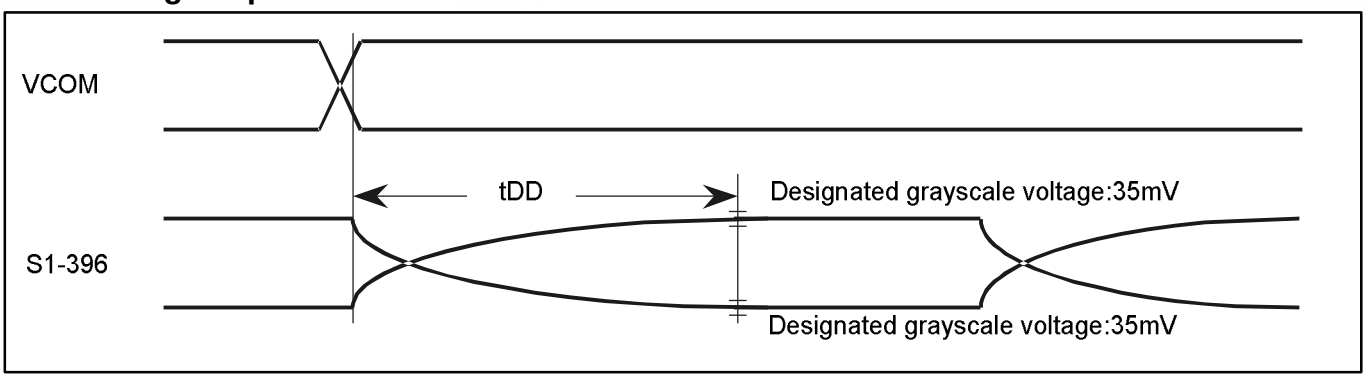


Figure 8. 5 LCD Driving Output

Reset Operation

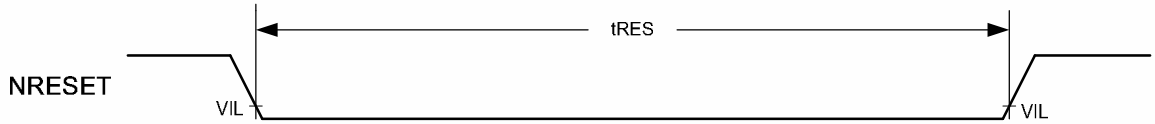


Figure 8. 6 Reset Timing

9. System Configuration

9.1 System Diagram

The system configuration diagram illustrates as following:

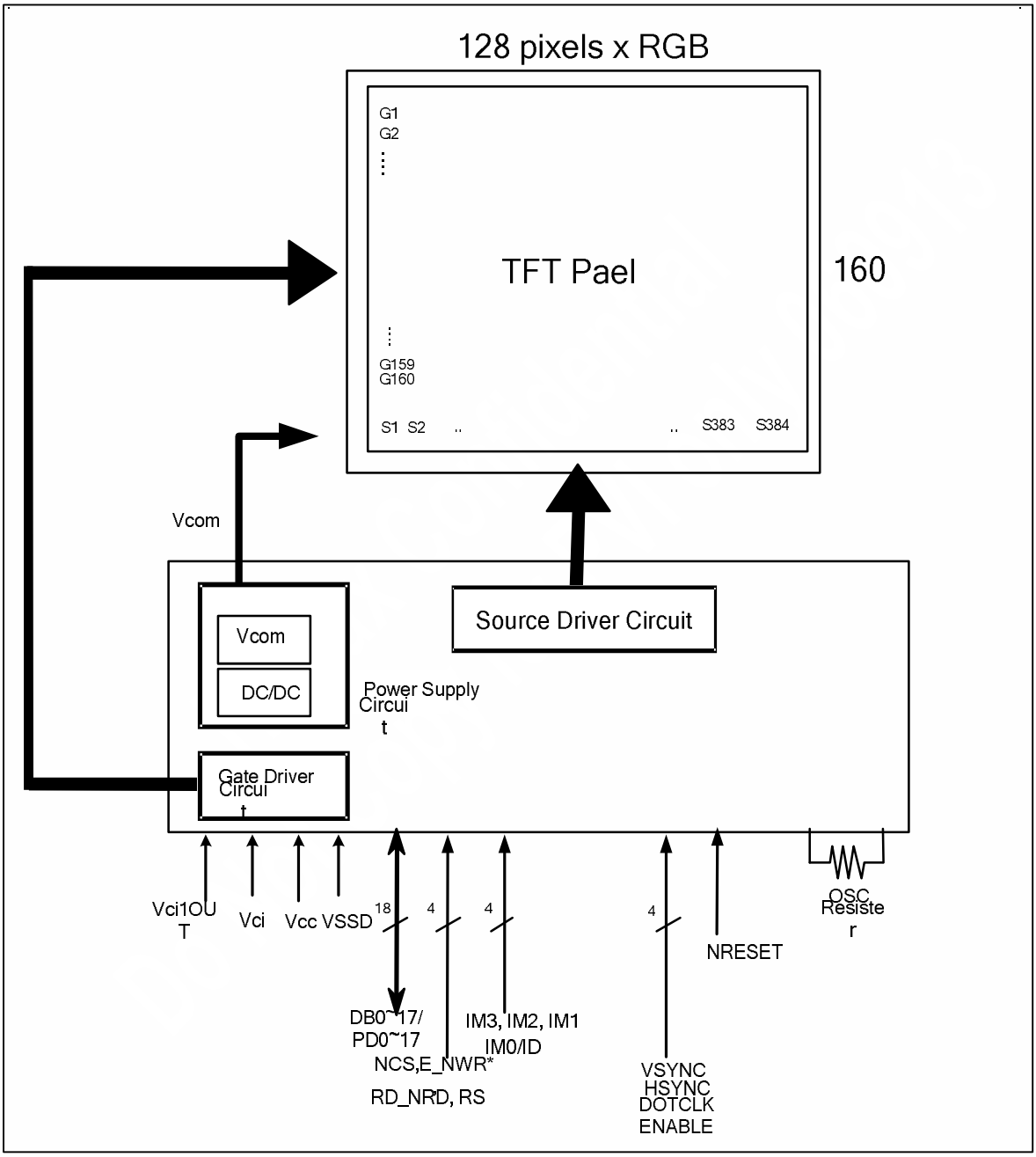
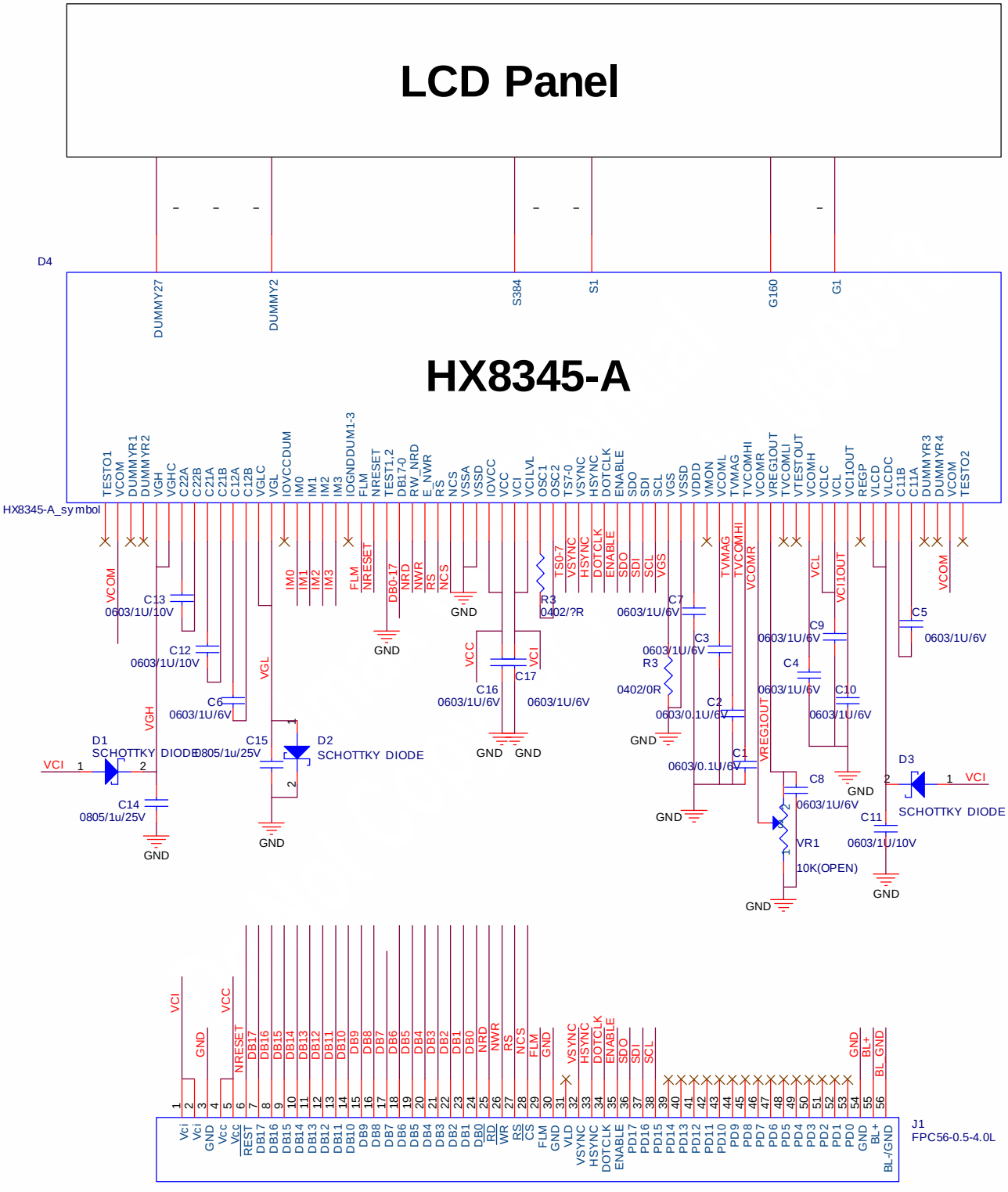


Figure 9. 1 System Diagram of HX8345-A

9.2 System Connection Diagram



1. TVCOMHI,TVMAG pin must be connected to 0.1uF capacitor (B characteristics).
2. Vcc and Vci are separated from different power source.
3. SDO pin is output pin. SDO pin must be left floating when no use.
4. The input pin must be fixed Vcc or GND when no use. Refer to "Pin Description".
5. nRD pin must be wring to the FPC connector and connect with MPU

Figure 9. 2 System Connection Diagram of HX8345-A

Capacitor	Connect to	Capacitor Value / Voltage	
C1	TVCOMHI	0.1uF (B characteristics)	6V
C2	TVMAG	0.1uF (B characteristics)	6V
C3	VCOMH	1uF (B characteristics)	6V
C4	VCOML	1uF (B characteristics)	6V
C5	C11A/B	1uF (B characteristics)	10V
C6	C12A/B	1uF (B characteristics)	6V
C7	VDDD	1uF (B characteristics)	6V
C8	VREG1OUT	1uF (B characteristics)	10V
C9	VCLC	1uF (B characteristics)	6V
C10	VCI1OUT	1uF (B characteristics)	6V
C11	VLCD	1uF (B characteristics)	10V
C12	C21A/B	1uF (B characteristics)	10V
C13	C22A/B	1uF (B characteristics)	10V
C14	VGHC	1uF (B characteristics)	25V
C15	VGLC	1uF (B characteristics)	25V
C16	VCC	1uF (B characteristics)	6V
C17	VCI	1uF (B characteristics)	6V

Table 9. 1 Connect Capacitors

Note: The aforementioned capacitors must be connected otherwise it will cause poor display quality.

Component	Spec	Remarks
Diode	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: HSC226)	Connect to Schottky Diode
Variable Resistor (VCOMR)	> 200KΩ	Connect to variable resistor while the VcomH1 is adjusted by external voltage input.

Table 9. 2 Connected Schottky Diode and Resistor

Note: The aforementioned Components must be connected otherwise it will cause poor display quality.

9.3 Layout Recommendation

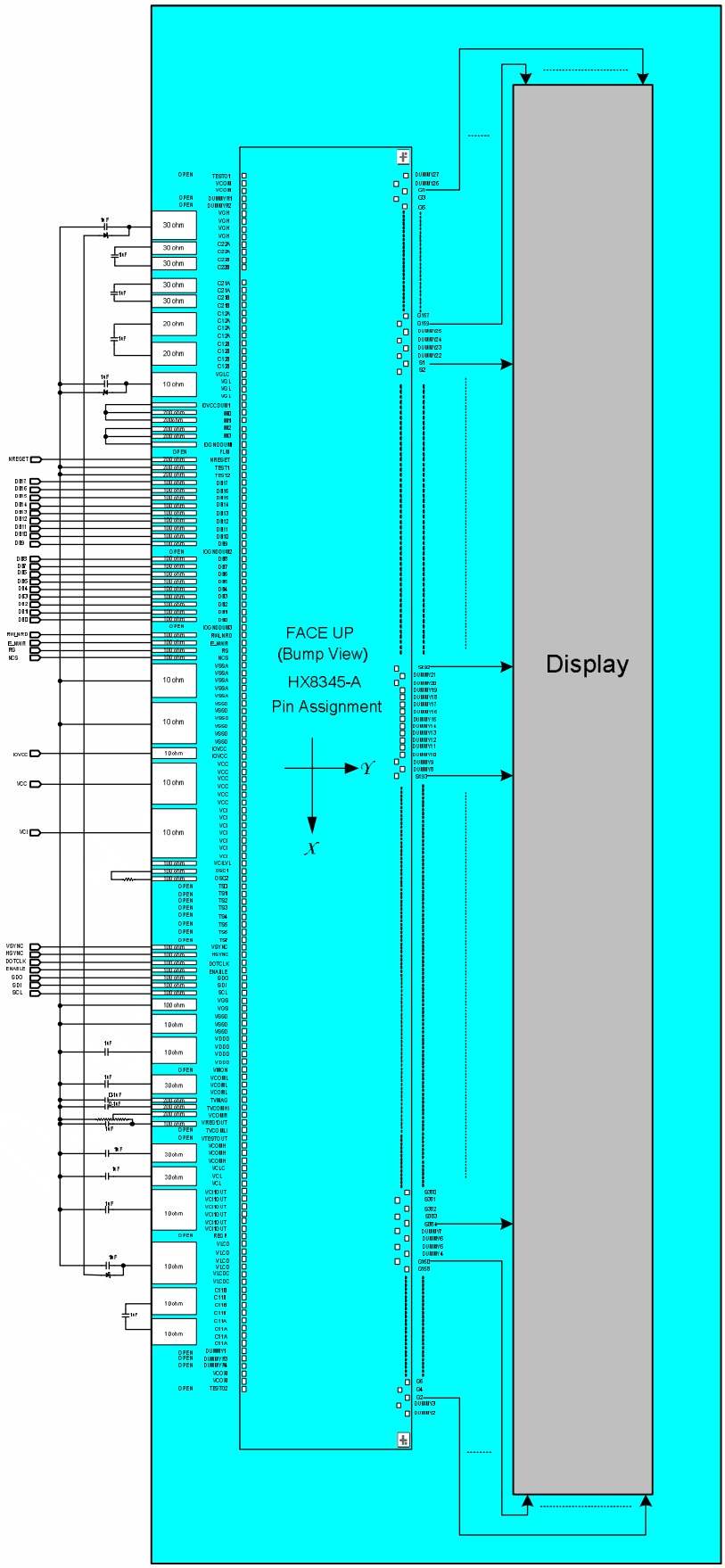


Figure 9. 3 Layout Recommendation of HX8345-A

10. Ordering Information

Part NO.	Package
HX8345-A000PDxxx	PD: means COG xxx: means chip thickness (um), default 400 um

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2006/05/02	New Setup
	2006/05/03	1. Page 15: Added Pin Assignments 2. Page 16 ~ 18: Added PAD Coordinate 3. Page 19: Added BUMP Arrangement
	2006/07/18	1. Page 145:Added System Connection Diagram 2. Page 146:Added Connected Capacitor, Diode, Resistor. 3. Page 147:Added Layout Recommendation.
	2006/08/09	1. Remove HWM related Data. 2. Page 15 Pin assignments. 3. Page 16 PAD Coordinate.
	2006/08/15	1. Page 15, Update chip size, including scribe line and seal ring 2. Page 101, Update Frame Rate Formula.
	2006/08/30	1. Page 9,Update Block diagram, take off graphic operation 2.
	2006/09/07	1. Page 15,Update Align mark's photo.