APPLICATION NOTE

(DOC No. HX8347-A-AN)

HX8347-A

240RGB x 320 dot, 262K color, with internal GRAM, TFT Mobile Single Chip Driver

Version 02 October, 2007

Himax Technologies, Inc.
http://www.himax.com.tw

HX8347-A

240RGB x 320 dot, 262K color, with internal GRAM, TFT Mobile Single Chip Driver

Himax Technologies, Inc.
http://www.himax.com.tw

List of Contents

October, 2007

List of Figures

List of Tables

1. Introduction

This document describes Himax's HX8347-A 240RGBx320 dots resolution driving controller. The HX8347-A is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

The HX8347-A supports three interface modes: Command-Parameter interface mode, Register-Content interface mode and RGB interface mode. Command-Parameter interface mode and Register-Content interface mode are selected by the external pins IFSEL0 setting, and RGB interface mode is selected by internal bit RGB_EN.

2. HX8347-A Chip Block Diagram

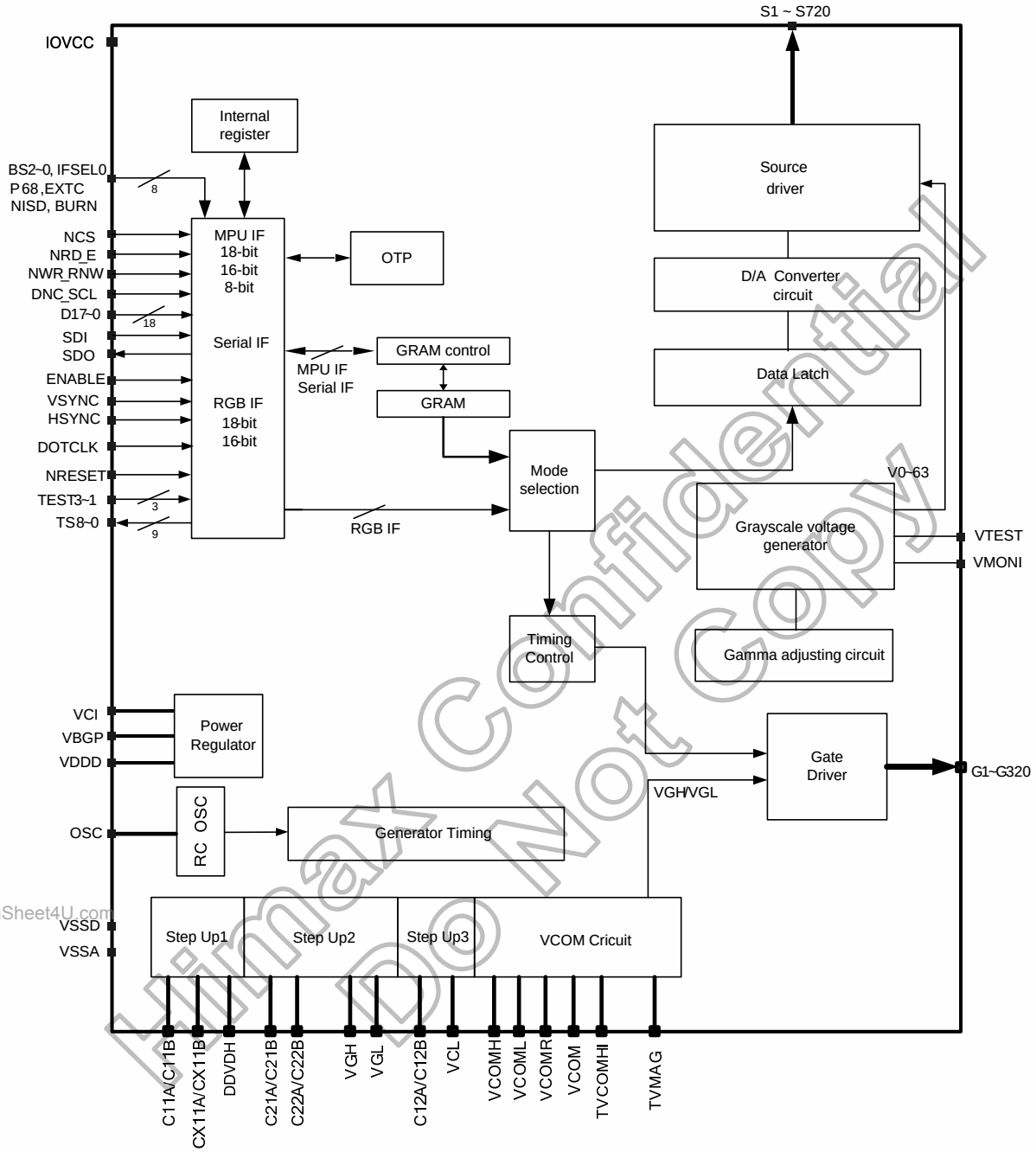


Figure 2. 1 HX8347-A block diagram

3. HX8347-A PAD Assignment

- Chip Size: 17820 um x 865 um
  (Including Seal-ring 20 um *2,
  Scribe line 40 um *2)
- Chip Thickness: 300 um (typ.)
- Pad Location: Pad center
- Coordinate Origin: Chip center
- Au Bump Size:
  1. 50 um x 120 um
     Input/Output
     (No. 1~ No. 243)
  2. 16 um x 98 um
     Staggered LCD output side
     (No. 244 ~ No. 1291)

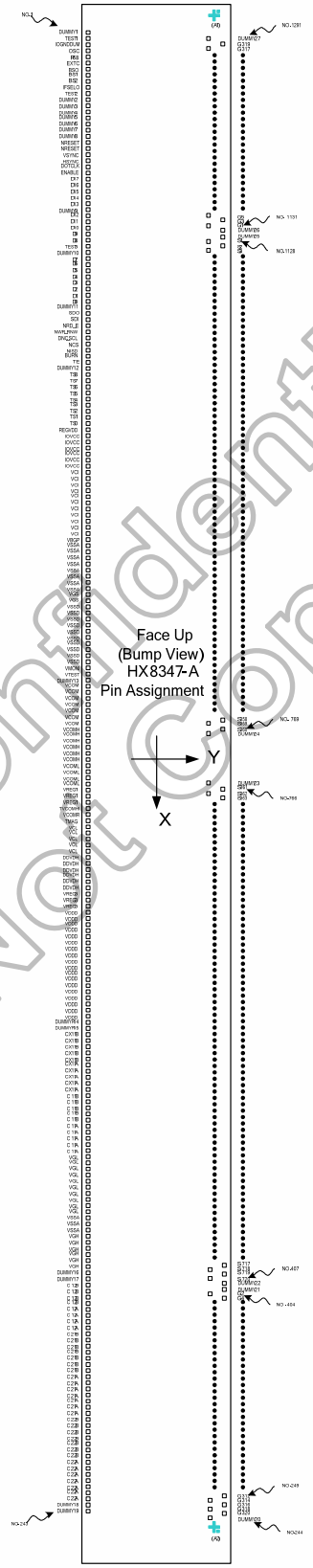
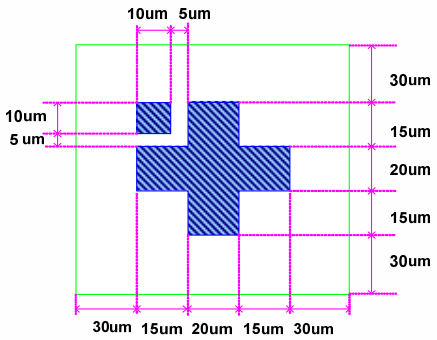


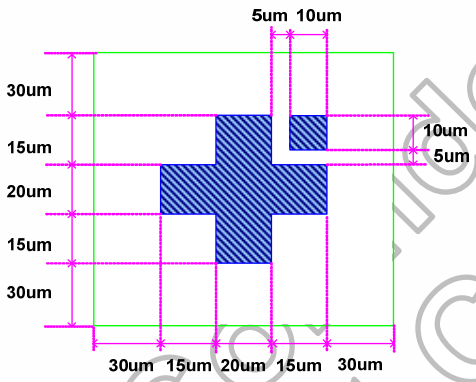
Figure 3. 1 HX8347-A pad assignment

3.1 Alignment mark

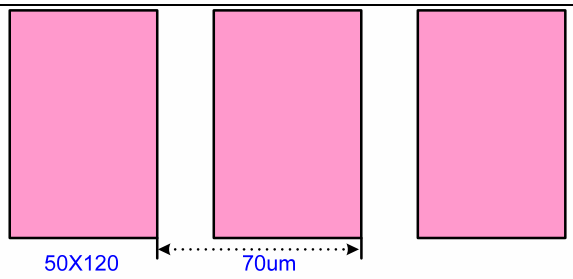
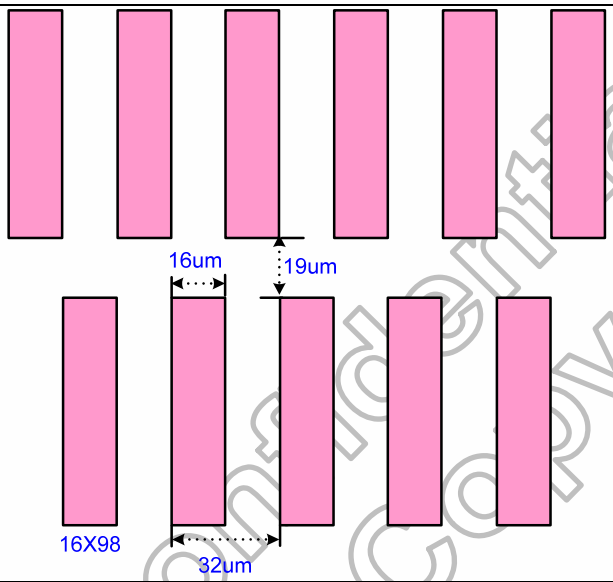
A_MARK (A1)



A_MARK (A2)



3.2 Bump size

Input PAD	
Output PAD	

4. Pin Description

<table>
<tr><th colspan="4">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>P68, BS2,BS1,BS0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>
Select the MPU interface mode as listed below
Use with IFSEL0=1 Register-content interface mode
<table>
<tr><th>P68</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 65K-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system, 262K-color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 80-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 80-system, 262-Color</td><td>D17-D8: Unused D7-D0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 262-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface, 80-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 65K-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system, 262K-color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 68-system, 262K-Color</td><td>D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 68-system, 262K-color</td><td>D17-D8:Unused D7-D0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 262K-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface, 68-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>ID</td><td>Serial bus IF</td><td>DNC_SCL, SDO,SDI</td></tr>
</table>
Use with IFSEL0=0 Command-Parameter interface mode
<table>
<tr><th>P68</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X</td><td>16-bit bus interface, 80-system,</td><td>D17-D16:Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td><td>8-bit bus interface, 80-system,</td><td>D17-D8:Unused, D7-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X</td><td>16-bit bus interface, 68-system,</td><td>D17-D16:Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>X</td><td>8-bit bus interface, 68-system,</td><td>D17-D8:Unused, D7-D0: Data</td></tr>
<tr><td>x</td><td>1</td><td>1</td><td>x</td><td>Serial interface</td><td>D17-D0:Unused SDI, SDO</td></tr>
<tr><td></td><td></td><td></td><td></td><td>(Other setting is inhibited)</td><td></td></tr>
</table>
</td></tr>
<tr><td>IFSEL0</td><td>I</td><td>1</td><td>MPU</td><td>
Interface format select pin
<table>
<tr><th>IFSEL0</th><th>Interface Format Selection</th></tr>
<tr><td>0</td><td>Command-Parameter interface mode</td></tr>
<tr><td>1</td><td>Register-content interface mode</td></tr>
</table>
In this case, the IFSEL0 has to be connected to IOVCC.
</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>Extended command set enable. (Only support Command-Parameter Interface mode à IFSEL0=0)
Low: extended command set is discarded
High: extended command set is accepted
If operate in Register-content interface mode, the EXTC can be connected to IOVCC or VSSD.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a write signal and writes data at the rising edge.
M68 system: 0: Write, 1: Read.
Fix it to IOVCC or VSSD level when using serial buss interface.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a read signal and read data at the low level.
M68 system: 0: Read/Write disable, 1: Read/Write enable.
Fix it to IOVCC or VSSD level when using serial buss interface.</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
BURN	I	1	MPU	Free Running mode If BURN=Hi, this can enable free running mode for burn in test. The display data alternates between full black and full white independent of input data in free running mode.
SDI	I	1	MPU	Serial data input pin. If not used, please let it connected to IOVCC or VSSD.
DNC_SCL	I	1	MPU	The signal for command or parameter select under parallel mode(i.e. Not serial interface): Low: command. High: parameter. When under serial interface, it servers as SCL.
VSYNC	I	1	MPU	Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.
HSYNC	I	1	MPU	Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.
ENABLE	I	1	MPU	A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level if unused (High active, if EPL=0).
DOTCLK	I	1	MPU	Dot clock signal. Has to be fixed to VSSD level if is not used.
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
OSC	I	1	Oscillation Resistor	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VCOMR	I	1	Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8347-A.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
SDO	O	1	MPU	Serial data output. If not use, let it to open.
NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B C12A,C12B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
CX11A, CX11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
D17~0	I/O	18	MPU	1. 18-bit bi-directional data bus for system interface. 8-bit bus: use D7-D0 and D17-D8 unused. 16-bit bus: use D15-D0 and D17-D16 unused. 18-bit bus: use D17-D0 2. 18-bit data bus for RGB interface 16-bit bus: use D17-D13, D11-D1 and D12, D0 unused. 18-bit bus: use D17-D0 Connected unused pins to the VSSD level. Notice: When register RGB_EN=1 and pin ENABLE=1, D[17:0] is used as stream image data for display. It means MPU data bus and RGB data bus is shared.

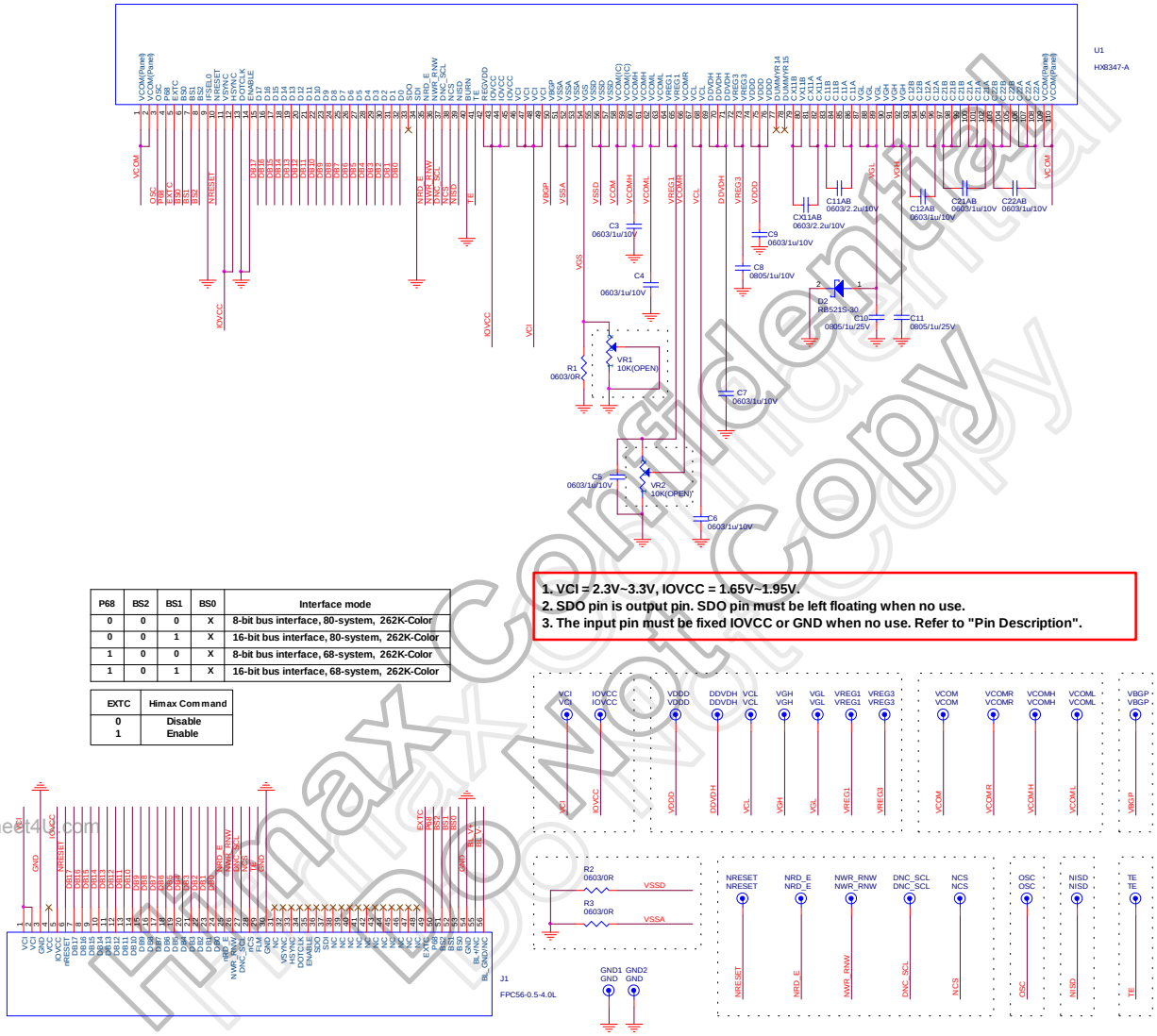
Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	1	Power Supply	Digital IO Pad power supply
VCI	P	1	Power Supply	Analog power supply
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	MPU	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. The REGVDD pin must be connected to IOVCC or VSSD.
VBGP	-	1	Open	Band Gap Voltage. Let it to be open.
VREG1	P	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREG3	P	1	Stabilizing Capacitor	A reference voltage for VGH&VGL.
VCOMH	P	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH. Place a schotkey barrier diode (see “configuration of the power supply”).
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH. Place a schottkey barrier diode between VCI and VGH. Place a schottkey barrier diode (see “configuration of the power supply ”).
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2.or –3 ~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply ”).

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
TS8~0	O	9	Open	A test pin. Disconnect it.
VMONI	O	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must be left open.
TVCOMHI	O	1	Open	A test pin output. Must be left open.
TVMAG	O	1	Open	A test pin output. Must be left open.
DUMMYR14-15	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR14 and DUMMYR15 are short-circuited within the chip.
DUMMY1-13 DUMMY16-27	-	25	Open	Dummy pads
IOGNDDUM	O	1	Open	Short-circuited within the chip

5. HX8347-A Reference FPC circuit (For CMO 3.2" / 2.4" / 2.8"LCD Panle)

5.1 Command-parameter interface mode

5.1.1 MPU Interface



P68	BS2	BS1	BS0	Interface mode
0	0	0	X	8-bit bus interface, 80-system, 262K-Color
0	0	1	X	16-bit bus interface, 80-system, 262K-Color
1	0	0	X	8-bit bus interface, 68-system, 262K-Color
1	0	1	X	16-bit bus interface, 68-system, 262K-Color

EXTC	Himax Command
0	Disable
1	Enable

Figure 5. 1 Reference FPC circuit Command-parameter interface mode's MPU interface

5.1.2 RGB interface

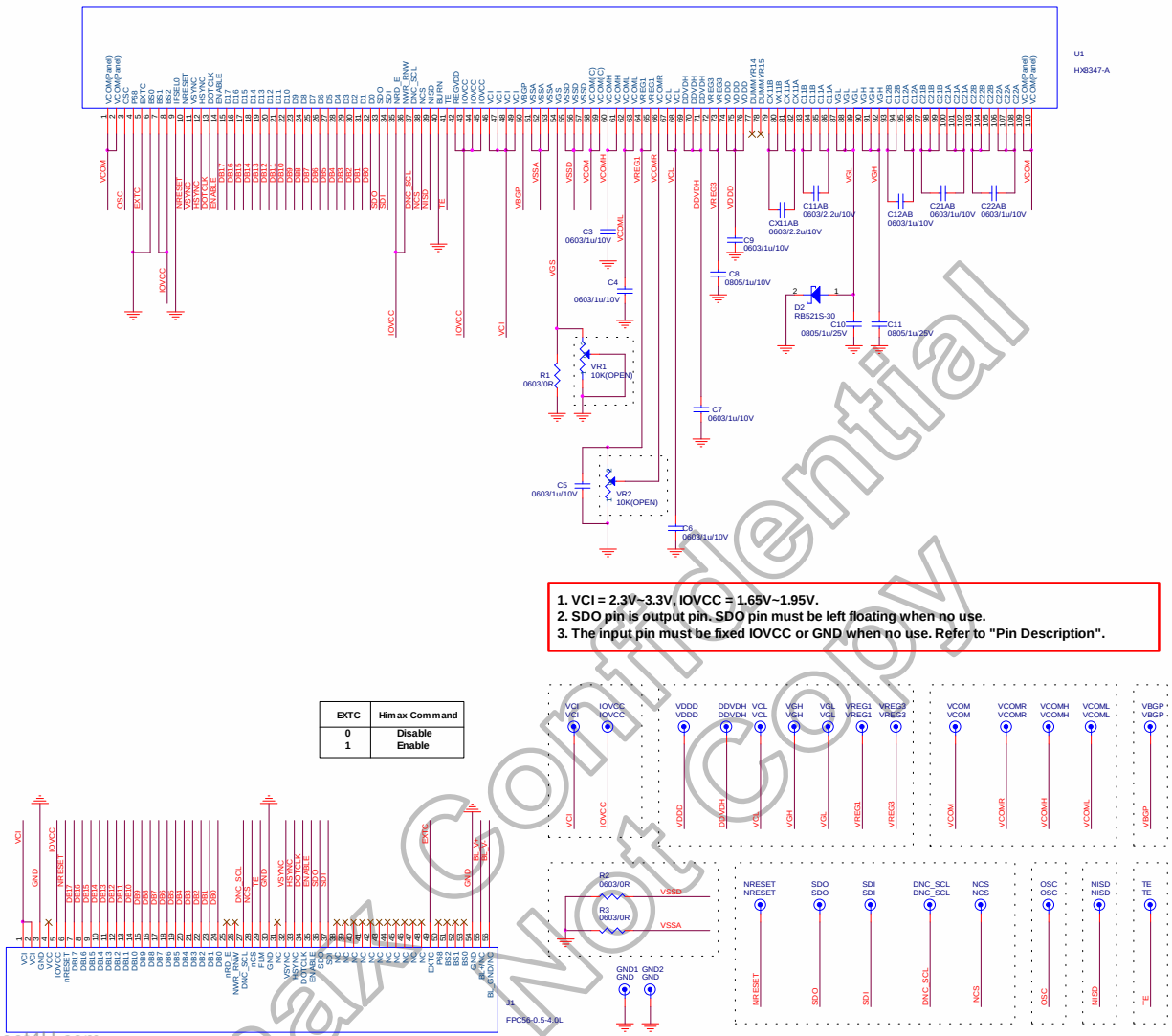
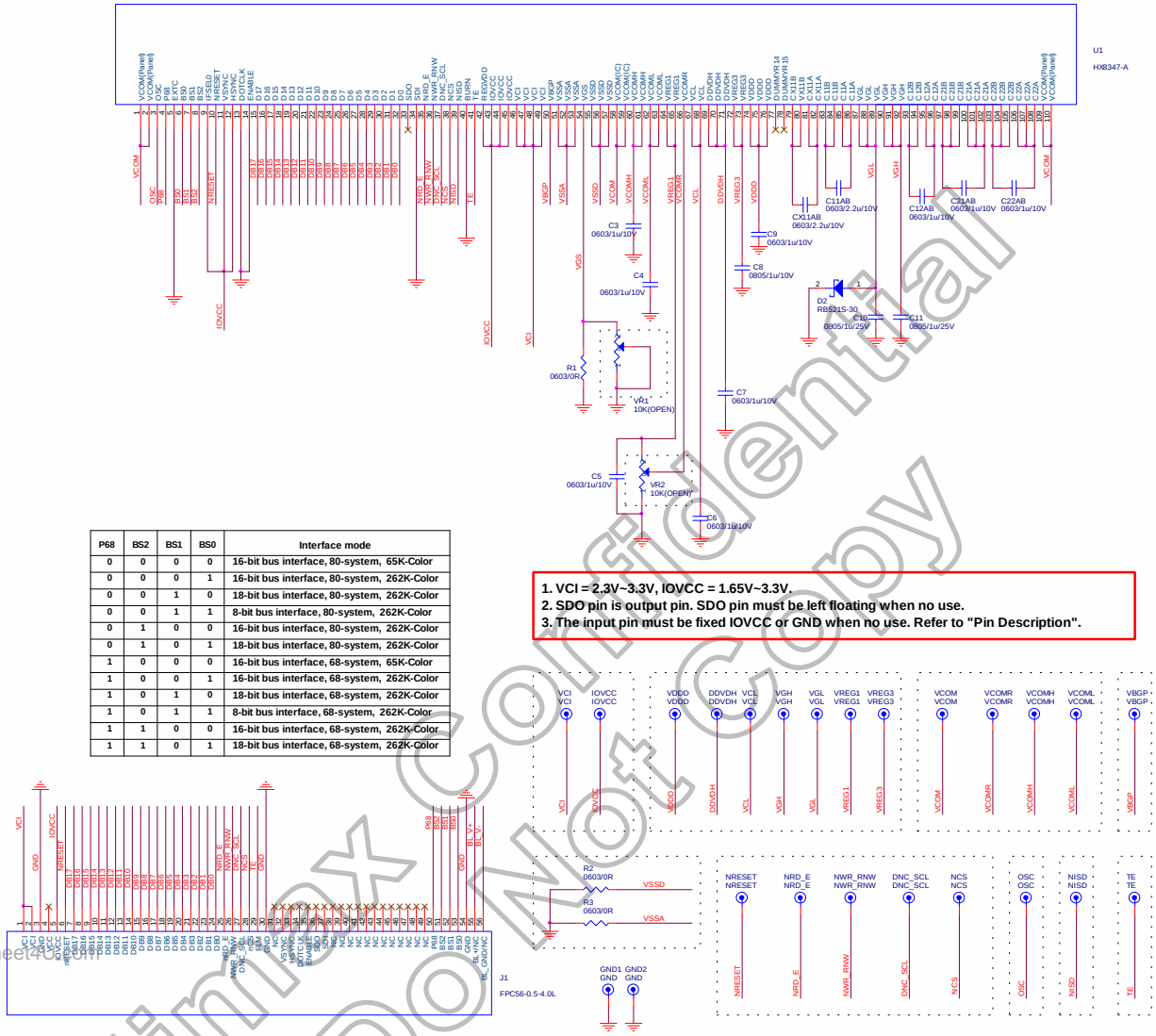


Figure 5. 2 Reference FPC circuit of Command-parameter interface mode's Serial + RGB interface

5.2 Register-content interface mode

5.2.1 MPU interface



P68	BS2	BS1	BS0	Interface mode
0	0	0	0	16-bit bus interface, 80-system, 65K-Color
0	0	0	1	16-bit bus interface, 80-system, 262K-Color
0	0	1	0	18-bit bus interface, 80-system, 262K-Color
0	0	1	1	8-bit bus interface, 80-system, 262K-Color
0	1	0	0	16-bit bus interface, 80-system, 262K-Color
0	1	0	1	18-bit bus interface, 80-system, 262K-Color
1	0	0	0	16-bit bus interface, 68-system, 65K-Color
1	0	0	1	16-bit bus interface, 68-system, 262K-Color
1	0	1	0	18-bit bus interface, 68-system, 262K-Color
1	0	1	1	8-bit bus interface, 68-system, 262K-Color
1	1	0	0	16-bit bus interface, 68-system, 262K-Color
1	1	0	1	18-bit bus interface, 68-system, 262K-Color

Figure 5. 3 Reference FPC circuit of Register-content interface mode's MPU interface

5.2.2 RGB with Serial interface

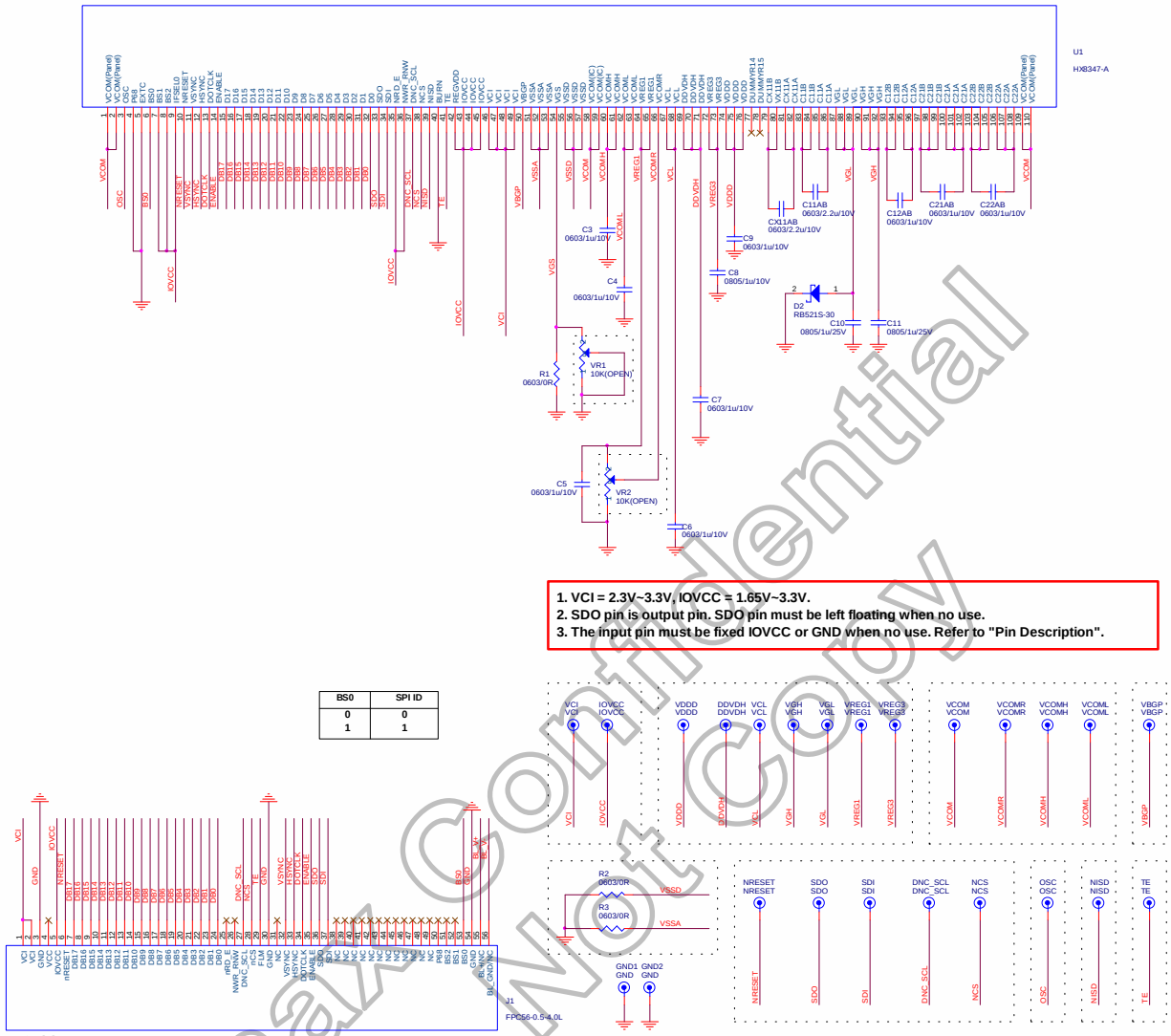


Figure 5. 4 Reference FPC circuit of Register-content interface mode's RGB interface

The specification of FPC circuit and pins connection is shown as following table:

Pad Name	Connection	Typical capacitance value (B characteristics)
VCOMH	Connect to Capacitor (Max 6V): VCOMH---(+)----| |--- (-)------ VSSA	1.0 uF
VCOML	Connect to Capacitor (Max 3V): VCOML ---(-)----| |--- (+)----- VSSA	1.0 uF
VGL	Connect to Capacitor (Max 16V): VGL ---(-)----| |--- (+)----- VSSA	1.0 uF
VGH	Connect to Capacitor (Max 21V): VGH ---(+)----| |--- (-)----- VSSA	1.0 uF
VCL	Connect to Capacitor (Max 5V): VCL ---(-)----| |--- (+)----- VSSA	1.0 uF
C22A - C22B	Connect to Capacitor (Max 7V): C22A ---(+)----| |--- (-)-----C22B	1.0 uF
C21A - C21B	Connect to Capacitor (Max 7V): C21A ---(+)----| |--- (-)-----C21B	1.0 uF
CX11A - CX11B	Connect to Capacitor (Max 7V): CX11A ---(+)----| |--- (-)-----CX11B	2.2 uF
C11A - C11B	Connect to Capacitor (Max 5V): C11A ---(+)----| |--- (-)-----C11B	2.2 uF
C12A - C12B	Connect to Capacitor (Max 5V): C12A ---(+)----| |--- (-)-----C12B	1.0 uF
VREG1	Connect to Capacitor (Max 10V): VREG1 ---(+)----| |--- (-)-----VSSA	1.0 uF
VREG3	Connect to Capacitor (Max 10V): VREG3 ---(+)----| |--- (-)-----VSSA	1.0 uF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 uF
DDVDH	Connect to Capacitor (Max 10V): DDVDH ---(+)----| |--- (-)-----VSSA	1.0 uF

Note: The aforementioned capacitor must be connected otherwise it will cause poor display quality.

Table 5. 1 Connected Capacitor

Pins connection	Feature
1. VSSD – VGL	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 5. 2 Connected Schottkey diode

6. LCD POWER GENERATION

6.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

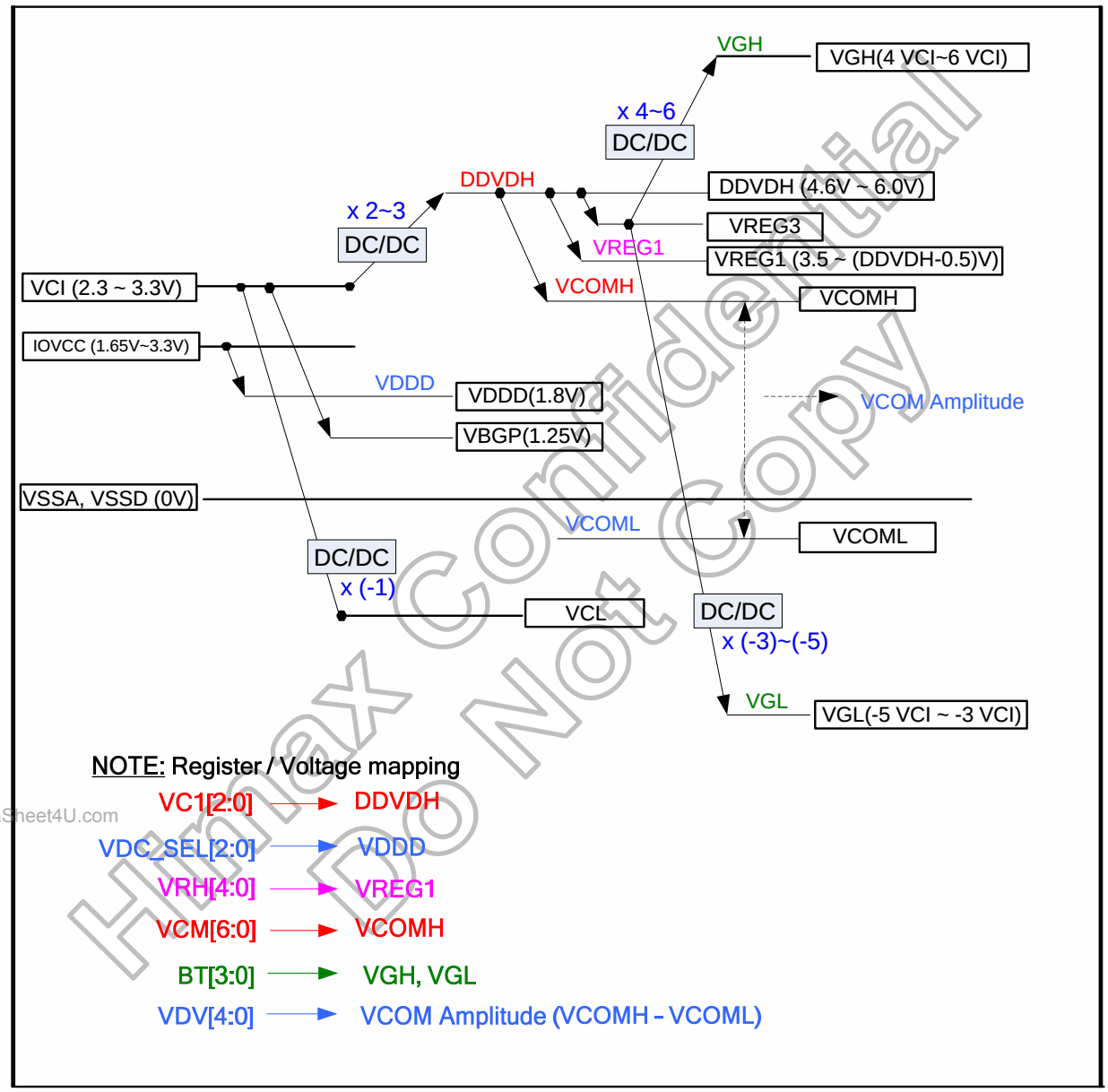


Figure 6. 1 LCD power generation scheme

6.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

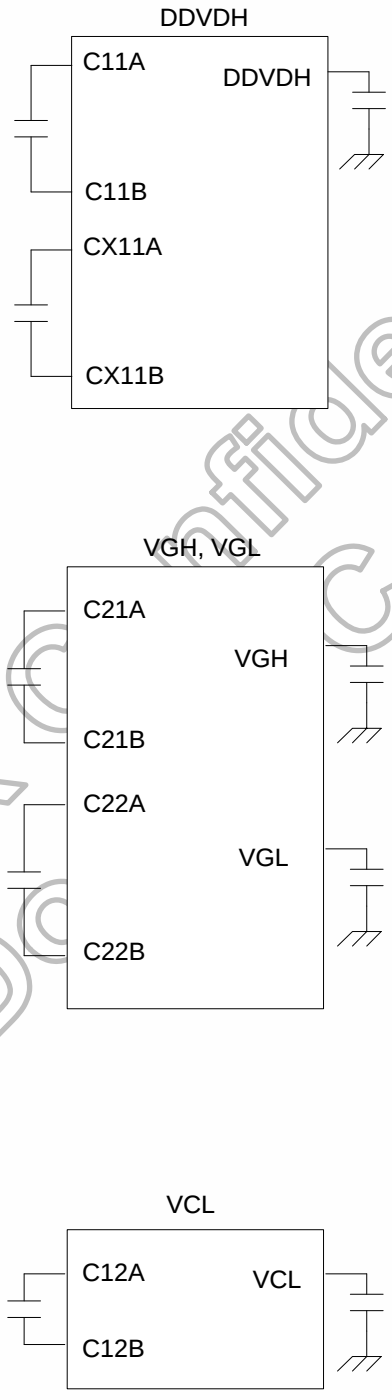


Figure 6. 2 Various boosting steps

7. Software Configuration

7.1 Features

7.1.1 Display

- Resolution: 240(H) x RGB(H) x 320(V)
- Display Color modes
  - A. Normal Display Mode On
    - a. Command-Parameter interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
    - b. Register-Content interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
      - ii. 65,536(R(5),G(6),B(5)) colors
  - B. Idle Mode On
    - a. 8 (R(1),G(1),B(1)) colors.

7.1.2 Display module

- AM-LCD glass 240xRGBx320
- Gamma correction (4 preset gamma curves)
- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - A. DDVDH = 4.6 to 6.0V (Source output voltage range)
  - B. VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - C. VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240 (H) x 320 (V) x 18 bit

7.1.3 Display/Control interface

- Display Interface types supported
  - A. Command-Parameter interface mode
    - 8-/16-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.
  - B. Register-Content interface mode
    - 8-/16-/18-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.

- Control Interface types supported
  - A. Command-Parameter interface mode.(IFSEL0= 0)
  - B. Register-Content interface mode (IFSEL0 = 1)

- Logic voltage (IOVCC):
  - A. HX8347-A00: 1.65V ~ 1.95V
  - B. HX8347-A01: 1.65V ~ 3.3V
- Driver power supply (VCI): 2.3 ~ 3.3V
- Color modes
  - A. 16 bit/pixel: R(5), G(6), B(5)
  - B. 18 bit/pixel: R(6), G(6), B(6)

7.1.4 Others

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDD for lower power consumption (such as 1.8 volts input)
- Support RGB through mode with lower power consumption
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (one-time-programming) non-volatile memory

7.2 GRAM mapping

Source Out		S1	S2	S3	S4	S5	S6	----------	S715	S716	S717	S718	S719	S720
RA								RGB Order —— :BGR=0 ----- :BGR=1						
MY=0	MY=1													
0	319	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R238 5-0	G238 5-0	B238 5-0	R239 5-0	G239 5-0	B239 5-0
1	318							–						
2	317							–						
3	316							–						
4	315							–						
5	314							–						
6	313							–						
7	312							–						
8	311							–						
9	310							–						
10	309							–						
11	308							–						
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
312	7							–						
313	6							–						
314	5							–						
315	4							–						
316	3							–						
317	2							–						
318	1							–						
319	0							–				RN 7-0	GN 7-0	BN 7-0
CA	MX=0	0			1				238			239		
	MX=1	239			238				1			0		

NOTE: RA = Row Address,
CA = Column Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control command
BGR= Red, Green and Blue pixel position change, D3 parameter of Memory Access Control command

Figure 7. 1 Memory Map. (240RGBx320)

7.3 Scan Function

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits MY, MX, MV as described below.

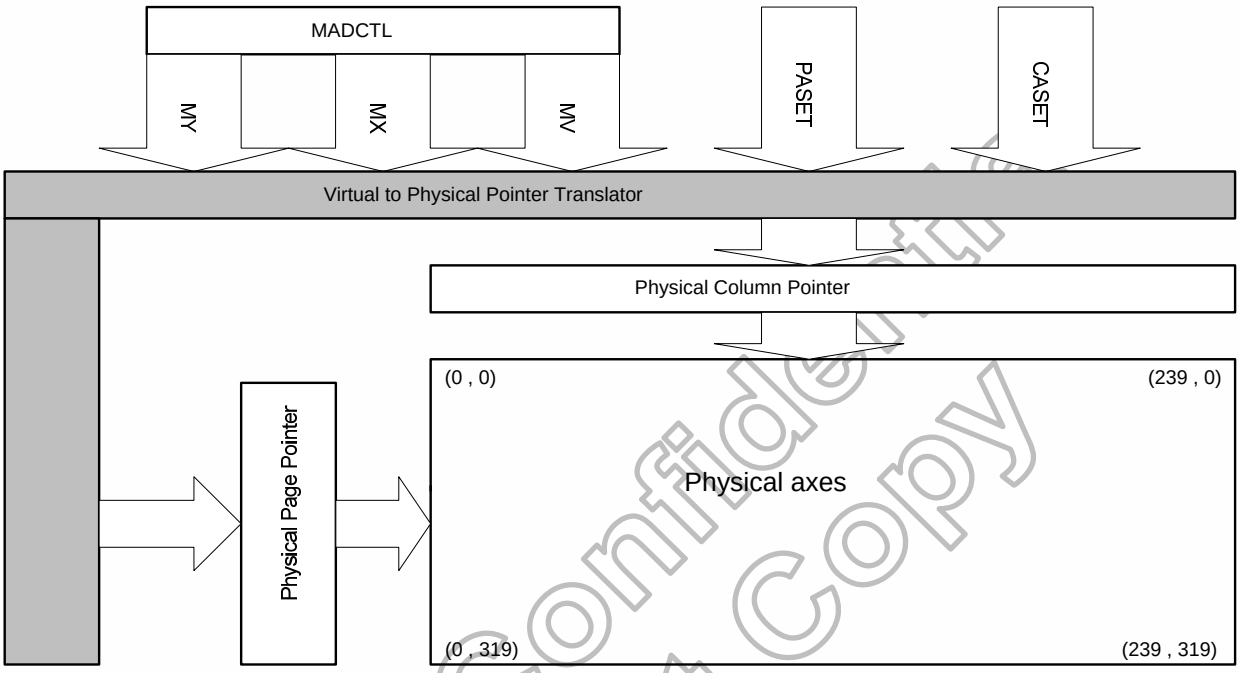


Figure 7. 2 MY, MX, MV Setting

MY	MX	MV	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

Table 7. 1 MY, MX, MV Setting

7.4 Interface Mode

7.4.1 Interface Mode Selection

IFSEL0	RGB_EN	Register Data	Display Data
0	0	Command-parameter interface (Parallel interface)	From SRAM
0	1	Command-parameter interface (Serial interface)	Sleep out Normal Display On : From RGB interface Sleep out Partial Mode On : From SRAM
1	0	Register-content interface (Parallel interface)	From SRAM
1	1	Register-content interface (Serial interface)	Normal display: From RGB interface Partial Mode: From SRAM

Table 7. 2 Interface Mode Selection

7.4.2 Register-Content Interface Mode

P68	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 7. 3 MPU selection in Register-content Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of GRAM data	Transferring Method of Command
0	0	0	16-bit system interface	16-bit 65K-color	8-bit collective
0	0	1	16-bit system interface	18-bit 262K-color (16+2)	
0	1	0	18-bit system interface	18-bit 262K-color	
0	1	1	8-bit system interface	18-bit 262K-color (6+6+6)	
1	0	0	16-bit system interface	18-bit 262K-color (6+6+6)	
1	0	1	18-bit system interface	18-bit 262K-color	
1	1	ID	Serial interface	RGB_EN=0,Select by register 72h	

Table 7. 4 Interface Selection in Register-content Interface Mode

Parallel Bus System Interface

a. Data Pin Function for I80/M68 Series CPU

Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 7. 5 Data Pin Function for I80 Series CPU

Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	1	0	0
Reads internal status	1	1	0
Writes command into register or data into GRAM	1	0	1
Reads command from register or data from GRAM	1	1	1

Table 7. 6 Data Pin Function for M68 Series CPU

b. Bit mapping of one pixel data:
Input Data (8-/16-/18-bit Interface) Written to GRAM through Write Data Register

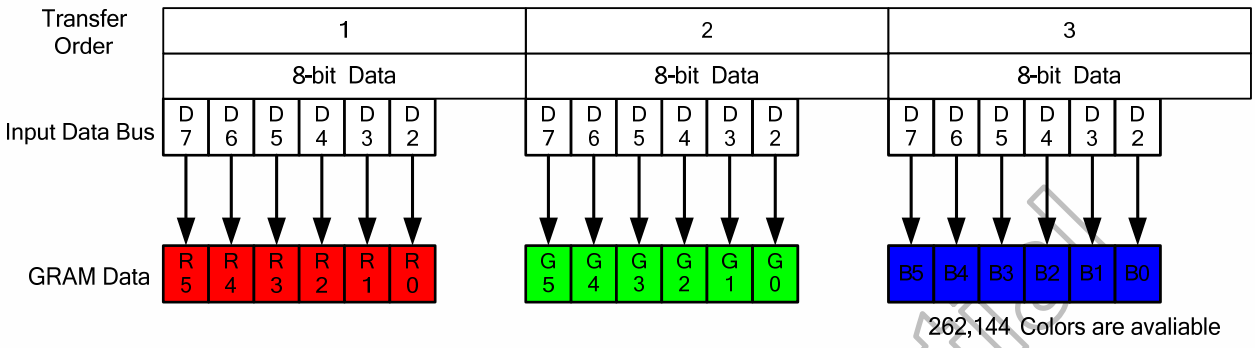


Figure 7. 3 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18(6 + 6 + 6) Bit-Data Input ("BS2, BS1, BS0"="011")

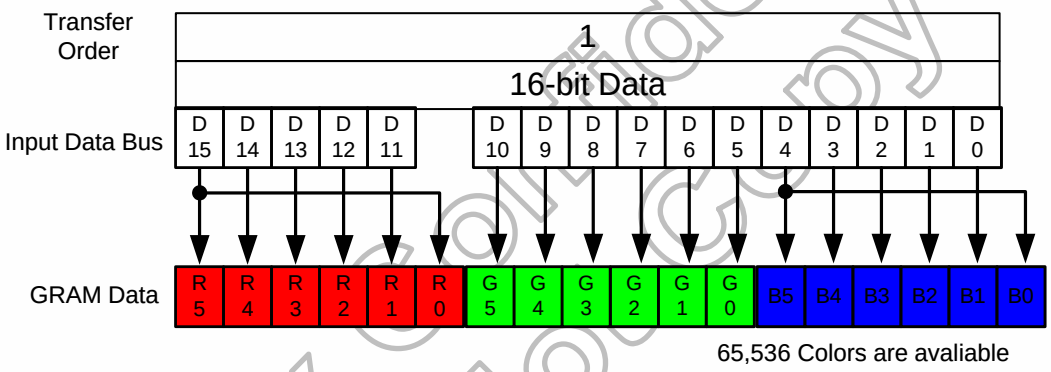


Figure 7. 4 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input ("BS2, BS1, BS0"="000")

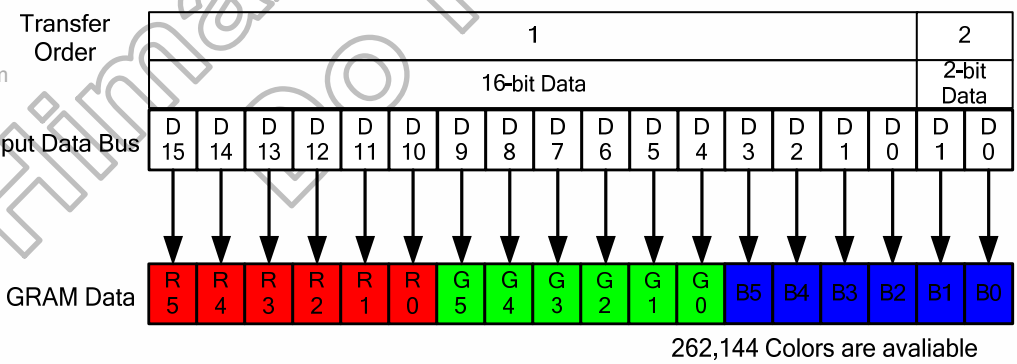


Figure 7. 5 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input ("BS2, BS1, BS0"="001")

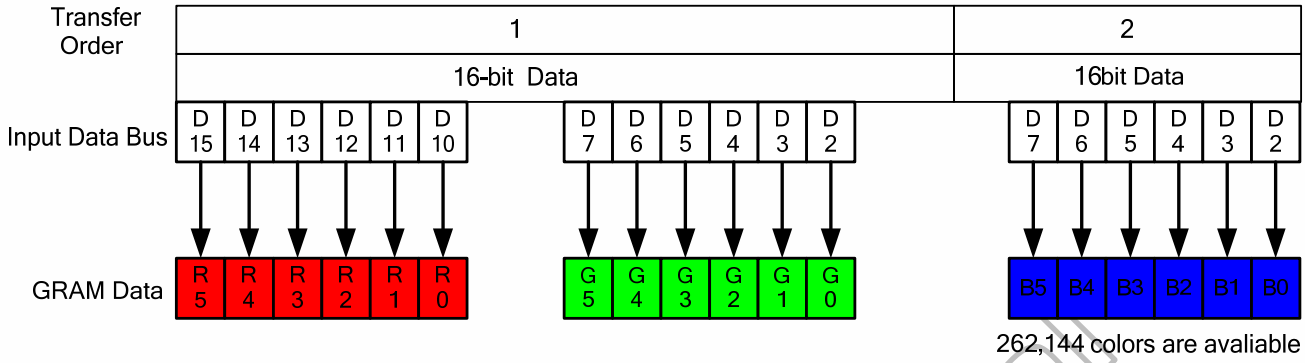


Figure 7. 6 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(6+6+6) Bit-Data Input ("BS2, BS1, BS0"="100")

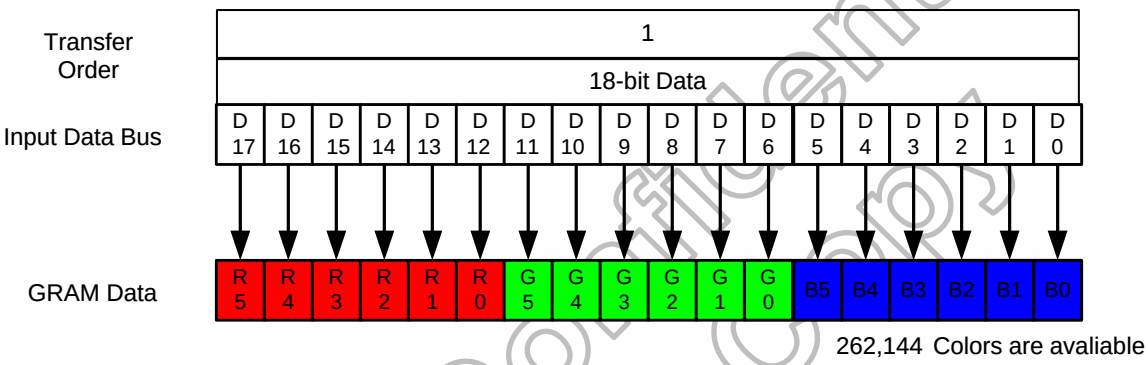
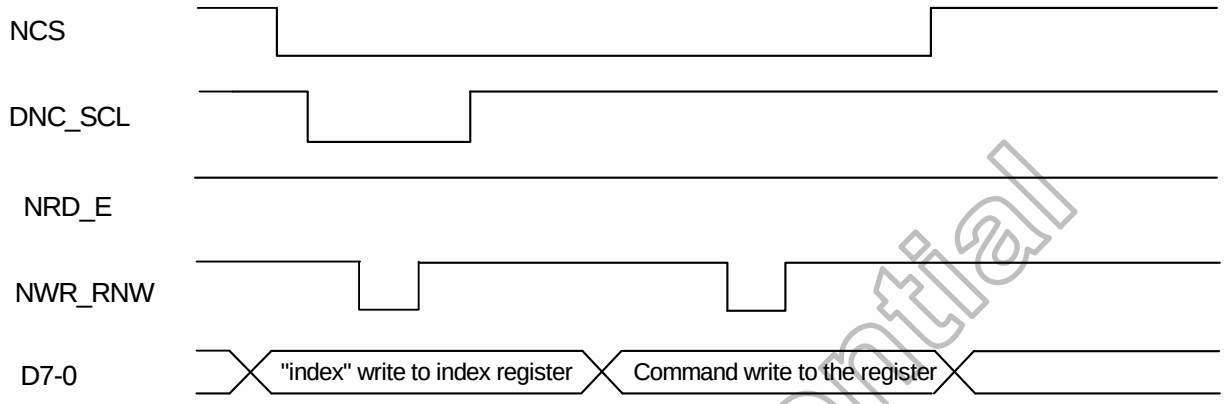


Figure 7. 7 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface ("BS2, BS1, BS0"="010" or "101")

I80- System Interface Timing

Write to the register



Read the register

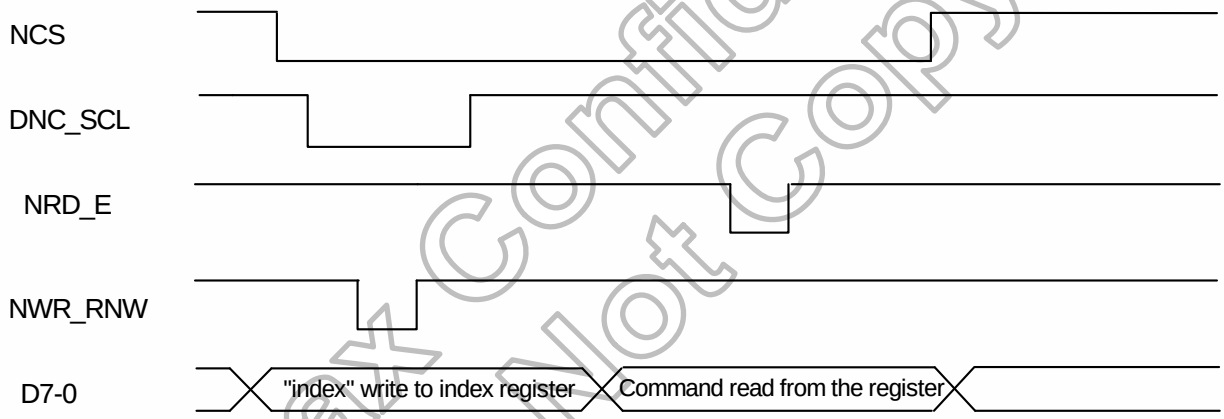


Figure 7. 8 Register read/write Timing in Parallel Bus System Interface (for I80 series MPU)

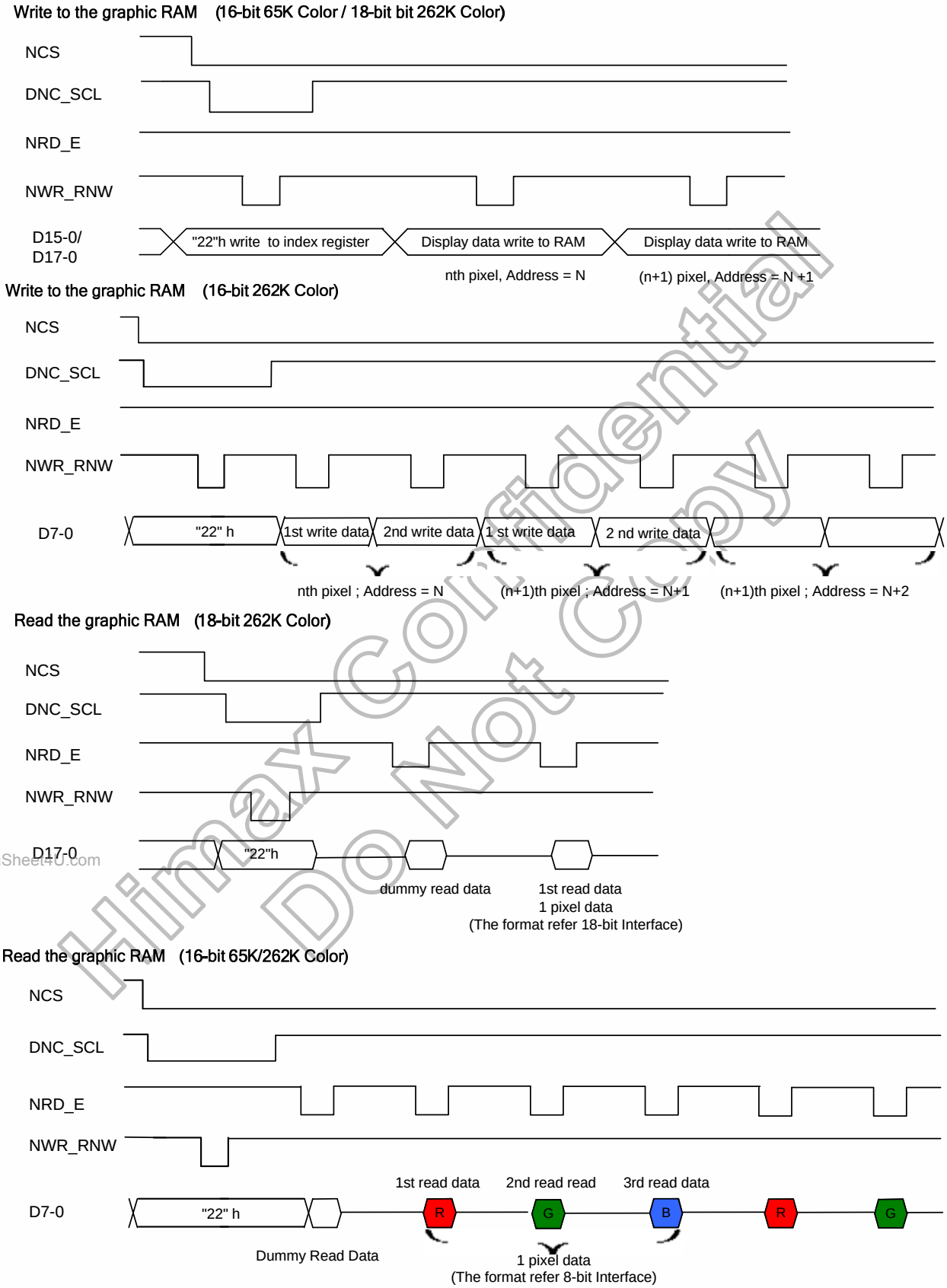
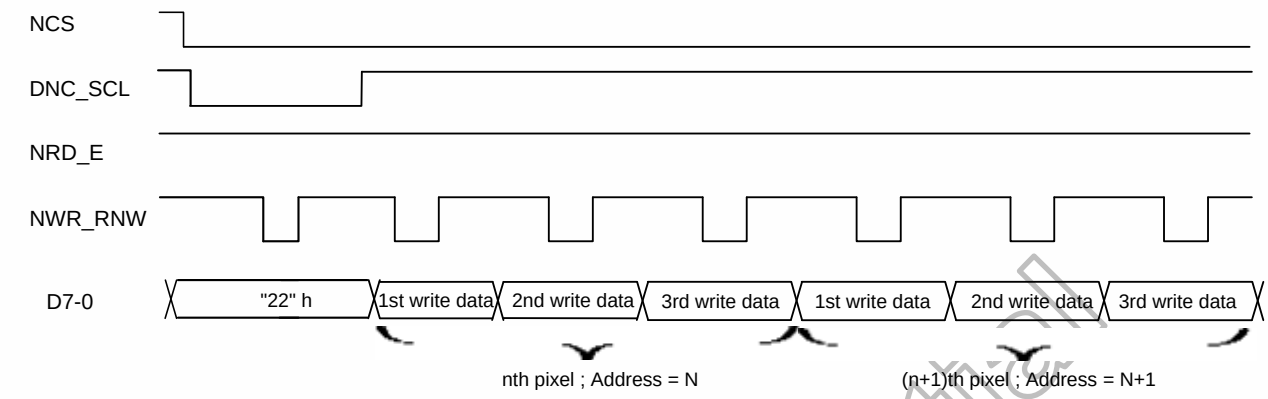


Figure 7. 9 GRAM read/write Timing in 16-/18-bit Parallel Bus System Interface (for I80 series MPU)

Write to the graphic RAM (8-bit 262K Color)



Read the graphic RAM (8-bit 262K Color)

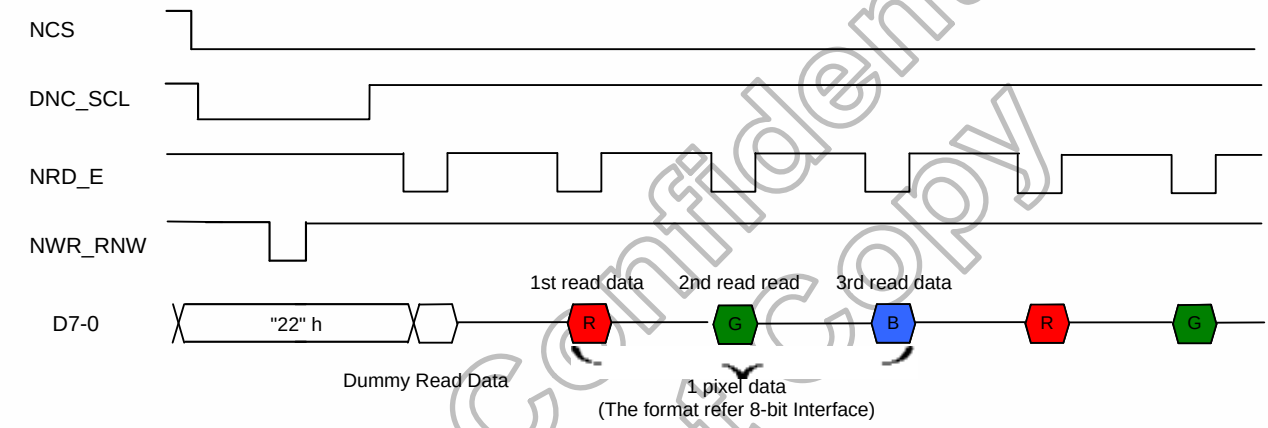


Figure 7. 10 GRAM read/write Timing in 8-bit Parallel Bus System Interface (for I80 series MPU)

M68- System Interface Timing

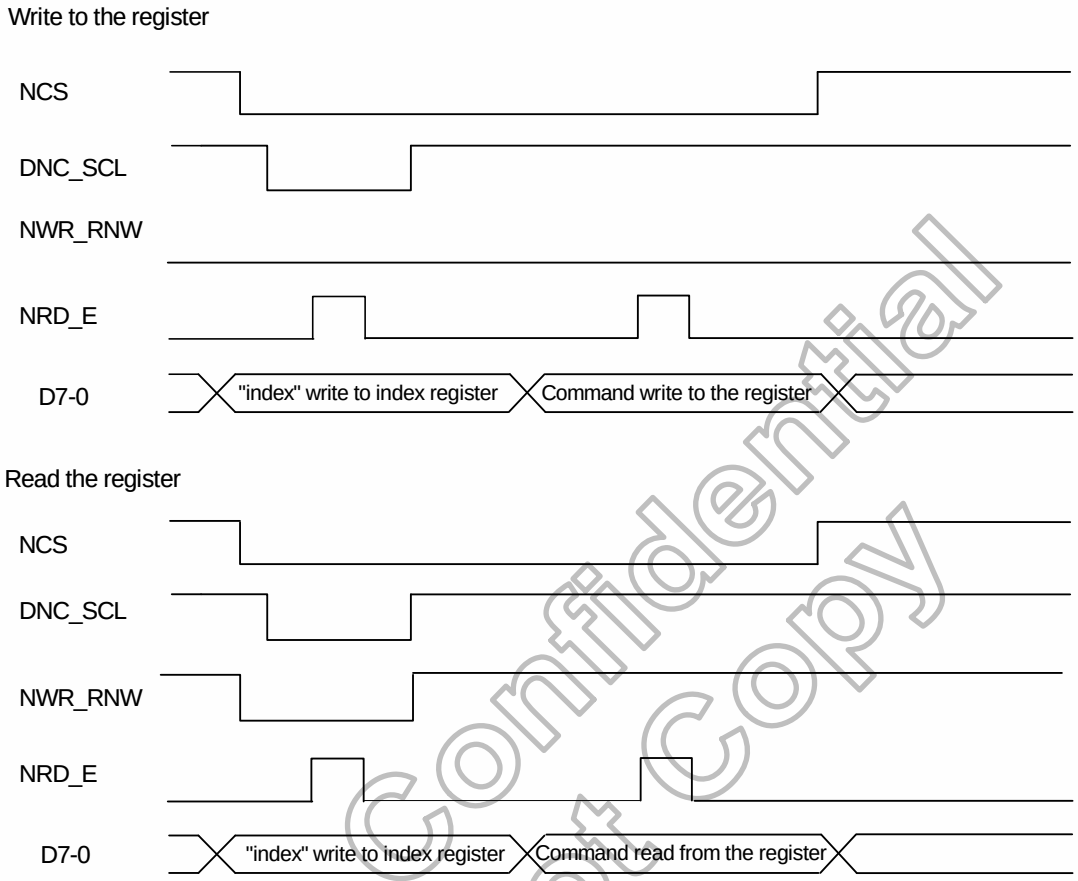
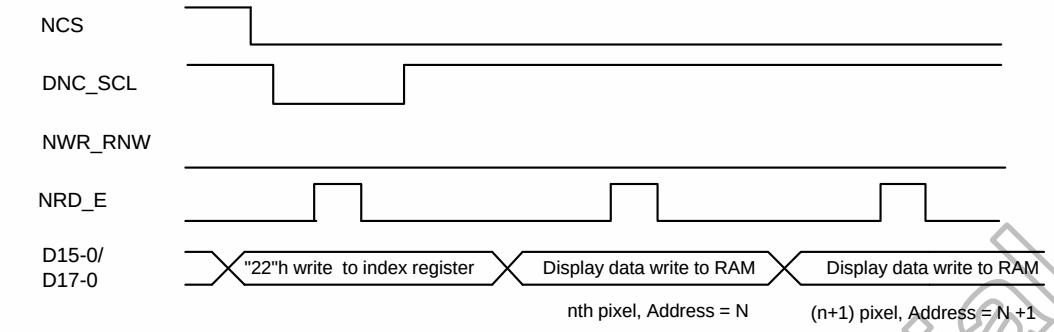
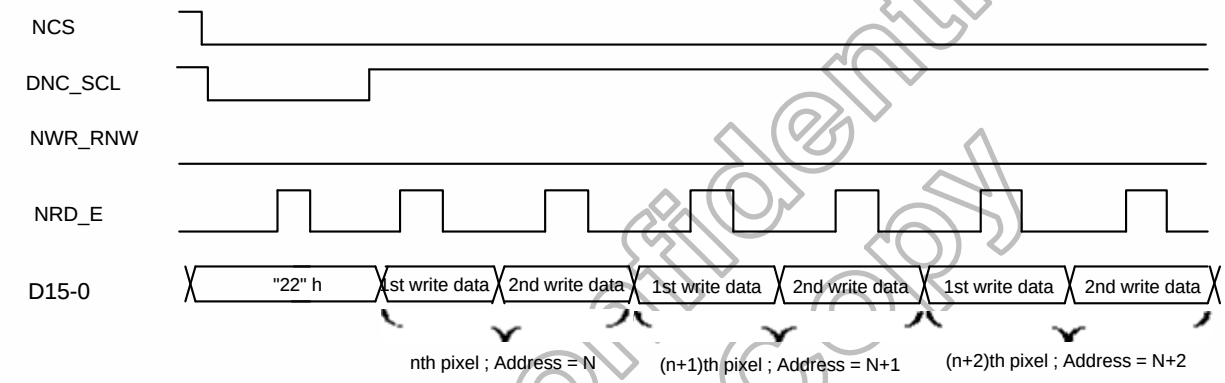


Figure 7. 11 Register read/write Timing in Parallel Bus System Interface (for M68 series MPU)

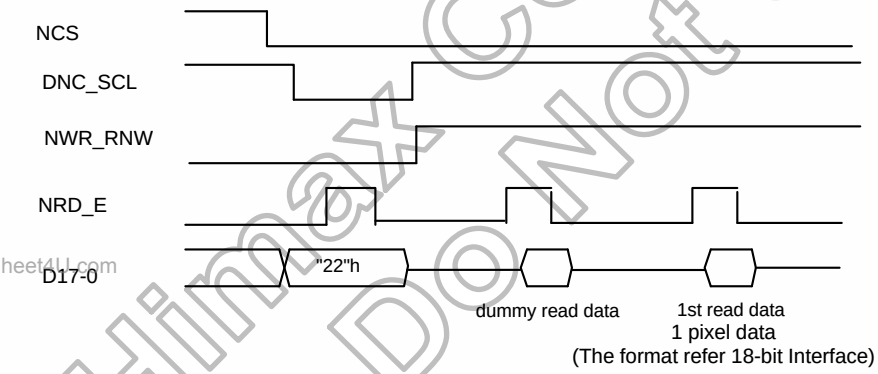
Write to the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)



Write to the graphic RAM (16+2-bit 262K Color)



Read the graphic RAM (18-bit bit 262K Color)



Read the graphic RAM (16-bit 65K/262K Color)

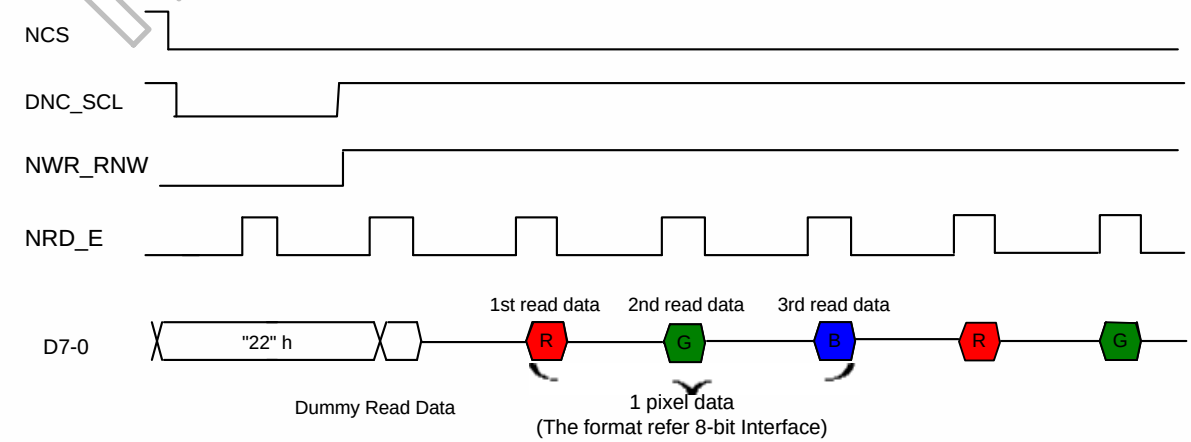
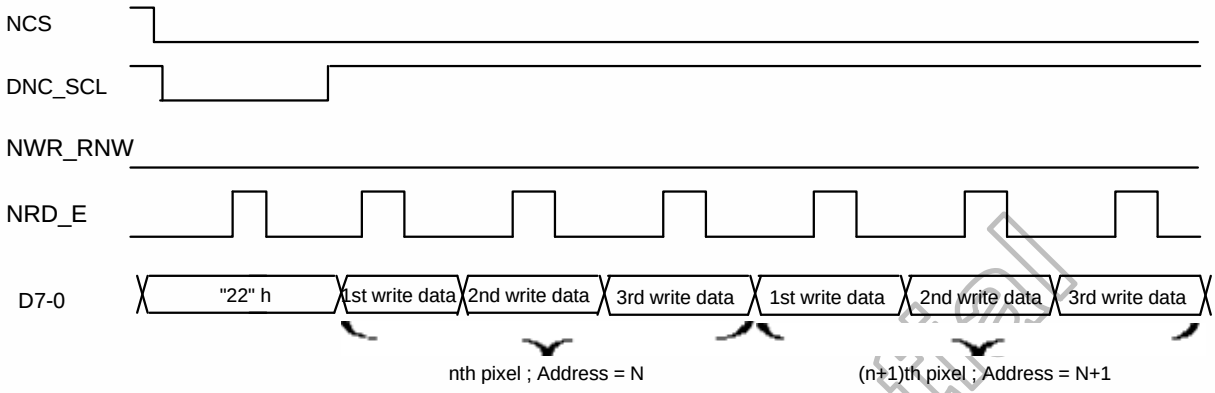


Figure 7. 12 GRAM read/write Timing in 16-/18-bit Parallel Bus System Interface (for M68 series MPU)

Write to the graphic RAM (8-bit 262K Color)



Read the graphic RAM (8-bit 262K Color)

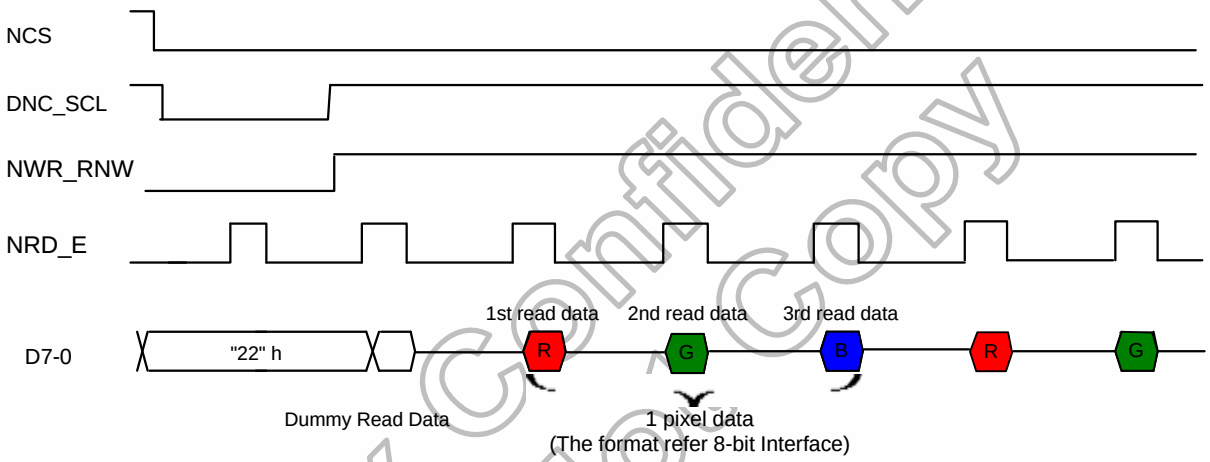


Figure 7. 13 GRAM read/write Timing in 8-bit Parallel Bus System Interface (for M68 series MPU)

7.4.3 Serial Data Transfer interface

RS	R/W	Function
0	0	Writes Indexes into IR
1	0	Writes command into register or data into GRAM
1	1	Reads command from register or data from GRAM

Table 7. 7 The Function of RS and R/W Bit bus

Serial Data Transfer interface Timing

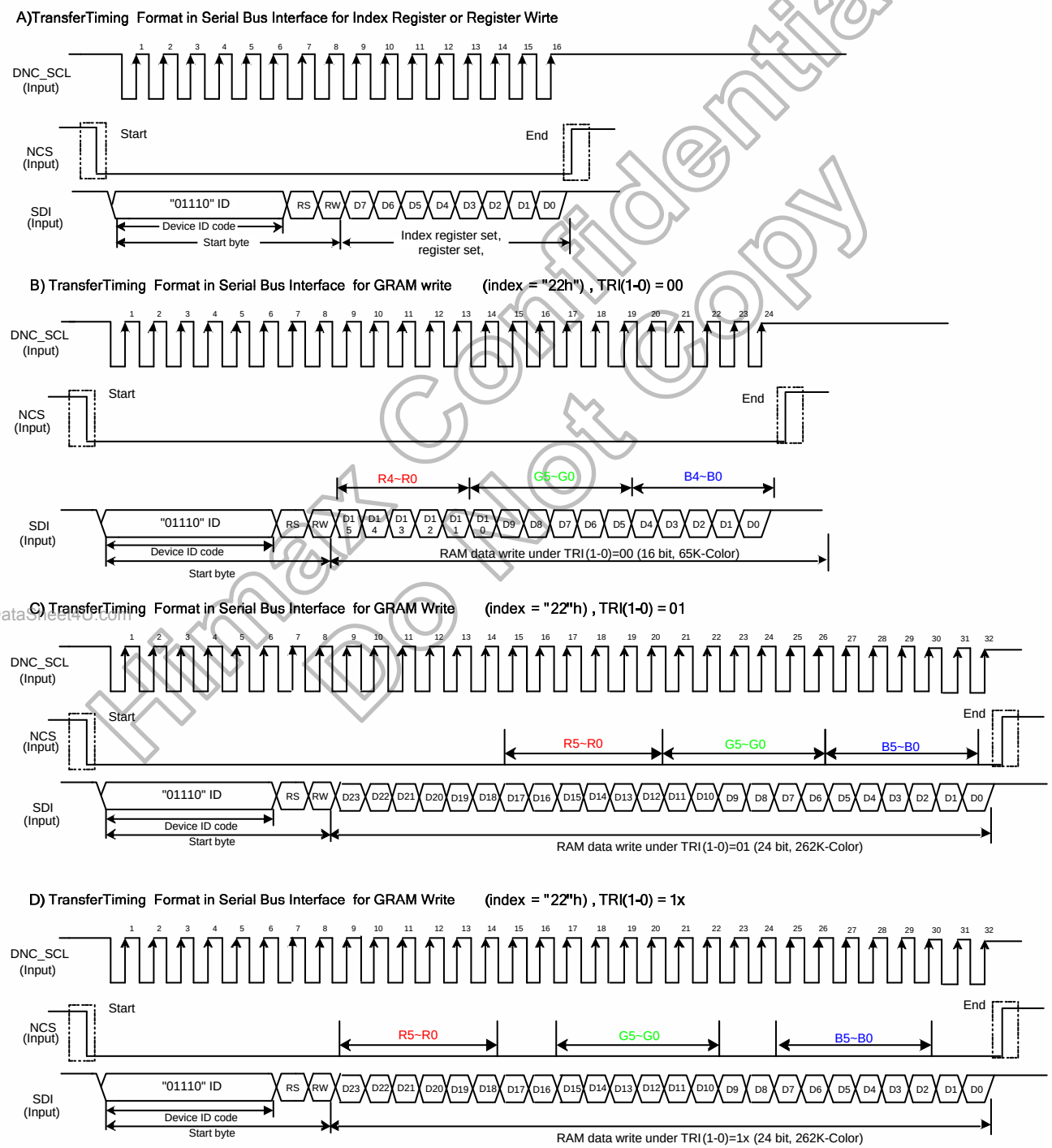
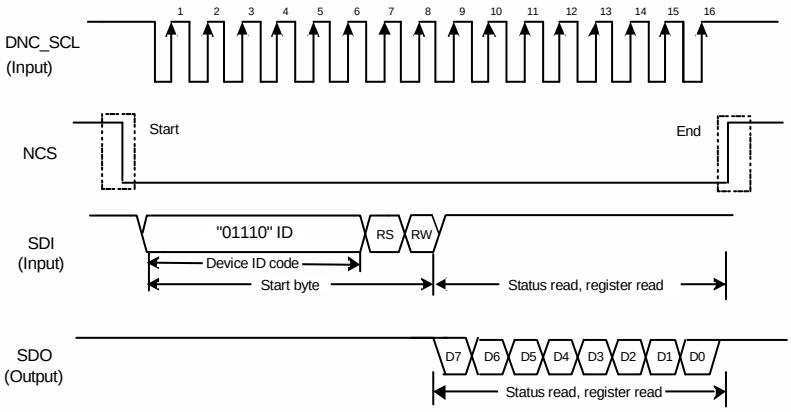
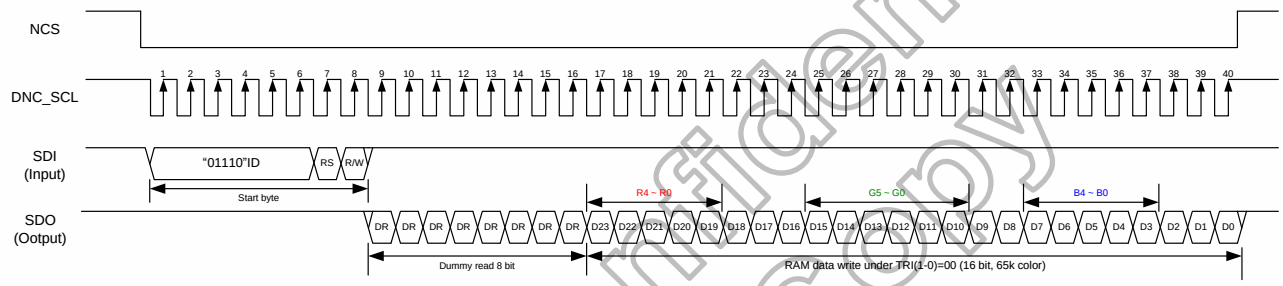


Figure 7. 14 Data Write Timing in Serial Bus System Interface

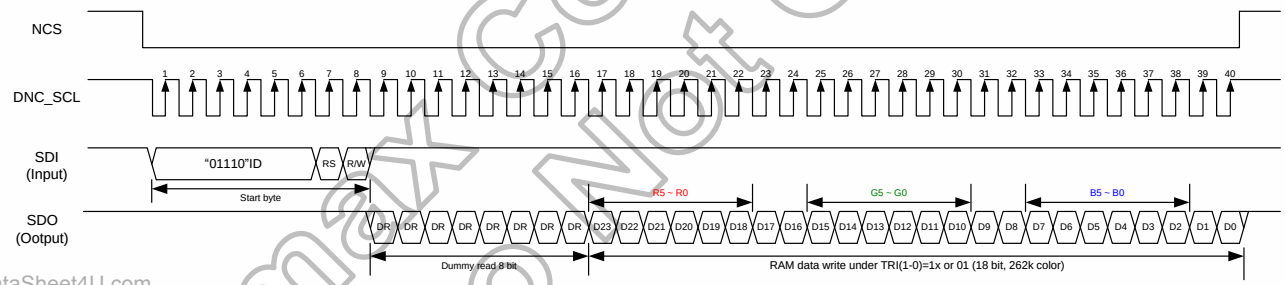
A)TransferTiming Format in Serial Bus Interface for Register Read



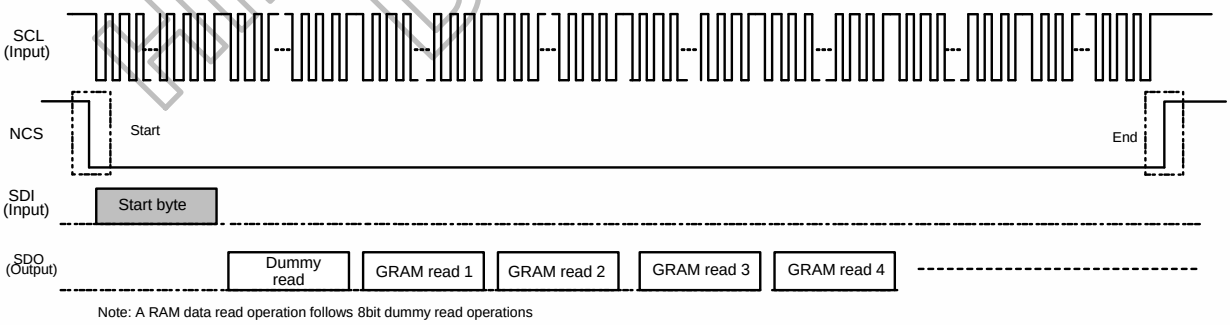
B) TransferTiming Format in Serial Bus Interface for GRAM Read (index = "22"h) , TRI(1-0) = 00



C) TransferTiming Format in Serial Bus Interface for GRAM Read (index = "22"h) , TRI(1-0) = 1x or 01



D) Timing Format of GRAM -Data Read



Note: A RAM data read operation follows 8bit dummy read operations

Figure 7. 15 Data Read Timing in Serial Bus System Interface

7.4.4 Command-Parameter Interface Mode

P68	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 7. 8 MPU selection in Command-Parameter Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of GRAM data	Transferring Method of Command
0	0	x	8-bit system interface	18-bit 262K-color (6 + 6 +6)	8-bit collective
0	1	x	16-bit system interface	18-bit 262K-color (6 + 6 + 6)	
1	1	ID	Serial interface	18-bit (6+6+6)	

X: Don't care.

Table 7. 9 Interface Selection in Command-Parameter Interface Mode

Operations	E_NWR	RW_NRD	DNC_SCL
Writes command code	0	1	0
Reads internal status	1	0	0
Writes parameter into command or data into GRAM	0	1	1
Reads parameter from command or data from GRAM	1	0	1

Table 7. 10 Data Pin Function for I80 Series CPU

Operations	E_NWR	RW_NRD	DNC_SCL
Writes command code	1	0	0
Reads internal status	1	1	0
Writes parameter into command or data into GRAM	1	0	1
Reads parameter from command or data from GRAM	1	1	1

Table 7. 11 Data Pin Function for M68 Series CPU

16-bit Parallel Bus System Interface

	DNC_SCL	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	x	x	x	x	x	x	x	x	GRAM Write command code (2Ch)								-
1 st write	1	R15	R14	R13	R12	R11	R10	x	x	G15	G14	G13	G12	G11	G10	x	x	-
2 nd write	1	B15	B14	B13	B12	B11	B10	x	x	R25	R24	R23	R22	R21	R20	x	x	1st pixel (R1/G1/B1)
3 rd write	1	G25	G24	G23	G22	G21	G20	x	x	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

X : Don't care

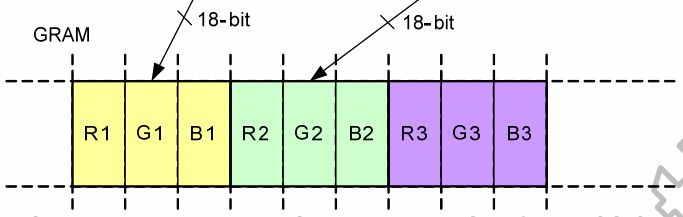


Figure 7. 16 GRAM Write Data Mapping for 16 bit interface

8-bit Parallel Bus System Interface

	DNC_SCL	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code (2Ch)								-
1st write	1	R15	R14	R13	R12	R11	R10	x	x	-
2nd write	1	G15	G14	G13	G12	G11	G10	x	x	-
3rd write	1	B15	B14	B13	B12	B11	B10	x	x	1st pixel (R1/G1/B1)
4th write	1	R25	R24	R23	R22	R21	R20	x	x	-
5th write	1	G25	G24	G23	G22	G21	G20	x	x	-
6th write	1	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

X : Don't care

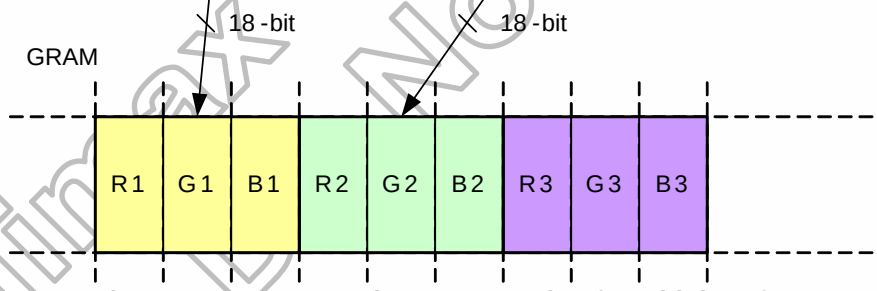


Figure 7. 17 GRAM Write Data Mapping for 8 bit interface

Command-Parameter Interface Mode Timing

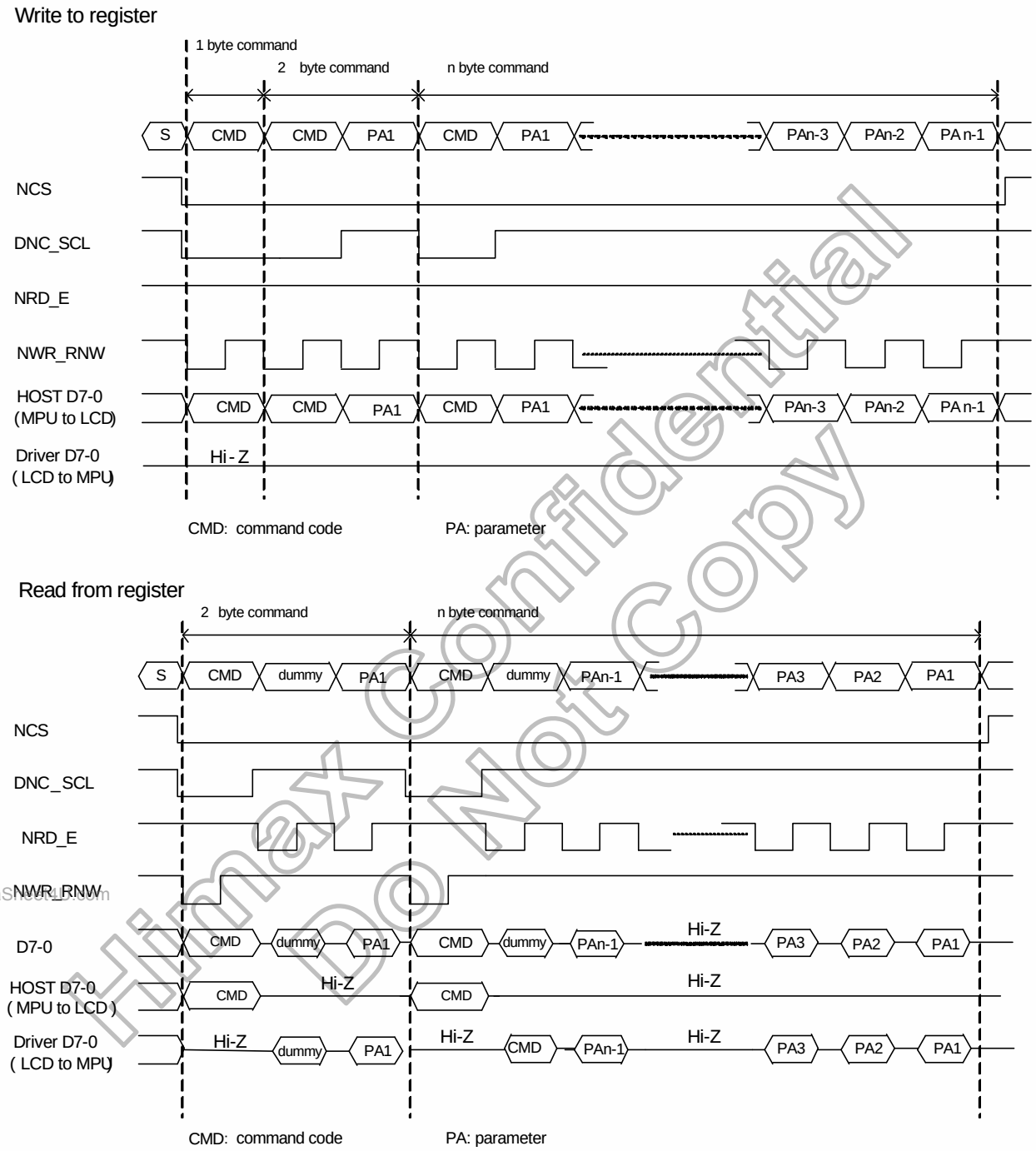
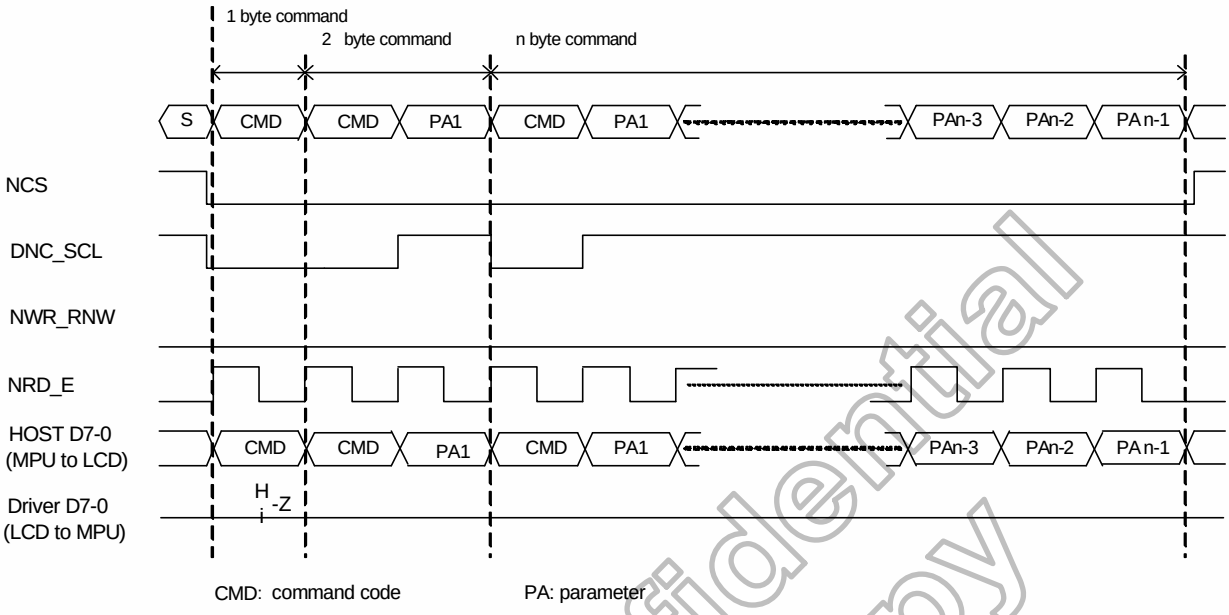


Figure 7. 18 Register Read/Write Timing in Parallel Bus System Interface (for I80 series MPU)

Write to register



Read from register

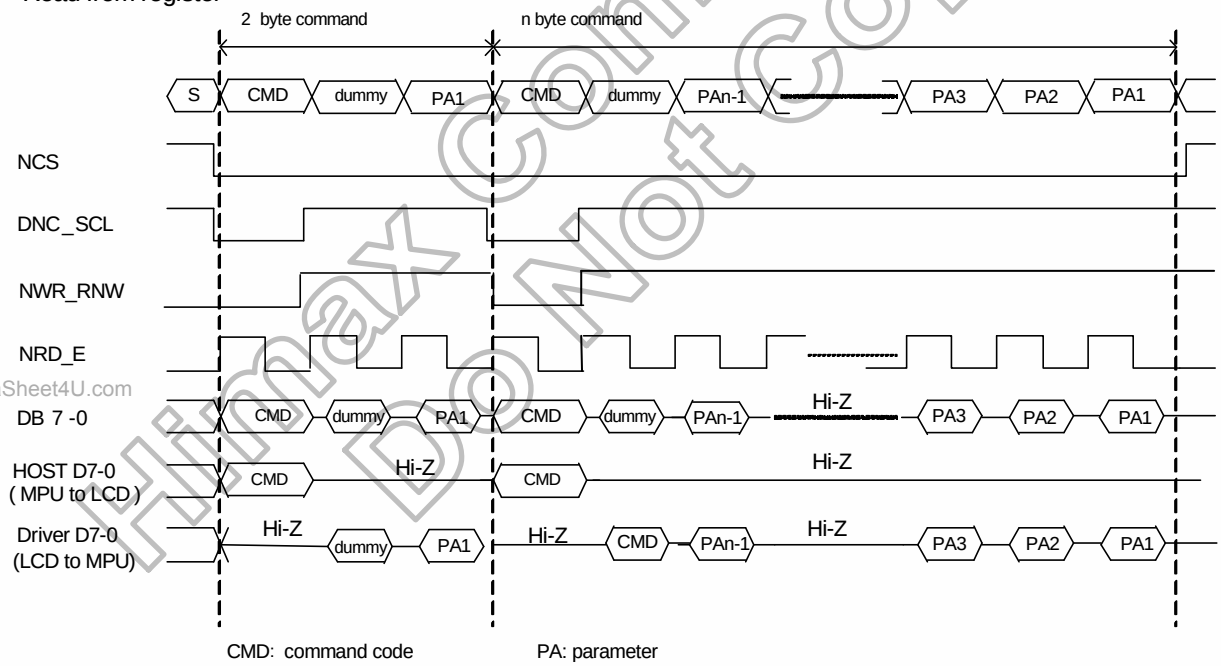


Figure 7. 19 Register read/write Timing in Parallel Bus System Interface (for M68 series MPU)

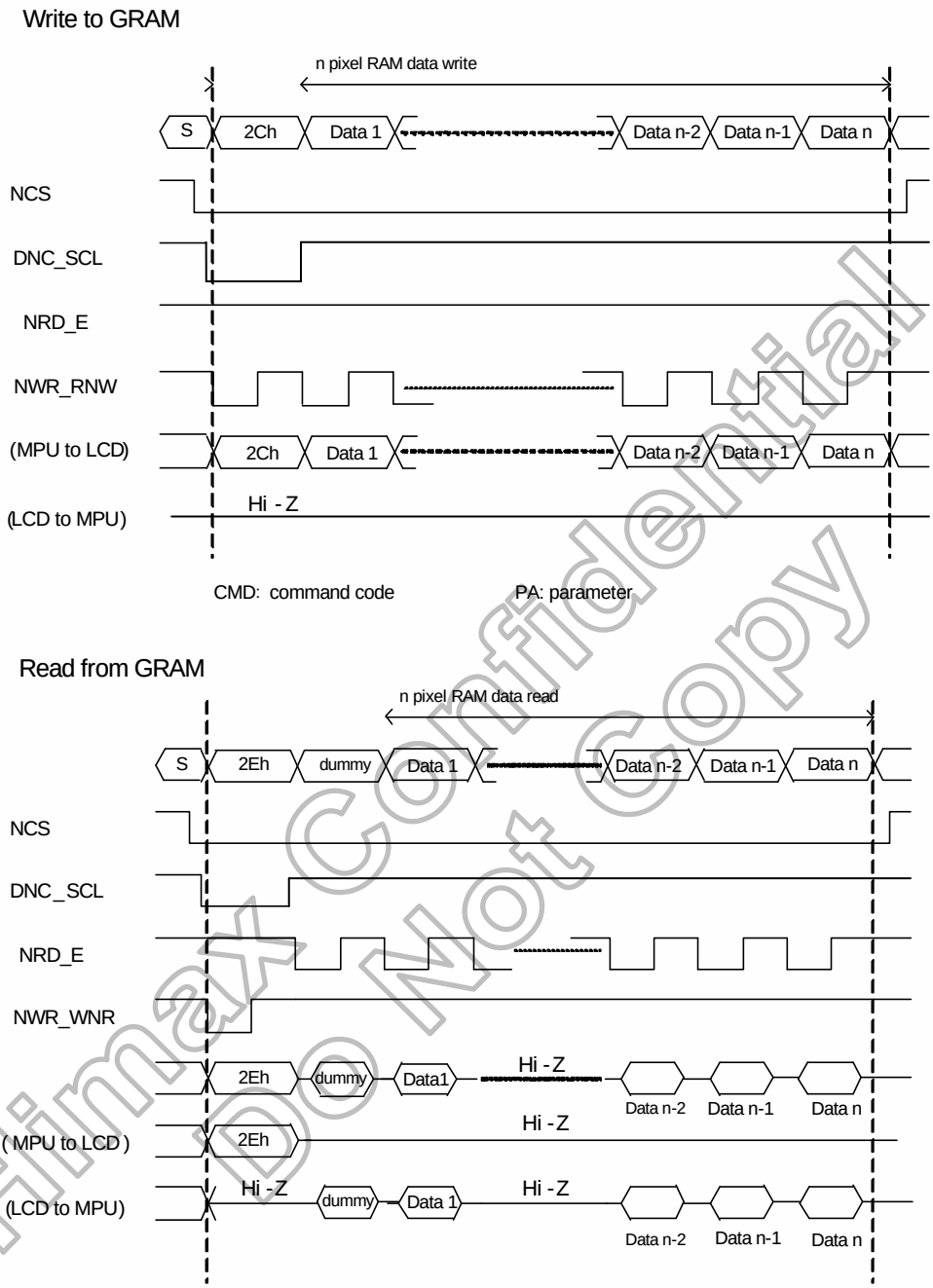


Figure 7. 20 GRAM Read/Write Timing in Parallel Bus System Interface (for I80 series MPU)

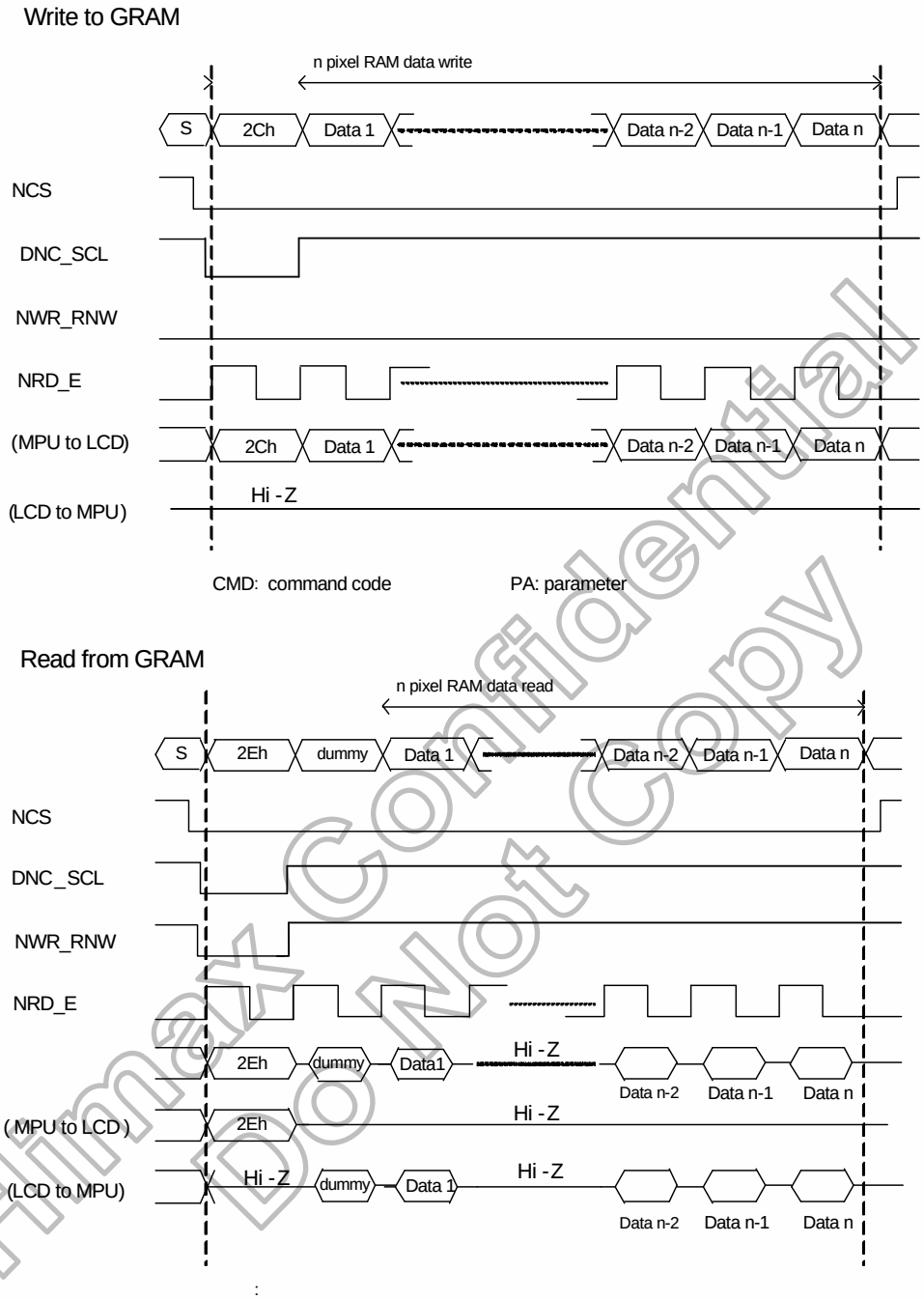


Figure 7. 21 GRAM Read/Write Timing in Parallel Bus System Interface (for M68 series MPU)

7.4.5 RGB Interface

EPL	ENABLE	Display
0	0	Disable
0	1	Enable
1	0	Enable
1	1	Disable

Table 7. 12 EPL bit Setting and Valid ENABLE Signal

RGB Interface Timing

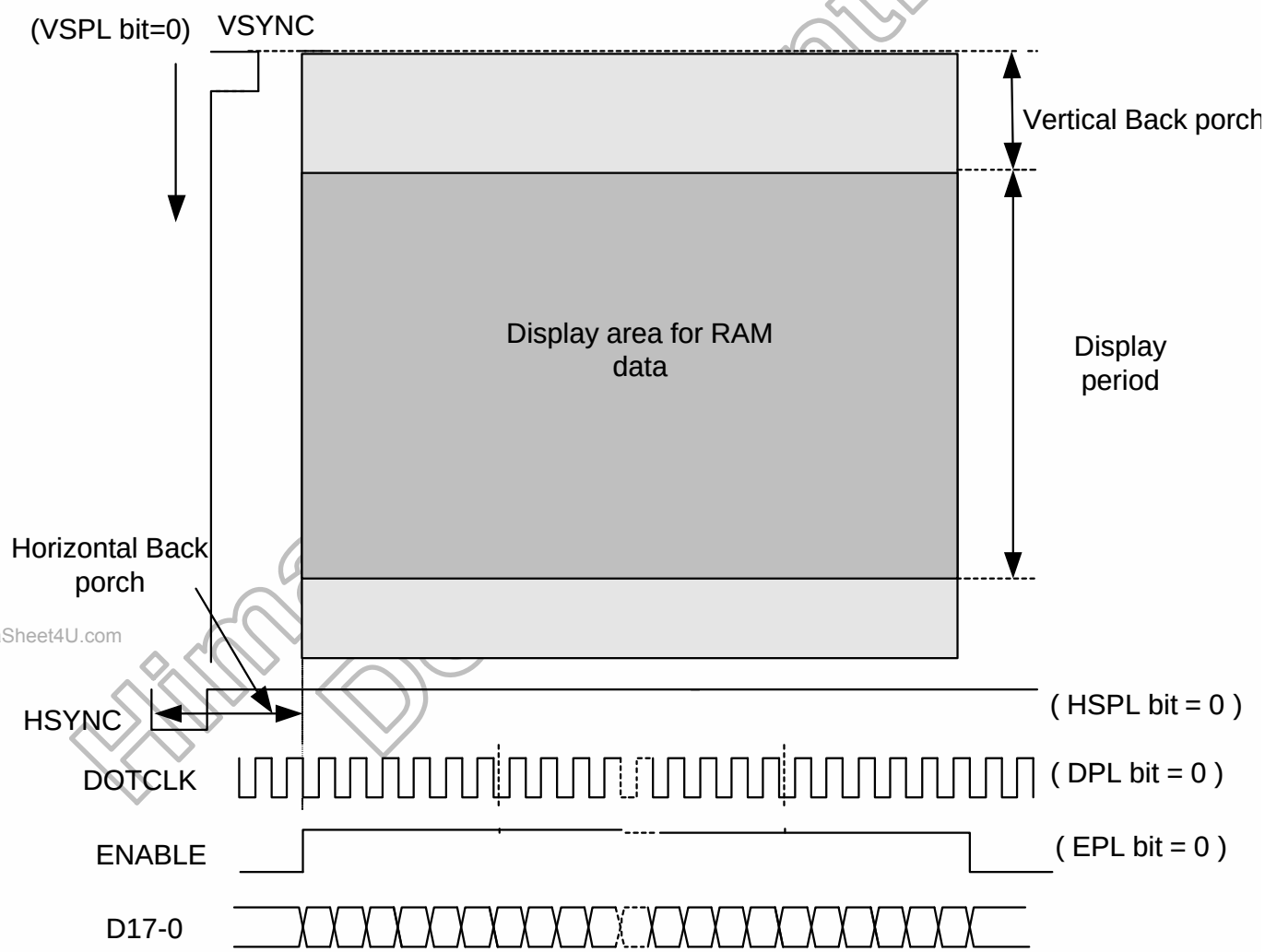


Figure 7. 22 RGB Interface Circuit Input Timing

(1) 18 bit/pixel color order (R 6-bit, G 6-bit, B 6-bit), 262,144 colors (CSEL(2-0) = "110")

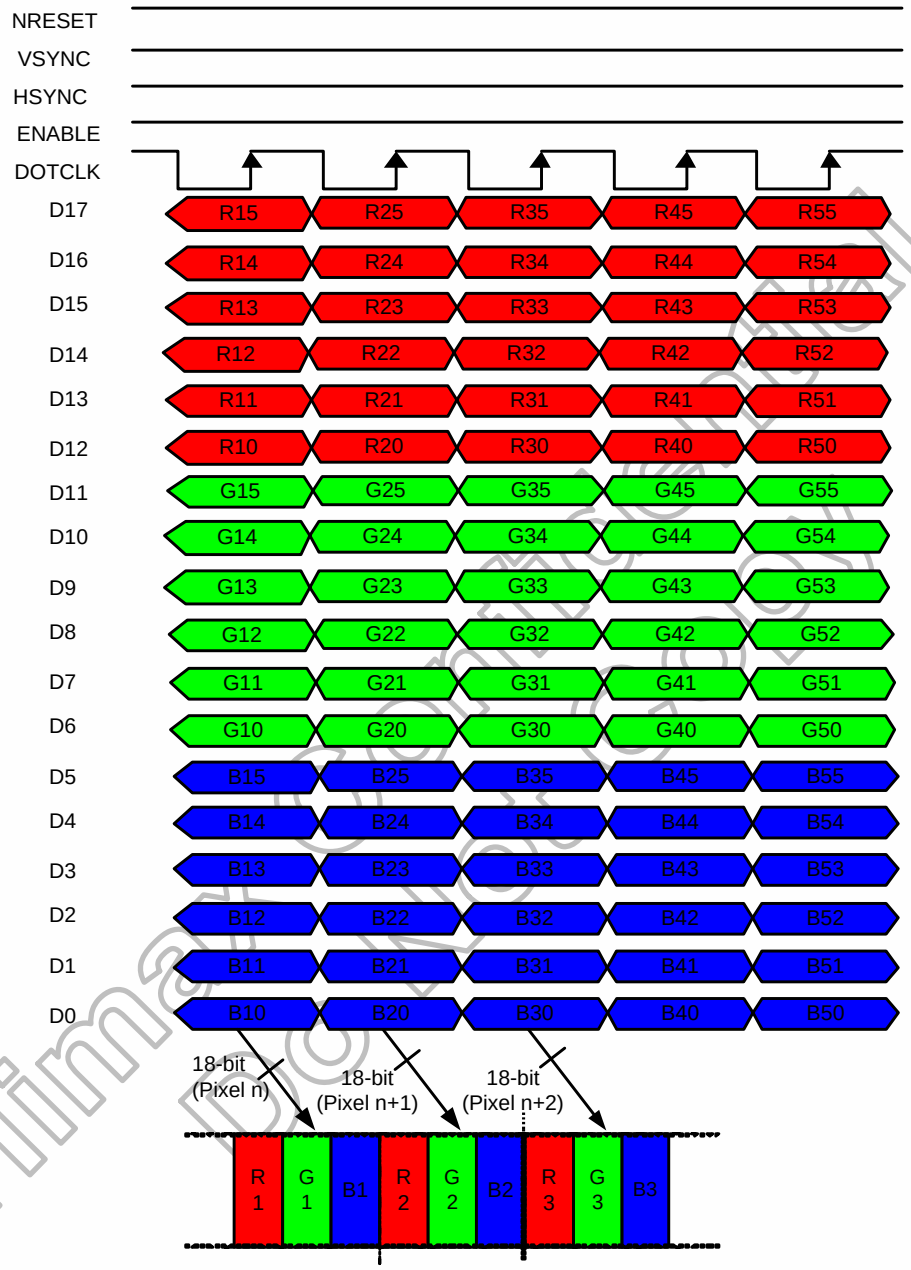


Figure 7. 23 18 bit / pixel Data Input of RGB Interface

(2) 16 bit/pixel color order (R 5-bit, G 6-bit, B 5-bit), 65,536 colors (CSEL(2-0) = "101")

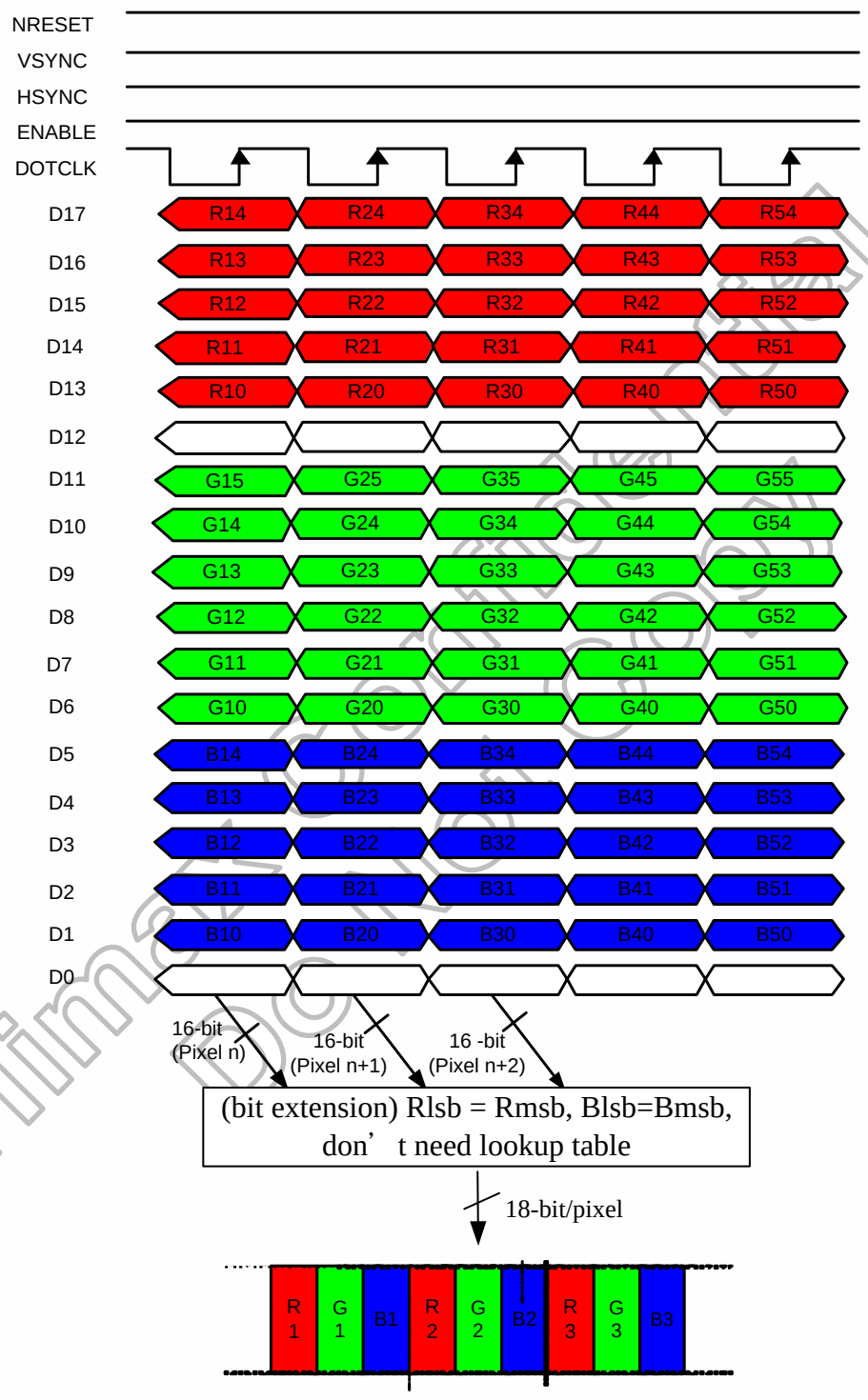


Figure 7. 24 16 bit / pixel Data Input of RGB Interface

7.5 Initial Procedure

7.5.1 Power Supply Setting Flow

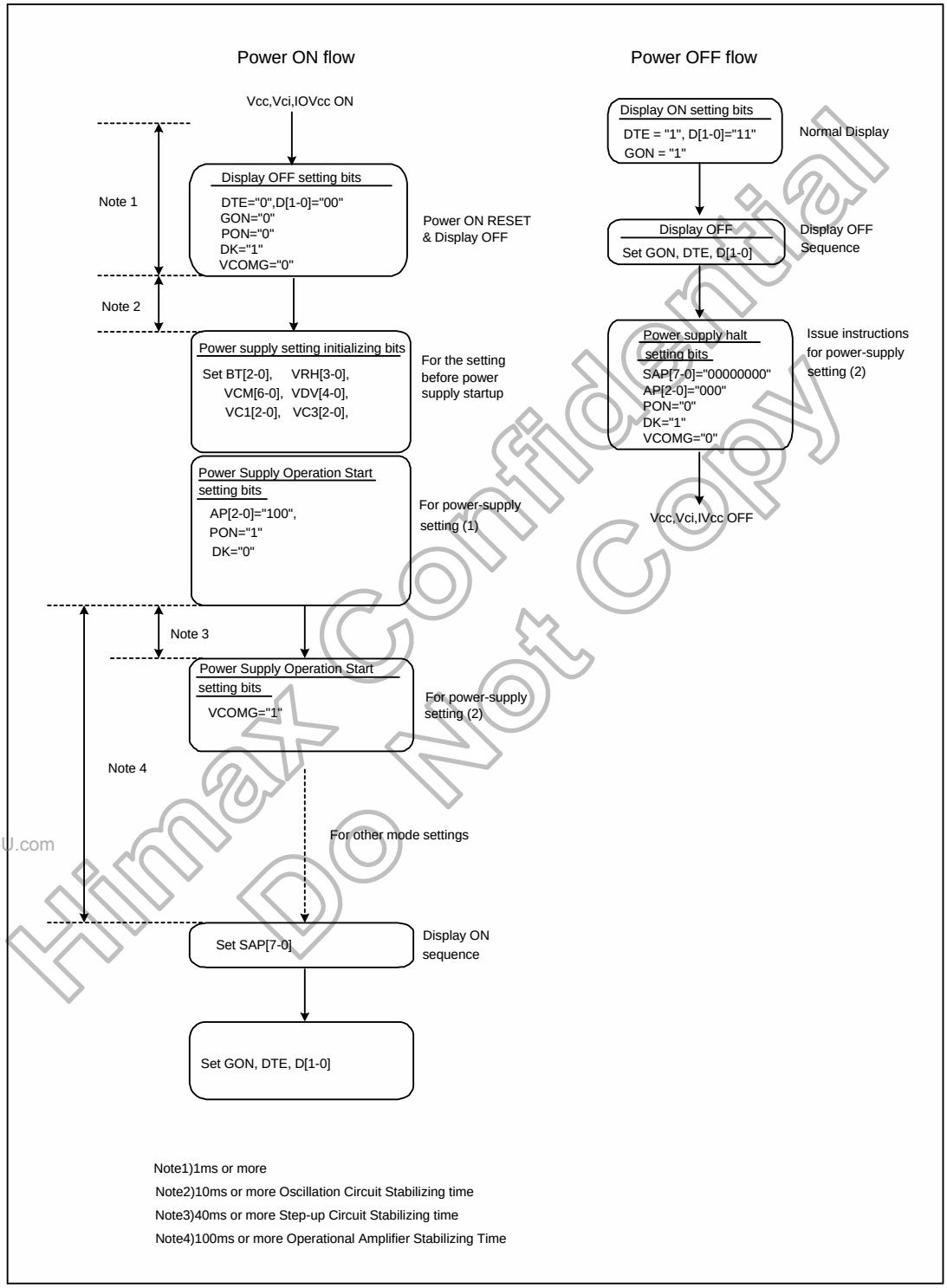


Figure 7. 25 Power Supply Setting Flow

7.5.2 Display on/off Setting Flow

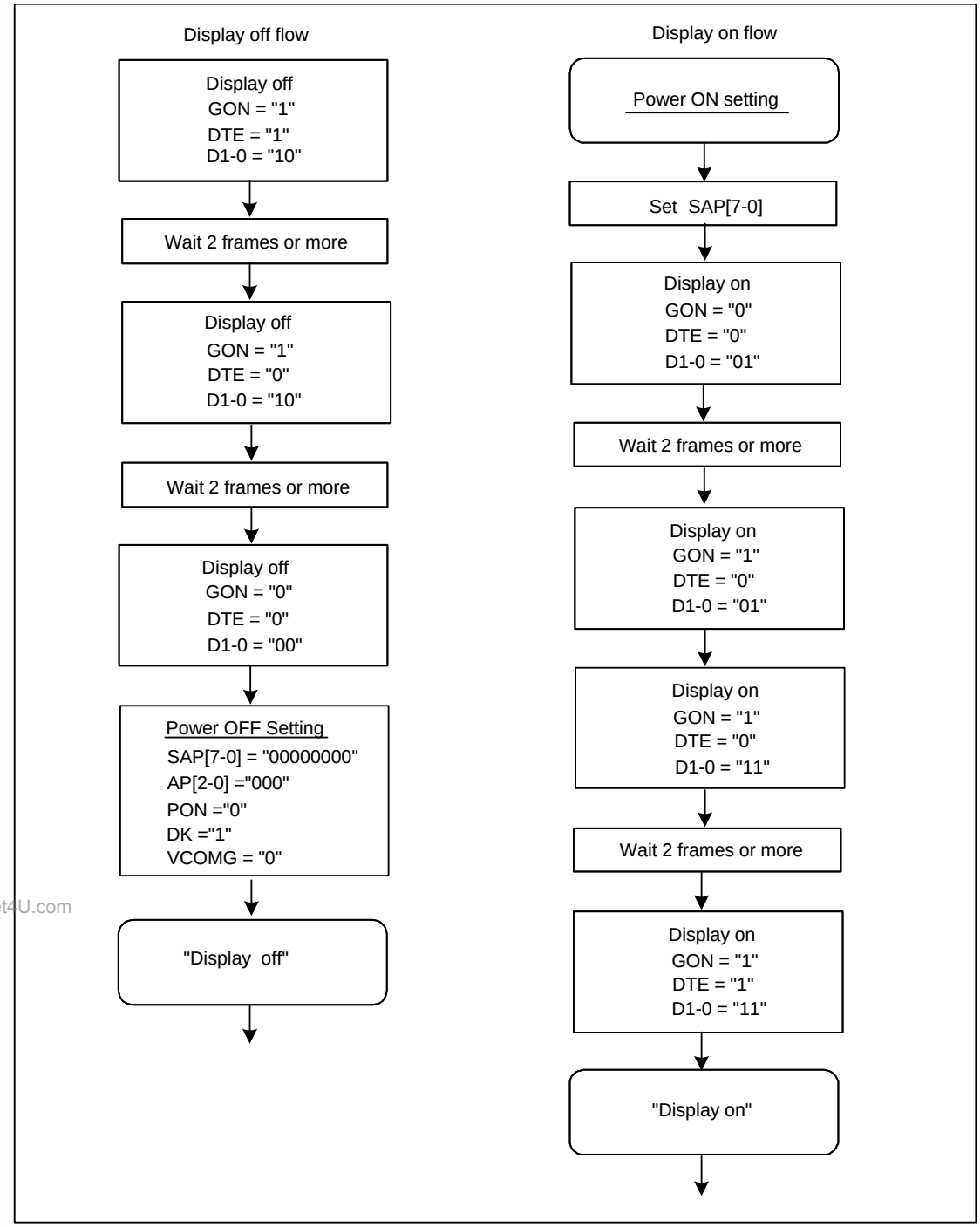


Figure 7. 26 Display On/Off Setting Flow

7.5.3 Standby Mode Setting Flow

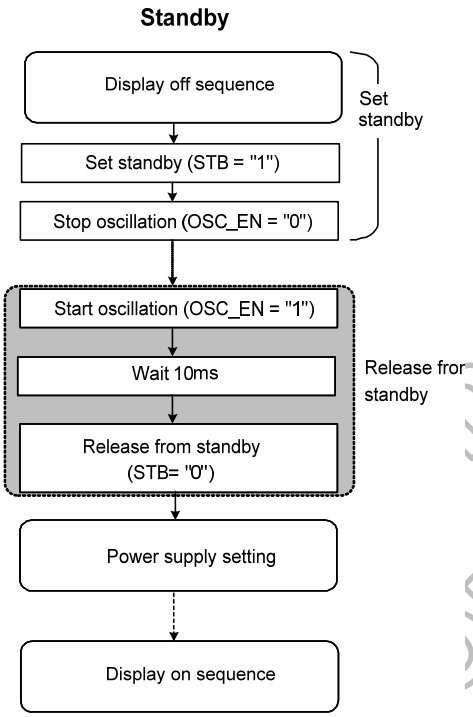


Figure 7. 27 Standby Mode Setting Flow

7.6 Initial code for reference

7.6.1 The reference setting of Normal Display for Command-Parameter Interface Mode

```
void HX8347_Init(void)
{

    RESET();
    DelayX1ms(150); // After Inter-MicroP Program (load OTP)

    Set_NOKIA_CMD(0x11);    // SLP out
    DelayX1ms(150);

    Set_NOKIA_CMD(0x29);    // Display on
    DelayX1ms(150);
}
```

7.6.2 The reference setting of Normal Display for Register-Content Interface Mode

7.6.2.1 The reference setting of CMO 3.2" Panel

void HX8347A_Init_CMO32(void)

```
{
      RESET();
     DelayX1ms(150);     // After Inter-MicroP Program (load OTP)

// Gamma for CMO 3.2"

     Set_LCD_8B_REG(0x0046,0x00A4);
    Set_LCD_8B_REG(0x0047,0x0053);
     Set_LCD_8B_REG(0x0048,0x0000);
     Set_LCD_8B_REG(0x0049,0x0044);
     Set_LCD_8B_REG(0x004A,0x0004);
     Set_LCD_8B_REG(0x004B,0x0067);
     Set_LCD_8B_REG(0x004C,0x0033);
     Set_LCD_8B_REG(0x004D,0x0077);
     Set_LCD_8B_REG(0x004E,0x0012);
     Set_LCD_8B_REG(0x004F,0x004C);
     Set_LCD_8B_REG(0x0050,0x0046);
     Set_LCD_8B_REG(0x0051,0x0044);

//240x320 window setting

     Set_LCD_8B_REG(0x0002,0x0000);     // Column address start2
     Set_LCD_8B_REG(0x0003,0x0000);     // Column address start1
     Set_LCD_8B_REG(0x0004,0x0000);     // Column address end2
     Set_LCD_8B_REG(0x0005,0x00EF);     // Column address end1
     Set_LCD_8B_REG(0x0006,0x0000);     // Row address start2
     Set_LCD_8B_REG(0x0007,0x0000);     // Row address start1
     Set_LCD_8B_REG(0x0008,0x0001);     // Row address end2
     Set_LCD_8B_REG(0x0009,0x003F);     // Row address end1

// Display Setting

     Set_LCD_8B_REG(0x0001,0x0006);     // IDMON=0, INVON=1, NORON=1, PTLON=0

     Set_LCD_8B_REG(0x0016,0x0048);     // MY=0, MX=0, MV=0, ML=1, BGR=0, TEON=0

    Set_LCD_8B_REG(0x38,0x00);       // RGB_EN=0, use MPU Interface

     Set_LCD_8B_REG(0x0023,0x0095);     // N_DC=1001 0101
     Set_LCD_8B_REG(0x0024,0x0095);     // PI_DC=1001 0101
     Set_LCD_8B_REG(0x0025,0x00FF);     // I_DC=1111 1111

     Set_LCD_8B_REG(0x0027,0x0002);     // N_BP=0000 0010
     Set_LCD_8B_REG(0x0028,0x0002);     // N_FP=0000 0010
     Set_LCD_8B_REG(0x0029,0x0002);     // PI_BP=0000 0010
     Set_LCD_8B_REG(0x002A,0x0002);     // PI_FP=0000 0010
     Set_LCD_8B_REG(0x002C,0x0002);     // I_BP=0000 0010
     Set_LCD_8B_REG(0x002D,0x0002);     // I_FP=0000 0010

     Set_LCD_8B_REG(0x003A,0x0001);     // N_RTN=0000, N_NW=001
     Set_LCD_8B_REG(0x003B,0x0000);     // PI_RTN=0000, PI_NW=000
```

```
Set_LCD_8B_REG(0x003C,0x00F0);     // I_RTN=1111, I_NW=000
Set_LCD_8B_REG(0x003D,0x0000);     // DIV=00
DelayX1ms(20);

Set_LCD_8B_REG(0x0035,0x0038);     // EQS=38h
Set_LCD_8B_REG(0x0036,0x0078);     // EQP=78h

Set_LCD_8B_REG(0x003E,0x0038);     // SON=38h

Set_LCD_8B_REG(0x0040,0x000F);     // GDON=0Fh
Set_LCD_8B_REG(0x0041,0x00F0);     // GDOFF
```

// Power Supply Setting

```
Set_LCD_8B_REG(0x0019,0x0049);     // CADJ=0100, CUADJ=100(FR:60Hz), OSD_EN=1
Set_LCD_8B_REG(0x0093,0x000F);     // RADJ=1111, 100%
DelayX1ms(10);

Set_LCD_8B_REG(0x0020,0x0040);      // BT=0100
Set_LCD_8B_REG(0x001D,0x0007);      // VC1=111
Set_LCD_8B_REG(0x001E,0x0000);      // VC3=000
Set_LCD_8B_REG(0x001F,0x0004);      // VRH=0100
```

// VCOM Setting for CMO 3.2” Panel

```
Set_LCD_8B_REG(0x0044,0x004D);      // VCM=100 1101
Set_LCD_8B_REG(0x0045,0x0011);      // VDV=1 0001
DelayX1ms(10);

Set_LCD_8B_REG(0x001C,0x0004);     // AP=100
DelayX1ms(20);
Set_LCD_8B_REG(0x001B,0x0018);     // GASENB=0, PON=1, DK=1, XDK=0, VLCD_TRI=0, STB=0
DelayX1ms(40);

Set_LCD_8B_REG(0x001B,0x0010);     // GASENB=0, PON=1, DK=0, XDK=0, VLCD_TRI=0, STB=0
DelayX1ms(40);

Set_LCD_8B_REG(0x0043,0x0080);     //Set VCOMG=1
DelayX1ms(100);
```

// Display ON Setting

```
Set_LCD_8B_REG(0x0090,0x007F);      // SAP=0111 1111

Set_LCD_8B_REG(0x0026,0x0004);     //GON=0, DTE=0, D=01
DelayX1ms(40);
Set_LCD_8B_REG(0x0026,0x0024);     //GON=1, DTE=0, D=01
Set_LCD_8B_REG(0x0026,0x002C);     //GON=1, DTE=0, D=11
DelayX1ms(40);

Set_LCD_8B_REG(0x0026,0x003C);     //GON=1, DTE=1, D=11
```

// Internal register setting

```
Set_LCD_8B_REG(0x0057,0x0002);     //Test_Mode Enable
Set_LCD_8B_REG(0x0095,0x0001);     // Set Display clock and Pumping clock to synchronize
Set_LCD_8B_REG(0x0057,0x0000);     // Test_Mode Disable

}
```

7.6.2.2 The reference setting of CMO 2.4" Panel

void HX8347A_Init_CMO24(void)

```
{
      RESET();
      DelayX1ms(150);     // After Inter-MicroP Program (load OTP)

// Gamma for CMO 2.4"

     Set_LCD_8B_REG(0x0046,0x0094);
     Set_LCD_8B_REG(0x0047,0x0041);
     Set_LCD_8B_REG(0x0048,0x0000);
     Set_LCD_8B_REG(0x0049,0x0033);
     Set_LCD_8B_REG(0x004A,0x0023);
     Set_LCD_8B_REG(0x004B,0x0045);
     Set_LCD_8B_REG(0x004C,0x0044);
     Set_LCD_8B_REG(0x004D,0x0077);
     Set_LCD_8B_REG(0x004E,0x0012);
     Set_LCD_8B_REG(0x004F,0x00CC);
     Set_LCD_8B_REG(0x0050,0x0046);
     Set_LCD_8B_REG(0x0051,0x0082);

//240x320 window setting

     Set_LCD_8B_REG(0x0002,0x0000);     // Column address start2
     Set_LCD_8B_REG(0x0003,0x0000);     // Column address start1
     Set_LCD_8B_REG(0x0004,0x0000);     // Column address end2
     Set_LCD_8B_REG(0x0005,0x00EF);     // Column address end1
     Set_LCD_8B_REG(0x0006,0x0000);     // Row address start2
     Set_LCD_8B_REG(0x0007,0x0000);     // Row address start1
     Set_LCD_8B_REG(0x0008,0x0001);     // Row address end2
     Set_LCD_8B_REG(0x0009,0x003F);     // Row address end1

// Display Setting

     Set_LCD_8B_REG(0x0001,0x0006);     // IDMON=0, INVON=1, NORON=1, PTLON=0

     Set_LCD_8B_REG(0x0016,0x0048);     // MY=0, MX=0, MV=0, ML=1, BGR=0, TEON=0

     Set_LCD_8B_REG(0x38,0x00);       // RGB_EN=0, use MPU Interface

     Set_LCD_8B_REG(0x0023,0x0095);     // N_DC=1001 0101
     Set_LCD_8B_REG(0x0024,0x0095);     // PI_DC=1001 0101
     Set_LCD_8B_REG(0x0025,0x00FF);     // I_DC=1111 1111

     Set_LCD_8B_REG(0x0027,0x0002);     // N_BP=0000 0010
     Set_LCD_8B_REG(0x0028,0x0002);     // N_FP=0000 0010
     Set_LCD_8B_REG(0x0029,0x0002);     // PI_BP=0000 0010
     Set_LCD_8B_REG(0x002A,0x0002);     // PI_FP=0000 0010
     Set_LCD_8B_REG(0x002C,0x0002);     // I_BP=0000 0010
     Set_LCD_8B_REG(0x002D,0x0002);     // I_FP=0000 0010

     Set_LCD_8B_REG(0x003A,0x0001);     // N_RTN=0000, N_NW=001
     Set_LCD_8B_REG(0x003B,0x0000);     // PI_RTN=0000, PI_NW=000
     Set_LCD_8B_REG(0x003C,0x00F0);     // I_RTN=1111, I_NW=000
     Set_LCD_8B_REG(0x003D,0x0000);     // DIV=00
     DelayX1ms(20);
```

```
    Set_LCD_8B_REG(0x0035,0x0038);     // EQS=38h
    Set_LCD_8B_REG(0x0036,0x0078);     // EQP=78h

    Set_LCD_8B_REG(0x003E,0x0038);     // SON=38h

    Set_LCD_8B_REG(0x0040,0x000F);     // GDON=0Fh
    Set_LCD_8B_REG(0x0041,0x00F0);     // GDOFF

// Power Supply Setting

    Set_LCD_8B_REG(0x0019,0x0049);     // CADJ=0100, CUADJ=100(FR:60Hz),, OSD_EN=1
    Set_LCD_8B_REG(0x0093,0x000F);     // RADJ=1111, 100%
    DelayX1ms(10);

    Set_LCD_8B_REG(0x0020,0x0040);      // BT=0100
    Set_LCD_8B_REG(0x001D,0x0007);      // VC1=111
    Set_LCD_8B_REG(0x001E,0x0000);      // VC3=000
    Set_LCD_8B_REG(0x001F,0x0004);      // VRH=0100

// VCOM Setting for CMO 2.4" Panel

    Set_LCD_8B_REG(0x0044,0x0040);      // VCM=100 0000
    Set_LCD_8B_REG(0x0045,0x0012);      // VDV=1 0001
    DelayX1ms(10);

    Set_LCD_8B_REG(0x001C,0x0004);     // AP=100
    DelayX1ms(20);
    Set_LCD_8B_REG(0x001B,0x0018);     // GASENB=0, PON=1, DK=1, XDK=0, VLCD_TRI=0, STB=0
    DelayX1ms(40);

    Set_LCD_8B_REG(0x001B,0x0010);     // GASENB=0, PON=1, DK=0, XDK=0, VLCD_TRI=0, STB=0
    DelayX1ms(40);

    Set_LCD_8B_REG(0x0043,0x0080);     //Set VCOMG=1
    DelayX1ms(100);

// Display ON Setting

    Set_LCD_8B_REG(0x0090,0x007F);      // SAP=0111 1111

    Set_LCD_8B_REG(0x0026,0x0004);     //GON=0, DTE=0, D=01
    DelayX1ms(40);
    Set_LCD_8B_REG(0x0026,0x0024);     //GON=1, DTE=0, D=01
    Set_LCD_8B_REG(0x0026,0x002C);     //GON=1, DTE=0, D=11
    DelayX1ms(40);

    Set_LCD_8B_REG(0x0026,0x003C);     //GON=1, DTE=1, D=11

// Internal register setting

    Set_LCD_8B_REG(0x0057,0x0002);     //Test_Mode Enable
    Set_LCD_8B_REG(0x0095,0x0001);     // Set Display clock and Pumping clock to synchronize
    Set_LCD_8B_REG(0x0057,0x0000);     // Test_Mode Disable

}
```

7.6.2.3 The reference setting of CMO 2.8” Panel

void HX8347A_Init_CMO28(void)

```
{
      RESET();
     DelayX1ms(150);     // After Inter-MicroP Program (load OTP)

// Gamma for CMO 2.8

    Set_LCD_8B_REG(0x46,0x95);
    Set_LCD_8B_REG(0x47,0x51);
    Set_LCD_8B_REG(0x48,0x00);
    Set_LCD_8B_REG(0x49,0x36);
    Set_LCD_8B_REG(0x4A,0x11);
    Set_LCD_8B_REG(0x4B,0x66);
    Set_LCD_8B_REG(0x4C,0x14);
    Set_LCD_8B_REG(0x4D,0x77);
    Set_LCD_8B_REG(0x4E,0x13);
    Set_LCD_8B_REG(0x4F,0x4C);
    Set_LCD_8B_REG(0x50,0x46);
    Set_LCD_8B_REG(0x51,0x46);

//240x320 window setting

    Set_LCD_8B_REG(0x02,0x00);      // Column address start2
    Set_LCD_8B_REG(0x03,0x00);      // Column address start1
    Set_LCD_8B_REG(0x04,0x00);      // Column address end2
    Set_LCD_8B_REG(0x05,0xEF);      // Column address end1
    Set_LCD_8B_REG(0x06,0x00);      // Row address start2
    Set_LCD_8B_REG(0x07,0x00);      // Row address start1
    Set_LCD_8B_REG(0x08,0x01);      // Row address end2
    Set_LCD_8B_REG(0x09,0x3F);      // Row address end1

// Display Setting

    Set_LCD_8B_REG(0x01,0x06);      // IDMON=0, INVON=1, NORON=1, PTLON=0

    Set_LCD_8B_REG(0x16,0x48);       // MY=0, MX=0, MV=0, ML=1, BGR=0, TEON=0

    Set_LCD_8B_REG(0x38,0x00);      // RGB_EN=0, use MPU Interface

    Set_LCD_8B_REG(0x23,0x95);      // N_DC=1001 0101
    Set_LCD_8B_REG(0x24,0x95);      // P_DC=1001 0101
    Set_LCD_8B_REG(0x25,0xFF);      // I_DC=1111 1111

    Set_LCD_8B_REG(0x27,0x06);      // N_BP=0000 0110
    Set_LCD_8B_REG(0x28,0x06);      // N_FP=0000 0110
    Set_LCD_8B_REG(0x29,0x06);      // P_BP=0000 0110
    Set_LCD_8B_REG(0x2A,0x06);      // P_FP=0000 0110
    Set_LCD_8B_REG(0x2C,0x06);      // I_BP=0000 0110
    Set_LCD_8B_REG(0x2D,0x06);      // I_FP=0000 0110

    Set_LCD_8B_REG(0x3A,0x01);      // N_RTN=0000, N_NW=001
    Set_LCD_8B_REG(0x3B,0x00);      // P_RTN=0000, P_NW=000
    Set_LCD_8B_REG(0x3C,0xF0);      // I_RTN=1111, I_NW=000
    Set_LCD_8B_REG(0x3D,0x00);      // DIV=00
    DelayX1ms(20);
```

```
    Set_LCD_8B_REG(0x35,0x38);      // EQS=38h
    Set_LCD_8B_REG(0x36,0x78);      // EQP=78h

    Set_LCD_8B_REG(0x3E,0x38);      // SON=38h

    Set_LCD_8B_REG(0x40,0x0F);      // GDON=0Fh
    Set_LCD_8B_REG(0x41,0xF0);      // GDOFF

// Power Supply Setting

    Set_LCD_8B_REG(0x19,0x49);      // OSCADJ=10 0000, OSD_EN=1 //60Hz
    Set_LCD_8B_REG(0x93,0x0C);      // RADJ=1100
    DelayX1ms(10);

    Set_LCD_8B_REG(0x20,0x40);      // BT=0100

    Set_LCD_8B_REG(0x1D,0x07);      // VC1=111
    Set_LCD_8B_REG(0x1E,0x00);      // VC3=000
    Set_LCD_8B_REG(0x1F,0x04);      // VRH=0100

// VCOM Setting for CMO 2.8" Panel

    Set_LCD_8B_REG(0x44,0x4D);      // VCM=101 0000
    Set_LCD_8B_REG(0x45,0x11);      // VDV=1 0001
    DelayX1ms(10);

    Set_LCD_8B_REG(0x1C,0x04);      // AP=100
    DelayX1ms(20);

    Set_LCD_8B_REG(0x1B,0x18);      // GASENB=0, PON=1, DK=1, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(40);

    Set_LCD_8B_REG(0x1B,0x10);      // GASENB=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(40);

    Set_LCD_8B_REG(0x43,0x80);      //Set VCOMG=1
    DelayX1ms(100);

// Display ON Setting

    Set_LCD_8B_REG(0x90,0x7F);      // SAP=0111 1111

    Set_LCD_8B_REG(0x26,0x04);      //GON=0, DTE=0, D=01
    DelayX1ms(40);
    Set_LCD_8B_REG(0x26,0x24);      //GON=1, DTE=0, D=01
    Set_LCD_8B_REG(0x26,0x2C);      //GON=1, DTE=0, D=11
    DelayX1ms(40);

    Set_LCD_8B_REG(0x26,0x3C);      //GON=1, DTE=1, D=11

// Internal register setting

    Set_LCD_8B_REG(0x0057,0x0002);  //Test_Mode Enable
    Set_LCD_8B_REG(0x0095,0x0001);  // Set Display clock and Pumping clock to synchronize
    Set_LCD_8B_REG(0x0057,0x0000);  // Test_Mode Disable

}
```

7.6.3 The reference setting of into Standby mode for Register-Content Interface Mode

void HX8347A_STB_INTO (void)

```
{

// Display Off

        Set_LCD_8B_REG(0x0026,0x0038);      //GON=1, DTE=1, D=10
        DelayX1ms (40);
        Set_LCD_8B_REG(0x0026,0x0028);      //GON=1, DTE=0, D=10
        DelayX1ms (40);
        Set_LCD_8B_REG(0x0026,0x0000);      //GON=0, DTE=0, D=00

// Power Off

        Set_LCD_8B_REG(0x0043,0x0000);      // VCOMG=0
        DelayX1ms(10);
        Set_LCD_8B_REG(0x001B,0x0000);      // GASENB=0, PON=0, DK=0, XDK=0,
                                            // VLCD_TRI=0, STB=0
        DelayX1ms(10);
        Set_LCD_8B_REG(0x001B,0x0008);      // GASENB=0, PON=0, DK=1, XDK=0,
                                            // VLCD_TRI=0, STB=0
        DelayX1ms(10);
        Set_LCD_8B_REG(0x001C,0x0000);      // AP=000
        DelayX1ms(10);
        Set_LCD_8B_REG(0x0090,0x0000);      // SAP=00000000
        DelayX1ms(10);

// Into STB mode

        Set_LCD_8B_REG(0x001B,0x0009);      // GASSENB=0, PON=0, DK=1, XDK=0,
                                            // VLCD_TRI=0, STB=1
        DelayX1ms(10);

// Stop Oscillation

        Set_LCD_8B_REG(0x0019,0x0048);      // CADJ=0100, CUADJ=100, OSD_EN=0

}
```

7.6.4 The reference setting of exit Standby mode for Register-Content Interface Mode

```
void HX8347A_STB_EXIT (void)
{

// Start Oscillation

        Set_LCD_8B_REG(0x0019,0x0049);      // OSCADJ=100 010(FR:60Hz), OSD_EN=1
        DelayX1ms(10);

// Exit STB mode

        Set_LCD_8B_REG(0x001B,0x0008);      // NIDSENB=0, PON=0, DK=1, XDK=0,
                                            // VLCD_TRI=0, STB=0

// Power Supply Setting

        Set_LCD_8B_REG(0x0020,0x0040);      // BT=0100
        Set_LCD_8B_REG(0x001D,0x0007);      // VC1=111
        Set_LCD_8B_REG(0x001E,0x0000);      // VC3=000
        Set_LCD_8B_REG(0x001F,0x0003);      // VRH=0011
        Set_LCD_8B_REG(0x0044,0x0020);      // VCM=010 0000
        Set_LCD_8B_REG(0x0045,0x000E);      // VDV=0 1110
        DelayX1ms(10);
        Set_LCD_8B_REG(0x001C,0x0004);      // AP=100
        DelayX1ms(20);
        Set_LCD_8B_REG(0x001B,0x0018);      // NIDSENB=0, PON=1, DK=1, XDK=0,
                                            // VLCD_TRI=0, STB=0
        DelayX1ms(40);
        Set_LCD_8B_REG(0x001B,0x0010);      // NIDSENB=0, PON=1, DK=0, XDK=0,
                                            // VLCD_TRI=1, STB=0
        DelayX1ms(40);
        Set_LCD_8B_REG(0x0043,0x0080);      // VCOMG=1
        DelayX1ms(100);

// Display ON Setting

        Set_LCD_8B_REG(0x0090,0x007F);      // SAP=01111111
        DelayX1ms(40);

        Set_LCD_8B_REG(0x0026,0x0004);      //GON=0, DTE=0, D=01
        DelayX1ms(40);
        Set_LCD_8B_REG(0x0026,0x0024);      //GON=1, DTE=0, D=01
        Set_LCD_8B_REG(0x0026,0x002C);      //GON=1, DTE=0, D=11
        DelayX1ms(40);

        Set_LCD_8B_REG(0x0026,0x003C);      //GON=1, DTE=1, D=11

}
```

8. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2007/04/24	New setup
	2007/05/22	1. Update Table 7.7.(P.33) 2. Update 5. HX8347-A Reference FPC circuit for CMO 3.2" LCD Panel.(P.13~P.16)
	2007/06/05	1. Update Initial code for Normal Display in Register-Content Interface mode.(P.48~P.49) 2. Add Normal Display Initial code for CMO 2.4" LCD in Register-Content Interface mode.(P.50~P51) 3. Modify Pin name in Figure 7.8~7.15 and . Figure 7.18~7.21.(P.21~P.40) 4. Modify SPI read GRAM timing.(P.33~P.34)
	2007/06/28	1. Update Initial code for Normal Display in Register-Content Interface mode. (Add VDC_SEL setting). (P.48~P.53) 2. Modify IOVCC input voltage range from 3.0V to 3.3V. (P.13~P.16)
	2007/07/25	1. Update Initial code for ESD protection in Register-Content Interface mode.(P.48~P.53)
	2007/07/26	1. Update Initial code. (P.48~P.53)
	2007/08/16	1. Add Normal Display Initial code for CMO 2.8" LCD in Register-Content Interface mode.(P.52~P.53) 2. Add Register R95h command for setting Display clock and Pumping clock to synchronize(P.48~P.53)
	2007/08/21	1. Update Reference FPC circuit.(P.13~P.16)
	2007/09/06	1. Update Initial code.(P.48~P.53)
02	2007/10/13	1. Update Reference FPC circuit.(P.13~P.16)
	2008/03/18	1. Add Register R38h command for Normal Display Initial code in Register-Content Interface mode.(P.48~P.53) 2. Remove Schottky Diode(D1, D3) and Capacitor(C1, C2) in 8. Reference Applications.(P.13~P.17)