DATA SHEET

(DOC No. HX8347-B-DS)

HX8347-B

240RGB x 320 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 December, 2009

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This document describes HX8347-B 240RGBx320 dots resolution driving controller. The HX8347-B is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-B can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-B also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-B is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Resolution:
  - 240(H) x RGB(H) x 320(V)
- Display Color modes
  - Normal Display Mode On
    1. System Interface Circuit
       a. Full color mode:
          -262k colours (18bit 6(R):6(G):6(B))
       b. Reduce color mode:
          -65k colours (16bit 5(R):6(G):5(B))
    2. RGB Interface Circuit
       a. 65,536(R(5),G(6),B(5)) colors
       b. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors

2.2 Display Module

- Frame Memory area 240 (H) x 320 (V) x 18 bit
- On module DC/DC converter
- DDVDH = 5.0 V for two time pump (Power supply for driver circuit range)
- DDVDH = 6.1 V for three time pump (Power supply for driver circuit range)
- VREG1 = 3.3V to 5.8V (Source output voltage range)
- VGH = +9.0 to +16.5V (Positive Gate output voltage range)
- VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)

2.3 Display Control Interface

- Display Interface types supported
  - System interface:
    1. 8-/9-/16-/18-bit parallel bus system interface
    2. 3-/4-wire serial bus system interface
  - RGB interface:
    1. 6-/16-/18-bit RGB interface
- Color modes
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)

2.4 Input power

- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V
- Outputs
  - Source outputs: 720 source lines.
  - Selectable gate line control signal for glass 320 gate lines
  - Adjusted source voltages (V0p ~V63p, V0n ~V63n)

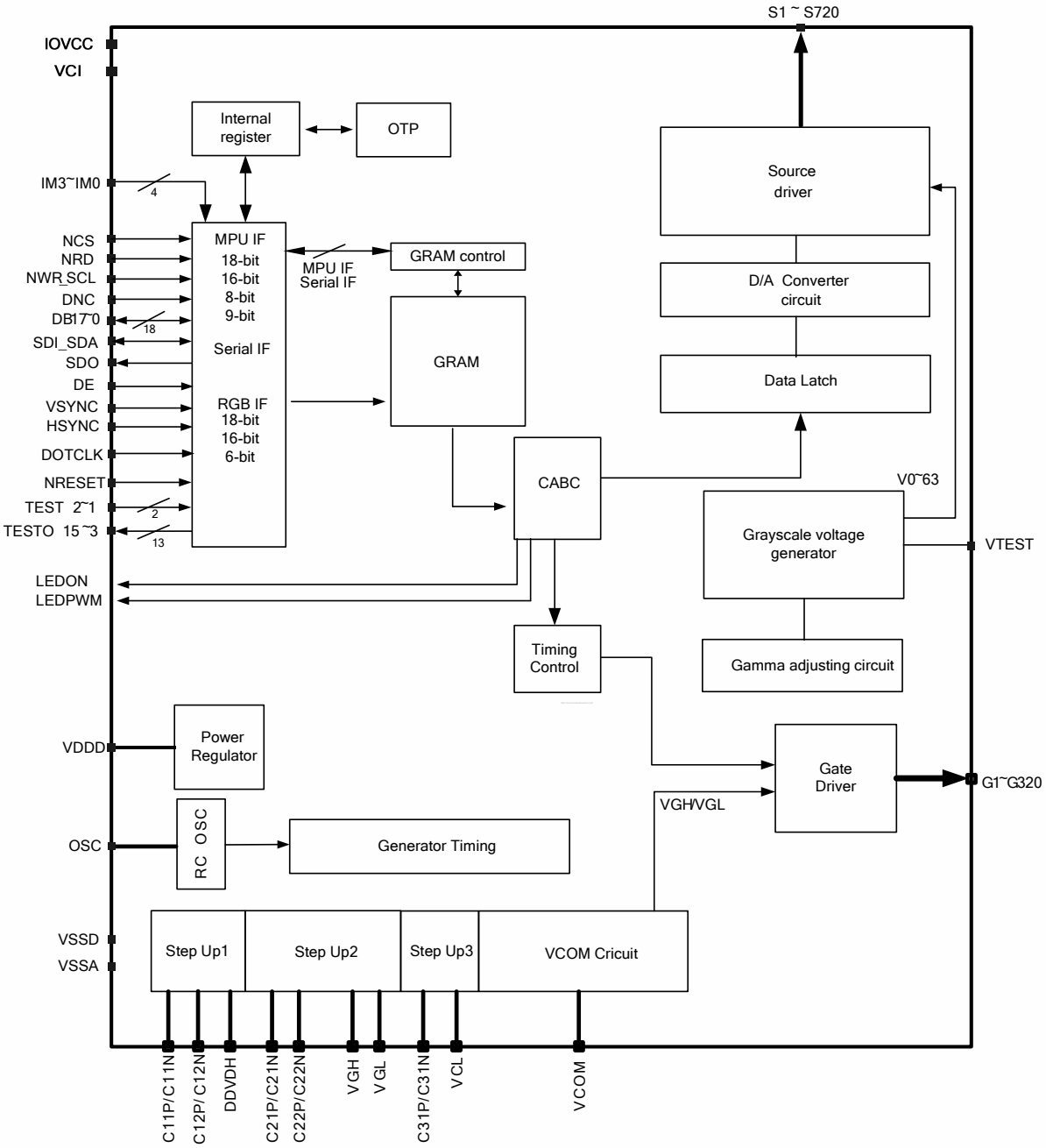
- Display interface:
  - System interface:
    a. 8-/9-/16-/18-bit parallel bus system interface
    b. 3-wire 24bits/3-wire 9bits/4-wire 8bits serial bus system interface
    c. Vsync interface
  - RGB interface:
    a. 6-/16-/18-bit RGB interface

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support Line inversion or Frame inversion
- Support Area scrolling
- Support Partial display mode
- Support Deep standby mode
- Support normal black/normal white LCD
- Support wide view angle display
- Audible noise reducing function
- On-chip OTP (One-time-programming) and MTP(8-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function
- Operating temperature range : -40℃~ 85℃

3. Block Diagram

3.1 Block diagram



3.2 Pin Description

<table>
<tr><th colspan="5">Interface Logic Pin</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM3, IM2,IM1,IM0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bit Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bit Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel type II</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel type II</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>3-wire 24-bits Serial interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3-wire 9-bits Serial interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bits Serial interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-bit parallel type I</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bit parallel type I</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel type II</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel type II</td></tr>
</table>
If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.</td></tr>
<tr><td>NWR_SCL</td><td>I</td><td>1</td><td>MPU</td><td>(NWR) Write enable pin I80 parallel bus system interface.
(SCL) server as serial data clock in serial bus system interface.
If not used, connected to IOVCC.</td></tr>
<tr><td>NRD</td><td>I</td><td>1</td><td>MPU</td><td>(NRD) Read enable pin I80 parallel bus system interface.
If not used, connected to IOVCC.</td></tr>
<tr><td>SDI_SDA</td><td>I</td><td>1</td><td>MPU</td><td>Serial data input pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal.
In the 8/9-bit serial peripheral interface, this pin is used as bi-directional data pin.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>DNC</td><td>I</td><td>1</td><td>MPU</td><td>(DNC) Command / parameter or display data selection pin.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Vertical synchronizing signal in RGB interface.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Horizontal synchronizing signal in RGB interface.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Data enable signal in RGB interface.
If not used, please connect to VSSD or let it open.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>DB17~0</td><td>I/O</td><td>18</td><td>MPU</td><td>18-bit bi-directional data bus.
The unused pins should be left open or connected to VSSD.</td></tr>
<tr><td>VGS</td><td>I</td><td>2</td><td>VSSD or external resistor</td><td>Connect to a variable resistor to adjust the internal gamma reference voltage for matching the characteristic of different panel used.</td></tr>
</table>

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	7	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
SDO	O	1	MPU	Serial data output pin in serial bus system interface. If not used, please let it open.
TE	O	1	MPU or open	Tearing effect output. If not used, please let it open.

LEDPWM/TESTO1	O	1	Backlight Circuit	CABC backlight control PWM signal output
LEDEN/TESTO2	O	1	Backlight Circuit	This pin is connected to external LED driver. It's a LED driver control pin which is used for turning ON/OFF of LED backlight.

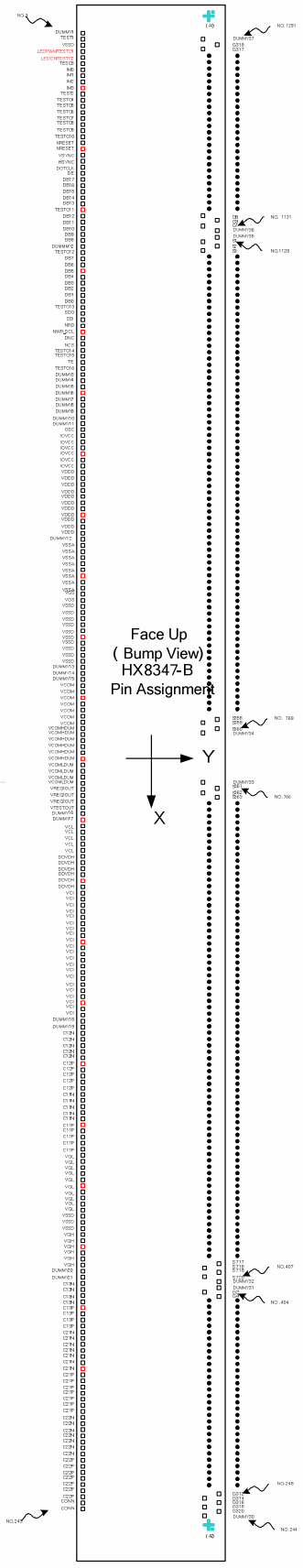
Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11P,C11N C12P, C12N	I/O	5,5 5,5	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C13P,C13N	I/O	4,4	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21P,C21N C22P,C22N	I/O	7,7 7,7	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	6	Power Supply	Digital IO Pad power supply.
VCI	P	21	Power Supply	Analog power supply.
VSSD	P	14	Ground	Digital ground.
VSSA	P	8	Ground	Analog ground.
VDDD	O	11	Stabilizing capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor between VSSD and VDDD
VREG1	O	4	Open	Internal generated stable power for source driver unit. Leave it open.
VCL	O	5	Stabilizing capacitor	An output from the step-up circuit3. A negative voltage for VCOML circuit, VCL= -VCI. Connect to a stabilizing capacitor between VSSA and VCL.
DDVDH	O	6	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	O	6	Stabilizing capacitor	A positive power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGH.
VGL	O	10	Stabilizing capacitor	A negative power output from the step-up circuit 2 for the gate line drive circuit. The step-up rate is determined by BT[2:0] bits. Connect to a stabilizing capacitor between GND and VGL.

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST2-1	I	2	GND	Test pin input (Internal pull low). Disconnect it.
TESTO15-3	O	13	Open	A test pin. Disconnect it.
OSC	I	1	Open or Connect to VSSD	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must leave it opens.
VCOMHDUM	-	6	Open	Dummy pads. Leave it open.
VCOMLDUM	-	7	Open	Dummy pads. Leave it open.
DUMMY37-1	-	37	Open	Dummy pads. Leave it open.

3.3 Pin Assignment

- Chip Size: 17820 um x 730 um
  (Including Seal-ring 20 um *2,
  Scribe line 40 um *2)
- Chip Thickness: 28 um (typ.)
- Pad Location: Pad center
- Coordinate Origin: Chip center
- Au Bump Size:
  1. 50 um x 80 um
     Input/Output
     (No. 1~ No. 243)
  2. 16 um x 98 um
     Staggered LCD output side
     (No. 244 ~ No. 1291)



3.4 PAD Coordinates

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY1	-8610	-263	61	DUMMY7	-4130	-263	121	VCOML	70	-263	181	C11P	4270	-263
2	TEST1	-8540	-263	62	DUMMY8	-4060	-263	122	VCOML	140	-263	182	C11P	4340	-263
3	VSSD	-8470	-263	63	DUMMY9	-3990	-263	123	VCOML	210	-263	183	C11P	4410	-263
4	LEDPWM/TESTO1	-8400	-263	64	DUMMY10	-3920	-263	124	VCOML	280	-263	184	C11P	4480	-263
5	LEDON/TESTO2	-8330	-263	65	DUMMY11	-3850	-263	125	VREG1OUT	350	-263	185	VGL	4550	-263
6	TESTO3	-8260	-263	66	OSC	-3780	-263	126	VREG1OUT	420	-263	186	VGL	4620	-263
7	IM0	-8190	-263	67	IOVCC	-3710	-263	127	VREG1OUT	490	-263	187	VGL	4690	-263
8	IM1	-8120	-263	68	IOVCC	-3640	-263	128	VTESTOUT	560	-263	188	VGL	4760	-263
9	IM2	-8050	-263	69	IOVCC	-3570	-263	129	DUMMY16	630	-263	189	VGL	4830	-263
10	IM3	-7980	-263	70	IOVCC	-3500	-263	130	DUMMY17	700	-263	190	VGL	4900	-263
11	TEST2	-7910	-263	71	IOVCC	-3430	-263	131	VCL	770	-263	191	VGL	4970	-263
12	TESTO4	-7840	-263	72	IOVCC	-3360	-263	132	VCL	840	-263	192	VGL	5040	-263
13	TESTO5	-7770	-263	73	VDDD	-3290	-263	133	VCL	910	-263	193	VGL	5110	-263
14	TESTO6	-7700	-263	74	VDDD	-3220	-263	134	VCL	980	-263	194	VGL	5180	-263
15	TESTO7	-7630	-263	75	VDDD	-3150	-263	135	VCL	1050	-263	195	VSSD	5250	-263
16	TESTO8	-7560	-263	76	VDDD	-3080	-263	136	DDVDH	1120	-263	196	VSSD	5320	-263
17	TESTO9	-7490	-263	77	VDDD	-3010	-263	137	DDVDH	1190	-263	197	VSSD	5390	-263
18	TESTO10	-7420	-263	78	VDDD	-2940	-263	138	DDVDH	1260	-263	198	VGH	5460	-263
19	nRESET	-7350	-263	79	VDDD	-2870	-263	139	DDVDH	1330	-263	199	VGH	5530	-263
20	nRESET	-7280	-263	80	VDDD	-2800	-263	140	DDVDH	1400	-263	200	VGH	5600	-263
21	VSYNC	-7210	-263	81	VDDD	-2730	-263	141	DDVDH	1470	-263	201	VGH	5670	-263
22	HSYNC	-7140	-263	82	VDDD	-2660	-263	142	VCI	1540	-263	202	VGH	5740	-263
23	DOTCLK	-7070	-263	83	VDDD	-2590	-263	143	VCI	1610	-263	203	VGH	5810	-263
24	DE	-7000	-263	84	DUMMY12	-2520	-263	144	VCI	1680	-263	204	DUMMY20	5880	-263
25	DB17	-6905	-263	85	VSSA	-2450	-263	145	VCI	1750	-263	205	DUMMY21	5950	-263
26	DB16	-6825	-263	86	VSSA	-2380	-263	146	VCI	1820	-263	206	C13N	6020	-263
27	DB15	-6745	-263	87	VSSA	-2310	-263	147	VCI	1890	-263	207	C13N	6090	-263
28	DB14	-6665	-263	88	VSSA	-2240	-263	148	VCI	1960	-263	208	C13N	6160	-263
29	DB13	-6585	-263	89	VSSA	-2170	-263	149	VCI	2030	-263	209	C13N	6230	-263
30	TESTO11	-6495	-263	90	VSSA	-2100	-263	150	VCI	2100	-263	210	C13P	6300	-263
31	DB12	-6405	-263	91	VSSA	-2030	-263	151	VCI	2170	-263	211	C13P	6370	-263
32	DB11	-6325	-263	92	VSSA	-1960	-263	152	VCI	2240	-263	212	C13P	6440	-263
33	DB10	-6245	-263	93	VGS	-1890	-263	153	VCI	2310	-263	213	C13P	6510	-263
34	DB9	-6165	-263	94	VGS	-1820	-263	154	VCI	2380	-263	214	C21N	6580	-263
35	DB8	-6085	-263	95	VSSD	-1750	-263	155	VCI	2450	-263	215	C21N	6650	-263
36	DUMMY2	-5990	-263	96	VSSD	-1680	-263	156	VCI	2520	-263	216	C21N	6720	-263
37	TESTO12	-5920	-263	97	VSSD	-1610	-263	157	VCI	2590	-263	217	C21N	6790	-263
38	DB7	-5825	-263	98	VSSD	-1540	-263	158	VCI	2660	-263	218	C21N	6860	-263
39	DB6	-5745	-263	99	VSSD	-1470	-263	159	VCI	2730	-263	219	C21N	6930	-263
40	DB5	-5665	-263	100	VSSD	-1400	-263	160	VCI	2800	-263	220	C21N	7000	-263
41	DB4	-5585	-263	101	VSSD	-1330	-263	161	VCI	2870	-263	221	C21P	7070	-263
42	DB3	-5505	-263	102	VSSD	-1260	-263	162	VCI	2940	-263	222	C21P	7140	-263
43	DB2	-5425	-263	103	VSSD	-1190	-263	163	DUMMY18	3010	-263	223	C21P	7210	-263
44	DB1	-5345	-263	104	VSSD	-1120	-263	164	DUMMY19	3080	-263	224	C21P	7280	-263
45	DB0	-5265	-263	105	DUMMY13	-1050	-263	165	C12N	3150	-263	225	C21P	7350	-263
46	TESTO13	-5180	-263	106	DUMMY14	-980	-263	166	C12N	3220	-263	226	C21P	7420	-263
47	SDO	-5110	-263	107	DUMMY15	-910	-263	167	C12N	3290	-263	227	C21P	7490	-263
48	SDI_SDA	-5040	-263	108	VCOM	-840	-263	168	C12N	3360	-263	228	C22N	7560	-263
49	nRD	-4970	-263	109	VCOM	-770	-263	169	C12N	3430	-263	229	C22N	7630	-263
50	nWR/SCL	-4900	-263	110	VCOM	-700	-263	170	C12P	3500	-263	230	C22N	7700	-263
51	DNC	-4830	-263	111	VCOM	-630	-263	171	C12P	3570	-263	231	C22N	7770	-263
52	nCS	-4760	-263	112	VCOM	-560	-263	172	C12P	3640	-263	232	C22N	7840	-263
53	TESTO14	-4690	-263	113	VCOM	-490	-263	173	C12P	3710	-263	233	C22N	7910	-263
54	TESTO15	-4620	-263	114	VCOM	-420	-263	174	C12P	3780	-263	234	C22N	7980	-263
55	TE	-4550	-263	115	VCOMH	-350	-263	175	C11N	3850	-263	235	C22P	8050	-263
56	TESTO16	-4480	-263	116	VCOMH	-280	-263	176	C11N	3920	-263	236	C22P	8120	-263
57	DUMMY3	-4410	-263	117	VCOMH	-210	-263	177	C11N	3990	-263	237	C22P	8190	-263
58	DUMMY4	-4340	-263	118	VCOMH	-140	-263	178	C11N	4060	-263	238	C22P	8260	-263
59	DUMMY5	-4270	-263	119	VCOMH	-70	-263	179	C11N	4130	-263	239	C22P	8330	-263
60	DUMMY6	-4200	-263	120	VCOMH	0	-263	180	C11P	4200	-263	240	C22P	8400	-263

No.	Pad name	X	Y
241	C22P	8470	-263
242	CONN	8540	-263
243	CONN	8610	-263
244	DUMMY30	8659	137
245	G320	8643	254
246	G318	8627	137
247	G316	8611	254
248	G314	8595	137
249	G312	8579	254
250	G310	8563	137
251	G308	8547	254
252	G306	8531	137
253	G304	8515	254
254	G302	8499	137
255	G300	8483	254
256	G298	8467	137
257	G296	8451	254
258	G294	8435	137
259	G292	8419	254
260	G290	8403	137
261	G288	8387	254
262	G286	8371	137
263	G284	8355	254
264	G282	8339	137
265	G280	8323	254
266	G278	8307	137
267	G276	8291	254
268	G274	8275	137
269	G272	8259	254
270	G270	8243	137
271	G268	8227	254
272	G266	8211	137
273	G264	8195	254
274	G262	8179	137
275	G260	8163	254
276	G258	8147	137
277	G256	8131	254
278	G254	8115	137
279	G252	8099	254
280	G250	8083	137
281	G248	8067	254
282	G246	8051	137
283	G244	8035	254
284	G242	8019	137
285	G240	8003	254
286	G238	7987	137
287	G236	7971	254
288	G234	7955	137
289	G232	7939	254
290	G230	7923	137
291	G228	7907	254
292	G226	7891	137
293	G224	7875	254
294	G222	7859	137
295	G220	7843	254
296	G218	7827	137
297	G216	7811	254
298	G214	7795	137
299	G212	7779	254
300	G210	7763	137

No.	Pad name	X	Y
301	G208	7747	254
302	G206	7731	137
303	G204	7715	254
304	G202	7699	137
305	G200	7683	254
306	G198	7667	137
307	G196	7651	254
308	G194	7635	137
309	G192	7619	254
310	G190	7603	137
311	G188	7587	254
312	G186	7571	137
313	G184	7555	254
314	G182	7539	137
315	G180	7523	254
316	G178	7507	137
317	G176	7491	254
318	G174	7475	137
319	G172	7459	254
320	G170	7443	137
321	G168	7427	254
322	G166	7411	137
323	G164	7395	254
324	G162	7379	137
325	G160	7363	254
326	G158	7347	137
327	G156	7331	254
328	G154	7315	137
329	G152	7299	254
330	G150	7283	137
331	G148	7267	254
332	G146	7251	137
333	G144	7235	254
334	G142	7219	137
335	G140	7203	254
336	G138	7187	137
337	G136	7171	254
338	G134	7155	137
339	G132	7139	254
340	G130	7123	137
341	G128	7107	254
342	G126	7091	137
343	G124	7075	254
344	G122	7059	137
345	G120	7043	254
346	G118	7027	137
347	G116	7011	254
348	G114	6995	137
349	G112	6979	254
350	G110	6963	137
351	G108	6947	254
352	G106	6931	137
353	G104	6915	254
354	G102	6899	137
355	G100	6883	254
356	G98	6867	137
357	G96	6851	254
358	G94	6835	137
359	G92	6819	254
360	G90	6803	137

No.	Pad name	X	Y
361	G88	6787	254
362	G86	6771	137
363	G84	6755	254
364	G82	6739	137
365	G80	6723	254
366	G78	6707	137
367	G76	6691	254
368	G74	6675	137
369	G72	6659	254
370	G70	6643	137
371	G68	6627	254
372	G66	6611	137
373	G64	6595	254
374	G62	6579	137
375	G60	6563	254
376	G58	6547	137
377	G56	6531	254
378	G54	6515	137
379	G52	6499	254
380	G50	6483	137
381	G48	6467	254
382	G46	6451	137
383	G44	6435	254
384	G42	6419	137
385	G40	6403	254
386	G38	6387	137
387	G36	6371	254
388	G34	6355	137
389	G32	6339	254
390	G30	6323	137
391	G28	6307	254
392	G26	6291	137
393	G24	6275	254
394	G22	6259	137
395	G20	6243	254
396	G18	6227	137
397	G16	6211	254
398	G14	6195	137
399	G12	6179	254
400	G10	6163	137
401	G8	6147	254
402	G6	6131	137
403	G4	6115	254
404	G2	6099	137
405	DUMMY31	6083	254
406	DUMMY32	6047	254
407	S720	6031	137
408	S719	6015	254
409	S718	5999	137
410	S717	5983	254
411	S716	5967	137
412	S715	5951	254
413	S714	5935	137
414	S713	5919	254
415	S712	5903	137
416	S711	5887	254
417	S710	5871	137
418	S709	5855	254
419	S708	5839	137
420	S707	5823	254

No.	Pad name	X	Y
421	S706	5807	137
422	S705	5791	254
423	S704	5775	137
424	S703	5759	254
425	S702	5743	137
426	S701	5727	254
427	S700	5711	137
428	S699	5695	254
429	S698	5679	137
430	S697	5663	254
431	S696	5647	137
432	S695	5631	254
433	S694	5615	137
434	S693	5599	254
435	S692	5583	137
436	S691	5567	254
437	S690	5551	137
438	S689	5535	254
439	S688	5519	137
440	S687	5503	254
441	S686	5487	137
442	S685	5471	254
443	S684	5455	137
444	S683	5439	254
445	S682	5423	137
446	S681	5407	254
447	S680	5391	137
448	S679	5375	254
449	S678	5359	137
450	S677	5343	254
451	S676	5327	137
452	S675	5311	254
453	S674	5295	137
454	S673	5279	254
455	S672	5263	137
456	S671	5247	254
457	S670	5231	137
458	S669	5215	254
459	S668	5199	137
460	S667	5183	254
461	S666	5167	137
462	S665	5151	254
463	S664	5135	137
464	S663	5119	254
465	S662	5103	137
466	S661	5087	254
467	S660	5071	137
468	S659	5055	254
469	S658	5039	137
470	S657	5023	254
471	S656	5007	137
472	S655	4991	254
473	S654	4975	137
474	S653	4959	254
475	S652	4943	137
476	S651	4927	254
477	S650	4911	137
478	S649	4895	254
479	S648	4879	137
480	S647	4863	254

No.	Pad name	X	Y
481	S646	4847	137
482	S645	4831	254
483	S644	4815	137
484	S643	4799	254
485	S642	4783	137
486	S641	4767	254
487	S640	4751	137
488	S639	4735	254
489	S638	4719	137
490	S637	4703	254
491	S636	4687	137
492	S635	4671	254
493	S634	4655	137
494	S633	4639	254
495	S632	4623	137
496	S631	4607	254
497	S630	4591	137
498	S629	4575	254
499	S628	4559	137
500	S627	4543	254
501	S626	4527	137
502	S625	4511	254
503	S624	4495	137
504	S623	4479	254
505	S622	4463	137
506	S621	4447	254
507	S620	4431	137
508	S619	4415	254
509	S618	4399	137
510	S617	4383	254
511	S616	4367	137
512	S615	4351	254
513	S614	4335	137
514	S613	4319	254
515	S612	4303	137
516	S611	4287	254
517	S610	4271	137
518	S609	4255	254
519	S608	4239	137
520	S607	4223	254
521	S606	4207	137
522	S605	4191	254
523	S604	4175	137
524	S603	4159	254
525	S602	4143	137
526	S601	4127	254
527	S600	4111	137
528	S599	4095	254
529	S598	4079	137
530	S597	4063	254
531	S596	4047	137
532	S595	4031	254
533	S594	4015	137
534	S593	3999	254
535	S592	3983	137
536	S591	3967	254
537	S590	3951	137
538	S589	3935	254
539	S588	3919	137
540	S587	3903	254

No.	Pad name	X	Y
541	S586	3887	137
542	S585	3871	254
543	S584	3855	137
544	S583	3839	254
545	S582	3823	137
546	S581	3807	254
547	S580	3791	137
548	S579	3775	254
549	S578	3759	137
550	S577	3743	254
551	S576	3727	137
552	S575	3711	254
553	S574	3695	137
554	S573	3679	254
555	S572	3663	137
556	S571	3647	254
557	S570	3631	137
558	S569	3615	254
559	S568	3599	137
560	S567	3583	254
561	S566	3567	137
562	S565	3551	254
563	S564	3535	137
564	S563	3519	254
565	S562	3503	137
566	S561	3487	254
567	S560	3471	137
568	S559	3455	254
569	S558	3439	137
570	S557	3423	254
571	S556	3407	137
572	S555	3391	254
573	S554	3375	137
574	S553	3359	254
575	S552	3343	137
576	S551	3327	254
577	S550	3311	137
578	S549	3295	254
579	S548	3279	137
580	S547	3263	254
581	S546	3247	137
582	S545	3231	254
583	S544	3215	137
584	S543	3199	254
585	S542	3183	137
586	S541	3167	254
587	S540	3151	137
588	S539	3135	254
589	S538	3119	137
590	S537	3103	254
591	S536	3087	137
592	S535	3071	254
593	S534	3055	137
594	S533	3039	254
595	S532	3023	137
596	S531	3007	254
597	S530	2991	137
598	S529	2975	254
599	S528	2959	137
600	S527	2943	254

No.	Pad name	X	Y
601	S526	2927	137
602	S525	2911	254
603	S524	2895	137
604	S523	2879	254
605	S522	2863	137
606	S521	2847	254
607	S520	2831	137
608	S519	2815	254
609	S518	2799	137
610	S517	2783	254
611	S516	2767	137
612	S515	2751	254
613	S514	2735	137
614	S513	2719	254
615	S512	2703	137
616	S511	2687	254
617	S510	2671	137
618	S509	2545	254
619	S508	2639	137
620	S507	2623	254
621	S506	2607	137
622	S505	2591	254
623	S504	2575	137
624	S503	2559	254
625	S502	2543	137
626	S501	2527	254
627	S500	2511	137
628	S499	2495	254
629	S498	2479	137
630	S497	2463	254
631	S496	2447	137
632	S495	2431	254
633	S494	2415	137
634	S493	2399	254
635	S492	2383	137
636	S491	2367	254
637	S490	2351	137
638	S489	2335	254
639	S488	2319	137
640	S487	2303	254
641	S486	2287	137
642	S485	2271	254
643	S484	2255	137
644	S483	2239	254
645	S482	2223	137
646	S481	2207	254
647	S480	2191	137
648	S479	2175	254
649	S478	2159	137
650	S477	2143	254
651	S476	2127	137
652	S475	2111	254
653	S474	2095	137
654	S473	2079	254
655	S472	2063	137
656	S471	2047	254
657	S470	2031	137
658	S469	2015	254
659	S468	1999	137
660	S467	1983	254

No.	Pad name	X	Y
661	S466	1967	137
662	S465	1951	254
663	S464	1935	137
664	S463	1919	254
665	S462	1903	137
666	S461	1887	254
667	S460	1871	137
668	S459	1855	254
669	S458	1839	137
670	S457	1823	254
671	S456	1807	137
672	S455	1791	254
673	S454	1775	137
674	S453	1759	254
675	S452	1743	137
676	S451	1727	254
677	S450	1711	137
678	S449	1695	254
679	S448	1679	137
680	S447	1663	254
681	S446	1647	137
682	S445	1631	254
683	S444	1615	137
684	S443	1599	254
685	S442	1583	137
686	S441	1567	254
687	S440	1551	137
688	S439	1535	254
689	S438	1519	137
690	S437	1503	254
691	S436	1377	137
692	S435	1471	254
693	S434	1455	137
694	S433	1439	254
695	S432	1423	137
696	S431	1407	254
697	S430	1391	137
698	S429	1375	254
699	S428	1359	137
700	S427	1343	254
701	S426	1327	137
702	S425	1311	254
703	S424	1295	137
704	S423	1279	254
705	S422	1263	137
706	S421	1247	254
707	S420	1231	137
708	S419	1215	254
709	S418	1199	137
710	S417	1183	254
711	S416	1167	137
712	S415	1151	254
713	S414	1135	137
714	S413	1119	254
715	S412	1103	137
716	S411	1087	254
717	S410	1071	137
718	S409	1055	254
719	S408	1039	137
720	S407	1023	254

No.	Pad name	X	Y
721	S406	1007	137
722	S405	991	254
723	S404	975	137
724	S403	959	254
725	S402	943	137
726	S401	927	254
727	S400	911	137
728	S399	895	254
729	S398	879	137
730	S397	863	254
731	S396	847	137
732	S395	831	254
733	S394	815	137
734	S393	799	254
735	S392	783	137
736	S391	767	254
737	S390	751	137
738	S389	735	254
739	S388	719	137
740	S387	703	254
741	S386	687	137
742	S385	671	254
743	S384	655	137
744	S383	639	254
745	S382	623	137
746	S381	607	254
747	S380	591	137
748	S379	575	254
749	S378	559	137
750	S377	543	254
751	S376	527	137
752	S375	511	254
753	S374	495	137
754	S373	479	254
755	S372	463	137
756	S371	447	254
757	S370	431	137
758	S369	415	254
759	S368	399	137
760	S367	383	254
761	S366	367	137
762	S365	351	254
763	S364	335	137
764	S363	319	254
765	S362	303	137
766	S361	287	254
767	DUMMY33	271	137
768	DUMMY34	-271	137
769	S360	-287	254
770	S359	-303	137
771	S358	-319	254
772	S357	-335	137
773	S356	-351	254
774	S355	-367	137
775	S354	-383	254
776	S353	-399	137
777	S352	-415	254
778	S351	-431	137
779	S350	-447	254
780	S349	-463	137

No.	Pad name	X	Y
781	S348	-479	254
782	S347	-495	137
783	S346	-511	254
784	S345	-527	137
785	S344	-543	254
786	S343	-559	137
787	S342	-575	254
788	S341	-591	137
789	S340	-607	254
790	S339	-623	137
791	S338	-639	254
792	S337	-655	137
793	S336	-671	254
794	S335	-687	137
795	S334	-703	254
796	S333	-719	137
797	S332	-735	254
798	S331	-751	137
799	S330	-767	254
800	S329	-783	137
801	S328	-799	254
802	S327	-815	137
803	S326	-831	254
804	S325	-847	137
805	S324	-863	254
806	S323	-879	137
807	S322	-895	254
808	S321	-911	137
809	S320	-927	254
810	S319	-943	137
811	S318	-959	254
812	S317	-975	137
813	S316	-991	254
814	S315	-1007	137
815	S314	-1023	254
816	S313	-1039	137
817	S312	-1055	254
818	S311	-1071	137
819	S310	-1087	254
820	S309	-1103	137
821	S308	-1119	254
822	S307	-1135	137
823	S306	-1151	254
824	S305	-1167	137
825	S304	-1183	254
826	S303	-1199	137
827	S302	-1215	254
828	S301	-1231	137
829	S300	-1247	254
830	S299	-1263	137
831	S298	-1279	254
832	S297	-1295	137
833	S296	-1311	254
834	S295	-1327	137
835	S294	-1343	254
836	S293	-1359	137
837	S292	-1375	254
838	S291	-1391	137
839	S290	-1407	254
840	S289	-1423	137

No.	Pad name	X	Y
841	S288	-1439	254
842	S287	-1455	137
843	S286	-1471	254
844	S285	-1487	137
845	S284	-1503	254
846	S283	-1519	137
847	S282	-1535	254
848	S281	-1551	137
849	S280	-1567	254
850	S279	-1583	137
851	S278	-1599	254
852	S277	-1615	137
853	S276	-1631	254
854	S275	-1647	137
855	S274	-1663	254
856	S273	-1679	137
857	S272	-1695	254
858	S271	-1711	137
859	S270	-1727	254
860	S269	-1743	137
861	S268	-1759	254
862	S267	-1775	137
863	S266	-1791	254
864	S265	-1807	137
865	S264	-1823	254
866	S263	-1839	137
867	S262	-1855	254
868	S261	-1871	137
869	S260	-1887	254
870	S259	-1903	137
871	S258	-1919	254
872	S257	-1935	137
873	S256	-1951	254
874	S255	-1967	137
875	S254	-1983	254
876	S253	-1999	137
877	S252	-2015	254
878	S251	-2031	137
879	S250	-2047	254
880	S249	-2063	137
881	S248	-2079	254
882	S247	-2095	137
883	S246	-2111	254
884	S245	-2127	137
885	S244	-2143	254
886	S243	-2159	137
887	S242	-2175	254
888	S241	-2191	137
889	S240	-2207	254
890	S239	-2223	137
891	S238	-2239	254
892	S237	-2255	137
893	S236	-2271	254
894	S235	-2287	137
895	S234	-2303	254
896	S233	-2319	137
897	S232	-2335	254
898	S231	-2351	137
899	S230	-2367	254
900	S229	-2383	137

No.	Pad name	X	Y
901	S228	-2399	254
902	S227	-2415	137
903	S226	-2431	254
904	S225	-2447	137
905	S224	-2463	254
906	S223	-2479	137
907	S222	-2495	254
908	S221	-2511	137
909	S220	-2527	254
910	S219	-2543	137
911	S218	-2559	254
912	S217	-2575	137
913	S216	-2591	254
914	S215	-2607	137
915	S214	-2623	254
916	S213	-2639	137
917	S212	-2655	254
918	S211	-2671	137
919	S210	-2687	254
920	S209	-2703	137
921	S208	-2719	254
922	S207	-2735	137
923	S206	-2751	254
924	S205	-2767	137
925	S204	-2783	254
926	S203	-2799	137
927	S202	-2815	254
928	S201	-2831	137
929	S200	-2847	254
930	S199	-2863	137
931	S198	-2879	254
932	S197	-2895	137
933	S196	-2911	254
934	S195	-2927	137
935	S194	-2943	254
936	S193	-2959	137
937	S192	-2975	254
938	S191	-2991	137
939	S190	-3007	254
940	S189	-3023	137
941	S188	-3039	254
942	S187	-3055	137
943	S186	-3071	254
944	S185	-3087	137
945	S184	-3103	254
946	S183	-3119	137
947	S182	-3135	254
948	S181	-3151	137
949	S180	-3167	254
950	S179	-3183	137
951	S178	-3199	254
952	S177	-3215	137
953	S176	-3231	254
954	S175	-3247	137
955	S174	-3263	254
956	S173	-3279	137
957	S172	-3295	254
958	S171	-3311	137
959	S170	-3327	254
960	S169	-3343	137

No.	Pad name	X	Y
961	S168	-3359	254
962	S167	-3375	137
963	S166	-3391	254
964	S165	-3407	137
965	S164	-3423	254
966	S163	-3439	137
967	S162	-3455	254
968	S161	-3471	137
969	S160	-3487	254
970	S159	-3503	137
971	S158	-3519	254
972	S157	-3535	137
973	S156	-3551	254
974	S155	-3567	137
975	S154	-3583	254
976	S153	-3599	137
977	S152	-3615	254
978	S151	-3631	137
979	S150	-3647	254
980	S149	-3663	137
981	S148	-3679	254
982	S147	-3695	137
983	S146	-3711	254
984	S145	-3727	137
985	S144	-3743	254
986	S143	-3759	137
987	S142	-3775	254
988	S141	-3791	137
989	S140	-3807	254
990	S139	-3823	137
991	S138	-3839	254
992	S137	-3855	137
993	S136	-3871	254
994	S135	-3887	137
995	S134	-3903	254
996	S133	-3919	137
997	S132	-3935	254
998	S131	-3951	137
999	S130	-3967	254
1000	S129	-3983	137
1001	S128	-3999	254
1002	S127	-4015	137
1003	S126	-4031	254
1004	S125	-4047	137
1005	S124	-4063	254
1006	S123	-4079	137
1007	S122	-4095	254
1008	S121	-4111	137
1009	S120	-4127	254
1010	S119	-4143	137
1011	S118	-4159	254
1012	S117	-4175	137
1013	S116	-4191	254
1014	S115	-4207	137
1015	S114	-4223	254
1016	S113	-4239	137
1017	S112	-4255	254
1018	S111	-4271	137
1019	S110	-4287	254
1020	S109	-4303	137

No.	Pad name	X	Y
1021	S108	-4319	254
1022	S107	-4335	137
1023	S106	-4351	254
1024	S105	-4367	137
1025	S104	-4383	254
1026	S103	-4399	137
1027	S102	-4415	254
1028	S101	-4431	137
1029	S100	-4447	254
1030	S99	-4463	137
1031	S98	-4479	254
1032	S97	-4495	137
1033	S96	-4511	254
1034	S95	-4527	137
1035	S94	-4543	254
1036	S93	-4559	137
1037	S92	-4575	254
1038	S91	-4591	137
1039	S90	-4607	254
1040	S89	-4623	137
1041	S88	-4639	254
1042	S87	-4655	137
1043	S86	-4671	254
1044	S85	-4687	137
1045	S84	-4703	254
1046	S83	-4719	137
1047	S82	-4735	254
1048	S81	-4751	137
1049	S80	-4767	254
1050	S79	-4783	137
1051	S78	-4799	254
1052	S77	-4815	137
1053	S76	-4831	254
1054	S75	-4847	137
1055	S74	-4863	254
1056	S73	-4879	137
1057	S72	-4895	254
1058	S71	-4911	137
1059	S70	-4927	254
1060	S69	-4943	137
1061	S68	-4959	254
1062	S67	-4975	137
1063	S66	-4991	254
1064	S65	-5007	137
1065	S64	-5023	254
1066	S63	-5039	137
1067	S62	-5055	254
1068	S61	-5071	137
1069	S60	-5087	254
1070	S59	-5103	137
1071	S58	-5119	254
1072	S57	-5135	137
1073	S56	-5151	254
1074	S55	-5167	137
1075	S54	-5183	254
1076	S53	-5199	137
1077	S52	-5215	254
1078	S51	-5231	137
1079	S50	-5247	254
1080	S49	-5263	137

No.	Pad name	X	Y
1081	S48	-5279	254
1082	S47	-5295	137
1083	S46	-5311	254
1084	S45	-5327	137
1085	S44	-5343	254
1086	S43	-5359	137
1087	S42	-5375	254
1088	S41	-5391	137
1089	S40	-5407	254
1090	S39	-5423	137
1091	S38	-5439	254
1092	S37	-5455	137
1093	S36	-5471	254
1094	S35	-5487	137
1095	S34	-5503	254
1096	S33	-5519	137
1097	S32	-5535	254
1098	S31	-5551	137
1099	S30	-5567	254
1100	S29	-5583	137
1101	S28	-5599	254
1102	S27	-5615	137
1103	S26	-5631	254
1104	S25	-5647	137
1105	S24	-5663	254
1106	S23	-5679	137
1107	S22	-5695	254
1108	S21	-5711	137
1109	S20	-5727	254
1110	S19	-5743	137
1111	S18	-5759	254
1112	S17	-5775	137
1113	S16	-5791	254
1114	S15	-5807	137
1115	S14	-5823	254
1116	S13	-5839	137
1117	S12	-5855	254
1118	S11	-5871	137
1119	S10	-5887	254
1120	S9	-5903	137
1121	S8	-5919	254
1122	S7	-5935	137
1123	S6	-5951	254
1124	S5	-5967	137
1125	S4	-5983	254
1126	S3	-5999	137
1127	S2	-6015	254
1128	S1	-6031	137
1129	DUMMY35	-6047	254
1130	DUMMY36	-6083	254
1131	G1	-6099	137
1132	G3	-6115	254
1133	G5	-6131	137
1134	G7	-6147	254
1135	G9	-6163	137
1136	G11	-6179	254
1137	G13	-6195	137
1138	G15	-6211	254
1139	G17	-6227	137
1140	G19	-6243	254

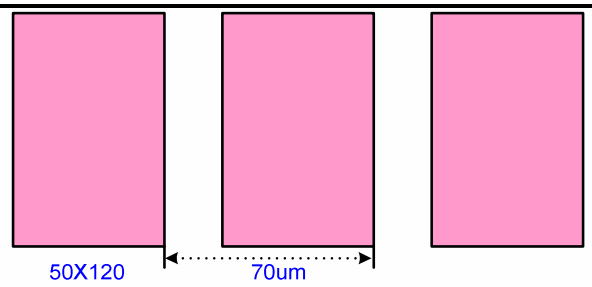
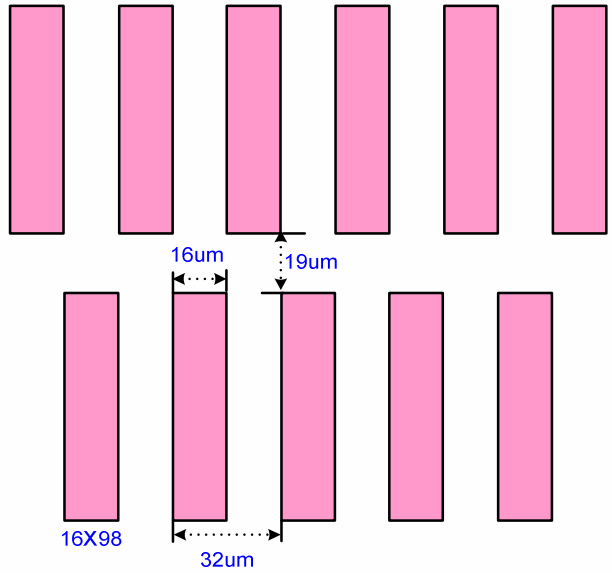
No.	Pad name	X	Y
1141	G21	-6259	137
1142	G23	-6275	254
1143	G25	-6291	137
1144	G27	-6307	254
1145	G29	-6323	137
1146	G31	-6339	254
1147	G33	-6355	137
1148	G35	-6371	254
1149	G37	-6387	137
1150	G39	-6403	254
1151	G41	-6419	137
1152	G43	-6435	254
1153	G45	-6451	137
1154	G47	-6467	254
1155	G49	-6483	137
1156	G51	-6499	254
1157	G53	-6515	137
1158	G55	-6531	254
1159	G57	-6547	137
1160	G59	-6563	254
1161	G61	-6579	137
1162	G63	-6595	254
1163	G65	-6611	137
1164	G67	-6627	254
1165	G69	-6643	137
1166	G71	-6659	254
1167	G73	-6675	137
1168	G75	-6691	254
1169	G77	-6707	137
1170	G79	-6723	254
1171	G81	-6739	137
1172	G83	-6755	254
1173	G85	-6771	137
1174	G87	-6787	254
1175	G89	-6803	137
1176	G91	-6819	254
1177	G93	-6835	137
1178	G95	-6851	254
1179	G97	-6867	137
1180	G99	-6883	254
1181	G101	-6899	137
1182	G103	-6915	254
1183	G105	-6931	137
1184	G107	-6947	254
1185	G109	-6963	137
1186	G111	-6979	254
1187	G113	-6995	137
1188	G115	-7011	254
1189	G117	-7027	137
1190	G119	-7043	254
1191	G121	-7059	137
1192	G123	-7075	254
1193	G125	-7091	137
1194	G127	-7107	254
1195	G129	-7123	137
1196	G131	-7139	254
1197	G133	-7155	137
1198	G135	-7171	254
1199	G137	-7187	137
1200	G139	-7203	254

No.	Pad name	X	Y
1201	G141	-7219	137
1202	G143	-7235	254
1203	G145	-7251	137
1204	G147	-7267	254
1205	G149	-7283	137
1206	G151	-7299	254
1207	G153	-7315	137
1208	G155	-7331	254
1209	G157	-7347	137
1210	G159	-7363	254
1211	G161	-7379	137
1212	G163	-7395	254
1213	G165	-7411	137
1214	G167	-7427	254
1215	G169	-7443	137
1216	G171	-7459	254
1217	G173	-7475	137
1218	G175	-7491	254
1219	G177	-7507	137
1220	G179	-7523	254
1221	G181	-7539	137
1222	G183	-7555	254
1223	G185	-7571	137
1224	G187	-7587	254
1225	G189	-7603	137
1226	G191	-7619	254
1227	G193	-7635	137
1228	G195	-7651	254
1229	G197	-7667	137
1230	G199	-7683	254
1231	G201	-7699	137
1232	G203	-7715	254
1233	G205	-7731	137
1234	G207	-7747	254
1235	G209	-7763	137
1236	G211	-7779	254
1237	G213	-7795	137
1238	G215	-7811	254
1239	G217	-7827	137
1240	G219	-7843	254
1241	G221	-7859	137
1242	G223	-7875	254
1243	G225	-7891	137
1244	G227	-7907	254
1245	G229	-7923	137
1246	G231	-7939	254
1247	G233	-7955	137
1248	G235	-7971	254
1249	G237	-7987	137
1250	G239	-8003	254
1251	G241	-8019	137
1252	G243	-8035	254
1253	G245	-8051	137
1254	G247	-8067	254
1255	G249	-8083	137
1256	G251	-8099	254
1257	G253	-8115	137
1258	G255	-8131	254
1259	G257	-8147	137
1260	G259	-8163	254

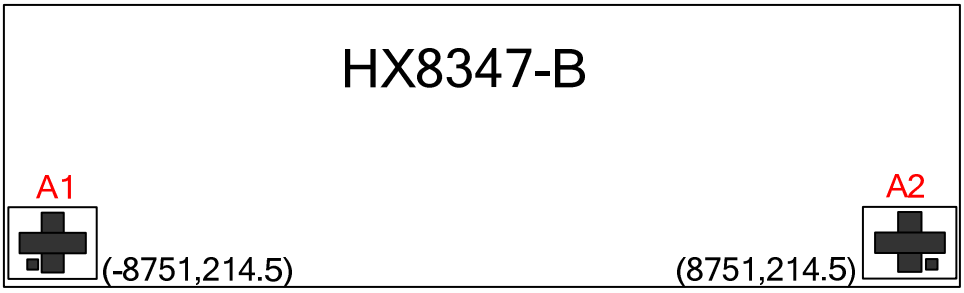
No.	Pad name	X	Y
1261	G261	-8179	137
1262	G263	-8195	254
1263	G265	-8211	137
1264	G267	-8227	254
1265	G269	-8243	137
1266	G271	-8259	254
1267	G273	-8275	137
1268	G275	-8291	254
1269	G277	-8307	137
1270	G279	-8323	254
1271	G281	-8339	137
1272	G283	-8355	254
1273	G285	-8371	137
1274	G287	-8387	254
1275	G289	-8403	137
1276	G291	-8419	254
1277	G293	-8435	137
1278	G295	-8451	254
1279	G297	-8467	137
1280	G299	-8483	254
1281	G301	-8499	137
1282	G303	-8515	254
1283	G305	-8531	137
1284	G307	-8547	254
1285	G309	-8563	137
1286	G311	-8579	254
1287	G313	-8595	137
1288	G315	-8611	254
1289	G317	-8627	137
1290	G319	-8643	254
1291	DUMMY37	-8659	137

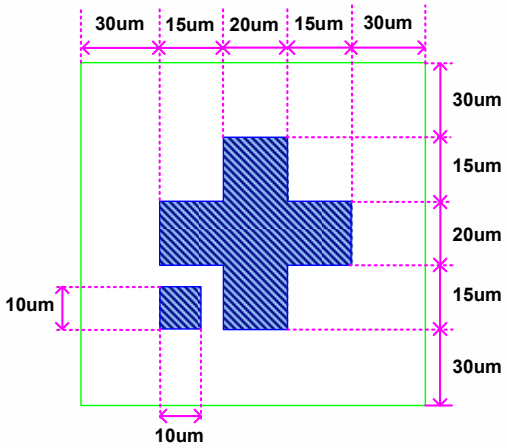
Alignment mark	X	Y
A1	-8751	214.5
A2	8751	214.5

3.5 Bump Size

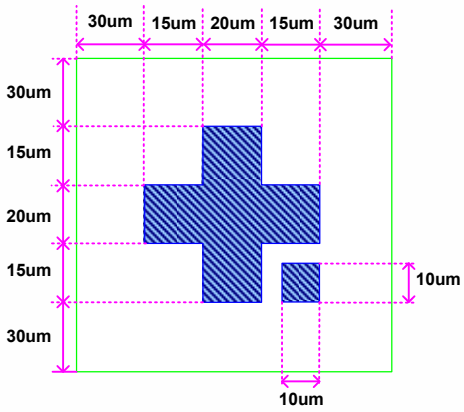
Input PAD	
Output PAD	

3.6 Alignment Mark





A_MARK (A1)



A_MARK (A2)

4. Interface

The HX8347-B has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8347-B shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface, the display data is written into the GRAM through the control signals of DE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

The HX8347-B also has VSYNC interface. In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization sign (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

4.1 System Interface Circuit

The system interface circuit in HX8347-B supports 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8347-B become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 4.1.

IM3	IM2	IM1	IM0	Interface	Data Bus use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 16-bit parallel type I	D7-D0	D15-D0: 16-bit data
0	0	0	1	8080 MCU 8-bit parallel type I	D7-D0	D7-D0: 8-bit data
0	0	1	0	8080 MCU 16-bits Parallel	D8-D1	D17-10, D8-D1: 16-bit data
0	0	1	1	8080 MCU 8-bits Parallel	D17-D10	D17-D10: 8-bits Data
0	1	0	ID	3-wire 24-bits Serial interface	SDI, SDO	
0	1	1	0	3-wire 9-bits Serial interface	SDI	
0	1	1	1	4-wire Serial interface	SDI	
1	0	0	0	8080 MCU 18-bit parallel type I	D7-D0	D17-D0: 18-bit data
1	0	0	1	8080 MCU 9-bit parallel type I	D7-D0	D8-D0: 9-bit data
1	0	1	0	8080 MCU 18-bits Parallel	D8-D1	D17-D0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel	D17-D10	D17-D9: 9-bits Data
Other Setting				Setting Invalid		

Table 4.1: Input Bus Format Selection of System Interface Circuit

It has an Index Register (IR) in HX8347-B to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

4.1.1 Parallel Bus System Interface

The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed in Table 4.2.

Operations	NWR_SCL	NRD	DNC
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 4.2: Data Pin Function for I80 Series CPU

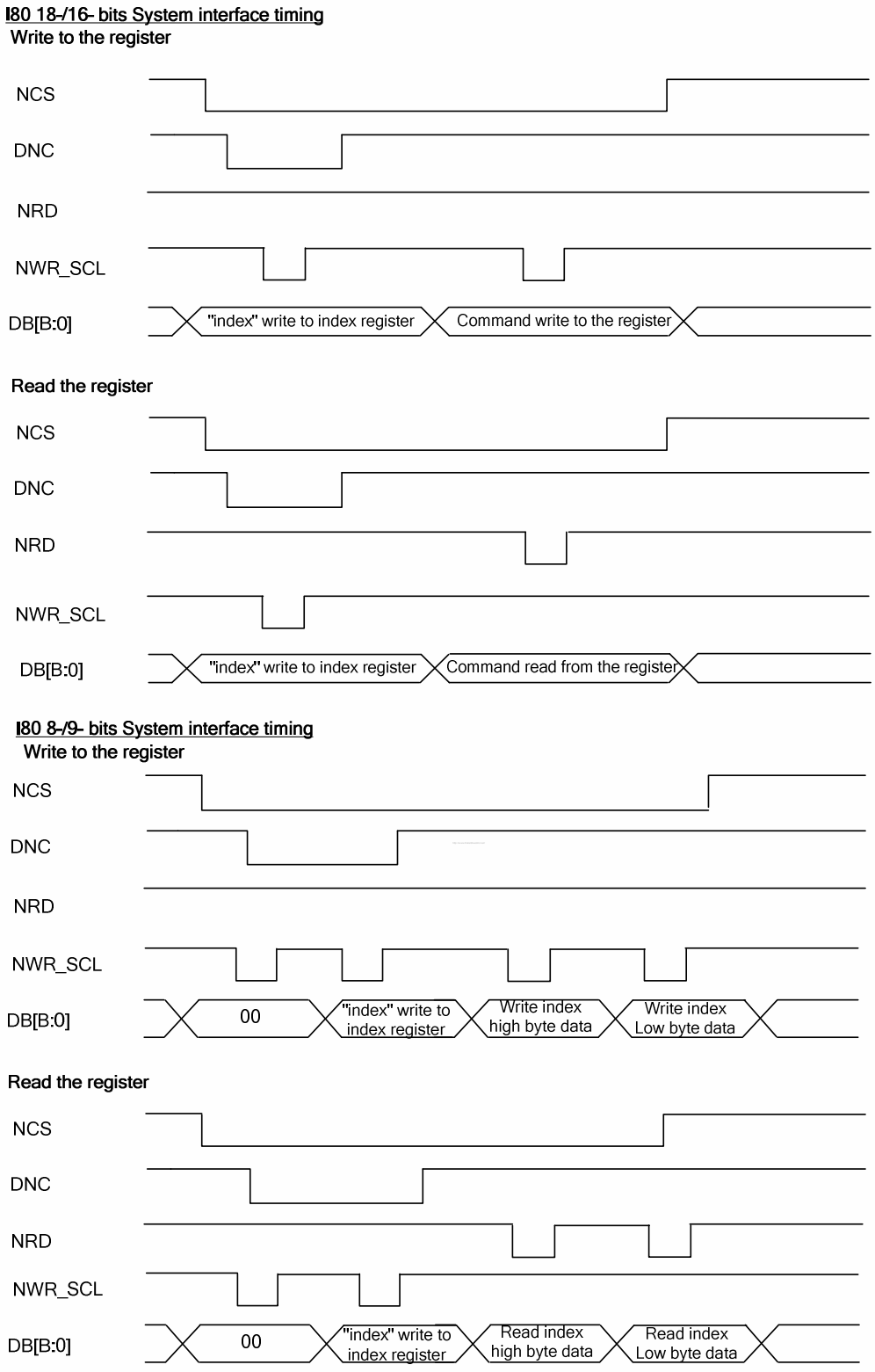
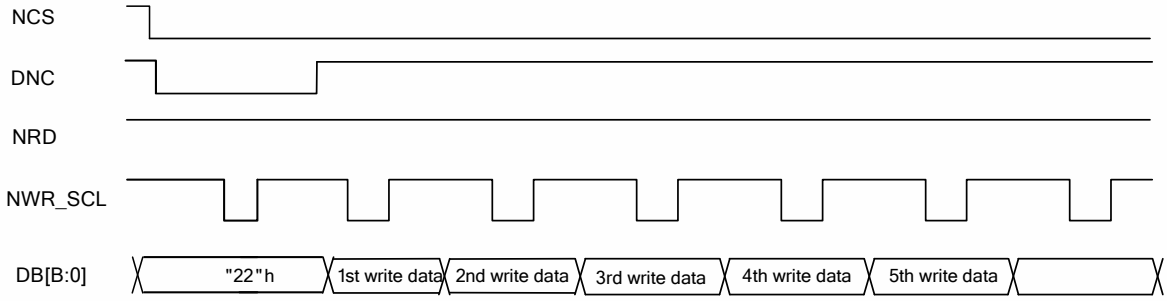


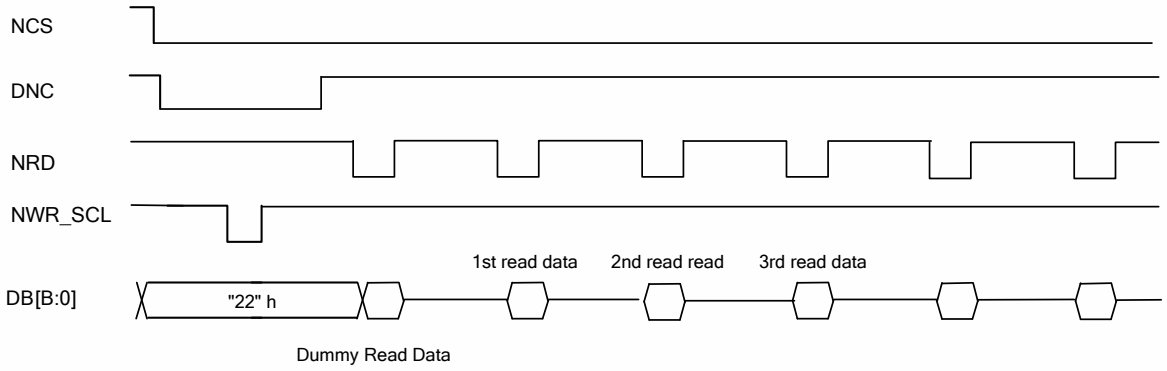
Figure 4.1: Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

I80 18-/16-bit System Bus Interface timing

Write to the graphic RAM

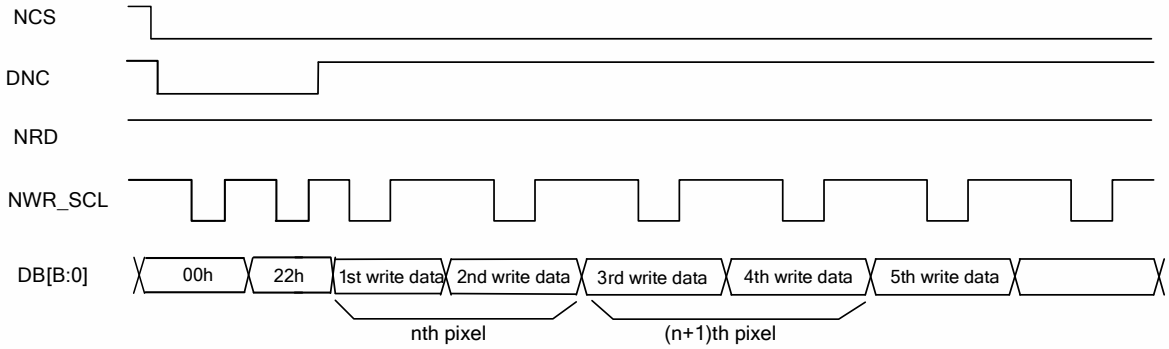


Read the graphic RAM



I80 9-/8-bit System Bus Interface timing

Write to the graphic RAM



Read the graphic RAM

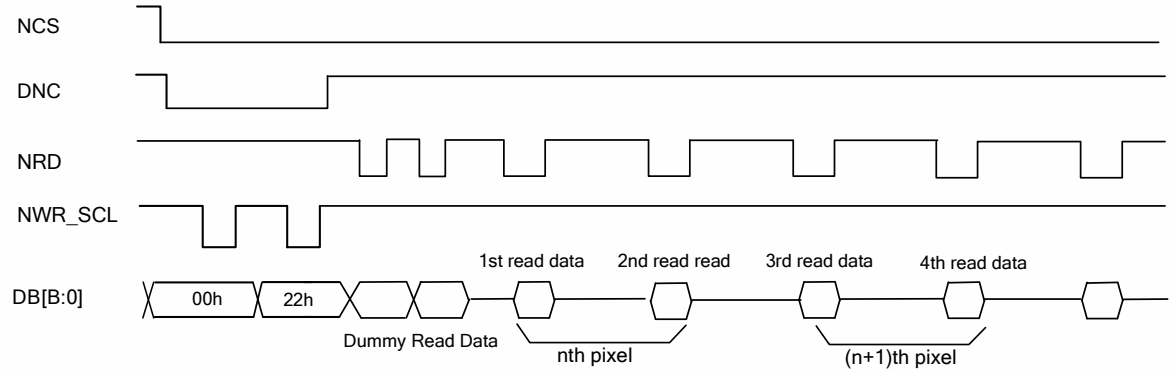


Figure 4.2: GRAM Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

4.1.2 MCU Data Color Coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0001")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
0	X	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
		x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
1	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.3: 8-Bits Parallel Interface type I **GRAM Write Table**

- Parallel 16-Bits Bus Interface type I (IM3,IM2,IM1,IM0="0000")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
0	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
1	0	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
		x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
		x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
1	1	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	X	x	B1	B0	

Table 4.4: 16-Bits Parallel Interface type I **GRAM Write Set Table**

- Parallel 9-Bits Bus Interface type I (IM3,IM2,IM1,IM0="1001")

Register		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
TRI	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
X	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2bytes)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.5: 9-Bits Parallel Interface type I **Set GRAM Write Table**

- Parallel 18-Bits Bus Interface type I (IM3,IM2,IM1,IM0="1000")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
TRI	**DFM**	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 4.6: 18-Bits Parallel Interface type I **GRAM Write Set Table**

- Parallel 8-Bits Bus Interface typeII (IM3,IM2,IM1,IM0="0011")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
0	X	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixels/ 2-bytes)
		G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
1	0	x	x	x	x	x	x	R5	R4	x	x	x	x	x	x	x	x	x	x	262K-Color (2+8+8)
		R3	R2	R1	R0	G5	G4	G3	G2	x	x	x	x	x	x	x	x	x	x	
		G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
1	1	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (6+6+6)
		G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
		B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 4.7: 8-Bits Parallel Interface type II GRAM Write Table

- Parallel 16-Bits Bus Interface typeII (IM3,IM2,IM1,IM0="0010")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM									x	0	0	1	0	0	0	1	0	x	**22H**
0	X	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
1	0	R5	R4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (16+2)
		B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	x	262K-Color (2+16)
		R3	R2	R1	R0	G5	G4	G3	G2	x	G1	G0	B5	B4	B3	B2	B1	B0	x	

Table 4.8: 16-Bits Parallel Interface type II GRAM Write Set Table

- Parallel 9-Bits Bus Interface typeII (IM3,IM2,IM1,IM0="1011")

Register		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
TRI	DFM	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
		G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 4.9: 9-Bits Parallel Interface type II Set GRAM Write Table

- Parallel 18-Bits Bus Interface typeII (IM3,IM2,IM1,IM0="1010")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
TRI	**DFM**	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 4.10: 18-Bits Parallel Interface type II GRAM Write Set Table

18-bit Parallel Bus System Interface

The I80-system 18-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “IM3, IM2, IM1, IM0” pins to “1000”. And the I80-system 18-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, and IM0”pins to“1010”. Figure 4.3 is the example of interface with I80 microcomputer system interface.

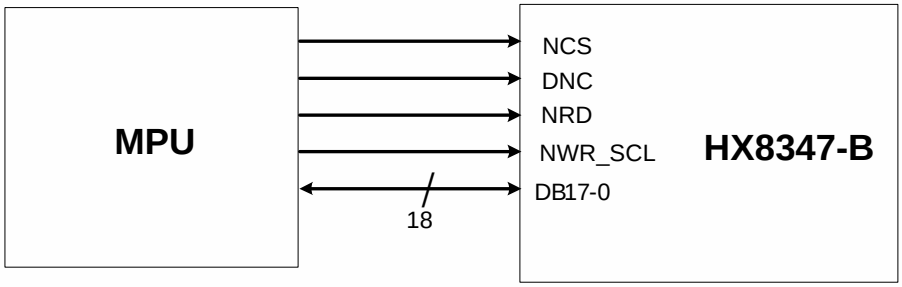


Figure 4.3: Example of I80- System 18-bit Parallel Bus Interface

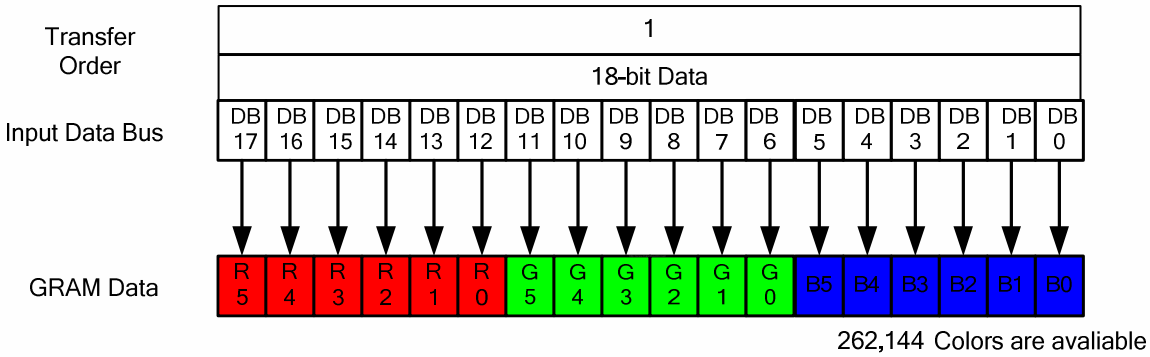


Figure 4.4: Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface with 18 Bit-Data Input (“IM3, IM2, IM1, IM”=”1010” or “1000”)

16-bit Parallel Bus System Interface

The I80-system 16-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins ““IM3, IM2, IM1, IM0” pins to “0000”. And I80-system 16-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ““IM3, IM2, IM1, and IM0”pins to“0010”. Figure 4.5 is the example of type I interface with I80 microcomputer system interface. And Figure 4.6 is the example of type II interface with I80 microcomputer system interface.

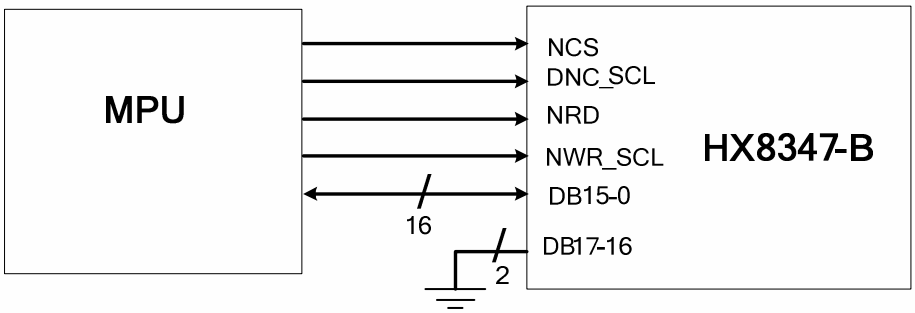


Figure 4.5: Example of I80 system 16-bit parallel bus interface type I

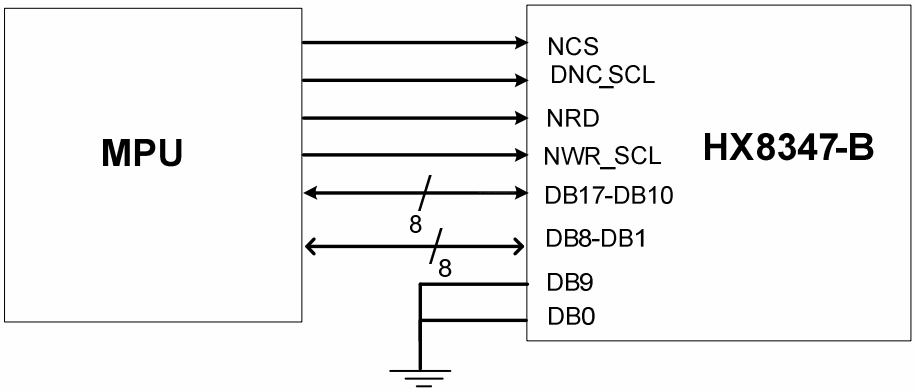


Figure 4.6: Example of I80 system 16-bit parallel bus interface type II

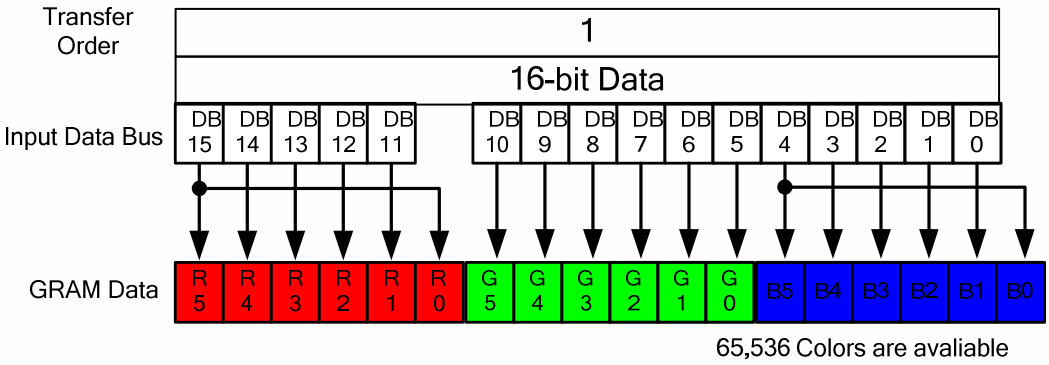


Figure 4.7: Input data bus and GRAM data mapping in 16-bit bus system interface with 16-bit-data input (TRI = ‘0’ and “IM3, IM2, IM1, IM0”=”0000”)

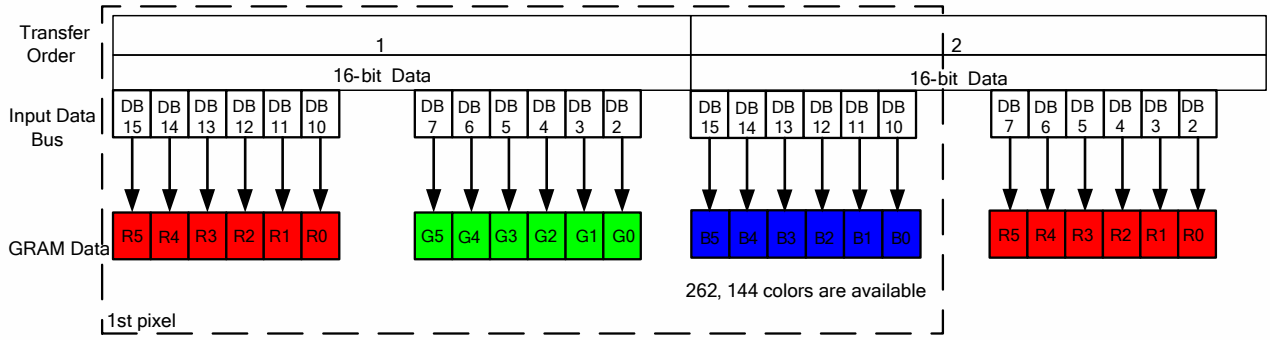


Figure 4.8: Input data bus and GRAM data mapping in 16-bit bus system interface with 18 bit-data input (TRI = '1', DFM = '0' and "IM3, IM2, IM1, IM0"="0000")

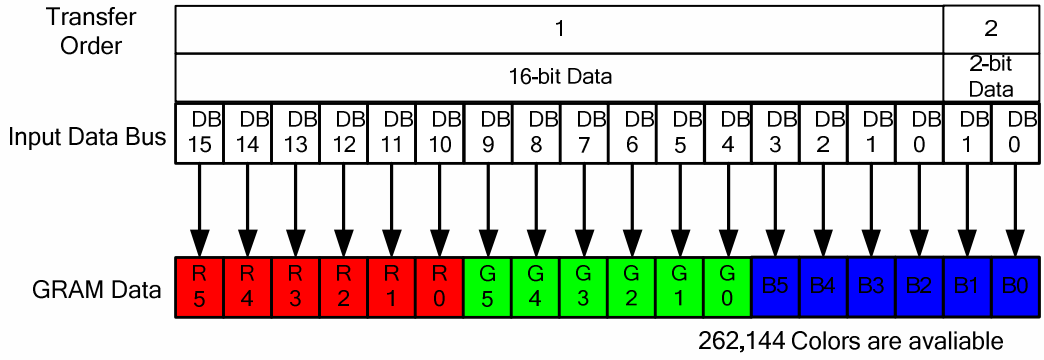


Figure 4.9: Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (TRI = '1', DFM = '1' and "IM3, IM2, IM1, IM0"="0000")

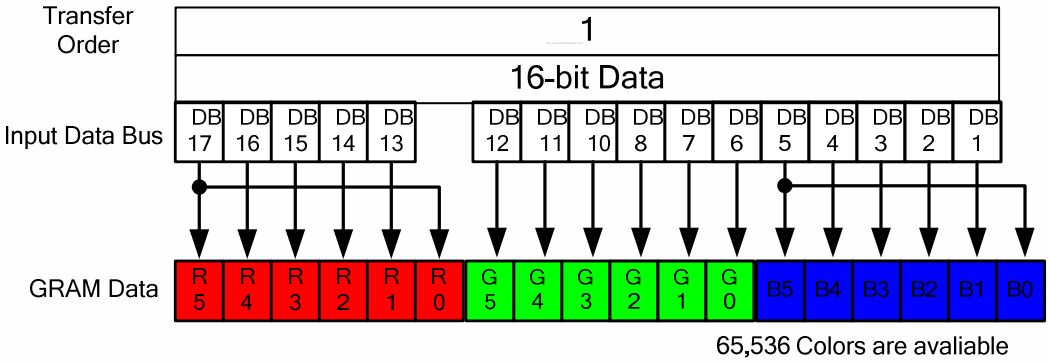


Figure 4.10: Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (TRI = 0 and "IM3, IM2, IM1, IM0"="0010")

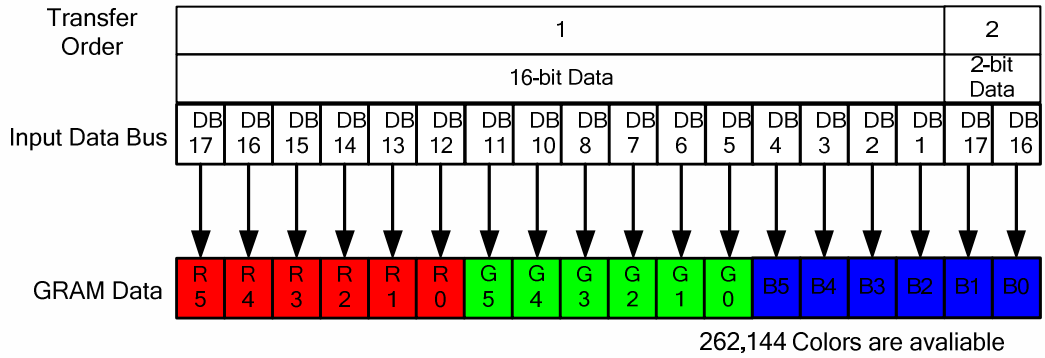


Figure 4.11: Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (TRI = '1', DFM = '0' and "IM3, IM2, IM1, IM0"="0010")

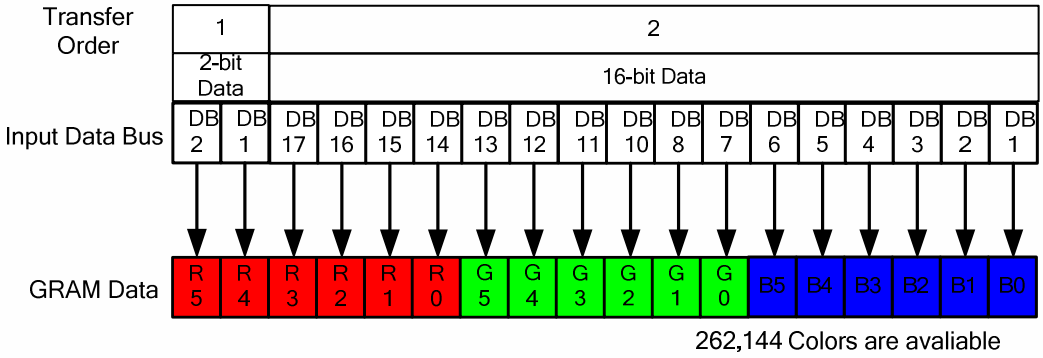


Figure 4.12 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(2+16) Bit-Data Input (TRI = '1', DFM = '1' and "IM3, IM2, IM1, IM0"="0010")

9-bit Parallel Bus System Interface

The I80-system 9-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins ""IM3, IM2, IM1, IM0" pins to "1001". And I80-system 9-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ""IM3, IM2, IM1, and IM0"pins to"1011". Figure 4.15 is the example of type I interface with I80 microcomputer system interface. And Figure 4.16 is the example of type II interface with I80 microcomputer system interface.

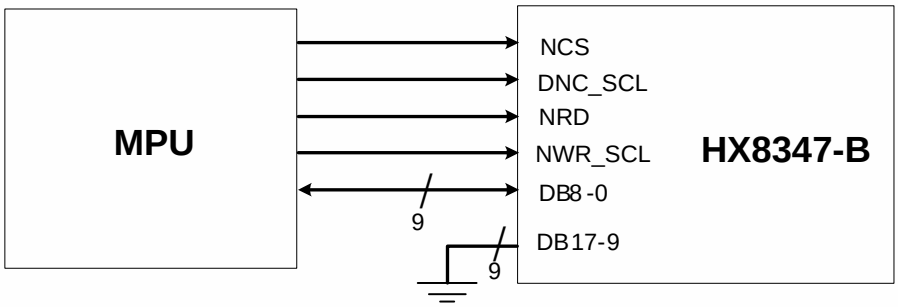


Figure 4.13: Example of I80 system 9-bit parallel bus interface type I

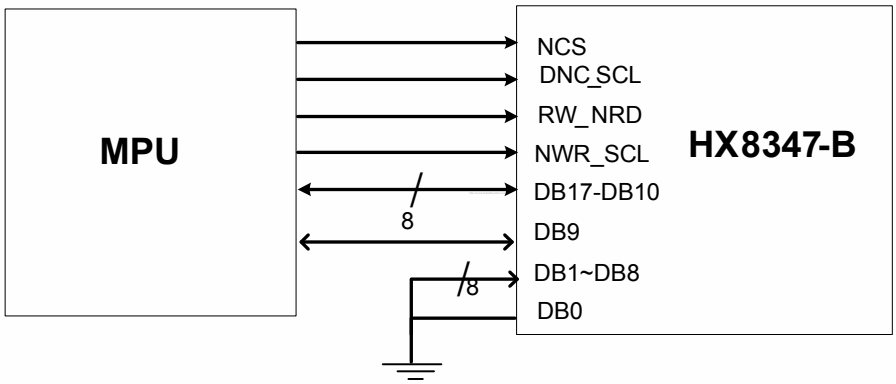


Figure 4.14: Example of I80 system 9-bit parallel bus interface type II

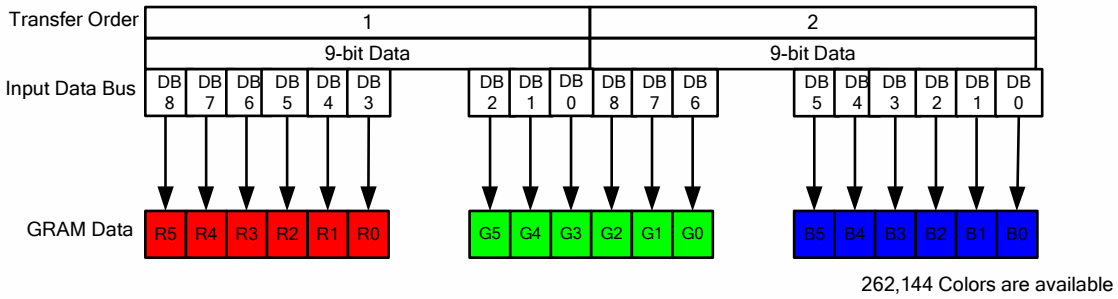


Figure 4.15: Input data bus and GRAM data mapping in 9-bit bus system interface with 18-bit-data input (“IM3, IM2, IM1, IM0”=”1001”)

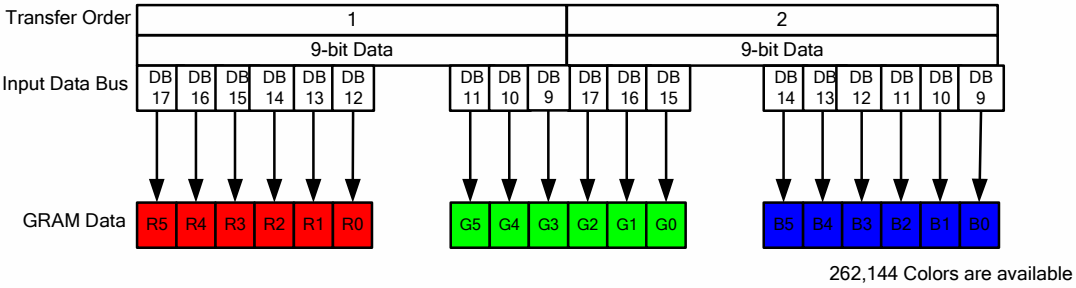


Figure 4.16 Input Data Bus and GRAM Data Mapping in 9-Bit Bus System Interface with 18 Bit-Data Input (“IM3, IM2, IM1, IM0”=”1011”)

8-bit Parallel Bus System Interface

The I80-system 8-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins ""IM3, IM2, IM1, IM0" pins to "0001". And I80-system 8-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ""IM3, IM2, IM1, and IM0"pins to"0011". Figure 4.19 is the example of type I interface with I80 microcomputer system interface. And Figure 4.20 is the example of type II interface with I80 microcomputer system interface.

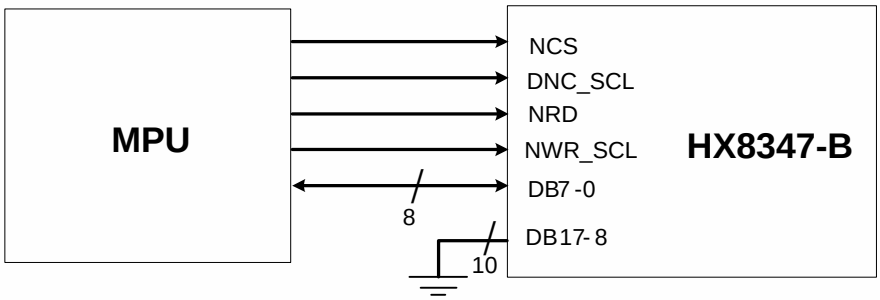


Figure 4.17: Example of I80 system 8-bit parallel bus interface type I

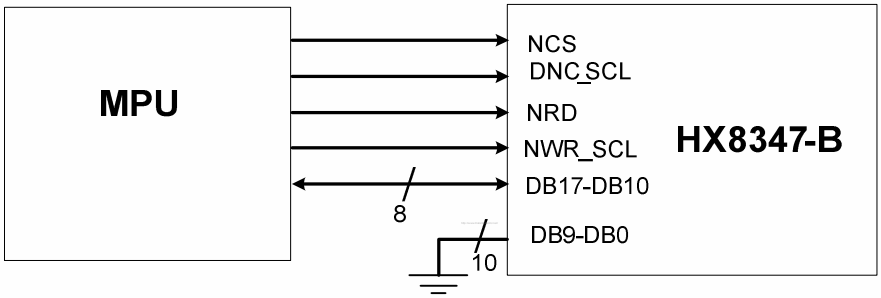


Figure 4.18: Example of I80 system 8-bit parallel bus interface type II

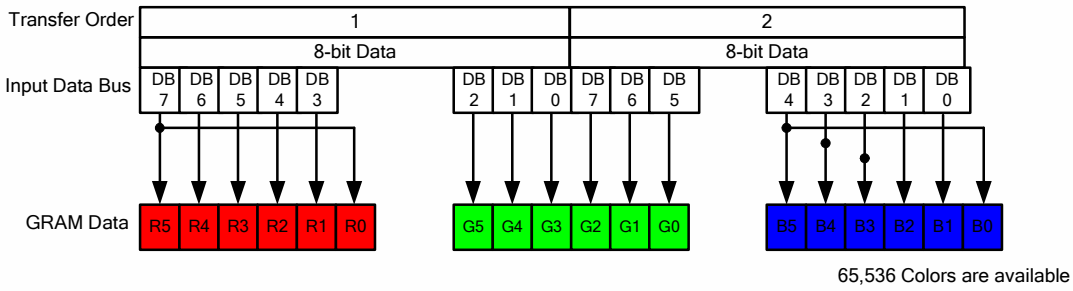


Figure 4.19: Input data bus and GRAM data mapping in 8-bit bus system interface with 16-bit-data input (TRI = '0' and "IM3, IM2, IM1, IM0"="0001")

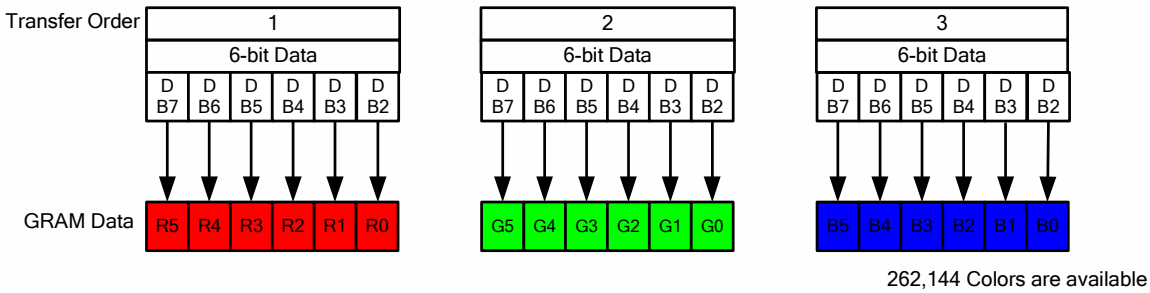


Figure 4.20: Input data bus and GRAM data mapping in 8-bit bus system interface with 18-bit-data input (TRI = '1' and "IM3, IM2, IM1, IM0"="0001)

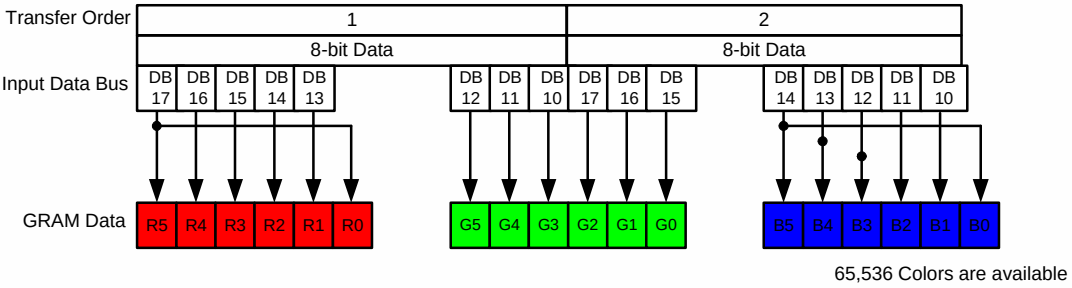


Figure 4.21: Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 16 Bit-Data Input (TRI = '0' and "IM3, IM2, IM1, IM0"="0011")

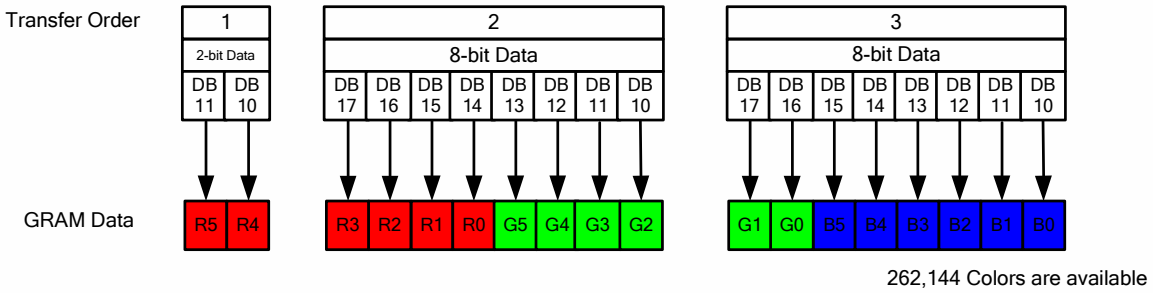


Figure 4.22: Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18 Bit-Data Input (TRI = '1', DFM = '0' and "IM3, IM2, IM1, IM0"="0011")

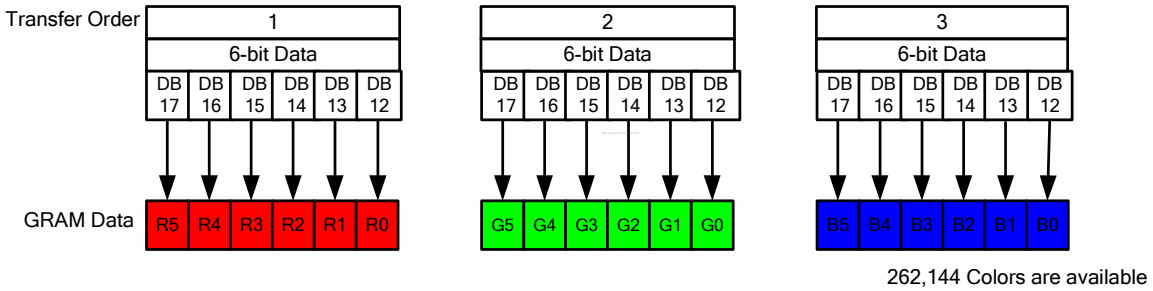


Figure 4.23: Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18 Bit-Data Input (TRI = '1', DFM = '1' and "IM3, IM2, IM1, IM0"="0011")

MCU Data Color Coding for RAM data ***Read***

- Parallel 8-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0001")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
0	X	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
		x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.11: 8-bit parallel interface type I GRAM read table

- Parallel 16-Bit Bus Interface type I (IM3,IM2,IM1,IM0="0000")

Register		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
TRI	DFM	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
				R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
		x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
		x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
		x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B1	B0	

Table 4.12: 16-bit parallel interface type I GRAM read table

- Parallel 9-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.13: 9-bit parallel interface type I GRAM read table

- Parallel 18-Bit Bus Interface type I (IM3,IM2,IM1,IM0="1000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4.14: 18-bit parallel interface type I GRAM read table

- Parallel 8-Bits Bus Interface (IM3,IM2,IM1,IM0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	R5	R4	R3	R2	R1	G5	G4	G3	X	X	X	X	X	X	X	X	X	X	65K-Color
	G2	G1	G0	B5	B4	B3	B2	B1	X	X	X	X	X	X	X	X	X	X	

Table 4.15: 8-Bits Parallel Interface type II GRAM Read Table

- Parallel 16-Bits Bus Interface (IM3,IM2,IM1,IM0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	0	X	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	R5	R4	R3	R2	R1	G5	G4	G3	X	G2	G1	G0	B5	B4	B3	B2	B1	X	65K-Color

Table 4.16: 16-Bits Parallel Interface type II GRAM Read Table

- Parallel 9-Bits Bus Interface (IM3,IM2,IM1,IM0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	X	X	X	X	X	X	X	X	X	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	X	X	X	X	X	X	X	X	X	

Table 4.17: 9-Bits Parallel Interface type II GRAM Read Table

- Parallel 18-Bits Bus Interface (IM3,IM2,IM1,IM0="1010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	1	0	X	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4.18: 18-Bits Parallel Interface type II GRAM Read Table

4.1.3 Serial Bus System Interface

The HX8347-B supports three kinds' serial bus interface in register-content mode by setting external pins "IM2, IM1,IM0" pins to "10x" 3-wire 24-bits serial interface and "IM2, IM1,IM0" pins to "110" 3-wire 9-bits serial interface and "IM2, IM1,IM0" pins to "111" 4-wire 8-bits serial interface. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), and the serial transfer clock signal (NWR_SCL).

4.1.3.1 3-wire serial interface

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to "01110", and the least significant bit of the identification code must be set as the external pin IM0 input as "ID".

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to "0" when writing data to the index register or reading the status and it must be set to "1" when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command or GRAM read

Table 4.19: The Function of RS and R/W Bit Bus

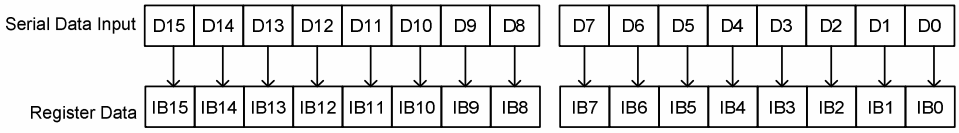


Figure 4.24: Index Register Read/Write Timing in 3-wire Serial Bus System Interface

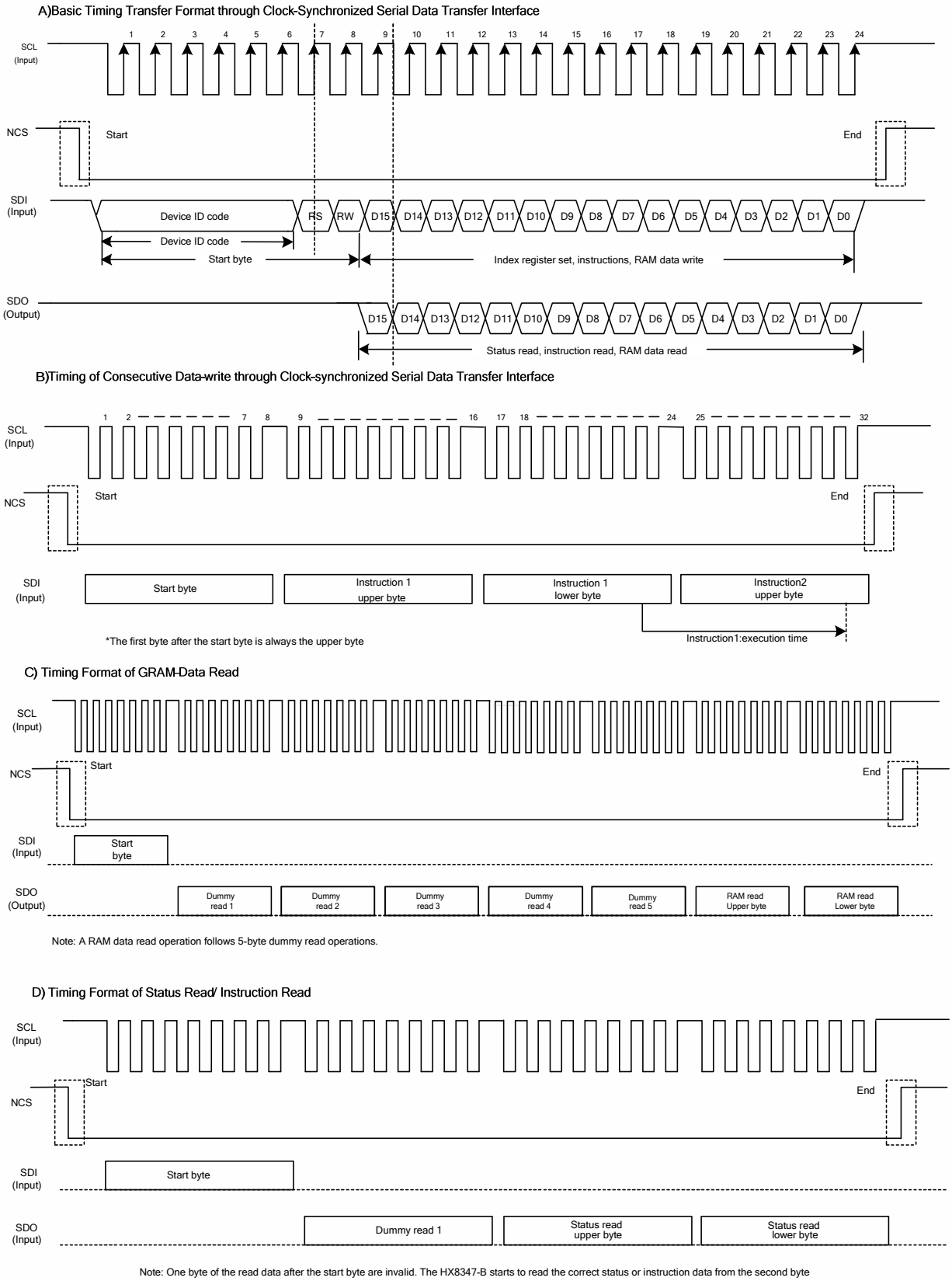


Figure 4.25: Index Register Read/Write Timing in 3-wire Serial Bus System Interface

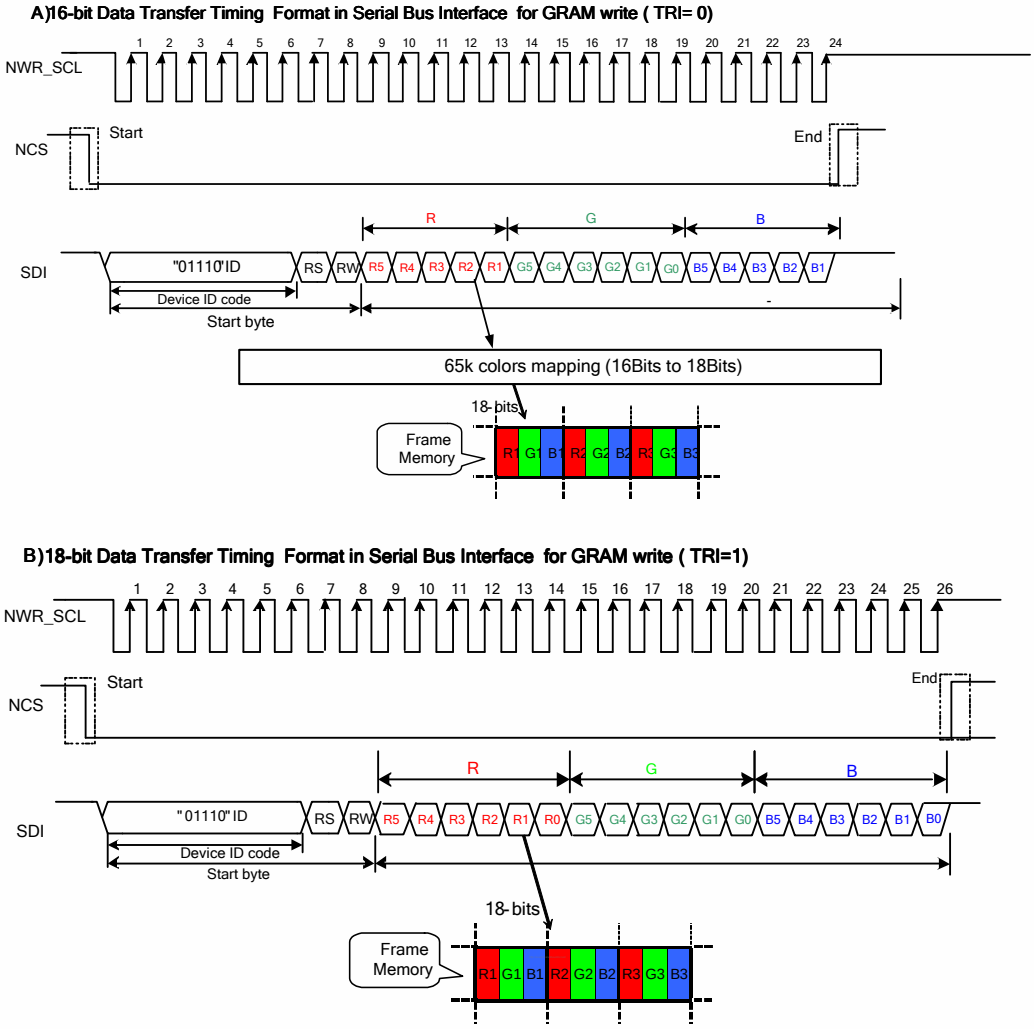


Figure 4.26: Data Write Timing in 3-wire Serial Bus System Interface

4.1.3.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC_SCL pin. If DNC_SCL is low, the transmission byte is command byte. If DNC_SCL is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR_SCL clock pulse or SDI data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

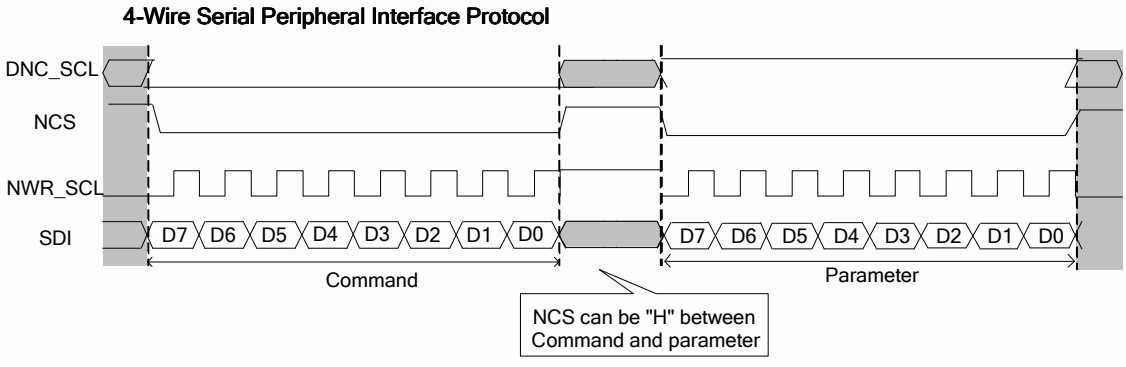


Figure 4.27: Index Register Write Timing in 4-wire Serial Bus System Interface

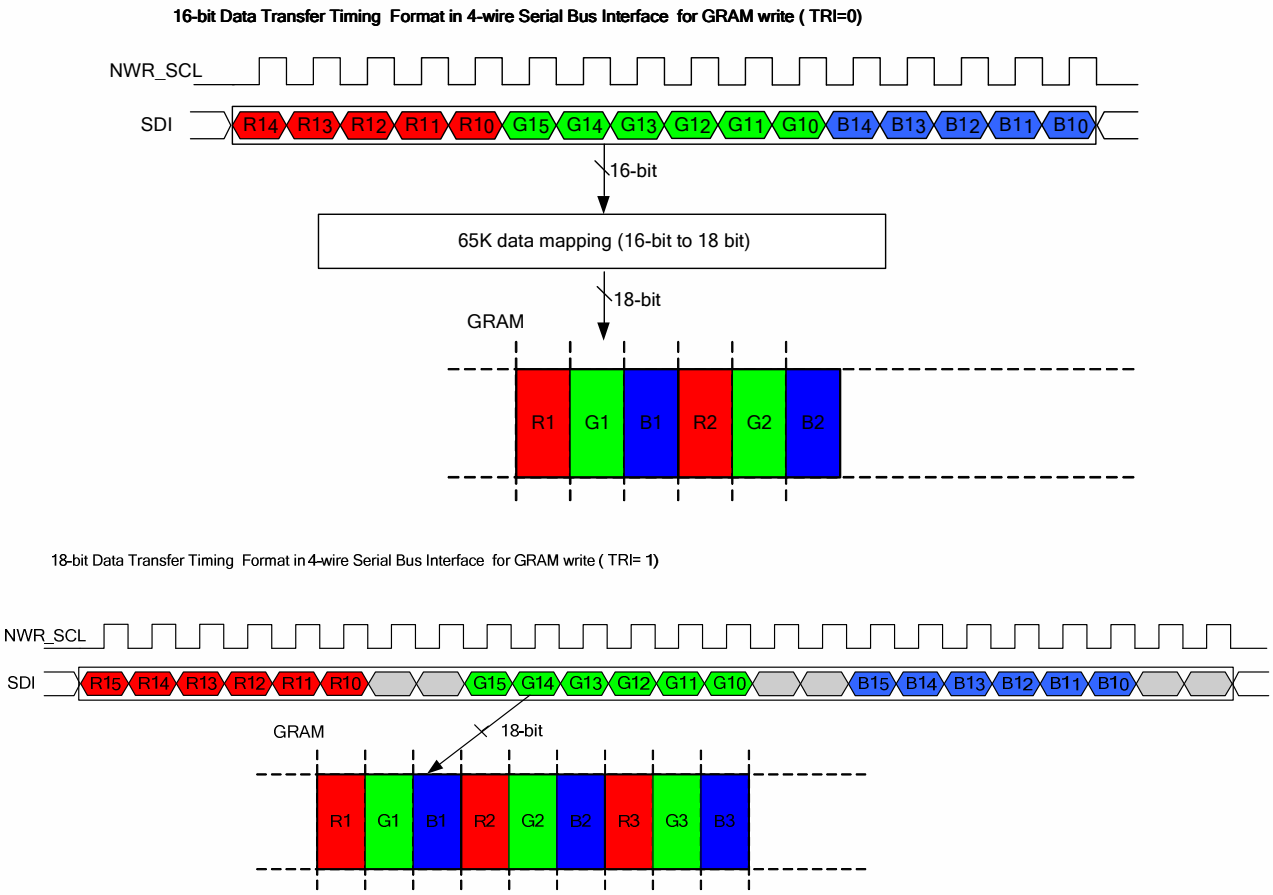


Figure 4.28: Data Write Timing in 4-wire Serial Bus System Interface

4.1.3.3 3-wire serial interface

Serial data must be input to **SDA** in the sequence D/NC, D7 to D0. The HX8347-B reads the SDA data at the rising edge of **SCL** signal. The first bit of serial data D/NC is data/command flag. When D/NC = "1", D7 to D0 bits are GRAM data or command parameters. When D/NC = "0" D7 to D0 bits are commands.

SCL is not a continuous clock and it can be stopped by the host MCU when **SCL** is low or high after a rising edge of **SCL** for D0 in the writing mode.

3-Wire Serial Peripheral Interface Data Format

When D/NC = "0", transmission byte (TB) must be a command
When D/NC = "1", transmission byte (TB) must be a command parameters or GRAM data

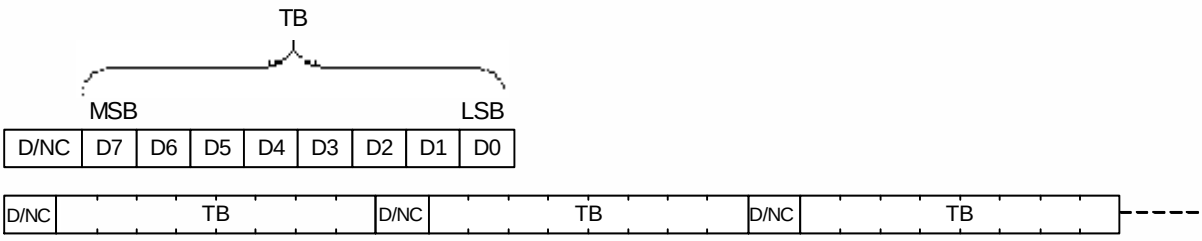


Figure 4.29: Serial Peripheral Interface Data Format

Write operation in serial peripheral interface

The host MCU drives the **NCS**pin low and starts by setting the D/CX-bit on **SDA**. The bit is read by the display on the first rising edge of **SCL**. On the next falling edge of **SCL** the MSB data bit (D7) is set on **SDA** by the MCU. On the next falling edge of **SCL** the next bit (D6) is set on **SDA**. This continues until all 8 Data bits have been transmitted as shown in Figure 4.30 and Figure 4.31.

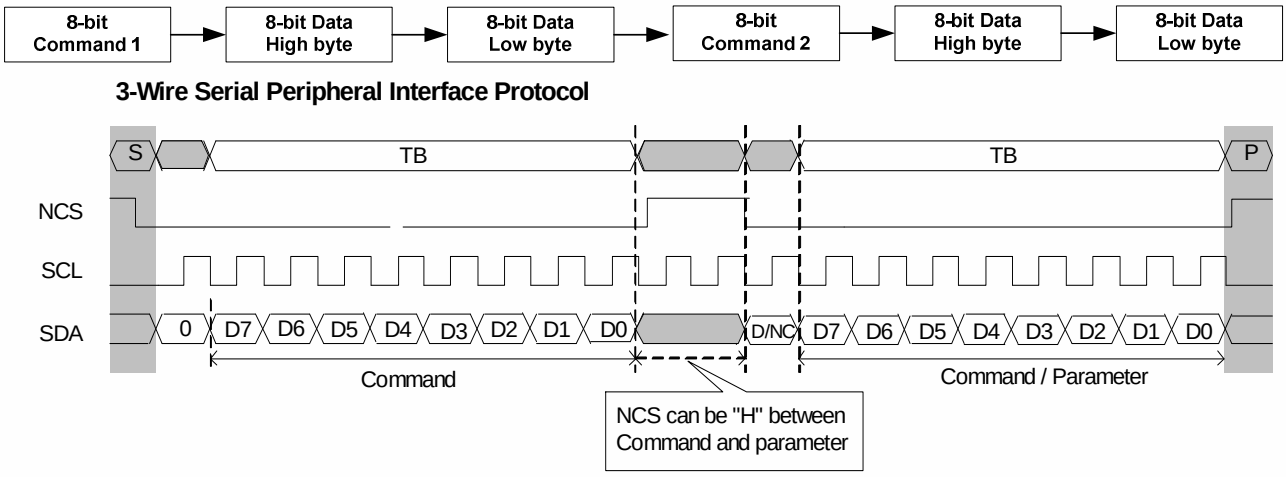


Figure 4.30: Serial Peripheral Interface Protocol in Command Write Operation

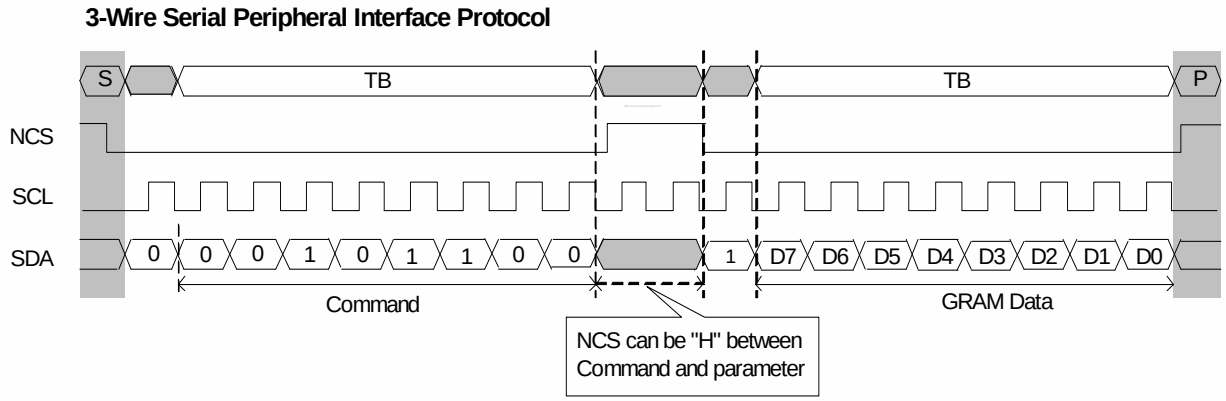


Figure 4.31: Serial Peripheral Interface Protocol in GRAM Write Operation

Read operation in serial peripheral interface

When users need to read back the register or GRAM data, the register R66h must be set as “1” first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

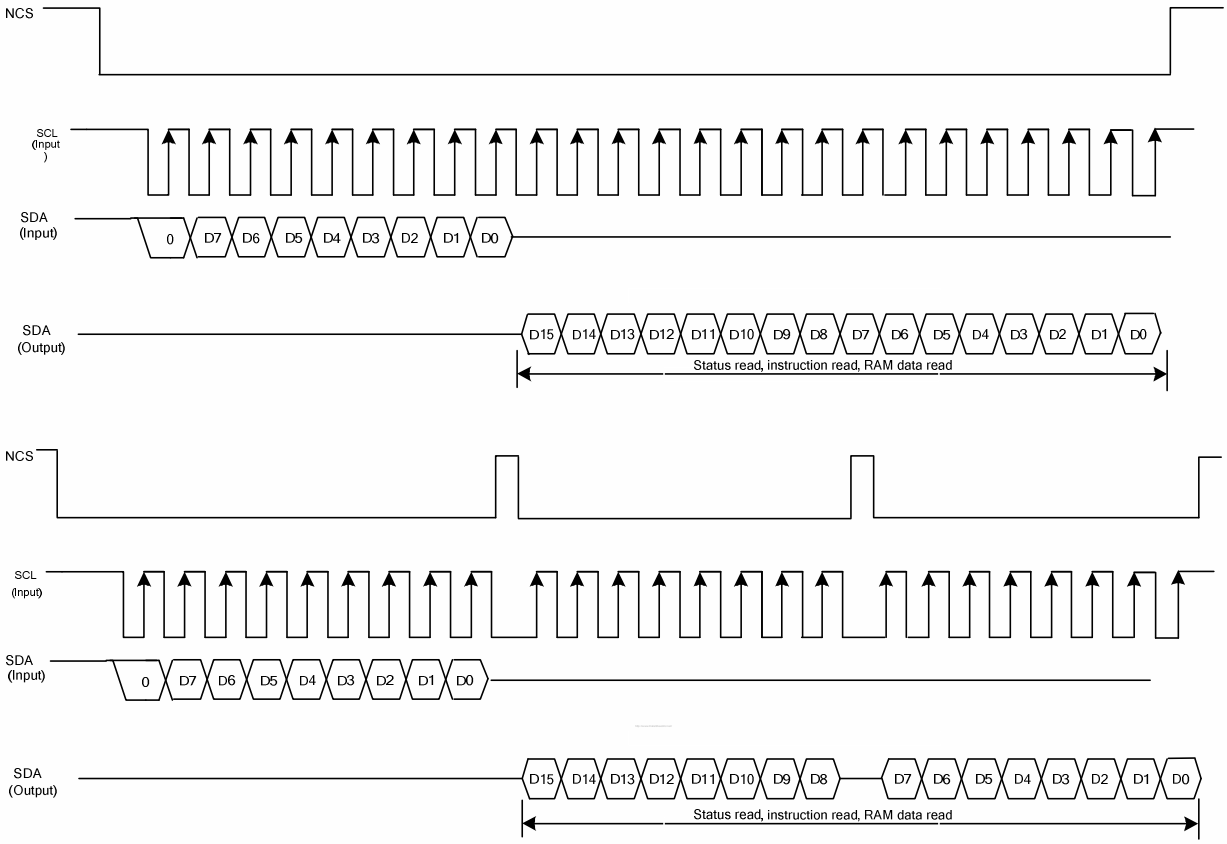


Figure 4.32: Command Read Operation in Serial Peripheral Interface

There are two types data format to write display data at Serial data bus Interface and it is as same as 8-bit bus Interface.

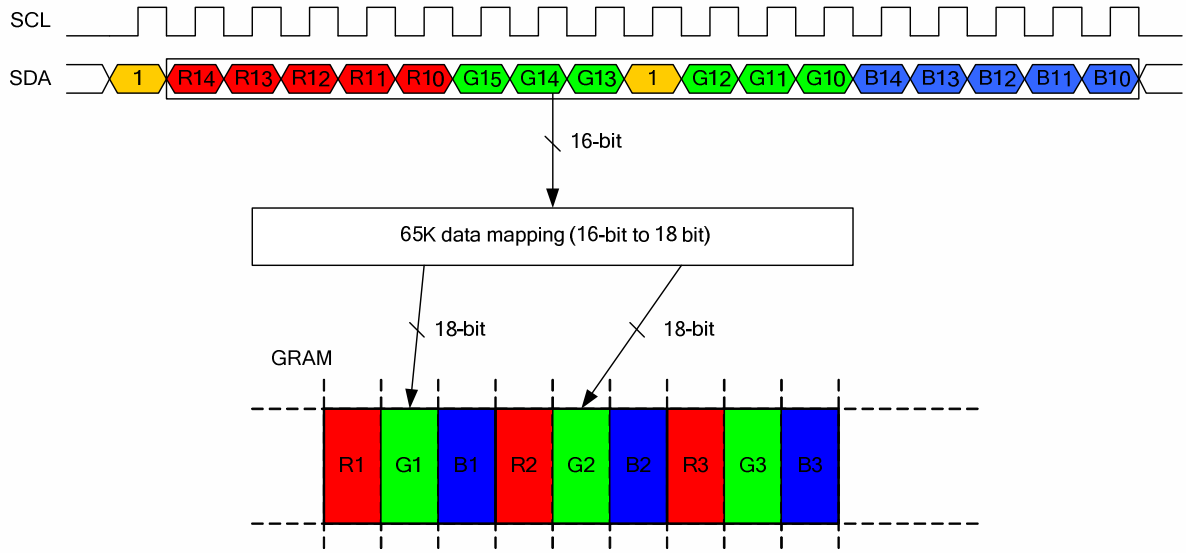


Figure 4.33: Write data for RGB 5-6-5-bits (65k colors) input (TRI='0')

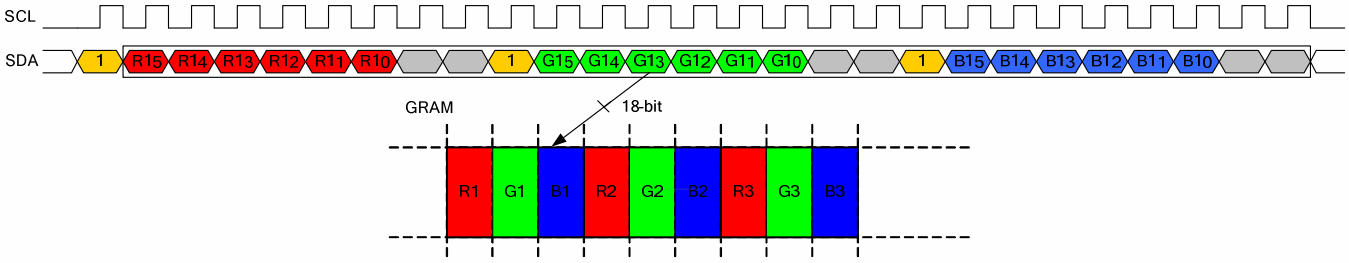


Figure 4.34: Write data for RGB 6-6-6-bits(262k colors) (TRI='1')

4.2 Vsync Interface

The HX8347-B supports the VSYNC interface mode that executes the display operation by the internal clocks. The internal clocks is generated from internal oscillators and synchronized with the frame synchronization signal VSYNC. When the VSYNC interface mode is selected, the interface display a moving picture through system interface with minimum modification that re-writes display data to the internal GRAM in a high speed RAM function. The VSYNC interface can be used by setting DM1-0=10 and RM=0.

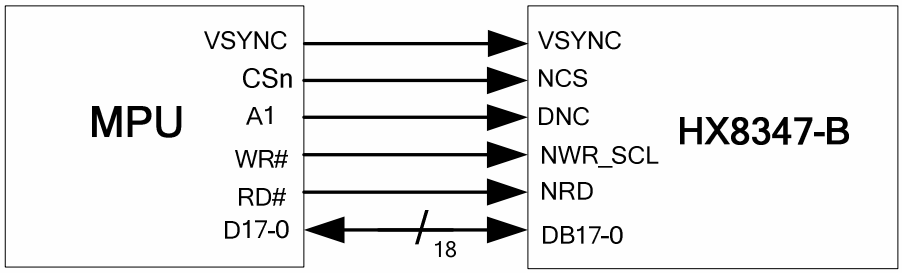


Figure 4.35: VSYNC Interface to MPU

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

Table 4.20: DIM Bit Set

When the HX8347-B is set up in VSYNC interface mode, the interface is used to display a moving picture when writing data to GRAM in high speed with low power consumption. Therefore, the VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface. It requires GRAM write speed more than the minimum value that system processed and calculated. The internal clock of VSYNC interfaces can be computed by the following formula that used some parameters with FP, BP and display lines duration (NL):

$$Internal\,ocillator\,clock\,(f_{osc})[Hz] = Frame\,Frequency \times [Display\,Lines(NL) + FP + BP] \times RTN \times frequency\ \ fluctuation$$

The parameter of frequency fluctuation is ascribed to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

The minimum speed for RAM can be computed by the following formula:

$$The\ Min.\ RAM\ Write\ Speed\ [Hz] \geqq \frac{240 \times DisplayLines(NL) \times f_{osc}}{[Back\ Proch(BP) + DisplyLines(NL) - margin\ lines] \times RTN}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation. The calculated value is the theoretical value that the HX8347-B start the RAM write operation must be taken into account. In other words, the actual value of RAM write speed must be more than theoretical value that calculated from forward formula by getting an internal oscillator clock (fosc) first.
An example of internal oscillator clock (fosc) and minimum speed for RAM writing set up in VSYNC interface mode is as follows.

Example
Display size: 240RGB*320 lines
Lines of be used: 320 lines
FP: 2 lines (0010)
BP: 14 lines (1110)

Frequency fluctuation: 5%
Frame frequency: 60Hz

Internal oscillator clock (fosc) [Hz] = 60 × [320 + 2 +14] × 16 × (1.05/0.95) ≒ 354 kHz
The Min. RAM Write Speed [Hz] ≧ 240 × 320 × 354k /{ [14 + 320 -2] × 16} ≒ 5.11MHz

In this example, the minimum RAM write speed of VSYNC interface is 5.11MHz and then necessary to setting enough or more on the falling edge of guarantees the completion write operation before the HX8347-B initiate the display operation and make it possible to re-write the display area set previously. Further, if the display area were different with the anterior example, the calculated result and margin setting would be revised. For example, if the display area is smaller than that, an extra will be created between the RAM write operation and display with regard to each line.
When the HX8347-B make the transition with system interface mode and VSYNC interface mode, the difference between that is the used of signal VSYNC for synchronization. Therefore, both of them are used the internal oscillator to generate the reference clock. The Figure 4.36 illustrates the process of VSNC interface with internal clock and system interface with internal clock mode transition, which is shown by setting register set.

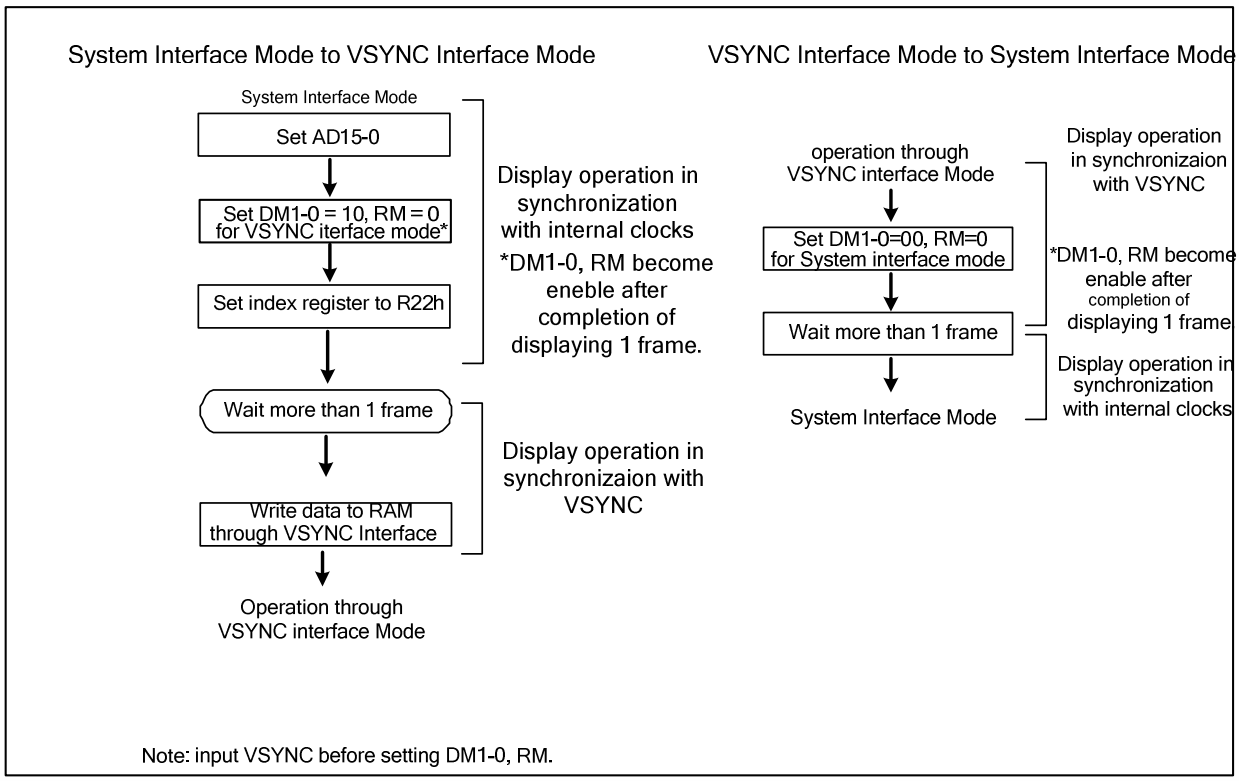


Figure 4.36: VSYNC Interface with Internal Clock and System Interface with Internal Clock Mode Transition

When HX8347-B is set up on VSYNC interface mode, it would access RAM in high speed with low power consumption for displaying a moving picture. But the partial display function, vertical scroll function and interlaced scan function are invalidity functions in VSYNC interface mode.

5.3 RGB Interface

The HX8347-B supports the RGB interface that display operations that executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK). The display data are transferred in pixel unit via DB17-0 bits. The RGB interface can be used by setting **DM[1:0]="01"** and **RM = "1"**. In RGB interface mode, with use of a window address function, enables to display data in a moving picture area and makes it possible to transfer the display only by re-writing a screen with minimum data transfers.

When the HX8347-B set up in RGB interface mode, a BP starts on the falling edge of VSYNC signal, which is made at the beginning by the display operation. Furthermore, the display duration (NL4-0) mean the numbers of driving lines is the subsequent data of display operation. And then the FP starts. The FP period would be continues until the next input of the VSYNC signal.

General timing diagram in RGB interface is as follow:

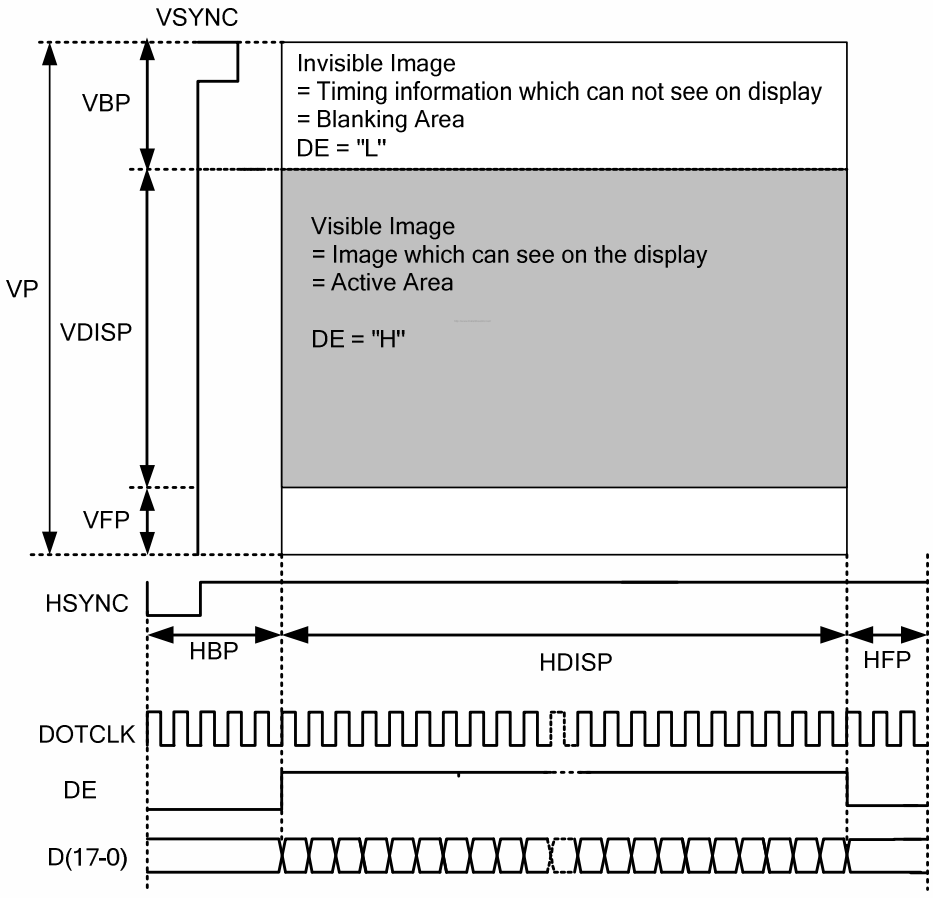


Figure 4.37: RGB Interface Circuit Input Timing Diagram

The data written to the internal GRAM were synchronized with DOTCLK inputs when DE is setting low. Contrary to set DE high, the data written to the GRAM would be entered to the process of using the system interface.

Moving picture mode

HX8347-B has the RGB interface to display moving picture and incorporates GRAM to store display data. The Figure 4.38 is shown the process of RAM access via the system interface with rewriting still picture and then return to RGB interface while displaying a moving picture in RGB interface mode.

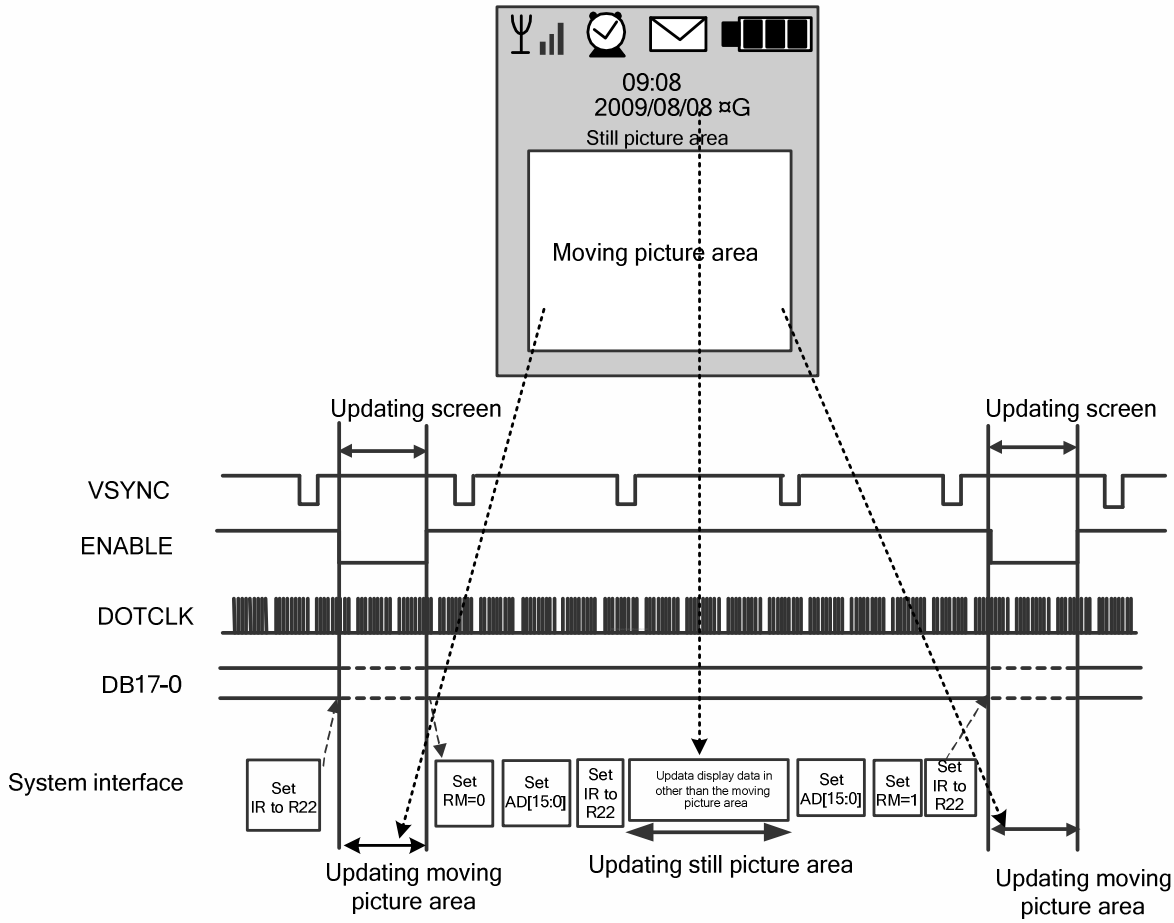


Figure 4.38: Example of Update Still and Moving Picture

When set up in RGB interface mode, the used of high speed RAM write mode to write data to the internal GRAM and GRAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC. Furthermore, the FP period would be continues until the next input of the VSYNC signal.

When the HX8347-B make the transition with system interface mode and RGB interface mode, the sequence of switching process must be following as Figure 4.39.

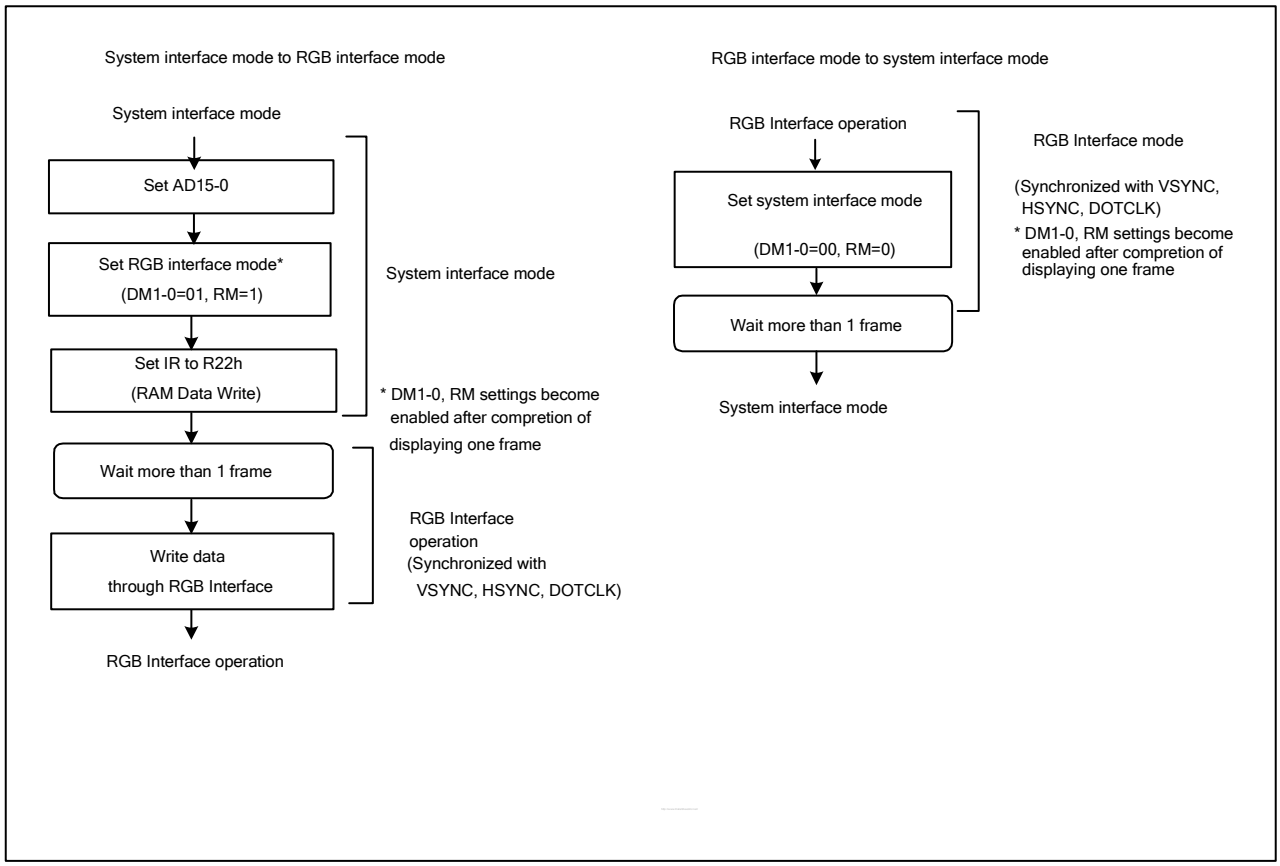


Figure 4.39: Transition between System Interface Mode and RGB Interface Mode

When operate in RGB interface and the RAM write data transfer through system interface, the sequence of switching process must be follow as Figure 4.40.

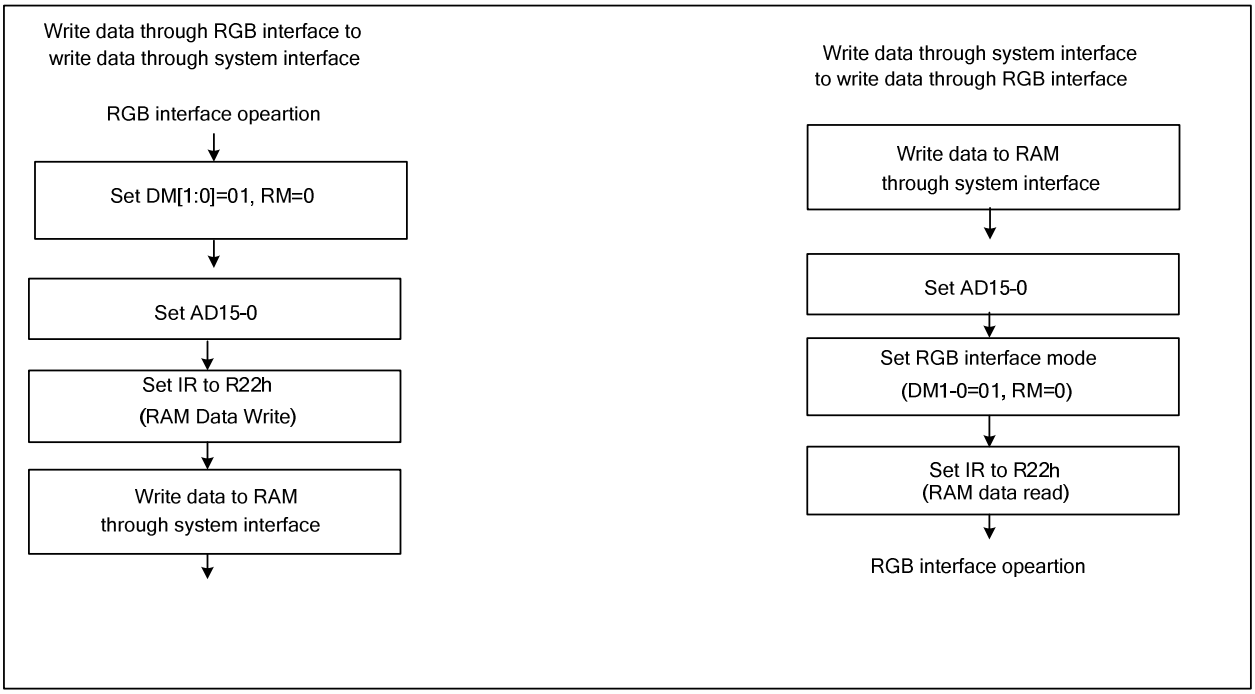


Figure 4.40: RAM Data Write Sequence through System Interface or RGB Interface during RGB Interface Mode

The HX8347-B supports 18-/16-/6-bit bus RGB interface by setting register RIM1-0 only through the system interface.

RIM[1:0]		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
0	0	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bits data
0	1	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
1	0	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
		x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

18-bit bus RGB interface

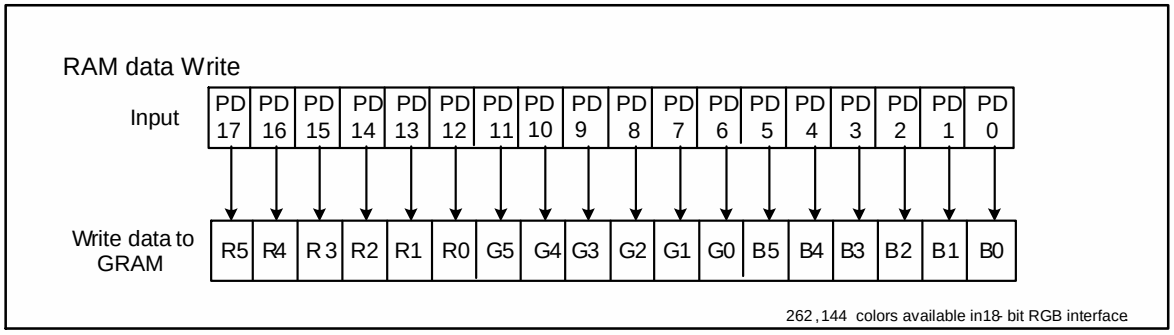


Figure 4.41: Data Format for 18-bit Interface

16-bit bus RGB interface

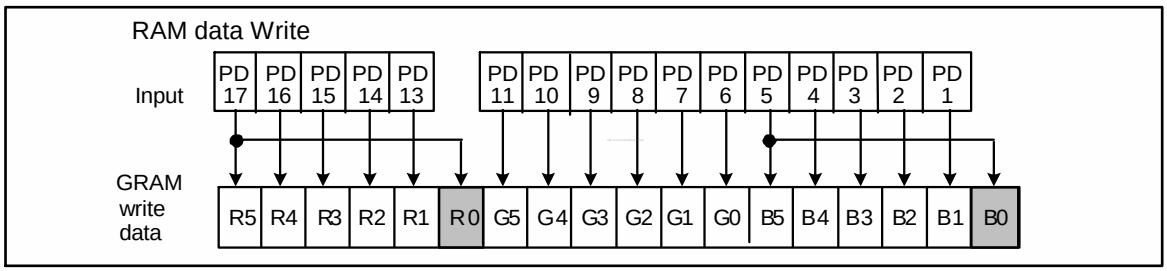


Figure 4.42: Data Format for16-bit Interface

6-bit bus RGB interface

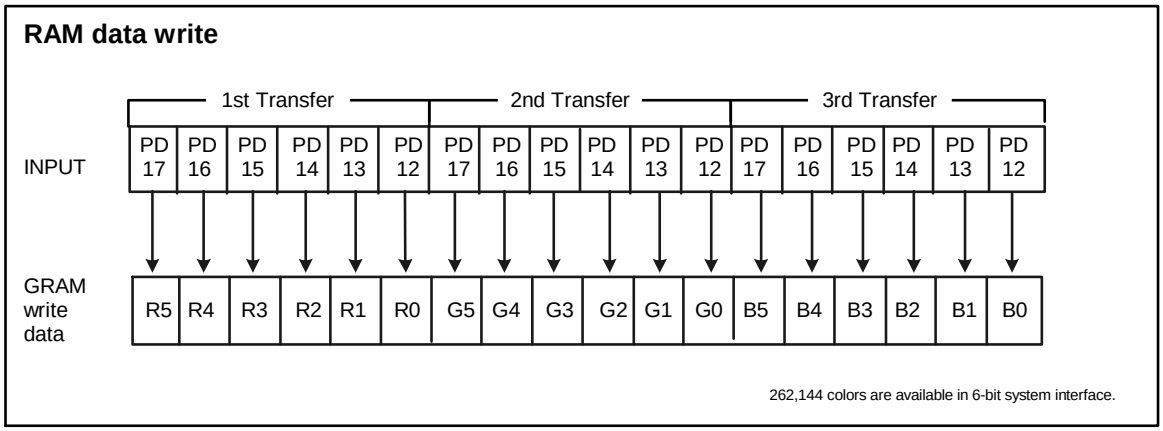


Figure 4.43: Data Format for 6-bit Interface

5. Functional Description

5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

(00,00)H	(00,01)H	(00,02)H	---------	(00,EC)H	(00,ED)H	(00,EE)H	(00,EF)H
(01,00)H	(01,01)H	(01,02)H	---------	(01,EC)H	(01,ED)H	(01,EE)H	(01,EF)H
(02,00)H	(02,01)H	(02,02)H	---------	(02,EC)H	(02,ED)H	(02,EE)H	(02,EF)H
(03,00)H	(03,01)H	(03,02)H	---------	(03,EC)H	(03,ED)H	(03,EE)H	(03,EF)H
(04,00)H	(04,01)H	(04,02)H	---------	(04,EC)H	(04,ED)H	(04,EE)H	(04,EF)H
(05,00)H	(05,01)H	(05,02)H	---------	(05,EC)H	(05,ED)H	(05,EE)H	(05,EF)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(13A,00)H	(13A,01)H	(13A,02)H	---------	(13A,EC)H	(13A,ED)H	(13A,EE)H	(13A,EF)H
(13B,00)H	(13B,01)H	(13B,02)H	---------	(13B,EC)H	(13B,ED)H	(13B,EE)H	(13B,EF)H
(13C,00)H	(13C,01)H	(13C,02)H	---------	(13C,EC)H	(13C,ED)H	(13C,EE)H	(13C,EF)H
(13D,00)H	(13D,01)H	(13D,02)H	---------	(13D,EC)H	(13DED)H	(13D17E)H	(13D,EF)H
(13E,00)H	(13E,01)H	(13E,02)H	---------	(13E,EC)H	(13E,ED)H	(13E,EE)H	(13E,EF)H
(13F,00)H	(13F,01)H	(13F,02)H	---------	(13F,EC)H	(13F,ED)H	(13F,EE)H	(13F,EF)H

Table 5.1: GRAM address for display panel position

5.2 GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS**, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 5.2, Table 5.3 and Table 5.4 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

BGR = '0'														
Source	**SS = '0'**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	-------	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
Output	**SS = '1'**	**S718**	**S719**	**S720**	**S715**	**S716**	**S717**	-------	**S4**	**S5**	**S6**	**S1**	**S2**	**S3**
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

BGR = '1'														
Source	**SS = '0'**	**S3**	**S2**	**S1**	**S6**	**S5**	**S4**	-------	**S717**	**S716**	**S715**	**S720**	**S719**	**S718**
Output	**SS = '1'**	**S720**	**S719**	**S718**	**S717**	**S716**	**S715**	-------	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
Bit Allocation		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Table 5.2: GRAM X address and display panel position

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G1	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G311	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G312	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G313	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G314	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G315	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G316	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G317	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G318	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G319	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G320	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 5.3: GRAM address and display panel position (GS ='0')

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G320	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G319	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G318	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G317	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G316	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G315	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G314	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G313	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G312	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G9	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G8	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G7	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G6	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G5	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G4	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G3	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G2	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G1	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 5.4: GRAM address and display panel position (GS ='0')

5.3 Window Address Function

The HX8347-B contains a GRAM address counter (AC), which assigns address for writing pixel data to GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (AM bit and I/D bits) setting. However, the AC will be not updated after reading from GRAM.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: HSA, end: HEA) or the vertical address register (start: VSA, end: VEA). Therefore, data can be written consecutively without thinking a data wrap by those bit function. The address setting of window and GRAM are listed as following:

The window addresses setting range:

00H≦HAS[7:0]≦HEA[7:0]≦EFH
000H≦VSA[8:0]≦VEA[8:0]≦13FH

GRAM address setting range:

HAS[7:0]≦AD[7:0]≦HEA[7:0]
VSA[8:0]≦AD[16:8]≦VEA[8:0]

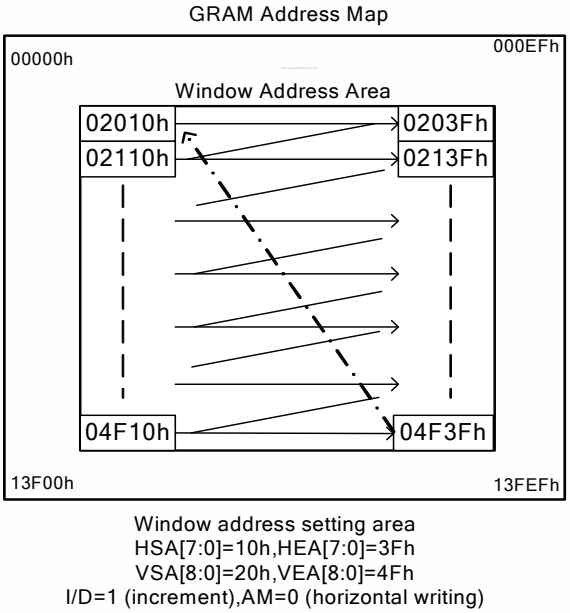


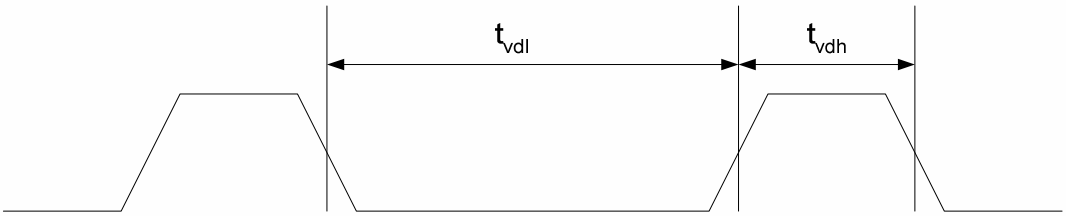
Figure 5.1: GRAM window address mapping example

5.4 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.
Tearing effect function is not support when at RGB interface.

5.4.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of Back Porch Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Figure 5.2: TE Mode 1 Output

Under Mode1, the TE output timing will be defined by TEP[8:0] setting.
Ex: a. TEP[8:0]=0, then TE signal will output after last Line finished.
b. TEP[8:0]=2, then TE signal will output at second Line start.

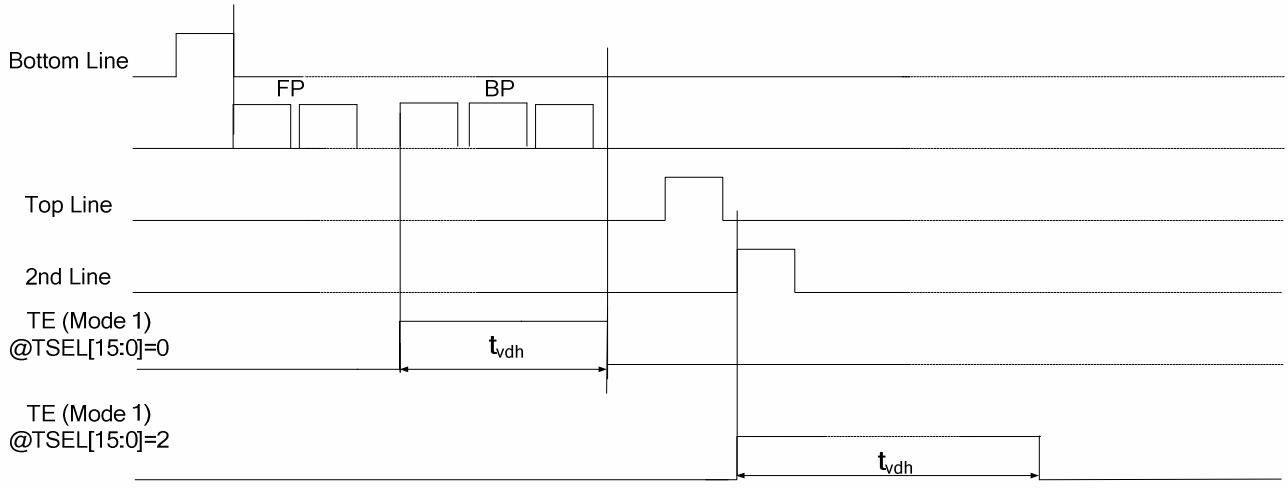
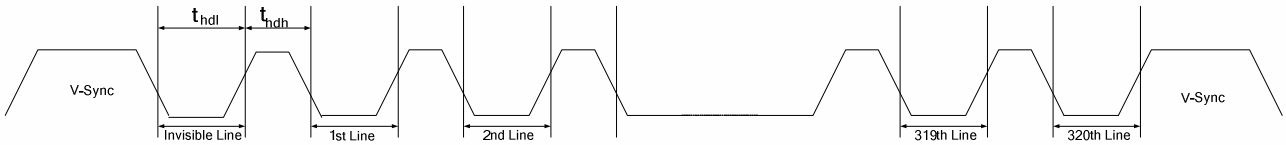


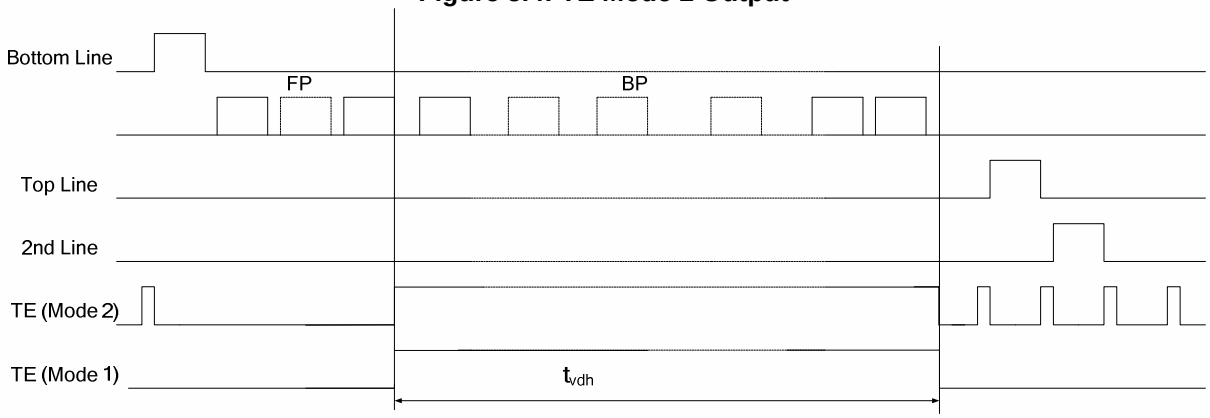
Figure 5.3: TE Delay Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 5.4: TE Mode 2 Output



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 5.5: TE Output Waveform

5.4.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.

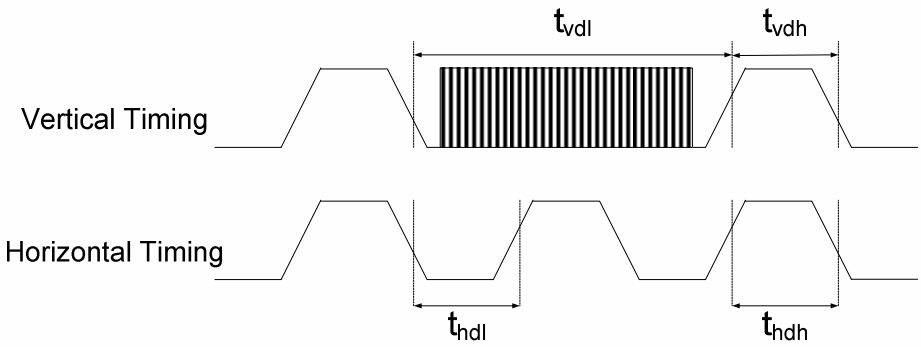


Figure 5.6: Waveform of Tearing Effect Signal

Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	TBD	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Table 5.5: AC characteristics of Tearing Effect Signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

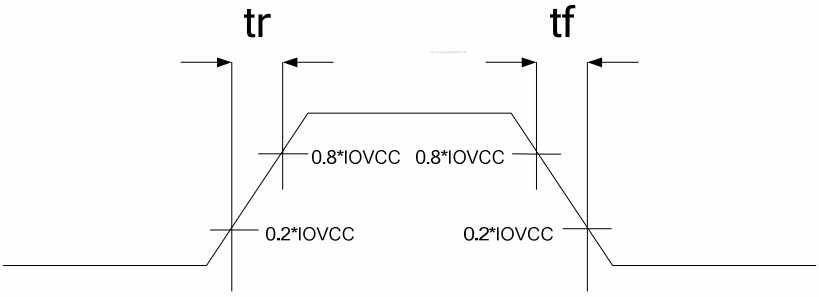


Figure 5.7: Timing of Tearing Effect Signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

5.4.3 Example 1: MPU Write is faster than Panel Read

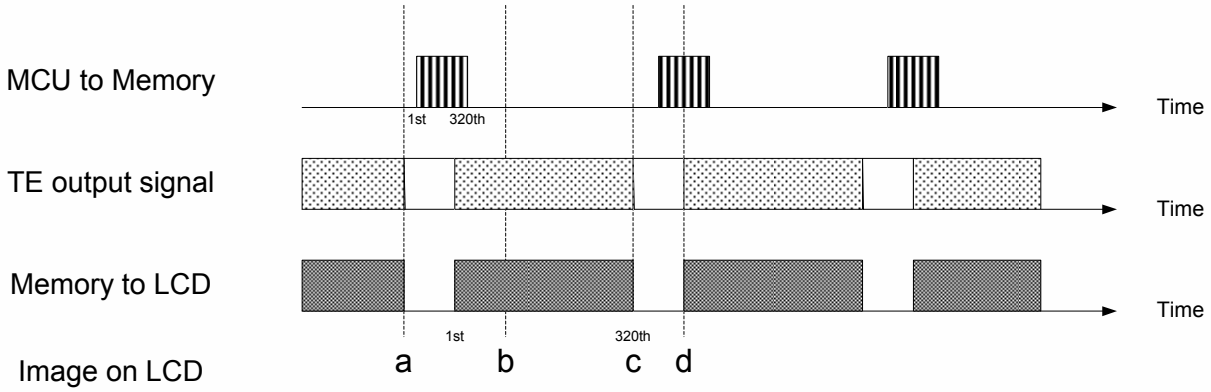


Figure 5.8: Timing of MPU Write is faster than Panel Read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

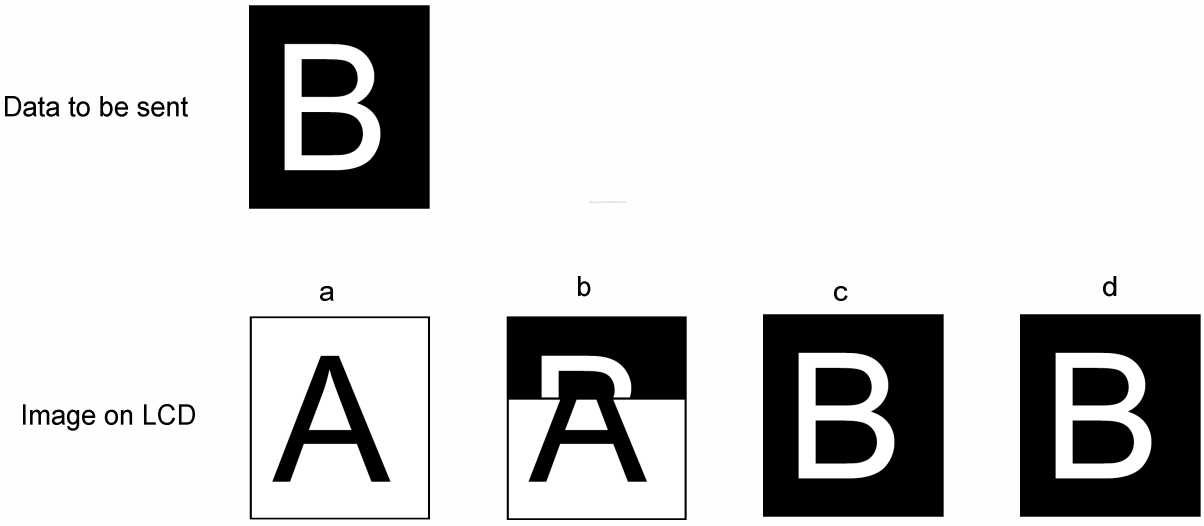


Figure 5.9: Display of MPU Write is faster than Panel Read

5.4.4 Example 2: MPU Write is slower than Panel Read

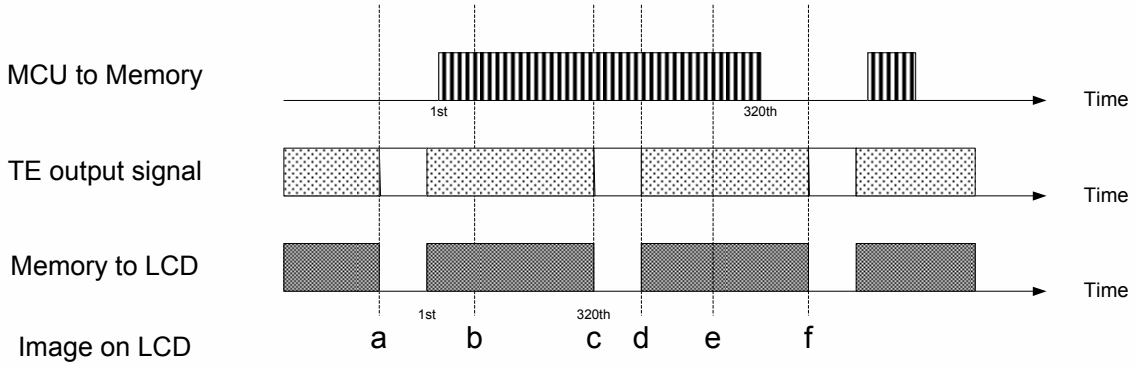


Figure 5.10: Timing of MPU Write is slower than Panel Read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

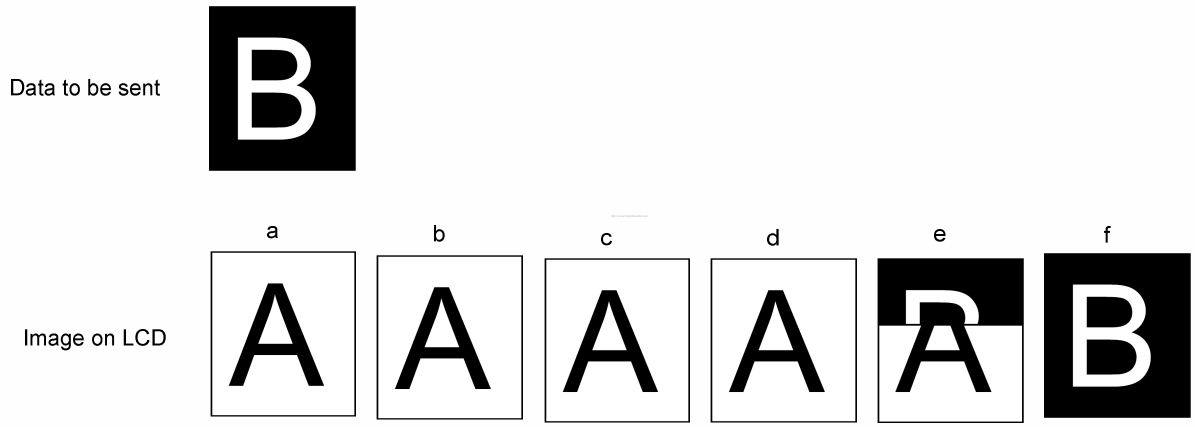


Figure 5.11: Display of MPU Write is slower than Panel Read

5.5 Internal Oscillator

The HX8347-B can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, **FRS [3:0]** bits for initial 2.85MHz internal clock generation. With other dividers setting, the 2.85MHz internal clock can be used to generate clock for other part of the chip using.

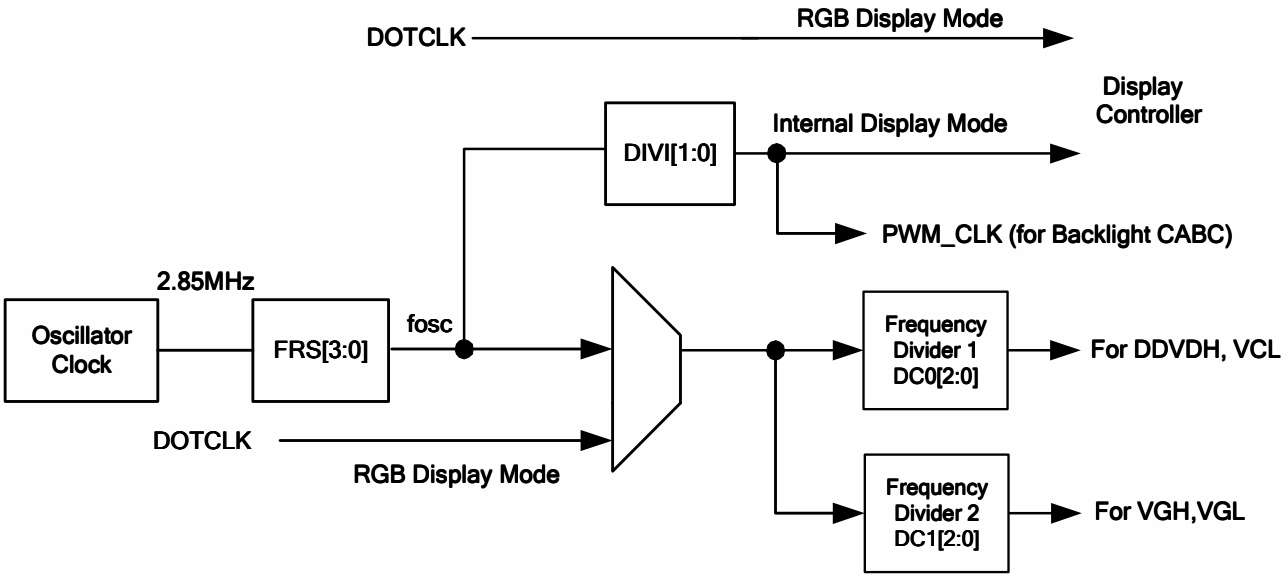


Figure 5.12: HX8347-B Internal Clock Circuit

5.6 Source driver

The HX8347-B contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.7 Gate driver

The HX8347-B contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.8 Scan mode setting

HX8347-B can set register GS and SM bit to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8347-B.

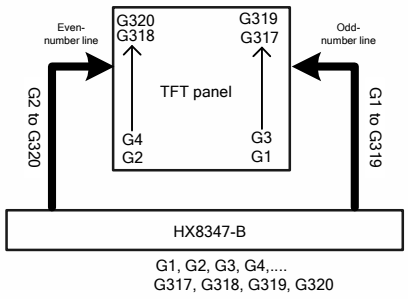
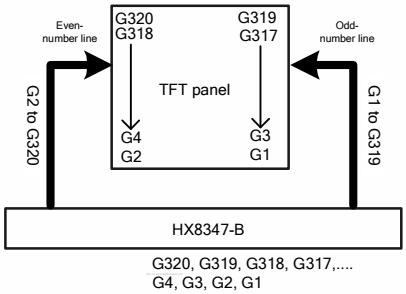
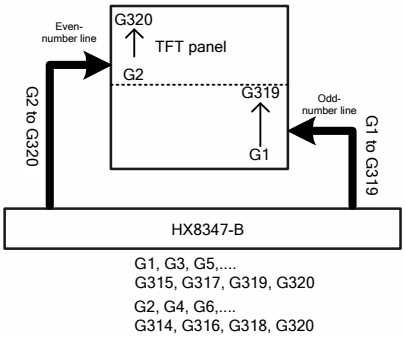
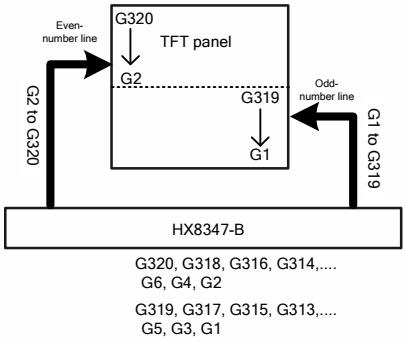
SM	GS	Scan direction
0	0	
0	1	
1	0	
1	1	

Figure 5.13: Gate scan mode

5.9 LCD Power Generation Circuit

5.9.1 Power Supply Circuit

The power circuit of HX8347-B is used to generate supply voltages for LCD panel driving.

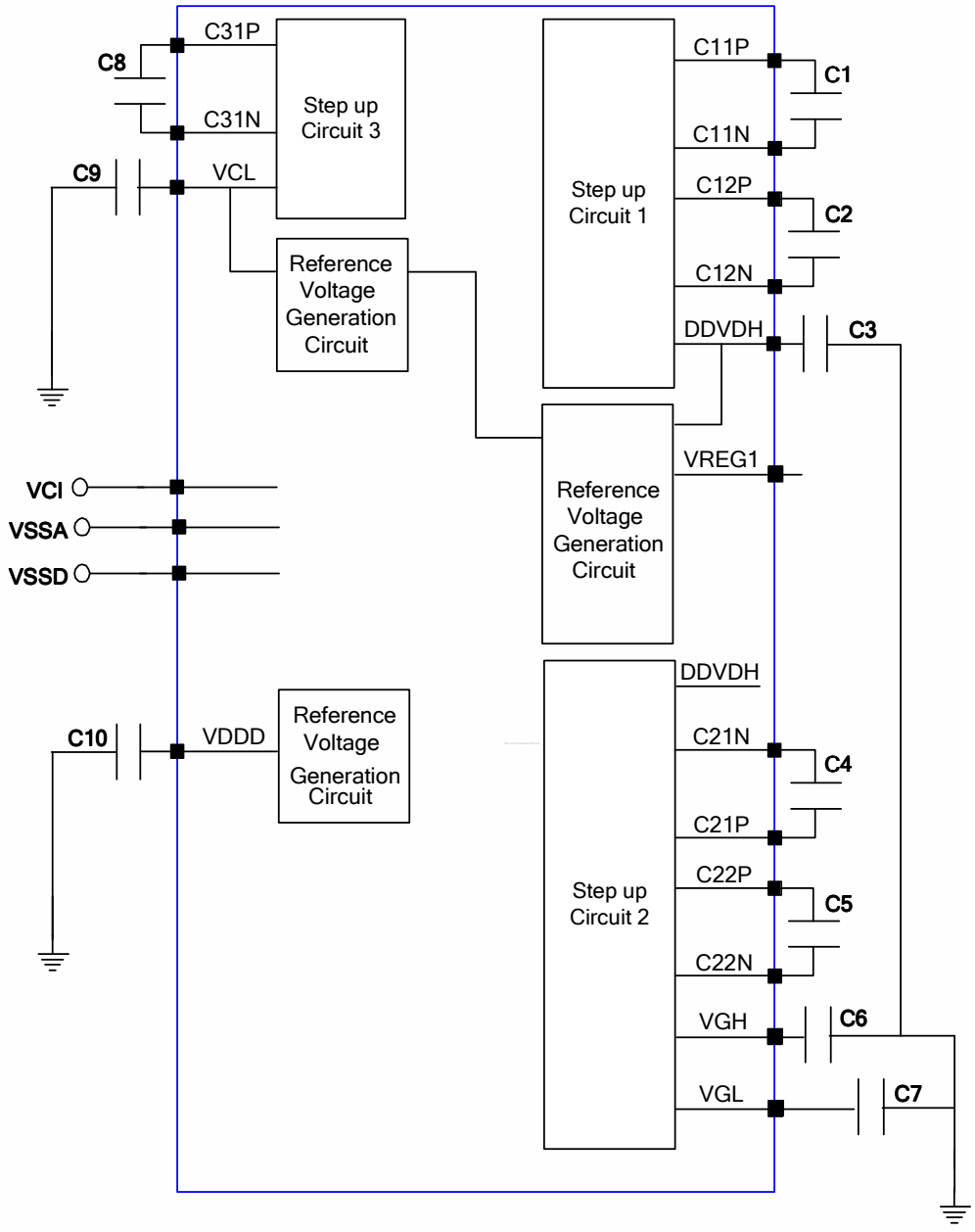


Figure 5.14: The Block Diagram of HX8347-B Power Circuit

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity
C1 (C11P/N)	6V	1µF (B characteristics)
C2 (C12P/N)	6V	1µF (B characteristics)
C3 (DDVDH)	10V	1µF (B characteristics)
C4 (C21P/N)	10V	1µF (B characteristics)
C5 (C22P/N)	10V	1µF (B characteristics)
C6 (VGH)	25V	1µF (B characteristics)
C7 (VGL)	16V	1µF (B characteristics)
C8 (C31P/N)	6V	1µF (B characteristics)
C9 (VCL)	6V	1µF (B characteristics)
C10 (VDDD)	6V	1µF (B characteristics)

Table 5.6: The adoptability of Capacitor

5.9.2 LCD Power Generation Scheme

The boost voltage generated is shown as below.

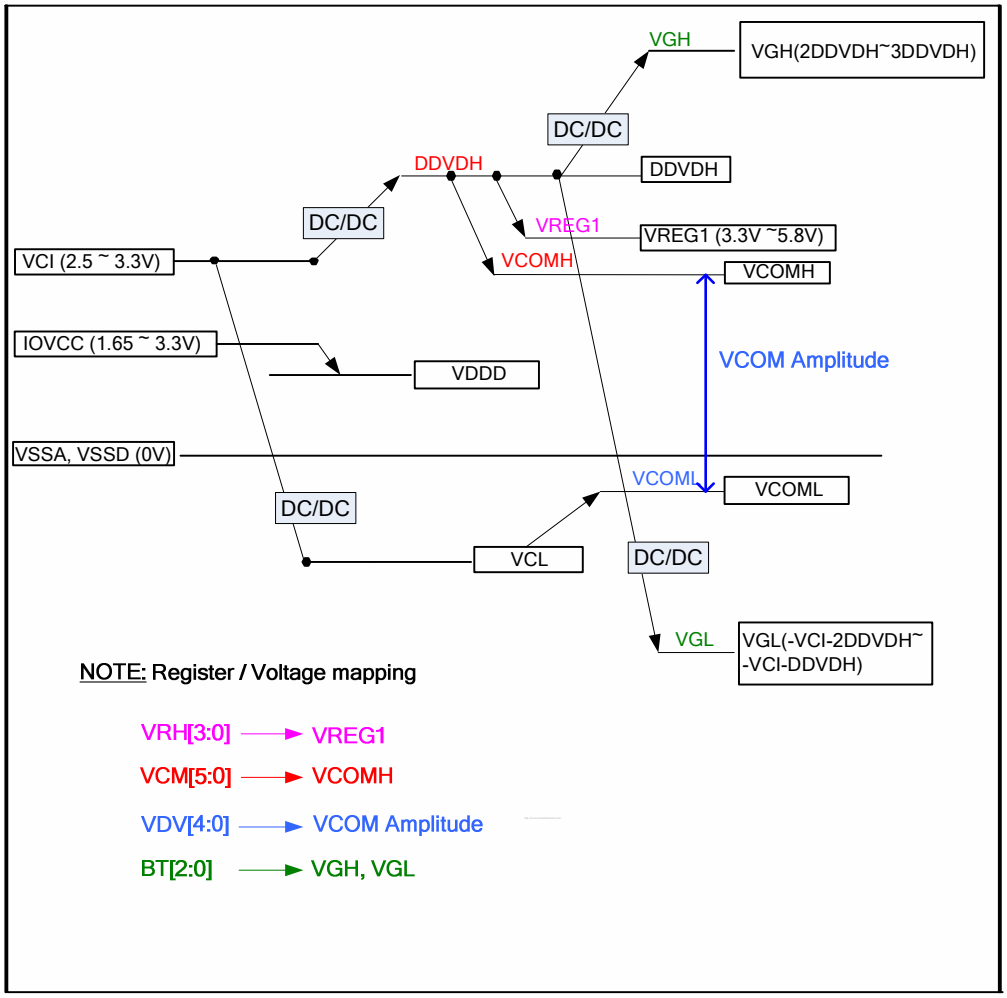


Figure 5.15: LCD Power Generation Scheme

5.10 Gamma Characteristic Correction Function

The HX8347-B incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

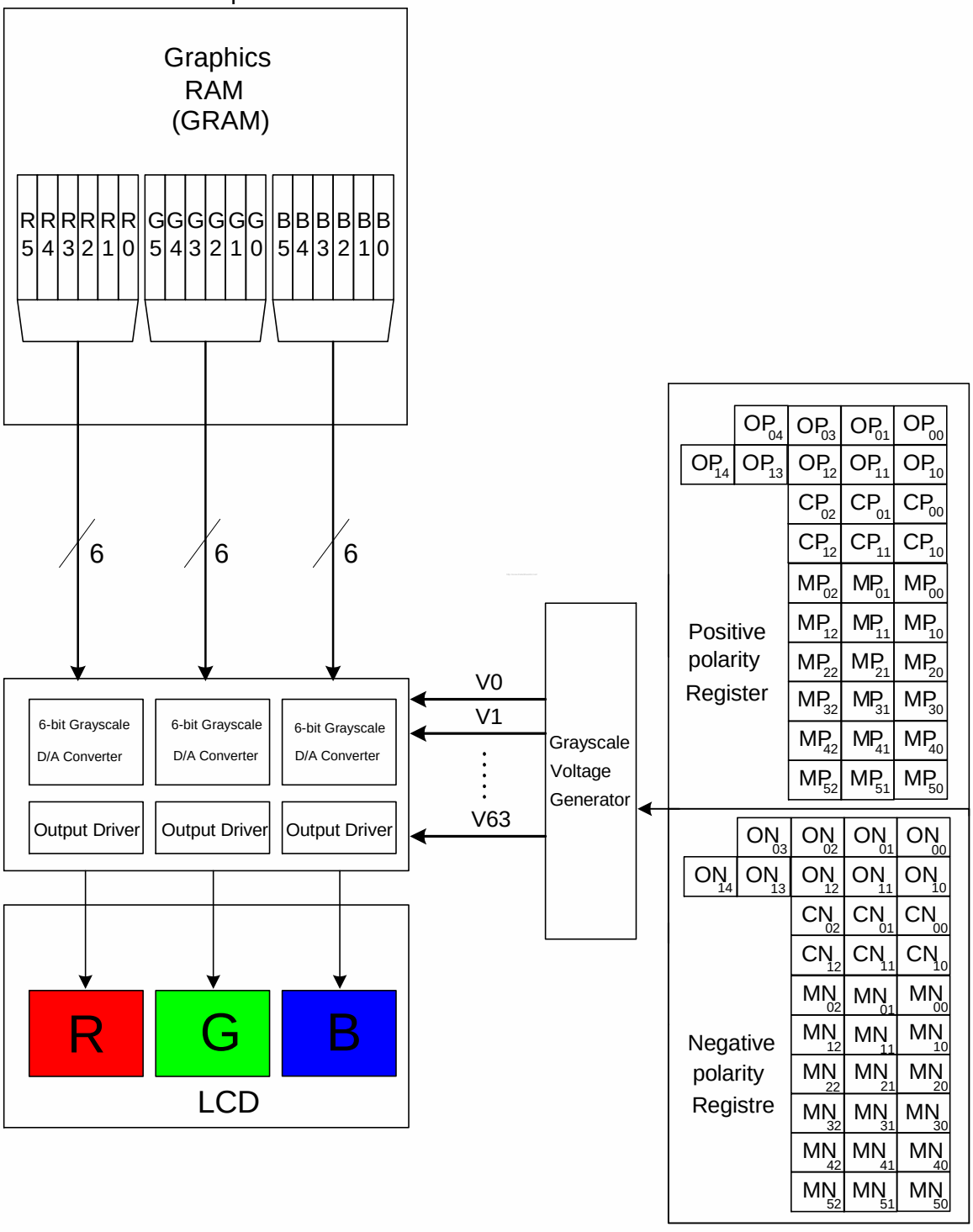


Figure 5.16: Grayscale Control

Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

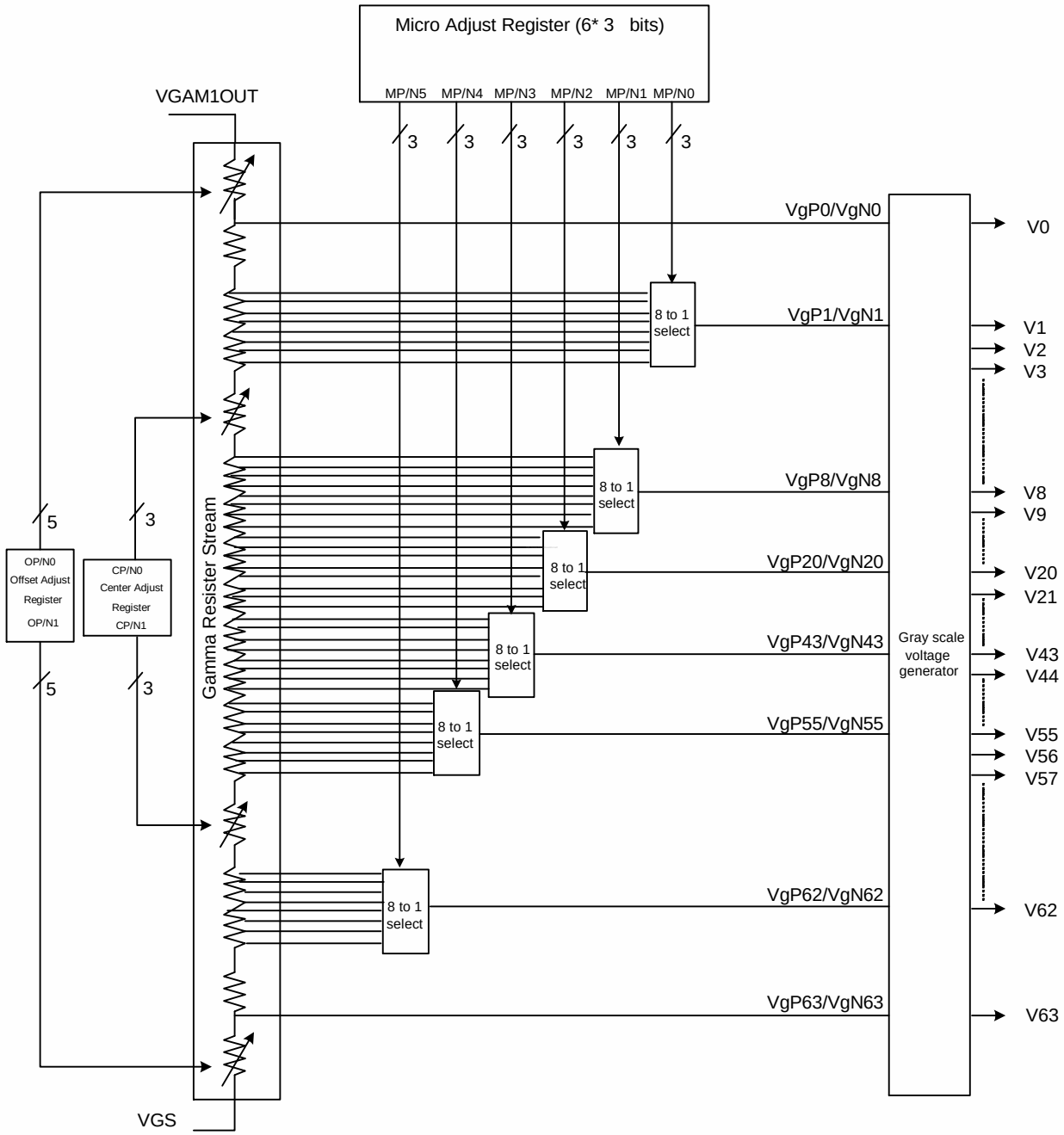


Figure 5.17: Structure of Grayscale Voltage Generator

Gamma-Characteristics Adjustment Register

This HX8347-B has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

A. Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

B. Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

C. Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0) for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1) for offset adjustment

Table 5.7: Gamma-Adjustment Registers

Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (VgP/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

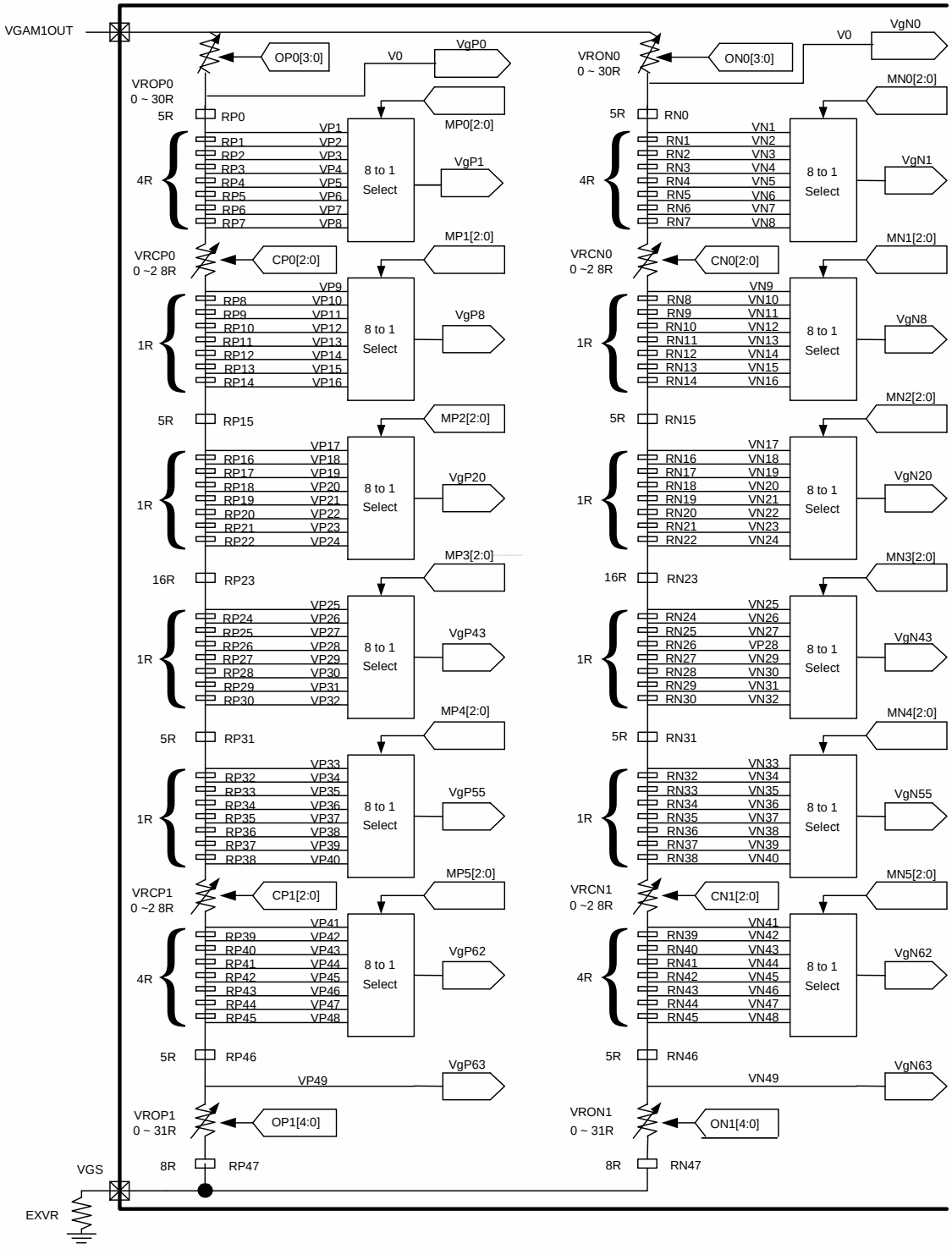


Figure 5.18: Gamma Resister Stream and Gamma Reference Voltage

Variable resister

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5.8: Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5.9: Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5.10: Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5.11: Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	-	VREG1OUT-VD*VROP0 /sumRP	VP0
VgP1	MP0 2-0=000	VREG1OUT -VD((VROP0+5R) /sumRP	VP1
	MP0 2-0=001	VREG1OUT -VD((VROP0+9R) /sumRP	VP2
	MP0 2-0=010	VREG1OUT -VD((VROP0+13R) /sumRP	VP3
	MP0 2-0=011	VREG1OUT -VD((VROP0+17R) /sumRP	VP4
	MP0 2-0=100	VREG1OUT -VD((VROP0+21R) /sumRP	VP5
	MP0 2-0=101	VREG1OUT -VD((VROP0+25R) /sumRP	VP6
	MP0 2-0=110	VREG1OUT -VD((VROP0+29R) /sumRP	VP7
	MP0 2-0=111	VREG1OUT -VD((VROP0+33R) /sumRP	VP8
VgP8	MP1 2-0=000	VREG1OUT -VD((VROP0+33R+VRCP0) /sumRP	VP9
	MP1 2-0=001	VREG1OUT -VD((VROP0+34R+VRCP0) /sumRP	VP10
	MP1 2-0=010	VREG1OUT -VD((VROP0+35R+VRCP0) /sumRP	VP11
	MP1 2-0=011	VREG1OUT -VD((VROP0+36R+VRCP0) /sumRP	VP12
	MP1 2-0=100	VREG1OUT -VD((VROP0+37R+VRCP0) /sumRP	VP13
	MP1 2-0=101	VREG1OUT -VD((VROP0+38R+VRCP0) /sumRP	VP14
	MP1 2-0=110	VREG1OUT -VD((VROP0+39R+VRCP0) /sumRP	VP15
	MP1 2-0=111	VREG1OUT -VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	MP2 2-0=000	VREG1OUT -VD((VROP0+45R+VRCP0) /sumRP	VP17
	MP2 2-0=001	VREG1OUT -VD((VROP0+46R+VRCP0) /sumRP	VP18
	MP2 2-0=010	VREG1OUT -VD((VROP0+47R+VRCP0) /sumRP	VP19
	MP2 2-0=011	VREG1OUT -VD((VROP0+48R+VRCP0) /sumRP	VP20
	MP2 2-0=100	VREG1OUT -VD((VROP0+49R+VRCP0) /sumRP	VP21
	MP2 2-0=101	VREG1OUT -VD((VROP0+50R+VRCP0) /sumRP	VP22
	MP2 2-0=110	VREG1OUT -VD((VROP0+51R+VRCP0) /sumRP	VP23
	MP2 2-0=111	VREG1OUT -VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	MP3 2-0=000	VREG1OUT -VD((VROP0+68R+VRCP0) /sumRP	VP25
	MP3 2-0=001	VREG1OUT -VD((VROP0+69R+VRCP0) /sumRP	VP26
	MP3 2-0=010	VREG1OUT -VD((VROP0+70R+VRCP0) /sumRP	VP27
	MP3 2-0=011	VREG1OUT -VD((VROP0+71R+VRCP0) /sumRP	V2P8
	MP3 2-0=100	VREG1OUT -VD((VROP0+72R+VRCP0) /sumRP	VP29
	MP3 2-0=101	VREG1OUT -VD((VROP0+73R+VRCP0) /sumRP	VP30
	MP3 2-0=110	VREG1OUT -VD((VROP0+74R+VRCP0) /sumRP	VP31
	MP3 2-0=111	VREG1OUT -VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	MP4 2-0=000	VREG1OUT -VD((VROP0+80R+VRCP0) /sumRP	VP33
	MP4 2-0=001	VREG1OUT -VD((VROP0+81R+VRCP0) /sumRP	VP34
	MP4 2-0=010	VREG1OUT -VD((VROP0+82R+VRCP0) /sumRP	VP35
	MP4 2-0=011	VREG1OUT -VD((VROP0+83R+VRCP0) /sumRP	VP36
	MP4 2-0=100	VREG1OUT -VD((VROP0+84R+VRCP0) /sumRP	VP37
	MP4 2-0=101	VREG1OUT -VD((VROP0+85R+VRCP0) /sumRP	VP38
	MP4 2-0=110	VREG1OUT -VD((VROP0+86R+VRCP0) /sumRP	VP39
	MP4 2-0=111	VREG1OUT -VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	MP5 2-0=000	VREG1OUT -VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	MP5 2-0=001	VREG1OUT -VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	MP5 2-0=010	VREG1OUT -VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	MP5 2-0=011	VREG1OUT -VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	MP5 2-0=100	VREG1OUT -VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	MP5 2-0=101	VREG1OUT -VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	MP5 2-0=110	VREG1OUT -VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	MP5 2-0=111	VREG1OUT -VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	-	VREG1OUT -VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD=(VREG1OUT -VGS)
[sumRP× (sumRN/ (sumRP+sumRN))]/ [sumRP×sumRN/ (sumRP+sumRN) +EXVR]

Table 5.12: Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula
V0	VINP0
V1	VINP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINP2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Table 5.13: Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	VREG1OUT -VD*VRON0 /sumRN	VN0
VgN1	MN0 2-0=000	VREG1OUT -VD((VRON0+5R) /sumRN	VN1
	MN0 2-0=001	VREG1OUT -VD((VRON0+9R) /sumRN	VN2
	MN0 2-0=010	VREG1OUT -VD((VRON0+13R) /sumRN	VN3
	MN0 2-0=011	VREG1OUT -VD((VRON0+17R) /sumRN	VN4
	MN0 2-0=100	VREG1OUT -VD((VRON0+21R) /sumRN	VN5
	MN0 2-0=101	VREG1OUT -VD((VRON0+25R) /sumRN	VN6
	MN0 2-0=110	VREG1OUT -VD((VRON0+29R) /sumRN	VN7
	MN0 2-0=111	VREG1OUT -VD((VRON0+33R) /sumRN	VN8
VgN8	MN1 2-0=000	VREG1OUT -VD((VRON0+33R+VRCN0) /sumRN	VN9
	MN1 2-0=001	VREG1OUT -VD((VRON0+34R+VRCN0) /sumRN	VN10
	MN1 2-0=010	VREG1OUT -VD((VRON0+35R+VRCN0) /sumRN	VN11
	MN1 2-0=011	VREG1OUT -VD((VRON0+36R+VRCN0) /sumRN	VN12
	MN1 2-0=100	VREG1OUT -VD((VRON0+37R+VRCN0) /sumRN	VN13
	MN1 2-0=101	VREG1OUT -VD((VRON0+38R+VRCN0) /sumRN	VN14
	MN1 2-0=110	VREG1OUT -VD((VRON0+39R+VRCN0) /sumRN	VN15
	MN1 2-0=111	VREG1OUT -VD((VRON0+40R+VRCN0) /sumRN	VN16
VgN20	MN2 2-0=000	VREG1OUT -VD((VRON0+45R+VRCN0) /sumRN	VN17
	MN2 2-0=001	VREG1OUT -VD((VRON0+46R+VRCN0) /sumRN	VN18
	MN2 2-0=010	VREG1OUT -VD((VRON0+47R+VRCN0) /sumRN	VN19
	MN2 2-0=011	VREG1OUT -VD((VRON0+48R+VRCN0) /sumRN	VN20
	MN2 2-0=100	VREG1OUT -VD((VRON0+49R+VRCN0) /sumRN	VN21
	MN2 2-0=101	VREG1OUT -VD((VRON0+50R+VRCN0) /sumRN	VN22
	MN2 2-0=110	VREG1OUT -VD((VRON0+51R+VRCN0) /sumRN	VN23
	MN2 2-0=111	VREG1OUT -VD((VRON0+52R+VRCN0) /sumRN	VN24
VgN43	MN3 2-0=000	VREG1OUT -VD((VRON0+68R+VRCN0) /sumRN	VN25
	MN3 2-0=001	VREG1OUT -VD((VRON0+69R+VRCN0) /sumRN	VN26
	MN3 2-0=010	VREG1OUT -VD((VRON0+70R+VRCN0) /sumRN	VN27
	MN3 2-0=011	VREG1OUT -VD((VRON0+71R+VRCN0) /sumRN	VNP8
	MN3 2-0=100	VREG1OUT -VD((VRON0+72R+VRCN0) /sumRN	VN29
	MN3 2-0=101	VREG1OUT -VD((VRON0+73R+VRCN0) /sumRN	VN30
	MN3 2-0=110	VREG1OUT -VD((VRON0+74R+VRCN0) /sumRN	VN31
	MN3 2-0=111	VREG1OUT -VD((VRON0+75R+VRCN0) /sumRN	VN32
VgN55	MN4 2-0=000	VREG1OUT -VD((VRON0+80R+VRCN0) /sumRN	VN33
	MN4 2-0=001	VREG1OUT -VD((VRON0+81R+VRCN0) /sumRN	VN34
	MN4 2-0=010	VREG1OUT -VD((VRON0+82R+VRCN0) /sumRN	VN35
	MN4 2-0=011	VREG1OUT -VD((VRON0+83R+VRCN0) /sumRN	VN36
	MN4 2-0=100	VREG1OUT -VD((VRON0+84R+VRCN0) /sumRN	VN37
	MN4 2-0=101	VREG1OUT -VD((VRON0+85R+VRCN0) /sumRN	VN38
	MN4 2-0=110	VREG1OUT -VD((VRON0+86R+VRCN0) /sumRN	VN39
	MN4 2-0=111	VREG1OUT -VD((VRON0+87R+VRCN0) /sumRN	VN40
VgN62	MN5 2-0=000	VREG1OUT -VD((VRON0+87R+VRCN0+VRCN1) /sumRN	VN41
	MN5 2-0=001	VREG1OUT -VD((VRON0+91R+VRCN0+VRCN1) /sumRN	VN42
	MN5 2-0=010	VREG1OUT -VD((VRON0+95R+VRCN0+VRCN1) /sumRN	VN43
	MN5 2-0=011	VREG1OUT -VD((VRON0+99R+VRCN0+VRCN1) /sumRN	VN44
	MN5 2-0=100	VREG1OUT -VD((VRON0+103R+VRCN0+VRCN1)/sumRN	VN45
	MN5 2-0=101	VREG1OUT -VD((VRON0+107R+VRCN0+VRCN1)/sumRN	VN46
	MN5 2-0=110	VREG1OUT -VD((VRON0+111R+VRCN0+VRCN1)/sumRN	VN47
	MN5 2-0=111	VREG1OUT -VD((VRON0+115R+VRCN0+VRCN1)/sumRN	VN48
VgN63	-	VREG1OUT -VD((VRON0+120R+VRCN0+VRCN1)/sumRN	VN49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1;
SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1
VD = (VREG1OUT -VGS)
[sumRP(sumRN/(sumRP+sumRN))]/[sumRP(sumRN/(sumRP+sumRN)+EXVR)

Table 5.14: Voltage Calculation Formula (Negative Polarity)

Grayscale Voltage	Formula
V0	VINN0
V1	VINN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINN2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINN5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINN6
V63	VINN7

Table 5.15: Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Relationship between GRAM Data and Output Level (“Normally White Panel”, GRAM data=0)

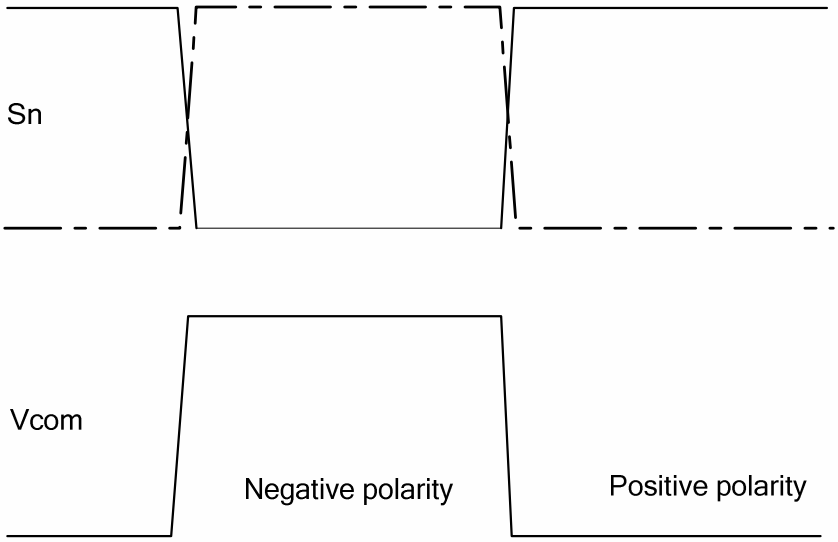


Figure 5.19: Relationship between Source Output and Vcom

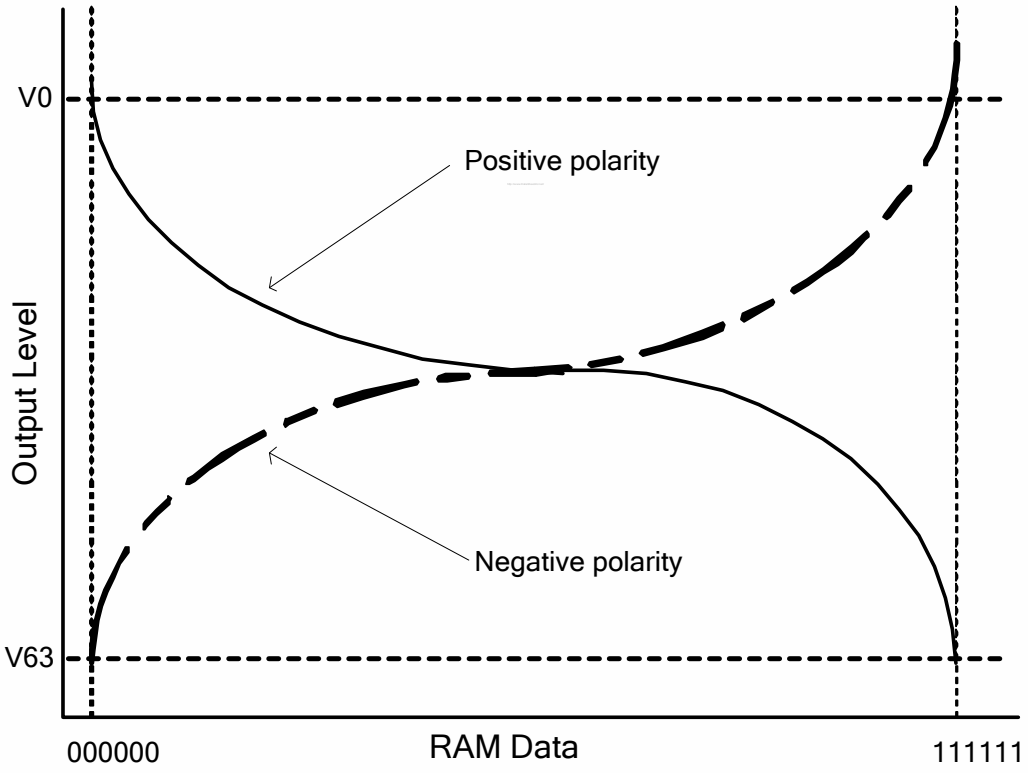


Figure 5.20: Relationship between GRAM Data and Output Level (Normal White Panel REV =“1”)

5.11 Power On/Off Sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display On/Off Set flow

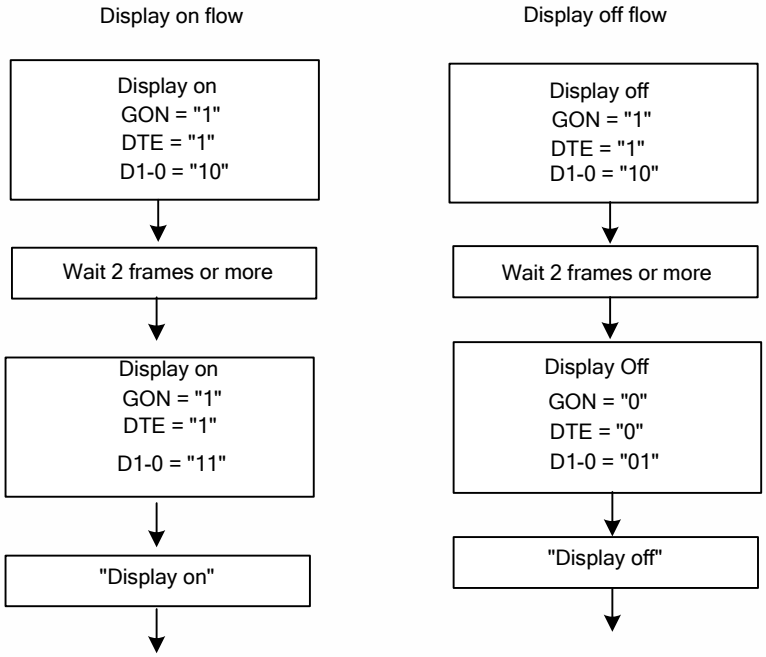


Figure 5.21: Display On/Off Set flow

Sleep Mode Set up Flow

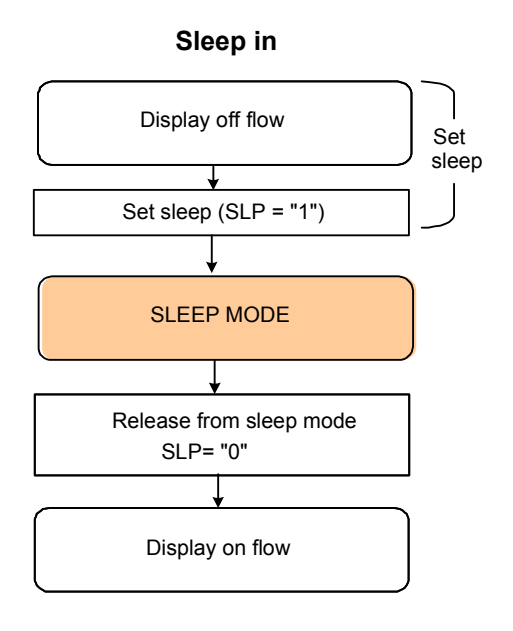


Figure 5.22: Sleep Mode Setting flow

Standby Mode Set up Flow

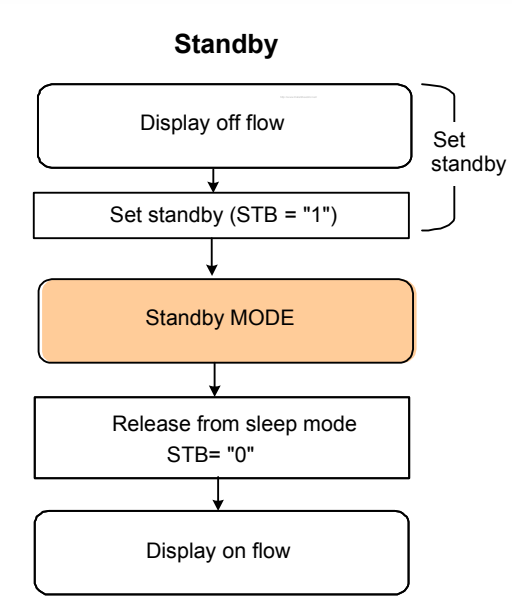


Figure 5.23: Standby Mode Setting flow

Deep Standby Mode Set up Flow

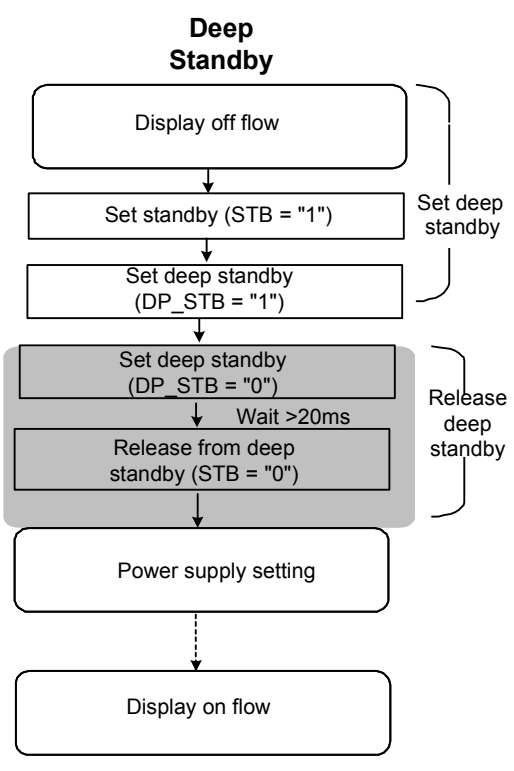


Figure 5.24: Deep Standby Mode Setting flow

Power On/Off Setting up Flow

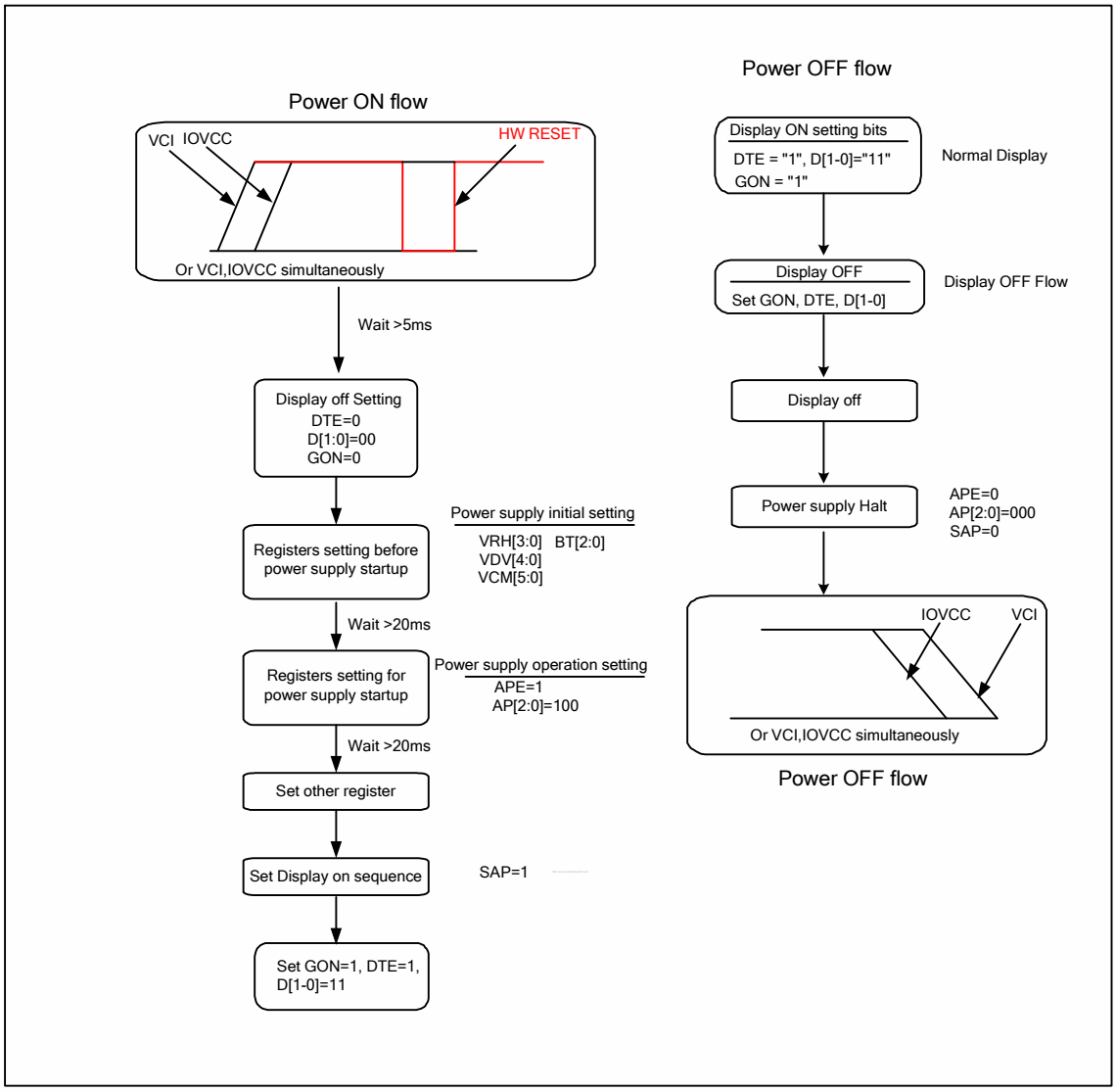


Figure 5.25: Power Supply Setting Flow

5.12 Input / Output Pin State

5.12.1 Output Pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low

Table 5.16: Characteristics of Output Pins

5.12.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
NRESET	Input valid	Input valid	Input valid	Input valid
NCS	Input invalid	Input valid	Input valid	Input invalid
NWR_SCL	Input invalid	Input valid	Input valid	Input invalid
NRD	Input invalid	Input valid	Input valid	Input invalid
DNC	Input invalid	Input valid	Input valid	Input invalid
SDI	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
DB[17:0]	Input invalid	Input valid	Input valid	Input invalid
OSC, IM3~0	Input invalid	Input valid	Input valid	Input invalid
TEST2-1	Input invalid	Input valid	Input valid	Input invalid

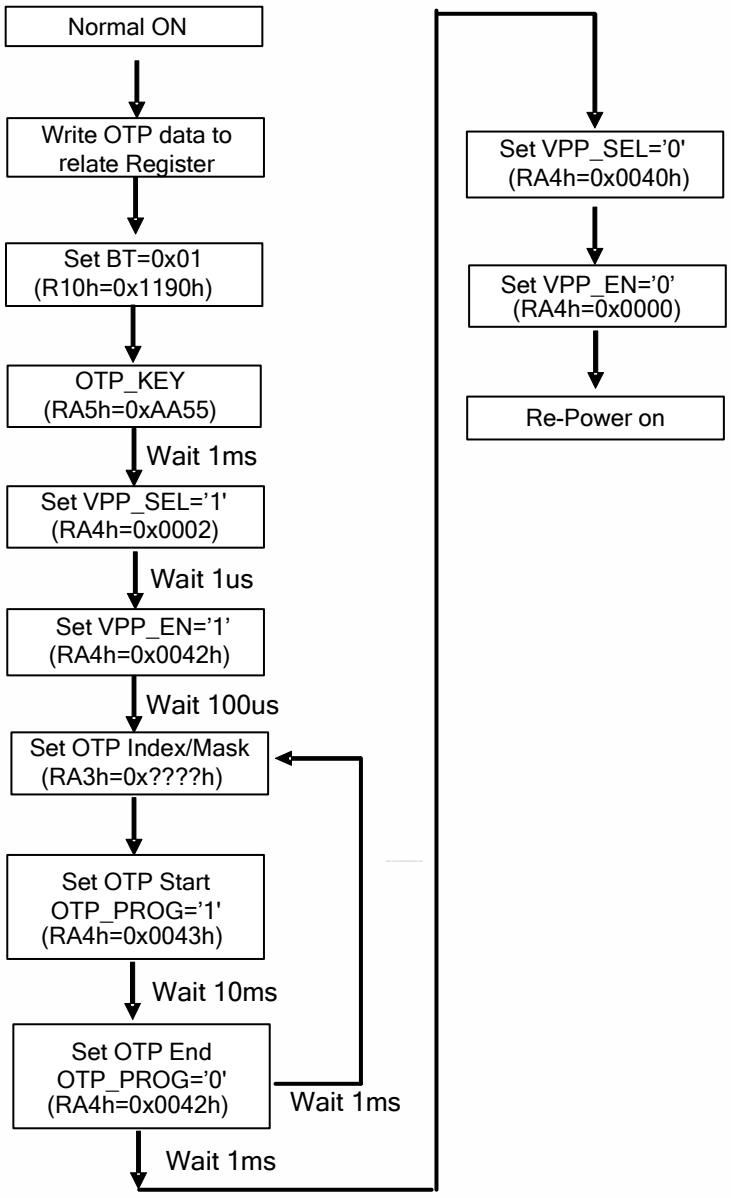
Table 5.17: Characteristics of Input Pins

5.13 OTP Programing

5.13.1 OTP table

OTP_INDEX (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Ref. Register
00	ID17_1	ID16_1	ID15_1	ID14_1	ID13_1	ID12_1	ID11_1	ID10_1	DAh
01	ID27_1	ID26_1	ID25_1	ID24_1	ID23_1	ID22_1	ID21_1	ID20_1	DBh
02	ID37_1	ID36_1	ID35_1	ID34_1	ID33_1	ID32_1	ID31_1	ID30_1	DCh
03	ID17_2	ID16_2	ID15_2	ID14_2	ID13_2	ID12_2	ID11_2	ID10_2	DAh
04	ID27_2	ID26_2	ID25_2	ID24_2	ID23_2	ID22_2	ID21_2	ID20_2	DBh
05	ID37_2	ID36_2	ID35_2	ID34_2	ID33_2	ID32_2	ID31_2	ID30_2	DCh
06	ID17_3	ID16_3	ID15_3	ID14_3	ID13_3	ID12_3	ID11_3	ID10_3	DAh
07	ID27_3	ID26_3	ID25_3	ID24_3	ID23_3	ID22_3	ID21_3	ID20_3	DBh
08	ID37_3	ID36_3	ID35_3	ID34_3	ID33_3	ID32_3	ID31_3	ID30_3	DCh
09	ID17_4	ID16_4	ID15_4	ID14_4	ID13_4	ID12_4	ID11_4	ID10_4	DAh
0A	ID27_4	ID26_4	ID25_4	ID24_4	ID23_4	ID22_4	ID21_4	ID20_4	DBh
0B	ID37_4	ID36_4	ID35_4	ID34_4	ID33_4	ID32_4	ID31_4	ID30_4	DCh
0C	ID17_5	ID16_5	ID15_5	ID14_5	ID13_5	ID12_5	ID11_5	ID10_5	DAh
0D	ID27_5	ID26_5	ID25_5	ID24_5	ID23_5	ID22_5	ID21_5	ID20_5	DBh
0E	ID37_5	ID36_5	ID35_5	ID34_5	ID33_5	ID32_5	ID31_5	ID30_5	DCh
0F	ID17_6	ID16_6	ID15_6	ID14_6	ID13_6	ID12_6	ID11_6	ID10_6	DAh
10	ID27_6	ID26_6	ID25_6	ID24_6	ID23_6	ID22_6	ID21_6	ID20_6	DBh
11	ID37_6	ID36_6	ID35_6	ID34_6	ID33_6	ID32_6	ID31_6	ID30_6	DCh
12	ID17_7	ID16_7	ID15_7	ID14_7	ID13_7	ID12_7	ID11_7	ID10_7	DAh
13	ID27_7	ID26_7	ID25_7	ID24_7	ID23_7	ID22_7	ID21_7	ID20_7	DBh
14	ID37_7	ID36_7	ID35_7	ID34_7	ID33_7	ID32_7	ID31_7	ID30_7	DCh
15	ID17_8	ID16_8	ID15_8	ID14_8	ID13_8	ID12_8	ID11_8	ID10_8	DAh
16	ID27_8	ID26_8	ID25_8	ID24_8	ID23_8	ID22_8	ID21_8	ID20_8	DBh
17	ID37_8	ID36_8	ID35_8	ID34_8	ID33_8	ID32_8	ID31_8	ID30_8	DCh
18	Valid_ID1_8	Valid_ID1_7	Valid_ID1_6	Valid_ID1_5	Valid_ID1_4	Valid_ID1_3	Valid_ID1_2	Valid_ID1_1	---
19	Valid_ID2_8	Valid_ID2_7	Valid_ID2_6	Valid_ID2_5	Valid_ID2_4	Valid_ID2_3	Valid_ID2_2	Valid_ID2_1	--
1A	Valid_ID3_8	Valid_ID3_7	Valid_ID3_6	Valid_ID3_5	Valid_ID3_4	Valid_ID3_3	Valid_ID3_2	Valid_ID3_1	--
1B	Valid_VCM_1		VCM5_1	VCM4_1	VCM3_1	VCM2_1	VCM1_1	VCM0_1	29h
1C	Valid_VDV_1			VDV4_1	VDV3_1	VDV2_1	VDV1_1	VDV0_1	13h
1D	Valid_VCM_2		VCM5_2	VCM4_2	VCM3_2	VCM2_2	VCM1_2	VCM0_2	29h
1E	Valid_VDV_2			VDV4_2	VDV3_2	VDV2_2	VDV1_2	VDV0_2	13h
1F	Valid_VCM_3		VCM5_3	VCM4_3	VCM3_3	VCM2_3	VCM1_3	VCM0_3	29h
20	Valid_VDV_3			VDV4_3	VDV3_3	VDV2_3	VDV1_3	VDV0_3	13h
21	Valid_VCM_4		VCM5_4	VCM4_4	VCM3_4	VCM2_4	VCM1_4	VCM0_4	29h
22	Valid_VDV_4			VDV4_4	VDV3_4	VDV2_4	VDV1_4	VDV0_4	13h
23	Valid_VCM_5		VCM5_5	VCM4_5	VCM3_5	VCM2_5	VCM1_5	VCM0_5	29h
24	Valid_VDV_5			VDV4_5	VDV3_5	VDV2_5	VDV1_5	VDV0_5	13h
25	Valid_VCM_6		VCM5_6	VCM4_6	VCM3_6	VCM2_6	VCM1_6	VCM0_6	29h
26	Valid_VDV_6			VDV4_6	VDV3_6	VDV2_6	VDV1_6	VDV0_6	13h
27	Valid_VCM_7		VCM5_7	VCM4_7	VCM3_7	VCM2_7	VCM1_7	VCM0_7	29h
28	Valid_VDV_7			VDV4_7	VDV3_7	VDV2_7	VDV1_7	VDV0_7	13h
29	Valid_VCM_8		VCM5_8	VCM4_8	VCM3_8	VCM2_8	VCM1_8	VCM0_8	29h
2A	Valid_VDV_8			VDV4_8	VDV3_8	VDV2_8	VDV1_8	VDV0_8	13h
2B	Valid_panel		DDVDH_TRI	SM_Panel	SS_Panel	GS_Panel	REV_Panel	BGR_Panel	98h

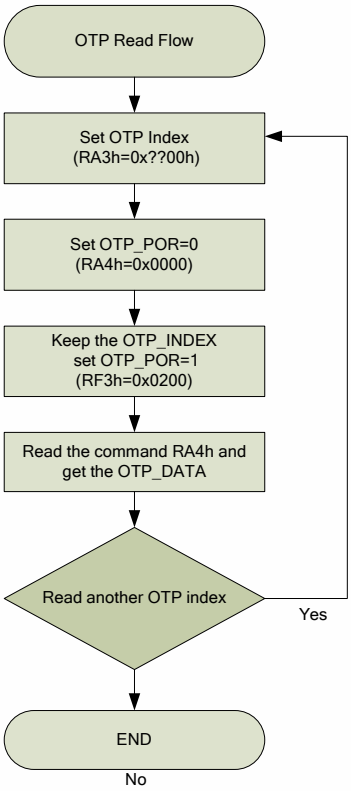
5.13.2 OTP programming flow



5.13.3 OTP Sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and IC normal operation</td></tr>
<tr><td>2</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td>ID1</td><td>RDAh</td><td>Set ID1 LCD version</td></tr>
<tr><td>ID2</td><td>RDBh</td><td>Set ID2 LCD version</td></tr>
<tr><td>ID3</td><td>RDCh</td><td>Set ID3 LCD version</td></tr>
<tr><td>Power control 4</td><td>R13h</td><td>Set VDV[4:0] VCOM amplitude</td></tr>
<tr><td>Power control 7</td><td>R29h</td><td>Set VCM[5:0] VCOMH voltage</td></tr>
</table></td></tr>
<tr><td>3</td><td>Set BT[2:0]=0x01 (R10h=0x1190)</td></tr>
<tr><td>4</td><td>Set OTP_KEY (RA5h=0xAA55)</td></tr>
<tr><td>5</td><td>Set OTP_SEL (RA4h=0x0002)</td></tr>
<tr><td>6</td><td>Set OTP_EN (RA4h=0x0042)</td></tr>
<tr><td>7</td><td>Set OTP Index
<table>
<tr><th>Index</th><th>Description</th></tr>
<tr><td>00h,01h,02h</td><td>ID1~ID3 index</td></tr>
<tr><td>1Bh,1Ch</td><td>VDV,VCM Vcom valid</td></tr>
<tr><td>2Bh</td><td>Panel characteristic, Valid_Panel</td></tr>
</table></td></tr>
<tr><td>8</td><td>Set OTP_Mask=0x00h, programming the entire bit of one parameter.</td></tr>
<tr><td>9</td><td>Set OTP Start OTP_PROG=’1’ (RA4h=0x0043h)</td></tr>
<tr><td>10</td><td>Wait 10ms</td></tr>
<tr><td>11</td><td>Set OTP Start OTP_PROG=’0’ (RA4h=0x0042h)
Complete programming one parameter to OTP.
If continue to programming other parameter, return to step (4). Otherwise power off module, and re-power on again.</td></tr>
</table>

5.13.4 OTP Read flow



5.14 Content Adaptive Brightness Control (CABC) function

The HX8347-B has support Content Adaptive Brightness Control (CABC) Function and will output one PWM signal to external LED Driver IC. The PWM signal is automatics adjust output duty by display image for saving LED backlight power consumption.

Example:

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

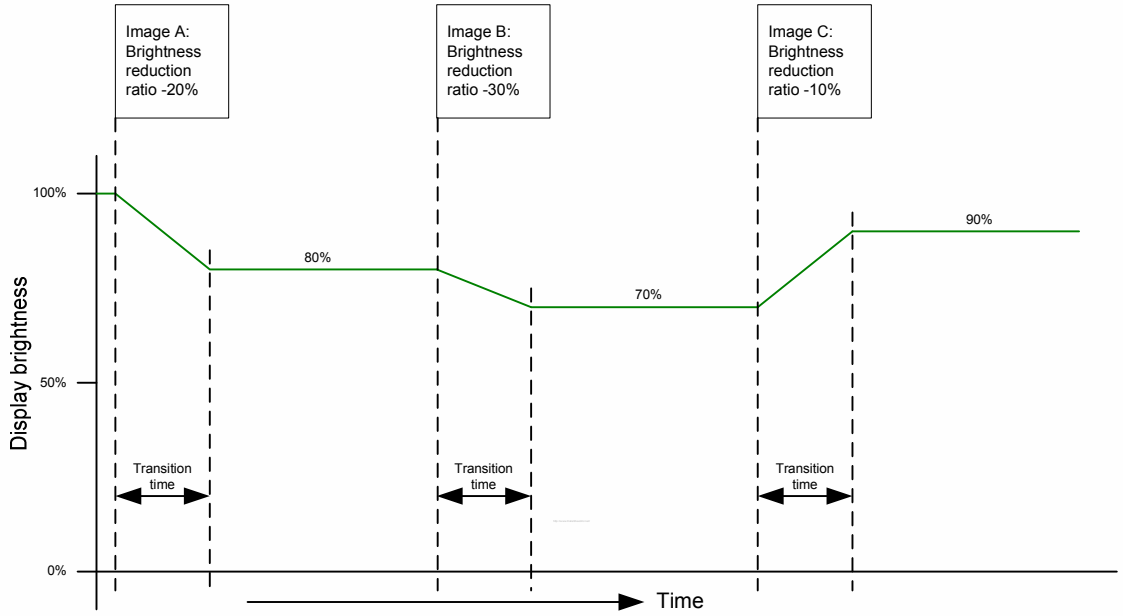


Figure 5.26: Example of CABC function

The general block diagram of the CABC and the brightness control is illustrated below:

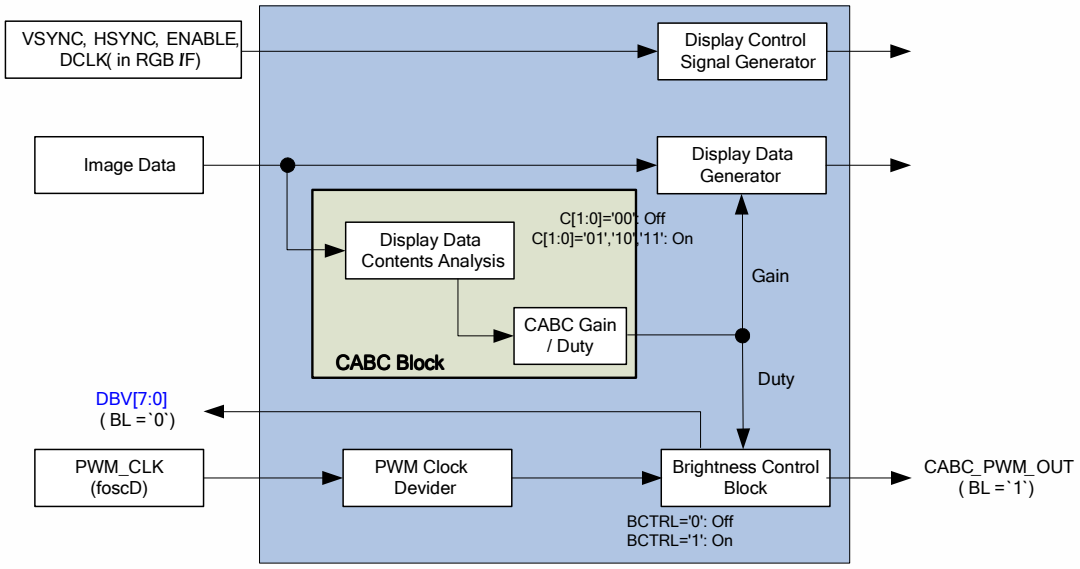
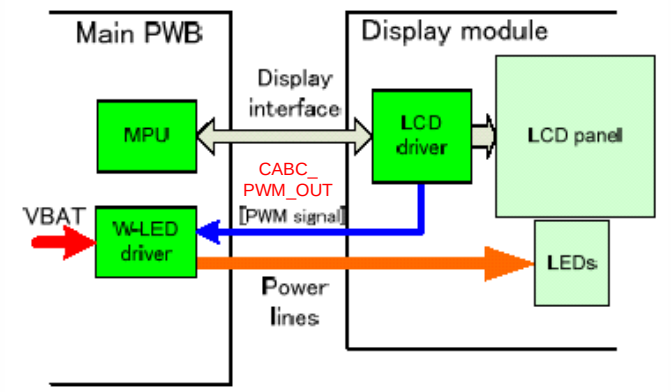


Figure 5.27: CABC block diagram

Module architectures

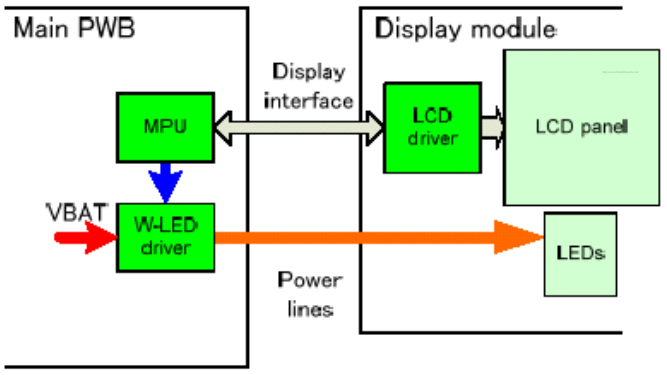
The HX8347-B can support two module architectures for CABC operation. The **BL** bit setting of R3Dh can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

• Architecture I



1. **BL** =`1` of RB3h
2. LED backlight brightness for the display is controlled by external output "CABC_PWM_OUT".

• Architecture II



1. **BL** =`0` of RB3h
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R3Ch.
3. Read commands RB2h should be synchronized with V-sync.

Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of RB1h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as DBV[7:0]/255 x CABC duty (generated after one-frame display data content analysis).

For example: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](RB2h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = 228 / 255 x 74% ≡ 65.90%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.94ms, and the low-level of CABC_PWM_OUT = 1.01ms.

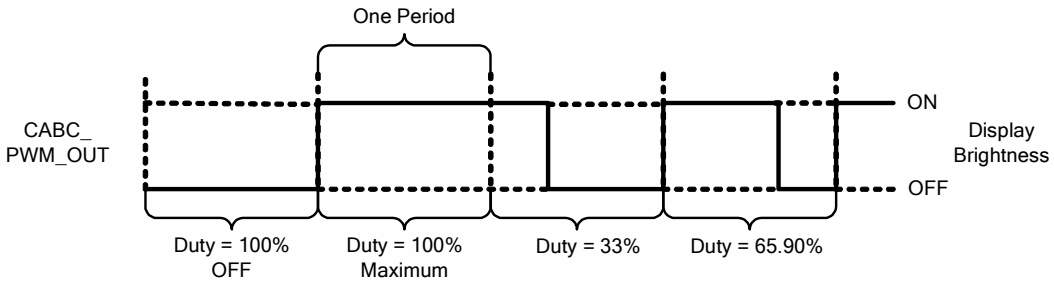


Figure 5.28: CABC_PWM_OUT output duty

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](RB2h) will be read a value as 169_{DEC} (169/255≡ 66.27%).

Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of RBEh) works to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function works as normal, even if the brightness can not be changed.

This function does not affect the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can work as normal.

When display brightness is turned off (**BCTRL='0'** of RB3h), CABC minimum brightness setting is ignored. Read CABC minimum brightness **CMB[7:0]** (RBFh) always reads the setting value.

Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

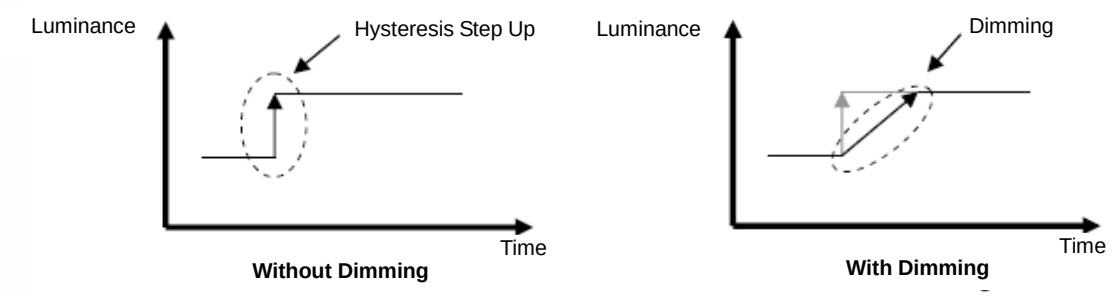
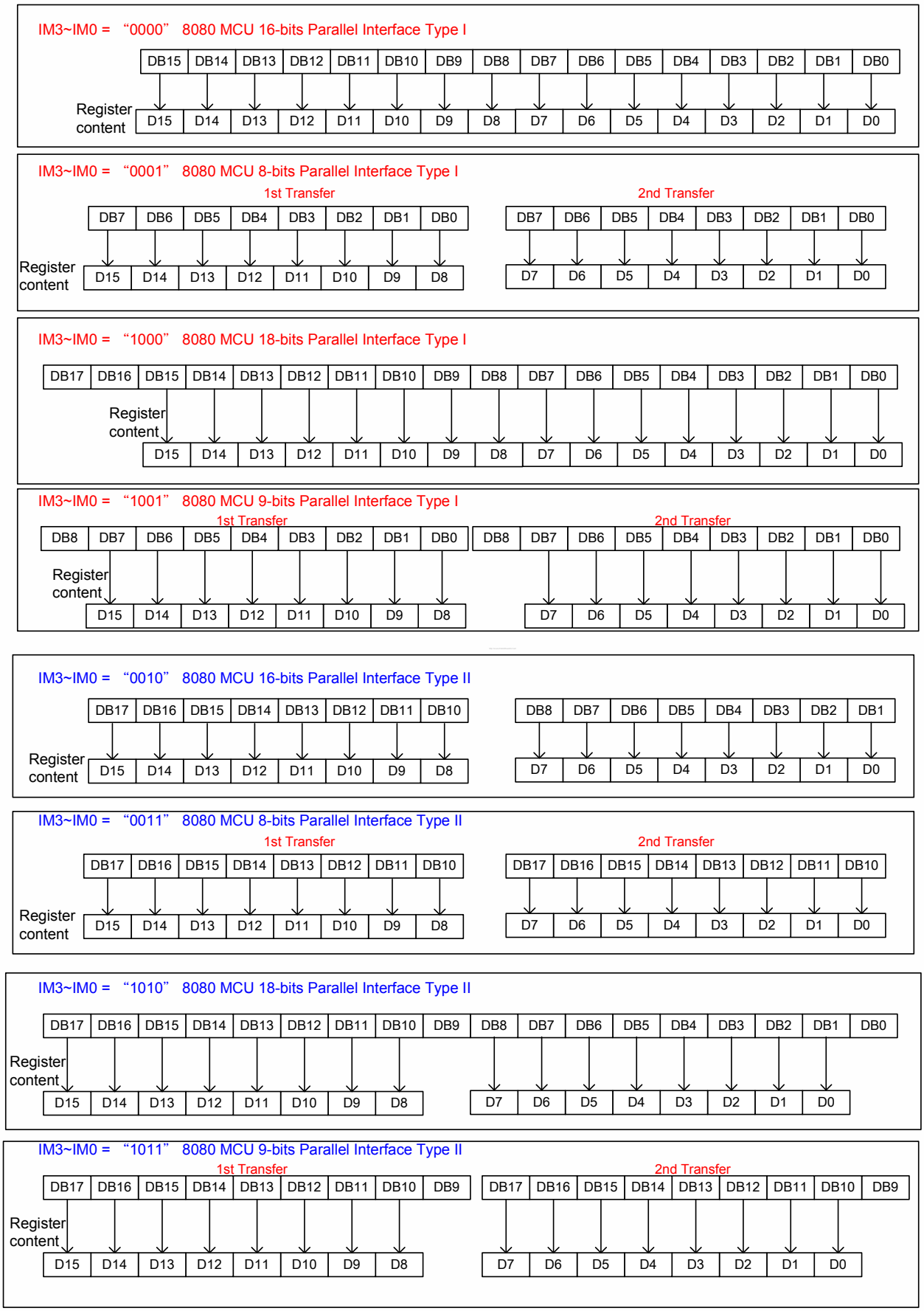


Figure 5.29: Dimming function

6. Command



6.1 Command Set

	Register	R/W	RS	Upper Code								Lower Code							
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
IR	Index	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Driver ID code	R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
R01h	Driver Output Control	RW	1	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
R02h	LCD driving Control	RW	1	0	0	0	0	0	0	B/C (0)	0	0	0	0	0	0	0	0	0
R03h	Entry Mode	RW	1	TRI (0)	DFM (0)	0	BGR (0)	0	0	0	0	0	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
R05h	16 bits data mapping	RW	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF[1:0] (00)	
R07h	Display Control 1	RW	1	0	0	PTDE[1:0] (00)		0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	CL (0)	0	D1 (0)	D0 (0)
R08h	Display Control 2	RW	1	0	0	0	0	FP[3:0] (1000)				0	0	0	0	BP[3:0] (1000)			
R09h	Display Control 3	RW	1	0	0	0	0	0	0	PTS[1:0] (00)		0	0	PTG[1:0] (00)		ISC[3:0] (0000)			
R0Ah	Display Control 4	RW	1	0	0	0	0	0	0	0	0	TE_Mode(0)	0	0	0	TEOE (0)	TEI[2:0] (000)		
R0Ch	RGB Interface Control 1	RW	1	0	ECN[2:0] (000)			0	0	0	RM (0)	0	0	DM[1:0] (00)		0	0	RIM[1:0] (00)	
R0Dh	TE Output Position	RW	1	0	0	0	0	0	0	0	TEP[8:0] (0 0000 0000)								
R0Fh	RGB Interface Control 2	RW	1	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
R10h	Power Control 1	RW	1	0	0	0	SAP0 (0)	0	BT2 (1)	BT1 (1)	BT0 (0)	APE (0)	AP2 (0)	AP1 (0)	AP0 (0)	0	0	SLP (0)	STB (0)
R11h	Power Control 2	RW	1	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (1)	0	DC02 (1)	DC01 (1)	DC00 (1)	0	0	0	0
R12h	Power Control 3	RW	1	0	0	0	0	0	0	DDVDH_TRI(0)	XDK (0)	VCIRE (0)	0	0		VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
R13h	Power Control 4	RW	1	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0

	Register	R/W	RS	Upper Code								Lower Code							
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R20h	RAM Address Set	RW	1	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
R21h	RAM Address Set	RW	1	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
R22h	RAM data Write/Read	RW	1	RAM				WD17-0 /RAM						(RD17-0)					
R29h	Power Control 7	RW	1	0	0	0	0	0	0	0	0	0	0	VCM[5:0] (0 0000)					
R2Bh	Frame rate Control	RW	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3:0] (1101)			
R30h	r Control (1)	RW	1	0	0	0	0	0	MP12 (0)	MP11 (0)	MP10 (0)	0	0	0	0	0	MP02 (0)	MP01 (0)	MP00 (0)
R31h	r Control (2)	RW	1	0	0	0	0	0	MP32 (0)	MP31 (0)	MP30 (0)	0	0	0	0	0	MP22 (0)	MP21 (0)	MP20 (0)
R32h	r Control (3)	RW	1	0	0	0	0	0	MP52 (0)	MP 51 (0)	MP 50 (0)	0	0	0	0	0	MP42 (0)	MP41 (0)	MP40 (0)
R35h	r Control (4)	RW	1	0	0	0	0	0	CP12 (0)	CP11 (0)	CP10 (0)	0	0	0	0	0	CP 02 (0)	CP 01 (0)	CP00 (0)
R36h	r Control (5)	RW	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)	0	0	0	0	OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)
R37h	r Control (6)	RW	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)
R38h	r Control (7)	RW	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)
R39h	r Control (8)	RW	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)
R3Ch	r Control (9)	RW	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)
R3Dh	r Control (10)	RW	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)	0	0	0	0	ON03 (0)	ON02 (0)	ON01 (0)	ON00 (0)
R50h	Horizontal Start	RW	1	0	0	0	0	0	0	0		HSA[7:0] (0x00)							
R51h	Horizontal END	RW	1	0	0	0	0	0	0	0		HSE[7:0] (0xEF)							
R52h	Vertical Start	RW	1	0	0	0	0	0	0	0	VSA[7:0] (0x00)								
R53h	Vertical END	RW	1	0	0	0	0	0	0	0	VSE[7:0] (0x13F)								
R60h	Gate Scan Start Position	RW	1	GS (0)	0	NL[5:0] (1 0111)				0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
R61h	Base Image Control	RW	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL(0)	VLE(0)	REV(0)
R66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RW

	Register	R/W	RS	Upper Code								Lower Code							
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R6Ah	Vertical Scroll Control	RW	1	0	0	0	0	0	0	0	VL8(0)	VL7(0)	VL6(0)	VL5(0)	VL4(0)	VL3(0)	VL2(0)	VL1(0)	VL0(0)
R80h	Partial Image 1 Display Position	RW	1	0	0	0	0	0	0	0	PTDP 08	PTDP0 7	PTDP0 6	PTDP0 5	PTDP0 4	PTDP0 3	PTDP0 2	PTDP0 1	PTDP0 0
R81h	Partial Image 1 Area (Start Line)	RW	1	0	0	0	0	0	0	0	PTSA0 8	PTSA0 7	PTSA0 6	PTSA0 5	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
R82h	Partial Image 1 Area (End Line)	RW	1	0	0	0	0	0	0	0	PTEA0 8	PTEA0 7	PTEA0 6	PTEA0 5	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
R83h	Partial Image 2 Display Position	RW	1	0	0	0	0	0	0	0	PTDP 18	PTDP1 7	PTDP1 6	PTDP1 5	PTDP1 4	PTDP1 3	PTDP1 2	PTDP1 1	PTDP1 0
R84h	Partial Image 2 Area (Start Line)	RW	1	0	0	0	0	0	0	0	PTSA1 8	PTSA1 7	PTSA1 6	PTSA1 5	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
R85h	Partial Image 2 Area (End Line)	RW	1	0	0	0	0	0	0	0	PTEA1 8	PTEA1 7	PTEA1 6	PTEA1 5	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
R90h	Panel Interface Control 1	RW	1	0	0	0	0	0	0	DIVI1(0)	DIVI00 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
R92h	Panel Interface Control 2	RW	1	0	0	0	0	0	NOWI 2(1)	NOWI1(1)	NOWI 0(0)	0	0	0	0	0	0	0	0
R97h	Panel Interface Control 3	RW		0	0	0	0	NOW E3	NOW E2	NOWE1	NOWE 0	0	0	0	0	0	0	0	0
R98h	Panel Interface Control 4	RW		0	0	0	0	0	0	0	0	0	0	0	SM_Pa nel	SS_Pan el	GS_Pa nel	REV_P anel	BGR_P anel
RA2h	OTP VCM Status and Enable	RW	1	0	0	VCM_ D5	VCM_ D4	VCM_ D3	VCM_ D2	VCM_D1	VCM_ D0	0	0	0	0	0	0	0	VCM_E N
RA3h	OTP Data and Index	RW	1	OTP_In dex7	OTP_In dex6	OTP_In dex5	OTP_In dex4	OTP_I ndex3	OTP_I ndex2	OTP_Inde x1	OTP_I ndex0	OTP_M ask7	OTP_M ask6	OTP_M ask5	OTP_M ask4	OTP_M ask3	OTP_M ask2	OTP_M ask1	OTP_M ask0
RA4h	OTP function	RW	1	0	0	0	0	0	0	0	0	Load_D isable	VPP_E N	OTP_P OR	OTP_P WE	OTP_P TM1	OTP_P TM0	VPP_S EL	OTP_P ROG
RA5h	OTP Programming ID Key	RW	1	KEY15	KEY14	KEY13	KEY12	KEY1 1	KEY1 0	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
RB1h	Write Display Brightness	W	1									DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
RB2h	Read Display Brightness	R	1									DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
RB3h	Write CTRL Display value	W	1									X	X	BCTRL	X	DD	BL	X	X
RB4h	Read CTRL Display value	R	1									X	X	BCTRL	X	DD	BL	X	X

	Register	R/W	RS	Upper Code								Lower Code							
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
RB5h	Write Content Adaptive Brightness Control value	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]	
RB6h	Read Content Adaptive Brightness Control value	R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]	
RBEh	Write CABC Minimum Brightness	W	1	0	0	0	0	0	0	0	0	CMB[7:0]							
RBFh	Read CABA Minimum Brightness	R	1	0	0	0	0	0	0	0	0	CMB[7:0]							
RC7h	CABC Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEDON POL	PWMP OL
RC8h	CABC Control 2	W	1	0	0	0	0	0	0	0	0	PWM_Period[7:0]							
RDAh	ID1	RW	1	0	0	0	0	0	0	0	0	ID1[7:0]							
RDBh	ID2	RW	1	0	0	0	0	0	0	0	0	ID2[7:0]							
RDCh	ID3	RW	1	0	0	0	0	0	0	0	0	ID3[7:0]							
RE6h	Deep stand by mode control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
RF3h	OTP Data Read	R	1	0	0	0	0	0	0	0	0	OTP_DATA_READ[7:0]							
RF4h	ID OTP CNT	R	1	0	0	ID1_CNT[3:0]				0	ID2_CNT[3:0]				0	ID3_CNT[3:0]			
Rf5h	VCOM OTP CNT	R	1	0	0	0	0	0	0	0	VCM_CNT[3:0]				0	VDV_CNT[3:0]			

6.2 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6.1: Index Register

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID6-0) in the range from 000000b to 1111111b in binary form.

6.3 Driver ID code(R00h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The device ID “9325h” is read out when read this register.

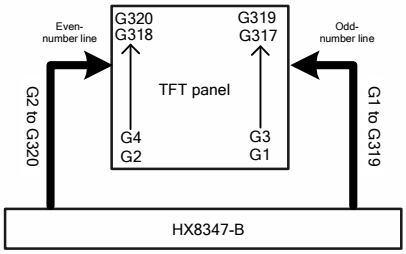
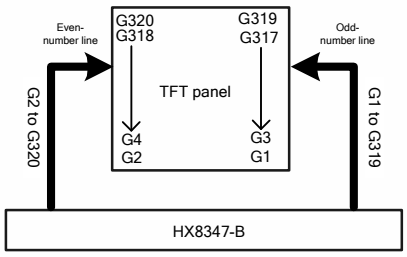
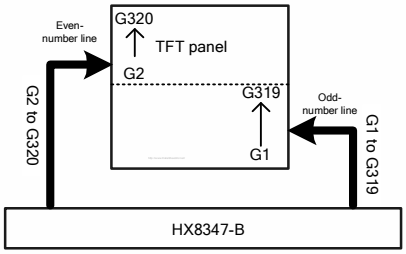
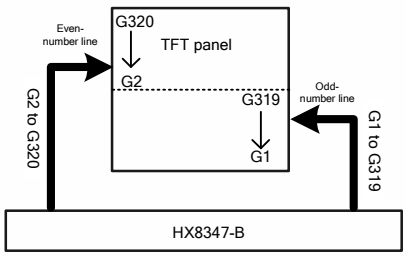
6.4 Driver Output Control (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

Figure 6.2: Driver Output Control Register (R01h)

SS: The source driver output shift direction selected. The shift direction from S1 to S528 when SS = 0. And shift direction from S528 to S1 when SS = 1. And if the BGR = 0, <R><G><B> color is assigned from S1. When SS = 1 and BGR = 1, <R><G><B> color is assigned from S528. Re-write to the GRAM after changed the SS bit or BGR bit.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

SM	GS	Scan direction
0	0	 G1, G2, G3, G4,.... G317, G318, G319, G320
0	1	 G320, G319, G318, G317,.... G4, G3, G2, G1
1	0	 G1, G3, G5,.... G315, G317, G319, G320 G2, G4, G6,.... G314, G316, G318, G320
1	1	 G320, G318, G316, G314,.... G6, G4, G2 G319, G317, G315, G313,.... G5, G3, G1

6.5 Driving Control (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0

Figure 6.3: Driving Control Register (R02h)

B/C: Specify LCD driving inversion type
"0" frame inversion
"1" line inversion

6.6 Entry Mode (R03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM			

Figure 6.4: Entry Control Register (R03h)

AM: The updating direction as write data to GRAM. The data will be written vertically when AM=1; the data will be written horizontally when AM=0. In case of window address range is given, data will be written to the GRAM in the range of the window address according to AM & I/D [1..0].

I/D[1..0]: The AC will incremented by 1 after data written to GRAM if I/D = 1; the AC will decremented by 1 after data written to GRAM if I/D=0.

The following figure depicts the update method with I/D1-0 & AM bit.

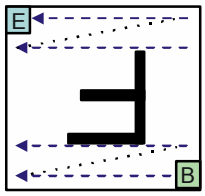
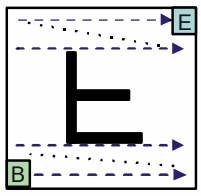
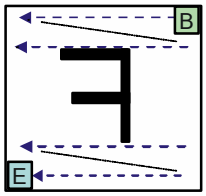
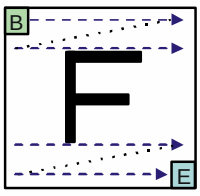
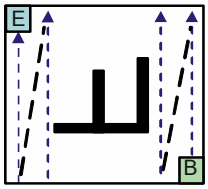
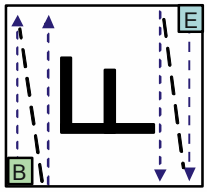
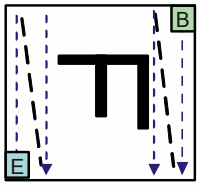
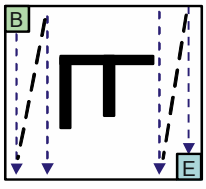
	I/D[1:0]= 00 Hortizontal:decrement Vertical:decrement	**I/D[1:0]= 01 Hortizontal:increment Vertical:decrement**	**I/D[1:0]= 10 Hortizontal:decrement Vertical:increment**	**I/D[1:0]= 11 Hortizontal:increment Vertical:increment**
AM=0 Horizontal				
AM=1 Vertical				

Figure 6.5: Address Direction Settings

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.
ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

BGR: RGB direction selection for Color filter setting.
BGR = "0": S1,S2,S3 filter order='R','G','B'
BGR = "1": S1,S2,S3 filter order='B','G','R'

TRI: When TRI=1, a pixel data is written to GRAM through transfer 3 times 8-bit bus interface.
DFM: Specify the data format when TRI=1.

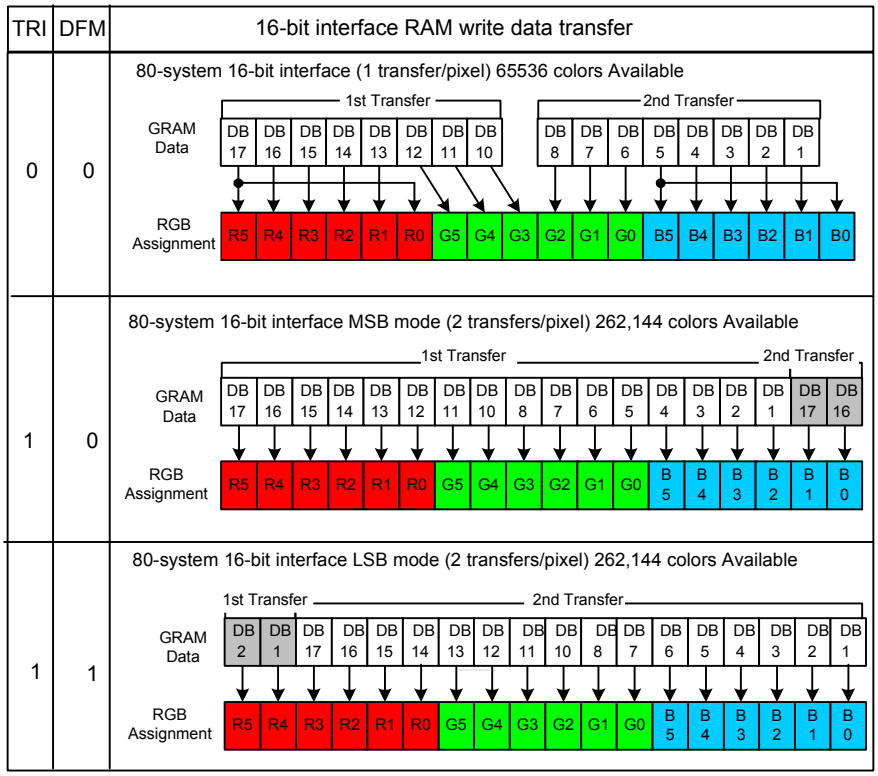


Figure 6.6: The Setting of DFM and TRI (80-system 16-bit Interface)

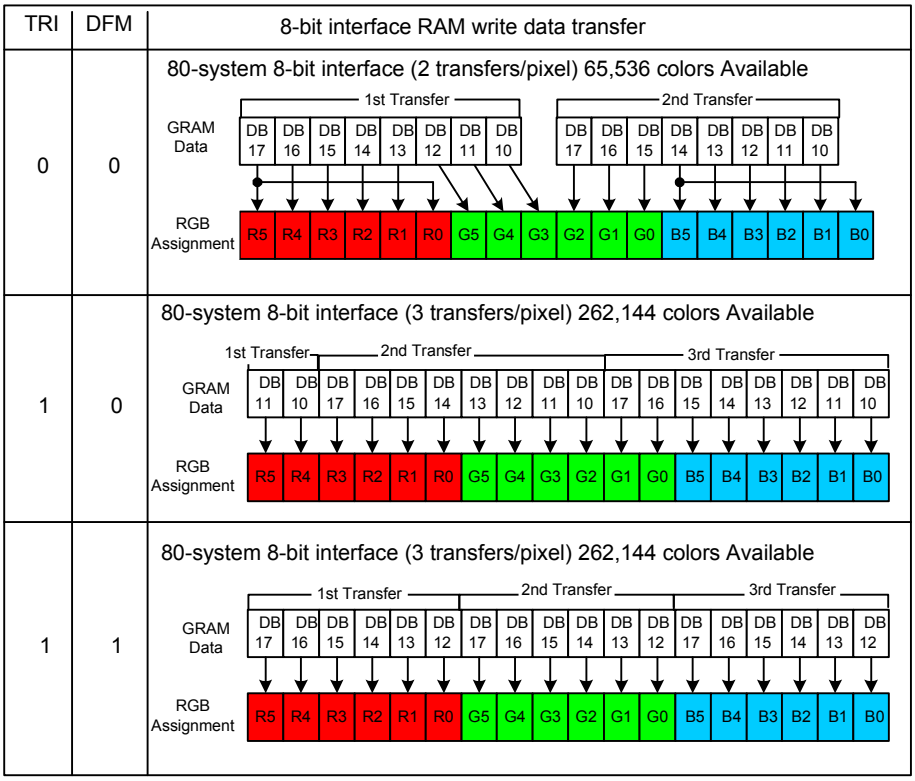


Figure 6.7: The Setting of DFM and TRI (80-system 8-bit Interface)

6.7 16 bits data mapping (R05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0

Figure 6.8: 16 bits color data mapping Register 2 (R05h)

EPF[1:0]: 65K color mode data format

EPF1	EPF0	16 bits color mapping
0	0	Data Bus: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 RGB Assignment: R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0 Data Read: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
0	1	Data Bus: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 RGB Assignment: R5 R4 R3 R2 R1 0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 0 Data Read: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
1	0	Data Bus: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 RGB Assignment: R5 R4 R3 R2 R1 1 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 1 Data Read: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
1	1	Data Bus: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 RGB Assignment: R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0 Data Read: DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 Green data=even — No → Red data=Blue data — Yes → G0 copy to R0/B0; Yes → Bypass; No → Bypass

6.8 Display Control 1 (R07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0

Figure 6.9: Display Control Register 1 (R07h)

D1–0: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8347-B can control the charging current for the LCD with AC driving.

Control the display on/off while control GON and DTE. When D1–0 = 01, the internal display of the HX8347-B is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	BASEE	Source Output	HX8347-B Internal Display Operations	Gate-Driver Control Signals
0	0	x	VSSD	Halt	Halt
0	1	x	VSSD	Operate	Operate
1	0	x	=PTS(0,0)	Operate	Operate
1	1	0	=PTS(0,0)	Operate	Operate
1	1	1	Base image Display	Operate	Operate

Note: Data can be written to the GRAM from the MPU regardless of the content of D1-0.

CL: CL = 1, the display mode is set to the 8-color display mode.

CL	Number of Display Colors
0	262,144
1	8

DTE, GON: Specify the output level of gate line.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

Note: GON bit is used in the gate driver. Control according to the bits' values is executed by the gate driver.

BASEE: Base image display enable bit. When BASEE = "0", no base image is displayed. The HX8347-B drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

Partial image 2 and Partial image 1 enable bits
PTDE1/0 = 0: turns off partial image. Only base image is displayed.
PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

6.9 Display Control 2 (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

Figure 6.10: Display Control Register 2 (R08h)

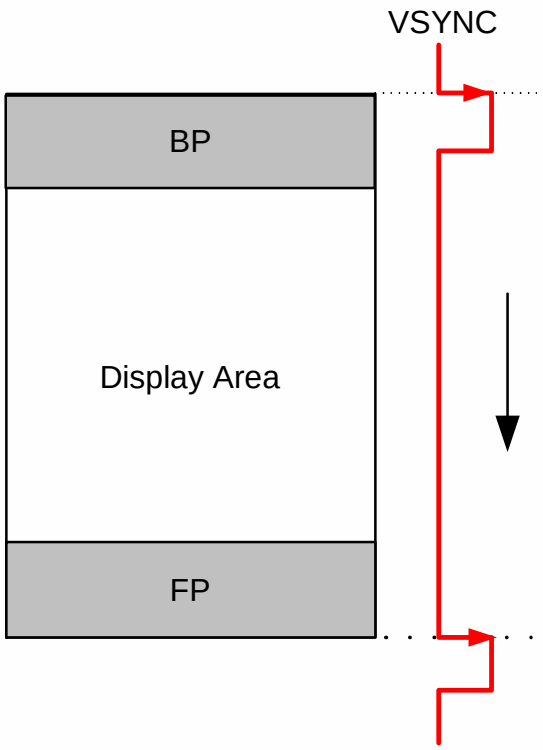
BP3-0: Specify the amount of scan line for back porch (BP).
FP3-0: Specify the amount of scan line for front porch (FP).

The setting vale, ensure that:
BP + FP ≦ 16 lines
PB ≧ 2 lines
FP ≧ 2 lines

In external display interface mode, the BP start on the falling edge of VSYNC signal, followed by he display operation. The FP starts after driving the number of scan line set with NL4-0. After the FP, the blank period continues until the next input of the VSYNC signal.

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	Number of FP Line	Number of BP Line
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	3 lines	
:	:	:	:	:	
1	1	0	1	13 lines	
1	1	1	0	14 lines	
1	1	1	1	Ignore	

Table 6.1: BP/FP Bits Setting



6.10 Display Control 3 (R09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

Figure 6.11: Display Control Register 3 (R09h)

PTG1-0: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	---
1	0	Interval scan
1	1	---

ISC3-0: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	0 frame	-
0	0	0	1	1 frame	-
0	0	1	0	3 frames	50 ms
0	0	1	1	5 frames	84 ms
0	1	0	0	7 frames	117 ms
0	1	0	1	9 frames	150 ms
0	1	1	0	11 frames	184 ms
0	1	1	1	13 frames	217 ms
1	0	0	0	15 frames	251 ms
1	0	0	1	17 frames	284 ms
1	0	1	0	19 frames	317 ms
1	0	1	1	21 frames	351 ms
1	1	0	0	23 frames	384 ms
1	1	0	1	25 frames	418 ms
1	1	1	0	27 frames	451 ms
1	1	1	1	29 frames	484 ms

PTS[1:0]: Specify the scan mode of Source in non-display area (front/back porch period and blank area between partial displays).

PTS[1:0]		Source/VCOM Outputs in Non-display Area
00	Refresh cycle	White
	Non-refresh cycle	Source=V63 VCOM=VCOML
01	Refresh cycle	Black
	Non-refresh cycle	Source=V0 VCOM=VCOML
10	Refresh cycle	White
	Non-refresh cycle	Source=GND VCOM=GND
11	Refresh cycle	White
	Non-refresh cycle	Source=Hi-Z VCOM=Hi-Z

6.11 Display Control 4 (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	TEMODE	0	0	0	TEOE	TEI2	TEI1	TEI0

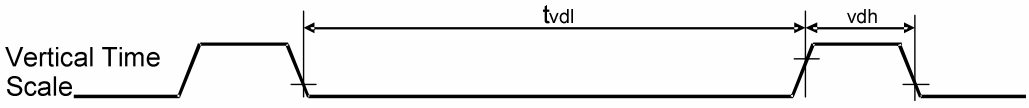
Figure 6.12: Display Control Register 4 (R0Bh)

TEI[2:0]: Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

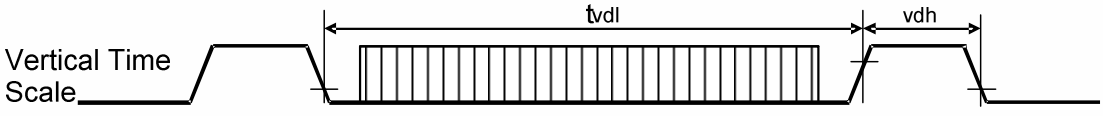
TEI[2:0]	Output Interval
000	1 frame
001	2 frame
010	3 frame
011	4 frame
100	5 frame
101	6 frame
110	7 frame
111	8 frame

TEOE: When TEOE=1, HX8347-B starts to output TE signal.

TEMODE: Specify the Tearing-Effect mode.
When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of Back Porch information only.



When **TEMODE** ='1': The Tearing Effect Output Line (TE) consists of both Back Porch and H-Blanking information



Note: During Stand by Mode with Tearing Effect Line On, Tearing Effect Output pin active low

6.12 RGB Interface Control 1 (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	ECN2	ECN1	ECN0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

Figure 6.13: RGB Interface Control Register (R0Ch)

RIM1-0: Specify the transfer mode of RGB interface. RIM, DM, RM must be set Before LCD display operation through the RGB interface. During the LCD display, not allow changing the setting vale.

RIM1	RIM0	Transfer Mode
0	0	18-bit bus RGB interface Mode (1 transfer/pixel)
0	1	16-bit bus RGB interface Mode (1 transfer/pixel)
1	0	6-bit bus RGB interface Mode (3 transfers/pixel)
1	1	Ignore

DM1-0: Specify the operation mode of LCD display. DM1-0 allows the switch operation between the internal clock operation mode and external display interface mode (RGB and VSYNC interface mode), but can't switch between RGB and VSYNC interface mode.

DM1	DM0	Operation Mode
0	0	System interface
0	1	RGB interface
1	0	VSYNC interface
1	1	Ignore

RM: Specify the access interface of GRAM. The setting value is not affected by the operation mode of LCD display. For example: In RGB interface operation mode, the data can be access to GRAM through RGB interface when RM=1, and then also access to GRAM through system interface when RM=0.

RM	Access Interface
0	• System interface • VSYNC interface
1	RGB interface

Note: (1) The register is set only through the system interface.
(2) A DOTCLK input and Data transfers must be executed in dot unit (R, G, B) for 6-bit bus RGB interface mode.

ENC[2:0]: Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle
000	1 frame
001	2 frame
010	3 frame
011	4 frame
100	5 frames
101	6 frames
110	7 frames
111	8 frame

6.13 TE Output Position (R0Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	TEP8	TEP7	TEP6	TEP5	TEP4	TEP3	TEP2	TEP1	TEP0

Figure 6.14: TE Output Position (R0Dh)

TEP[8:0] Sets the output position of frame cycle (TE signal).
When TEP[8:0]=0, a high-active pulse TE is output at the start of back porch period for one display line period (1H).Make sure the 9'h000 ≦ TEP ≦ BP+NL+FP

TEP[8:0]	TE Output Position
9'h000	0th line
9'h001	1st line
9'h002	3rd line
9'h003	4th line
:	:
:	:
9'h175	373rd line
9'h176	374th line
9'h177	375th line

6.14 RGB Interface Control 2 (R0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

Figure 6.15: RGB Interface Control Register 2 (R0Fh)

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	ENABLE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to DB17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to DB17-0

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

6.15 Power Control 1 (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB

Figure 6.16: Power Control Register 1 (R10h)

STB: When STB = "1", the HX8347-B into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator thus the current consumption can be reduced.

SLP: When SLP = 1, the HX8347-B into the sleep mode, where the internal display operations are suspend except for the R-C oscillator, thus the current consumption can be reduced.

AP2–0: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Gamma driver amplifiers	Source driver amplifiers
0	0	0	Stop	Stop
0	0	1	1.00	1.00
0	1	0	1.00	0.75
0	1	1	1.00	0.50
1	0	0	0.75	1.00
1	0	1	0.75	0.75
1	1	0	0.75	0.50
1	1	1	0.5	0.50

BT2–0: Switch the output factor for step-up circuit. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.0V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	1	5.0V	-VCI	3DDVDH	-2DDVDH
0	1	0	5.0V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	5.0V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
1	0	0	5.0V	-VCI	VCI+2DDVDH	-2DDVDH
1	0	1	5.0V	-VCI	VCI+2DDVDH	VCI-2DDVDH
1	1	0	5.0V	-VCI	2DDVDH	-2DDVDH
1	1	1	5.0V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V, DDVDH_TRI=0

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	6.1V	-VCI	Setting inhabited	Setting inhabited
0	0	1	6.1V	-VCI	3DDVDH	-2DDVDH
0	1	0	6.1V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	6.1V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
1	0	0	6.1V	-VCI	VCI+2DDVDH	-2DDVDH
1	0	1	6.1V	-VCI	VCI+2DDVDH	VCI-2DDVDH
1	1	0	6.1V	-VCI	2DDVDH	-2DDVDH
1	1	1	6.1V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V, DDVDH_TRI=1

SAP: Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = “1” to start the generation of power supply according to the power supply startup sequence.

6.16 Power Control 2 (R11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	0	0	0

Figure 6.17: Power Control Register 2 (R11h)

DC0[2:0]: Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DC02	DC01	DC00	Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

DC1[2:0]: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DC12	DC11	DC10	Operation Frequency of Step-up Circuit 2 and Extra Step-up Circuit 2
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note : Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

6.17 Power Control 3 (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	DDVDH_TRI	XDK	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0

Figure 6.18: Power Control Register 3 (R12h)

VRH[3:0]: Set the magnification of amplification for VREG1OUT voltage. (VCOM, reference voltage for grayscale voltage).

XDK, DDVDH_TRI: Specify the ratio of step-up circuit for DDVDH voltage generation.

DDVDH_TRI	XDK	Step-up Circuit 1	Capacitor Connection Pins Used
0	0	2 x VCI	C11P, C11N
0	1	2 x VCI	C11P, C11N, C12P, C12N
1	0	3 x VCI	C11P, C11N, C12P, C12N
1	1	Setting inhabited	Setting inhabited

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.
VCIRE=0, External reference voltage VCI (default)
VCIRE =1, Internal reference voltage 2.5V

VCIRE=0				
VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt
0	0	0	1	VCIx2.00
0	0	1	0	VCIx2.05
0	0	1	1	VCIx2.10
0	1	0	0	VCIx2.20
0	1	0	1	VCIx2.30
0	1	1	0	VCIx2.40
0	1	1	1	VCIx2.40
1	0	0	0	VCIx1.60
1	0	0	1	VCIx1.65
1	0	1	0	VCIx1.70
1	0	1	1	VCIx1.75
1	1	0	0	VCIx1.80
1	1	0	1	VCIx1.85
1	1	1	0	VCIx1.90
1	1	1	1	VCIx1.95

VCIRE=1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt
0	0	0	1	2.5Vx2.00=5.000V
0	0	1	0	2.5Vx2.05=5.125V
0	0	1	1	2.5Vx2.10=5.250V
0	1	0	0	2.5Vx2.20=5.500V
0	1	0	1	2.5Vx2.30=5.750V
0	1	1	0	2.5Vx2.40=6.000V
0	1	1	1	2.5Vx2.40=6.000V
1	0	0	0	2.5Vx1.60=4.000V
1	0	0	1	2.5Vx1.65=4.125V
1	0	1	0	2.5Vx1.70=4.250V
1	0	1	1	2.5Vx1.75=4.375V
1	1	0	0	2.5Vx1.80=4.500V
1	1	0	1	2.5Vx1.85=4.625V
1	1	1	0	2.5Vx1.90=4.75V
1	1	1	1	2.5Vx1.95=4.875V

6.18 Power Control 4 (R13h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

Figure 6.19: Power Control Register 4 (R13h)

VDV4-0: Sets the amplification factors for Vcom.

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VRGE1OUT x 0.70
0	0	0	0	1	VRGE1OUT x 0.72
0	0	0	1	0	VRGE1OUT x 0.74
0	0	0	1	1	VRGE1OUT x 0.76
0	0	1	0	0	VRGE1OUT x 0.78
0	0	1	0	1	VRGE1OUT x 0.80
0	0	1	1	0	VRGE1OUT x 0.82
0	0	1	1	1	VRGE1OUT x 0.84
0	1	0	0	0	VRGE1OUT x 0.86
0	1	0	0	1	VRGE1OUT x 0.88
0	1	0	1	0	VRGE1OUT x 0.90
0	1	0	1	1	VRGE1OUT x 0.92
0	1	1	0	0	VRGE1OUT x 0.94
0	1	1	0	1	VRGE1OUT x 0.96
0	1	1	1	0	VRGE1OUT x 0.98
0	1	1	1	1	VRGE1OUT x 1.00

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VRGE1OUT x 0.94
0	0	0	0	1	VRGE1OUT x 0.96
0	0	0	1	0	VRGE1OUT x 0.98
0	0	0	1	1	VRGE1OUT x 1.00
0	0	1	0	0	VRGE1OUT x1.02
0	0	1	0	1	VRGE1OUT x 1.04
0	0	1	1	0	VRGE1OUT x1.06
0	0	1	1	1	VRGE1OUT x 1.08
0	1	0	0	0	VRGE1OUT x1.10
0	1	0	0	1	VRGE1OUT x 1.12
0	1	0	1	0	VRGE1OUT x1.14
0	1	0	1	1	VRGE1OUT x 1.16
0	1	1	0	0	VRGE1OUT x1.18
0	1	1	0	1	VRGE1OUT x 1.20
0	1	1	1	0	VRGE1OUT x1.22
0	1	1	1	1	VRGE1OUT x 1.24

Note: Set the Vcom Amplitude is lower than 6.0V.

6.19 RAM Address Set (R20h~R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 6.20: RAM Address Register (R20h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

Figure 6.21: RAM Address Register (R21h)

AD[16:0]: Set GRAM addresses to the address counter (AC) before access the GRAM. Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bits. During the standby mode, the GRAM cannot be accessed.

AD[16:0]	GRAM Setting
“00000”h – “000EF”h	Bitmap data for G1
“00100”h – “001EF”h	Bitmap data for G2
“00200”h – “002EF”h	Bitmap data for G3
:	:
“13D00”h – “13DEF”h	Bitmap data for G318
“13D00”h – “13EEF”h	Bitmap data for G319
“13F00”h – “13FEF”h	Bitmap data for G320

6.20 RAM data Write/Read (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 6.22: Read data register (R22h)

WD[17:0]: Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

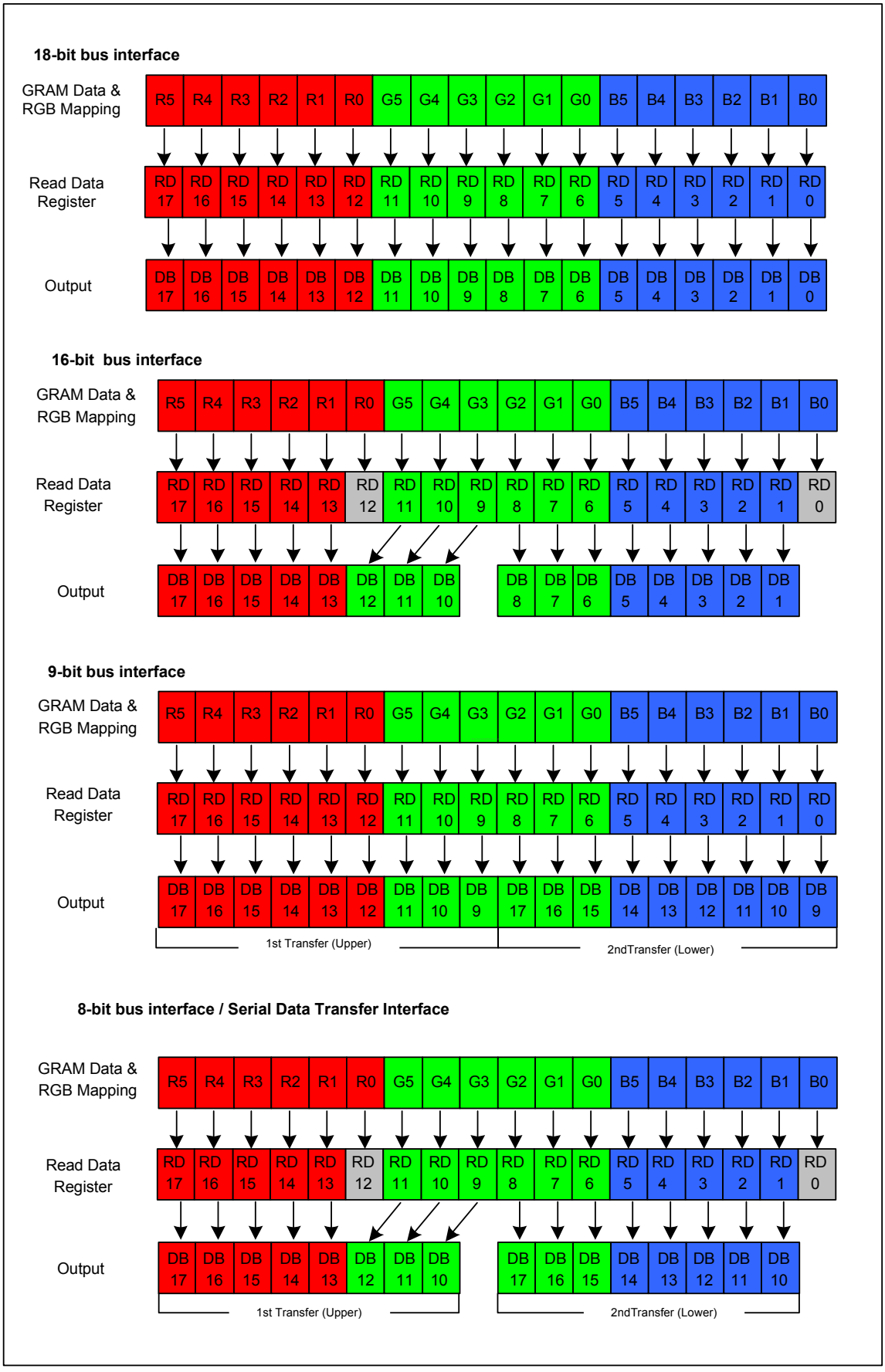


Figure 6.23: Output Data Read from GRAM through Read Data Register in 18-/16- /9- /8-bit Interface Mode

6.21 Power Control 7 (R29h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 6.24: Power Control Register 7 (R29h)

VCM[5:0]: Sets the VCOM High voltage.

VCM[5:0]	Vcom High Voltage
6'h00	VRGE1OUT x 0.685
6'h01	VRGE1OUT x 0.690
6'h02	VRGE1OUT x 0.695
6'h03	VRGE1OUT x 0.700
6'h04	VRGE1OUT x 0.705
6'h05	VRGE1OUT x 0.710
6'h06	VRGE1OUT x 0.715
6'h07	VRGE1OUT x 0.720
6'h08	VRGE1OUT x 0.725
6'h09	VRGE1OUT x 0.730
6'h0A	VRGE1OUT x 0.735
6'h0B	VRGE1OUT x 0.740
6'h0C	VRGE1OUT x 0.745
6'h0D	VRGE1OUT x 0.750
6'h0E	VRGE1OUT x 0.755
6'h0F	VRGE1OUT x 0.760
6'h10	VRGE1OUT x 0.765
6'h11	VRGE1OUT x 0.770
6'h12	VRGE1OUT x 0.775
6'h13	VRGE1OUT x 0.780
6'h14	VRGE1OUT x 0.785
6'h15	VRGE1OUT x 0.790
6'h16	VRGE1OUT x 0.795
6'h17	VRGE1OUT x 0.800
6'h18	VRGE1OUT x 0.805
6'h19	VRGE1OUT x 0.810
6'h1A	VRGE1OUT x 0.815
6'h1B	VRGE1OUT x 0.820
6'h1C	VRGE1OUT x 0.825
6'h1D	VRGE1OUT x 0.830
6'h1E	VRGE1OUT x 0.835
6'h1F	VRGE1OUT x 0.840

VCM[5:0]	Vcom High Voltage
6'h20	VRGE1OUT x 0.845
6'h21	VRGE1OUT x 0.850
6'h22	VRGE1OUT x 0.855
6'h23	VRGE1OUT x 0.860
6'h24	VRGE1OUT x 0.865
6'h25	VRGE1OUT x 0.870
6'h26	VRGE1OUT x 0.875
6'h27	VRGE1OUT x 0.880
6'h28	VRGE1OUT x 0.885
6'h29	VRGE1OUT x 0.890
6'h2A	VRGE1OUT x 0.895
6'h2B	VRGE1OUT x 0.900
6'h2C	VRGE1OUT x 0.905
6'h2D	VRGE1OUT x 0.910
6'h2E	VRGE1OUT x 0.915
6'h2F	VRGE1OUT x 0.920
6'h30	VRGE1OUT x 0.925
6'h31	VRGE1OUT x 0.930
6'h32	VRGE1OUT x 0.935
6'h33	VRGE1OUT x 0.940
6'h34	VRGE1OUT x 0.945
6'h35	VRGE1OUT x 0.950
6'h36	VRGE1OUT x 0.955
6'h37	VRGE1OUT x 0.960
6'h38	VRGE1OUT x 0.965
6'h39	VRGE1OUT x 0.970
6'h3A	VRGE1OUT x 0.975
6'h3B	VRGE1OUT x 0.980
6'h3C	VRGE1OUT x 0.985
6'h3D	VRGE1OUT x 0.990
6'h3E	VRGE1OUT x 0.995
6'h3F	VRGE1OUT x 1.000

6.22 Frame rate Control (R2Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0

Figure 6.25: Frame rate Register 7 (R2Bh)

FRS[3:0]: Set the frame rate when using the internal oscillator.

FRS[3:0]	Frame Rate(Hz)	FRS[3:0]	Frame Rate(Hz)
4'h0	30	4'h8	50
4'h1	35	4'h9	55
4'h2	40	4'hA	60
4'h3	45	4'hB	70
4'h4	65	4'hC	80
4'h5	75	4'hD	90
4'h6	120	4'hE	100
4'h7	130	4'hF	110

6.23 Gamma Control Register (R30h~R3Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	MP12	MP11	MP10	0	0	0	0	0	MP02	MP01	MP00
W	1	0	0	0	0	0	MP32	MP31	MP30	0	0	0	0	0	MP22	MP21	MP20
W	1	0	0	0	0	0	MP52	MP51	MP50	0	0	0	0	0	MP42	MP41	MP40
W	1	0	0	0	0	0	MN32	MN31	MN30	0	0	0	0	0	MN22	MN21	MN20
W	1	0	0	0	0	0	MN52	MN51	MN50	0	0	0	0	0	MN42	MN41	MN40
W	1	0	0	0	0	0	CN12	CN11	CN10	0	0	0	0	0	CN02	CN01	CN00
W	1	0	0	0	OP14	OP13	OP12	OP11	OP10	0	0	0	0	OP03	OP02	OP01	OP00
W	1	0	0	0	ON14	ON13	ON12	ON11	ON10	0	0	0	0	ON03	ON02	ON01	ON00

Figure 6.26: Gamma Control Register 1~10 (R30h~R3Dh)

MP5-0 [2:0]: Gamma adjustment registers for positive polarity output
CP1-0 [2:0]: Gamma gradient adjustment registers for positive polarity output
MN5-0 [2:0]: Gamma adjustment registers for negative polarity output
CN1-0 [2:0]: Gamma gradient adjustment registers for negative polarity output
OP0 [3:0]/OP1 [4:0]: amplification adjustment resistor for positive polarity output
ON0 [3:0]/ON1 [4:0]: amplification average adjustment resistor for negative polarity output
For details, refer to Gamma Adjustment Function section.

6.24 Get Scan lines (R45h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	SL8	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

Figure 6.27: Get Sacn lines Register (R45h)

HX8347-B can return the current scanline N; customer can use to update the display. The first scanline is defined as the first line as Line 0.

6.25 Horizontal Start (R50h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

Figure 6.28: Horizontal RAM Start Address Position Register (R50h)

6.26 Horizontal END (R51h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HAE2	HEA1	HEA0

Figure 6.29: Horizontal RAM END Address Position Register (R51h)

6.27 Vertical Start (R52h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 6.30: Vertical RAM Start Address Position Register (R52h)

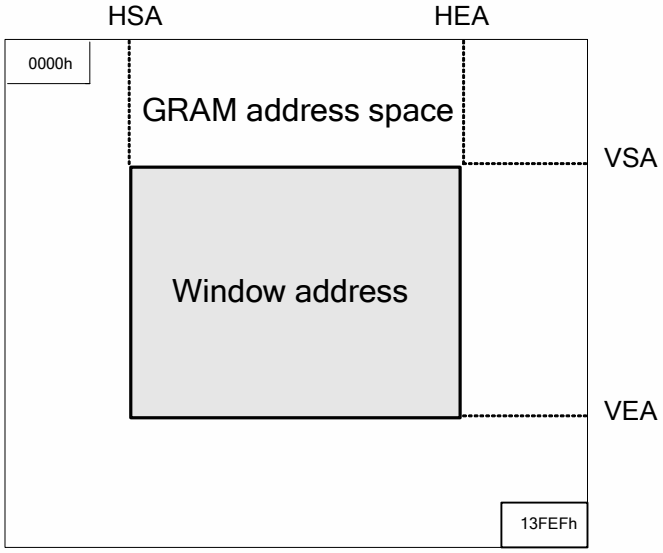
6.28 Vertical END (R53h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

Figure 6.31: Vertical RAM END Address Position Register (R53h)

HAS[7:0]/HEA[7:0]: Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by HAS[7:0] to the address specified by HEA[7:0].Ensure that “00”h ≤HAS[7:0] ≤HEA[7:0] ≤”EF”h

VSA[8:0]/VEA[8:0]: Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM from the address specified by VSA[8:0] to the address specified by VEA[8:0]. Ensure that “000”h ≤VSA[8:0] ≤VEA[8:0] ≤”13F”h



Window address setting range
“00”h ≤HAS[7:0] ≤HEA[7:0] ≤”EF”h
“000”h ≤VSA[8:0] ≤VEA[8:0] ≤”13F”h

Note: The window address range must be within the GRAM address space.

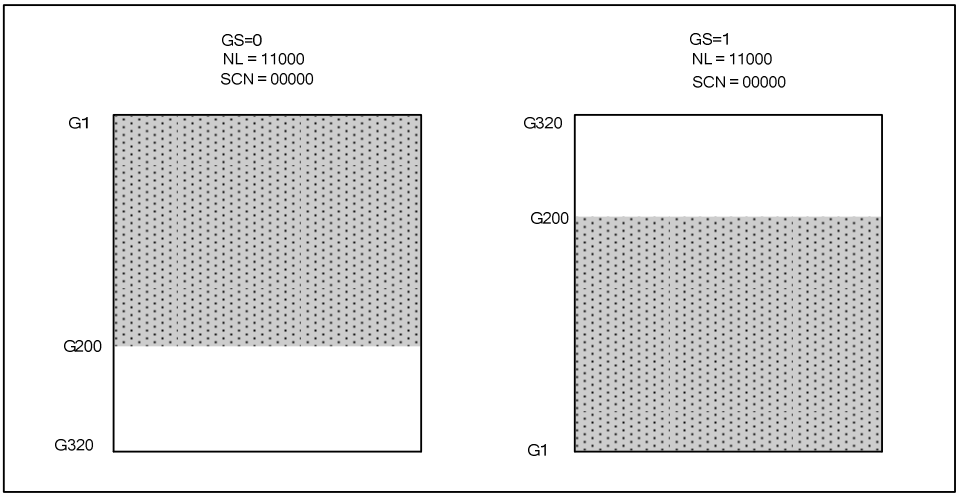
6.29 Gate Scan Start Position (R60h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 6.32: Gate Scan Position Register (R60h)

SCN[5:0]: Set the scanning starting position of the gate driver.

Scanning Start Position				
SCN[5:0]	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h~3Fh	Setting disabled			



Note: (1) Don't set NL, SCN over the end position of gate line (G220)
(2) Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 220.

Figure 6.33: SCN Bits and Scanning Start Position for Gate Driver

NL[4:0]: Specify the number of scan lines for the LCD driver can be adjusted by every 8 lines. Select the setting value for the panel size or higher.

NL[5:0]	LCD Drive line	NL[5:0]	LCD Drive line
00h	8 line	14h	168 line
01h	16 line	15h	176 line
02h	24 line	16h	184 line
03h	32 line	17h	192 line
04h	40 line	18h	200 line
05h	48 line	19h	208 line
06h	56 line	1Ah	216 line
07h	64 line	1Bh	224 line
08h	72 line	1Ch	232 line
09h	80 line	1Dh	240 line
0Ah	88 line	1Eh	248 line
0Bh	96 line	1Fh	256 line
0Ch	104 line	20h	264 line
0Dh	112 line	21h	272 line
0Eh	120 line	22h	280 line
0Fh	128 line	23h	288 line
10h	136 line	24h	296 line
11h	144 line	25h	304 line
12h	152 line	26h	312 line
13h	160 line	27h	320 line
others	Setting disabled		

GS: Specify the shift direction of gate driver output. When GS = 0, the shift direction from G1 to G320. When GS = 1, the shift direction from G320 to G1.

6.30 Base Image Control (R61h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

Figure 6.34: Base Image Control Register (R61h)

REV: REV = 1 selects the inversion of the display of all characters and graphics. This bit allows the display of the same data on both normally-white and normally-black panels.

REV	GRAM data	Display area	
		Positive Polarity	Negative Polarity
0	18'h00000 . . 18'h3FFFF	V63 . . V0	V0 . . V63
1	18'h00000 . . 18'h3FFFF	V0 . . V63	V63 . . V0

VLE: This bit turns on scroll mode by setting VLE = '1'. The scroll mode window is described by the Vertical Scroll Area command **VL[8:0]**. To leave scroll mode to normal mode, the **VLE** bit should be set to '0'.

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Display area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

6.31 SPI Read/Write Control (R66h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RW

Figure 6.35: SPI Read/Write Control (R66h)

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used. If users need to read back the register data by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

RW	Description
0	Register write mode (default)
1	Register read mode

6.32 Vertical Scroll Control (R6Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 6.36: Vertical Scroll Control (R6Ah)

VL[8:0]: Specify the amount of scrolling line from 0 to 320 in the display to enable smooth vertical scrolling.

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling Length
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	1	1	3 lines
	:	:	:	:	:		:	:	:
1	0	0	1	1	1	1	0	0	317 lines
1	0	0	1	1	1	1	1	0	318 lines
1	0	0	1	1	1	1	1	1	319 lines

6.33 Partial Image 1 Display Position (R80h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTDP 08	PTDP 07	PTDP 06	PTDP 05	PTDP 04	PTDP 03	PTDP 02	PTDP 01	PTDP 00

Figure 6.37: Partial Image 1 Display Position (R80h)

PTDP0[8:0]: Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

6.34 Partial Image 1 Area (Start Line) (R81h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTSA 08	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00

Figure 6.38: Partial Image 1 Area (Start Line) (R81h)

6.35 Partial Image 1 Area (End Line) (R82h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTEA 08	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 11	PTEA 10

Figure 6.39: Partial Image 1 Area (Start Line) (R81h)

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

6.36 Partial Image 2 Display Position (R83h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTDP 18	PTDP 17	PTDP 16	PTDP 15	PTDP 14	PTDP 13	PTDP 12	PTDP 11	PTDP 10

Figure 6.40: Partial Image 2 Display Position (R83h)

PTDP1[8:0]: Sets the display start position of partial image 2. The display areas of the partial images 1 and 2 must not overlap each another.

6.37 Partial Image 2 Area (Start Line) (R84h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTSA 18	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10

Figure 6.41: Partial Image 2 Area (Start Line) (R84h)

6.38 Partial Image 2 Area (End Line) (R85h)

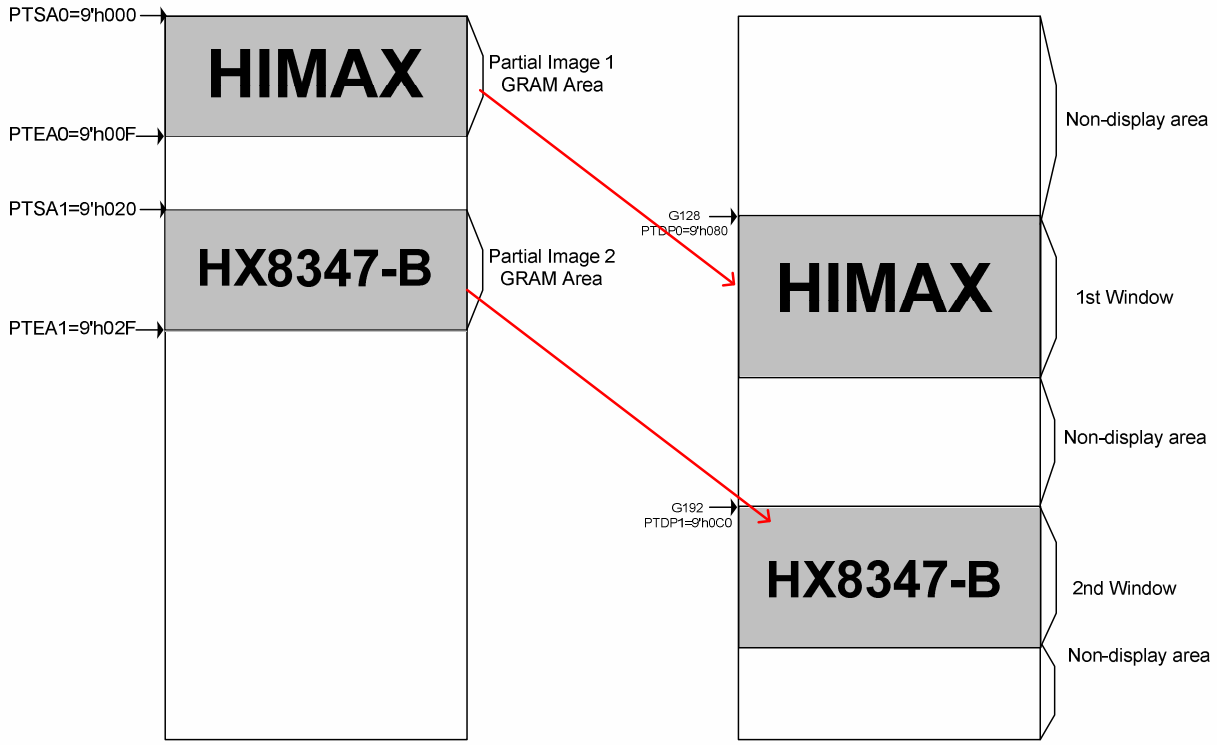
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	PTEA 18	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10

Figure 6.42: Partial Image 2 Area (Start Line) (R85h)

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[8:0] ≤ PTEA1[8:0].

The following example shows the setting for partial display function.

Base Image Setting	
BASEE	0
NL[5:0]	6'h27
Partial Display 1 Setting	
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Display 2 Setting	
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0



Base image OFF:BASEE='0'
Number of Scan Line : NL[5:0] = 6'h27 (320 lines)
Partial Display 1: PTDP[8:0]=9'h080,PTSA0[8:0]=9'h000,PTEA0[8:0]=9'h00F
Partial Display 2: PTDP[8:0]=9'h0C0,PTSA0[8:0]=9'h020,PTEA0[8:0]=9'h02F

6.39 Panel Interface Control 1 (R90h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0

Figure 6.43: Panel Interface Control 1 (R90h)

RTNI[4:0]: Sets 1H (line) clock number of internal clock operating mode. In this mode, HX8347-B display operation is synchronized with internal clock signal.

Clock cycles=1/internal operation clock frequency (fosc)

RTNI[4:0]	Clock number per Line	RTNI[3:0]	Clock number per Line
5'b00000	127	5'b10000	143
5'b00001	128	5'b10001	144
5'b00010	129	5'b10010	145
5'b00011	130	5'b10011	146
5'b00100	131	5'b10100	147
5'b00101	132	5'b10101	148
5'b00110	133	5'b10110	149
5'b00111	134	5'b10111	150
5'b01000	135	5'b11000	151
5'b01001	136	5'b11001	152
5'b01010	137	5'b11010	153
5'b01011	138	5'b11011	154
5'b01100	139	5'b11100	155
5'b01101	140	5'b11101	156
5'b01110	141	5'b11110	157
5'b01111	142	5'b11111	158

DIVI[1:0]: Specify the division ratio of internal clocks for internal operation. When used internal clock for the display operation.

DIVI1	DIVI0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Note: fosc = R-C oscillation frequency

6.40 Panel Interface Control 2 (R92h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

Figure 6.44: Panel Interface Control 2 (R92h)

NOWI[2:0]: Sets the gate output non-overlap period when HX8347-B display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	Invalid
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	Invalid

6.41 Panel Interface Control 3 (R97h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

Figure 6.45: Panel Interface Control 5 (R97h)

NOWE[2:0]: Sets the gate output non-overlap period when HX8347-B display operation is synchronized with RGB interface signal.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	Setting disabled	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	11 clocks
0100	4 clocks	1100	12 clocks
0101	5 clocks	1101	Setting disabled
0110	6 clocks	1110	Setting disabled
0111	7 clocks	1111	Setting disabled

6.42 Panel Interface Control 4 (R98h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SM_P	SS_P	GS_P	REV_P	BGR_P

Figure 6.46: Panel Interface Control 4 (R98h)

This command is internal use for display panel setting.

REV_P: The source output data polarity selected. When REV_P=0, the data will not reverse. When REV_P = 1, the data will reverse.

BGR_P: The color filter order direction selected. When BGR_PANEL=0, don't reverse the BGR setting. When BGR_P = 1, the color filter order will be reversed.

GS_P: The gate driver output shift direction selected. When GS_P=0, the shift direction don't reverse GS setting. When GS_P = 1, the shift direction will be reversed.

SS_P: The source driver output shift direction selected. When SS_P=0, the shift direction don't reverse SS setting. When SS_P = 1, the shift direction will be reversed.

SM_P: The gate scan direction selected. When SM_P=0, the shift direction don't reverse SM setting. When SM_P = 1, the shift direction will be reversed.

6.43 OTP VCM Status and Enable (RA2h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN

Figure 6.47: OTP VCM Status and Enable (RA2h)

PGM_CNT[1:0]: OTP programmed record, when VCM programming time <4. These bits are read only.

OTP_PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times
11	OTP programmed 3 times

VCM_D[5:0]: OTP VCM data read value.

VCM_EN: OTP VCM data enable.
'1': Set this bit to enable OTP VCM data to replace R29h VCM value.
'0': Default value, use R29h VCM value

6.44 OTP Index and OTP Mask (RA3h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	OTP_Index7	OTP_Index6	OTP_Index5	OTP_Index4	OTP_Index3	OTP_Index2	OTP_Index1	OTP_Index0	OTP_Mask7	OTP_Mask6	OTP_Mask5	OTP_Mask4	OTP_Mask3	OTP_Mask2	OTP_Mask1	OTP_Mask0

Figure 6.48: OTP Index and Mask (RA3h)

OTP_Index[7:0]: Set index location in OTP to be programmed.
OTP_Mask[7:0]: OTP bit programming mask, if set to '1', it means the related bit in OTP can not be programmed.

6.45 OTP Programming Function (RA4h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	Load_Dis	VPP_EN	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG

Figure 6.49: OTP Programming ID Key (RA4h)

OTP_PROG: When this bit is set to '1', LSI writes data to OTP from internal register.
OTP_PTM[1:0]: Internal use, not open.
OTP_PWE: Internal use, not open.
OTP_POR: When set to '1', OTP data can be read the related OTP Index data at OTP_DATA[7:0]
VPP_SEL: When set to '1', Internal Power voltage is fed to OTP.
VPP_EN: When set to '1', OTP Power OP is ready.
OTP_LOAD_DISABLE: Internal use, not open.

6.46 OTP Programming ID Key (RA5h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY1 0	KEY 9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0

Figure 6.50: OTP Programming ID Key (RA5h)

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

.

6.47 Write Display Brightness (RB1h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Figure 6.51: Write Display Brightness (RB1h)

6.48 Read Display Brightness (RB2h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Figure 6.52: Read Display Brightness (RB2h)

6.49 Write CTRL Display Value (RB3h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	BCTR L	0	DD	BL	0	0

Figure 6.53: Write CTRL Display Value (RB3h)

6.50 Read CTRL Display Value (RB4h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	0	0	BCTR L	0	DD	BL	0	0

Figure 6.54: Read CTRL Display Value (RB3h)

6.51 Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

Figure 6.55: Write Content Adaptive Brightness Control Value (RB5h)

6.52 Read Content Adaptive Brightness Control value (RB6h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

Figure 6.56: Read Content Adaptive Brightness Control Value (RB6h)

6.53 Write CABC Minimum Brightness (RBEh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

Figure 6.57: Write CABC Minimum Brightness (RBEh)

6.54 Read CABC Minimum Brightness (RBFh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

Figure 6.58: Read CABC Minimum Brightness (RBFh)

These commands are used to set CABC parameter

DBV[7:0]: The backlight PWM pulse output duty is equal to DBV[7:0]/255 x CABC_duty.

BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.
'0' = Off (Equal to DBV[7:0] = '00h')
'1' = On (Brightness registers are active.)

DD: Display Dimming (Only for manual brightness setting)
'0': Display Dimming is off.
'1': Display Dimming is on.

BL: Backlight Control On/Off
'0' = Off (Completely turn off backlight circuit. Control lines must be low.)
'1' = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

C[1:0]: This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

CMB[7:0]: This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

6.55 CABC Control 1 (RC7h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEDONPOL	LEDPWMPOL

Figure 6.59: CABC Control 1 (RC7h)

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM Pin
0	0	0
1	0	PWM signal
0	1	1
1	1	Inversed PWM signal

LEDONPOL: This bit is used to control LEDON pin.

'0': LEDON pin='L'

'1': LEDON pin='H'

6.56 CABC Control 2 (RC8h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	PWM DIV7	PWM DIV6	PWM DIV5	PWMDIV4	PWM DIV3	PWM DIV2	PWM DIV1	PWM DIV0

Figure 6.60: CABC Control 2 (RBFh)

PWM_PERIOD[7:0] : The backlight PWM output period setting.

Backlight PWM output period = (PWM_CLK / (255x(PWM_PERIOD[7:0]+1))

6.57 ID Control (RDAh~DCh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 6.61: ID1 (RDAh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 6.62: ID2 (RDBh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 6.63: ID3 (RDCh)

ID1~ID3: ID setting related register.

6.58 Deep stand by control (RE6h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB

Figure 6.64: Deep stand by control (RE6h)

DP_STB: It can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained. For details, please refer to “6.7 Power On/Off Sequence” section for detail use.

6.59 OTP Data (RF3h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	OTP_DATA7	OTP_DATA6	OTP_DATA5	OTP_DATA4	OTP_DATA3	OTP_DATA2	OTP_DATA1	OTP_DATA0

Figure 6.65: OTP Data (RF3h)

OTP_DATA[7:0]: Read OTP data.

6.60 OTP ID CNT (RF4h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	ID1_CNT3	ID1_CNT2	ID1_CNT1	ID1_CNT0	0	ID2_CNT3	ID2_CNT2	ID2_CNT1	ID2_CNT0	0	ID3_CNT3	ID3_CNT2	ID3_CNT1	ID3_CNT0

Figure 6.66: OTP ID CNT (RF4h)

6.61 OTP VCOM CNT (RF5h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	0	0	0	0	OTP_DATA7	OTP_DATA6	OTP_DATA5	OTP_DATA4	OTP_DATA3	OTP_DATA2	OTP_DATA1	OTP_DATA0

Figure 6.67: OTP VCOM CNT (RF3h)

ID3_CNT[3:0]: ID3 OTP Programming time counter.
ID2_CNT[3:0]: ID2 OTP Programming time counter.
ID1_CNT[3:0]: ID1 OTP Programming time counter.
VDV_CNT[3:0]: VDV voltage OTP Programming time counter.
VCM_CNT[3:0]: VCOMH OTP Programming time counter.

CNT[3:0]	Description
0000	OTP clean
0001	OTP programmed 1 time
0010	OTP programmed 2 times
0011	OTP programmed 3 times
0100	OTP programmed 4 times
0101	OTP programmed 5 times
0110	OTP programmed 6 times
0111	OTP programmed 7 times
1000	OTP programmed 8 times

7. Layout Recommendation

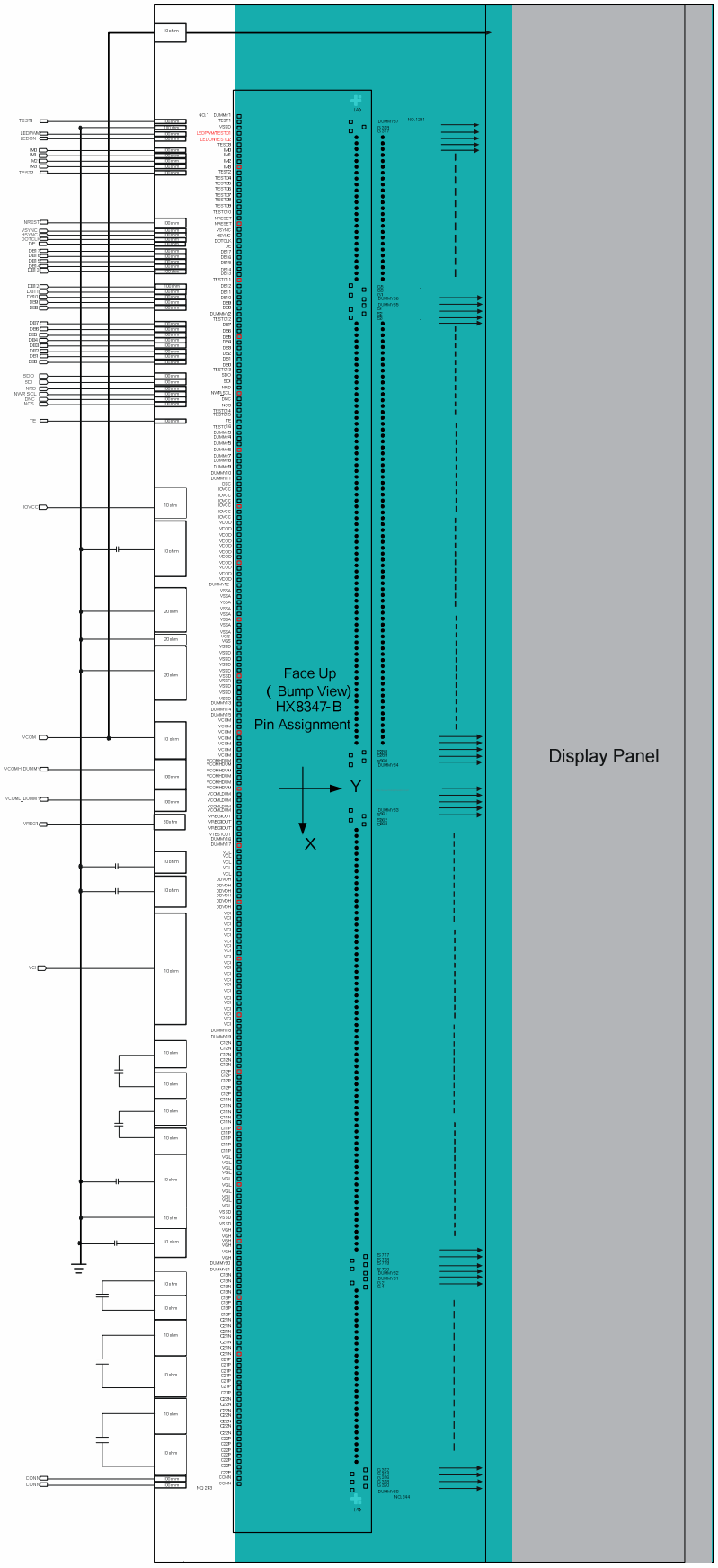


Figure 7.1: Layout recommendation of HX8347-B

7.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
IM[3:0]	Input	100	Ω
NRD, NWR_SCL, DNC, NCS, SDA	Input	100	Ω
NRESET	Input	100	Ω
TE, LEDPWM,LEDON	Output	100	Ω
DB[17:0],	I/O	100	Ω
DOTCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1OUT	Capacitor connection	50	Ω
C11P, C11N, C12P, C12N	Capacitor connection	10	Ω
C31P, C12N	Capacitor connection	10	Ω
C21P, C21N	Capacitor connection	15	Ω
C22P, C22N	Capacitor connection	15	Ω
TESTO15~0	Input	100	Ω
VCOMHDUM, VCOMLDUM,DUMMY	Dummy	100	Ω
VTEST	Test Pin	100	Ω

7.2 External components connection

Capacitor	Recommended voltage	Capacity
C1 (C11P/N)	6V	1µF (B characteristics)
C2 (C12P/N)	6V	1µF (B characteristics)
C3 (DDVDH)	10V	1µF (B characteristics)
C4 (C21P/N)	10V	1µF (B characteristics)
C5 (C22P/N)	10V	1µF (B characteristics)
C6 (VGH)	25V	1µF (B characteristics)
C7 (VGL)	16V	1µF (B characteristics)
C8 (C31P/N)	6V	1µF (B characteristics)
C9 (VCL)	6V	1µF (B characteristics)
C10(VDDD)	6V	1µF (B characteristics)

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3 to +6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to +4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	0 to -16.5	Note(8)
Logic Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3 to IOVCC+0.5	-
Operating Temperature	Topr	℃	-40 to +85	Note(9),(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

Table 8.1: Absolute Maximum Ratings

8.2 ESD Protection Level

Mode	Test Condition	Protection Level	Unit
Human Body Model	C=100 pF, R=1.5 kΩ	±2.0K	V
Machine Model	C=200 pF, R=0.0 Ω	±200	V

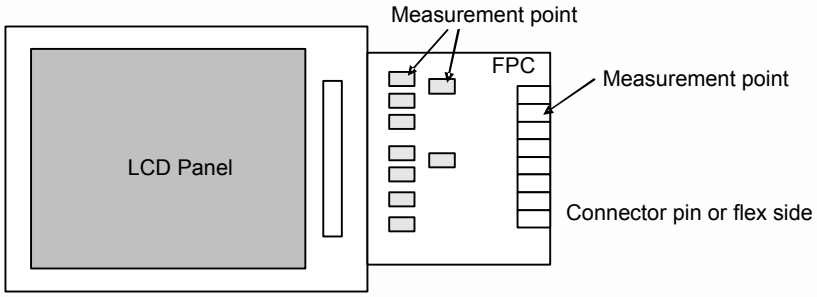
Table 8.2: ESD Protection Level

8.3 DC Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.3	2.8	3.3	
Source Drive Voltage	VREG1	Triple Pump	3.3	4.65	5.8	
	VREG1	Dual Pump	3.3	4.65	4.8	
Gate Drive High Voltage	VGH	IVGH=30uA (Typ:BT=001) VCI=2.8 Dual Pump	TBD	TBD	-	
		IVGH=30uA (Typ:BT=001) VCI=2.8 Triple Pump	TBD	TBD	-	
Gate Drive Low Voltage	VGL	IVGL=30uA (Typ:BT=001) VCI=2.8 Dual Pump	TBD	TBD	-	
		IVGL=30uA (Typ:BT=001) VCI=2.8 Triple Pump	TBD	TBD	-	
Drive Supply Voltage	|VGH-VGL|	-	-	-	30	
Input / Output						
High level input voltage	VIH	IOVCC=1.65~1.95	0.7IOVCC	-	IOVCC	V
Low level input voltage	VIL		VSSD	-	0.3IOVCC	
High level input voltage	VIH	IOVCC=1.95~3.3	0.8IOVCC	-	IOVCC	
Low level input voltage	VIL		VSSD	-	0.2IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
Oscillator frequency	fOSC	Frame rate at 60hz,default Vs and Hs setting T_A=25℃	2.76	2.85	2.94	MHz
Booster(VCI=2.8V)						
DDVDH boost voltage1	DDVDH	Dual Pump IDDVDH=300uA	4.8	5.0	5.2	V
		Triple Pump IDDVDH=300uA	5.9	6.1	6.3	
VCL boost voltage	VCL	ICL=-100uA	-2.5	-2.65	2.75	
VCOM Generator(VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	2.5	4.4	7.3	V
		No load Triple Pump	2.5	4.4	8.3	V
VCOM high level	VCOMH	No load Dual Pump	2.5	3.205	4.8	V
		No load Triple Pump	2.5	3.205	5.8	V
VCOM low level	VCOML	No load	-2.5	-1.195	VSSD	V
Source Driver(Typ:T_A=25℃ VCI=2.8V)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VREG1-1.0	-	±10	±20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	±30	±50	mV
Output voltage range	VOS	-	0.1	-	DDVDH-0.1	V
Output offset voltage	Voff	-		±30	±50	mV

Current Consumption(Typ: T_A=25℃ IOVCC=VCI=2.8V)						
Normal operation	Iiovcc	GRAM data =0000h Frame rate=60Hz	-	TBD	-	mA
	Ivci		-	TBD	-	mA
Sleep in	Iiovcc	-	-	-	20	µA
	Ivci	-	-	-	10	µA

Note: VREG1/VCOMH/VCOML conditions: When Internal Voltage VREF=4.8V for dual pump and VREF=5.8V for Triple pump



8.4 AC Characteristics

8.4.1 Parallel Interface Characteristics (8080-series MPU)

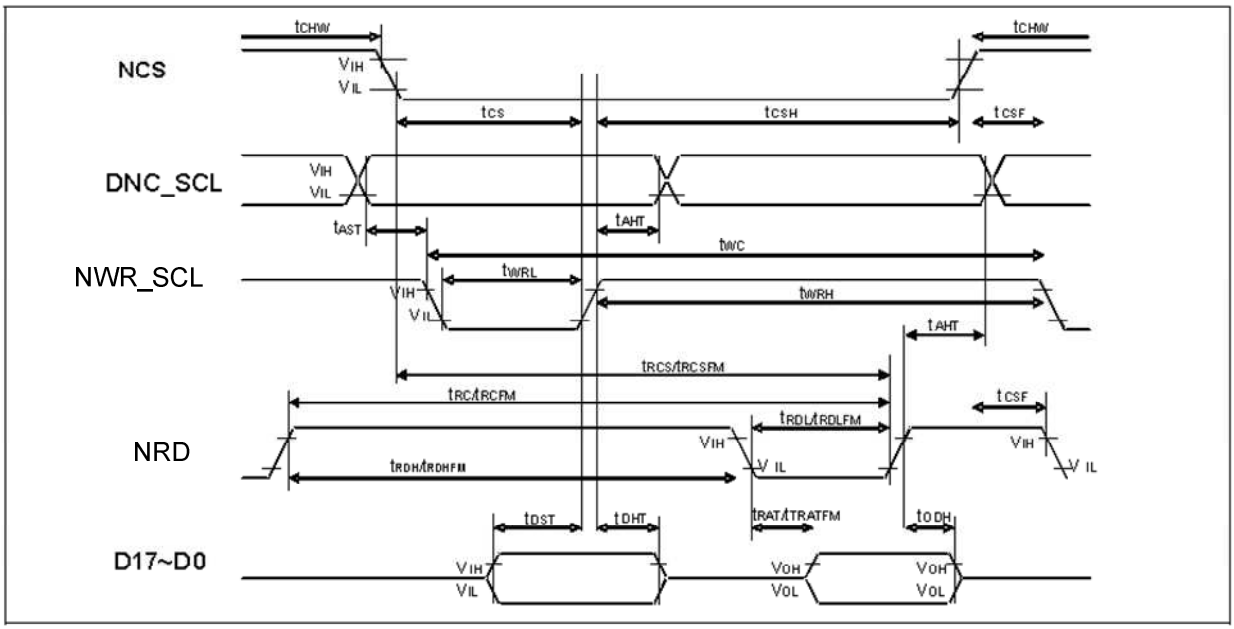
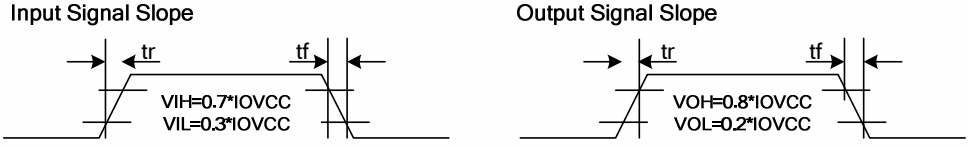


Figure 8.1: Parallel Interface Characteristics (8080-Series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select "H" pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 15 45 355 10 10	- - - - - -	ns	-
NWR_SCL	t_{WC} twc t_{WRH} t_{WRL}	Write cycle(18bits interface) Write cycle(8/9/16 bits 262k interface) Control pulse "H" duration Control pulse "L" duration	100 66 15 15	- - -	ns	-
NRD(ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse "H" duration (ID) Control pulse "L" duration (ID)	160 90 45	- - -	ns	When read ID data
NRD(FM)	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) Control pulse "H" duration (FM) Control pulse "L" duration (FM)	450 90 355	- - -	ns	When read from frame memory
DB17 to DB0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - 60 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



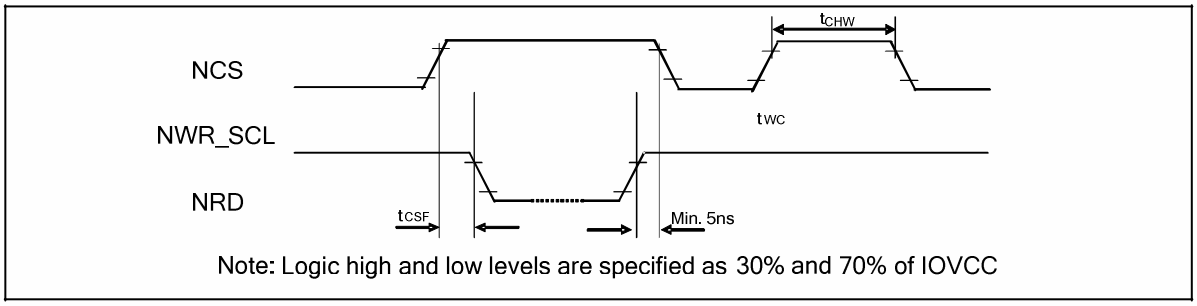


Figure 8.2: Chip Select Timing

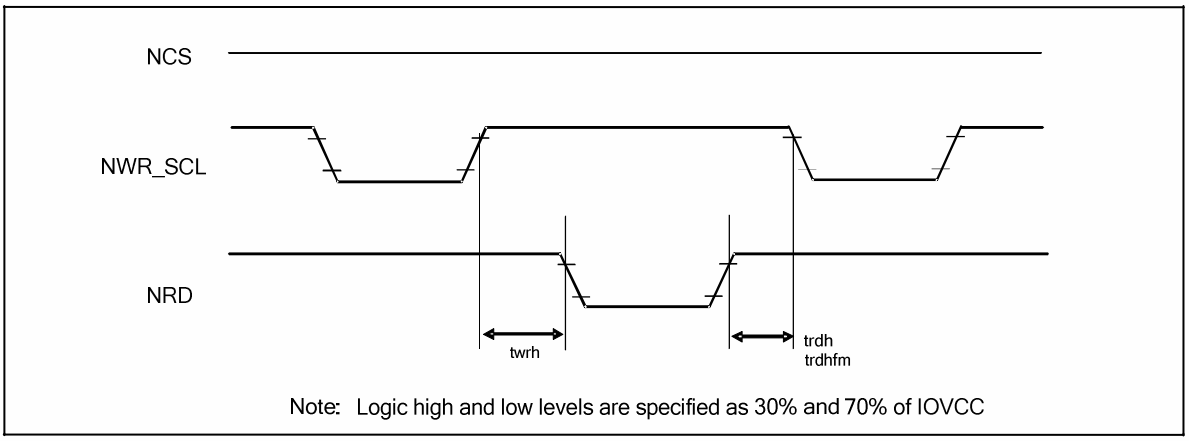


Figure 8.3: Write to Read and Read to Write Timing

8.4.2 Serial Interface Characteristics

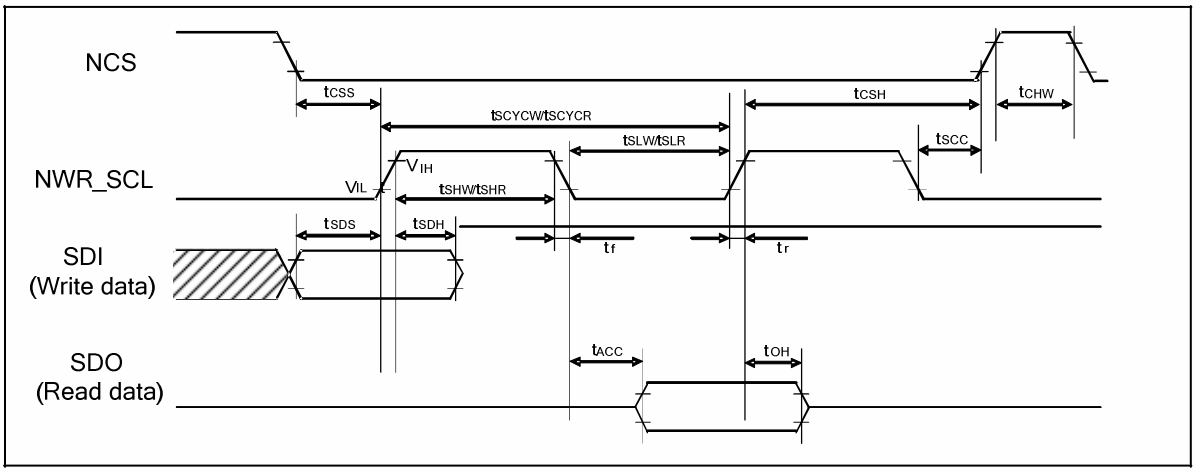


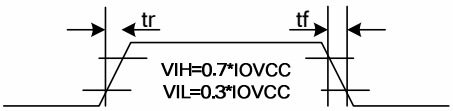
Figure 8.4: Serial Interface Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)

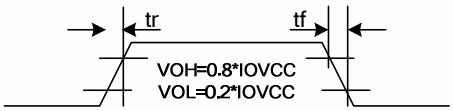
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	66 15 15	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDI	10 10	- -	- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDI for maximum C_L=30pF For minimum C_L=8pF	10	-	50	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	50	ns
SCL to Chip select	t_{SCC}	SCL, NCS	15	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	40	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 65	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

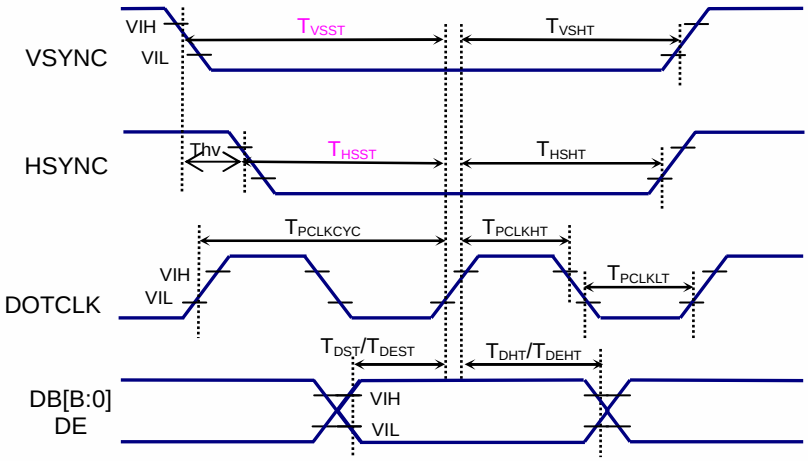
Input Signal Slope



Output Signal Slope



8.4.3 RGB Interface Characteristics

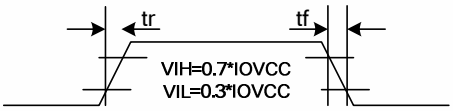


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70° C)

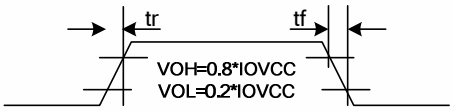
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	T_{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T_{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T_{VSST}	-	15	-	-	ns
Vertical Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T_{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T_{VSSHT}	-	15	-	-	ns
Data Enable set-up time	T_{DEST}	-	15	-	-	ns
Data Enable hold time	T_{DEHT}	-	15	-	-	ns
Data set-up time	T_{DST}	-	15	-	-	ns
Data hold time	T_{DHT}	-	15	-	-	ns
Phase difference of sync signal falling edge	Thv	-	0	-	240	Dotclk

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

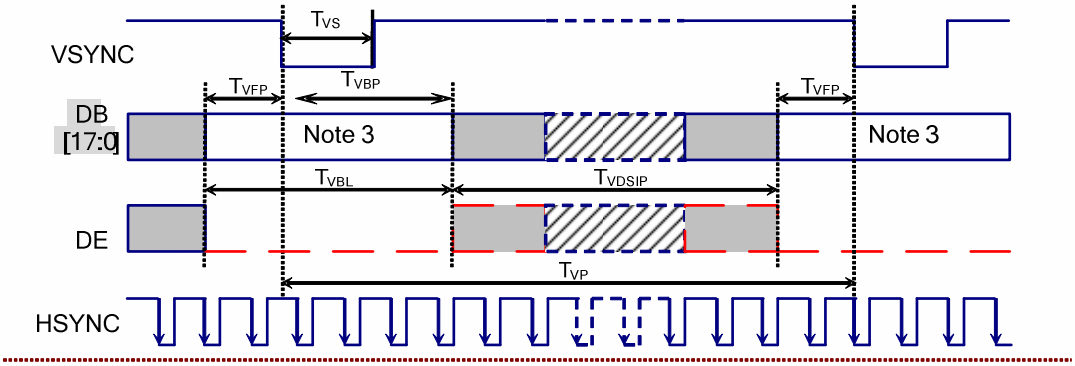
Input Signal Slope



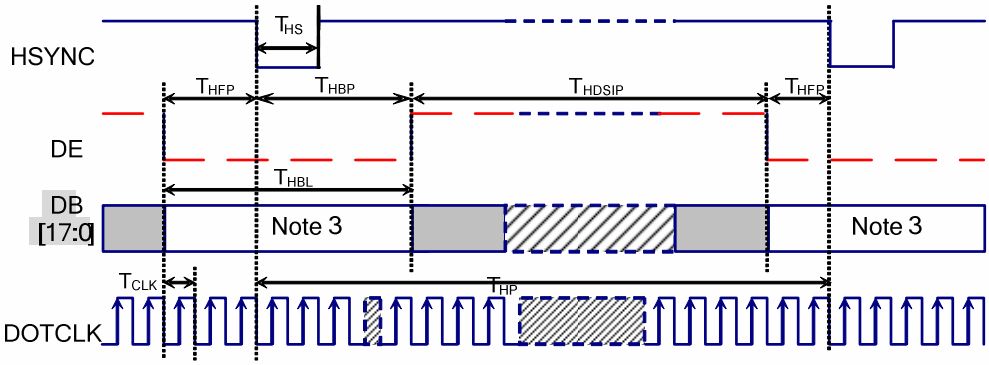
Output Signal Slope



Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



Item	Symbol	Condition	Specification			Unit
			Min	Typ.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	324	326	352	HS
Vertical low pulse width	T_{VS}	-	2	2	-	HS
Vertical front porch	T_{VFP}	-	2	2	16	HS
Vertical back porch	T_{VBP}	-	2	4	16	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	6	32	HS
Vertical active area	T_{VDISP}	-	-	320	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	TVRR	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	244	252	272	DOTCLK
Horizontal low pulse width	T_{HS}	-	2	2	-	DOTCLK
Horizontal front porch	T_{HFP}	-	2	4	16	DOTCLK
Horizontal back porch	T_{HBP}	-	2	8	16	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	4	12	32	DOTCLK
Horizontal active area	T_{HDISP}	-	-	240	-	DOTCLK
Pixel clock cycle TVRR=60Hz	f_{CLKCYC}	-	3.9	-	10	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, T_A=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(3) HP is multiples of DOTCLK.

8.4.4 Reset Input Timing

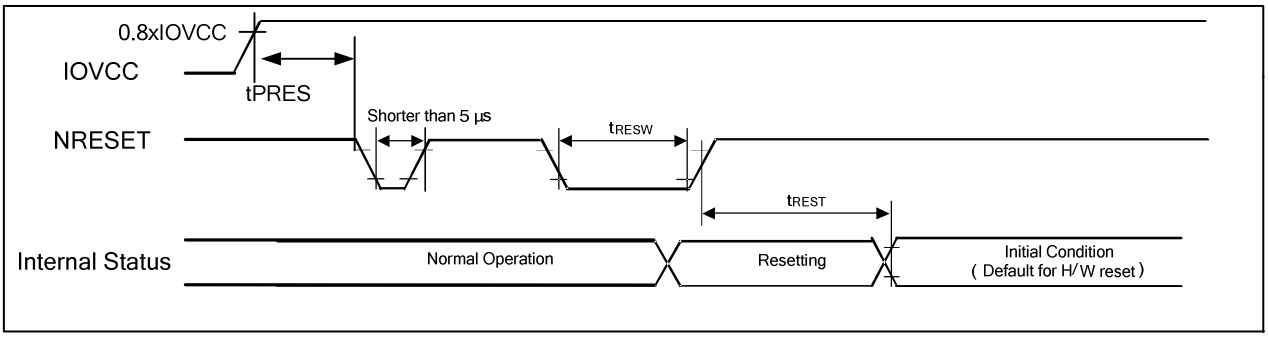


Figure 8.5: Reset Input Timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

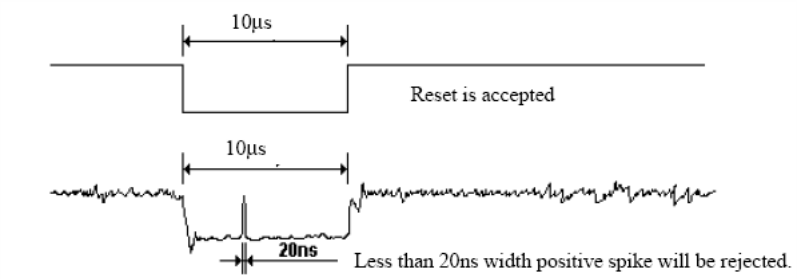
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5 µs and 10µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

9. Ordering Information

Part No.	Package
HX8347-B000 PDxxx	PD : mean COG xxx : mean chip thickness (µm), (default: 280 µm)

10.Revision History

Version	Date	Description of Changes
01	2009/12/24	New setup