DATA SHEET

(DOC No. HX8352-B01-DS)

HX8352-B01(T)

240RGB x 432 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 November, 2009

Himax Technologies, Inc.
http://www.himax.com.tw

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List of Contents

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1. General Description

This document describes HX8352-B01 240RGBx432 dots resolution driving controller. The HX8352-B01 is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx432 dots at maximum.

The HX8352-B01 can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8352-B01 also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8352-B01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

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2. Features

2.1 Display

- Resolution:
  - 240(H) x RGB(H) x 320(V)
  - 240(H) x RGB(H) x 400(V)
  - 240(H) x RGB(H) x 432(V)
- Display Color modes
  - Normal Display Mode On
    1. System Interface Circuit
       a. 4,096(R(4),G(4),B(4)) colors
       b. 65,536(R(5),G(6),B(5)) colors
       c. 262,144(R(6),G(6),B(6)) colors
    2. RGB Interface Circuit
       1. 65,536(R(5),G(6),B(5)) colors
       2. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors

- Display color modes
  - Full color mode:
    - 262k colours (18bit 6(R):6(G):6(B))
  - Reduce color mode:
    - 65k colours (16bit 5(R):6(G):5(B))
    - 4096 colours(12bit 4(R):4(G):4(B))

2.2 Display module

- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - VLCD = 4.6 to 6.0V (Source output voltage range)
  - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240(H) x 432(V) x 18bit

2.3 Display/control interface

- Display Interface types supported
  - System interface:
    a. 8-/9-/16-/18-bit parallel bus system interface
    b. 3-/4-wire serial bus system interface
  - RGB interface:
    a. 6-/16-/18-bit RGB interface
  - MDDI (Mobile Display Digital Interface) interface

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- Color modes
  - 12 bit/pixel: R(4), G(4), B(4)
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6))

2.4 Power supply

- Logic voltage (IOVCC): 1.65V ~ 3.3V
- Analog voltage (VCC): 2.3V ~ 3.3V
- Analog voltage (VCI): 2.3V ~ 3.3V
- MDDI power supply (MDDI_VCC): 2.3V ~ 3.3V

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support 1~7 Line inversion or Farme inversion
- Support Digital gamme correction
- Support Area scrolling
- Support Partial display mode
- Support Deep standby mode
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (One-time-programming) and MTP(three-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function

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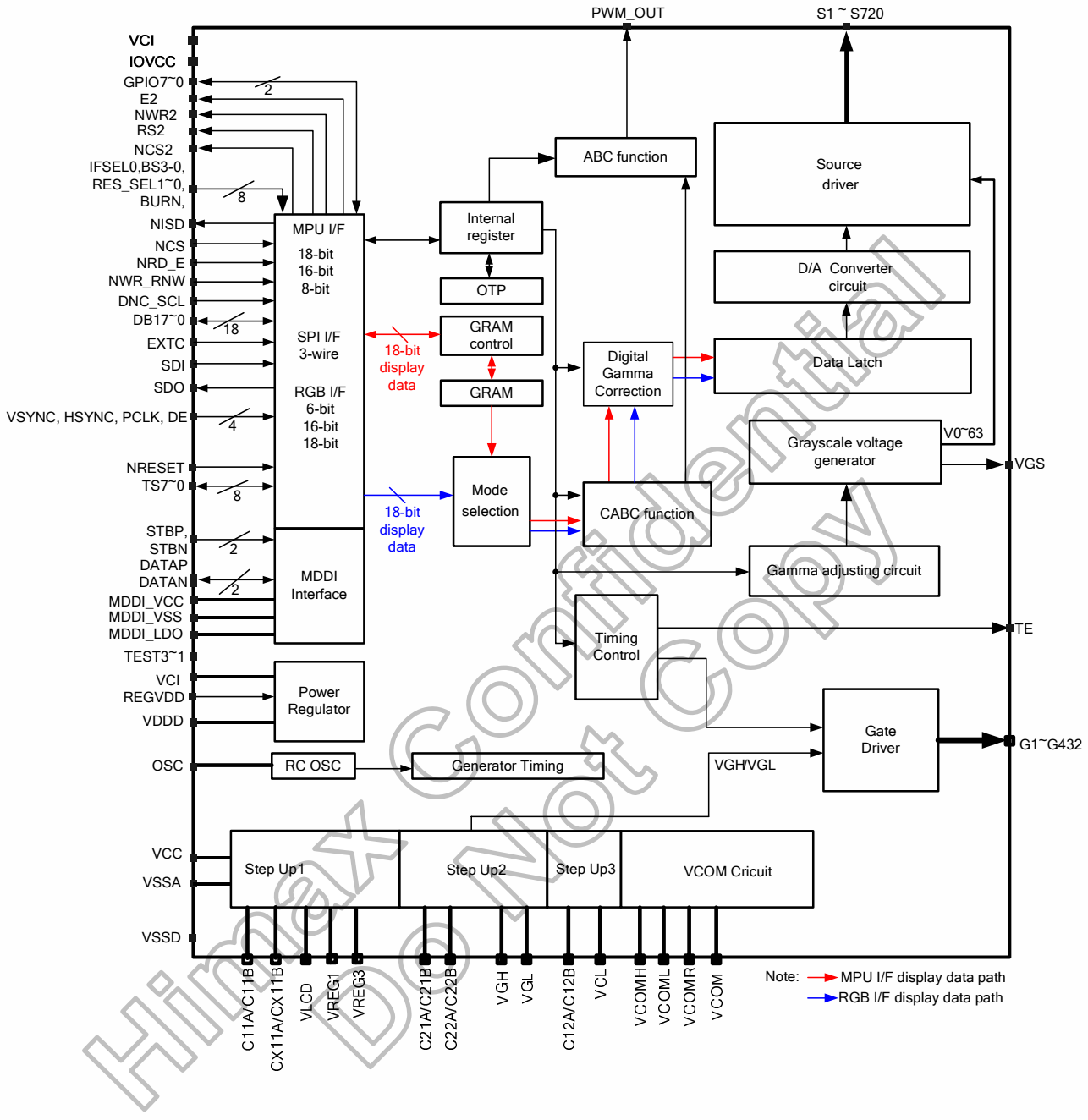
3. Block Diagram



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4. Pin Description

4.1 Pin description

<table>
<tr><th colspan="4">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>ILSEF0, BS3, BS2, BS1, BS0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
If not used, please fix this pin to IOVCC or VSSD level.
<table>
<tr><th>IFSEL0</th><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface</th></tr>
<tr><td rowspan="8">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-bits Parallel II</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel II</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bits Parallel II</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel II</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>3-wire Serial interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire Serial interface(1)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>SPI (2), MDDI Interface</td></tr>
<tr><td rowspan="9">1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">8080 MCU 16-bits Parallel I</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel I</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">8080 MCU 8-bits Parallel I</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 9-bits Parallel I</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>ID</td><td>3w serial interface</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>1</td><td>SPI (2), MDDI Interface</td></tr>
</table>
Note: (1) Under BS(3-0)=110X, the NWR_RNW signal wil be as DNC function.
(2) Under BS(3-0)=1111, SPI -3W(ID=1) just support to asscess CMD to, when MDDI into hibernation mode.</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>The pin as Dummy Pin.</td></tr>
<tr><td>RES_SEL1~0</td><td>I</td><td>2</td><td>MPU</td><td>Panel Resolution select pin.
<table>
<tr><th rowspan="2">RES_SEL1~0</th><th rowspan="2">Panel Resolution</th><th colspan="2">Gate pin state</th></tr>
<tr><th>Connect to Panel</th><th>Open</th></tr>
<tr><td>11</td><td>Ignore</td><td>---</td><td>---</td></tr>
<tr><td>10</td><td>240RGB x 432 dot</td><td>G1 ~ G432</td><td>---</td></tr>
<tr><td>01</td><td>240RGB x 400 dot</td><td>G1 ~ G400</td><td>G401 ~ G432</td></tr>
<tr><td>00</td><td>240RGB x 320 dot</td><td>G1 ~ G320</td><td>G321 ~ G432</td></tr>
</table></td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a write signal and write data at the low level.
M68 I/F mode: 0: Write , 1: Read.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a read signal and read data at the low level.
M68 I/F mode: : 0: Read/Write disable, 1: Read/Write enable.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>Data / Command Selection pin
When under SPI interface, it servers as SCL (Serial Clock)
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td>Free Running mode
If BURN=Hi, this can enable free running mode for burn in test.
The display data alternates between full black and full white independent of input data in free running mode. (weak pull low)</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Pixel clock signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
</table>

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Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
ENABLE	I	1	MPU	A data ENABLE signal for RGB I/F mode. Must be connected to VSSD or IOVCC.
OSC	I	1	Oscillation Resistor	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VCOMR	I	1	Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8352-B01.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G432	O	432	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL, Source and VCOM would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.
PWM_OUT	O	1	LED driver IC	Backlight On/Off control pin. If use ABC function, the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC.
NWR2	O	1	Sub Panel	80-interface NWR signal output pin for Sub Panel
E2	O	1	Sub Panel	80-interface Enable signal output pin for Sub Panel
NCS2	O	1	Sub Panel	The signal is Chip select for Sub Panel.
RS2	O	1	Sub Panel	The signal is register index or register parameter select for Sub Panel

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B CX11A,CX11B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
DB17~0 (DBS17~0)	I/O	24	MPU	When Operates in MPU interface mode, it is used liked an 18-bit bi-directional data bus. About data bus format, please refer “Table 5.1 Input Bus Format Selection of System Interface Circuit”. When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. About RGB data bus format, please refer “Table 5.20 RGB interface Bus Width Set Table” If use MDDI interface, these pins are sub panel data bus (DBS17~DBS0). Let unused pins to the open.
SDI	I	1	MPU	Serial data input pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. **If not use, let it open or connected to IOVCC.**

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Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial data output pin in serial bus system interface. The data is outputted on the rising edge of the SCL signal. **If not use, let it open.**
GPIO7~0	I/O	8	-	Standard Input/Output pin As for GPIO7 to 0 terminal, setting of an input and output direction is possible.

MDDI Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
STBP, STBN	-	2	MDDI Host	MDDI Strobe differential signal input pins. STBP pin for Strobe+, STBN pin for Strobe-. Connect to a terminal resistance (100Ω) between STBP and STBN. If not used, please let it connected to VSSD.
DATAP DATAN	-	2	MDDI Host	MDDI Data differential signal input pins. DATAP pin for Data+, DATAN pin for Data-. Connect to a terminal resistance (100Ω) between DATAP and DATAN. If not used, please let it connected to VSSD.
MDDI_VCC	P	1	Power Supply	MDDI I/O power supply pin, 2.3V~3.3V.
MDDI_VSS	P	1	Ground	MDDI I/O ground pin.
MDDI_LDO	O	1	Capacitor	MDDI regulator output pin. Connect to a stabilizing capacitor between MDDI_VSS and MDDI_LDO. If not used, please open these pins.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	1	Power Supply	IO Pad and Digital power supply, 1.65V~3.3V
VCC	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VCI	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	VSSD/ IOVCC	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. Must be connected to IOVCC or VSSD. **(weak pull high)**
VREG1	P	1	open	Internal generated stable power for source driver unit.
VREF	O	1	Open	Internal reference voltage output pin, please open this pin.
VCOMH	P	1	open	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	open	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI.
VLCD	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and VLCD.
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2.or 2 ~ 3 time the VLCD level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH.

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Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2.or –(2VLCD-VCI)~ –(2VLCD+ VCI). The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL.
VREG3	P	1	open	The power for internal measurement used, please let it open..

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
TS8~0	O	9	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
TEST_MODE	I	1	Open	MDDI test pin. Must be left open.
TEST_PAD_DRV	I	1	Open	MDDI test pin. Must be left open.
TEST_MODE_CLK	I	1	Open	MDDI test pin. Must be left open.
DUMMYR1-2	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.
DUMMYR3-4	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR3 and DUMMYR4 are short-circuited within the chip.
DUMMY1~88	-	88	Open	Dummy pads
IOGNDDUM1-10	O	10	Open	Dummy pin between MDDI pin, Leave them open.
DMY_IOVCC	O	10	-	Dummy IOVCC output pads, Internal connected to IOVCC and only for external Hardware setting pin use. If not used, please open these pins.
DMY_GND	O	8	-	Dummy GND output pads, Internal connected to VSSD and only for external Hardware setting pin use. If not used, please open these pins.

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4.2 Pin assignment

Chip Size: 18680 um x 720 um
(Including Seal-ring 15 um*2
Scribe line 80 um*2)

Chip Thickness: 300 um(typ.)

Pad Location: Pad center

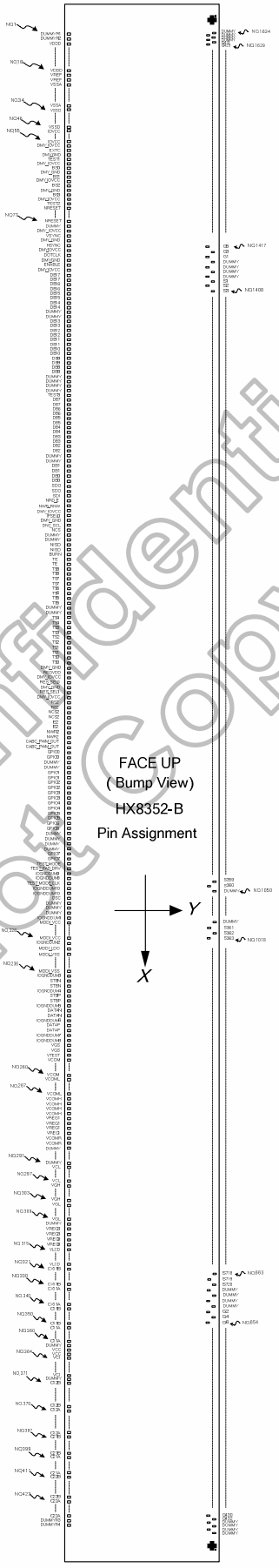
Coordinate Origin: Chip center

Au Bump Size
1. 24 um x 120um
Input / Output
(No. 1~No. 436)

2. 14 um x 106um
Staggered LCD output side
(No. 437~No. 658)

3. 14 um x 106um
Staggered LCD output side
(No. 659~No. 1412)

4. 14 um x 106um
Staggered LCD output side
(No. 1413~No. 1634)



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4.3 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMYR1	-8989	-208	61	BS0	-6589	-208	121	DB4	-4189	-208	181	E2	-1789	-208
2	DUMMYR2	-8949	-208	62	DMY_GND	-6549	-208	122	DB4	-4149	-208	182	E2	-1749	-208
3	VDDD	-8909	-208	63	BS1	-6509	-208	123	DB3	-4109	-208	183	NWR2	-1709	-208
4	VDDD	-8869	-208	64	DMY_IOVCC	-6469	-208	124	DB3	-4069	-208	184	NWR2	-1669	-208
5	VDDD	-8829	-208	65	BS2	-6429	-208	125	DB2	-4029	-208	185	CABC_PWM_OUT	-1629	-208
6	VDDD	-8789	-208	66	DMY_GND	-6389	-208	126	DB2	-3989	-208	186	CABC_PWM_OUT	-1589	-208
7	VDDD	-8749	-208	67	BS3	-6349	-208	127	DUMMY8	-3949	-208	187	GPIO0	-1549	-208
8	VDDD	-8709	-208	68	DMY_IOVCC	-6309	-208	128	DUMMY9	-3909	-208	188	GPIO0	-1509	-208
9	VDDD	-8669	-208	69	TEST2	-6269	-208	129	DB1	-3869	-208	189	DUMMY14	-1469	-208
10	VDDD	-8629	-208	70	NRESET	-6229	-208	130	DB1	-3829	-208	190	DUMMY15	-1429	-208
11	VDDD	-8589	-208	71	NRESET	-6189	-208	131	DB0	-3789	-208	191	GPIO1	-1389	-208
12	VDDD	-8549	-208	72	NRESET	-6149	-208	132	DB0	-3749	-208	192	GPIO1	-1349	-208
13	VDDD	-8509	-208	73	NRESET	-6109	-208	133	SDO	-3709	-208	193	GPIO2	-1309	-208
14	VDDD	-8469	-208	74	NRESET	-6069	-208	134	SDO	-3669	-208	194	GPIO2	-1269	-208
15	VDDD	-8429	-208	75	NRESET	-6029	-208	135	SDI	-3629	-208	195	GPIO3	-1229	-208
16	VDDD	-8389	-208	76	NRESET	-5989	-208	136	NRD_E	-3589	-208	196	GPIO3	-1189	-208
17	VDDD	-8349	-208	77	NRESET	-5949	-208	137	NWR_RNW	-3549	-208	197	GPIO4	-1149	-208
18	VDDD	-8309	-208	78	DUMMY1	-5909	-208	138	DMY_IOVCC	-3509	-208	198	GPIO4	-1109	-208
19	VREF	-8269	-208	79	DMY_IOVCC	-5869	-208	139	IFSEL0	-3469	-208	199	GPIO5	-1069	-208
20	VREF	-8229	-208	80	VSYNC	-5829	-208	140	DMY_GND	-3429	-208	200	GPIO5	-1029	-208
21	VSSA	-8189	-208	81	DMY_GND	-5789	-208	141	DNC_SCL	-3389	-208	201	GPIO6	-989	-208
22	VSSA	-8149	-208	82	HSYNC	-5749	-208	142	NCS	-3349	-208	202	GPIO6	-949	-208
23	VSSA	-8109	-208	83	DMY_IOVCC	-5709	-208	143	DUMMY10	-3309	-208	203	DUMMY16	-909	-208
24	VSSA	-8069	-208	84	DOTCLK	-5669	-208	144	DUMMY11	-3269	-208	204	DUMMY17	-869	-208
25	VSSA	-8029	-208	85	DMY_GND	-5629	-208	145	NISD	-3229	-208	205	DUMMY18	-829	-208
26	VSSA	-7989	-208	86	ENABLE	-5589	-208	146	NISD	-3189	-208	206	DUMMY19	-789	-208
27	VSSA	-7949	-208	87	DMY_IOVCC	-5549	-208	147	BURN	-3149	-208	207	GPIO7	-749	-208
28	VSSA	-7909	-208	88	DB17	-5509	-208	148	TE	-3109	-208	208	GPIO7	-709	-208
29	VSSA	-7869	-208	89	DB17	-5469	-208	149	TE	-3069	-208	209	TEST_MODE_DBV	-669	-208
30	VSSA	-7829	-208	90	DB16	-5429	-208	150	TS8	-3029	-208	210	TEST_PAD_DBV	-629	-208
31	VSSA	-7789	-208	91	DB16	-5389	-208	151	TS8	-2989	-208	211	IOGNDDUM_6	-589	-208
32	VSSA	-7749	-208	92	DB15	-5349	-208	152	TS7	-2949	-208	212	IOGNDDUM_5	-549	-208
33	VSSA	-7709	-208	93	DB15	-5309	-208	153	TS7	-2909	-208	213	TEST_MODE_CLK	-509	-208
34	VSSD	-7669	-208	94	DB14	-5269	-208	154	TS6	-2869	-208	214	IOGNDDUM_10	-469	-208
35	VSSD	-7629	-208	95	DB14	-5229	-208	155	TS6	-2829	-208	215	IOGNDDUM_10	-429	-208
36	VSSD	-7589	-208	96	DUMMY2	-5189	-208	156	TS5	-2789	-208	216	OSC	-389	-208
37	VSSD	-7549	-208	97	DUMMY3	-5149	-208	157	TS5	-2749	-208	217	DUMMY20	-349	-208
38	VSSD	-7509	-208	98	DB13	-5109	-208	158	DUMMY12	-2709	-208	218	DUMMY21	-309	-208
39	VSSD	-7469	-208	99	DB13	-5069	-208	159	DUMMY13	-2669	-208	219	DUMMY22	309	-208
40	VSSD	-7429	-208	100	DB12	-5029	-208	160	TS4	-2629	-208	220	IOGNDDUM_1	349	-208
41	VSSD	-7389	-208	101	DB12	-4989	-208	161	TS4	-2589	-208	221	MDDI_VCC	389	-208
42	VSSD	-7349	-208	102	DB11	-4949	-208	162	TS3	-2549	-208	222	MDDI_VCC	429	-208
43	VSSD	-7309	-208	103	DB11	-4909	-208	163	TS3	-2509	-208	223	MDDI_VCC	469	-208
44	VSSD	-7269	-208	104	DB10	-4869	-208	164	TS2	-2469	-208	224	MDDI_VCC	509	-208
45	VSSD	-7229	-208	105	DB10	-4829	-208	165	TS2	-2429	-208	225	MDDI_VCC	549	-208
46	VSSD	-7189	-208	106	DB9	-4789	-208	166	TS1	-2389	-208	226	MDDI_VCC	589	-208
47	IOVCC	-7149	-208	107	DB9	-4749	-208	167	TS1	-2349	-208	227	MDDI_VCC	629	-208
48	IOVCC	-7109	-208	108	DB8	-4709	-208	168	TS0	-2309	-208	228	MDDI_VCC	669	-208
49	IOVCC	-7069	-208	109	DB8	-4669	-208	169	TS0	-2269	-208	229	IOGNDDUM_2	709	-208
50	IOVCC	-7029	-208	110	DUMMY4	-4629	-208	170	DMY_GND	-2229	-208	230	MDDI_LDO	749	-208
51	IOVCC	-6989	-208	111	DUMMY5	-4589	-208	171	REGVDD	-2189	-208	231	MDDI_VSS	789	-208
52	IOVCC	-6949	-208	112	DUMMY6	-4549	-208	172	DMY_IOVCC	-2149	-208	232	MDDI_VSS	829	-208
53	IOVCC	-6909	-208	113	DUMMY7	-4509	-208	173	RES_SEL0	-2109	-208	233	MDDI_VSS	869	-208
54	IOVCC	-6869	-208	114	TEST3	-4469	-208	174	DMY_GND	-2069	-208	234	MDDI_VSS	909	-208
55	IOVCC	-6829	-208	115	DB7	-4429	-208	175	RES_SEL1	-2029	-208	235	MDDI_VSS	949	-208
56	DMY_IOVCC	-6789	-208	116	DB7	-4389	-208	176	DMY_IOVCC	-1989	-208	236	MDDI_VSS	989	-208
57	EXTC	-6749	-208	117	DB6	-4349	-208	177	RS2	-1949	-208	237	IOGNDDUM_3	1029	-208
58	DMY_GND	-6709	-208	118	DB6	-4309	-208	178	RS2	-1909	-208	238	STB-	1069	-208
59	TEST1	-6669	-208	119	DB5	-4269	-208	179	NCS2	-1869	-208	239	STB-	1109	-208
60	DMY_IOVCC	-6629	-208	120	DB5	-4229	-208	180	NCS2	-1829	-208	240	IOGNDDUM_4	1149	-208

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
241	STB+	1189	-208	301	VGH	3589	-208	361	DUMMY38	5989	-208	421	C22B	8389	-208
242	STB+	1229	-208	302	VGH	3629	-208	362	VCC	6029	-208	422	C22B	8429	-208
243	IOGNDDUM5	1269	-208	303	VGH	3669	-208	363	VCC	6069	-208	423	C22A	8469	-208
244	DATA-	1309	-208	304	VGL	3709	-208	364	VCI	6109	-208	424	C22A	8509	-208
245	DATA-	1349	-208	305	VGL	3749	-208	365	VCI	6149	-208	425	C22A	8549	-208
246	IOGNDDUM6	1389	-208	306	VGL	3789	-208	366	VCI	6189	-208	426	C22A	8589	-208
247	DATA+	1429	-208	307	VGL	3829	-208	367	VCI	6229	-208	427	C22A	8629	-208
248	DATA+	1469	-208	308	VGL	3869	-208	368	VCI	6269	-208	428	C22A	8669	-208
249	IOGNDDUM7	1509	-208	309	VGL	3909	-208	369	VCI	6309	-208	429	C22A	8709	-208
250	IOGNDDUM8	1549	-208	310	DUMMY37	3949	-208	370	DUMMY39	6349	-208	430	C22A	8749	-208
251	VGS	1589	-208	311	VREG3	3989	-208	371	C12B	6389	-208	431	C22A	8789	-208
252	VGS	1629	-208	312	VREG3	4029	-208	372	C12B	6429	-208	432	C22A	8829	-208
253	VTEST	1669	-208	313	VREG3	4069	-208	373	C12B	6469	-208	433	C22A	8869	-208
254	VCOM	1709	-208	314	VREG3	4109	-208	374	C12B	6509	-208	434	C22A	8909	-208
255	VCOM	1749	-208	315	VLCD	4149	-208	375	C12B	6549	-208	435	DUMMYR3	8949	-208
256	VCOM	1789	-208	316	VLCD	4189	-208	376	C12B	6589	-208	436	DUMMYR4	8989	-208
257	VCOM	1829	-208	317	VLCD	4229	-208	377	C12B	6629	-208	437	DUMMY40	9007	250
258	VCOM	1869	-208	318	VLCD	4269	-208	378	C12B	6669	-208	438	DUMMY41	8991	128
259	VCOM	1909	-208	319	VLCD	4309	-208	379	C12A	6709	-208	439	DUMMY42	8975	250
260	VCOM	1949	-208	320	VLCD	4349	-208	380	C12A	6749	-208	440	DUMMY43	8959	128
261	VCOML	1989	-208	321	CX11B	4389	-208	381	C12A	6789	-208	441	G432	8943	250
262	VCOML	2029	-208	322	CX11B	4429	-208	382	C12A	6829	-208	442	G430	8927	128
263	VCOML	2069	-208	323	CX11B	4469	-208	383	C12A	6869	-208	443	G428	8911	250
264	VCOML	2109	-208	324	CX11B	4509	-208	384	C12A	6909	-208	444	G426	8895	128
265	VCOML	2149	-208	325	CX11B	4549	-208	385	C12A	6949	-208	445	G424	8879	250
266	VCOML	2189	-208	326	CX11B	4589	-208	386	C12A	6989	-208	446	G422	8863	128
267	VCOML	2229	-208	327	CX11B	4629	-208	387	C21B	7029	-208	447	G420	8847	250
268	VCOMH	2269	-208	328	CX11B	4669	-208	388	C21B	7069	-208	448	G418	8831	128
269	VCOMH	2309	-208	329	CX11B	4709	-208	389	C21B	7109	-208	449	G416	8815	250
270	VCOMH	2349	-208	330	CX11B	4749	-208	390	C21B	7149	-208	450	G414	8799	128
271	VCOMH	2389	-208	331	CX11A	4789	-208	391	C21B	7189	-208	451	G412	8783	250
272	VREG1	2429	-208	332	CX11A	4829	-208	392	C21B	7229	-208	452	G410	8767	128
273	VREG1	2469	-208	333	CX11A	4869	-208	393	C21B	7269	-208	453	G408	8751	250
274	VREG1	2509	-208	334	CX11A	4909	-208	394	C21B	7309	-208	454	G406	8735	128
275	VREG1	2549	-208	335	CX11A	4949	-208	395	C21B	7349	-208	455	G404	8719	250
276	VCOMR	2589	-208	336	CX11A	4989	-208	396	C21B	7389	-208	456	G402	8703	128
277	VCOMR	2629	-208	337	CX11A	5029	-208	397	C21B	7429	-208	457	G400	8687	250
278	DUMMY23	2669	-208	338	CX11A	5069	-208	398	C21B	7469	-208	458	G398	8671	128
279	DUMMY24	2709	-208	339	CX11A	5109	-208	399	C21A	7509	-208	459	G396	8655	250
280	DUMMY25	2749	-208	340	CX11A	5149	-208	400	C21A	7549	-208	460	G394	8639	128
281	DUMMY26	2789	-208	341	C11B	5189	-208	401	C21A	7589	-208	461	G392	8623	250
282	DUMMY27	2829	-208	342	C11B	5229	-208	402	C21A	7629	-208	462	G390	8607	128
283	DUMMY28	2869	-208	343	C11B	5269	-208	403	C21A	7669	-208	463	G388	8591	250
284	DUMMY29	2909	-208	344	C11B	5309	-208	404	C21A	7709	-208	464	G386	8575	128
285	DUMMY30	2949	-208	345	C11B	5349	-208	405	C21A	7749	-208	465	G384	8559	250
286	DUMMY31	2989	-208	346	C11B	5389	-208	406	C21A	7789	-208	466	G382	8543	128
287	DUMMY32	3029	-208	347	C11B	5429	-208	407	C21A	7829	-208	467	G380	8527	250
288	DUMMY33	3069	-208	348	C11B	5469	-208	408	C21A	7869	-208	468	G378	8511	128
289	DUMMY34	3109	-208	349	C11B	5509	-208	409	C21A	7909	-208	469	G376	8495	250
290	DUMMY35	3149	-208	350	C11B	5549	-208	410	C21A	7949	-208	470	G374	8479	128
291	DUMMY36	3189	-208	351	C11A	5589	-208	411	C22B	7989	-208	471	G372	8463	250
292	VCL	3229	-208	352	C11A	5629	-208	412	C22B	8029	-208	472	G370	8447	128
293	VCL	3269	-208	353	C11A	5669	-208	413	C22B	8069	-208	473	G368	8431	250
294	VCL	3309	-208	354	C11A	5709	-208	414	C22B	8109	-208	474	G366	8415	128
295	VCL	3349	-208	355	C11A	5749	-208	415	C22B	8149	-208	475	G364	8399	250
296	VCL	3389	-208	356	C11A	5789	-208	416	C22B	8189	-208	476	G362	8383	128
297	VCL	3429	-208	357	C11A	5829	-208	417	C22B	8229	-208	477	G360	8367	250
298	VGH	3469	-208	358	C11A	5869	-208	418	C22B	8269	-208	478	G358	8351	128
299	VGH	3509	-208	359	C11A	5909	-208	419	C22B	8309	-208	479	G356	8335	250
300	VGH	3549	-208	360	C11A	5949	-208	420	C22B	8349	-208	480	G354	8319	128

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
481	G352	8303	250	541	G232	7343	250	601	G112	6383	250	661	S720	5427	250
482	G350	8287	128	542	G230	7327	128	602	G110	6367	128	662	S719	5413	128
483	G348	8271	250	543	G228	7311	250	603	G108	6351	250	663	S718	5399	250
484	G346	8255	128	544	G226	7295	128	604	G106	6335	128	664	S717	5385	128
485	G344	8239	250	545	G224	7279	250	605	G104	6319	250	665	S716	5371	250
486	G342	8223	128	546	G222	7263	128	606	G102	6303	128	666	S715	5357	128
487	G340	8207	250	547	G220	7247	250	607	G100	6287	250	667	S714	5343	250
488	G338	8191	128	548	G218	7231	128	608	G98	6271	128	668	S713	5329	128
489	G336	8175	250	549	G216	7215	250	609	G96	6255	250	669	S712	5315	250
490	G334	8159	128	550	G214	7199	128	610	G94	6239	128	670	S711	5301	128
491	G332	8143	250	551	G212	7183	250	611	G92	6223	250	671	S710	5287	250
492	G330	8127	128	552	G210	7167	128	612	G90	6207	128	672	S709	5273	128
493	G328	8111	250	553	G208	7151	250	613	G88	6191	250	673	S708	5259	250
494	G326	8095	128	554	G206	7135	128	614	G86	6175	128	674	S707	5245	128
495	G324	8079	250	555	G204	7119	250	615	G84	6159	250	675	S706	5231	250
496	G322	8063	128	556	G202	7103	128	616	G82	6143	128	676	S705	5217	128
497	G320	8047	250	557	G200	7087	250	617	G80	6127	250	677	S704	5203	250
498	G318	8031	128	558	G198	7071	128	618	G78	6111	128	678	S703	5189	128
499	G316	8015	250	559	G196	7055	250	619	G76	6095	250	679	S702	5175	250
500	G314	7999	128	560	G194	7039	128	620	G74	6079	128	680	S701	5161	128
501	G312	7983	250	561	G192	7023	250	621	G72	6063	250	681	S700	5147	250
502	G310	7967	128	562	G190	7007	128	622	G70	6047	128	682	S699	5133	128
503	G308	7951	250	563	G188	6991	250	623	G68	6031	250	683	S698	5119	250
504	G306	7935	128	564	G186	6975	128	624	G66	6015	128	684	S697	5105	128
505	G304	7919	250	565	G184	6959	250	625	G64	5999	250	685	S696	5091	250
506	G302	7903	128	566	G182	6943	128	626	G62	5983	128	686	S695	5077	128
507	G300	7887	250	567	G180	6927	250	627	G60	5967	250	687	S694	5063	250
508	G298	7871	128	568	G178	6911	128	628	G58	5951	128	688	S693	5049	128
509	G296	7855	250	569	G176	6895	250	629	G56	5935	250	689	S692	5035	250
510	G294	7839	128	570	G174	6879	128	630	G54	5919	128	690	S691	5021	128
511	G292	7823	250	571	G172	6863	250	631	G52	5903	250	691	S690	5007	250
512	G290	7807	128	572	G170	6847	128	632	G50	5887	128	692	S689	4993	128
513	G288	7791	250	573	G168	6831	250	633	G48	5871	250	693	S688	4979	250
514	G286	7775	128	574	G166	6815	128	634	G46	5855	128	694	S687	4965	128
515	G284	7759	250	575	G164	6799	250	635	G44	5839	250	695	S686	4951	250
516	G282	7743	128	576	G162	6783	128	636	G42	5823	128	696	S685	4937	128
517	G280	7727	250	577	G160	6767	250	637	G40	5807	250	697	S684	4923	250
518	G278	7711	128	578	G158	6751	128	638	G38	5791	128	698	S683	4909	128
519	G276	7695	250	579	G156	6735	250	639	G36	5775	250	699	S682	4895	250
520	G274	7679	128	580	G154	6719	128	640	G34	5759	128	700	S681	4881	128
521	G272	7663	250	581	G152	6703	250	641	G32	5743	250	701	S680	4867	250
522	G270	7647	128	582	G150	6687	128	642	G30	5727	128	702	S679	4853	128
523	G268	7631	250	583	G148	6671	250	643	G28	5711	250	703	S678	4839	250
524	G266	7615	128	584	G146	6655	128	644	G26	5695	128	704	S677	4825	128
525	G264	7599	250	585	G144	6639	250	645	G24	5679	250	705	S676	4811	250
526	G262	7583	128	586	G142	6623	128	646	G22	5663	128	706	S675	4797	128
527	G260	7567	250	587	G140	6607	250	647	G20	5647	250	707	S674	4783	250
528	G258	7551	128	588	G138	6591	128	648	G18	5631	128	708	S673	4769	128
529	G256	7535	250	589	G136	6575	250	649	G16	5615	250	709	S672	4755	250
530	G254	7519	128	590	G134	6559	128	650	G14	5599	128	710	S671	4741	128
531	G252	7503	250	591	G132	6543	250	651	G12	5583	250	711	S670	4727	250
532	G250	7487	128	592	G130	6527	128	652	G10	5567	128	712	S669	4713	128
533	G248	7471	250	593	G128	6511	250	653	G8	5551	250	713	S668	4699	250
534	G246	7455	128	594	G126	6495	128	654	G6	5535	128	714	S667	4685	128
535	G244	7439	250	595	G124	6479	250	655	G4	5519	250	715	S666	4671	250
536	G242	7423	128	596	G122	6463	128	656	G2	5503	128	716	S665	4657	128
537	G240	7407	250	597	G120	6447	250	657	DUMMY44	5487	250	717	S664	4643	250
538	G238	7391	128	598	G118	6431	128	658	DUMMY45	5471	128	718	S663	4629	128
539	G236	7375	250	599	G116	6415	250	659	DUMMY46	5455	250	719	S662	4615	250
540	G234	7359	128	600	G114	6399	128	660	DUMMY47	5441	128	720	S661	4601	128

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
721	S660	4587	250	781	S600	3747	250	841	S540	2907	250	901	S480	2067	250
722	S659	4573	128	782	S599	3733	128	842	S539	2893	128	902	S479	2053	128
723	S658	4559	250	783	S598	3719	250	843	S538	2879	250	903	S478	2039	250
724	S657	4545	128	784	S597	3705	128	844	S537	2865	128	904	S477	2025	128
725	S656	4531	250	785	S596	3691	250	845	S536	2851	250	905	S476	2011	250
726	S655	4517	128	786	S595	3677	128	846	S535	2837	128	906	S475	1997	128
727	S654	4503	250	787	S594	3663	250	847	S534	2823	250	907	S474	1983	250
728	S653	4489	128	788	S593	3649	128	848	S533	2809	128	908	S473	1969	128
729	S652	4475	250	789	S592	3635	250	849	S532	2795	250	909	S472	1955	250
730	S651	4461	128	790	S591	3621	128	850	S531	2781	128	910	S471	1941	128
731	S650	4447	250	791	S590	3607	250	851	S530	2767	250	911	S470	1927	250
732	S649	4433	128	792	S589	3593	128	852	S529	2753	128	912	S469	1913	128
733	S648	4419	250	793	S588	3579	250	853	S528	2739	250	913	S468	1899	250
734	S647	4405	128	794	S587	3565	128	854	S527	2725	128	914	S467	1885	128
735	S646	4391	250	795	S586	3551	250	855	S526	2711	250	915	S466	1871	250
736	S645	4377	128	796	S585	3537	128	856	S525	2697	128	916	S465	1857	128
737	S644	4363	250	797	S584	3523	250	857	S524	2683	250	917	S464	1843	250
738	S643	4349	128	798	S583	3509	128	858	S523	2669	128	918	S463	1829	128
739	S642	4335	250	799	S582	3495	250	859	S522	2655	250	919	S462	1815	250
740	S641	4321	128	800	S581	3481	128	860	S521	2641	128	920	S461	1801	128
741	S640	4307	250	801	S580	3467	250	861	S520	2627	250	921	S460	1787	250
742	S639	4293	128	802	S579	3453	128	862	S519	2613	128	922	S459	1773	128
743	S638	4279	250	803	S578	3439	250	863	S518	2599	250	923	S458	1759	250
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745	S636	4251	250	805	S576	3411	250	865	S516	2571	250	925	S456	1731	250
746	S635	4237	128	806	S575	3397	128	866	S515	2557	128	926	S455	1717	128
747	S634	4223	250	807	S574	3383	250	867	S514	2543	250	927	S454	1703	250
748	S633	4209	128	808	S573	3369	128	868	S513	2529	128	928	S453	1689	128
749	S632	4195	250	809	S572	3355	250	869	S512	2515	250	929	S452	1675	250
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751	S630	4167	250	811	S570	3327	250	871	S510	2487	250	931	S450	1647	250
752	S629	4153	128	812	S569	3313	128	872	S509	2473	128	932	S449	1633	128
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755	S626	4111	250	815	S566	3271	250	875	S506	2431	250	935	S446	1591	250
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757	S624	4083	250	817	S564	3243	250	877	S504	2403	250	937	S444	1563	250
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759	S622	4055	250	819	S562	3215	250	879	S502	2375	250	939	S442	1535	250
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761	S620	4027	250	821	S560	3187	250	881	S500	2347	250	941	S440	1507	250
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763	S618	3999	250	823	S558	3159	250	883	S498	2319	250	943	S438	1479	250
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765	S616	3971	250	825	S556	3131	250	885	S496	2291	250	945	S436	1451	250
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769	S612	3915	250	829	S552	3075	250	889	S492	2235	250	949	S432	1395	250
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771	S610	3887	250	831	S550	3047	250	891	S490	2207	250	951	S430	1367	250
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773	S608	3859	250	833	S548	3019	250	893	S488	2179	250	953	S428	1339	250
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775	S606	3831	250	835	S546	2991	250	895	S486	2151	250	955	S426	1311	250
776	S605	3817	128	836	S545	2977	128	896	S485	2137	128	956	S425	1297	128
777	S604	3803	250	837	S544	2963	250	897	S484	2123	250	957	S424	1283	250
778	S603	3789	128	838	S543	2949	128	898	S483	2109	128	958	S423	1269	128
779	S602	3775	250	839	S542	2935	250	899	S482	2095	250	959	S422	1255	250
780	S601	3761	128	840	S541	2921	128	900	S481	2081	128	960	S421	1241	128

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
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962	S419	1213	128	1022	DUMMY49	373	128	1082	S329	-835	250	1142	S269	-1675	250
963	S418	1199	250	1023	DUMMY50	359	250	1083	S328	-849	128	1143	S268	-1689	128
964	S417	1185	128	1024	DUMMY51	331	250	1084	S327	-863	250	1144	S267	-1703	250
965	S416	1171	250	1025	DUMMY52	303	250	1085	S326	-877	128	1145	S266	-1717	128
966	S415	1157	128	1026	DUMMY53	275	250	1086	S325	-891	250	1146	S265	-1731	250
967	S414	1143	250	1027	DUMMY54	247	250	1087	S324	-905	128	1147	S264	-1745	128
968	S413	1129	128	1028	DUMMY55	219	250	1088	S323	-919	250	1148	S263	-1759	250
969	S412	1115	250	1029	DUMMY56	191	250	1089	S322	-933	128	1149	S262	-1773	128
970	S411	1101	128	1030	DUMMY57	163	250	1090	S321	-947	250	1150	S261	-1787	250
971	S410	1087	250	1031	DUMMY58	135	250	1091	S320	-961	128	1151	S260	-1801	128
972	S409	1073	128	1032	DUMMY59	107	250	1092	S319	-975	250	1152	S259	-1815	250
973	S408	1059	250	1033	DUMMY60	79	250	1093	S318	-989	128	1153	S258	-1829	128
974	S407	1045	128	1034	DUMMY61	51	250	1094	S317	-1003	250	1154	S257	-1843	250
975	S406	1031	250	1035	DUMMY62	23	250	1095	S316	-1017	128	1155	S256	-1857	128
976	S405	1017	128	1036	DUMMY63	-23	250	1096	S315	-1031	250	1156	S255	-1871	250
977	S404	1003	250	1037	DUMMY64	-51	250	1097	S314	-1045	128	1157	S254	-1885	128
978	S403	989	128	1038	DUMMY65	-79	250	1098	S313	-1059	250	1158	S253	-1899	250
979	S402	975	250	1039	DUMMY66	-107	250	1099	S312	-1073	128	1159	S252	-1913	128
980	S401	961	128	1040	DUMMY67	-135	250	1100	S311	-1087	250	1160	S251	-1927	250
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982	S399	933	128	1042	DUMMY69	-191	250	1102	S309	-1115	250	1162	S249	-1955	250
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984	S397	905	128	1044	DUMMY71	-247	250	1104	S307	-1143	250	1164	S247	-1983	250
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1000	S381	681	128	1060	S351	-527	250	1120	S291	-1367	250	1180	S231	-2207	250
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1014	S367	485	128	1074	S337	-723	250	1134	S277	-1563	250	1194	S217	-2403	250
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1203	S208	-2529	128	1263	S148	-3369	128	1323	S88	-4209	128	1383	S28	-5049	128
1204	S207	-2543	250	1264	S147	-3383	250	1324	S87	-4223	250	1384	S27	-5063	250
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1483	G137	-6591	128
1484	G139	-6607	250
1485	G141	-6623	128
1486	G143	-6639	250
1487	G145	-6655	128
1488	G147	-6671	250
1489	G149	-6687	128
1490	G151	-6703	250
1491	G153	-6719	128
1492	G155	-6735	250
1493	G157	-6751	128
1494	G159	-6767	250
1495	G161	-6783	128
1496	G163	-6799	250
1497	G165	-6815	128
1498	G167	-6831	250
1499	G169	-6847	128
1500	G171	-6863	250

No.	Name	X	Y
1501	G173	-6879	128
1502	G175	-6895	250
1503	G177	-6911	128
1504	G179	-6927	250
1505	G181	-6943	128
1506	G183	-6959	250
1507	G185	-6975	128
1508	G187	-6991	250
1509	G189	-7007	128
1510	G191	-7023	250
1511	G193	-7039	128
1512	G195	-7055	250
1513	G197	-7071	128
1514	G199	-7087	250
1515	G201	-7103	128
1516	G203	-7119	250
1517	G205	-7135	128
1518	G207	-7151	250
1519	G209	-7167	128
1520	G211	-7183	250
1521	G213	-7199	128
1522	G215	-7215	250
1523	G217	-7231	128
1524	G219	-7247	250
1525	G221	-7263	128
1526	G223	-7279	250
1527	G225	-7295	128
1528	G227	-7311	250
1529	G229	-7327	128
1530	G231	-7343	250
1531	G233	-7359	128
1532	G235	-7375	250
1533	G237	-7391	128
1534	G239	-7407	250
1535	G241	-7423	128
1536	G243	-7439	250
1537	G245	-7455	128
1538	G247	-7471	250
1539	G249	-7487	128
1540	G251	-7503	250
1541	G253	-7519	128
1542	G255	-7535	250
1543	G257	-7551	128
1544	G259	-7567	250
1545	G261	-7583	128
1546	G263	-7599	250
1547	G265	-7615	128
1548	G267	-7631	250
1549	G269	-7647	128
1550	G271	-7663	250
1551	G273	-7679	128
1552	G275	-7695	250
1553	G277	-7711	128
1554	G279	-7727	250
1555	G281	-7743	128
1556	G283	-7759	250
1557	G285	-7775	128
1558	G287	-7791	250
1559	G289	-7807	128
1560	G291	-7823	250

No.	Name	X	Y
1561	G293	-7839	128
1562	G295	-7855	250
1563	G297	-7871	128
1564	G299	-7887	250
1565	G301	-7903	128
1566	G303	-7919	250
1567	G305	-7935	128
1568	G307	-7951	250
1669	G309	-7967	128
1570	G311	-7983	250
1571	G313	-7999	128
1572	G315	-8015	250
1573	G317	-8031	128
1574	G319	-8047	250
1575	G321	-8063	128
1576	G323	-8079	250
1577	G325	-8095	128
1578	G327	-8111	250
1579	G329	-8127	128
1580	G331	-8143	250
1581	G333	-8159	128
1582	G335	-8175	250
1583	G337	-8191	128
1584	G339	-8207	250
1585	G341	-8223	128
1586	G343	-8239	250
1587	G345	-8255	128
1588	G347	-8271	250
1589	G349	-8287	128
1590	G351	-8303	250
1591	G353	-8319	128
1592	G355	-8335	250
1593	G357	-8351	128
1594	G359	-8367	250
1595	G361	-8383	128
1596	G363	-8399	250
1597	G365	-8415	128
1598	G367	-8431	250
1599	G369	-8447	128
1600	G371	-8463	250
1601	G373	-8479	128
1602	G375	-8495	250
1603	G377	-8511	128
1604	G379	-8527	250
1605	G381	-8543	128
1606	G383	-8559	250
1607	G385	-8575	128
1608	G387	-8591	250
1609	G389	-8607	128
1610	G391	-8623	250
1611	G393	-8639	128
1612	G395	-8655	250
1613	G397	-8671	128
1614	G399	-8687	250
1615	G401	-8703	128
1616	G403	-8719	250
1617	G405	-8735	128
1618	G407	-8751	250
1619	G409	-8767	128
1620	G411	-8783	250

No.	Name	X	Y
1621	G413	-8799	128
1622	G415	-8815	250
1623	G417	-8831	128
1624	G419	-8847	250
1625	G421	-8863	128
1626	G423	-8879	250
1627	G425	-8895	128
1628	G427	-8911	250
1629	G429	-8927	128
1630	G431	-8943	250
1631	DUMMY82	-8959	128
1632	DUMMY83	-8975	250
1633	DUMMY84	-8991	128
1634	DUMMY85	-9007	250

Alignment mark	X	Y
A1	-9200	227
A2	9200	227

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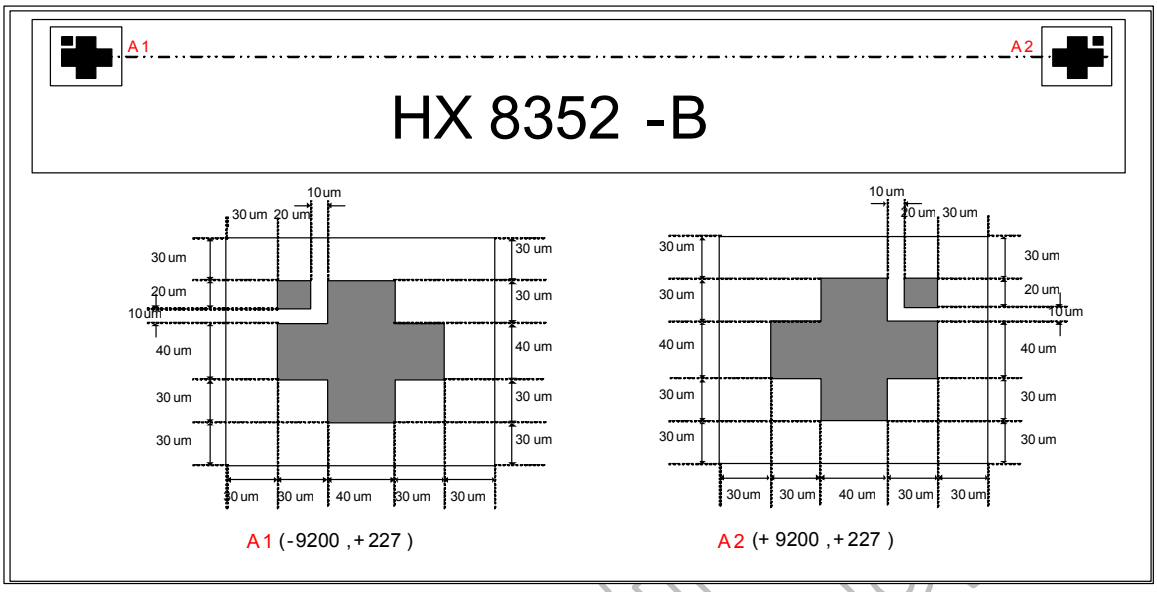
4.4 Alignment mark

HX8352-B Alignment mark

-+	A1	-9200	227
++	A2	9200	227



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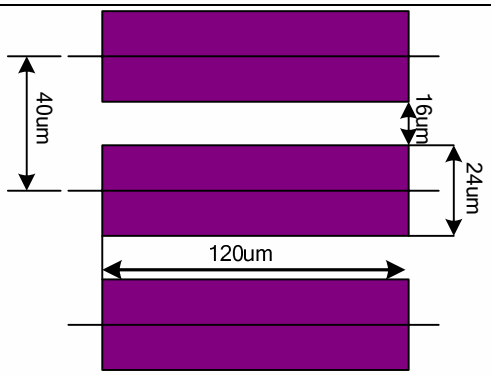
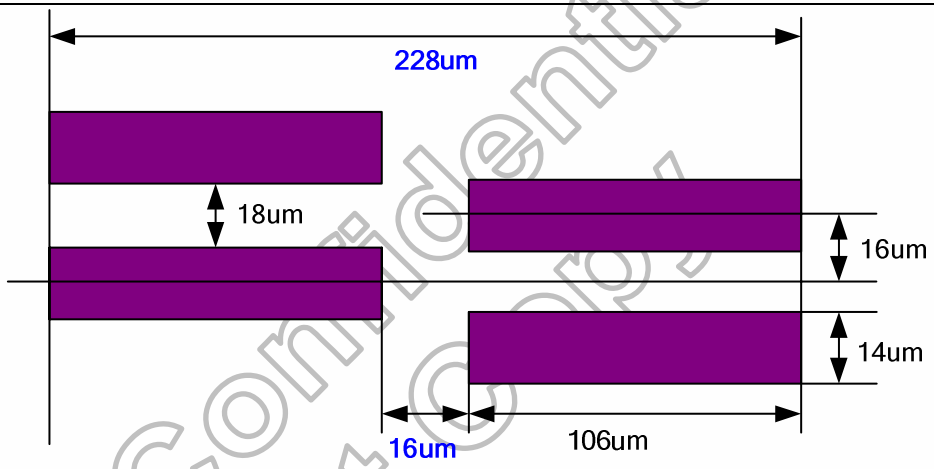
4.5 Bump size

Input PAD



NO.1~NO.436

Output PAD



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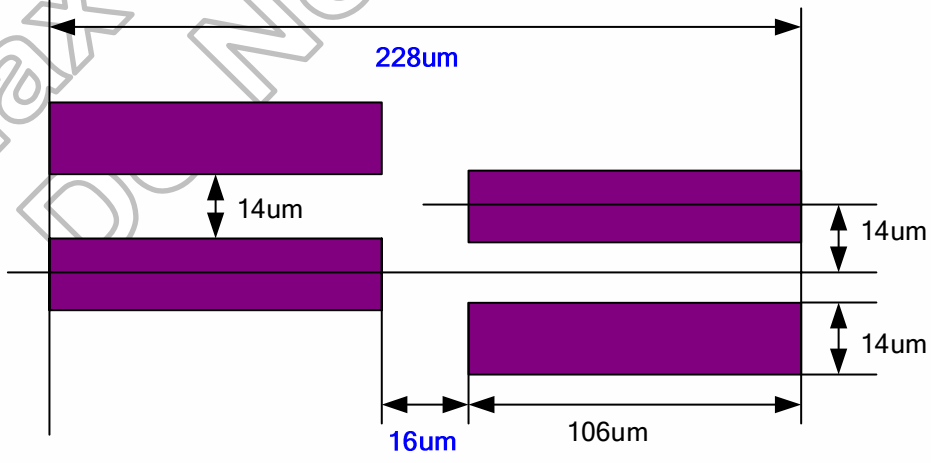

NO.659~NO.1412

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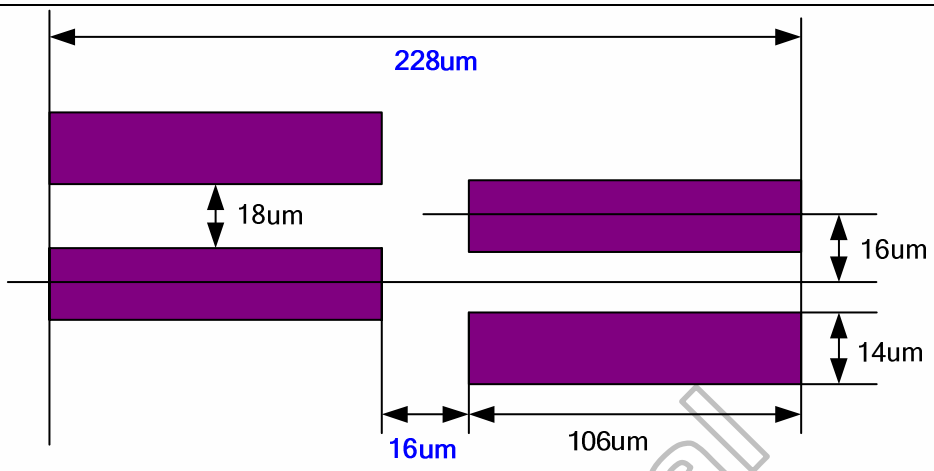
Output PAD	

NO.1413~NO.1634

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5. Interface

The HX8352-B01 supports two-type interface: Parallel type I and Parallel type II.

The HX8352-B01 has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8352-B01 shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

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5.1 System interface circuit

The system interface circuit in HX8352-B01 supports, 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and 4-/3-wire serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8352-B01 become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 5.1.

IFSEL0	BS3	BS2	BS1	BS0	Interface	NWR_RNW	DNC_SCL	Data Bus use	
								Register/ Content	GRAM
0	0	0	0	0	8080 MCU 18-bits Parallel type II	NWR	DNC	DB8-DB1	DB17-DB0: 18-bits Data
	0	0	1	0	8080 MCU 16-bits Parallel type II	NWR	DNC	DB8-DB1	DB17-DB10, DB8-DB1: 16-bit data
	0	0	0	1	8080 MCU 9-bits Parallel type II	NWR	DNC	DB17-DB10	DB17-DB9: 9-bits Data
	0	0	1	1	8080 MCU 8-bits Parallel type II	NWR	DNC	DB17-DB10	DB17-DB10: 8-bits Data
	0	1	0	ID	3-wire Serial interface	x	SCL	SDI, SDO	
	0	1	1	0	4-wire Serial interface	DNC(1)	SCL	SDI, SDO	
	0	1	1	1	SPI(2), MDDI I/F	x	SCL	SDI, SDO	
1	0	0	0	0	8080 MCU 16-bits Paralle type I	NWR	DNC	DB7-DB0	DB15-DB0: 16-bit data
	0	0	0	1					
	0	0	1	0	8080 MCU 18-bits Parallel type I	NWR	DNC	DB7-DB0	DB17-DB0: 18-bits Data
	0	0	1	1	8080 MCU 8-bits Parallel type I	NWR	DNC	DB7-DB0	DB7-DB0: 8-bits Data
	0	1	0	0					
	1	0	0	0	8080 MCU 9-bits Parallel type I	NWR	DNC	DB7-DB0	DB8-DB0: 9-bits Data
	X	1	1	ID	3-W serial interface	X	SCL	SDI, SDO	DB17-DB0: 18-bits Dat
	X	1	0	1	SPI(2), MDDI I/F	X	X	MDDI, SDI, SDO	MDDI

Note: (1) Under IFSEL0=0, BS(3-0)=0110, the NWR_RNW will be DNC used.
(2) Under IFSEL0=0, BS(3-0)=0111, the SPI-3W(ID=1) just can accseee CMD, when MDDI into hibernation mode.
Under IFSEL0=1, BS(3-0)=X101, the SPI-3W(ID=1) just can accseee CMD, when MDDI into hibernation mode.

Table 5.1 Input bus format selection of system interface circuit

It has an Index Register (IR) in HX8352-B01 to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

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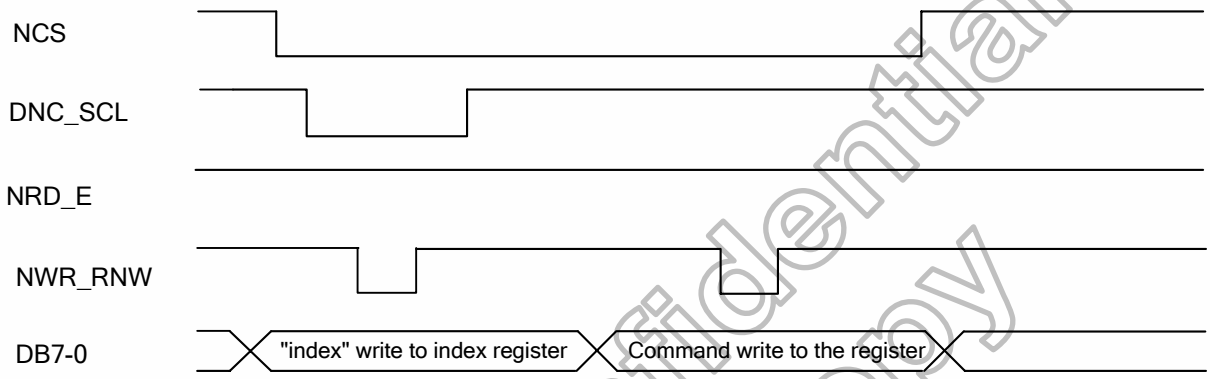
5.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed in Table 5.2.

Operations	NWR_RNW	NRD_E	DNC_SCL
Writes Indexes into IR	0	1	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5.2 Data pin function for I80 series CPU

Write to the register



Read the register

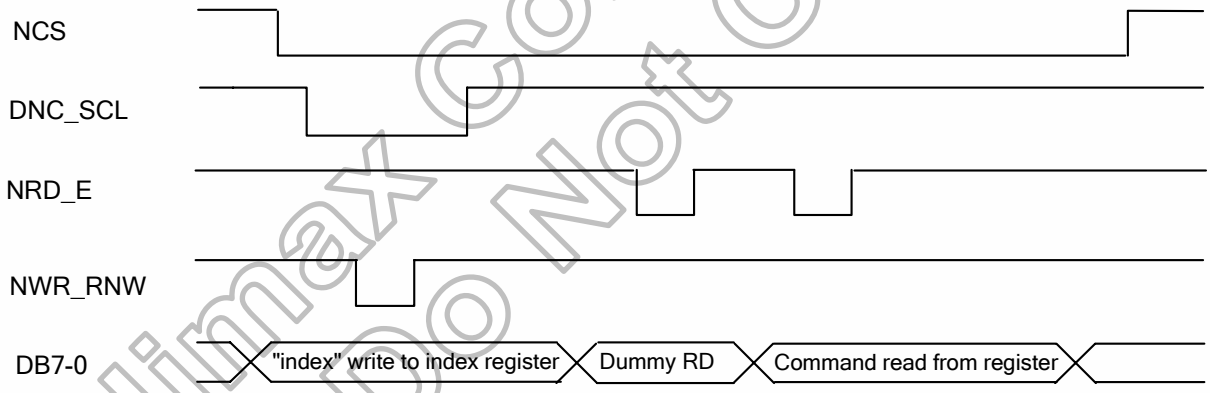


Figure 5.1 Register read/write timing in parallel bus system interface (for I80 series MPU)

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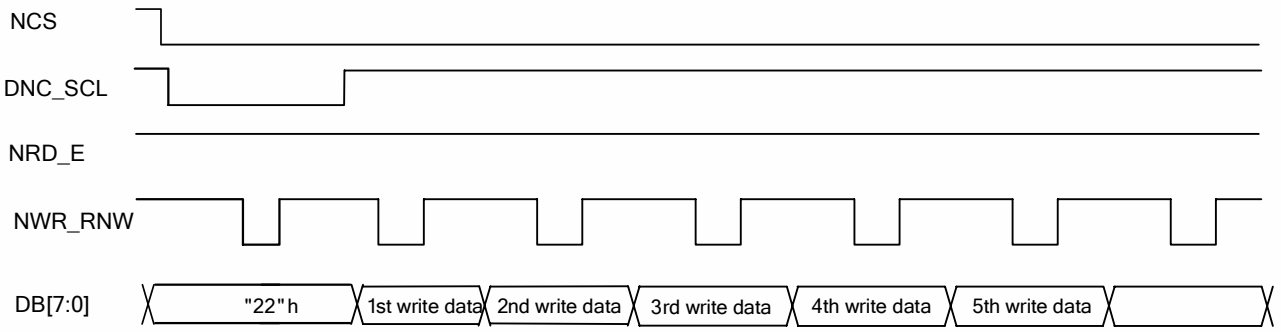
Write to the graphic RAM



Read the graphic RAM

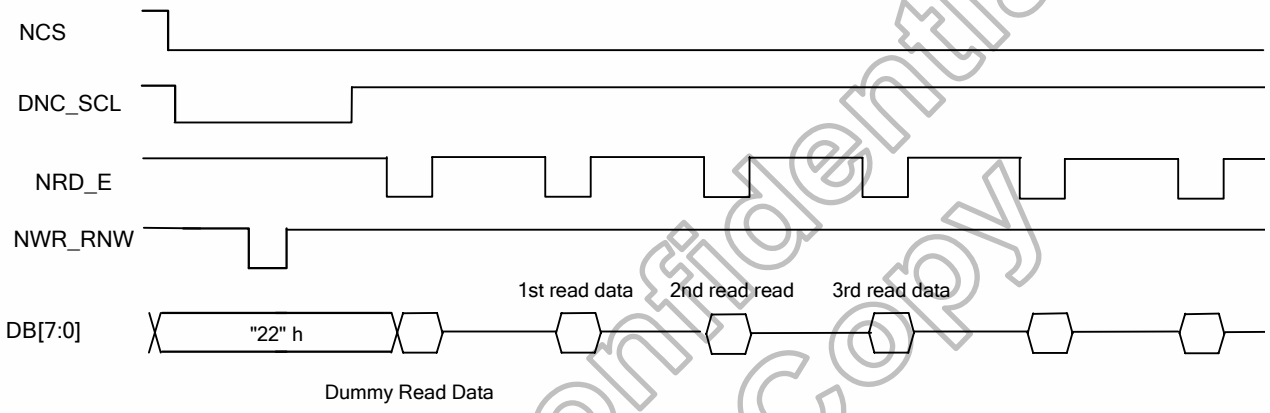


Figure 5.2 GRAM read/write timing in parallel bus system interface (for I80 series MPU)

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5.1.2 MCU data color coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface typeI (IFSEL0=1, BS3,BS2,BS1,BS0="0011" or "0100")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixel/ 3-byte)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	RR4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-byte)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	RR5	RR4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.3 8-bit parallel interface type I GRAM write table

- Parallel 16-Bits Bus Interface typeI (IFSEL0=1, BS3,BS2,BS1,BS0="0000 or "0001"")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h			x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
04h			x	x	x	x	x	x	x	x	X	x	x	x	x	x	RR5	RR4	262K-Color (2+16)
			R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	
05h	x	x	RR4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
07h	x	x	RR5	RR4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
	x	x	x	x	x	x	x	x	x	x	X	x	x	x	x	x	B1	B0	

Table 5.4 16-bit parallel interface type I GRAM write table

- Parallel 9-Bits Bus Interface typeI (IFSEL=0, BS3,BS2,BS1,BS0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	x	x	x	x	x	x	x	x	x	RR5	RR4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.5 9-bit parallel interface type I GRAM write table

- Parallel 18-Bits Bus Interface typeI (IFSEL0=1, BS3,BS2,BS1,BS0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	RR5	RR4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 5.6 18-bit parallel interface type I GRAM write table

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- Parallel 8-Bits Bus Interface typeII (IFSEL0=0, BS3,BS2,BS1,BS0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixel/ 3-bytes)
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	RR4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixel/ 2-bytes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	RR5	RR4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.7 8-bit parallel interface type II GRAM write table

- Parallel 16-Bits Bus Interface typeII (IFSEL0=0, BS3,BS2,BS1,BS0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
									x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4K-Color
04h	x	x	x	x	x	X	x	x	x	x	x	x	x	x	x	RR5	RR4	x	262K-Color (2+16)
	R3	R2	R1	R0	G5	G4	G3	G2	x	G1	G0	B5	B4	B3	B2	B1	B0	x	
05h	RR4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	RR5	RR4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixel/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	RR5	RR4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	
07h	RR5	RR4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (16+2)
	x	x	x	x	x	X	x	x	x	x	x	x	x	x	x	B1	B0	x	

Table 5.8 16-bit parallel interface type II GRAM write table

- Parallel 9-Bits Bus Interface typeII (IFSEL0=0, BS3,BS2,BS1,BS0="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	1	1	0	0	x	X	x	x	x	x	x	x	x	x	**22H**
17H	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	RR5	RR4	R3	R2	R1	R0	G5	G4	G3	X	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	X	x	x	x	x	x	x	x	x	

Table 5.9 9-bit parallel interface set type II GRAM write table

- Parallel 18-Bits Bus Interface typeII (IFSEL0=0, BS3,BS2,BS1,BS0="0000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	X	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	RR5	RR4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 5.10 18-bit parallel interface type II GRAM write set table

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18-bit parallel bus system interface

The I80-system 18-bit parallel bus interface **type I** can be used by setting external pins “IFSEL0=1” and “BS3, BS2, BS1, BS0” pins to “0010”. And the I80-system 18-bit parallel bus interface **type II** can be used by setting “IFSEL0=0“ and “BS3, BS2, BS1, BS0” pins to “0000”. Figure 5.3 is the example of interface with I80 microcomputer system interface.

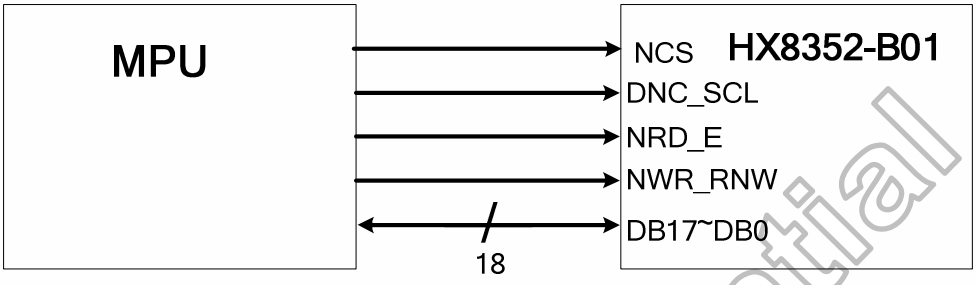

Figure 5.3 Example of I80- system 18-bit parallel bus interface

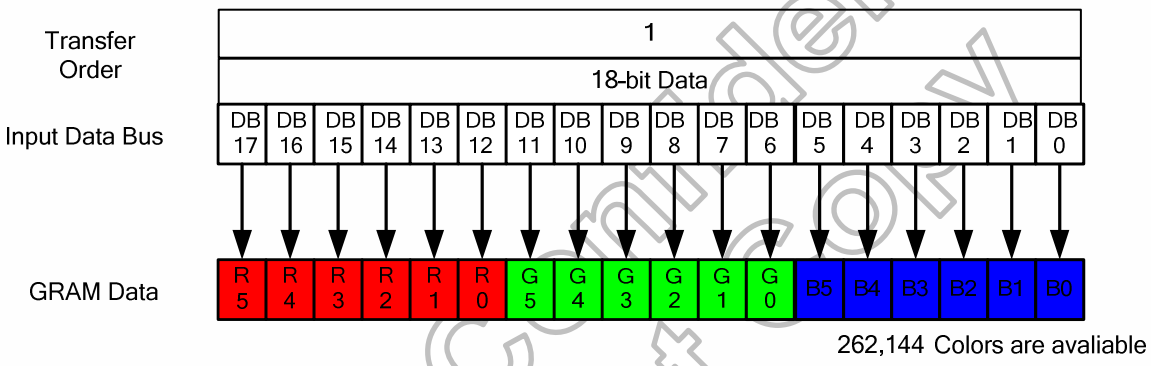

Figure 5.4 Input data bus and GRAM data mapping in 18-bit bus system interface with 18 bit-data input (“IFSEL0=1” and “BS3, BS2, BS1, BS0=0010” or “IFSEL0=0” and “BS3, BS2, BS1, BS0=0000”)

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16-bit parallel bus system interface

The I80-system 16-bit parallel bus interface **type I** can be used by setting external pins "IFSEL0=1" and "BS3, BS2, BS1, BS0" pins to "0000 or 0001". And I80-system 16-bit parallel bus interface **type II** can be used by setting "IFSEL0=0" and "BS3, BS2, BS1, BS0" pins to "0010". Figure 5.5 (IFSEL0=0is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

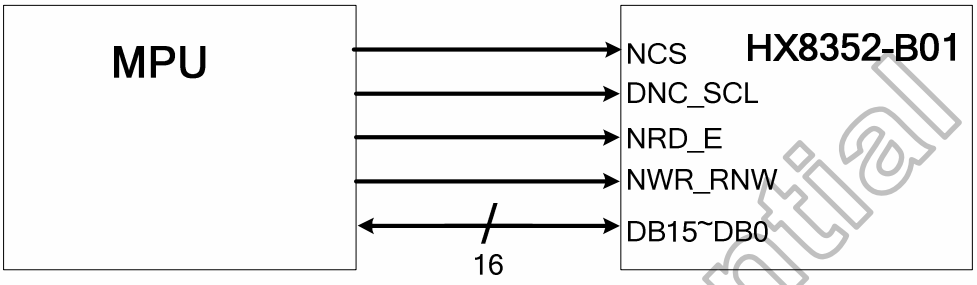

Figure 5.5 Example of I80 system 16-bit parallel bus interface type I

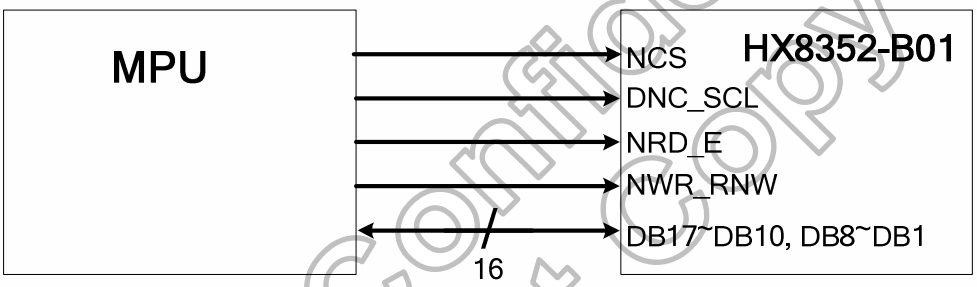

Figure 5.6 Example of I80 system 16-bit parallel bus interface type II

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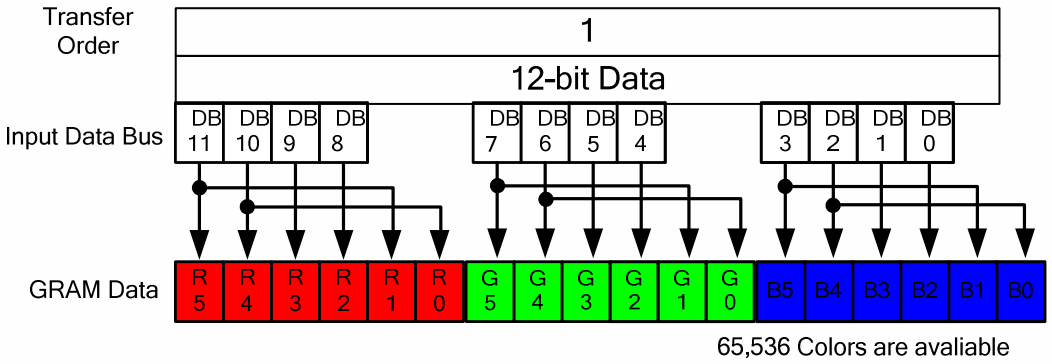

Figure 5.7 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(2+16) bit-data input (R17H=03h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0000 or 0001")

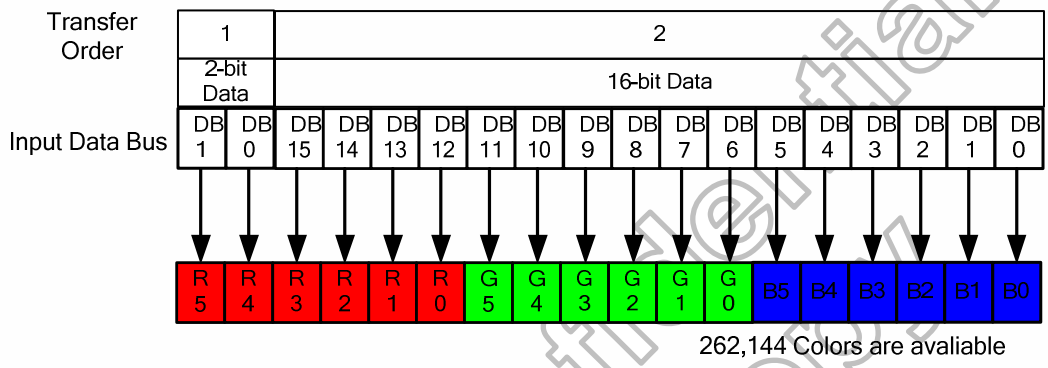

Figure 5.8 Input data bus and GRAM data mapping in 16-bit bus system interface with 12 bit-data input (R17H=04h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0000 or 0001")

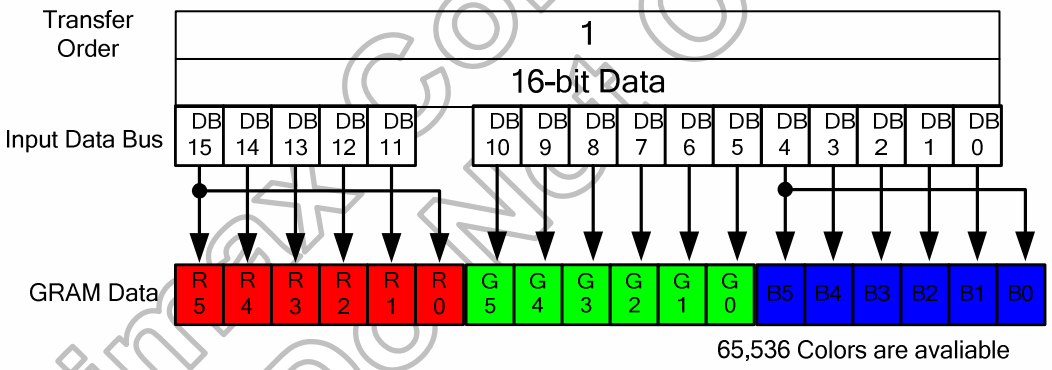

Figure 5.9 Input data bus and GRAM data mapping in 16-bit bus system interface with 16 bit-data input (R17H=05h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0000 or 0001")

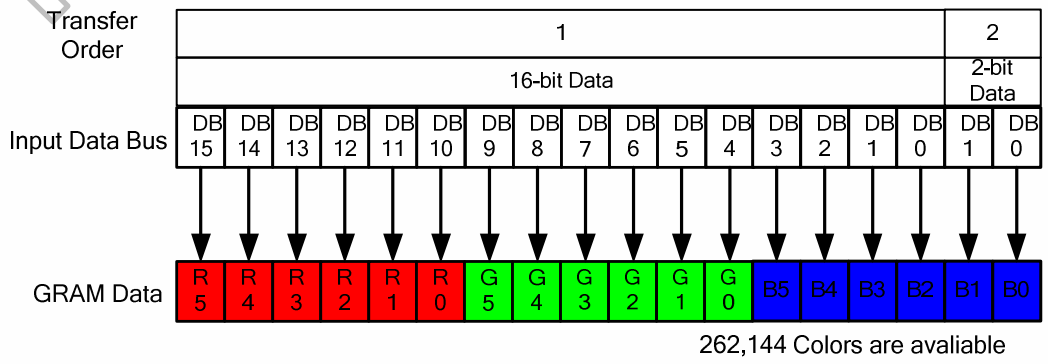

Figure 5.10 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IFSEL0=1" and "BS3,BS2, BS1, BS0"="0000 or 0001")

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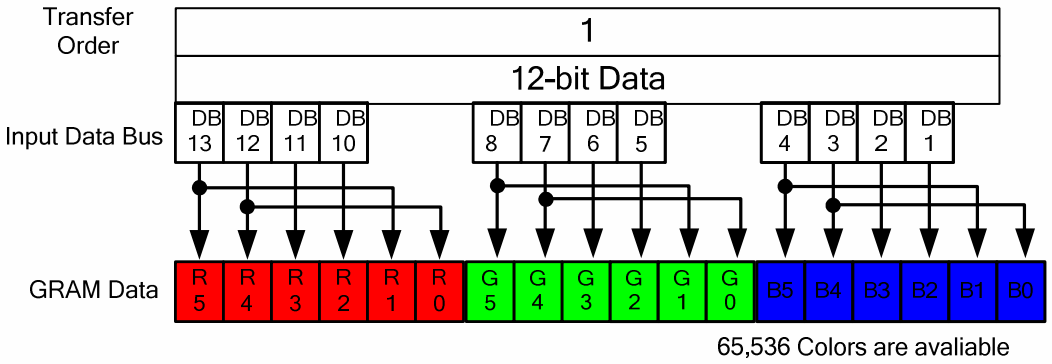

Figure 5.11 Input data bus and GRAM data mapping in 16-bit bus system interface with 12 bit-data input (R17H=03h and "IFSEL0=0" and "BS3, BS2, BS1, BS0"="0010")

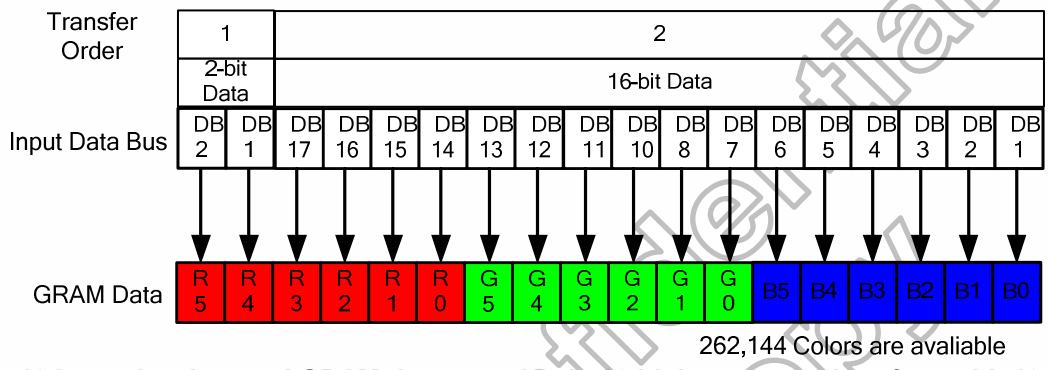

Figure 5.12 Input data bus and GRAM data mapping in 16-bit bus system interface with 12 bit-data input (R17H=04h and "IFSEL0=0" and "BS3, BS2, BS1, BS0"="0010")

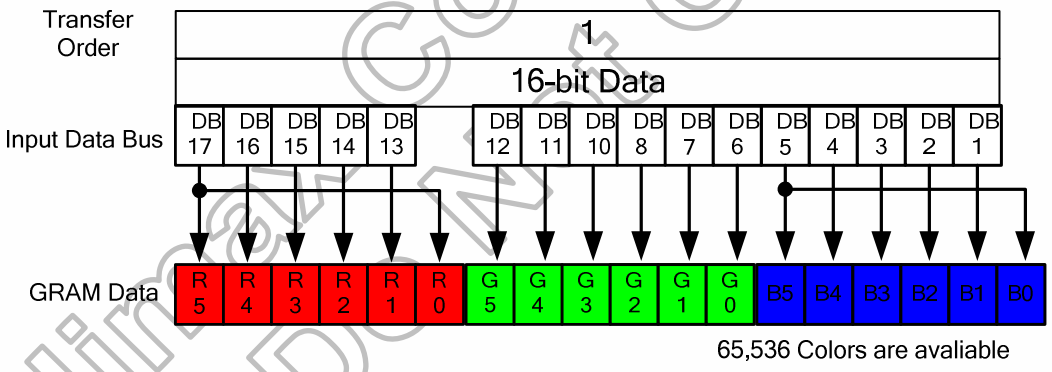

Figure 5.13 Input data bus and GRAM data mapping in 16-bit bus system interface with 16 bit-data input (R17H=05h and "IFSEL0=0" and "BS3, BS2, BS1, BS0"="0010")

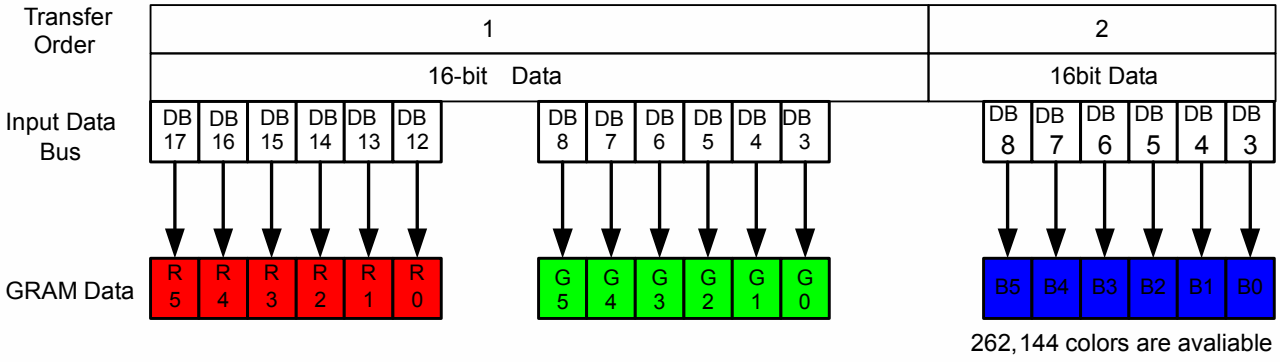

Figure 5.14 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(12+6) bit-data input (R17H=06h and "IFSEL0=0" and "BS3, BS2, BS1, BS0"="0010")

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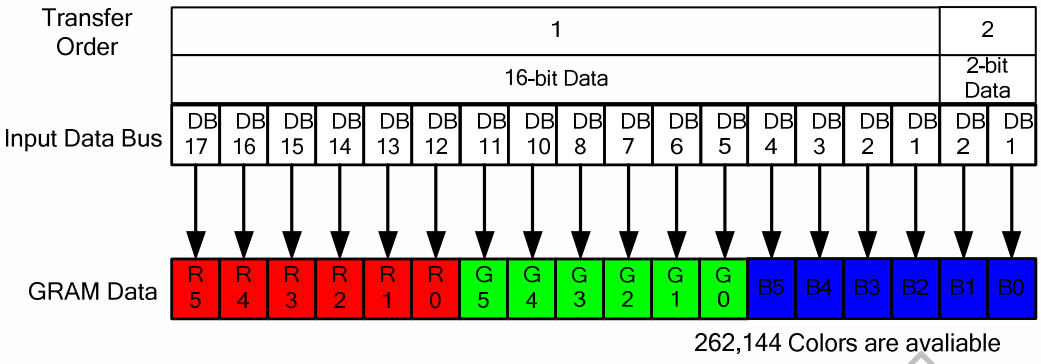

Figure 5.15 Input data bus and GRAM data mapping in 16-bit bus system interface with 18(16+2) bit-data input (R17H=07h and "IFSEL0=0" and "BS3, BS2, BS1, BS0"="0010")

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9-bit parallel bus system interface

The I80-system 9-bit parallel bus interface **type I** can be used by setting external pins "IFSEL0=1" and "BS3, BS2, BS1, BS0" pins to "1000". And I80-system 9-bit parallel bus interface **type II** can be used by setting "IFSEL0=0" and "BS3, BS2, BS1, BS0" pins to "0001". Figure 5.17 is the example of type I interface with I80 microcomputer system interface. And Figure 5.18 is the example of type II interface with I80 microcomputer system interface.

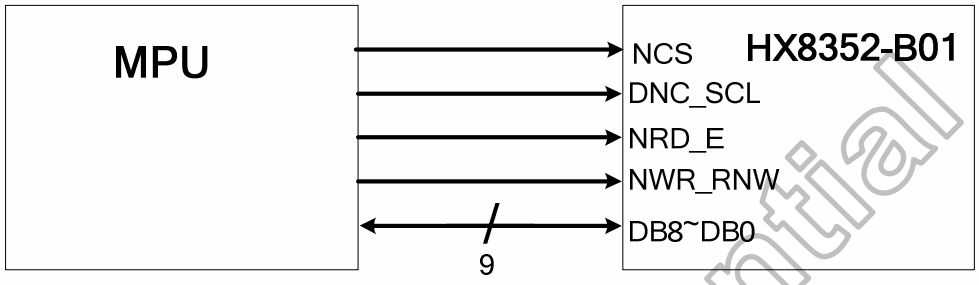

Figure 5.16 Example of I80 system 9-bit parallel bus interface type I

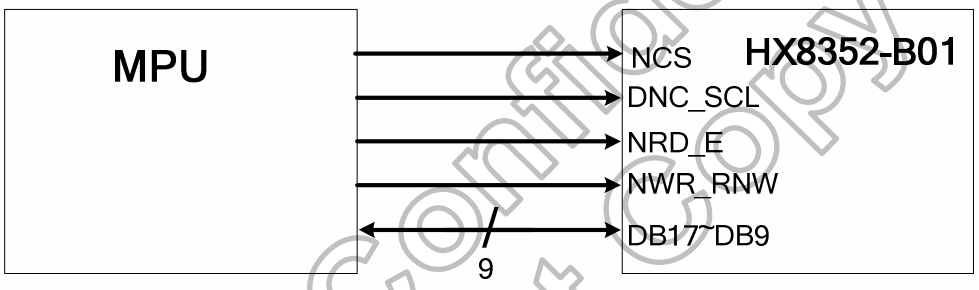

Figure 5.17 Example of I80 system 9-bit parallel bus interface type II

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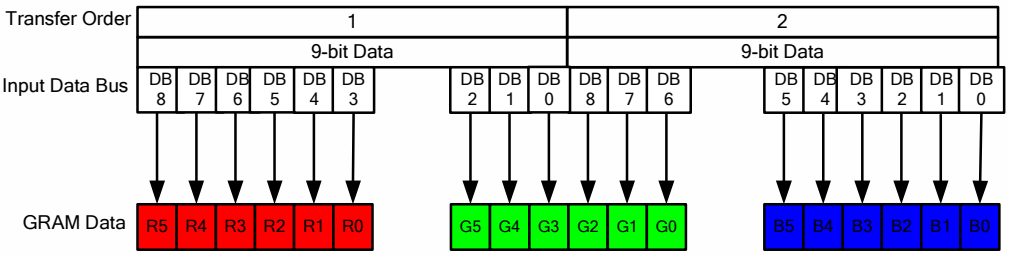

Figure 5.18 Input data bus and GRAM data mapping in 9-bit bus system interface with 18 bit-data input (R17H=06h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="1000")

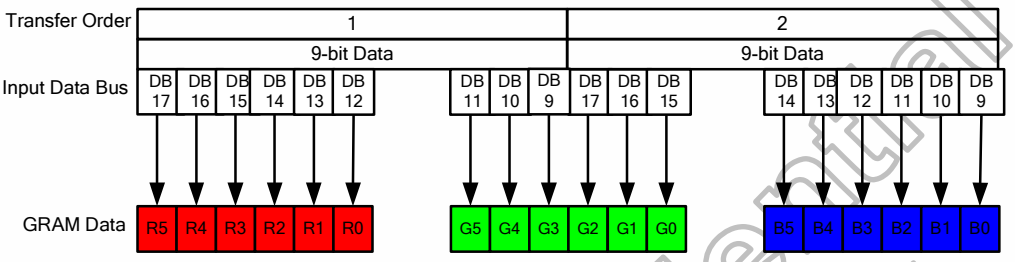

Figure 5.19 Input data bus and GRAM data mapping in 9-bit bus system interface with 18 bit-data input (R17H=06h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0001")

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8-bit parallel bus system interface

The I80-system 8-bit parallel bus interface **type I** can be used by setting external pins "IFSEL0=1" and "BS3, BS2, BS1, BS0" pins to "0011 or 0100". And I80-system 8-bit parallel bus interface **type II** can be used by setting "IFSEL0=0" and "BS3, BS2, BS1, BS0" pins to "0011". Figure 5.21 is the example of type I interface with I80 microcomputer system interface. And Figure 5.22 is the example of type II interface with I80 microcomputer system interface.

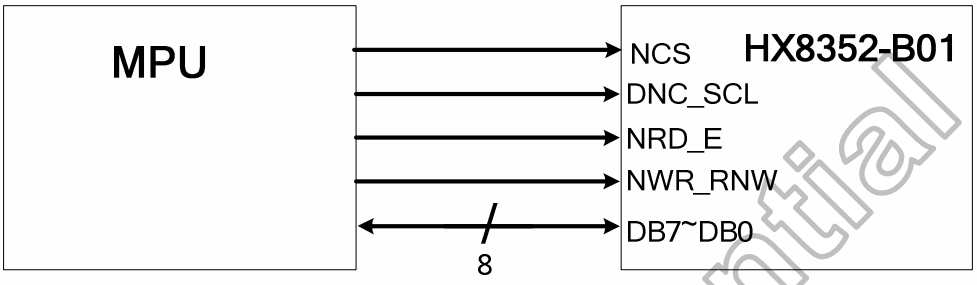

Figure 5.20 Example of I80-system 8-bit parallel bus interface type I

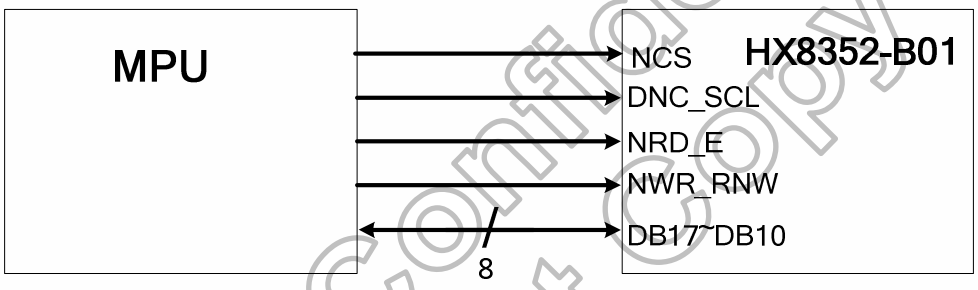

Figure 5.21 Example of I80-system 8-bit parallel bus interface type II

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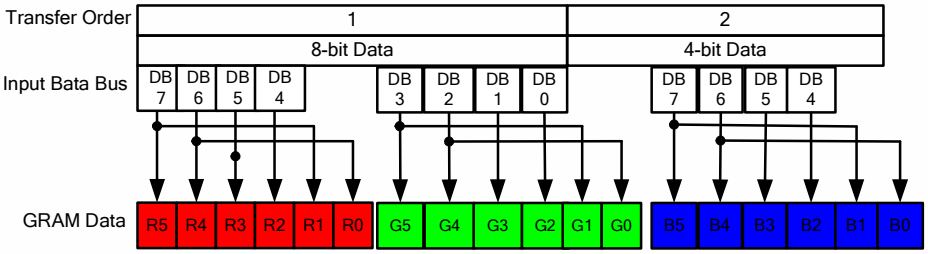

Figure 5.22 Input data bus and GRAM data mapping in 8-bit bus system interface with 12 bit-data input (R17H=03h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0011 or 0100")

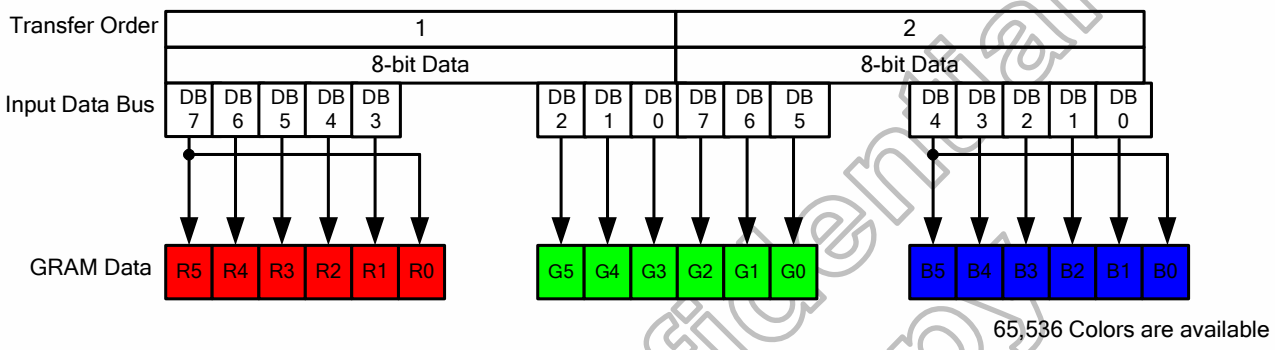

Figure 5.23 Input data bus and GRAM data mapping in 8-bit bus system interface with 16 bit-data input (R17H=05h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0011 or 0100")

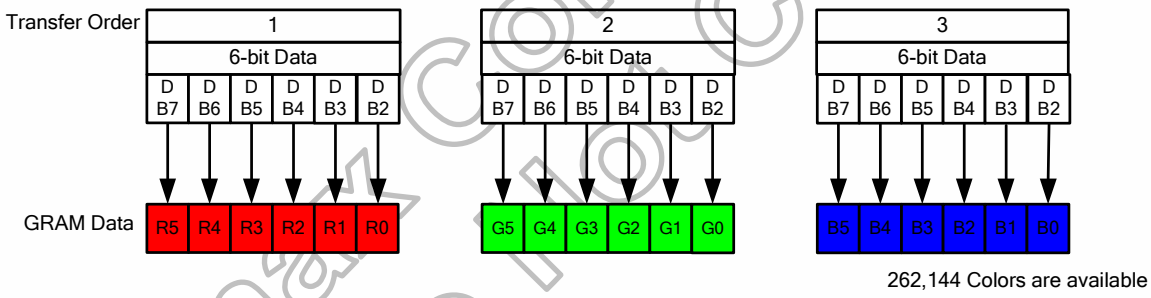

Figure 5.24 Input data bus and GRAM data mapping in 8-bit bus system interface with 18 bit-data input (R17H=06h and "IFSEL0=1" and "BS3, BS2, BS1, BS0"="0011 or 0100")

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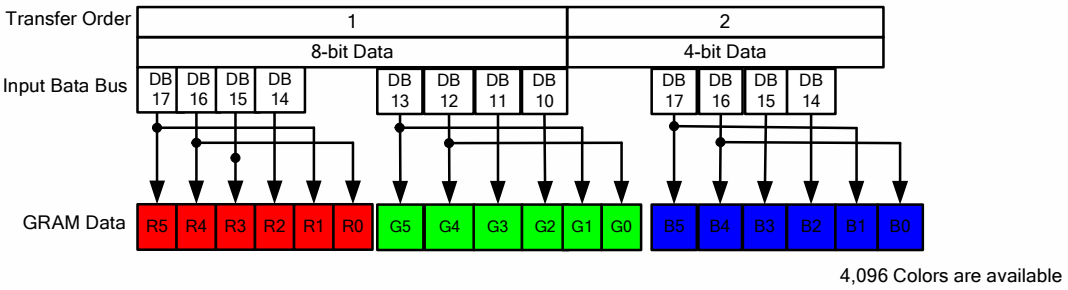

Figure 5.25 Input data bus and GRAM data mapping in 8-bit bus system interface with 12 bit-data input (R17H=03h and " IFSEL0=0" and "BS3, BS2, BS1, BS0"="0011")

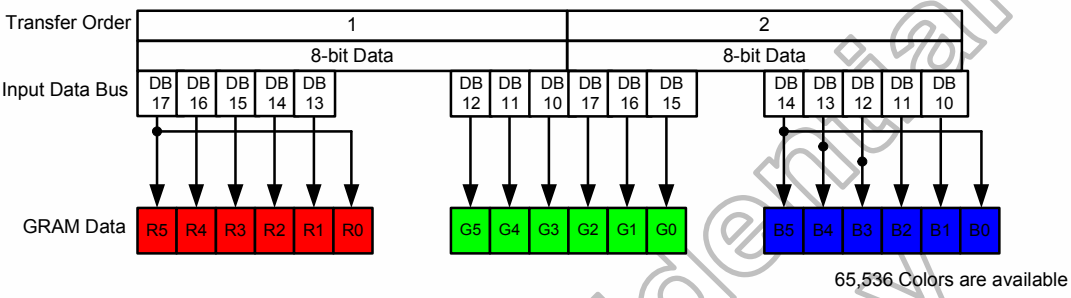

Figure 5.26 Input data bus and GRAM data mapping in 8-bit bus system interface with 16 bit-data input (R17H=05h and " IFSEL0=0" and "BS3, BS2, BS1, BS0"="0011")

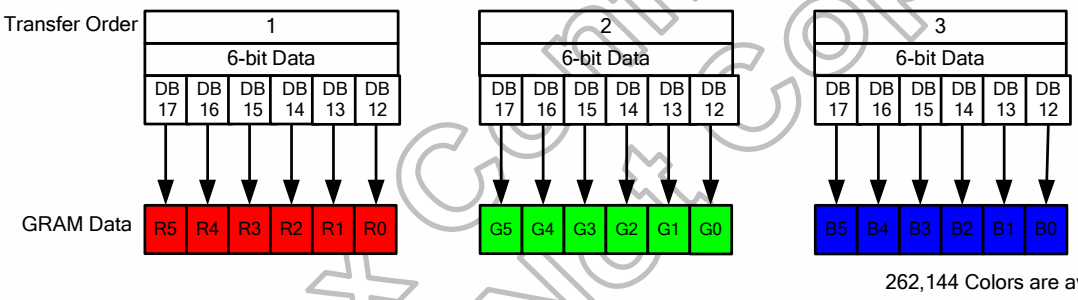

Figure 5.27 Input data bus and GRAM data mapping in 8-bit bus system interface with 18 bit-data input (R17H=06h and " IFSEL0=0" and "BS3, BS2, BS1, BS0"="0011")

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MCU Data Color Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface type I
("IFSEL0=1" and "BS3,BS2,BS1,BS0"="0011 or 0100")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.11 8-bit parallel interface type I GRAM read table

- Parallel 16-Bits Bus Interface type I
("IFSEL0=1" and "BS3,BS2,BS1,BS0"="0000 or 0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.12 16-bit parallel interface type I GRAM read table

- Parallel 9-Bits Bus Interface type I
("IFSEL0=1" and "BS3,BS2,BS1,BS0"="1000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.13 9-bit parallel interface type I GRAM read table

- Parallel 18-Bits Bus Interface type I
("IFSEL0=1" and "BS3,BS2,BS1,BS0"="0010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.14 18-bit parallel interface type I GRAM read table

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- Parallel 8-Bits Bus Interface type II
("IFSEL0=0" and "BS3,BS2,BS1,BS0"="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5.15 8-bit parallel interface type II GRAM read table

- Parallel 16-Bits Bus Interface type II
("IFSEL0=0" and "BS3,BS2,BS1,BS0"="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
		x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixel/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5.16 16-bit parallel interface type II GRAM read table

- Parallel 9-Bits Bus Interface type II
("IFSEL0=0" and "BS3,BS2,BS1,BS0"="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixel/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5.17 9-bit parallel interface type II GRAM read table

- Parallel 18-Bits Bus Interface type II
("IFSEL0=0" and "BS3,BS2,BS1,BS0"="0000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.18 18-bit parallel interface type II GRAM read table

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5.1.3 Serial bus system interface

The HX8352-B01 supports two kinds serial bus interface: 3-wire /4-wire serial interface. The 3-wire serial interface can be selected by setting external pins (“IFSLE0=1” and “BS3, bS2, BS1” pins to “X11”) or (“IFSEL0=0” and “BS3, BS2, BS1” pins to “010”).The 4-wire serial interface can be selected by setting external pins (“IFSLE0=0” and “BS3, bS2, BS1” pins to “011”). The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), serial output data (SDO) and the serial transfer clock signal (DNC_SCL).

5.1.3.1 3-wire serial interface

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

Table 5.19 Function of RS and R/W bit bus

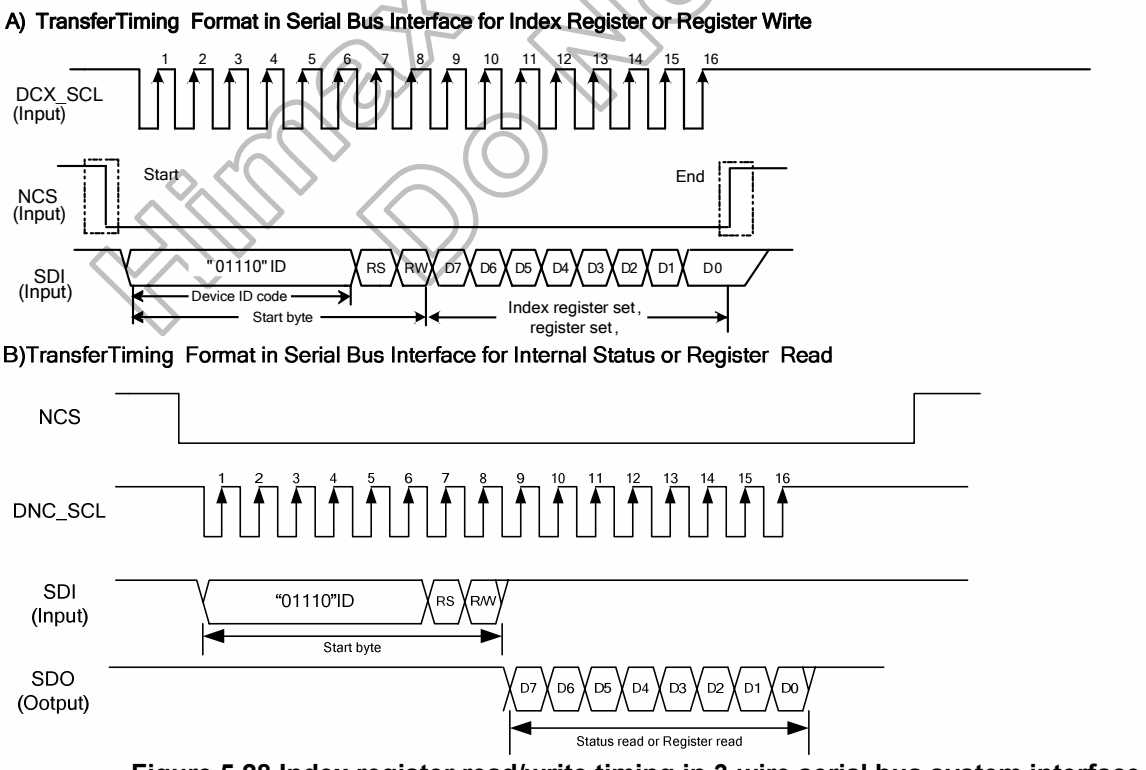

Figure 5.28 Index register read/write timing in 3-wire serial bus system interface

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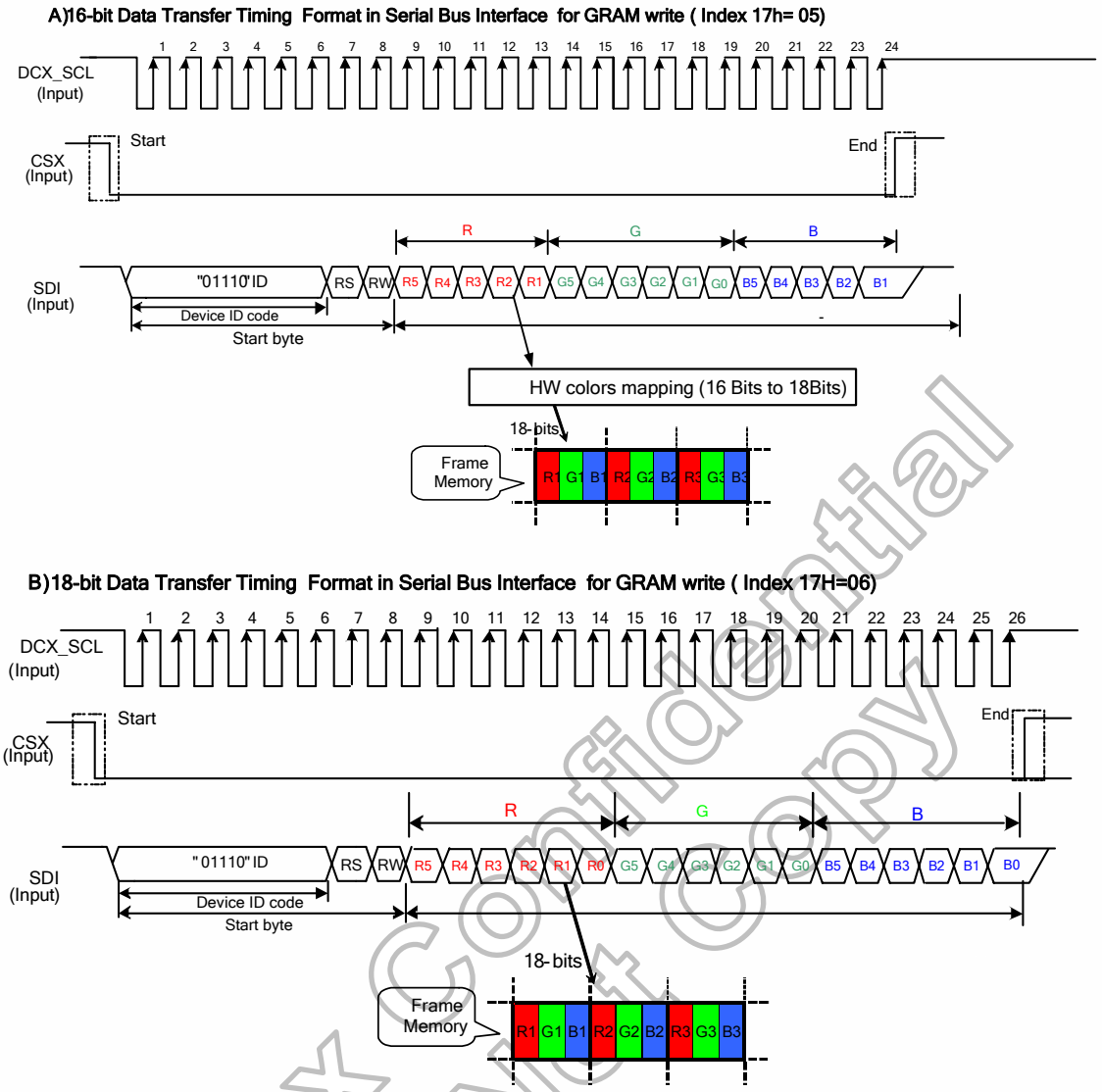

Figure 5.29 Data write timing in 3-wire serial bus system interface

5.1.3.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by NWR_RNW pin. If NWR_RNW is low, the transmission byte is command byte. If NWR_RNW is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, DNC_SCL clock pulse or SDI data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

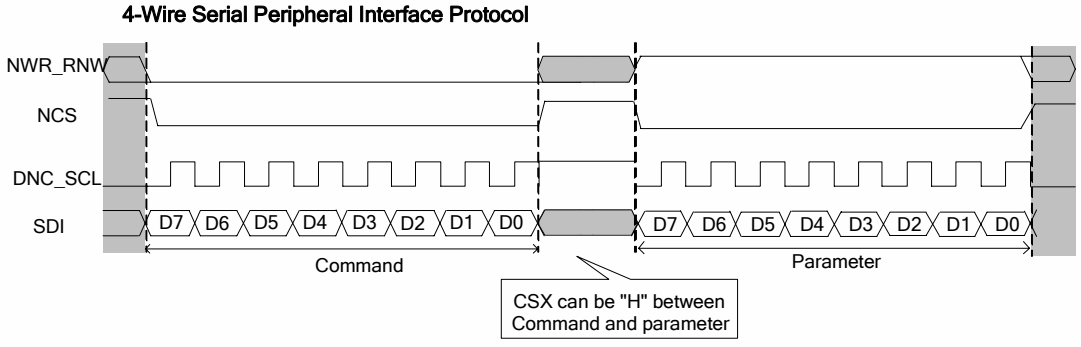

Figure 5.30 Index register write timing in 4-wire serial bus system interface

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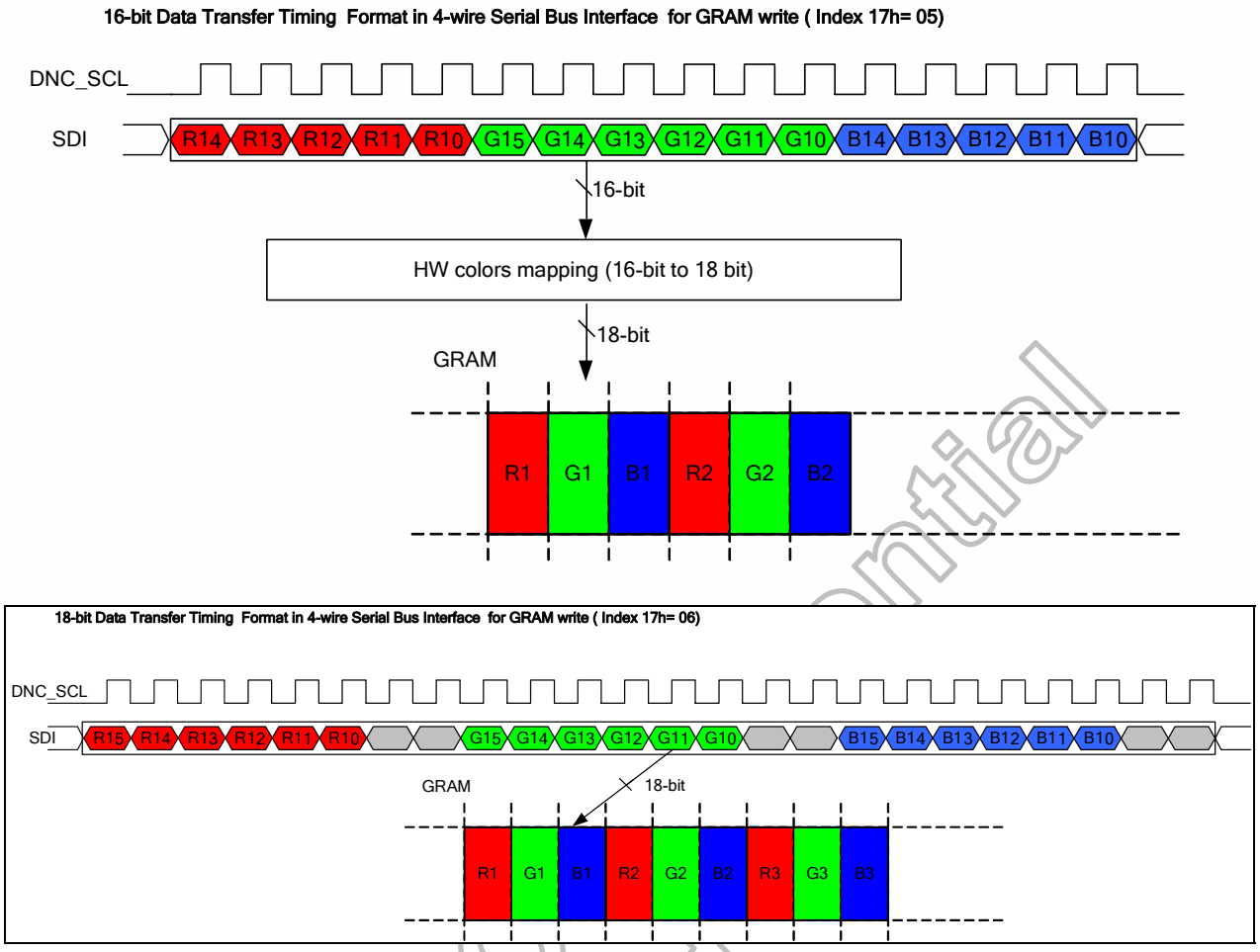

Figure 5.31 Data write timing in 4-wire serial bus system interface

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5.2 RGB interface

The HX8352-B01 uses **R31h[1:0](RCM[1:0] bit) ='10' or '11' setting to select RGB interface.** When after Power on Sequence, the RGB interface is activated. When RCM[1:0]='10' use VSYNC, HSYNC, ENABLE, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM[1:0]='11' use VSYNC, HSYNC, DOTCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (DOTCLK) must be running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLEand DB17-0 lines states when there is a rising edge of the DOTCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level('H') of ENABLE signal, and display operations are executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and pixel clock (DOTCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HSYNC signal, and the VBP setting of VS. In these two RGB interface mode, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VSYNC) signal is used to tell when a new frame of the display is received, and this is negative ('-', '0', low) active. Horizontal synchronization signal (HSYNC) is used to tell when a new line of the frame is received, and this is negative ('-', '0', low) active. Data enable (ENABLE) is used to tell when to receive RGB information that should be transferred on the display, and this is positive ('+', '1', high) active. DB17-0 are used to tell what is the information of the image that is transferred on the display when ENABLE='H'.

The pixel clock cycle is described in the following figure.

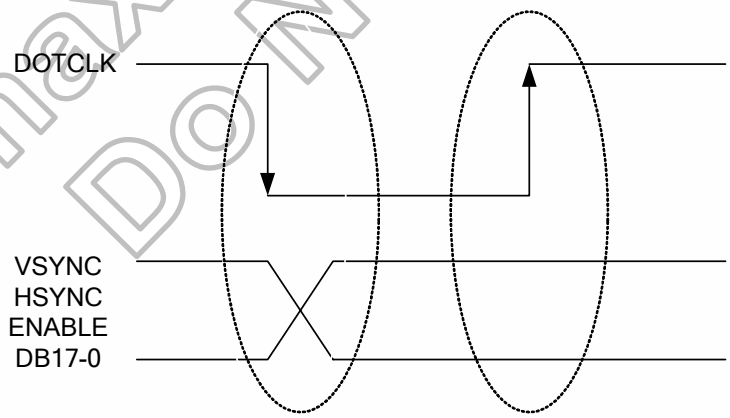

Figure 5.32 DOTCLK cycle

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General timing diagram in RGB interface is as below.

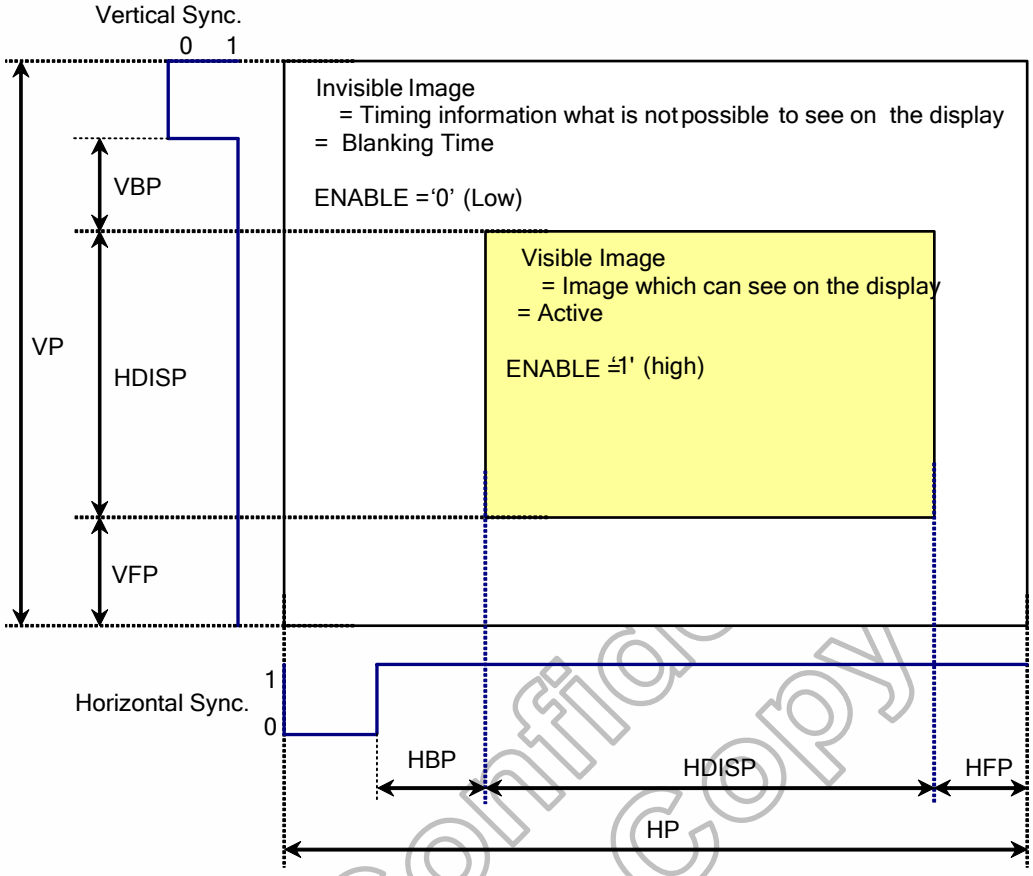

Figure 5.33 RGB interface circuit input timing diagram

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.

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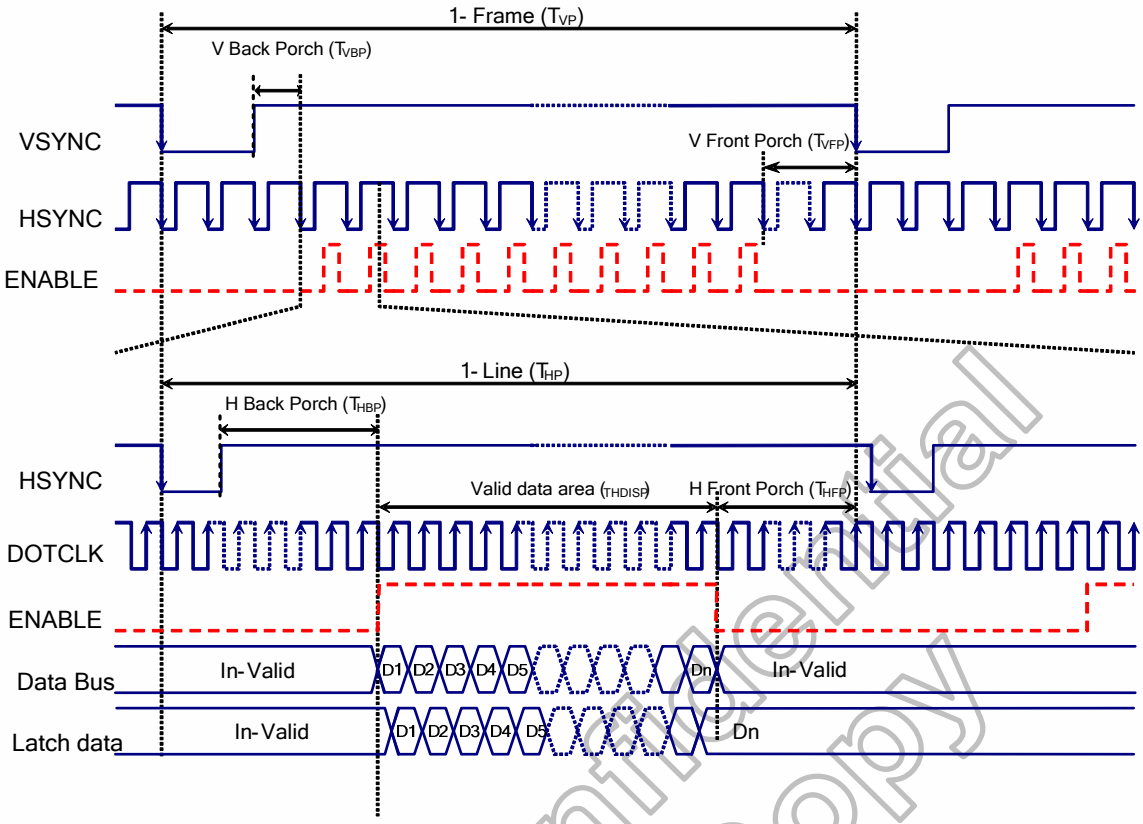

Note: (1) RGB mode 2 doesn't need DE signal
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of RGB interface control 2(R32H) command.

Figure 5.34 RGB mode timing diagram

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All 3-kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bits, 16-bits and 18-bits data width)

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
00h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bit data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	16-bit data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data

Note: (1) When 17H="00h", 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(2) Only 17H= "00h","50h", "60h" are valid on RGB I/F, Others are invalid.
(3) 'x' don't care, but need to set IOVCC or VSSD level.

Table 5.20 RGB interface bus width set table

RGB interface mode

RGB I/F Mode	DOTCLK	ENABLE	VSYNC	HSYNC	Video Data bus DB[B:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2-kinds of RGB mode which is selected by R31h[1:0](RCM[1:0] bit) setting.

In RGB Mode 1 (RCM[1:0] = "10"), writing data to display is done by DOTCLK and Video Data Bus (DB[17:0]), when ENABLE is high state. The external synchronization signals (DOTCLK, VSYNC and HSYNC) are used for internal display signals. So, controller (host) must always transfer DOTCLK, VSYNC, HSYNC and ENABLE signals to driver.

In RGB Mode 2 (RCM[1:0] = "11"), blanking porch setting of VSYNC and HSYNC signals are defined by RGB interface control 1 (R32h) command. DE pin is not used.

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5.2.1 Color order on RGB interface

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on RGB interface, is describing on the following table:

Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colors on this table - Not all gray levels of colors.

Table 5.21 Meaning of pixel information for main colors on RGB interface

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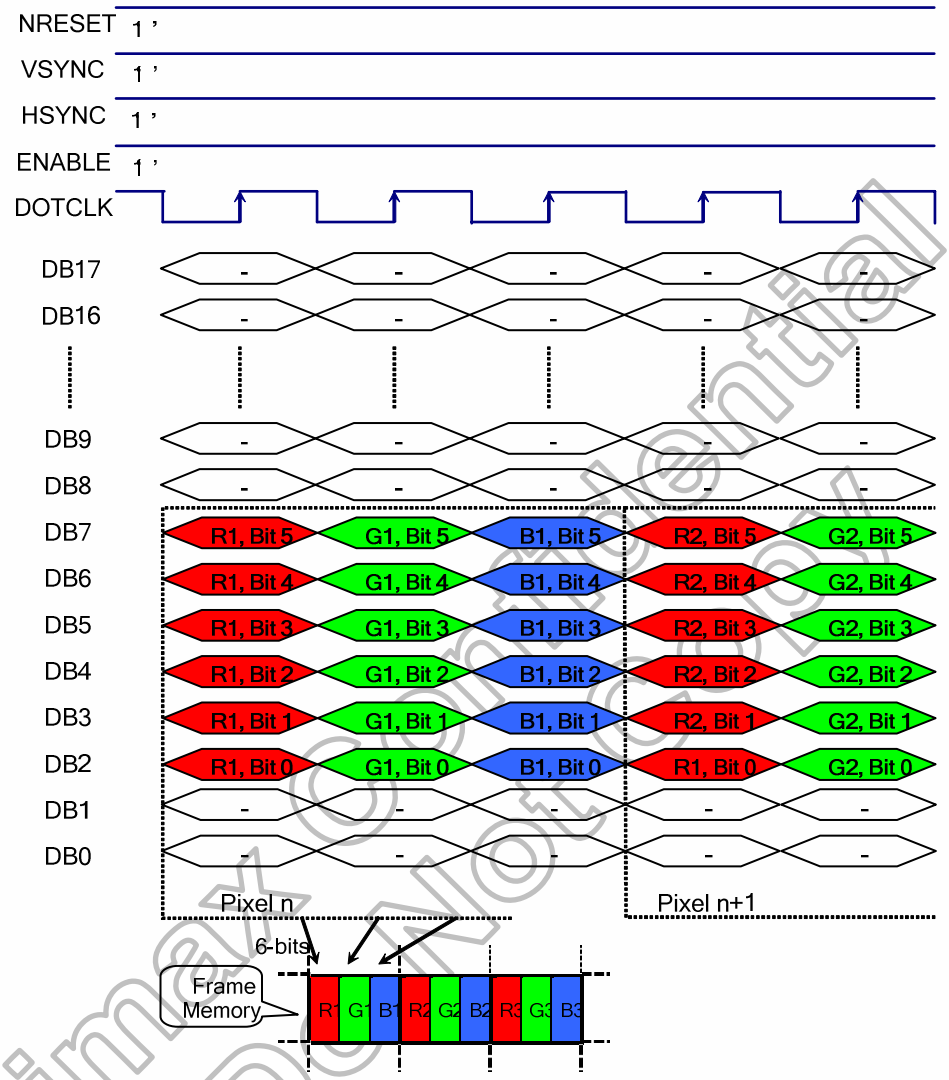
5.2.2 RGB data color coding

18-bits/pixel Colors Order on 6-bits Data width RGB Interface (RGB 6-6-6-bits input). There are 1 pixel (3 sub-pixels) per 3 bytes, 262k-colors, 17H="00h"



Note: (1) The data order is as follows, MSB=DB7, LSB=DB2 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data. (3-trandfer data one pixel)
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5.35 RGB 18-bit/pixel on 6-bit data width

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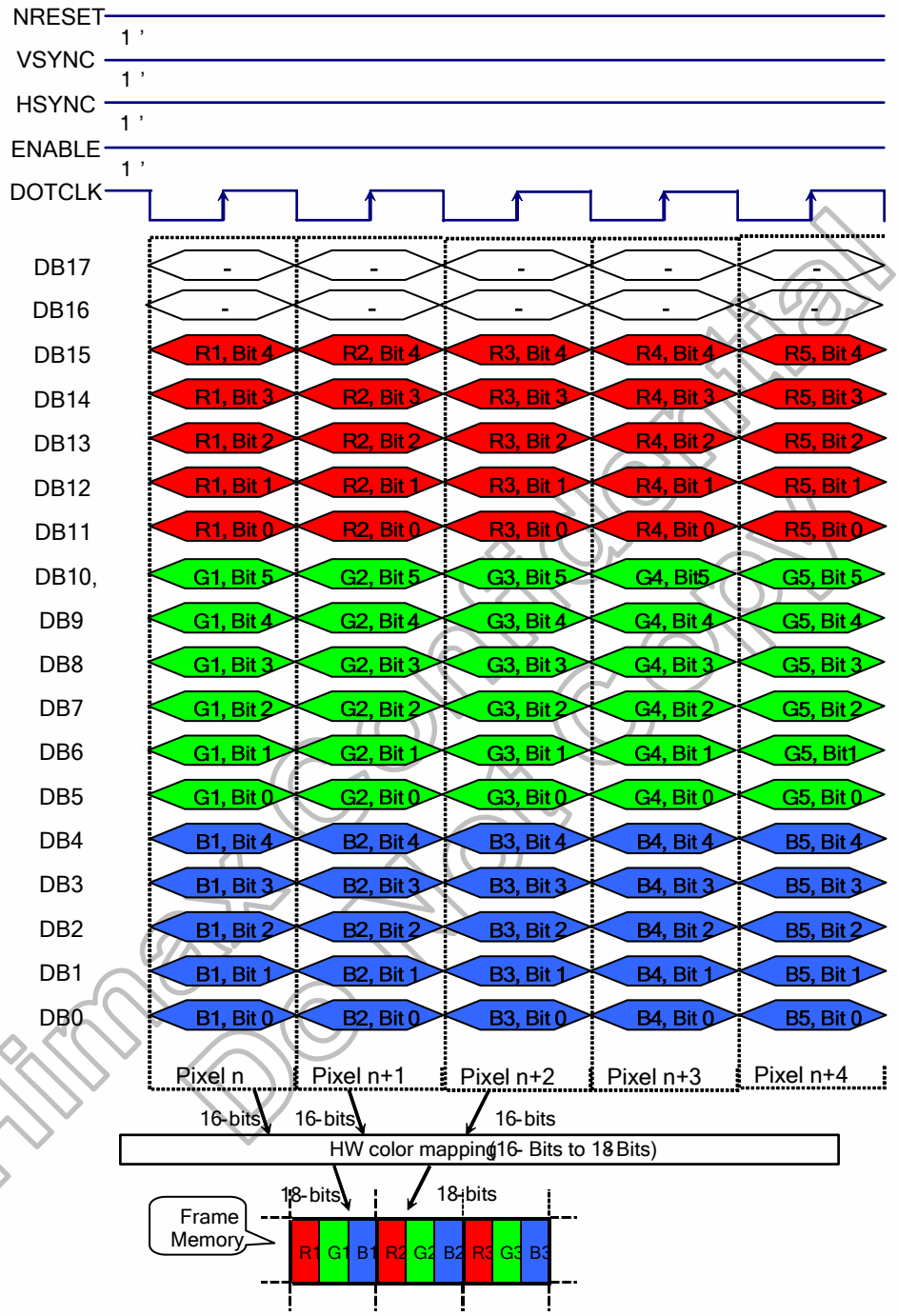
16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input). There are 1 pixel (3 sub-pixels) per 1 bytes, 65K-colors, 17H="50h"



Note: (1) The data order is as follows, MSB=DB15, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5.36 RGB 16-bit/pixel on 16-bit data width

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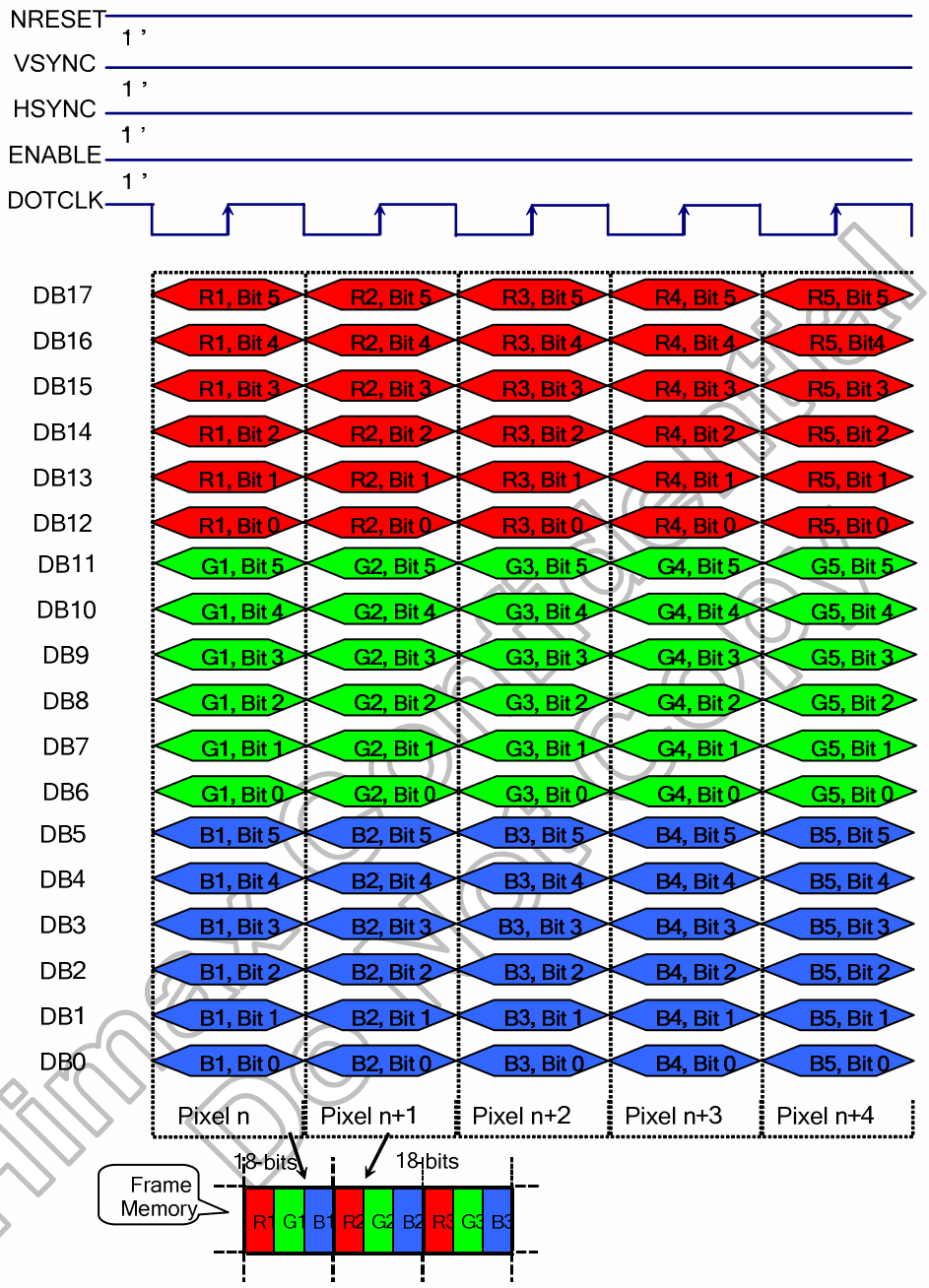
18-bits/pixel Colors Order on the 18-bits Data width RGB Interface (RGB 6-6-6-bits input). There are 1 pixel (3 sub-pixels) per 1 bytes, 262K-colors, 17H="60h"



Note: (1) The data order is as follows, MSB=DB17, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.

Figure 5.37 RGB 18-bit/pixel on 18-bit data width

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5.2.3 MDDI interface (mobile display digital interface)

5.2.3.1 Introduction of MDDI

The HX8352-B01 supports MDDI, which is a differential serial interface with high-speed, low voltage swing characteristics. Both command and display image data can be transferred by MDDI. The devices connected by Data and STB link are host and client part.

Host transfer data to client in “forward” direction, client transfer data to host in “reverse” direction. The Data line is Dual direction, both command and image data are all send through the Data line. The STB line send strobe signal from host to client.

Data transferred in MDDI link are encoded as packet type.

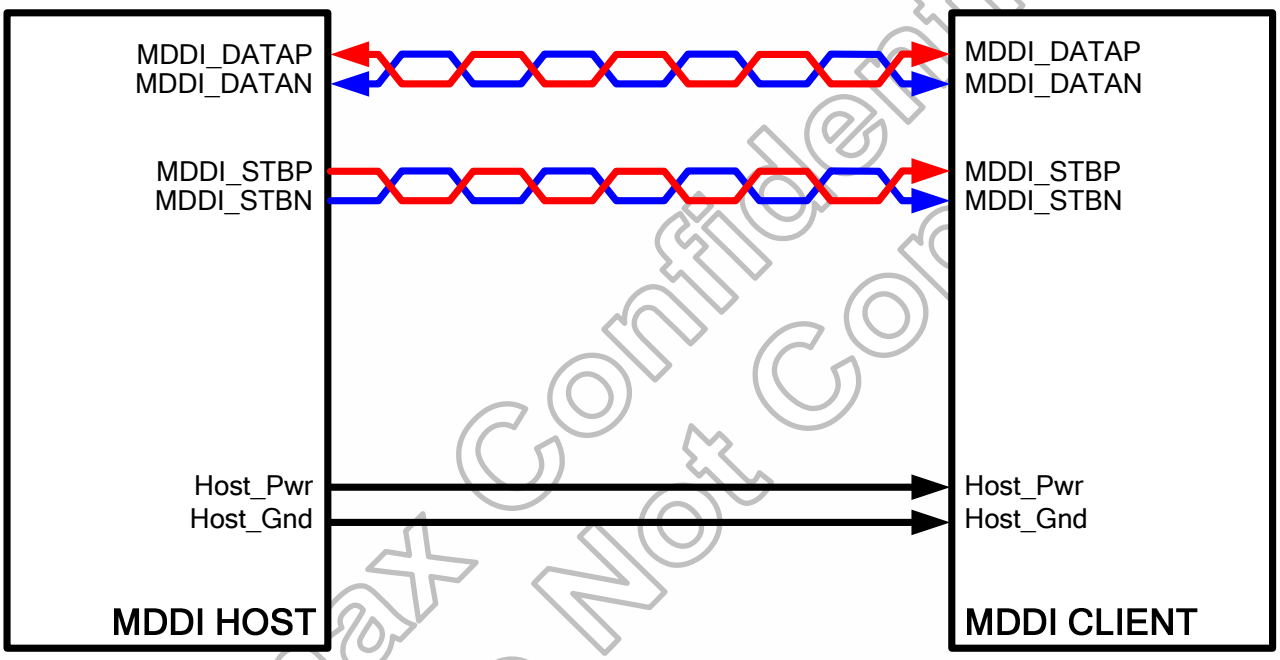

Figure 5.38 Physical connection of MDDI host and client

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5.2.3.2 Terminology

The devices connected by the MDDI link are called the host and client. Data going from the host to the client travels in the ***forward*** direction, and data from the client to the host travels in the ***reverse*** direction.

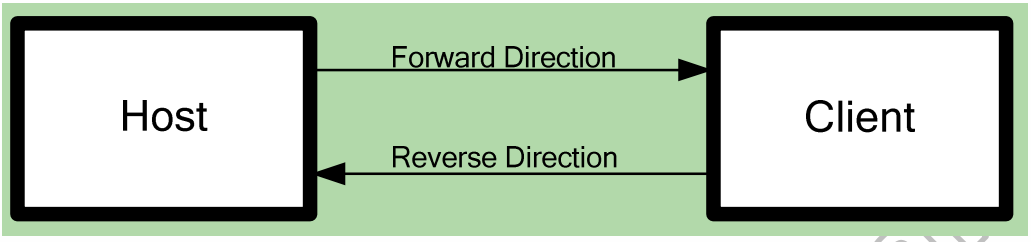

Figure 5.39 MDDI terminology

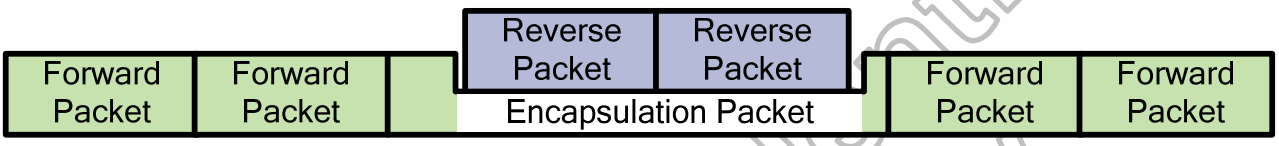

Figure 5.40 Example of bi-directional MDDI communication

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5.2.3.3 Data-STB encoding

Data is encoded using a DATA-STB format. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure 5.42 illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

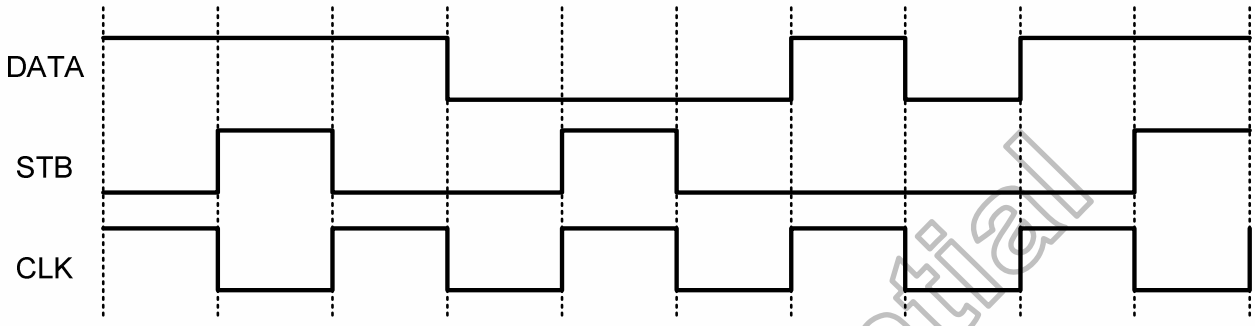

Figure 5.41 Data-STB encoding

Figure 5.43 shows a sample circuit to generate DATA and STB from input data, and them recover the input data from DATA and STB.

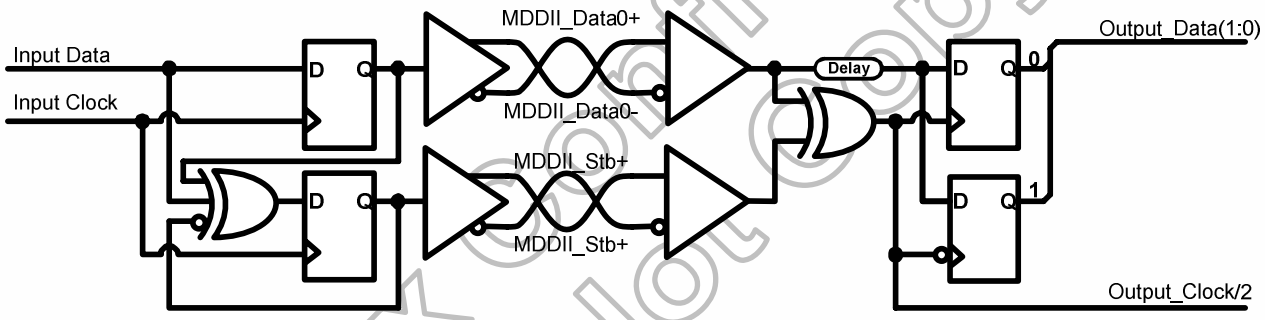

Figure 5.42 Data / STB generation & recovery circuit

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5.2.3.4 MDDI data/STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

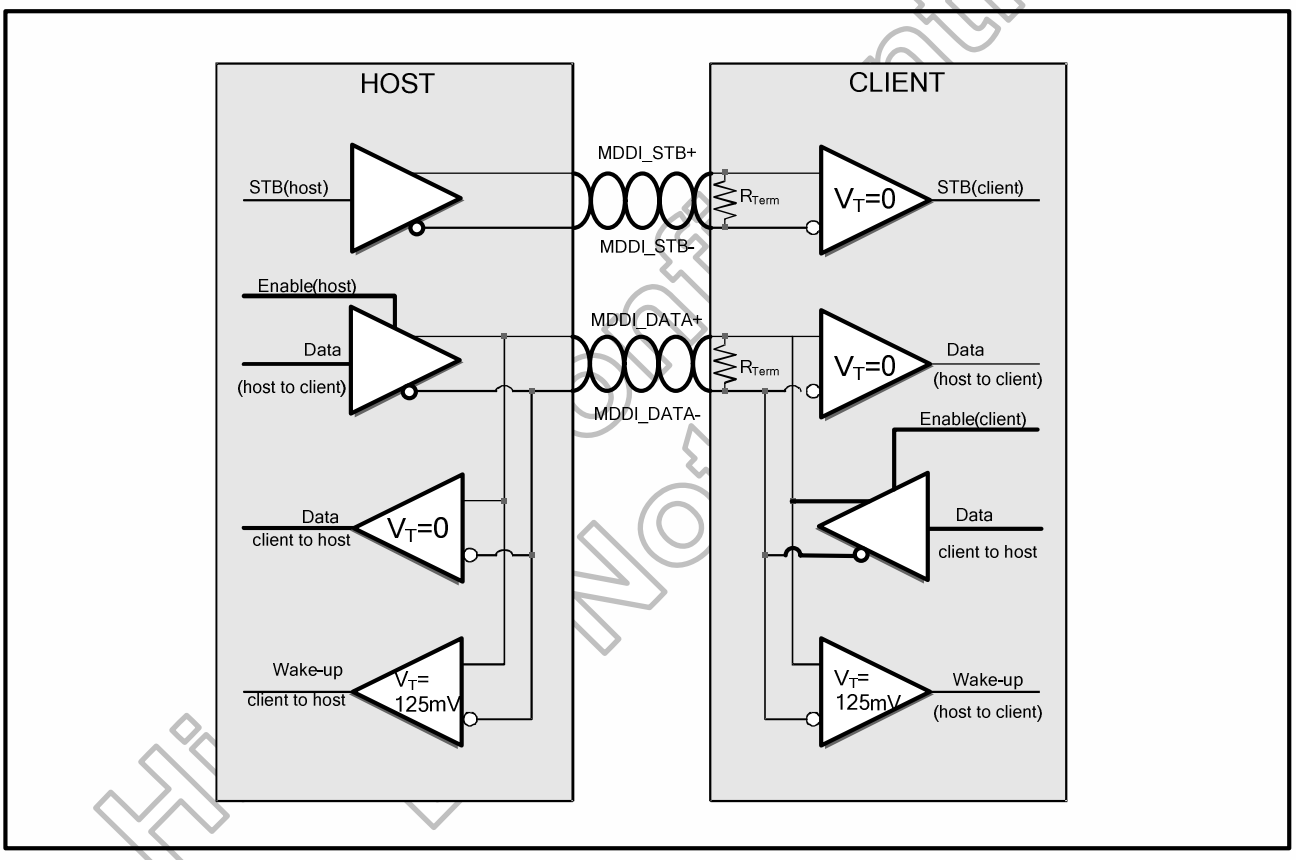

Figure 5.43 Differential connection between host and client

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5.2.3.5 MDDI packet

Data transmitted over the MDDI link is grouped into packets. Several packets format is supported in HX8352-B01. Most packets are in forward direction, transferred from host to client; but reverse encapsulation packet is in reverse direction, transferred from MDDI client to host. A number of packets, started by sub-frame header packet, construct one sub frame.

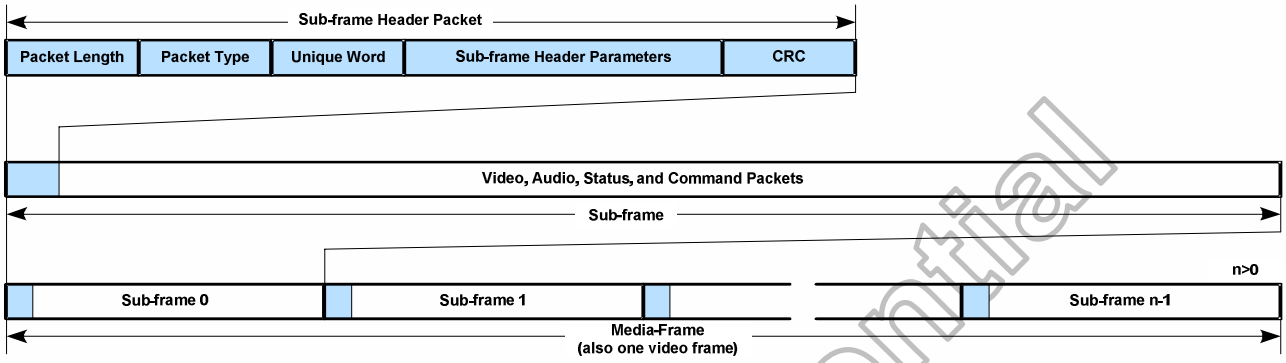

Figure 5.44 MDDI packet structure

Refer to MDDI frame structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frames make up a media-frame.

The HX8352-B01 supports 9 types of packets, which is described in the table below.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse

Table 5.22 List of supported MDDI packet

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Sub-frame header packet

Packet Length	Packet type =0x3bffh	Unique word =0x005a	Reserved 1	Sub-frame length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 0x3bffh for sub-frame header packet
unique word : link packet type to form a 32-bit unique word for good autocorrelation.
reserved 1 : not used(all zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet.
media frame count : specifies number of media frame
CRC : error check

Register access packet

Packet Length	Packet type =146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data list	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 146(decimal) for register access packet
bClient ID : set all zero
Read/Write Info : when write value to register, bit[15:14] = “00”
when request data from register, bit[15:14]=“10”
when data from register, bit[15:14] = “11”
bit[13:0] : 00_0000_0000_0001
register address : Register address is set written here.
parameter CRC : To error check from packet length to register address
register data list : Paramter data is written here.
register data CRC : To error check register data list.

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Video stream packet

Packet Length	Packet type =16	bClient ID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom dedge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
bClient ID : set all zero
video data format descriptor : bits[15:13]=010, raw RGB format (fixed value)
bit[12]=1,only packed type is available (fixed value)
bits[11:0]=0110_0110_0110, 18bit pixel
bits[11:0]=0101_0110_0101, 16bit pixel
: bits[1:0]=11, displayed both eyes (fixed value)
pixel data attributes : bit[5]=1, X left edge .. Y start is not defined.(fixed value)
others are all zero
X left edge : X coordinate of the left edge of the active window filled by the Pixel Data field.
X top edge : Y coordinate of the top edge of the active window filled by the Pixel Data field
X right edge : X coordinate of the right edge of the active window filled by the Pixel Data field.
Y bottom edge : Y coordinate of the bottom edge of the active window filled by the Pixel Data field.
X start : X coordinate of the first pixel in the Pixel Data field below
Y start : X coordinate of the first pixel in the Pixel Data field below
Pixel count : Write number of pixel
Patameter CRC : To error check from packet length to pixel count
pixel data : pixel data info. Number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

Filler packet

Packet Length	Packet type =0	filler bytes (all zero)	CRC
2 bytes	2 bytes	packet length – 4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
filler bytes : set to all zero (The size is under packet length available)
CRC : To error check

Link shutdown packet

Packet Length	Packet type =69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
CRC : To error check
All zeros : write all zero (size is 16 bytes, because MDDI for HX83xx is type 1)

Fixed Value

For more information about MDDI packet refer to VESA MDDI spec.

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5.2.3.6 Tearing-iess display

When you use the HX8352-B01, it is important to match timing at which to write data with timing at which to read data. If the two types of timing not match each other, tearing effect will occur. In HX8352-B01, two ways to prevent display-tearing phenomenon are supported.

The first case is such that the speed at which to write data is lower than the speed at which to read data. Under this situation, the writing data speed not critical, but longer period during transferring data will cause a larger current consumption in the interface. The system, therefore, selects a wider period during writing data.

The second case is such that the data writing speed is higher than the data reading speed. Under that situation, the data updating speed becomes very high, but the transfer period can be shortened. Current consumption by the interface can be minimized, but higher-speed data is required. Most important is to prevent contention of updating data and scanning display data.

Figure below provides an example of preventing tearing effects.

(1) Panel read is faster than MPU write

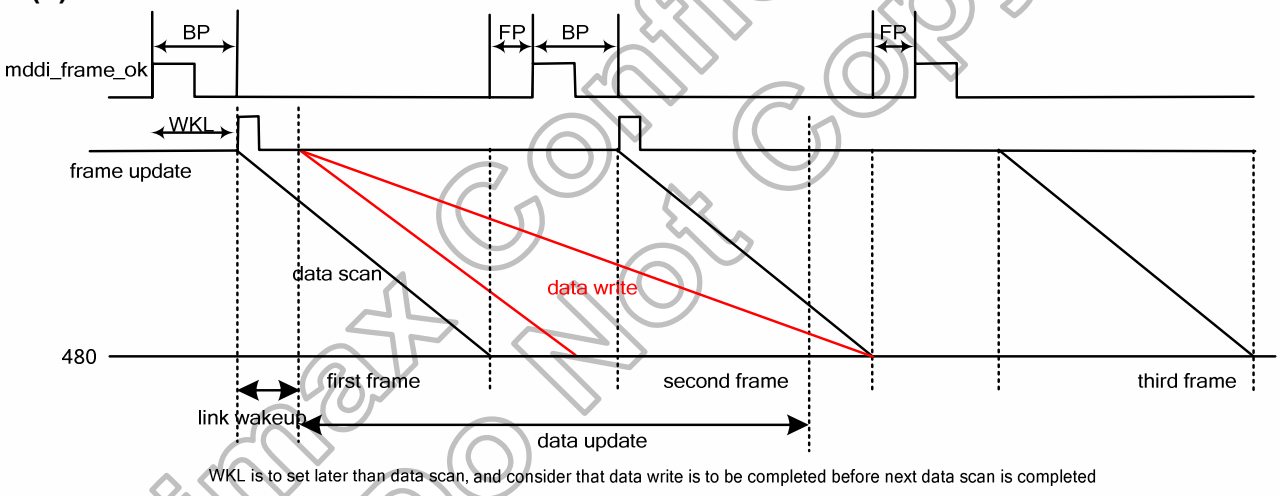

Figure 5.45 Panel read is faster than MPU write

Tearing-less display: The panel read speed is faster than MPU write.

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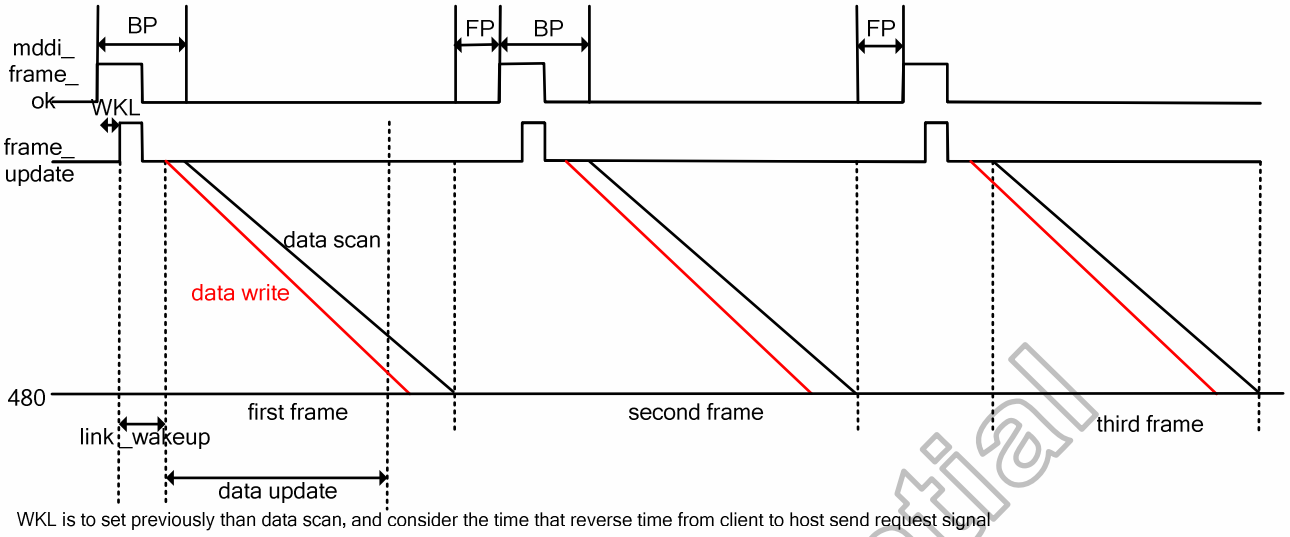
(2) Panel read is slower than MPU write



WKL is to set previously than data scan, and consider the time that reverse time from client to host send request signal

Figure 5.46 Panel read is slower than MPU write

Tearing-less display: The panel read speed is slower than MPU write.

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5.2.3.7 Hibernation / wake up

For reducing current consumption, the HX8352-B01 supports hibernation mode. The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption. In hibernation mode, hi-speed drivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

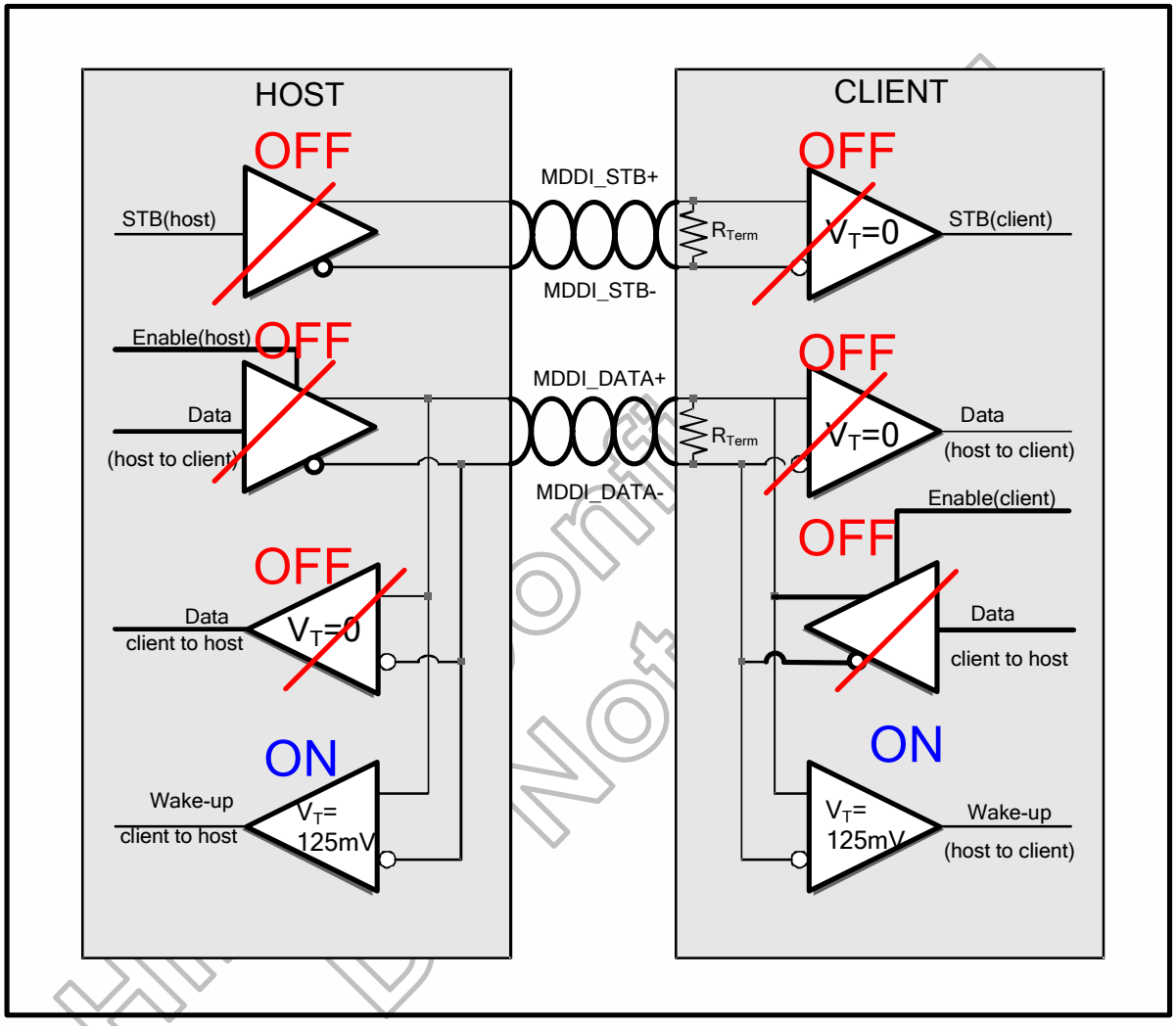

Figure 5.47 MDDI transceiver / receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulsed can be detected using low-speed line receivers that consume only a fraction of the current as the differential receivers required to receive the signals at the maximum link operating speed.

Either the host or client can wake up the link, which are supported in HX8352-B01: Host-Initial Wakeup & Client-Initial Wakeup.

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5.2.3.8 MDDI link wakeup sequence

Figure 5.49 below provides a host-initiated wake-up which is described below without contention from the client trying to wake up at the same time. The labeled events are:

Host-initiated wake-up:

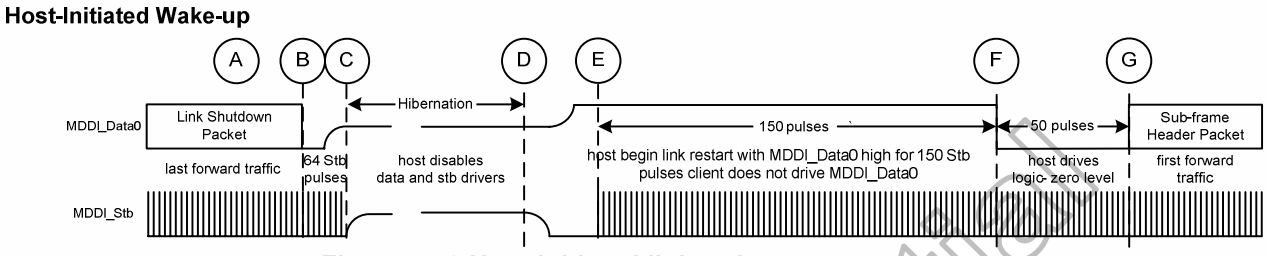

Figure 5.48 Host-initiated link wakeup sequence

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

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An example of a typical client-initiated service request event with no contention is illustrated in below figure 5.50. The labeled events are:

Client-initiated wake-up:

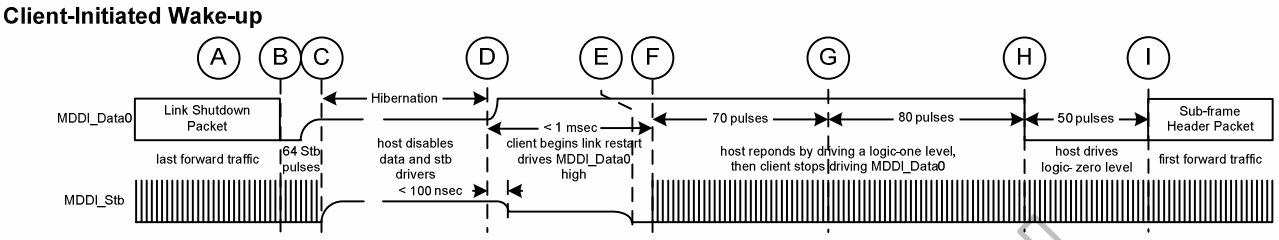

Figure 5.49 Client-initiated link wake-up sequence

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data0 driver while driving MDDI_Data0 to a logic-one level. It is allowed for MDDI_Data0 and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid fullydriven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data0 at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data0. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

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G. The client continues to drive MDDI_Data0 to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data0 driver at point G. The host continues to drive MDDI_Data0 to a logic-one level for a duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data0 to a logic-zero level.

H. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

I. After asserting MDDI_Data0 to a logic-zero level and driving MDDI_Stb for a duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

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5.2.3.9 Sequence for the client to wake up the link

The HX8352-B01 supports two link wake up mode for the client based on VSYNC. Only in hibernation mode, the client can wake up the link. User should configure the register for a wakeup before link is shut down.

Link wakeup based on VSYNC

When all display data finishes being displayed in display mode, a data request is sent to the MDDI host for new video data. The MDDI link is normally in hibernation mode for reducing power dissipation by the interface. Before the on-chip RAM is updated, the MDDI link must be woken up. In that case, you can use a link wakeup by the client as a data request. When the link wakeup register VWAKE_EN is set in VSYNC mode, the link is woken up by the client synchronously with a vertical sync signal generated in the HX8352-B01. If the interface speed and the wakeup period are well known, link wakeup based on VSYNC can be used to attain consistent display.

Figure below shows detailed timing on a link wakeup based on VSYNC.

GPIO based link wake-up

In VSYNC-based link wake-up, wake-up enable register setting prior to link shut-down. GPIO based Link wake-up is enabled by interrupt from outside of the IC. For GPIO based link wake-up, GPIO interrupt enable and GPIO PAD mode (to input mode) setting must be set. Once the HX8352-B01 receives interrupt, internal GPIO base link wake-up flag is set to high, and the following procedure is similar to that of VSYNC based link wake-up.

The following figure shows detailed timing for GPIO based link wake-up.

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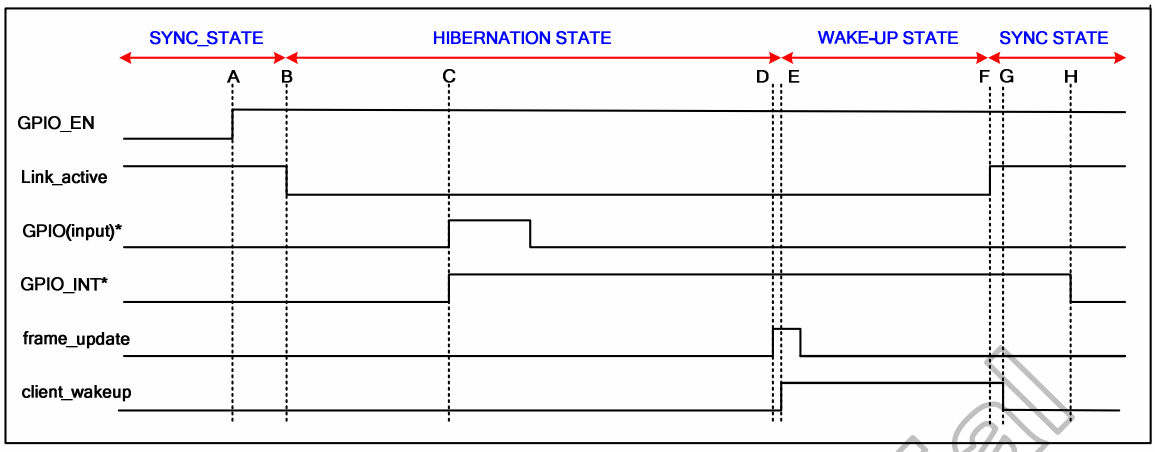

The detailed descriptions for labeled events are as follows:

A. Host send register access packet to sets GPIO clear interrupt register to disable clear interrupt (R6Fh:GPIO_CLR) and GPIO interrupt enable register (R6Dh: GPIO_EN) for a particular GPIO.
B. After host sending all data, Link goes into hibernation (and link_active goes low).
C. GPIO input goes high, and the GPIO interrupt (GPIO_INT) is latched.
D. Frame_update signal goes high indicating that the display has wrapped around. Link wake-up point can be set using WKF and WKL (R68h) registers.
E. Client_wakeup signal of the MDDI client goes high to start the client initiated link wake-up.
F. Link_active goes high after the host make link leaving hibernation.
G. After link wake-up, client_wakeup signal is reset to low.
H. MDDI host clears the interrupt by writing '0' to the register with the bit set for that particular interrupt (GPCLR: R6Fh). Between point G and H the host will have read the GPIO_INT values to see what interrupts are active.

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GPIO control

The HX8352-B01 offers 8 GPIO that can be used as input or output independently. Some application or device on the upper clamshell needs several control signals which are supplied by base band modem or application processor directly. If number of application on the upper clamshell increases, also control signals increase, causing the interface more costly. In HX8352-B01, GPIO can be the solution for that problem. User may control the 8 GPIOs as input or output by use of simple register setting. So additional connection between base band modem / AP (application processor) and components on upper clamshell are not needed.

The following table shows several set of register for GPIO.

Register	Width	Description		Reset Value
GPIO (6Bh)	[7:0]	Write	For GPIO output mode: output GPIO register value to GPIO PAD	8'h00
		Read	For GPIO input mode: read GPIO PAD status	
GPIO_CON (6Ch)	[7:0]	Write	GPIO PAD input/output mode control : (0 : input / 1 : output)	8'h00
		Read	GPIO_CON register value	
GPCLR (6Fh)	[7:0]	Write	For GPIO input mode: clear specified GPIO interrupt (set by GPIO PAD input).	8'h00
		Read	GPIO interrupt state (set by GPIO PAD input).	
GPIO_EN (6Dh)	[7:0]	Write	For GPIO input mode: enable specified GPIO interrupt	8'h00
		Read	GPIO_EN register value.	
GPPOL (6Eh)	[7:0]	Write	For GPIO input mode: GPIO interrupt polarity setting	8'hFF
		Read	GPPOL register value.	

Table 5.23 GPIO control related register

In GPIO output mode, the IC output GPIO (6Dh) register value to the defined PAD. Set GPIO_CON register as output mode before use GPIO output.

8 different GPIO output can be controlled simultaneously using 1-register access packet (6Dh register access) so that minimum access time for each GPIO output will be 1-register access time.
GPIO input mode can only be used as client-initiated link wake-up.

For more information, refer to GPIO based link wake-up section.

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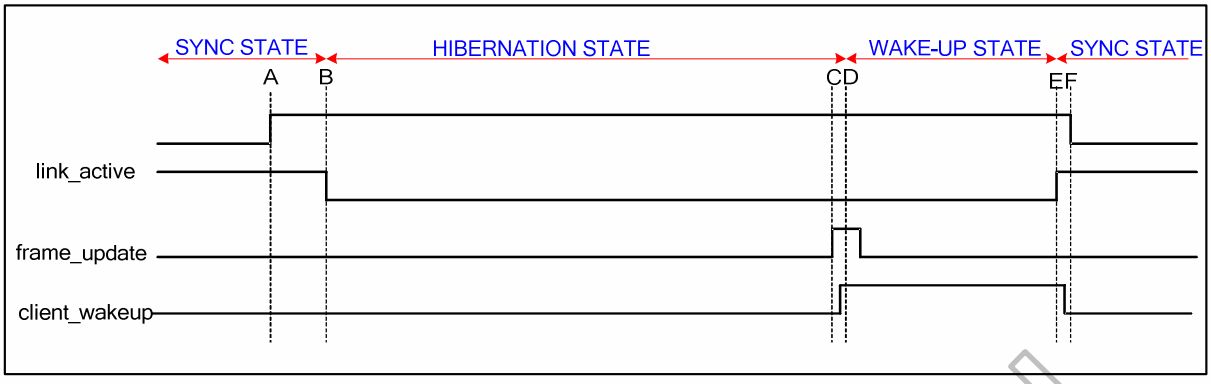

The detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.
B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the HX8352-B01.
C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up point can be set using WKF and WKL (R68h~R69h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.
D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.
E. link_active goes high after the host brings the link out of hibernation.
F. After link wake-up, client_wakeup signal and the VWAKE register are cleared automatically.

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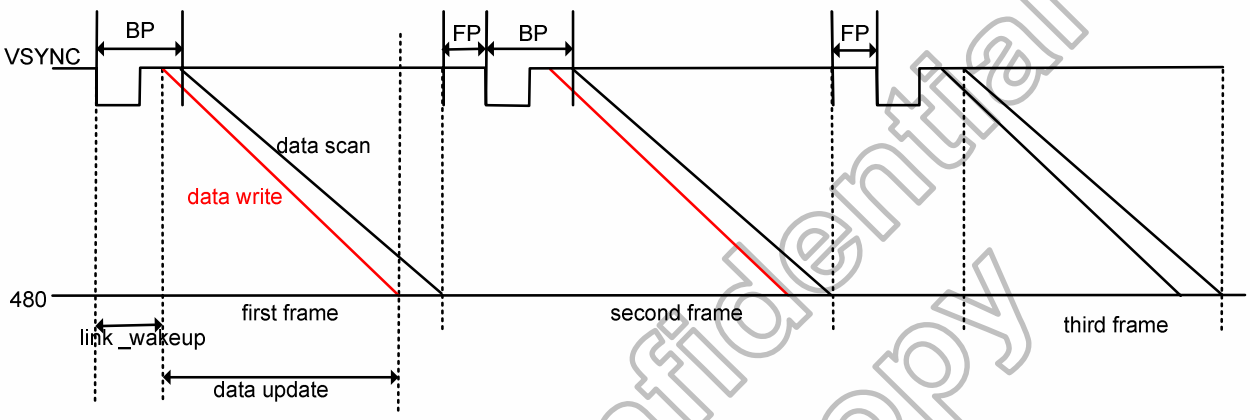
5.2.3.10 VSYNC mode in MDDI (host initiated wake-up)

VSYNC mode in MDDI can enable host initiated wakeup. In this mode, wake up from hibernation state need no special signal. Host only sends wakeup signal & data synchronizing with VSYNC signal. To operate VSYNC mode, MY, MX, MY bit (R16h) must set to '000'. Next figures show timing for data writing to GRAM and displaying read data.

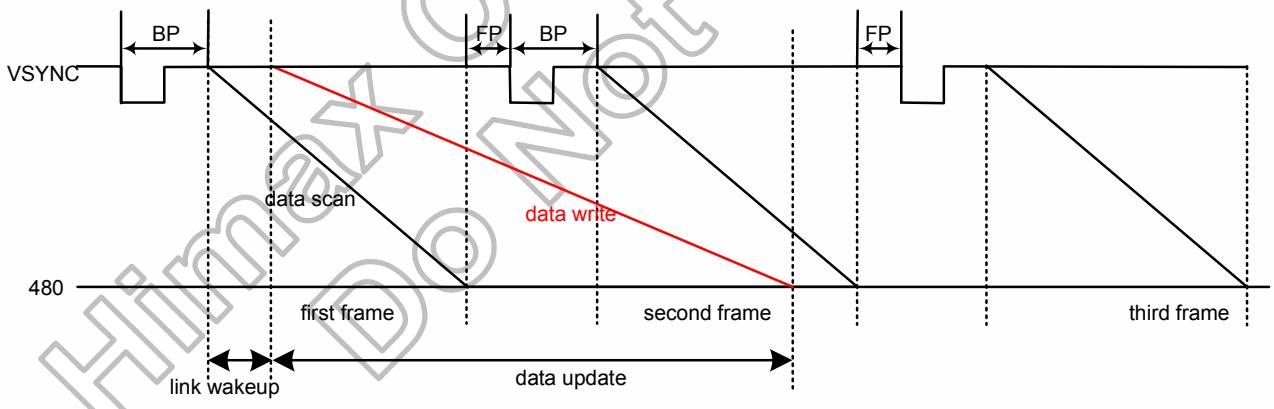
When data writing is completed within on frame

This case is that MPU write speed faster Panel Read speed



When completion of data writing takes one frame or more period:

This case is that MPU write speed slower Panel Read speed



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5.2.3.11 MDDI operation mode

The MDDI Link supports six operation modes, the mode flow is illustrated as below.

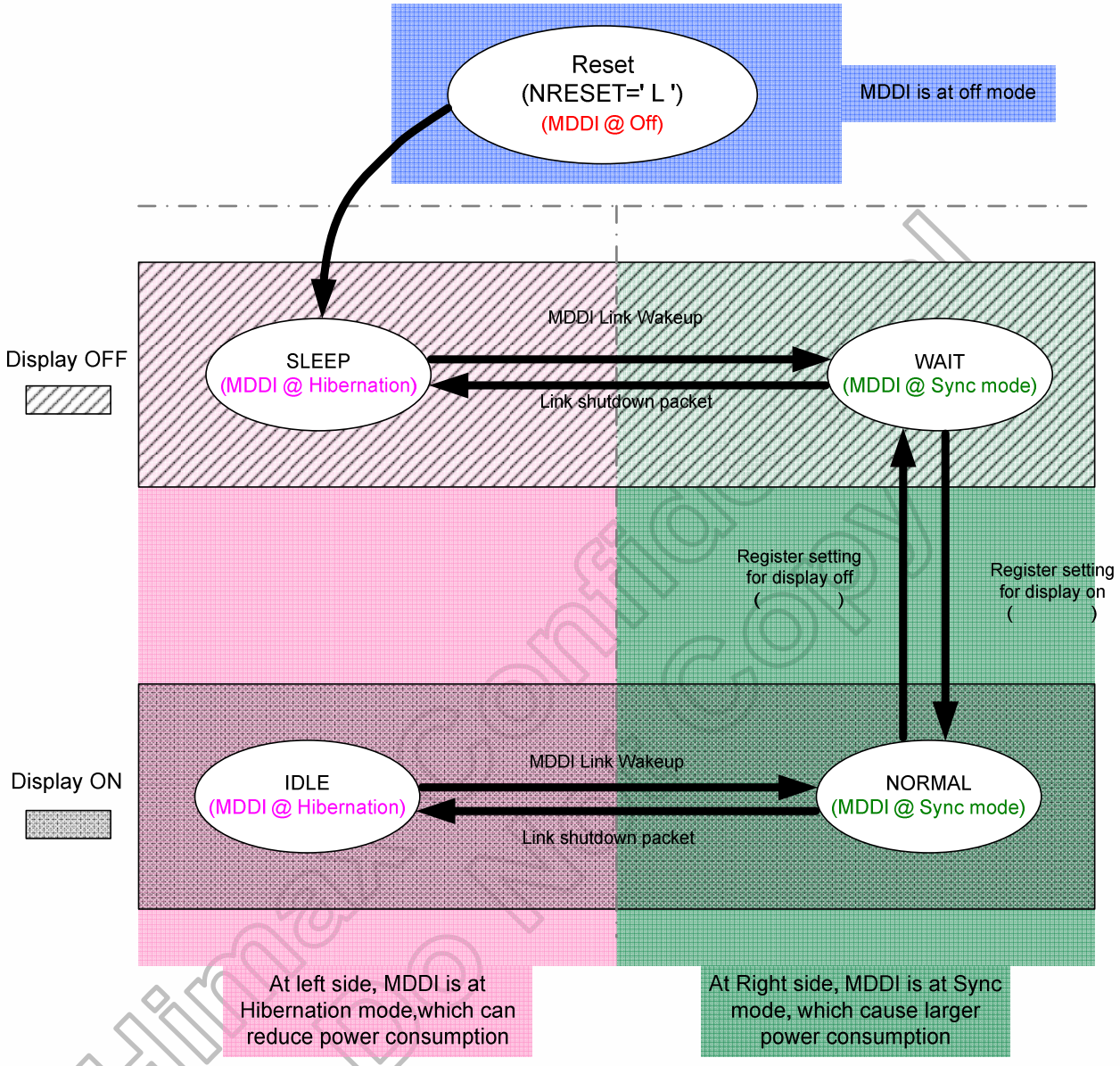

Figure 5.50 MDDI operation mode

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The MDDI Link supports five operation modes listed in Table below

Function	RESET	SLEEP	WAIT	NORMAL	IDLE
MDDI hibernation receiver	OFF	ON	OFF	OFF	ON
MDDI normal receiver or normal driver	OFF	OFF	ON	ON	OFF
Register and RAM access	Disable	Disable	Enable	Enable	Disable
Internal oscillator(OSC)	OFF	OFF	ON/OFF(1)	ON(2)	ON(2)
Booster(VVLCD,VGH,VGL,VCL)	OFF	OFF	OFF	ON	ON
Regulator (VCOMH,VCOML,VREG1)	OFF	OFF	OFF	ON	ON

Note: (1) If OSC_EN = 0 is OFF, and if OSC_EN = 1 is ON.
(2) Do not set OSC_EN = 1 in Normal mode, If OSC stopped, indication also stops.

Table 5.24 Operation mode list

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5.2.3.12 Sub panel interface

The MDDI Link supports six operation modes, the mode flow is illustrated as below.

The HX8352-B01 supports the Sub Panel interface which connected to Sub Panel driver IC with Parallel Interface. When the HX8352-B01 receives MDDI packets from host device, the HX8352-B01 will convert MDDI packet to parallel data and send to sub panel driver IC.

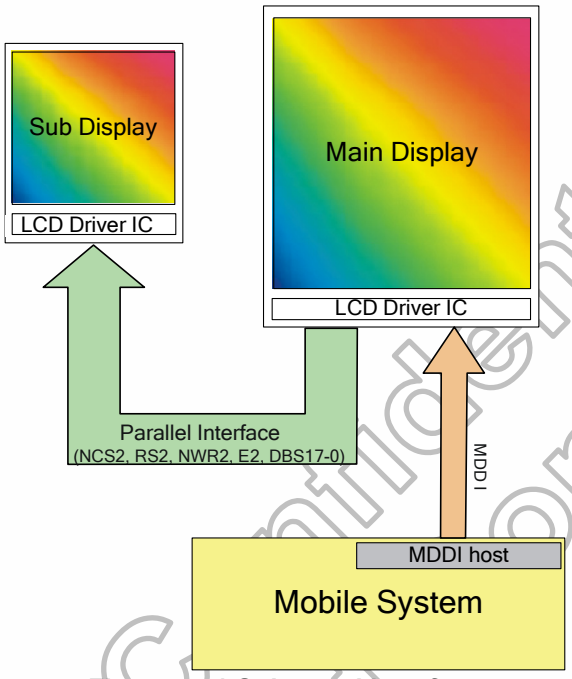

Figure 5.51 Sub panel interface

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5.2.3.13 Sub panel function

When the register access packet is received, then following register access packets or video stream packets are transferred to the sub panel via Sub Panel Interface. Sub panel selection address (R72h) can be changed by setting register SUB_SEL. The SUB_SEL value must be set to unused address in both Main/Sub Panel Driver IC. If video data is transferred to the sub panel driver IC via the Sub Panel Interface, additional RAM Index (default 0022h) is automatically generated by HX8352-B01.

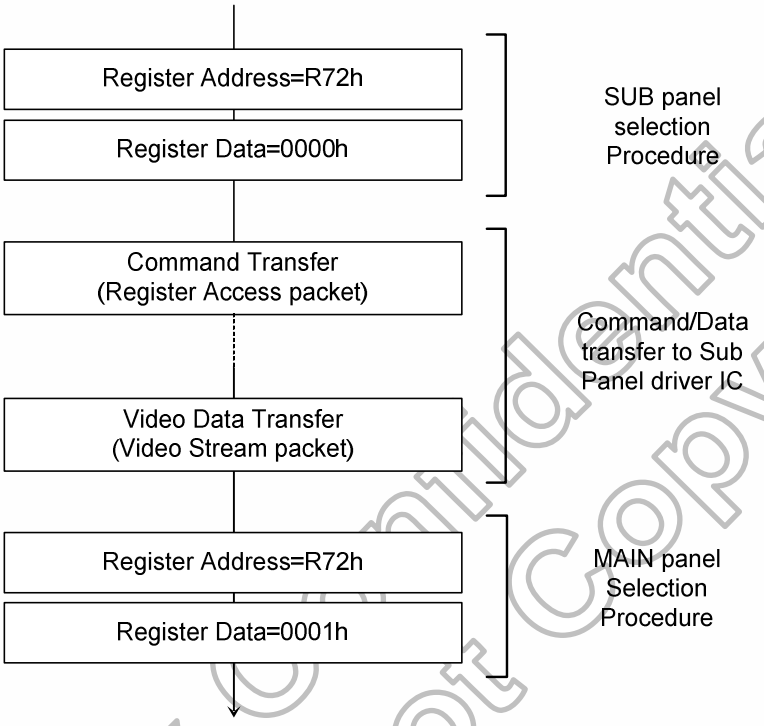

Figure 5.52 Main/sub panel selection procedure

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5.2.3.14 Sub panel interface timing

The HX8352-B01's Sub Panel Interface is supports two type panel (TFT and STN) and offer 18-/16-/9-/8-bit interface format (i80 and m68 system).

TFT type sub panel timing

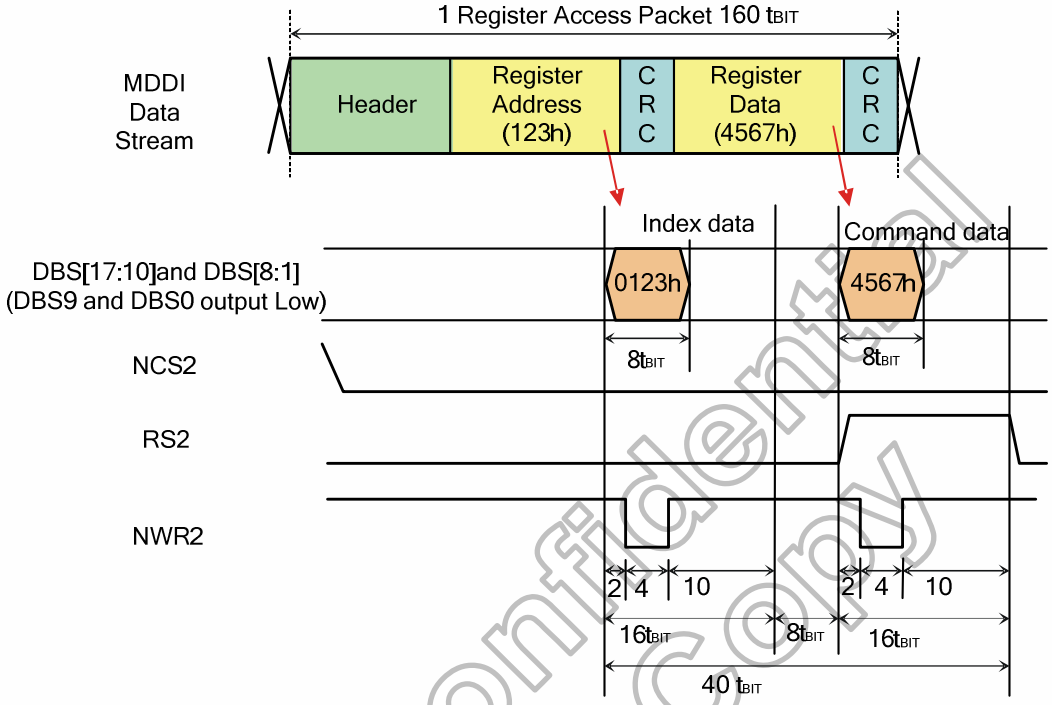

Figure 5.53 18-/16-bit sub panel interface register access data timing for I80 series TFT sub panel

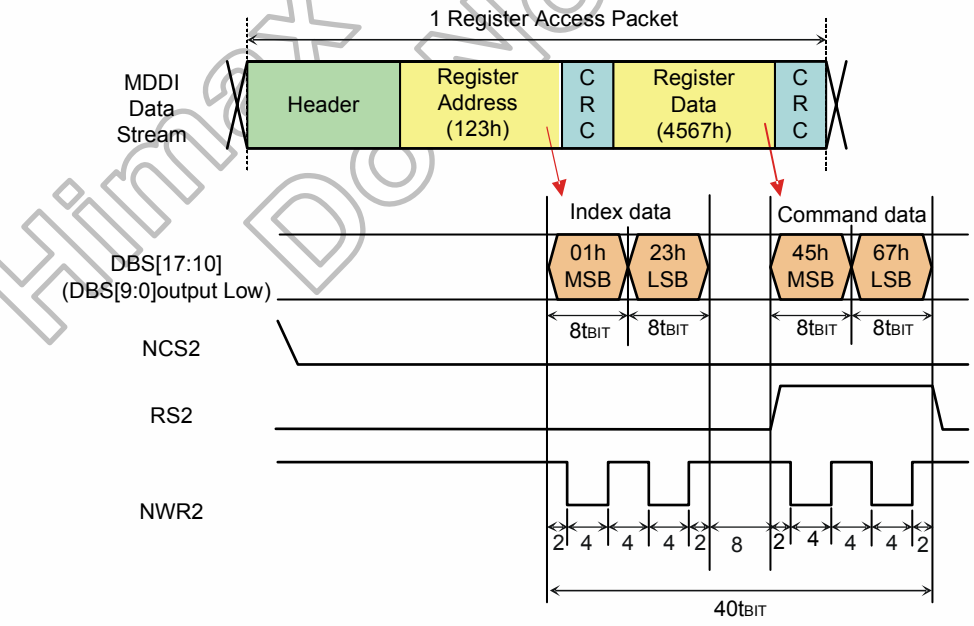

Figure 5.54 9-/8-bit sub panel interface register access data timing for I80 series TFT sub panel

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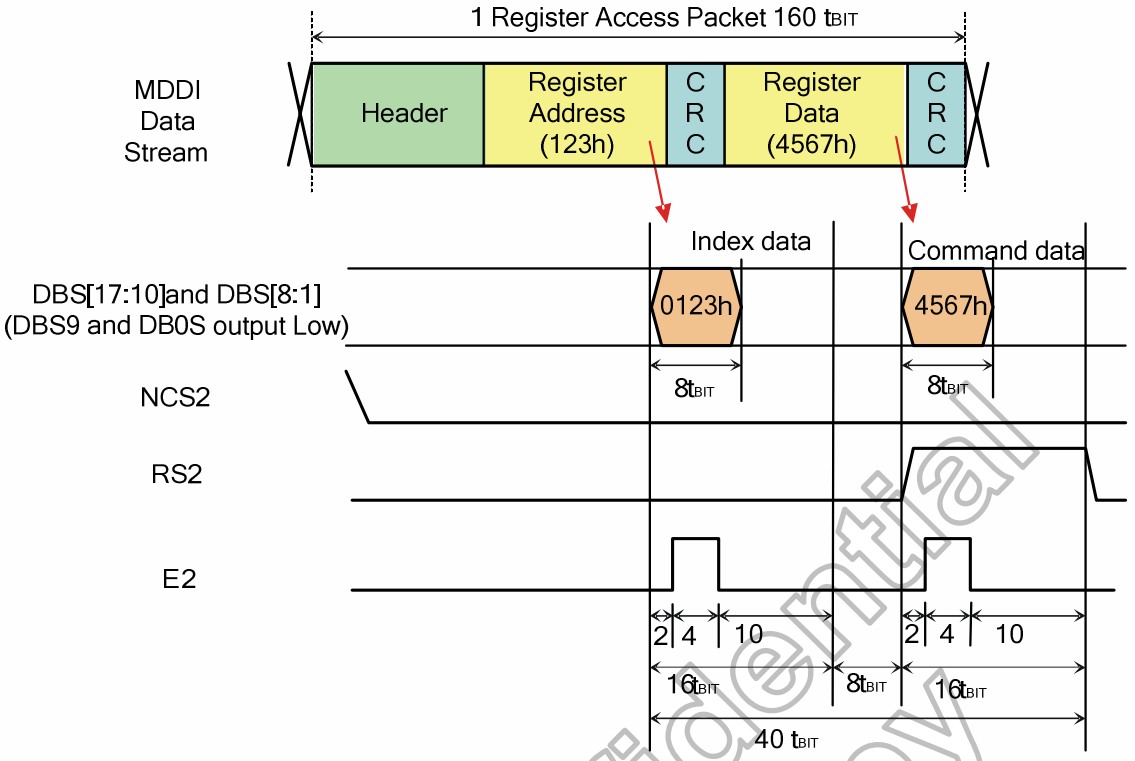

Figure 5.55 18-/16-bit sub panel interface register access data timing for I80 series TFT sub panel

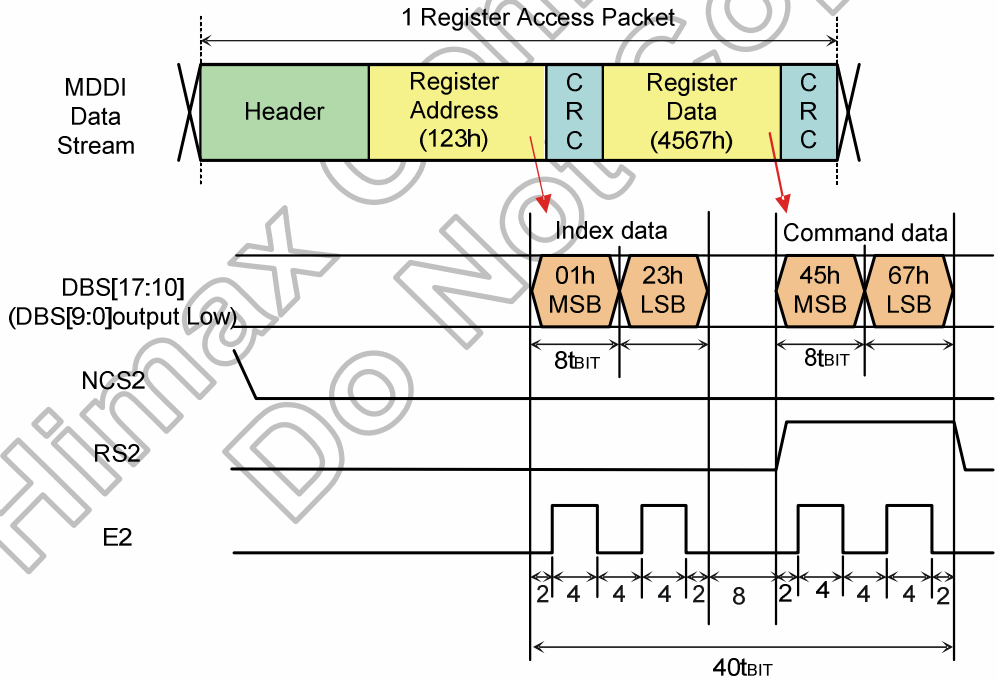

Figure 5.56 9-/8-bit sub panel interface register access data timing for M68 series TFT sub panel

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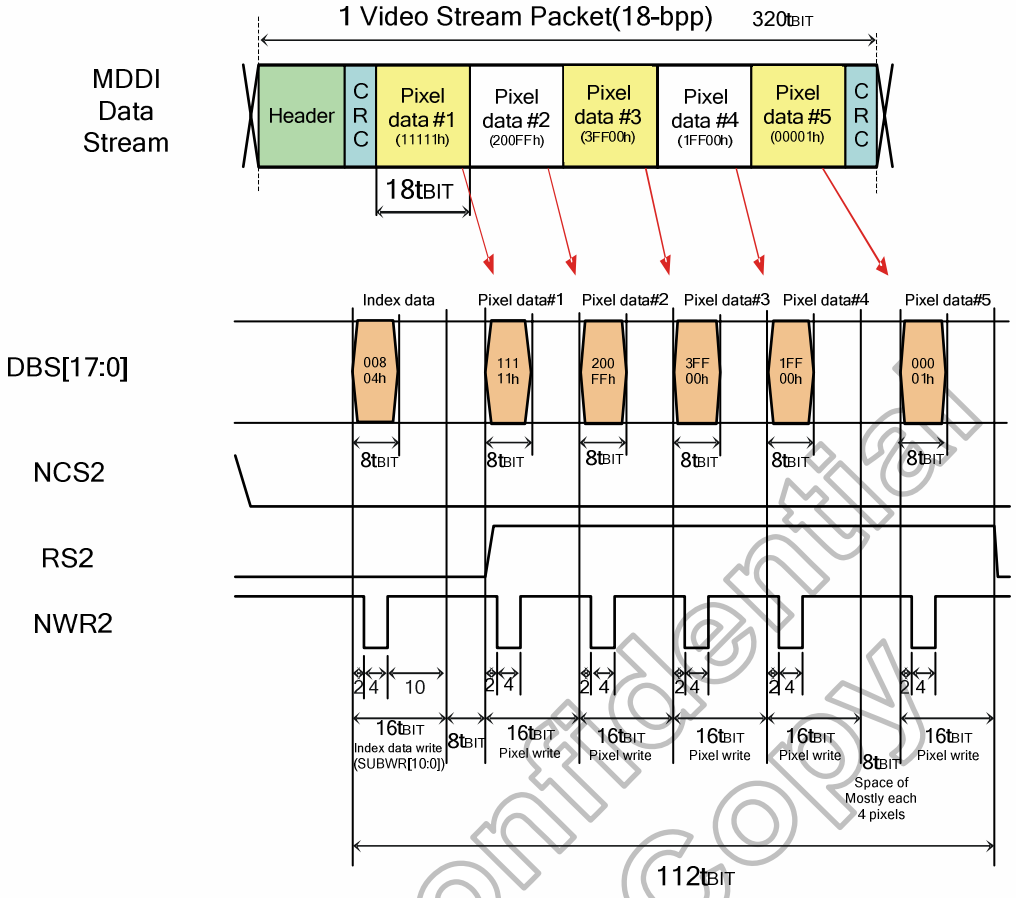

Figure 5.57 18-bit sub panel interface video data timing for I80 series TFT sub panel

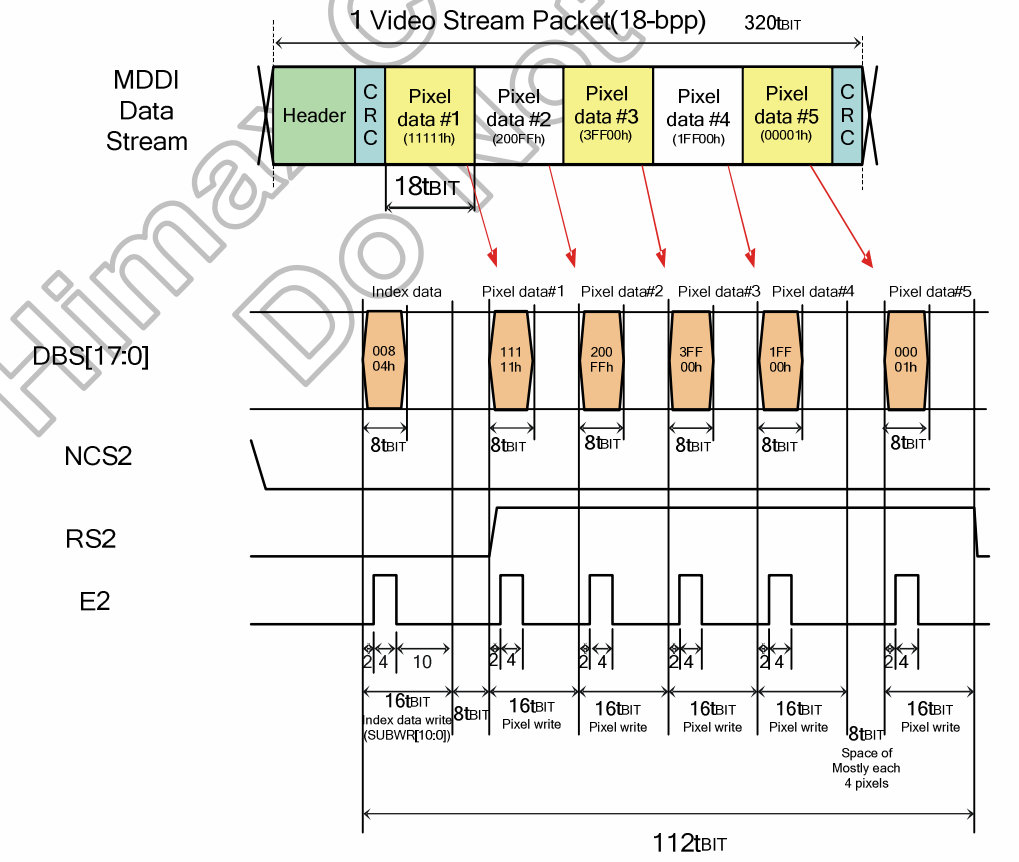

Figure 5.58 18-bit sub panel interface video data timing for M68 series TFT sub panel

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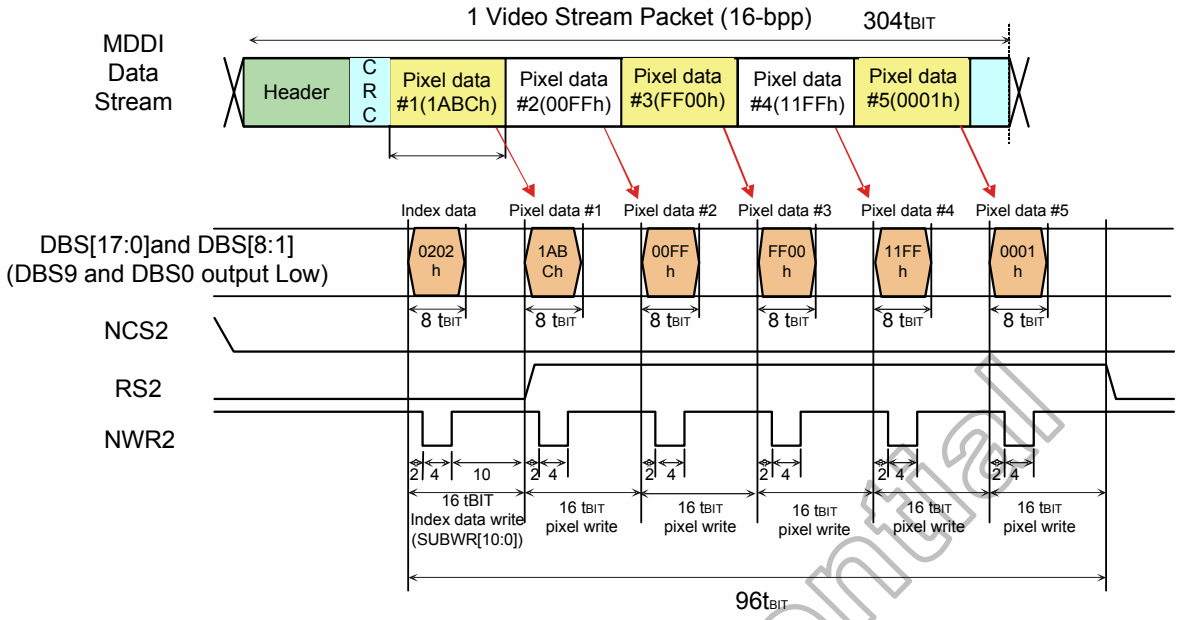

Figure 5.59 16-bit sub panel interface video data timing for I80 series TFT sub panel

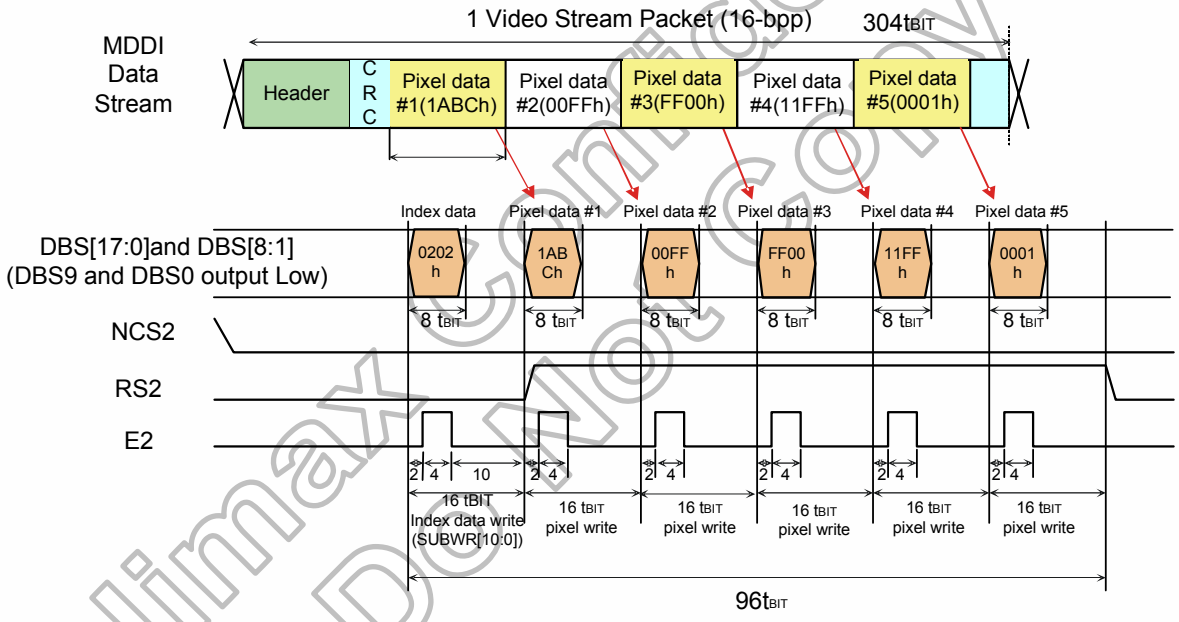

Figure 5.60 16-bit sub panel interface video data timing for M68 series TFT sub panel

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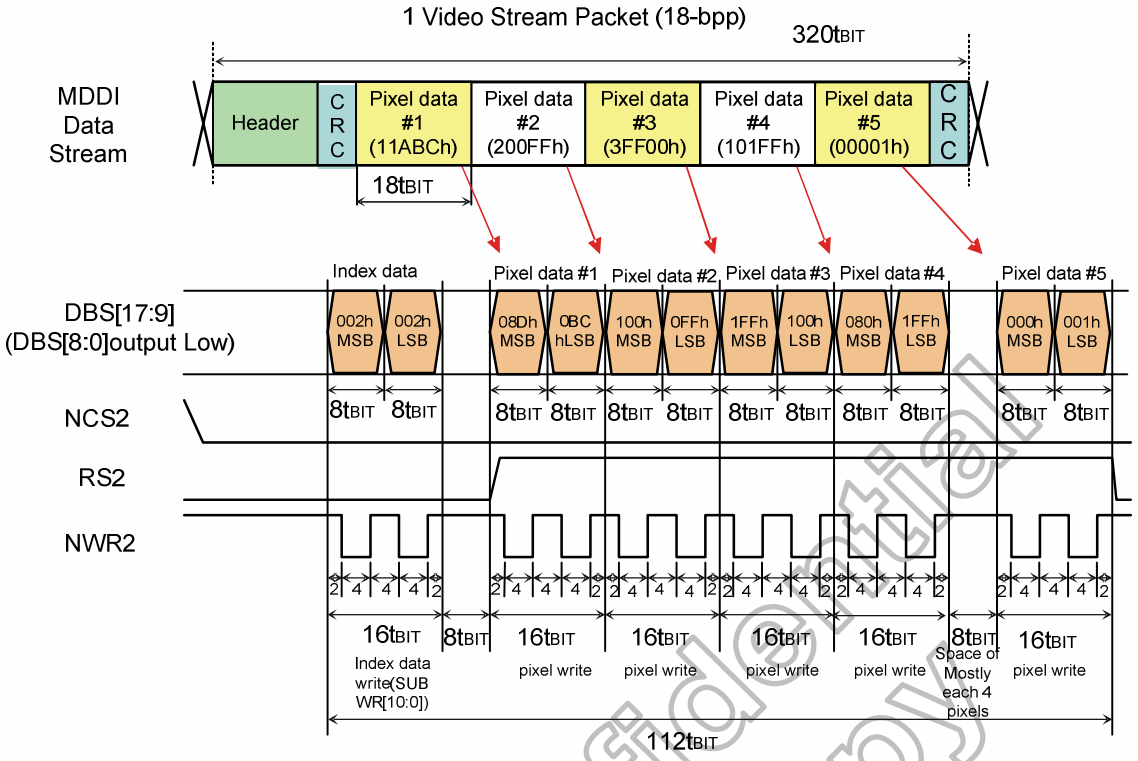

Figure 5.61 9-bit sub panel interface video data timing for I80 series TFT sub panel

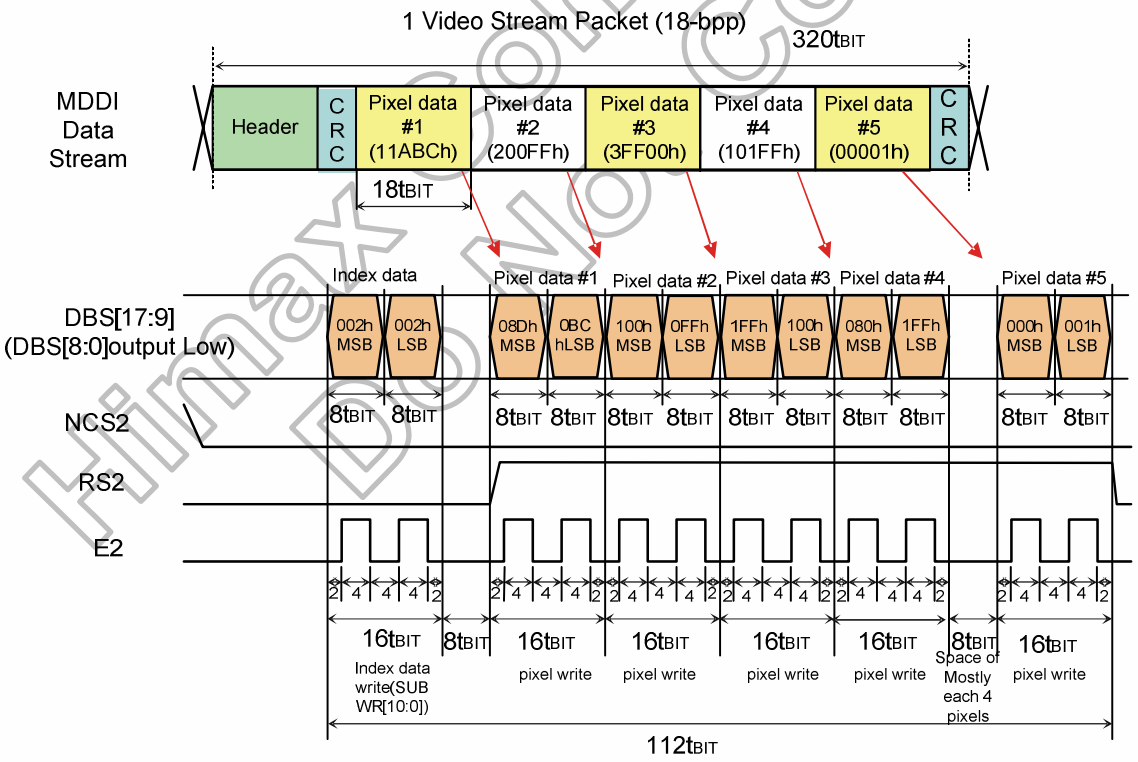

Figure 5.62 9-bit sub panel interface video data timing for M68 series TFT sub panel

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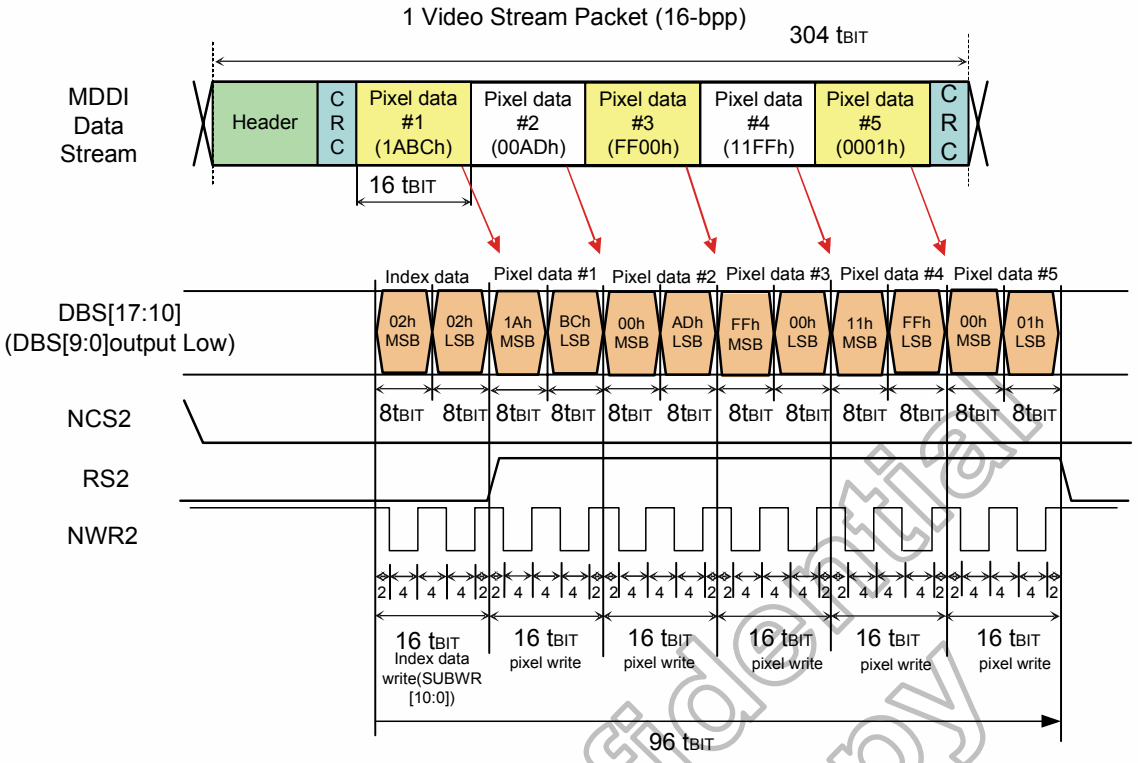

Figure 5.63 8-bit sub panel interface video data timing for I80 series TFT sub panel

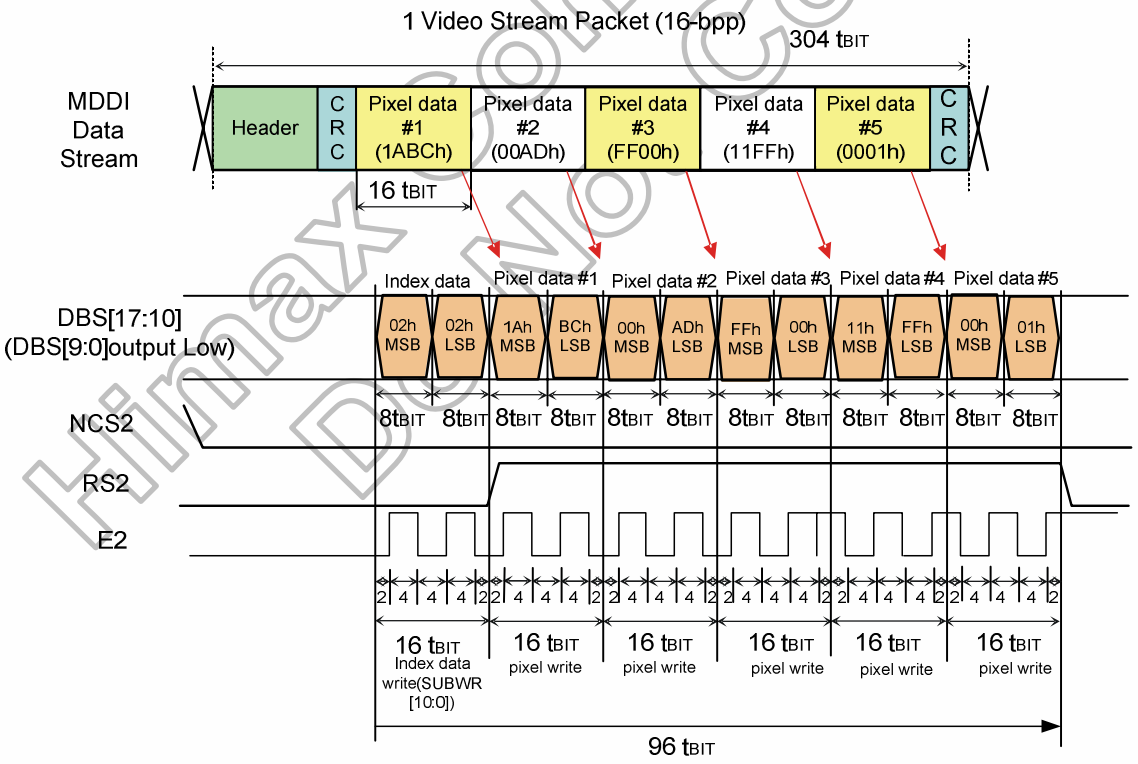

Figure 5.64 8-bit sub panel interface video data timing for M68 series TFT sub panel

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STN type sub panel timing

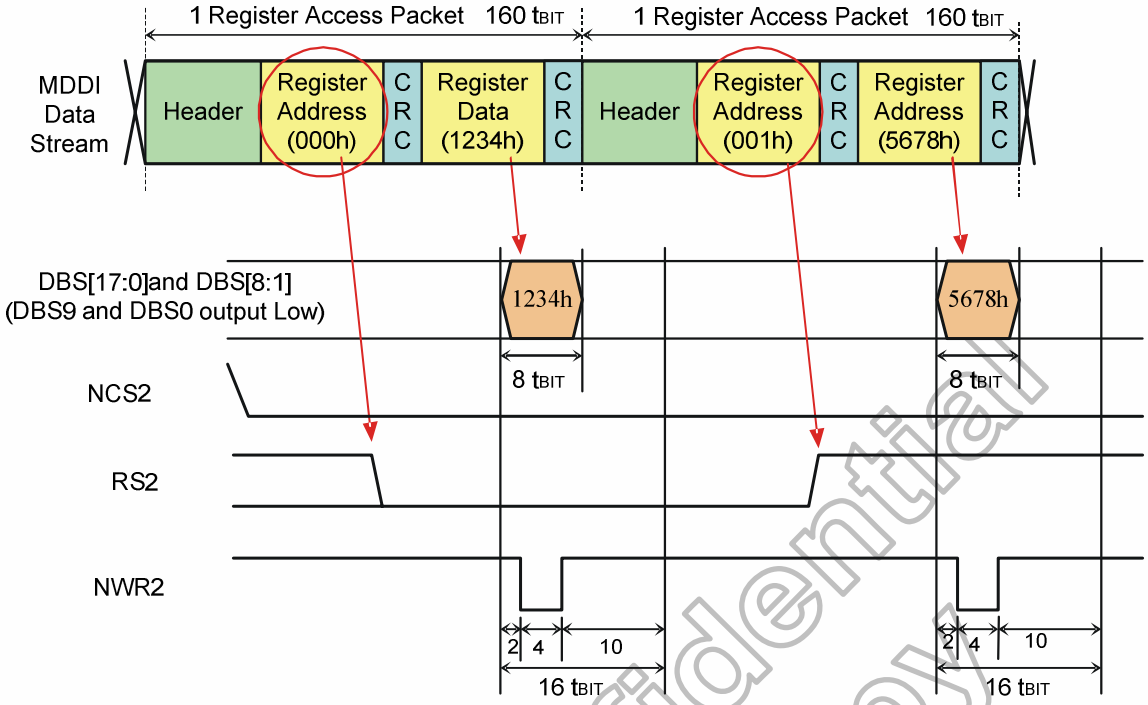

Figure 5.65 18-/16-bit sub panel interface register access data timing for I80 series STN sub panel

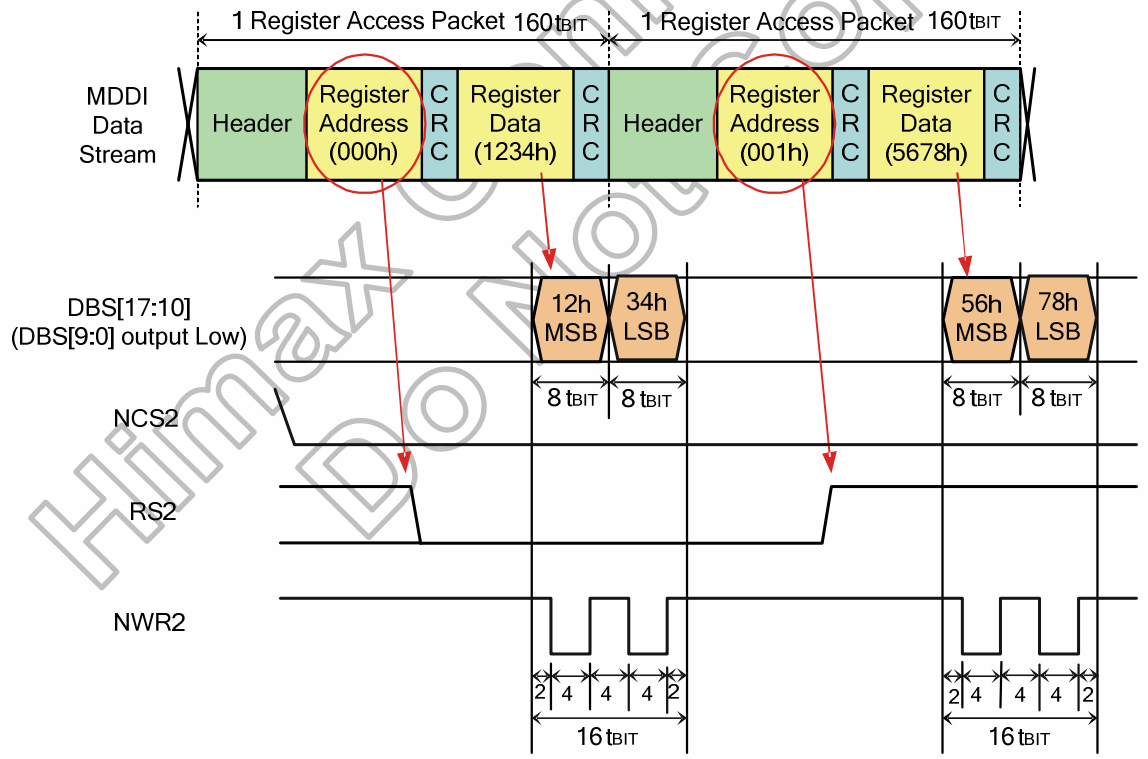

Figure 5.66 9-/8-bit sub panel interface register access data timing for I80 series STN sub panel

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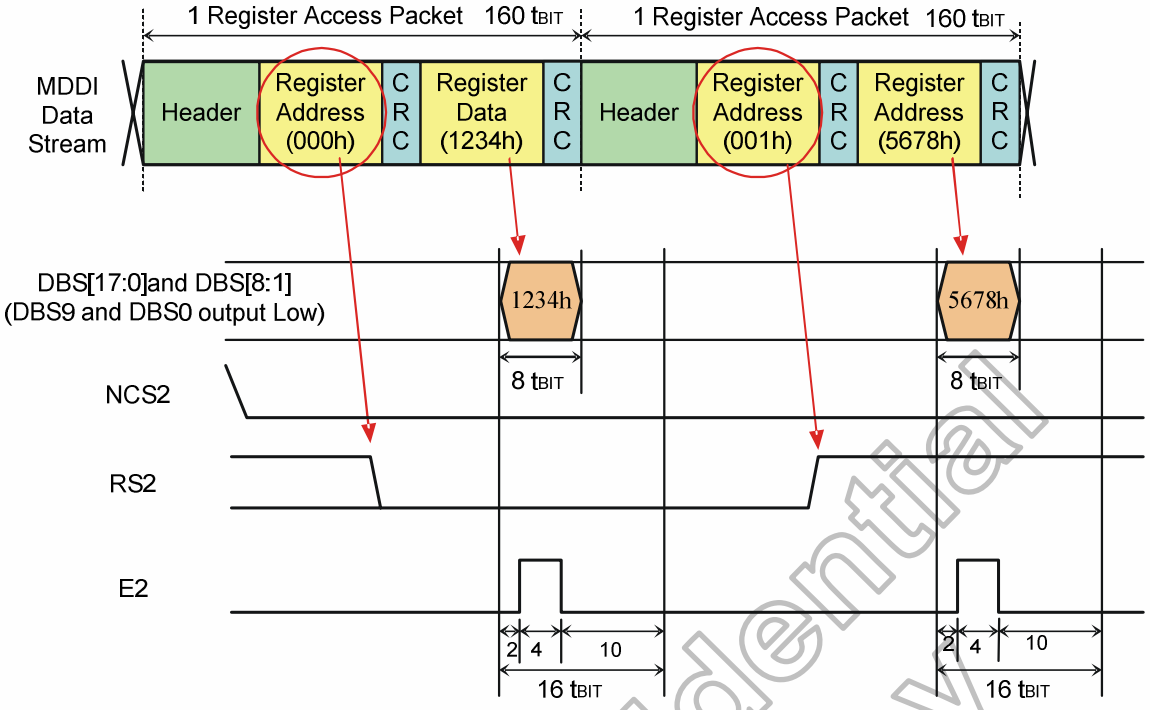

Figure 5.67 18-/16-bit sub panel interface register access data timing for M68 series STN sub panel

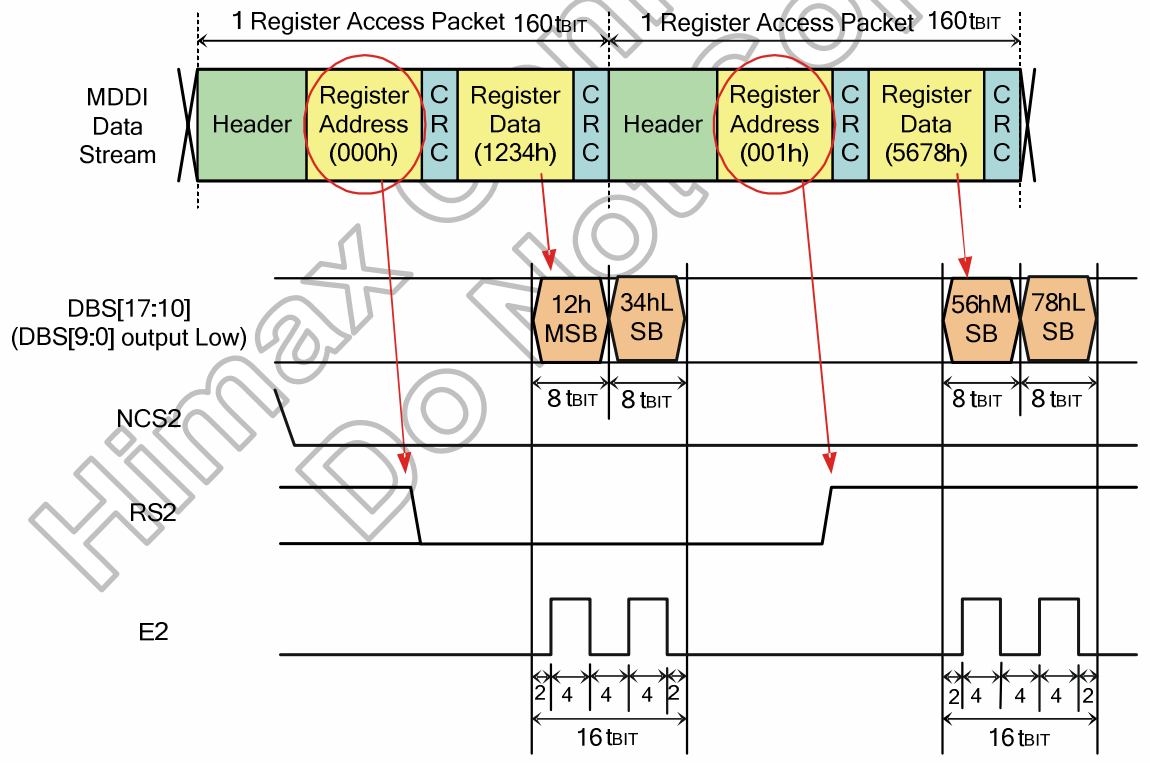

Figure 5.68 9-/8-bit sub panel interface register access data timing for M68 series STN sub panel

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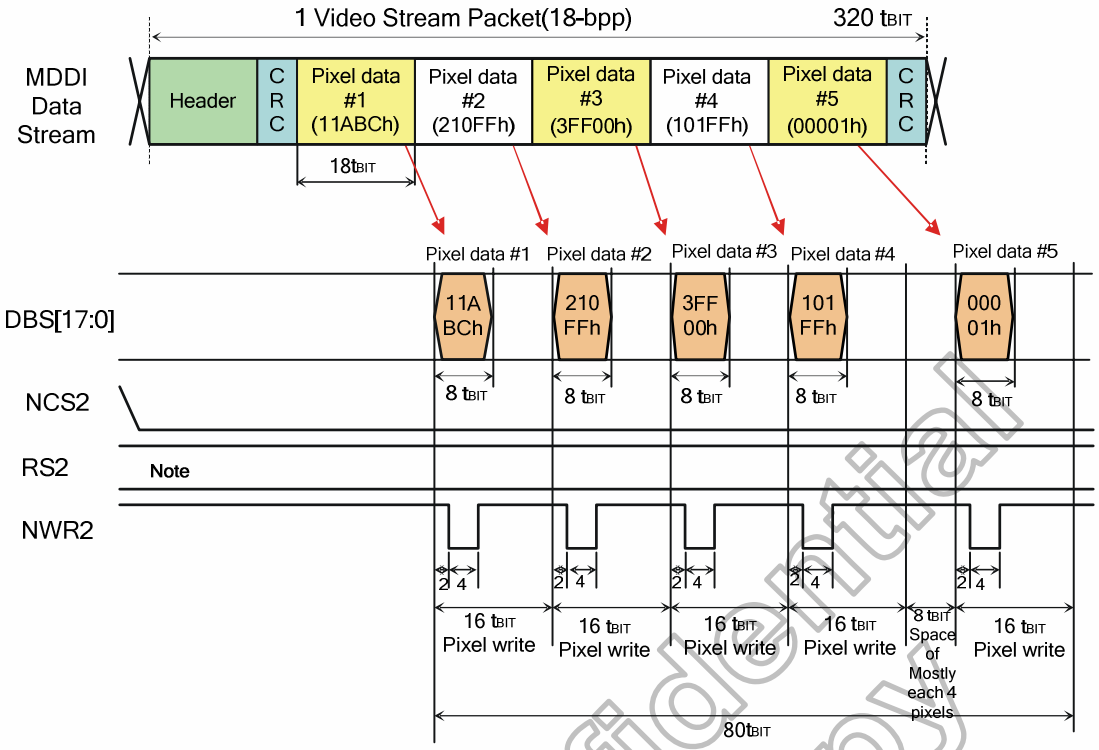
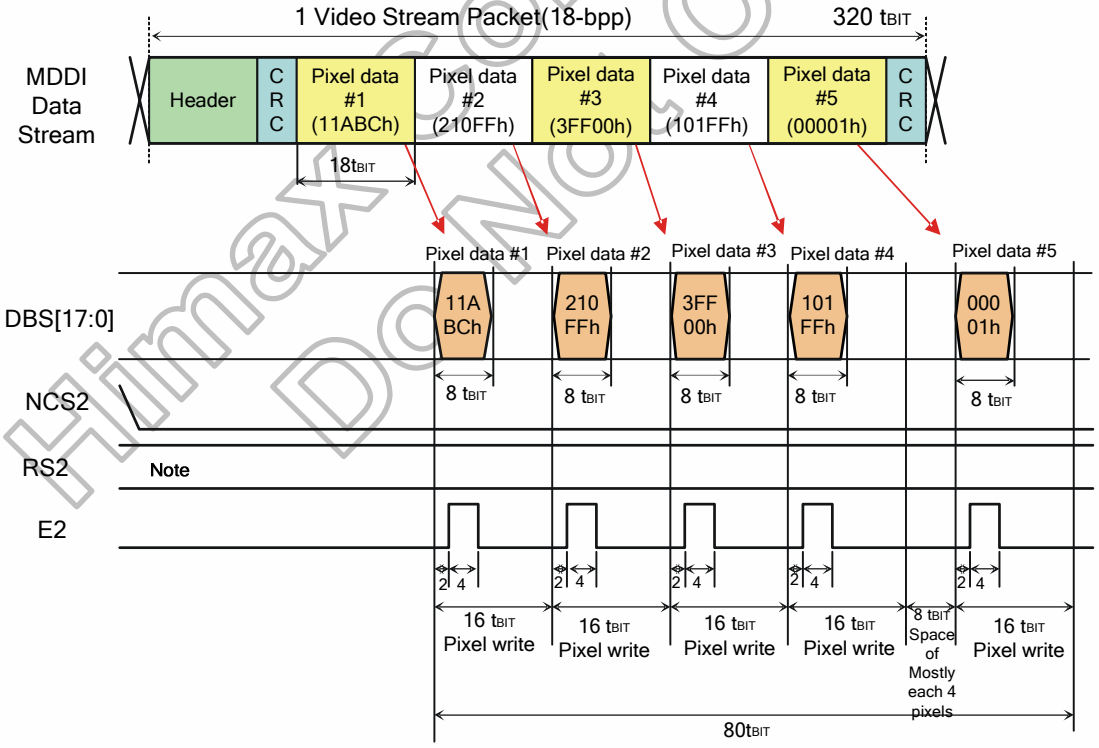


Note: The status RS2 output is specified by SUBRS[1:0] bit of index:020h

Figure 5.69 18-bit sub panel interface video data timing for I80 series STN sub panel



Note: The status RS2 output is specified by SUBRS[1:0] bit of index:020h

Figure 5.70 18-bit sub panel interface video data timing for M68 series STN sub panel

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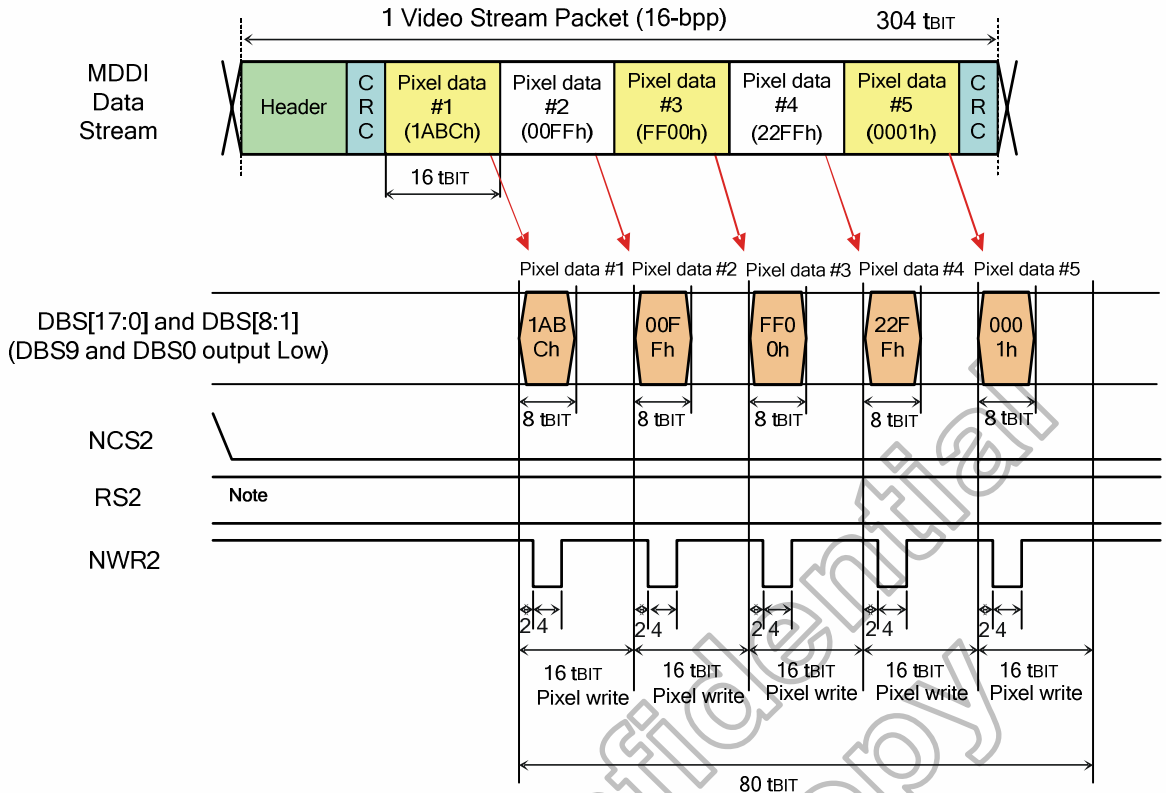
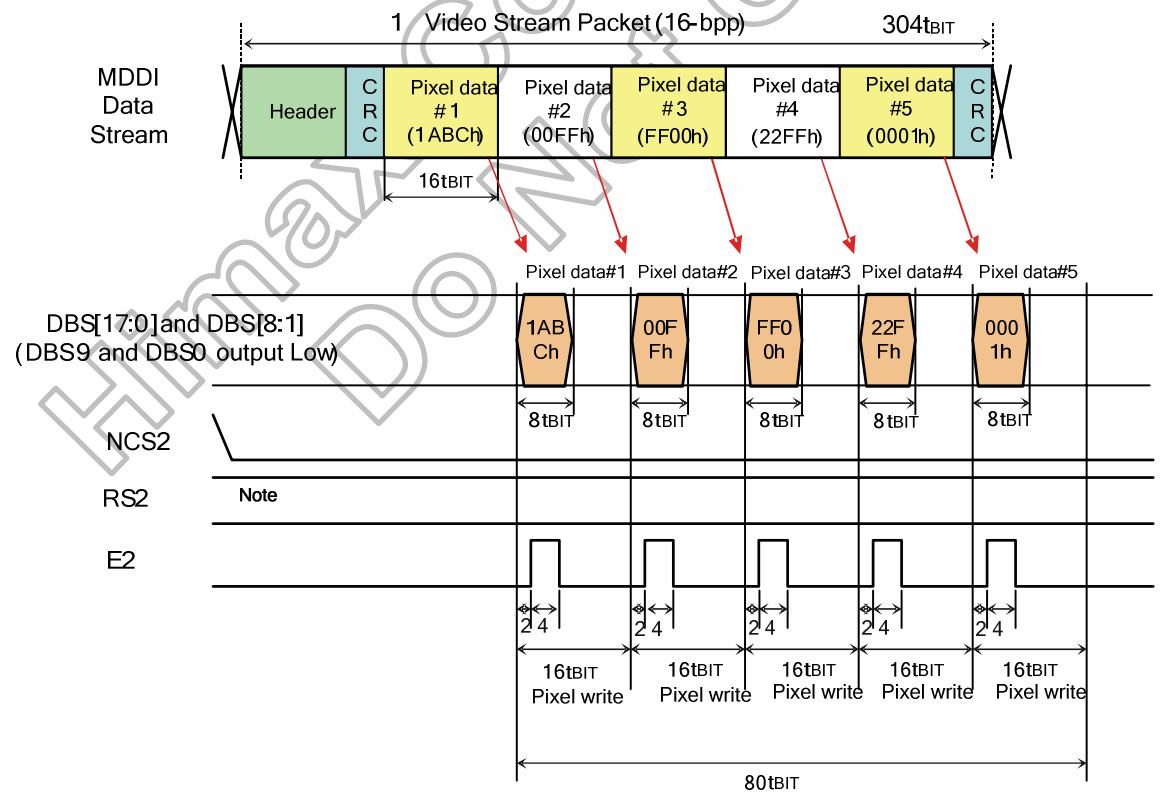


Note : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.71 16-bit sub panel interface video data timing for I80 series STN sub panel



Note : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.72 16-bit sub panel interface video data timing for M68 series STN sub panel

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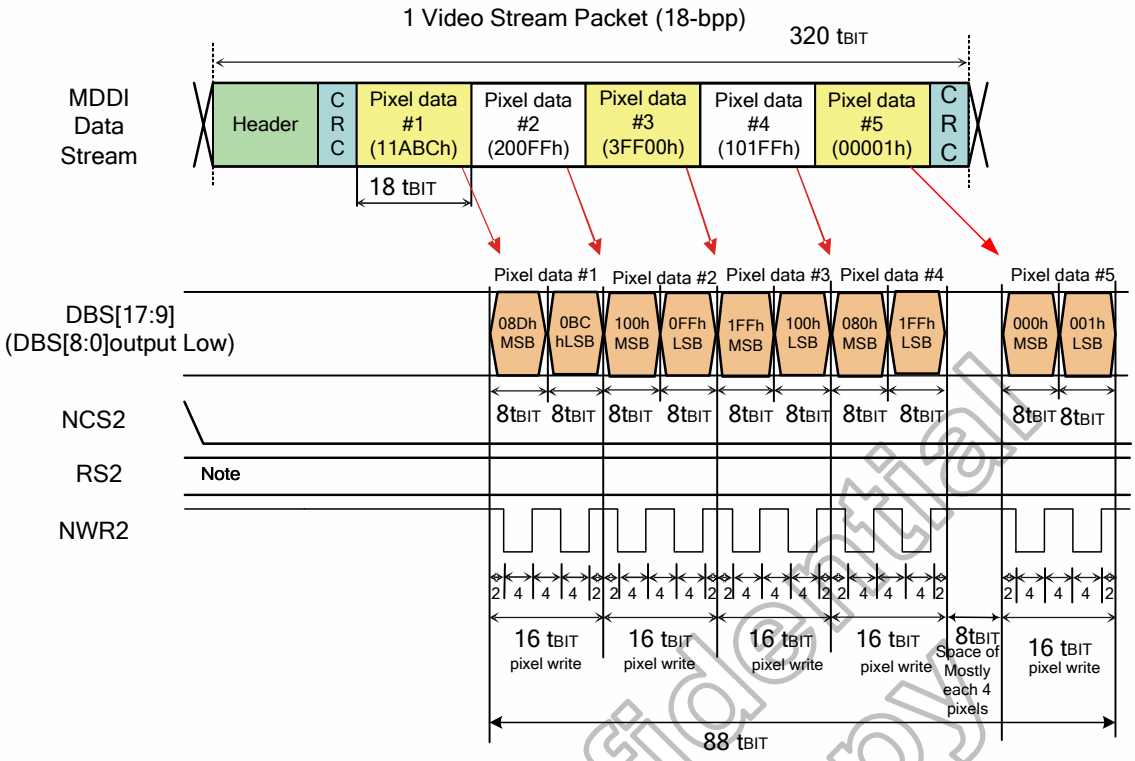
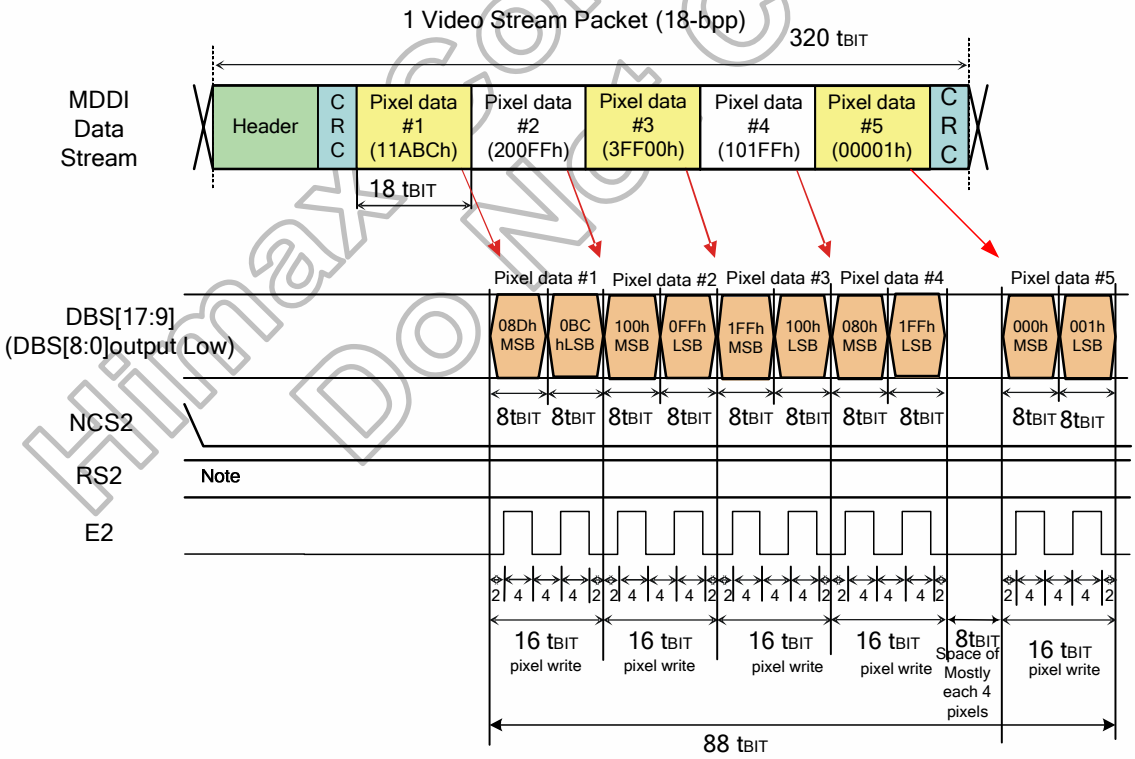


Note : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.73 9-bit sub panel interface video data timing for I80 series STN sub panel



Note : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.74 9-bit sub panel interface video data timing for M68 series STN sub panel

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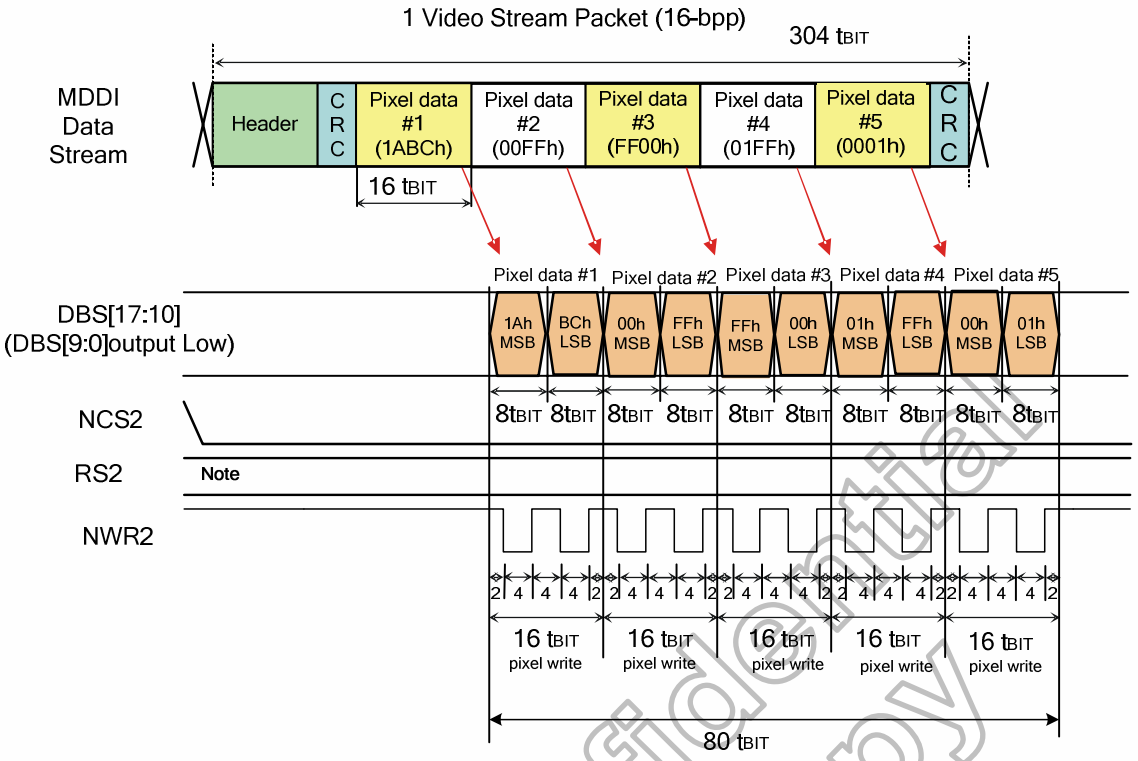
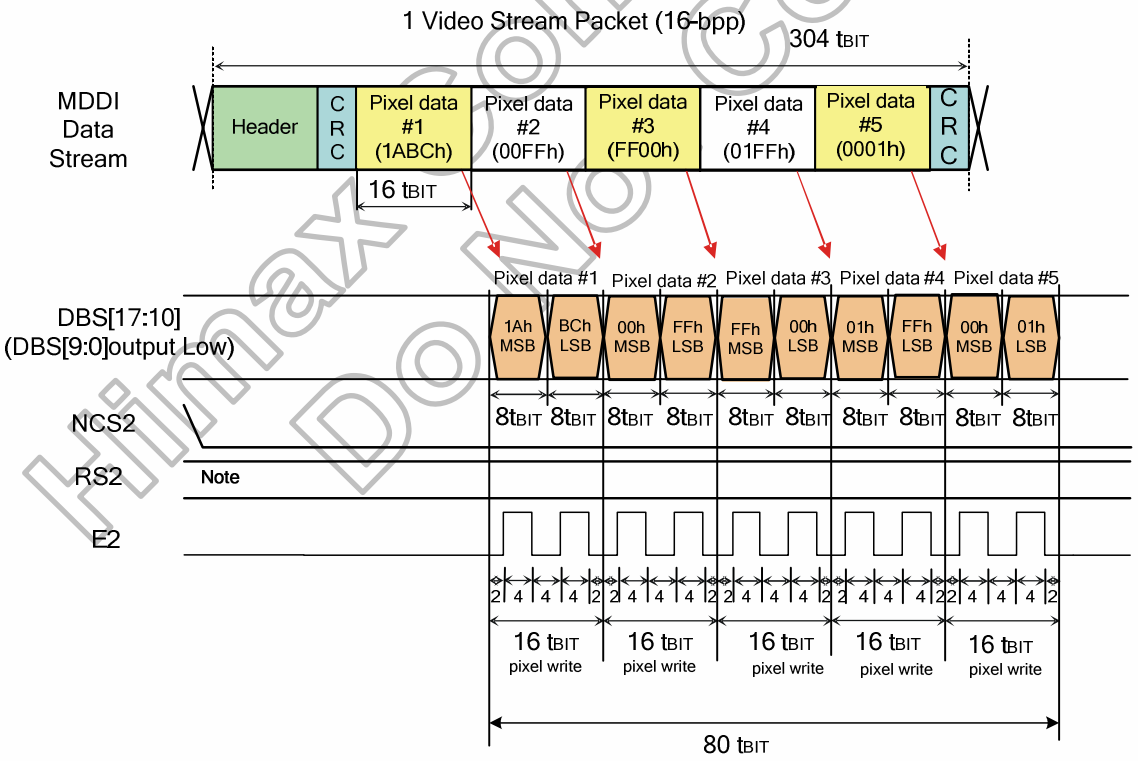


Note： The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.75 8-bit sub panel interface video data timing for I80 series STN sub panel



Note： The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5.76 8-bit sub panel interface video data timing for M68 series STN sub panel

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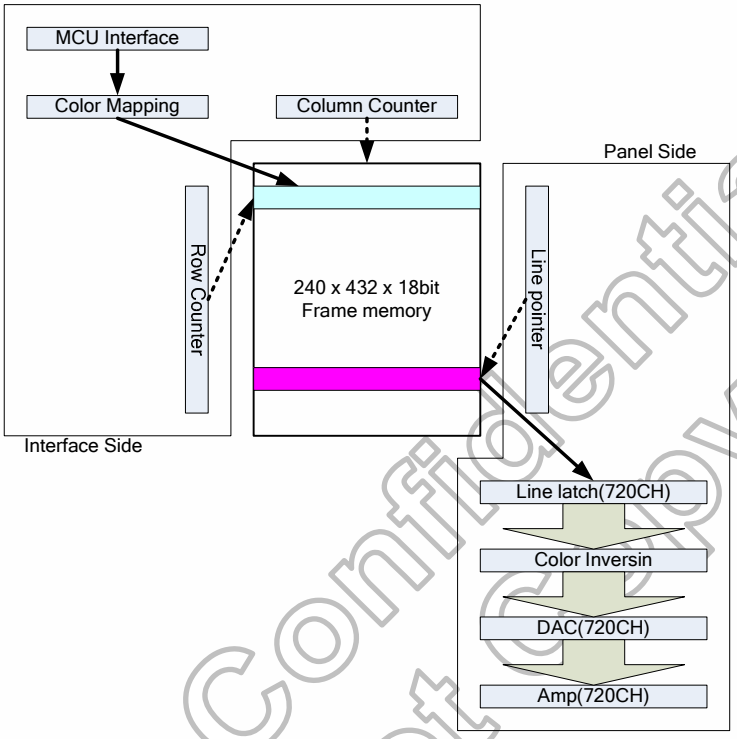
6. Display Data GRAM

The display data RAM stores display dots and consists of 1,866,240 bits (240x432x18bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



6.1 Display data GRAM mapping

Every pixel (18-bit) data in GRAM is located by a (Row, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting R22h commands from start positions of the window address.

(000,000)H	(000,001)H	(000,002)H	---------	(000,EC)H	(00,ED)H	(000,EE)H	(000,EF)H
(001,000)H	(001,001)H	(001,002)H	---------	(001, EC)H	(01, ED)H	(001,EE)H	(001, EF)H
(002,000)H	(002,001)H	(002,002)H	---------	(002, EC)H	(02, ED)H	(002,EE)H	(002, EF)H
(003,000)H	(003,001)H	(003,002)H	---------	(003, EC)H	(03, ED)H	(003,EE)H	(003, EF)H
(004,000)H	(004,001)H	(004,002)H	---------	(004, EC)H	(04, ED)H	(004,EE)H	(004, EF)H
(005,000)H	(005,001)H	(005,002)H	---------	(005, EC)H	(05, ED)H	(005,EE)H	(005, EF)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(1AA,000)H	(1AA,001)H	(1AA,002)H	---------	(1AA, EC)H	(1AA, ED)H	(1AA,EE)H	(1AA, EF)H
(1AB,000)H	(1AB,001)H	(1AB,002)H	---------	(1AB, EC)H	(1AB, ED)H	(1AB,EE)H	(1AB, EF)H
(1AC,000)H	(1AC,001)H	(1AC,002)H	---------	(1AC, EC)H	(1AC, ED)H	(1AC,EE)H	(1AC, EF)H
(1AD,000)H	(1AD,001)H	(1AD,002)H	---------	(1AD, EC)H	(1AD, ED)H	(1AD,EE)H	(1AD, EF)H
(1AE,000)H	(1AE,001)H	(1AE,002)H	---------	(1AE, EC)H	(1AE, ED)H	(1AE,EE)H	(1AE, EF)H
(1AF,000)H	(1AF,001)H	(1AF,002)H	---------	(1AF, EC)H	(1AF, ED)H	(1AF,EE)H	(1AF, EF)H

Table 6.1 GRAM address for display panel position (240 X 432)

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6.2 Address counter (AC) of GRAM

The HX8352-B01 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers register (**CAC** and **RAC**) can set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

The address pointers set the position of GRAM whose addresses range:

RES_SEL1	RES_SEL0	MV	X Range	Y Range	Panel Resolution
1	1	-	-	-	Ignore
1	0	0	0~239d.	0~431d.	240RGB x 432 dot
		1	0~431d.	0~239d.	
0	1	0	0~239d.	0~399d.	240RGB x 400 dot
		1	0~399d.	0~239d.	
0	0	0	0~239d.	0~319d.	240RGB x 320 dot
		1	0~319d.	0~239d.	

Table 6.2 Address counter range

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6.2.1 System interface to GRAM write direction

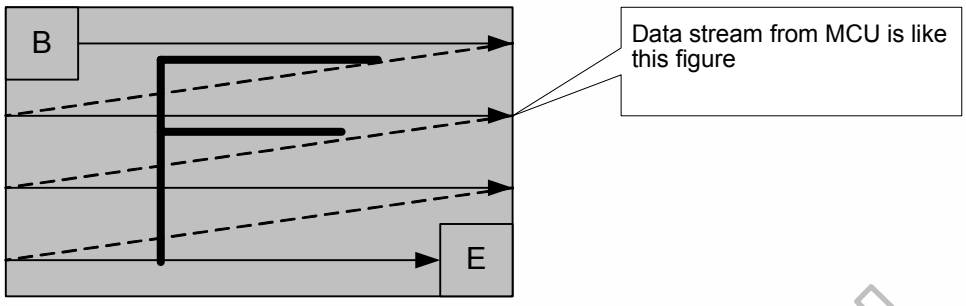

Figure 6.1 Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting.

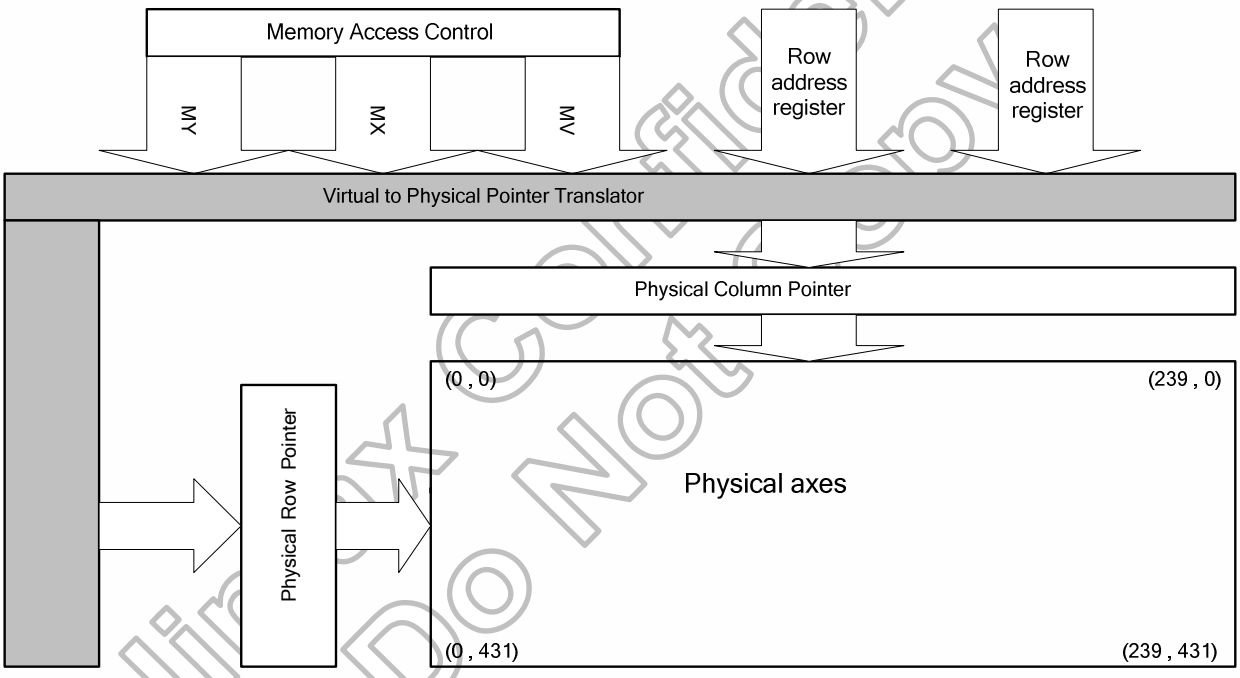

Figure 6.2 MY, MX, MV setting of 240RGB x 432 dot

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6.3 CASET and PASET control for physical column/page pointers

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For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Do not return to "Start Column"(2)	Do not Return to "Start Page"(2)
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: (1) Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MX, MY, MV.
(2) When RAMWR/RAMRD CMD is accepted, then Page counter and page counuter do not return to start counter automatically. Unless re-set CAC and RAC before RAMWR / RAMRD CMD.

Table 6.4 Rules for updating GRAM order

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The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

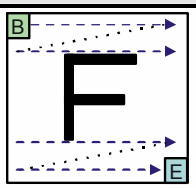
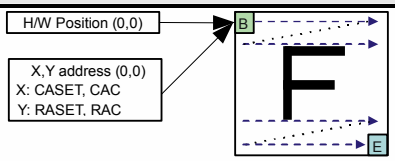
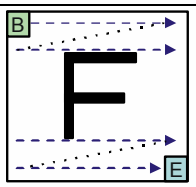
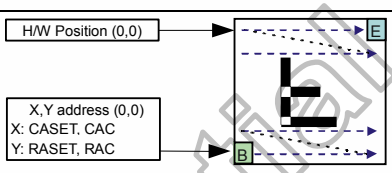
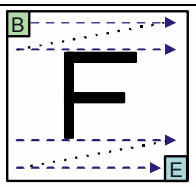
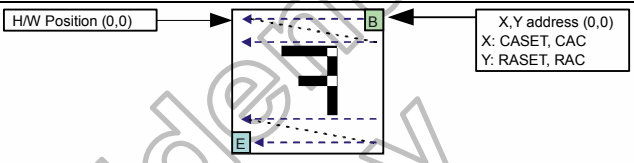
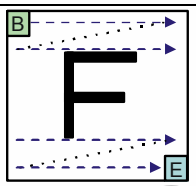
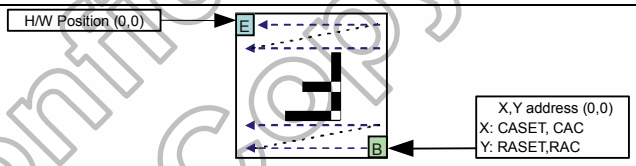
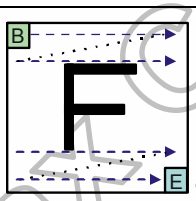
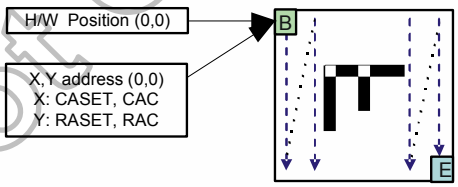
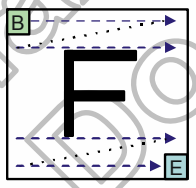
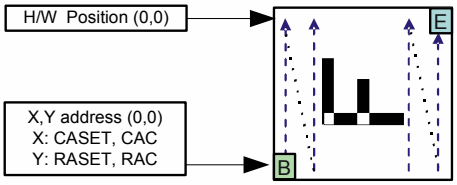
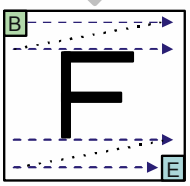
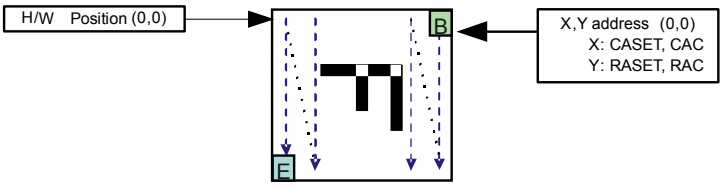
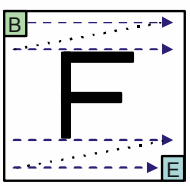
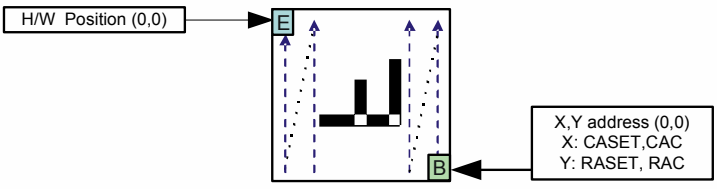
Display Data Direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6.5 Address direction settings

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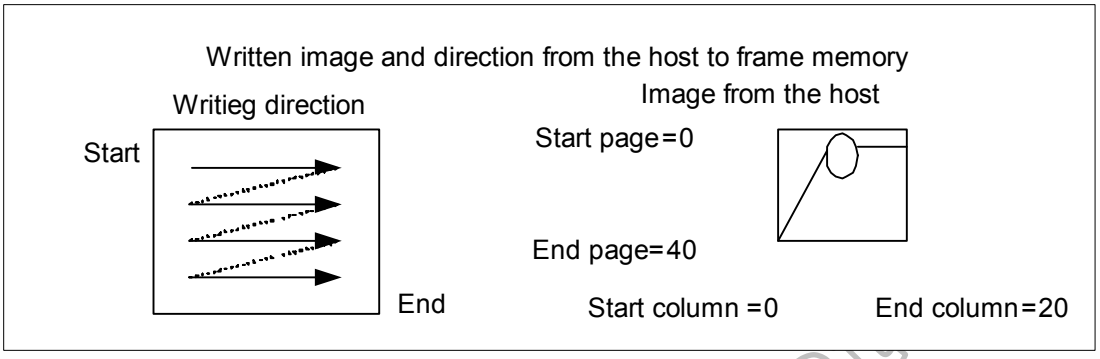
Example for rotation with MY, MX and MV

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20 => commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.



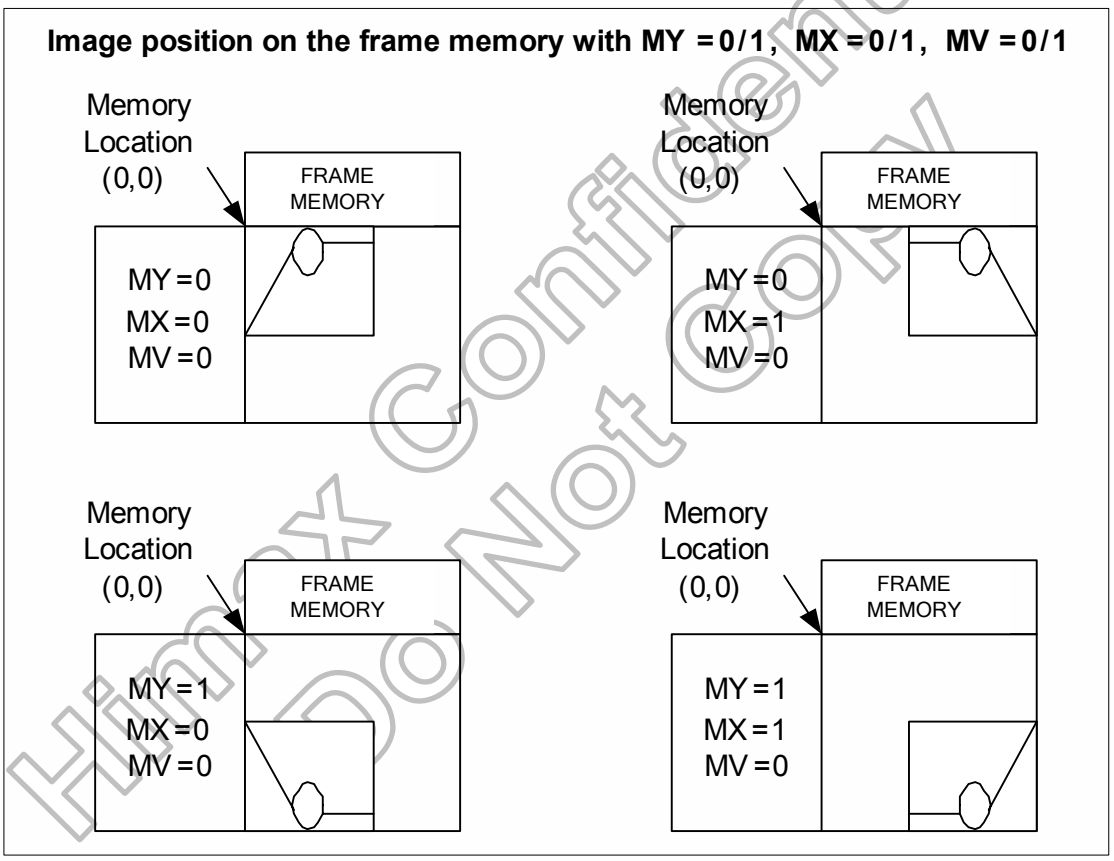


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Figure 6.3 Example for rotation with MY, MX and MV – 1

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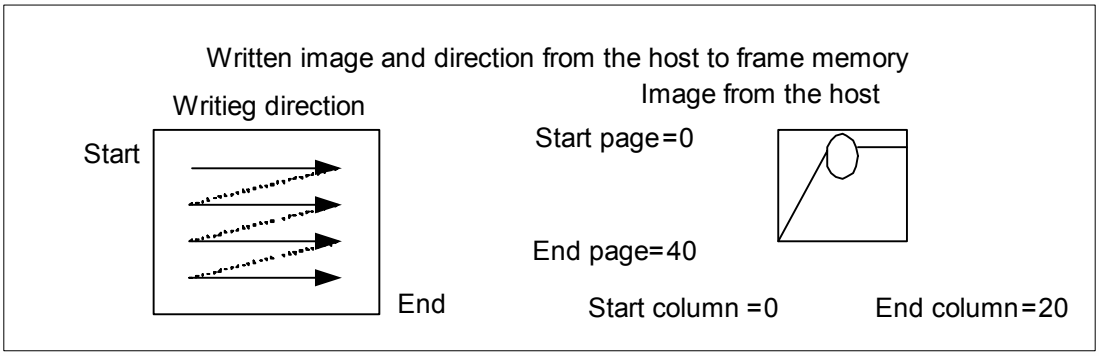

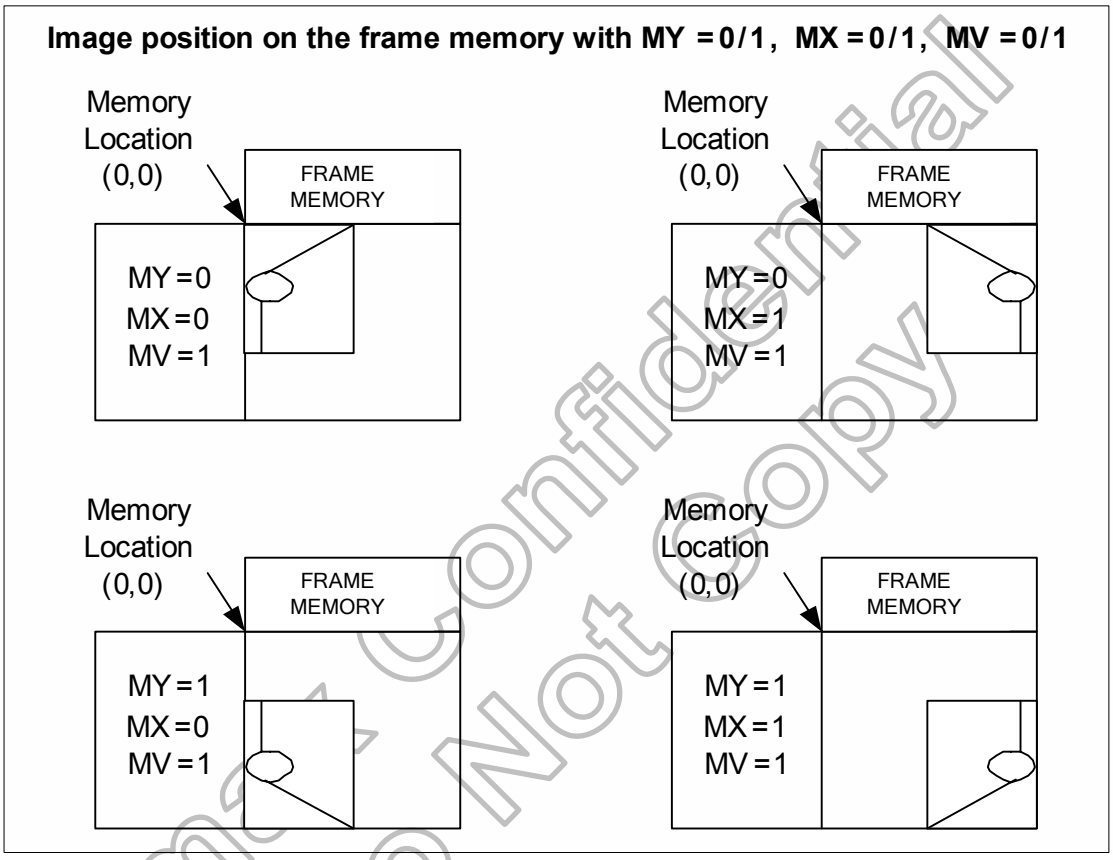

Figure 6.4 Example for rotation with MY, MX and MV - 2

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6.3 GRAM to display address mapping

By setting the **SS** bit, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** bit, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR** bit, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 6.6, Table 6.7 and Table 6.8 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

	SS	BGR='L'												
Source Output	0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
	1													
	0	S718	S719	S710	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
	1													
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

	SS	BGR='H'												
Source Output	0	S3	S2	S1	S6	S5	S4	-------	S717	S716	S715	S720	S719	S718
	1													
	0	S720	S179	S178	S177	S176	S715	-------	S6	S5	S4	S3	S2	S1
	1													
X Address		"00"h			"01"h			-------	"EE"h			"EF"h		
Bit Allocation		R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Note: (1) RGB direction default setting is defined by R16h[4] (BGR) bit..

Table 6.6 GRAM X address and display panel position (240RGBx432 dot)

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S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---------	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G1	000000h			000001h			000002h			---------	000ECh			00013Dh			00013Eh			00013Fh		
G2	001000h			001001h			001002h			---------	001ECh			00113Dh			00113Eh			00113Fh		
G3	002000h			002001h			002002h			---------	002ECh			00213Dh			00213Eh			00213Fh		
G4	003000h			003001h			003002h			---------	003ECh			00313Dh			00313Eh			00313Fh		
G5	004000h			004001h			004002h			---------	004ECh			00413Dh			00413Eh			00413Fh		
G6	005000h			005001h			005002h			---------	005ECh			00513Dh			00513Eh			00513Fh		
G7	006000h			006001h			006002h			---------	006ECh			00613Dh			00613Eh			00613Fh		
G8	007000h			007001h			007002h			---------	007ECh			00713Dh			00713Eh			00713Fh		
G9	008000h			008001h			008002h			---------	008ECh			00813Dh			00813Eh			00813Fh		
⋮	⋮			⋮			⋮			---------	⋮			⋮			⋮			⋮		
G422	1A6000h			1A6001h			1A6002h			---------	1A6ECh			1A6EDh			1A6EEh			1A6EFh		
G423	1A7000h			1A7001h			1A7002h			---------	1A7ECh			1A7EDh			1A7EEh			1A7EFh		
G424	1A8000h			1A8001h			1A8002h			---------	1A8ECh			1A8EDh			1A8EEh			1A8EFh		
G425	1A9000h			1A9001h			1A9002h			---------	1A9ECh			1A9EDh			1A9EEh			1A9EFh		
G426	1AA000h			1AA001h			1AA002h			---------	1AAECh			1AAEDh			1AAEEh			1AAEFh		
G427	1AB000h			1AB001h			1AB002h			---------	1ABECh			1ABEDh			1ABEEh			1ABEFh		
G428	1AC000h			1AC001h			1AC002h			---------	1ACECh			1ACEDh			1ACEEh			1ACEFh		
G429	1AD000h			1AD001h			1AD002h			---------	1ADECh			1ADEDh			1ADEEh			1ADEFh		
G430	1AE000h			1AE001h			1AE002h			---------	1AEECh			1AEEDh			1AEEEh			1AEEFh		
G431	1AF000h			1AF001h			1AF002h			---------	1AFECh			1AFEDh			1AFEEh			1AFEFh		

Table 6.7 GRAM address and display panel position (GS=L, 240RGBx432 dot)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---------	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
G431	000000h			000001h			000002h			---------	000ECh			00013Dh			00013Eh			00013Fh		
G430	001000h			001001h			001002h			---------	001ECh			00113Dh			00113Eh			00113Fh		
G429	002000h			002001h			002002h			---------	002ECh			00213Dh			00213Eh			00213Fh		
G428	003000h			003001h			003002h			---------	003ECh			00313Dh			00313Eh			00313Fh		
G427	004000h			004001h			004002h			---------	004ECh			00413Dh			00413Eh			00413Fh		
G426	005000h			005001h			005002h			---------	005ECh			00513Dh			00513Eh			00513Fh		
G425	006000h			006001h			006002h			---------	006ECh			00613Dh			00613Eh			00613Fh		
G424	007000h			007001h			007002h			---------	007ECh			00713Dh			00713Eh			00713Fh		
G423	008000h			008001h			008002h			---------	008ECh			00813Dh			00813Eh			00813Fh		
⋮	⋮			⋮			⋮			---------	⋮			⋮			⋮			⋮		
G10	1A6000h			1A6001h			1A6002h			---------	1A6ECh			1A6EDh			1A6EEh			1A6EFh		
G9	1A7000h			1A7001h			1A7002h			---------	1A7ECh			1A7EDh			1A7EEh			1A7EFh		
G8	1A8000h			1A8001h			1A8002h			---------	1A8ECh			1A8EDh			1A8EEh			1A8EFh		
G7	1A9000h			1A9001h			1A9002h			---------	1A9ECh			1A9EDh			1A9EEh			1A9EFh		
G6	1AA000h			1AA001h			1AA002h			---------	1AAECh			1AAEDh			1AAEEh			1AAEFh		
G5	1AB000h			1AB001h			1AB002h			---------	1ABECh			1ABEDh			1ABEEh			1ABEFh		
G4	1AC000h			1AC001h			1AC002h			---------	1ACECh			1ACEDh			1ACEEh			1ACEFh		
G3	1AD000h			1AD001h			1AD002h			---------	1ADECh			1ADEDh			1ADEEh			1ADEFh		
G2	1AE000h			1AE001h			1AE002h			---------	1AEECh			1AEEDh			1AEEEh			1AEEFh		
G1	1AF000h			1AF001h			1AF002h			---------	1AFECh			1AFEDh			1AFEEh			1AFEFh		

Table 6.8 GRAM address and display panel position (GS=H , 240RGBx432 dot)

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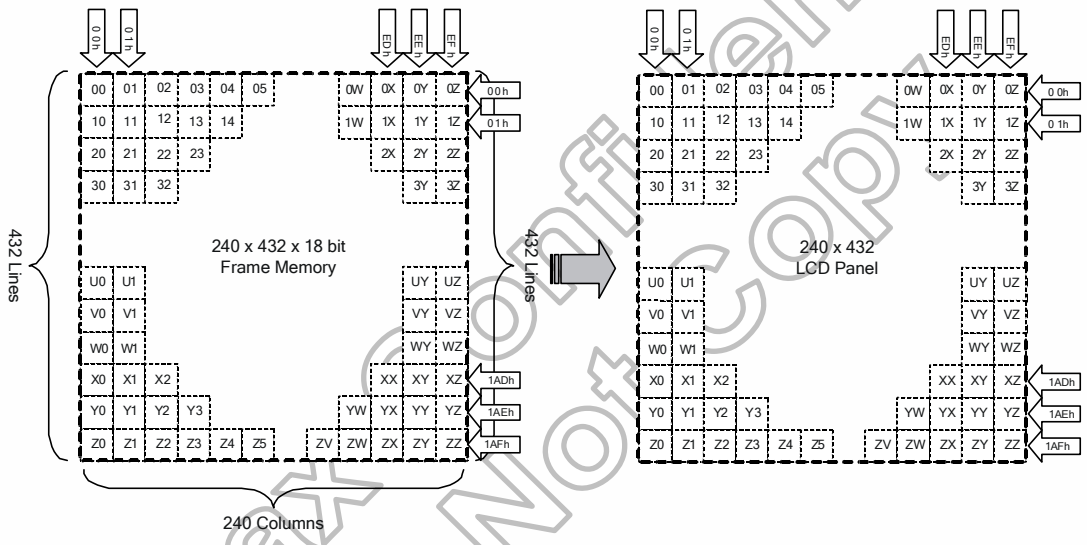
The HX8352-B01 supports three kinds of display mode: one is Normal Display Mode, another is Partial Display Mode, and Scrolling Display Mode.

When the **PLTON** = '0' is set, HX8352-B01 will be into Normal Display Mode. When the **PLTON** = '1' is set, HX8352-B01 will be into Partial Display Mode. When the **SCROL** = '1' is set, HX8352-B01 will go into Scrolling Display Mode.

Note: The HX8358-B01 does not support PLTON ON and SCROL ON at the same time, so PLTON and SCROL cannot set as "1" together.

6.3.1 Normal display on or partial Mode on, vertical scroll off

In this mode(240x432 dot), content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 01AFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



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Example:

(1) **PLTON** = '1',

(2) PSL[15:0]=11_{DEC}, PEL[15:0]=130_{DEC}

(3) 240RGBx432 dot display mode.

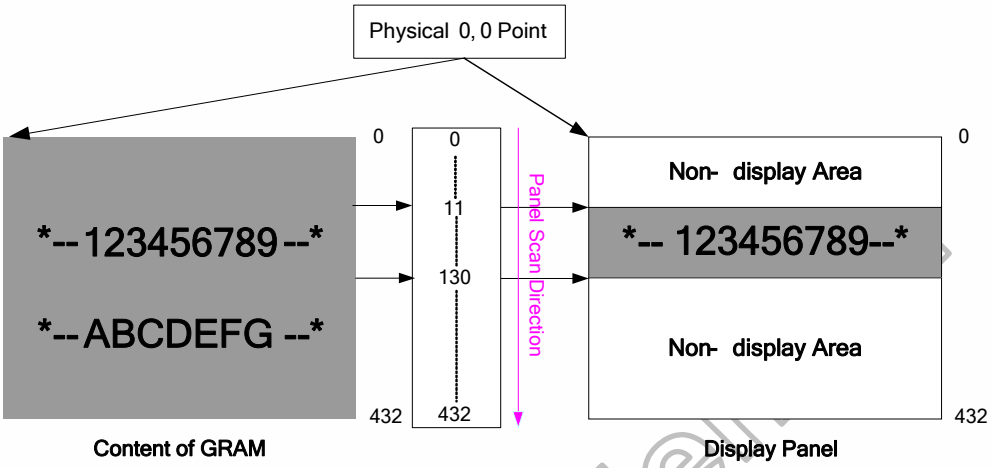

Figure 6.5 Partial display area setting (240x432 panel)

The refresh gate scan cycle in the rest display area of the screen (non-display area) can be specified by **ISC[3:0]** bits. The scan cycle is set to an odd number from 0~13.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
:	:	:	:	:	
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

Table 6.9 ISC[3:0] bits definition

The rest display area (non-display area) will be the white display if the type of LCD is normally white **(INVON = "0")** and will be the black display if the type of LCD is normally black **(INVON = "1")** in refresh gate scan cycle.

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6.3.2 Vertical scroll display mode

When **SCROL** bit is set to '1', the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

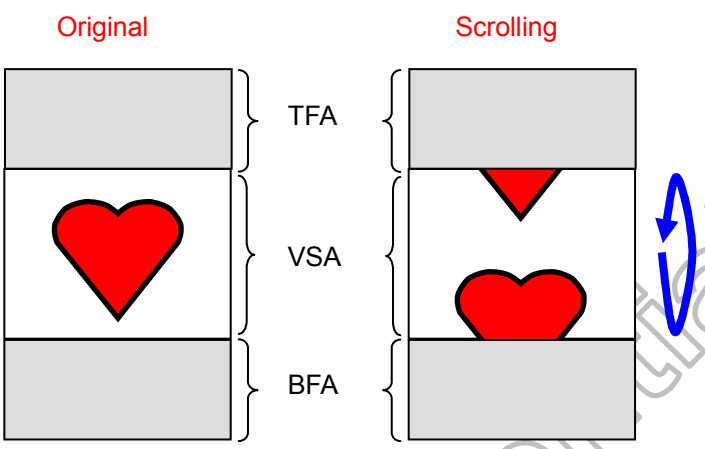

Figure 6.6 Vertical scrolling

When Vertical Scrolling Definition (TFA+VSA+BFA)=432. In this case, scrolling is applied as shown below.

Example 1:

(1) TFA='2d', VSA='432d', BFA='0d', VSP='3d'

(2) 240RGBx432 dot display mode.

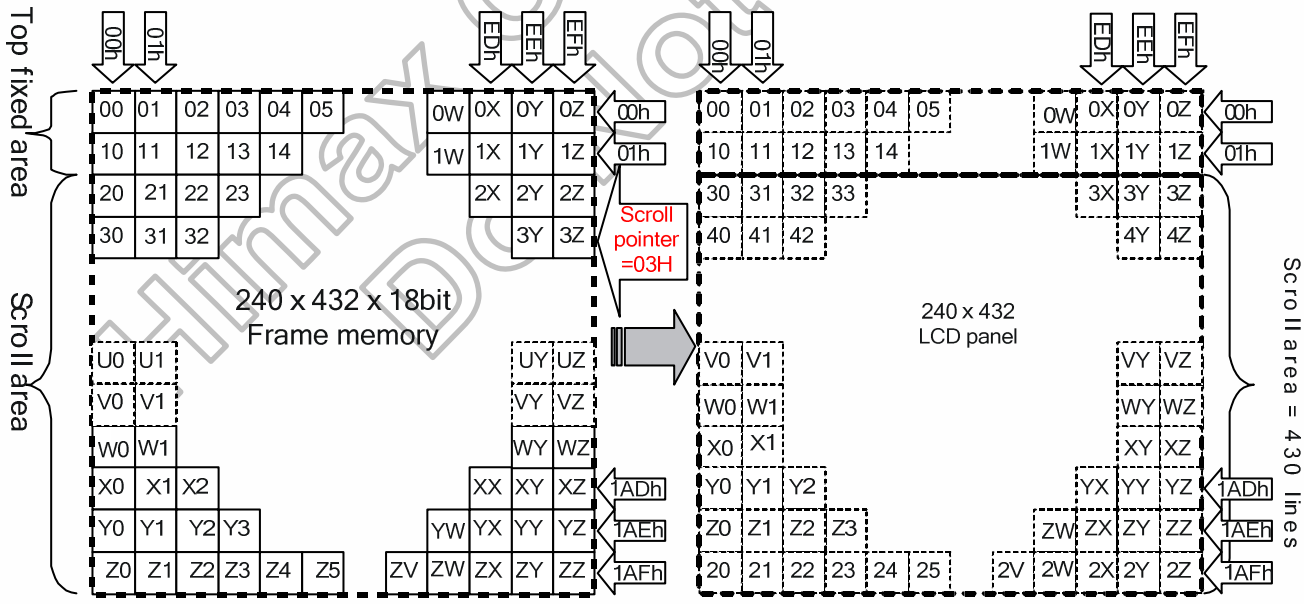

Figure 6.7 Memory map of vertical scrolling 1

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Example 2:

(1) TFA='2d', VSA='432d', BFA='2d', VSP='3d'

(2) 240RGBx432 dot display mode

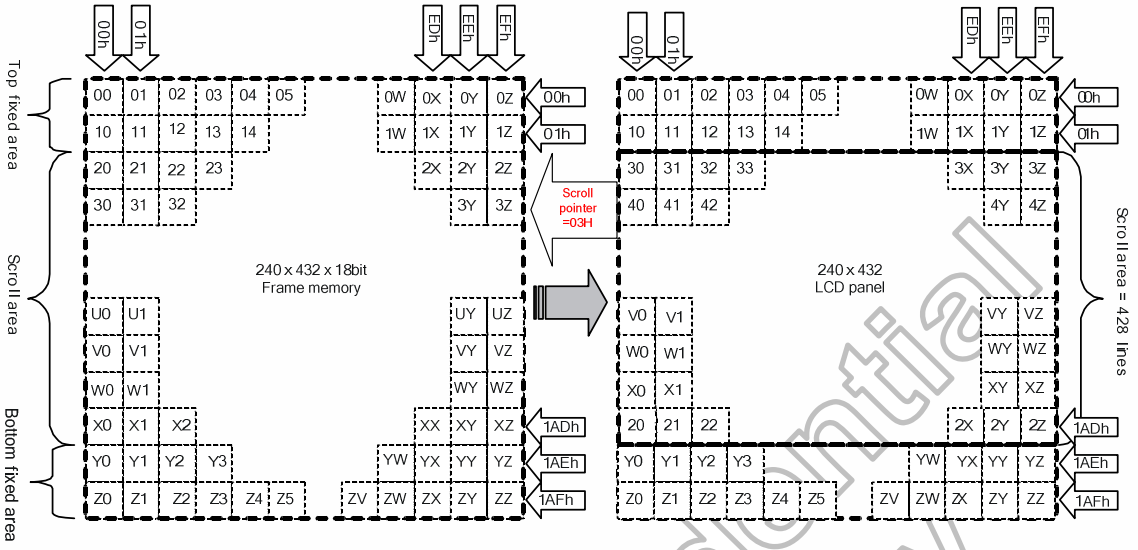

Figure 6.8 Memory map of vertical scrolling 2

Example 3:

(1) TFA='2d', VSA='432d', BFA='2d', VSP='5d'

(2) 240RGBx432 dot display mode

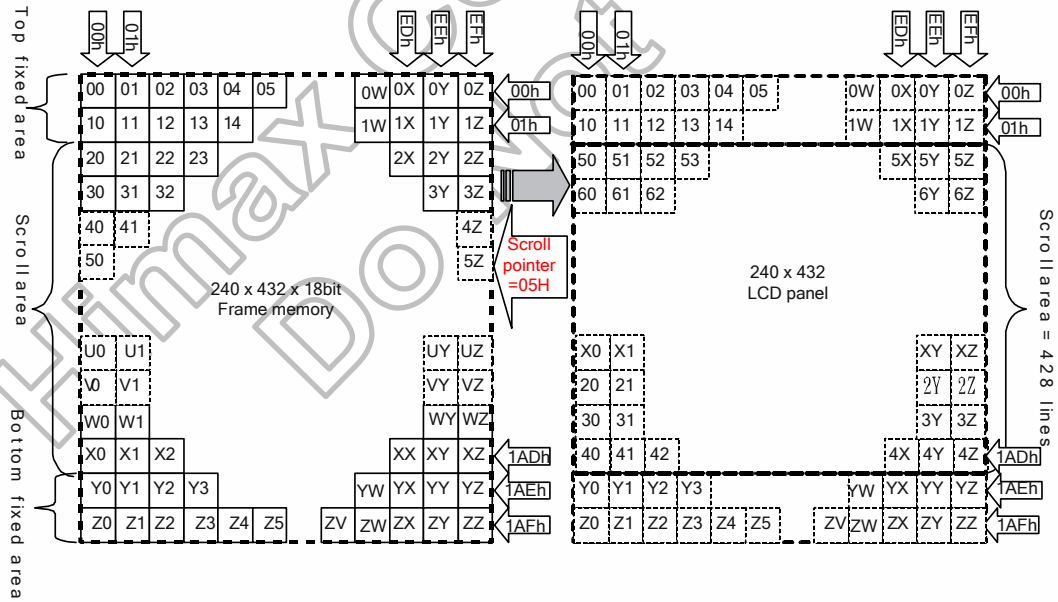

Figure 6.9 Memory map of vertical scrolling 3

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Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

Case 1: TFA + VSA + BFA ≠ '432d'
N/A. Do not set TFA + VSA + BFA ≠ '432d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '432d' (Scrolling)
Example:

(1) When TFA='0d', VSA='432d', BFA='0d' and VSP='40d'

(2) 240RGBx432 dot display mode

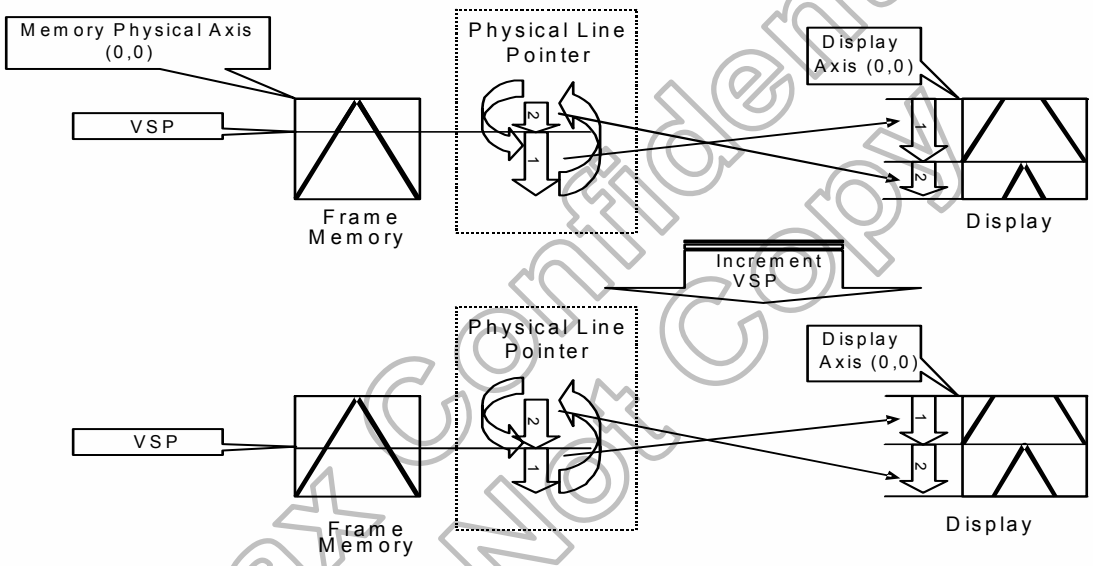

Figure 6.10 Vertical scrolling example

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7. Functional Description

7.1 Internal oscillator

The HX8352-B01 can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±10%, **RADJ [3:0]** bits for initial 3.5MHz internal clock generation. With other dividers setting, the 3.5MHz internal clock can be used to generate clock for other part of the chip using.

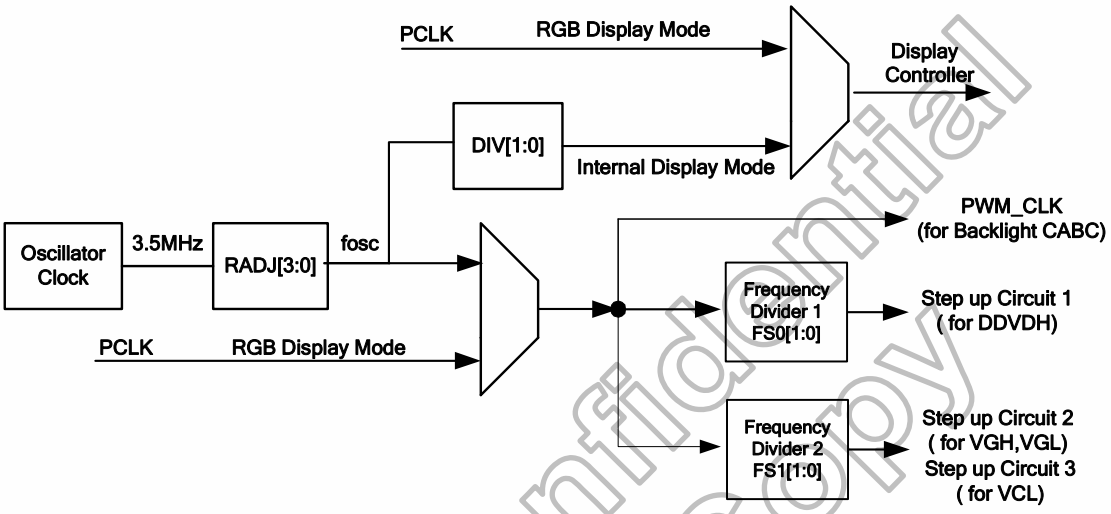

Figure 7.1 HX8352-B01 internal clock circuit

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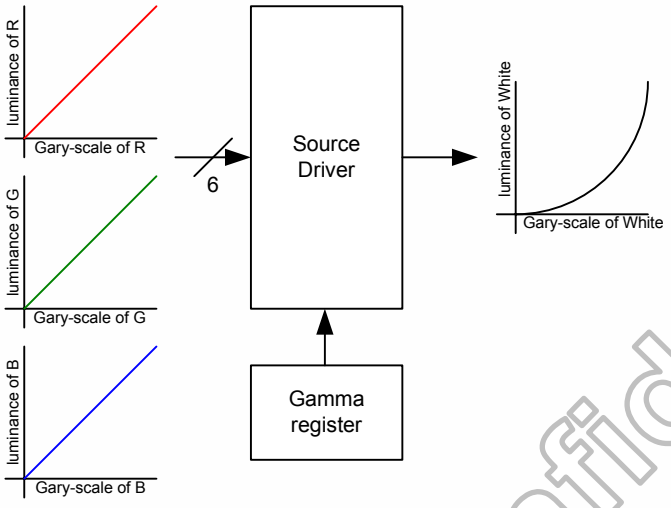
7.2 Gamma characteristic correction function

The HX8352-B01 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

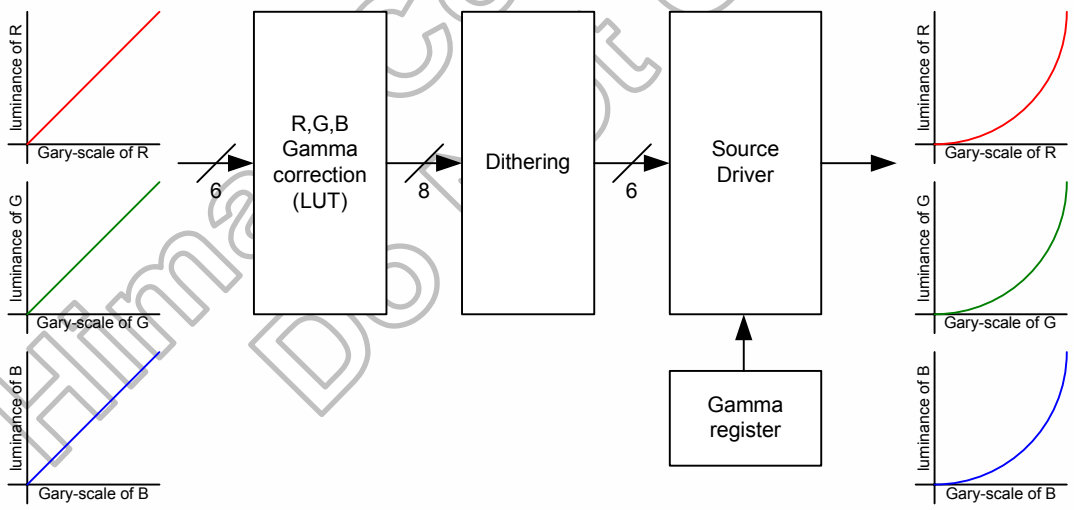


Figure 7.2 Gamma adjustments different of source driver with digital gamma correction

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7.2.1 Gray voltage generator for source driver

The HX8352-B01 incorporates gamma adjustment function for the 262,144-color display (63 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

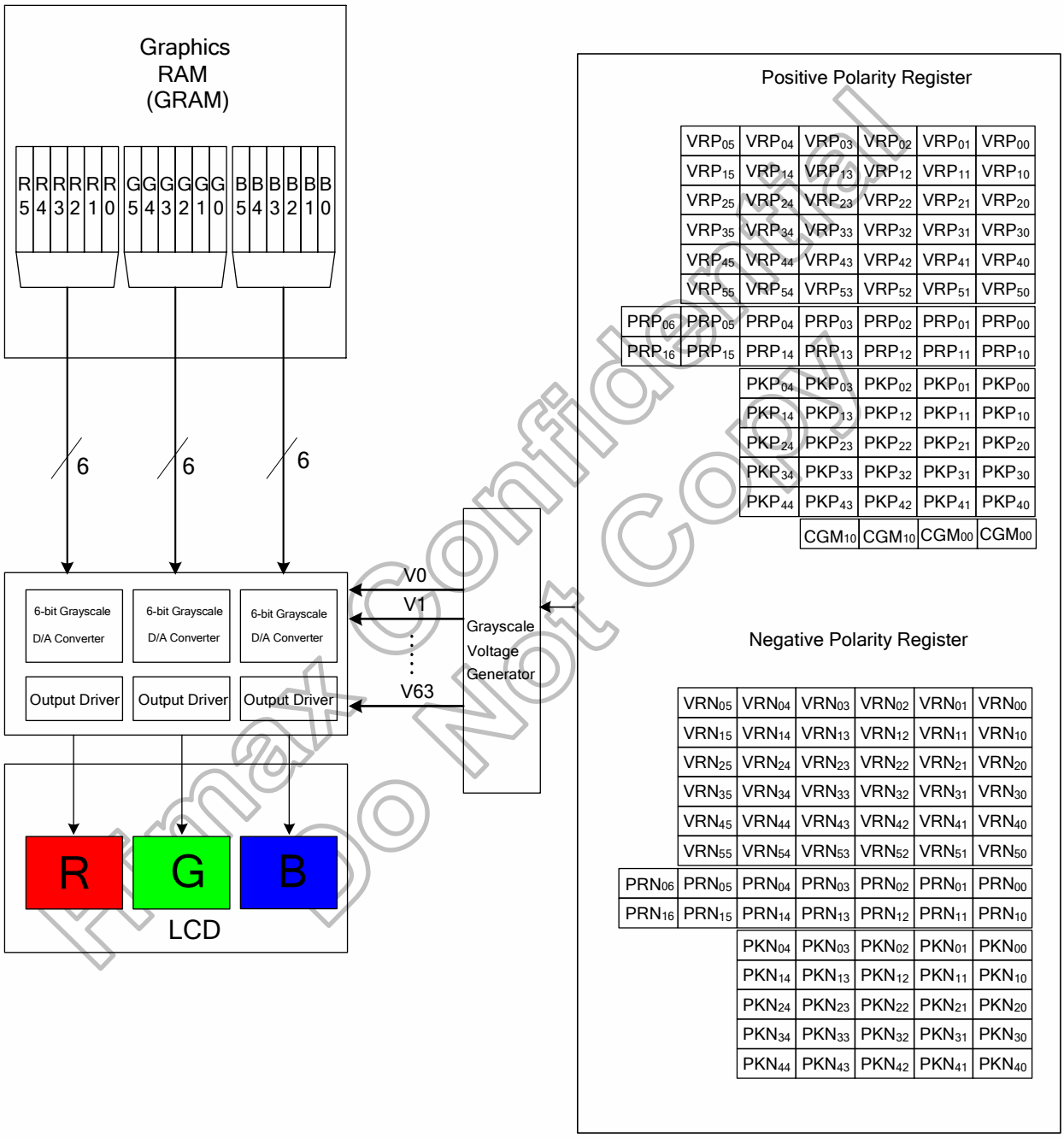

Figure 7.3 Grayscale control

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7.2.1.1 Structure of grayscale voltage generator

Eight reference gamma voltages (RVP 0, 1, 8, 20, 43, 55, 62 and 63). For positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

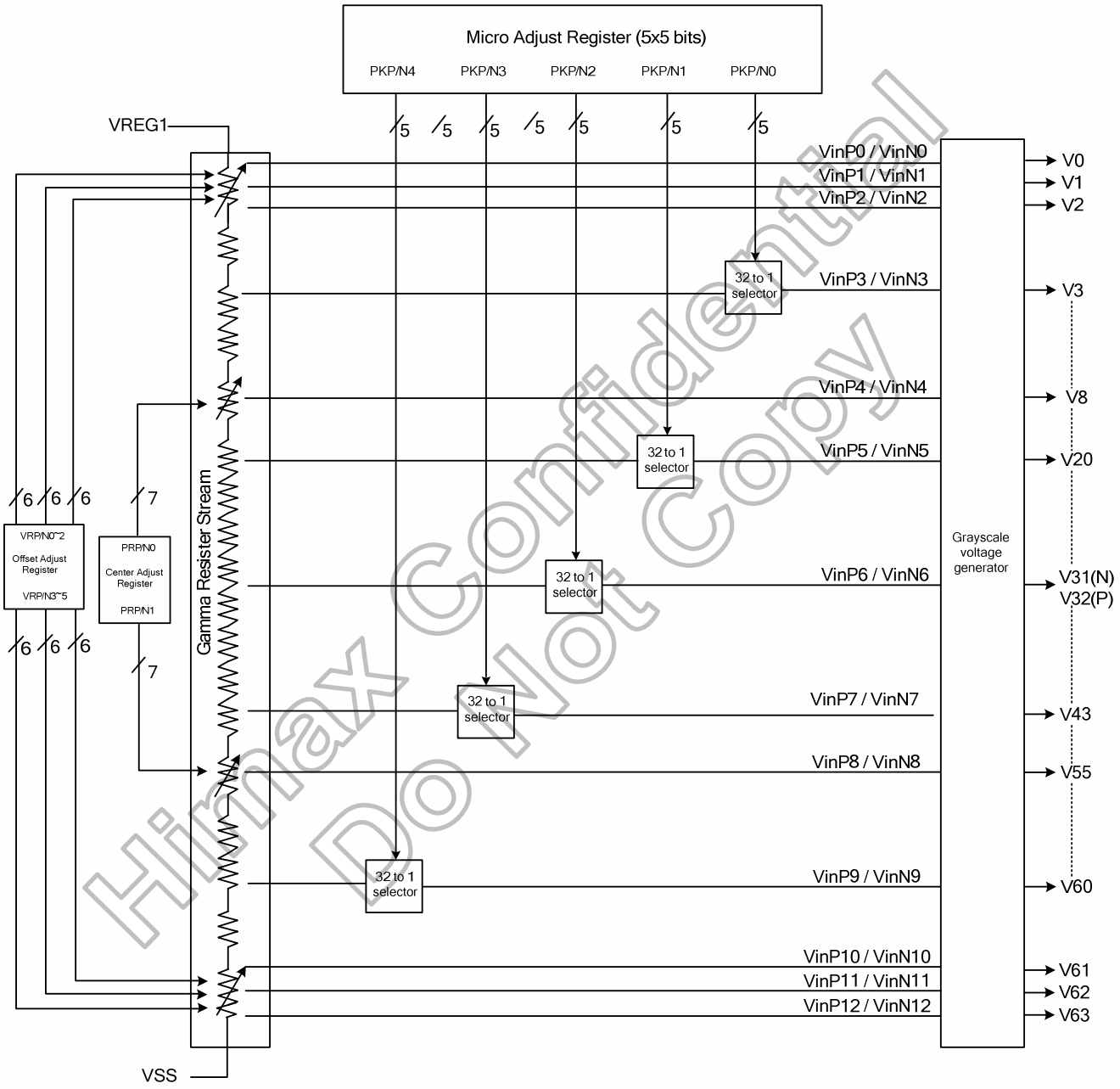

Figure 7.4 Structure of grayscale voltage generator

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7.2.1.2 Gamma-characteristics adjustment register

This HX8352-B01 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common).

Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

7.2.1.3 Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N) 0, 1, 2, ,3, 8, 20, 32(31), 43, 55, 60, 61, 62, 63).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 43)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Table 7.1 Gamma-adjustment registers

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7.2.1.4 Gamma resister stream and 8 to 1 selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. VgP/N (0, 1, 2, 3, 8 20, 32, 43, 55, 60, 61, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

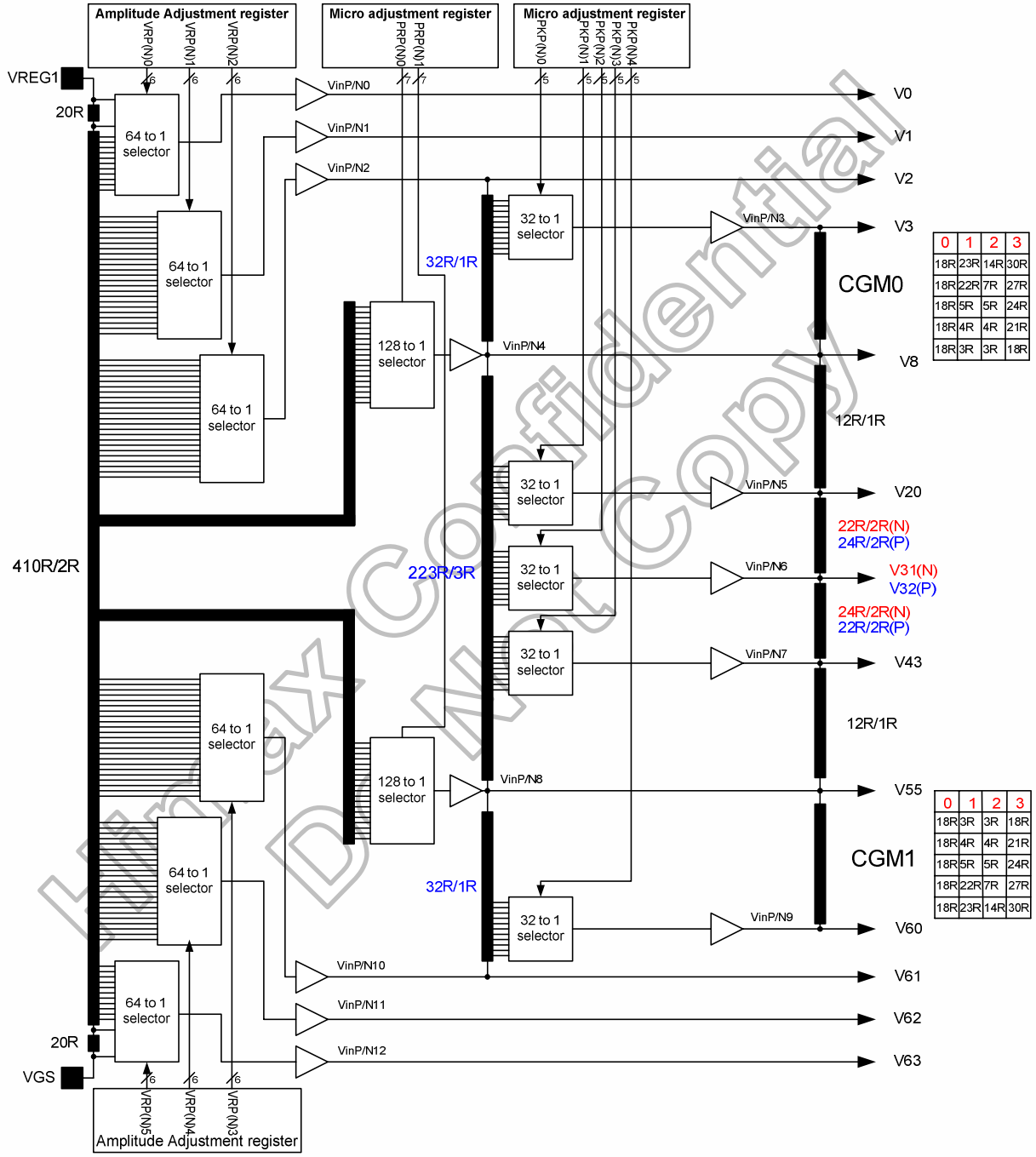

Figure 7.5 Gamma resister stream and gamma reference voltage

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7.2.1.5 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0	Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1	Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	20R	000001	2R	000001	2R
000010	22R	000010	4R	000010	4R
000011	24R	000011	6R	000011	6R
• •	• •	• •	• •	• •	• •
011101	76R	011101	58R	011101	58R
011110	78R	011110	60R	011110	60R
011111	80R	011111	62R	011111	62R
100000	84R	100000	66R	100000	66R
100001	88R	100001	70R	100001	70R
100010	92R	100010	74R	100010	74R
• •	• •	• •	• •	• •	• •
111101	200R	111101	182R	111101	182R
111110	204R	111110	186R	111110	186R
111111	208R	111111	190R	111111	190R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3	Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4	Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	4R	000001	4R	000001	4R
000010	8R	000010	8R	000010	8R
• •	• •	• •	• •	• •	• •
011101	116R	011101	116R	011101	116R
011110	120R	011110	120R	011110	120R
011111	124R	011111	124R	011111	124R
100000	128R	100000	128R	100000	128R
100001	130R	100001	130R	100001	130R
100010	132R	100010	132R	100010	132R
• •	• •	• •	• •	• •	• •
111100	184R	111100	184R	111100	184R
111101	186R	111101	186R	111101	186R
111110	188R	111110	188R	111110	188R
111111	190R	111111	190R	111111	208R

Table 7.2 Offset adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0	Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R	0000000	0R
0000001	2R	0000001	2R
0000010	4R	0000010	4R
• •	• •	• •	• •
1111101	250R	1010101	250R
1111110	252R	1111110	252R
1111111	254R	1111111	254R

Table 7.3 Center adjustment

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The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP/N0	VRP/N0 5-0 = 000000	VREG1
	VRP/N0 5-0 = 000001	((450R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000010	((450R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000011	((450R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000100	((450R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000101	((450R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000110	((450R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000111	((450R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001000	((450R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001001	((450R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001010	((450R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001011	((450R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001100	((450R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001101	((450R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001110	((450R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001111	((450R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010000	((450R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010001	((450R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010010	((450R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010011	((450R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010100	((450R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010101	((450R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010110	((450R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010111	((450R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011000	((450R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011001	((450R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011010	((450R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011011	((450R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011100	((450R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011101	((450R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011110	((450R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011111	((450R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100000	((450R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100001	((450R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100010	((450R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100011	((450R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100100	((450R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100101	((450R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100110	((450R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100111	((450R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101000	((450R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101001	((450R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101010	((450R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101011	((450R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101100	((450R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101101	((450R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101110	((450R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101111	((450R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110000	((450R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110001	((450R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110010	((450R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110011	((450R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110100	((450R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110101	((450R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110110	((450R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110111	((450R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111000	((450R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111001	((450R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111010	((450R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111011	((450R - 192R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111100	((450R - 196R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111101	((450R - 200R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111110	((450R - 204R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111111	((450R - 208R) / 450R) * (VREG1 - VGS) + VGS

Table 7.4 Voltage calculation formula for VinP/N 0

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For TCL Only

Reference Voltage	Macro Adjustment Value	VinP/N1 Formula
VinP/N1	VRP/N1 5-0 = 000000	(430R / 450R) * (VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000001	((430R - 2R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000010	((430R - 4R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000011	((430R - 6R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000100	((430R - 8R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000101	((430R - 10R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000110	((430R - 12R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000111	((430R - 14R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001000	((430R - 16R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001001	((430R - 18R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001010	((430R - 20R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001011	((430R - 22R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001100	((430R - 24R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001101	((430R - 26R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001110	((430R - 28R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001111	((430R - 30R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010000	((430R - 32R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010001	((430R - 34R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010010	((430R - 36R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010011	((430R - 38R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010100	((430R - 40R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010101	((430R - 42R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010110	((430R - 44R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010111	((430R - 46R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011000	((430R - 48R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011001	((430R - 50R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011010	((430R - 52R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011011	((430R - 54R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011100	((430R - 56R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011101	((430R - 58R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011110	((430R - 60R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011111	((430R - 62R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100000	((430R - 66R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100001	((430R - 70R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100010	((430R - 74R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100011	((430R - 78R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100100	((430R - 82R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100101	((430R - 86R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100110	((430R - 90R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100111	((430R - 94R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101000	((430R - 98R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101001	((430R - 102R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101010	((430R - 106R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101011	((430R - 110R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101100	((430R - 114R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101101	((430R - 118R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101110	((430R - 122R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101111	((430R - 126R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110000	((430R - 130R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110001	((430R - 134R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110010	((430R - 138R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110011	((430R - 142R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110100	((430R - 146R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110101	((430R - 150R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110110	((430R - 154R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110111	((430R - 158R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111000	((430R - 162R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111001	((430R - 166R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111010	((430R - 170R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111011	((430R - 174R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111100	((430R - 178R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111101	((430R - 182R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111110	((430R - 186R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111111	((430R - 190R) / 450R) *(VREG1 - VGS) + VGS

Table 7.5 Voltage calculation formula for VinP/N 1

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Reference Voltage	Macro Adjustment Value	VinP/N2 Formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000001	((410R - 2R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000010	((410R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000011	((410R - 6R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000100	((410R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000101	((410R - 10R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000110	((410R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000111	((410R - 14R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001000	((410R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001001	((410R - 18R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001010	((410R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001011	((410R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001100	((410R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001101	((410R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001110	((410R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001111	((410R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010000	((410R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010001	((410R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010010	((410R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010011	((410R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010100	((410R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010101	((410R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010110	((410R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010111	((410R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011000	((410R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011001	((410R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011010	((410R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011011	((410R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011100	((410R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011101	((410R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011110	((410R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011111	((410R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100000	((410R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100001	((410R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100010	((410R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100011	((410R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100100	((410R - 82R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100101	((410R - 86R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100110	((410R - 90R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100111	((410R - 94R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101000	((410R - 98R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101001	((410R - 102R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101010	((410R - 106R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101011	((410R - 110R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101100	((410R - 114R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101101	((410R - 118R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101110	((410R - 122R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101111	((410R - 126R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110000	((410R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110001	((410R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110010	((410R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110011	((410R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110100	((410R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110101	((410R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110110	((410R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110111	((410R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111000	((410R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111001	((410R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111010	((410R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111011	((410R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111100	((410R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111101	((410R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111110	((410R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111111	((410R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7.6 Voltage calculation formula for VinP/N 2

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For TCL Only

Reference Voltage	Macro Adjustment Value	VinP/N3 Formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R - 10R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R - 11R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R - 12R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R - 13R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R - 14R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R - 15R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R - 16R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R - 17R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R - 18R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R - 19R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R - 20R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R - 21R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R - 22R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R - 23R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R - 24R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R - 25R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R - 26R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R - 27R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R - 28R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R - 29R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R - 30R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R - 31R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4

Table 7.7 Voltage calculation formula for VinP/N 3

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Reference Voltage	Macro Adjustment Value	VinP/N4 Formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000001	((350R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000010	((350R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000111	((350R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010001	((350R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011011	((350R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100000	((350R - 64R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101010	((350R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111110	((350R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000010	((350R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VREG1 - VGS) + VGS

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Reference Voltage	Macro Adjustment Value	VinP/N4 Formula
	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001100	((350R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010111	((350R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101111	((350R – 223R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111001	((350R – 243R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VREG1 - VGS) + VGS

Table 7.8 Voltage calculation formula for VinP/N 4

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Reference Voltage	Macro Adjustment Value	VinP/N5 Formula
VinP/N5	PKP/N3 4-0 = 00000	(193R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((193R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((193R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((193R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((193R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((193R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((193R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((193R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((193R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((193R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((193R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((193R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((193R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((193R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((193R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((193R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((193R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((193R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((193R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((193R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((193R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((193R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((193R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((193R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((193R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((193R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((193R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((193R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((193R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((193R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((193R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((193R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.9 Voltage calculation formula for VinP/N 5

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Reference Voltage	Macro Adjustment Value	VinP/N6 Formula
VinP/N6	PKP/N4 4-0 = 00000	(158R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00001	((158R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00010	((158R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00011	((158R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00100	((158R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00101	((158R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00110	((158R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00111	((158R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01000	((158R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01001	((158R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01010	((158R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01011	((158R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01100	((158R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01101	((158R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01110	((158R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01111	((158R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10000	((158R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10001	((158R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10010	((158R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10011	((158R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10100	((158R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10101	((158R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10110	((158R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10111	((158R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11000	((158R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11001	((158R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11010	((158R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11011	((158R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11100	((158R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11101	((158R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11110	((158R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11111	((158R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.10 Voltage calculation formula for VinP/N 6

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Reference Voltage	Macro Adjustment Value	VinP/N7 Formula
VinP/N7	PKP/N6 4-0 = 00000	(123R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00001	((123R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00010	((123R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00011	((123R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00100	((123R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00101	((123R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00110	((123R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00111	((123R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01000	((123R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01001	((123R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01010	((123R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01011	((123R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01100	((123R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01101	((123R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01110	((123R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01111	((123R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10000	((123R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10001	((123R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10010	((123R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10011	((123R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10100	((123R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10101	((123R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10110	((123R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10111	((123R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11000	((123R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11001	((123R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11010	((123R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11011	((123R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11100	((123R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11101	((123R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11110	((123R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11111	((123R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7.11 Voltage calculation formula for VinP/N 7

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Reference Voltage	Macro Adjustment Value	VinP/N8 Formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000001	((354R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000010	((354R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000111	((354R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010001	((354R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011011	((354R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100000	((354R - 64R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101010	((354R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111110	((354R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000010	((354R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VREG1 - VGS) + VGS

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Reference Voltage	Macro Adjustment Value	VinP/N8 Formula
	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001100	((354R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010111	((354R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011001	((354R - 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011100	((354R - 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011110	((354R - 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100001	((354R - 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100011	((354R - 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100110	((354R - 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101000	((354R - 208R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101011	((354R - 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101101	((354R - 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110000	((354R - 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110010	((354R - 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110101	((354R - 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110111	((354R - 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111010	((354R - 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111100	((354R - 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111111	((354R - 254R) / 450R) * (VREG1 - VGS) + VGS

Table 7.12 Voltage calculation formula for VinP/N 8

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Reference Voltage	Macro Adjustment Value	VinP/N9 Formula
VinP/N9	PKP/N7 4-0 = 00000	(31R / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00001	((31R - 1R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00010	((31R - 2R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00011	((31R - 3R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00100	((31R - 4R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00101	((31R - 5R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00110	((31R - 6R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00111	((31R - 7R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01000	((31R - 8R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01001	((31R - 9R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10

Table 7.13 Voltage calculation formula for VinP/N 9

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Reference Voltage	Macro Adjustment Value	VinP/N10 Formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000001	((230R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000010	((230R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000011	((230R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000100	((230R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000101	((230R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000110	((230R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000111	((230R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001000	((230R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001001	((230R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001010	((230R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001011	((230R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001100	((230R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001101	((230R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001110	((230R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001111	((230R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010000	((230R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010001	((230R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010010	((230R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010011	((230R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010100	((230R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010101	((230R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010110	((230R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010111	((230R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011000	((230R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011001	((230R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011010	((230R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011011	((230R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011100	((230R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011101	((230R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011110	((230R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011111	((230R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100000	((230R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100001	((230R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100010	((230R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100011	((230R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100100	((230R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100101	((230R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100110	((230R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100111	((230R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101000	((230R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101001	((230R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101010	((230R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101011	((230R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101100	((230R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101101	((230R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101110	((230R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101111	((230R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110000	((230R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110001	((230R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110010	((230R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110011	((230R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110100	((230R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110101	((230R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110110	((230R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110111	((230R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111000	((230R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111001	((230R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111010	((230R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111011	((230R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111100	((230R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111101	((230R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111110	((230R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111111	((230R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7.14 Voltage calculation formula for VinP/N 10

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Reference Voltage	Macro Adjustment Value	VinP/N11 Formula
VinP/N11	VRP/N4 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000001	((210R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000010	((210R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000011	((210R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000100	((210R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000101	((210R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000110	((210R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000111	((210R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001000	((210R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001001	((210R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001010	((210R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001011	((210R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001100	((210R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001101	((210R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001110	((210R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001111	((210R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010000	((210R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010001	((210R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010010	((210R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010011	((210R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010100	((210R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010101	((210R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010110	((210R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010111	((210R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011000	((210R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011001	((210R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011010	((210R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011011	((210R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011100	((210R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011101	((210R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011110	((210R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011111	((210R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100000	((210R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100001	((210R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100010	((210R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100011	((210R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100100	((210R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100101	((210R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100110	((210R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100111	((210R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101000	((210R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101001	((210R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101010	((210R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101011	((210R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101100	((210R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101101	((210R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101110	((210R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101111	((210R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110000	((210R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110001	((210R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110010	((210R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110011	((210R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110100	((210R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110101	((210R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110110	((210R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110111	((210R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111000	((210R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111001	((210R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111010	((210R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111011	((210R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111100	((210R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111101	((210R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111110	((210R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111111	((210R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7.15 Voltage calculation formula for VinP/N 11

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Reference Voltage	Macro Adjustment Value	VinP/N12 Formula
VinP/N12	VRP/N5 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000001	((208R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000010	((208R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000011	((208R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000100	((208R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000101	((208R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000110	((208R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000111	((208R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001000	((208R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001001	((208R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001010	((208R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001011	((208R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001100	((208R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001101	((208R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001110	((208R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001111	((208R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010000	((208R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010001	((208R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010010	((208R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010011	((208R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010100	((208R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010101	((208R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010110	((208R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010111	((208R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011000	((208R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011001	((208R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011010	((208R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011011	((208R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011100	((208R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011101	((208R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011110	((208R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011111	((208R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100000	((208R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100001	((208R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100010	((208R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100011	((208R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100100	((208R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100101	((208R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100110	((208R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100111	((208R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101000	((208R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101001	((208R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101010	((208R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101011	((208R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101100	((208R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101101	((208R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101110	((208R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101111	((208R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110000	((208R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110001	((208R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110010	((208R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110011	((208R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110100	((208R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110101	((208R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110110	((208R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110111	((208R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111000	((208R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111001	((208R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111010	((208R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111011	((208R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111100	((208R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111101	((208R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111110	((208R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111111	VGS

Table 7.16 Voltage calculation formula for VinP/N 12

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Grayscale Voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	VinP4+ (VinP3 - VinP4)*CT1
V5	VinP4+ (VinP3 - VinP4)*CT2
V6	VinP4+ (VinP3 - VinP4)*CT3
V7	VinP4+ (VinP3 - VinP4)*CT4
V8	VinP4
V9	VinP5+(VinP4- VinP5)*(22R/24R)
V10	VinP5+(VinP4- VinP5)*(20R/24R)
V11	VinP5+(VinP4- VinP5)*(18R/24R)
V12	VinP5+(VinP4- VinP5)*(16R/24R)
V13	VinP5+(VinP4- VinP5)*(14R/24R)
V14	VinP5+(VinP4- VinP5)*(12R/24R)
V15	VinP5+(VinP4- VinP5)*(10R/24R)
V16	VinP5+(VinP4- VinP5)*(8R/24R)
V17	VinP5+(VinP4- VinP5)*(6R/24R)
V18	VinP5+(VinP4- VinP5)*(4R/24R)
V19	VinP5+(VinP4- VinP5)*(2R/24R)
V20	VinP5
V21	VinP6+(VinP5- VinP6)*(22R/24R)
V22	VinP6+(VinP5- VinP6)*(20R/24R)
V23	VinP6+(VinP5- VinP6)*(18R/24R)
V24	VinP6+(VinP5- VinP6)*(16R/24R)
V25	VinP6+(VinP5- VinP6)*(14R/24R)
V26	VinP6+(VinP5- VinP6)*(12R/24R)
V27	VinP6+(VinP5- VinP6)*(10R/24R)
V28	VinP6+(VinP5- VinP6)*(8R/24R)
V29	VinP6+(VinP5- VinP6)*(6R/24R)
V30	VinP6+(VinP5- VinP6)*(4R/24R)
V31	VinP6+(VinP5- VinP6)*(2R/24R)

Grayscale Voltage	Formula
V32	VinP6
V33	VinP7+(VinP6- VinP7)*(20R/22R)
V34	VinP7+(VinP6- VinP7)*(18R/22R)
V35	VinP7+(VinP6- VinP7)*(16R/22R)
V36	VinP7+(VinP6- VinP7)*(14R/22R)
V37	VinP7+(VinP6- VinP7)*(12R/22R)
V38	VinP7+(VinP6- VinP7)*(10R/22R)
V39	VinP7+(VinP6- VinP7)*(8R/22R)
V40	VinP7+(VinP6- VinP7)*(6R/22R)
V41	VinP7+(VinP6- VinP7)*(4R/22R)
V42	VinP7+(VinP6- VinP7)*(2R/22R)
V43	VinP7
V44	VinP8+(VinP7- VinP8)*(22R/24R)
V45	VinP8+(VinP7- VinP8)*(20R/24R)
V46	VinP8+(VinP7- VinP8)*(18R/24R)
V47	VinP8+(VinP7- VinP8)*(16R/24R)
V48	VinP8+(VinP7- VinP8)*(14R/24R)
V49	VinP8+(VinP7- VinP8)*(12R/24R)
V50	VinP8+(VinP7- VinP8)*(10R/24R)
V51	VinP8+(VinP7- VinP8)*(8R/24R)
V52	VinP8+(VinP7- VinP8)*(6R/24R)
V53	VinP8+(VinP7- VinP8)*(4R/24R)
V54	VinP8+(VinP7- VinP8)*(2R/24R)
V55	VinP8
V56	VinP9+ (VinP8 – VinP9)*CB1
V57	VinP9+ (VinP8 – VinP9)*CB2
V58	VinP9+ (VinP8 – VinP9)*CB3
V59	VinP9+ (VinP8 – VinP9)*CB4
V60	VinP9
V61	VinP10
V62	VinP11
V63	VinP12

Table 7.17 Voltage calculation formula of 64-grayscale voltage (positive polarity)

CGMP0[1:0]	"00"	"01"	"10"	"11"
CT1	4/5	2/3	3/5	31/41
CT2	3/5	1/2	9/20	22/41
CT3	2/5	1/3	3/10	14/41
CT4	1/5	1/6	3/20	6/41

CGMP1[1:0]	"00"	"01"	"10"	"11"
CB1	4/5	5/6	17/20	13/16
CB2	3/5	2/3	7/10	5/8
CB3	2/5	1/2	11/20	41/96
CB4	1/5	1/3	2/5	7/32

Table 7.18 Voltage calculation formula of grayscale voltage V2~V7 and V56~V61

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Grayscale Voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	VinN4+ (VinN3 - VinN4)*CT1
V5	VinN4+ (VinN3 - VinN4)*CT2
V6	VinN4+ (VinN3 - VinN4)*CT3
V7	VinN4+ (VinN3 - VinN4)*CT4
V8	VinN4
V9	VinN5+(VinN4- VinN5)*(22R/24R)
V10	VinN5+(VinN4- VinN5)*(20R/24R)
V11	VinN5+(VinN4- VinN5)*(18R/24R)
V12	VinN5+(VinN4- VinN5)*(16R/24R)
V13	VinN5+(VinN4- VinN5)*(14R/24R)
V14	VinN5+(VinN4- VinN5)*(12R/24R)
V15	VinN5+(VinN4- VinN5)*(10R/24R)
V16	VinN5+(VinN4- VinN5)*(8R/24R)
V17	VinN5+(VinN4- VinN5)*(6R/24R)
V18	VinN5+(VinN4- VinN5)*(4R/24R)
V19	VinN5+(VinN4- VinN5)*(2R/24R)
V20	VinN5
V21	VinN6+(VinN5- VinN6)*(20R/22R)
V22	VinN6+(VinN5- VinN6)*(18R/22R)
V23	VinN6+(VinN5- VinN6)*(16R/22R)
V24	VinN6+(VinN5- VinN6)*(14R/22R)
V25	VinN6+(VinN5- VinN6)*(12R/22R)
V26	VinN6+(VinN5- VinN6)*(10R/22R)
V27	VinN6+(VinN5- VinN6)*(8R/22R)
V28	VinN6+(VinN5- VinN6)*(6R/22R)
V29	VinN6+(VinN5- VinN6)*(4R/22R)
V30	VinN6+(VinN5- VinN6)*(2R/22R)
V31	VinN6

Grayscale Voltage	Formula
V32	VinN7+(VinN6- VinN7)*(22R/24R)
V33	VinN7+(VinN6- VinN7)*(20R/24R)
V34	VinN7+(VinN6- VinN7)*(18R/24R)
V35	VinN7+(VinN6- VinN7)*(16R/24R)
V36	VinN7+(VinN6- VinN7)*(14R/24R)
V37	VinN7+(VinN6- VinN7)*(12R/24R)
V38	VinN7+(VinN6- VinN7)*(10R/24R)
V39	VinN7+(VinN6- VinN7)*(8R/24R)
V40	VinN7+(VinN6- VinN7)*(6R/24R)
V41	VinN7+(VinN6- VinN7)*(4R/24R)
V42	VinN7+(VinN6- VinN7)*(2R/24R)
V43	VinN7
V44	VinN8+(VinN7- VinN8)*(22R/24R)
V45	VinN8+(VinN7- VinN8)*(20R/24R)
V46	VinN8+(VinN7- VinN8)*(18R/24R)
V47	VinN8+(VinN7- VinN8)*(16R/24R)
V48	VinN8+(VinN7- VinN8)*(14R/24R)
V49	VinN8+(VinN7- VinN8)*(12R/24R)
V50	VinN8+(VinN7- VinN8)*(10R/24R)
V51	VinN8+(VinN7- VinN8)*(8R/24R)
V52	VinN8+(VinN7- VinN8)*(6R/24R)
V53	VinN8+(VinN7- VinN8)*(4R/24R)
V54	VinN8+(VinN7- VinN8)*(2R/24R)
V55	VinN8
V56	VinN9+ (VinN8 – VinN9)*CB1
V57	VinN9+ (VinN8 – VinN9)*CB2
V58	VinN9+ (VinN8 – VinN9)*CB3
V59	VinN9+ (VinN8 – VinN9)*CB4
V60	VinN9
V61	VinN10
V62	VinN11
V63	VinN12

Table 7.19 Voltage calculation formula of 64-grayscale voltage (negative polarity)

CGMN0[1:0]	"00"	"01"	"10"	"11"
CT1	4/5	2/3	3/5	31/41
CT2	3/5	1/2	9/20	22/41
CT3	2/5	1/3	3/10	14/41
CT4	1/5	1/6	3/20	6/41

CGMN1[1:0]	"00"	"01"	"10"	"11"
CB1	4/5	5/6	17/20	13/16
CB2	3/5	2/3	7/10	5/8
CB3	2/5	1/2	11/20	41/96
CB4	1/5	1/3	2/5	7/32

Table 7.20 Voltage calculation formula of grayscale voltage V2~V7 and V56~V61

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Relationship between GRAM Data and Output Level (INVON = 0 "Normally White Panel", GRAM data=0)

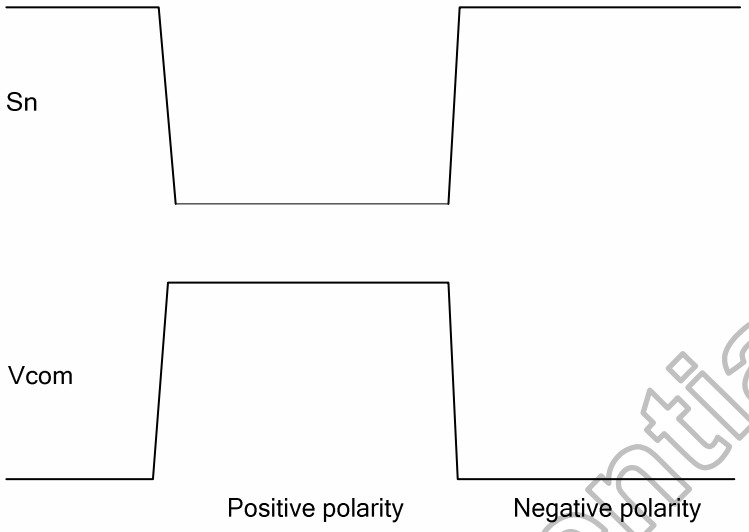
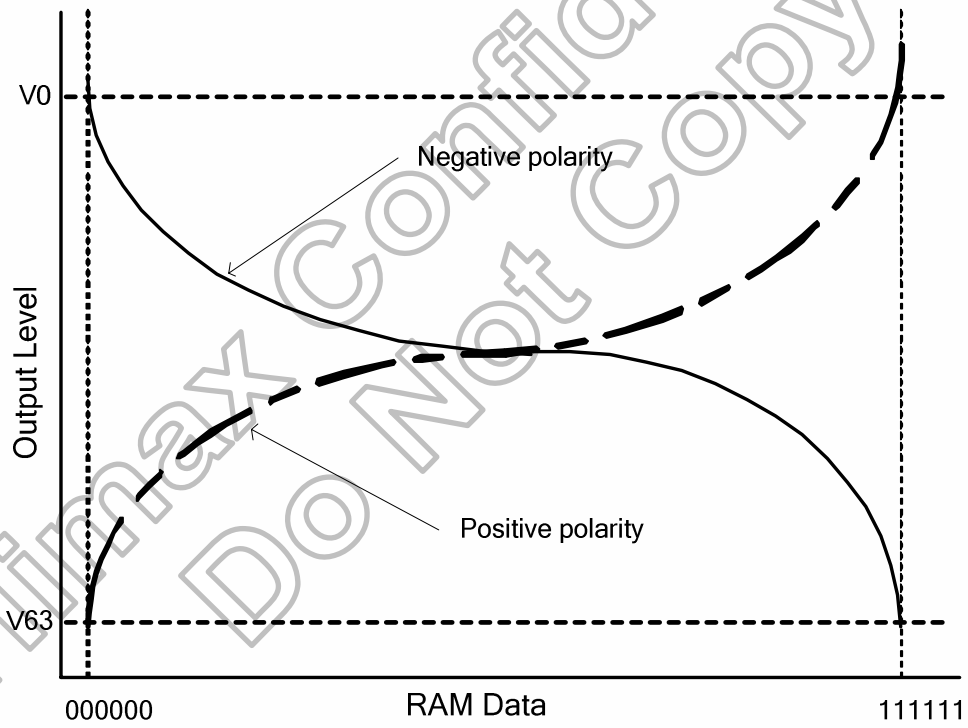


Figure 7.6 Relationship between source output and Vcom



(Same characteristic for each RGB)

Figure 7.7 Relationship between GRAM data and output level (normal white panel INVON="0")

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7.2.2 Gray voltage generator for digital gamma correction

The HX8352-B01 digital gamma correction can reach the independent GAMMA curve of RGB. HX8352-B01 utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

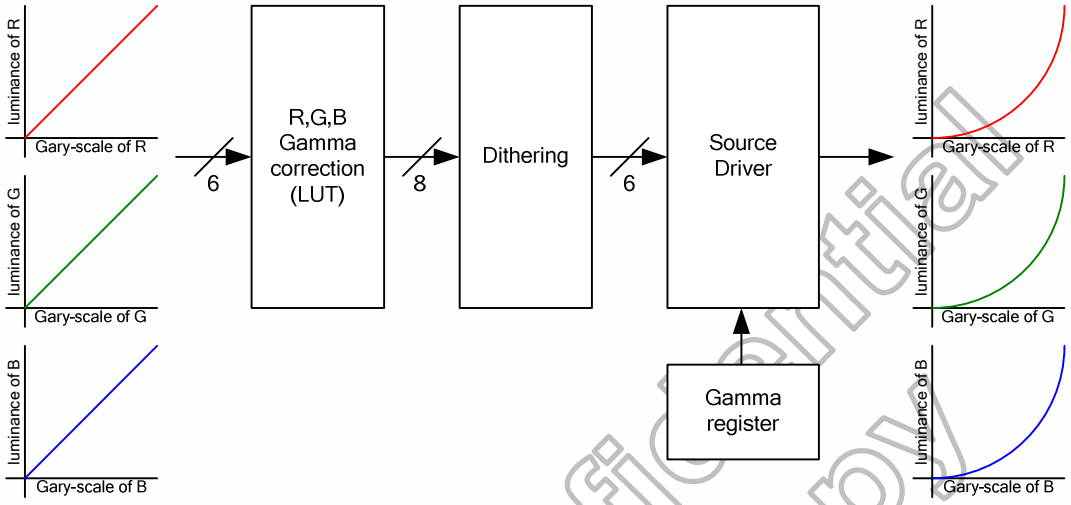

Figure 7.8 Block diagram of digital gamma correction

The HX8352-B01 builds one 192-byte DGC_LUT (Digital Gamma Correction Look Up Table) to transfer every display data of Dithering circuit input and setting by DGLUT register.

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DGC_LUT Parameter byte	Command set		R input (6 bit)	R output (8bit)
	Page	Address		
1	01h	R01h	000000	R_{007} $R_{006}R_{005}$ $R_{004}R_{003}R_{002}R_{001}R_{000}$
2	01h	R02h	000001	$R_{017}R_{016}R_{015}R_{014}R_{013}R_{012}R_{011}R_{010}$
3	01h	R03h	000010	$R_{027}R_{026}R_{025}R_{024}R_{023}R_{022}R_{021}R_{020}$
4	01h	R04h	000011	$R_{037}R_{036}R_{035}R_{034}R_{033}R_{032}R_{031}R_{030}$
5	01h	R05h	000100	$R_{047}R_{046}R_{045}R_{044}R_{043}R_{042}R_{041}R_{040}$
6	01h	R06h	000101	$R_{057}R_{056}R_{055}R_{054}R_{053}R_{052}R_{051}R_{050}$
7	01h	R07h	000110	$R_{067}R_{066}R_{065}R_{064}R_{063}R_{062}R_{061}R_{060}$
8	01h	R08h	000111	$R_{077}R_{076}R_{075}R_{074}R_{073}R_{072}R_{071}R_{070}$
9	01h	R09h	001000	$R_{087}R_{086}R_{085}R_{084}R_{083}R_{082}R_{081}R_{080}$
10	01h	R0Ah	001001	$R_{097}R_{096}R_{095}R_{094}R_{093}R_{092}R_{091}R_{090}$
11	01h	R0Bh	001010	$R_{107}R_{106}R_{105}R_{104}R_{103}R_{102}R_{101}R_{100}$
12	01h	R0Ch	001011	$R_{117}R_{116}R_{115}R_{114}R_{113}R_{112}R_{111}R_{110}$
13	01h	R0Dh	001100	$R_{127}R_{126}R_{125}R_{124}R_{123}R_{122}R_{121}R_{120}$
14	01h	R0Eh	001101	$R_{137}R_{136}R_{135}R_{134}R_{133}R_{132}R_{131}R_{130}$
15	01h	R0Fh	001110	$R_{147}R_{146}R_{145}R_{144}R_{143}R_{142}R_{141}R_{140}$
16	01h	R10h	001111	$R_{157}R_{156}R_{155}R_{154}R_{153}R_{152}R_{151}R_{150}$
17	01h	R11h	010000	R_{167} $R_{166}R_{165}$ $R_{164}R_{163}R_{162}R_{161}R_{160}$
18	01h	R12h	010001	$R_{177}R_{176}R_{175}R_{174}R_{173}R_{172}R_{171}R_{170}$
19	01h	R13h	010010	$R_{187}R_{186}R_{185}R_{184}R_{183}R_{182}R_{181}R_{180}$
20	01h	R14h	010011	$R_{197}R_{196}R_{195}R_{194}R_{193}R_{192}R_{191}R_{190}$
21	01h	R15h	010100	$R_{207}R_{206}R_{205}R_{204}R_{203}R_{202}R_{201}R_{200}$
22	01h	R16h	010101	$R_{217}R_{216}R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$
23	01h	R17h	010110	$R_{227}R_{226}R_{225}R_{224}R_{223}R_{222}R_{221}R_{220}$
24	01h	R18h	010111	$R_{237}R_{236}R_{235}R_{234}R_{233}R_{232}R_{231}R_{230}$
25	01h	R19h	011000	$R_{247}R_{246}R_{245}R_{244}R_{243}R_{242}R_{241}R_{240}$
26	01h	R1Ah	011001	$R_{257}R_{256}R_{255}R_{254}R_{253}R_{252}R_{251}R_{250}$
27	01h	R1Bh	011010	$R_{267}R_{266}R_{265}R_{264}R_{263}R_{262}R_{261}R_{260}$
28	01h	R1Ch	011011	$R_{277}R_{276}R_{275}R_{274}R_{273}R_{272}R_{271}R_{270}$
29	01h	R1Dh	011100	$R_{287}R_{286}R_{285}R_{284}R_{283}R_{282}R_{281}R_{280}$
30	01h	R1Eh	011101	$R_{297}R_{296}R_{295}R_{294}R_{293}R_{292}R_{291}R_{290}$
31	01h	R1Fh	011110	$R_{307}R_{306}R_{305}R_{304}R_{303}R_{302}R_{301}R_{300}$
32	01h	R20h	011111	$R_{317}R_{316}R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$

Table 7.21 DGLUT for red color (1)

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DGC_LUT Parameter byte	Command		R input (6 bit)	R output (8bit)
	Page	Address		
33	01h	R21h	100000	R_{327} $R_{326}R_{325}$ $R_{324}R_{323}R_{322}R_{321}R_{320}$
34	01h	R22h	100001	$R_{337}R_{336}R_{335}R_{334}R_{333}R_{332}R_{331}R_{330}$
35	01h	R23h	100010	$R_{347}R_{346}R_{345}R_{344}R_{343}R_{342}R_{341}R_{340}$
36	01h	R24h	100011	$R_{357}R_{356}R_{355}R_{354}R_{353}R_{352}R_{351}R_{350}$
37	01h	R25h	100100	$R_{367}R_{366}R_{365}R_{364}R_{363}R_{362}R_{361}R_{360}$
38	01h	R26h	100101	$R_{377}R_{376}R_{375}R_{374}R_{373}R_{372}R_{371}R_{370}$
39	01h	R27h	100110	$R_{387}R_{386}R_{385}R_{384}R_{383}R_{382}R_{381}R_{380}$
40	01h	R28h	100111	$R_{397}R_{396}R_{395}R_{394}R_{393}R_{392}R_{391}R_{390}$
41	01h	R29h	101000	$R_{407}R_{406}R_{405}R_{404}R_{403}R_{402}R_{401}R_{400}$
42	01h	R2Ah	101001	$R_{417}R_{416}R_{415}R_{414}R_{413}R_{412}R_{411}R_{410}$
43	01h	R2Bh	101010	$R_{427}R_{426}R_{425}R_{424}R_{423}R_{422}R_{421}R_{420}$
44	01h	R2Ch	101011	$R_{437}R_{436}R_{435}R_{434}R_{433}R_{432}R_{431}R_{430}$
45	01h	R2Dh	101100	$R_{447}R_{446}R_{445}R_{444}R_{443}R_{442}R_{441}R_{440}$
46	01h	R2Eh	101101	$R_{457}R_{456}R_{455}R_{454}R_{453}R_{452}R_{451}R_{450}$
47	01h	R2Fh	101110	$R_{467}R_{466}R_{465}R_{464}R_{463}R_{462}R_{461}R_{460}$
48	01h	R30h	101111	$R_{477}R_{476}R_{475}R_{474}R_{473}R_{472}R_{471}R_{470}$
49	01h	R31h	110000	R_{487} $R_{486}R_{485}$ $R_{484}R_{483}R_{482}R_{481}R_{480}$
50	01h	R32h	110001	$R_{497}R_{496}R_{495}R_{494}R_{493}R_{492}R_{491}R_{490}$
51	01h	R33h	110010	$R_{507}R_{506}R_{505}R_{504}R_{503}R_{502}R_{501}R_{500}$
52	01h	R34h	110011	$R_{517}R_{516}R_{515}R_{514}R_{513}R_{512}R_{511}R_{510}$
53	01h	R35h	110100	$R_{527}R_{526}R_{525}R_{524}R_{523}R_{522}R_{521}R_{520}$
54	01h	R36h	110101	$R_{537}R_{536}R_{535}R_{534}R_{533}R_{532}R_{531}R_{530}$
55	01h	R37h	110110	$R_{547}R_{546}R_{545}R_{544}R_{543}R_{542}R_{541}R_{540}$
56	01h	R38h	110111	$R_{557}R_{556}R_{555}R_{554}R_{553}R_{552}R_{551}R_{550}$
57	01h	R39h	111000	$R_{567}R_{566}R_{565}R_{564}R_{563}R_{562}R_{561}R_{560}$
58	01h	R3Ah	111001	$R_{577}R_{576}R_{575}R_{574}R_{573}R_{572}R_{571}R_{570}$
59	01h	R3Bh	111010	$R_{587}R_{586}R_{585}R_{584}R_{583}R_{582}R_{581}R_{580}$
60	01h	R3Ch	111011	$R_{597}R_{596}R_{595}R_{594}R_{593}R_{592}R_{591}R_{590}$
61	01h	R3Dh	111100	$R_{607}R_{606}R_{605}R_{604}R_{603}R_{602}R_{601}R_{600}$
62	01h	R3Eh	111101	$R_{617}R_{616}R_{615}R_{614}R_{613}R_{612}R_{611}R_{610}$
63	01h	R3Fh	111110	$R_{627}R_{626}R_{625}R_{624}R_{623}R_{622}R_{621}R_{620}$
64	01h	R40h	111111	$R_{637}R_{636}R_{635}R_{634}R_{633}R_{632}R_{631}R_{630}$

Table 7.22 DGLUT for red color (2)

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DGC_LUT Parameter byte	Command		G input (6 bit)	G output (8bit)
	Page	Address		
65	01h	R41h	000000	G_{007} $G_{006}G_{005}$ $G_{004}G_{003}G_{002}G_{001}G_{000}$
66	01h	R42h	000001	$G_{017}G_{016}G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$
67	01h	R43h	000010	$G_{027}G_{026}G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$
68	01h	R44h	000011	$G_{037}G_{036}G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$
69	01h	R45h	000100	$G_{047}G_{046}G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$
70	01h	R46h	000101	$G_{057}G_{056}G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$
71	01h	R47h	000110	$G_{067}G_{066}G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$
72	01h	R48h	000111	$G_{077}G_{076}G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$
73	01h	R49h	001000	$G_{087}G_{086}G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$
74	01h	R4Ah	001001	$G_{097}G_{096}G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$
75	01h	R4Bh	001010	$G_{107}G_{106}G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$
76	01h	R4Ch	001011	$G_{117}G_{116}G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$
77	01h	R4Dh	001100	$G_{127}G_{126}G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$
78	01h	R4Eh	001101	$G_{137}G_{136}G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$
79	01h	R4Fh	001110	$G_{147}G_{146}G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$
80	01h	R50h	001111	$G_{157}G_{156}G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$
81	01h	R51h	010000	G_{167} $G_{166}G_{165}$ $G_{164}G_{163}G_{162}G_{161}G_{160}$
82	01h	R52h	010001	$G_{177}G_{176}G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$
83	01h	R53h	010010	$G_{187}G_{186}G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$
84	01h	R54h	010011	$G_{197}G_{196}G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$
85	01h	R55h	010100	$G_{207}G_{206}G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$
86	01h	R56h	010101	$G_{217}G_{216}G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$
87	01h	R57h	010110	$G_{227}G_{226}G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$
88	01h	R58h	010111	$G_{237}G_{236}G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$
89	01h	R59h	011000	$G_{247}G_{246}G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$
90	01h	R5Ah	011001	$G_{257}G_{256}G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$
91	01h	R5Bh	011010	$G_{267}G_{266}G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$
92	01h	R5Ch	011011	$G_{277}G_{276}G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$
93	01h	R5Dh	011100	$G_{287}G_{286}G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$
94	01h	R5Eh	011101	$G_{297}G_{296}G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$
95	01h	R5Fh	011110	$G_{307}G_{306}G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$
96	01h	R60h	011111	$G_{317}G_{316}G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$

Table 7.23 DGLUT for green color (1)

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DGC_LUT Parameter byte	Command		G input (6 bit)	G output (8bit)
	Page	Address		
97	01h	R61h	100000	G_{327} $G_{326}G_{325}$ $G_{324}G_{323}G_{322}G_{321}G_{320}$
98	01h	R62h	100001	$G_{337}G_{336}G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$
99	01h	R63h	100010	$G_{347}G_{346}G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$
100	01h	R64h	100011	$G_{357}G_{356}G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$
101	01h	R65h	100100	$G_{367}G_{366}G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$
102	01h	R66h	100101	$G_{377}G_{376}G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$
103	01h	R67h	100110	$G_{387}G_{386}G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$
104	01h	R68h	100111	$G_{397}G_{396}G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$
105	01h	R69h	101000	$G_{407}G_{406}G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$
106	01h	R6Ah	101001	$G_{417}G_{416}G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$
107	01h	R6Bh	101010	$G_{427}G_{426}G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$
108	01h	R6Ch	101011	$G_{437}G_{436}G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$
109	01h	R6Dh	101100	$G_{447}G_{446}G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$
110	01h	R6Eh	101101	$G_{457}G_{456}G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$
111	01h	R6Fh	101110	$G_{467}G_{466}G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$
112	01h	R70h	101111	$G_{477}G_{476}G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$
113	01h	R71h	110000	G_{487} $G_{486}G_{485}$ $G_{484}G_{483}G_{482}G_{481}G_{480}$
114	01h	R72h	110001	$G_{497}G_{496}G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$
115	01h	R73h	110010	$G_{507}G_{506}G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$
116	01h	R74h	110011	$G_{517}G_{516}G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$
117	01h	R75h	110100	$G_{527}G_{526}G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$
118	01h	R76h	110101	$G_{537}G_{536}G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$
119	01h	R77h	110110	$G_{547}G_{546}G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$
120	01h	R78h	110111	$G_{557}G_{556}G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$
121	01h	R79h	111000	$G_{567}G_{566}G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$
122	01h	R7Ah	111001	$G_{577}G_{576}G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$
123	01h	R7Bh	111010	$G_{587}G_{586}G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$
124	01h	R7Ch	111011	$G_{597}G_{596}G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$
125	01h	R7Dh	111100	$G_{607}G_{606}G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$
126	01h	R7Eh	111101	$G_{617}G_{616}G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$
127	01h	R7Fh	111110	$G_{627}G_{626}G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$
128	01h	R80h	111111	$G_{637}G_{636}G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$

Table 7.24 DGLUT for green color (2)

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DGC_LUT Parameter byte	Command		B input (6 bit)	B output (8bit)
	Page	Address		
129	01h	R81h	000000	B_{007} $B_{006}B_{005}$ $B_{004}B_{003}B_{002}B_{001}B_{000}$
130	01h	R82h	000001	$B_{017}B_{016}B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$
131	01h	R83h	000010	$B_{027}B_{026}B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$
132	01h	R84h	000011	$B_{037}B_{036}B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$
133	01h	R85h	000100	$B_{047}B_{046}B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$
134	01h	R86h	000101	$B_{057}B_{056}B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$
135	01h	R87h	000110	$B_{067}B_{066}B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$
136	01h	R88h	000111	$B_{077}B_{076}B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$
137	01h	R89h	001000	$B_{087}B_{086}B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$
138	01h	R8Ah	001001	$B_{097}B_{096}B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$
139	01h	R8Bh	001010	$B_{107}B_{106}B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$
140	01h	R8Ch	001011	$B_{117}B_{116}B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$
141	01h	R8Dh	001100	$B_{127}B_{126}B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$
142	01h	R8Eh	001101	$B_{137}B_{136}B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$
143	01h	R8Fh	001110	$B_{147}B_{146}B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$
144	01h	R90h	001111	$B_{157}B_{156}B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$
145	01h	R91h	010000	B_{167} $B_{166}B_{165}$ $B_{164}B_{163}B_{162}B_{161}B_{160}$
146	01h	R92h	010001	$B_{177}B_{176}B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$
147	01h	R93h	010010	$B_{187}B_{186}B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$
148	01h	R94h	010011	$B_{197}B_{196}B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$
149	01h	R95h	010100	$B_{207}B_{206}B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$
150	01h	R96h	010101	$B_{217}B_{216}B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$
151	01h	R97h	010110	$B_{227}B_{226}B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$
152	01h	R98h	010111	$B_{237}B_{236}B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$
153	01h	R99h	011000	$B_{247}B_{246}B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$
154	01h	R9Ah	011001	$B_{257}B_{256}B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$
155	01h	R9Bh	011010	$B_{267}B_{266}B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$
156	01h	R9Ch	011011	$B_{277}B_{276}B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$
157	01h	R9Dh	011100	$B_{287}B_{286}B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$
158	01h	R9Eh	011101	$B_{297}B_{296}B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$
159	01h	R9Fh	011110	$B_{307}B_{306}B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$
160	01h	RA0h	011111	$B_{317}B_{316}B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$

Table 7.25 DGLUT for blue color (1)

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DGC_LUT Parameter byte	Command		B input (6 bit)	B output (8bit)
	Page	Address		
161	01h	RA1h	100000	B_{327} $B_{326}B_{325}$ $B_{324}B_{323}B_{322}B_{321}B_{320}$
162	01h	RA2h	100001	$B_{337}B_{336}B_{335}B_{334}B_{333}B_{332}B_{331}B_{330}$
163	01h	RA3h	100010	$B_{347}B_{346}B_{345}B_{344}B_{343}B_{342}B_{341}B_{340}$
164	01h	RA4h	100011	$B_{357}B_{356}B_{355}B_{354}B_{353}B_{352}B_{351}B_{350}$
165	01h	RA5h	100100	$B_{367}B_{366}B_{365}B_{364}B_{363}B_{362}B_{361}B_{360}$
166	01h	RA6h	100101	$B_{377}B_{376}B_{375}B_{374}B_{373}B_{372}B_{371}B_{370}$
167	01h	RA7h	100110	$B_{387}B_{386}B_{385}B_{384}B_{383}B_{382}B_{381}B_{380}$
168	01h	RA8h	100111	$B_{397}B_{396}B_{395}B_{394}B_{393}B_{392}B_{391}B_{390}$
169	01h	RA9h	101000	$B_{407}B_{406}B_{405}B_{404}B_{403}B_{402}B_{401}B_{400}$
170	01h	RAAh	101001	$B_{417}B_{416}B_{415}B_{414}B_{413}B_{412}B_{411}B_{410}$
171	01h	RABh	101010	$B_{427}B_{426}B_{425}B_{424}B_{423}B_{422}B_{421}B_{420}$
172	01h	RACh	101011	$B_{437}B_{436}B_{435}B_{434}B_{433}B_{432}B_{431}B_{430}$
173	01h	RADh	101100	$B_{447}B_{446}B_{445}B_{444}B_{443}B_{442}B_{441}B_{440}$
174	01h	RAEh	101101	$B_{457}B_{456}B_{455}B_{454}B_{453}B_{452}B_{451}B_{450}$
175	01h	RAFh	101110	$B_{467}B_{466}B_{465}B_{464}B_{463}B_{462}B_{461}B_{460}$
176	01h	RB0h	101111	$B_{477}B_{476}B_{475}B_{474}B_{473}B_{472}B_{471}B_{470}$
177	01h	RB1h	110000	B_{487} $B_{486}B_{485}$ $B_{484}B_{483}B_{482}B_{481}B_{480}$
178	01h	RB2h	110001	$B_{497}B_{496}B_{495}B_{494}B_{493}B_{492}B_{491}B_{490}$
179	01h	RB3h	110010	$B_{507}B_{506}B_{505}B_{504}B_{503}B_{502}B_{501}B_{500}$
180	01h	RB4h	110011	$B_{517}B_{516}B_{515}B_{514}B_{513}B_{512}B_{511}B_{510}$
181	01h	RB5h	110100	$B_{527}B_{526}B_{525}B_{524}B_{523}B_{522}B_{521}B_{520}$
182	01h	RB6h	110101	$B_{537}B_{536}B_{535}B_{534}B_{533}B_{532}B_{531}B_{530}$
183	01h	RB7h	110110	$B_{547}B_{546}B_{545}B_{544}B_{543}B_{542}B_{541}B_{540}$
184	01h	RB8h	110111	$B_{557}B_{556}B_{555}B_{554}B_{553}B_{552}B_{551}B_{550}$
185	01h	RB9h	111000	$B_{567}B_{566}B_{565}B_{564}B_{563}B_{562}B_{561}B_{560}$
186	01h	RBAh	111001	$B_{577}B_{576}B_{575}B_{574}B_{573}B_{572}B_{571}B_{570}$
187	01h	RBBh	111010	$B_{587}B_{586}B_{585}B_{584}B_{583}B_{582}B_{581}B_{580}$
188	01h	RBCh	111011	$B_{597}B_{596}B_{595}B_{594}B_{593}B_{592}B_{591}B_{590}$
189	01h	RBDh	111100	$B_{607}B_{606}B_{605}B_{604}B_{603}B_{602}B_{601}B_{600}$
190	01h	RBEh	111101	$B_{617}B_{616}B_{615}B_{614}B_{613}B_{612}B_{611}B_{610}$
191	01h	RBFh	111110	$B_{627}B_{626}B_{625}B_{624}B_{623}B_{622}B_{621}B_{620}$
192	01h	RC0h	111111	$B_{637}B_{636}B_{635}B_{634}B_{633}B_{632}B_{631}B_{630}$

Table 7.26 DGLUT for blue color (2)

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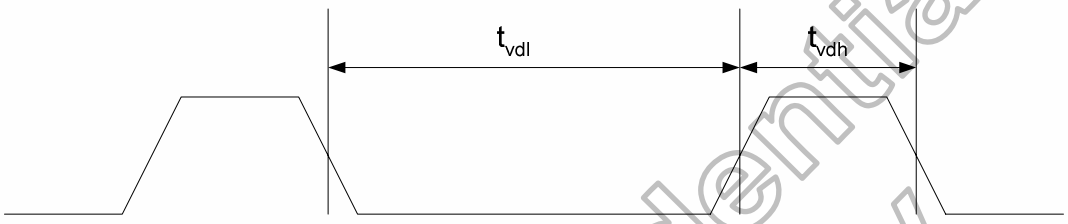
7.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images. Tearing effect function is not supported in RGB interface mode.

7.3.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

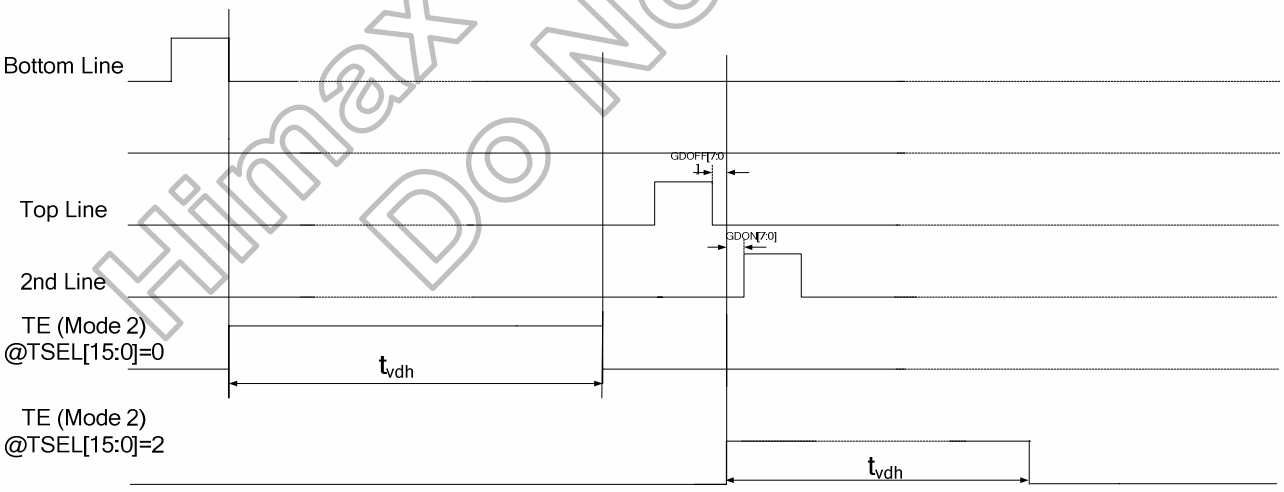


t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Figure 7.9 TE Mode 1 output

Under Mode 1, the TE ouptu tming will define by TSEL[15:0] setting.
Example:

(1) TSEL[15:0]=0, then TE signal will output after last Line finished.
(2) TSEL[15:0]=2, then TE signal will output after second Line finished.



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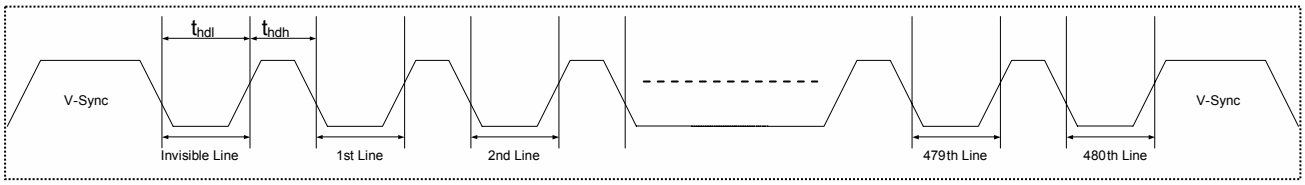
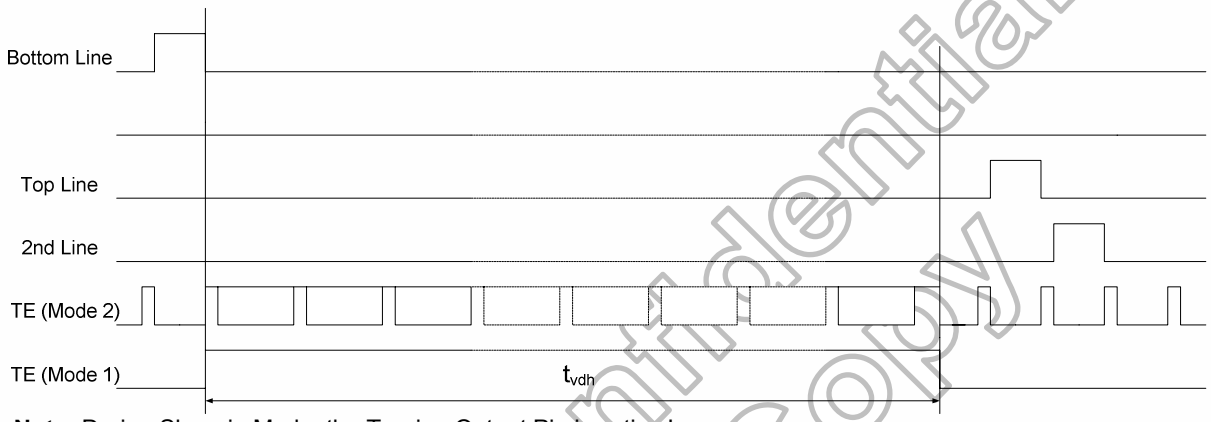
Mode 2 the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 432 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 7.10 TE Mode 2 output



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 7.11 TE Mode 2 output

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7.3.2 Tearing effect line timing

The Tearing Effect signal is described below.

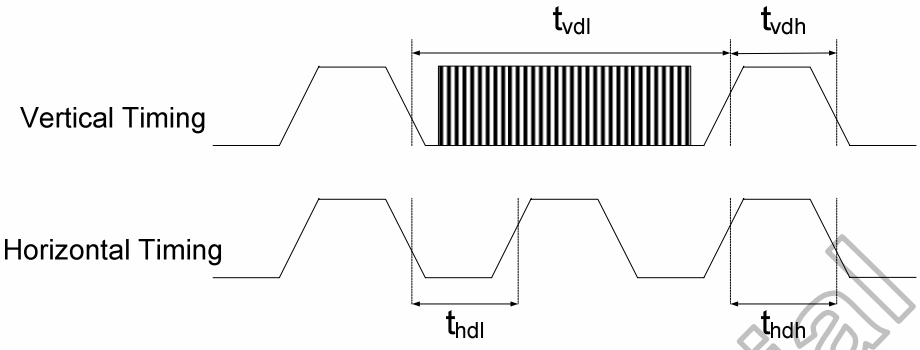

Figure 7.12 Waveform of tearing effect signal

Idle Mode Off (Frame Rate=60 Hz)

Symbol	Parameter	Spec.			Unit	Description
		Min.	Typ.	Max.		
tvdl	Vertical Timing Low Duration	-	-	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	-	µs	-
thdl	Horizontal Timing Low Duration	-	-	-	µs	-
thdh	Horizontal Timing High Duration	-	-	500	µs	-

Note: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Table 7.27 AC characteristics of tearing effect signal

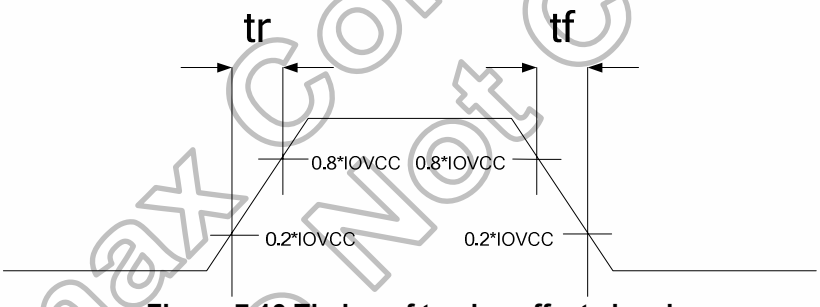

Figure 7.13 Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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7.3.3 Example 1: MPU write is faster than panel read

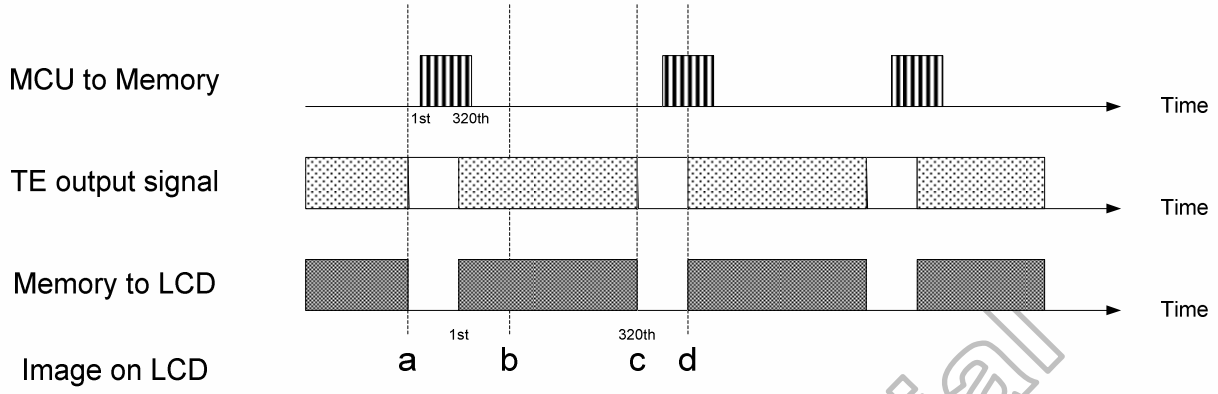

Figure 7.14 Timing of MPU write is faster than panel read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

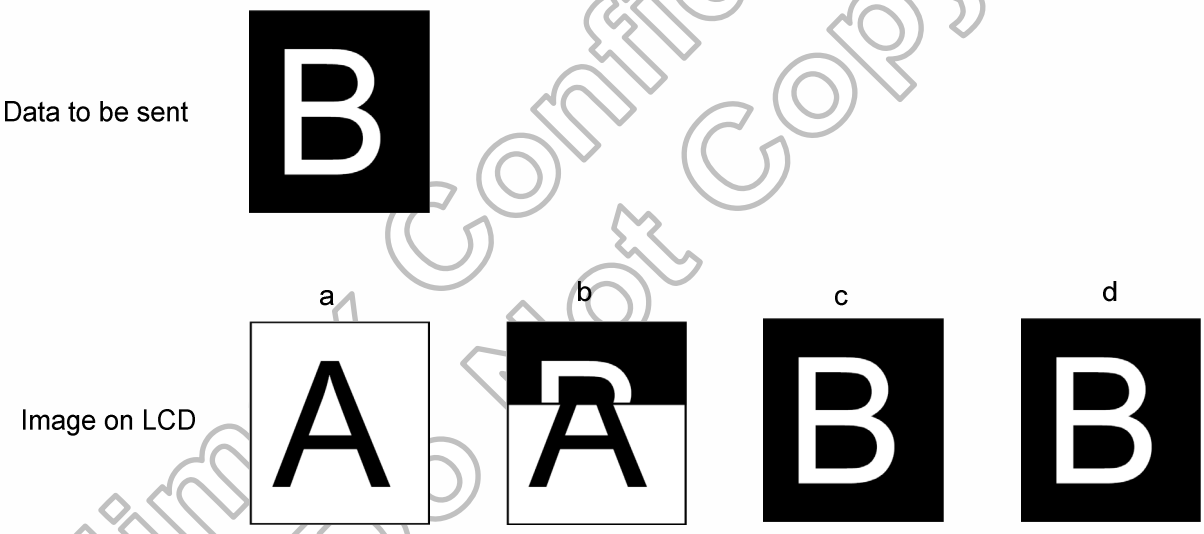

Figure 7.15 Display of MPU write is faster than panel read

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7.3.4 Example 2: MPU write is slower than panel read

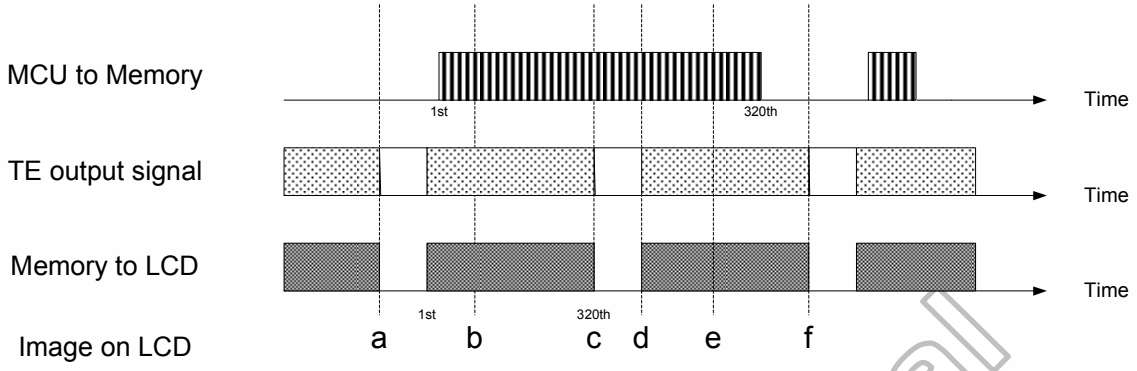

Figure 7.16 Timing of MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

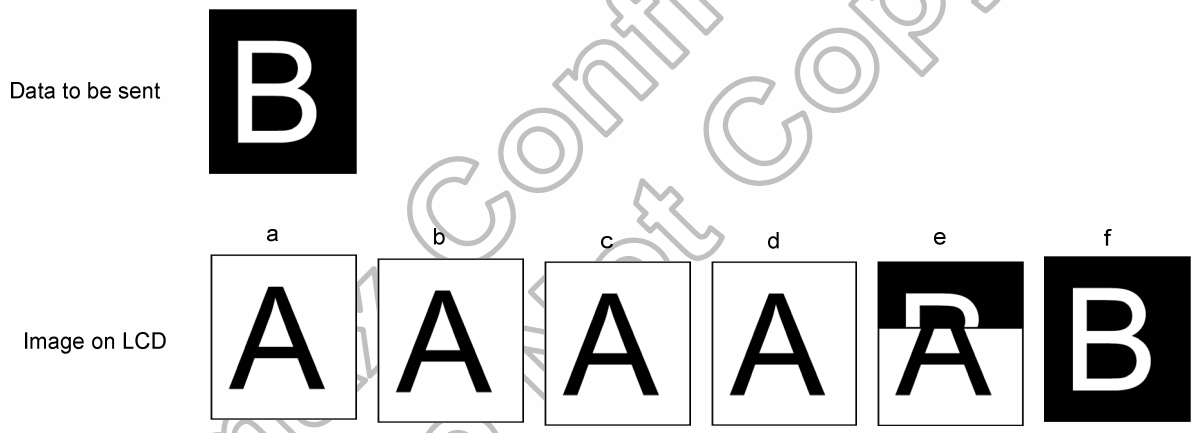

Figure 7.17 Display of MPU write is slower than panel read

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7.4 Content adaptive brightness control (CABC) function

The HX8352-B01 supports Content Adaptive Brightness Control (CABC) Function and will output one PWM signal to external LED Driver IC. The PWM signal automatically adjusts output duty by display image for saving LED backlight power consumption.

Example:

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

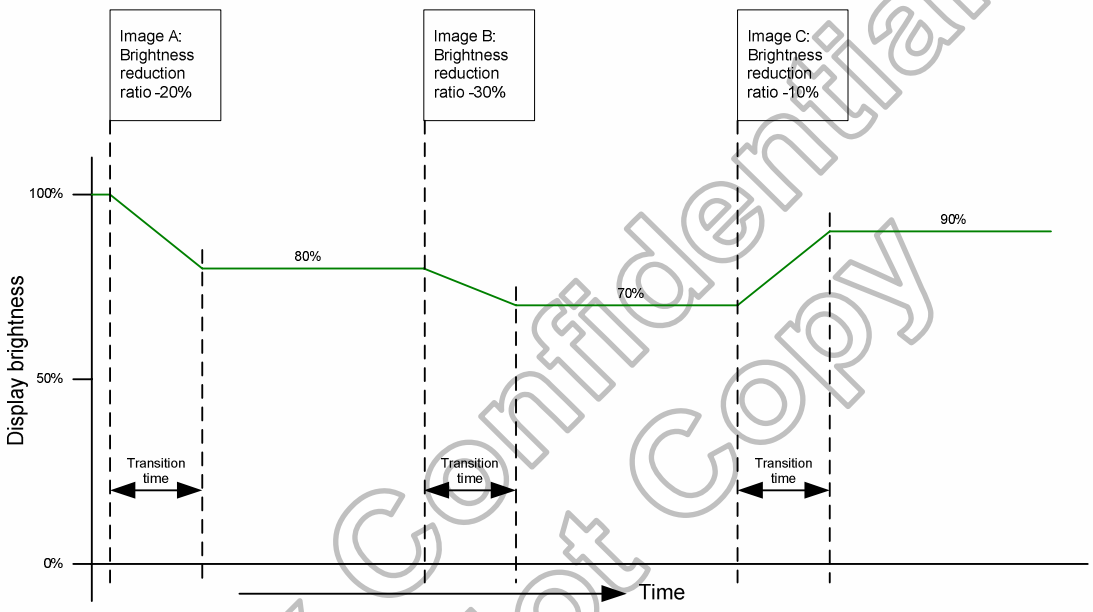

Figure 7.18 Example of CABC function

The general block diagram of the CABC and the brightness control is illustrated below:

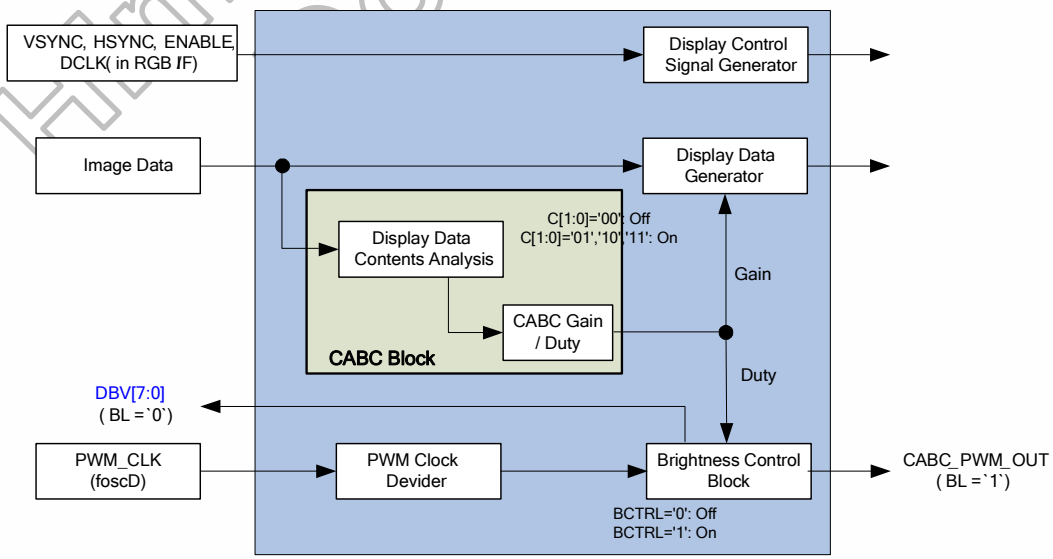

Figure 7.19 CABC block diagram

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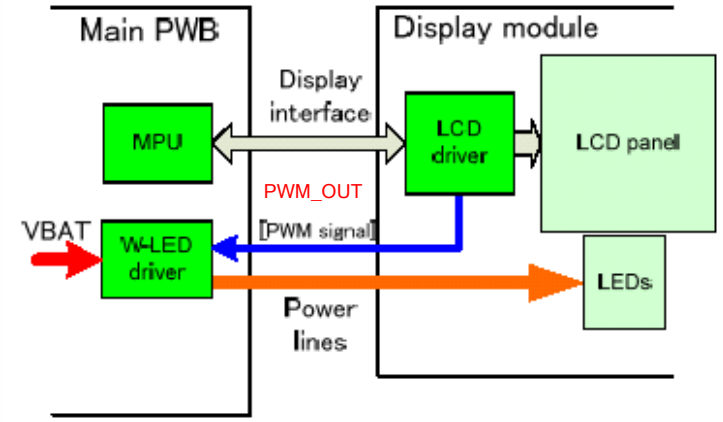
7.4.1 Module architectures

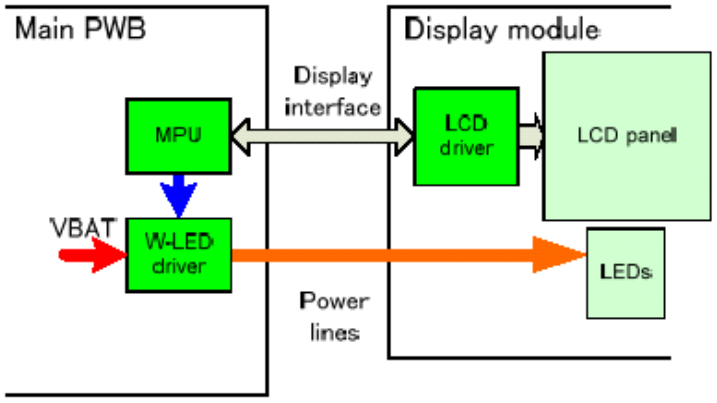
The HX8352-B01 supports two module architectures for CABC operation. The **BL** bit setting of R3Dh can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



1. **BL** =`1` of R3Dh
2. LED backlight brightness for the display is controlled by external output "PWM_OUT".

- Architecture II



1. **BL** =`0` of R3Dh
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R3Ch.
3. Read commands R3Dh should be synchronized with V-sync.

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7.4.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R3Ch, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV[7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R3Ch) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = (228) / 255 x 74.42% ≡ 66.54%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT = 0.99ms.

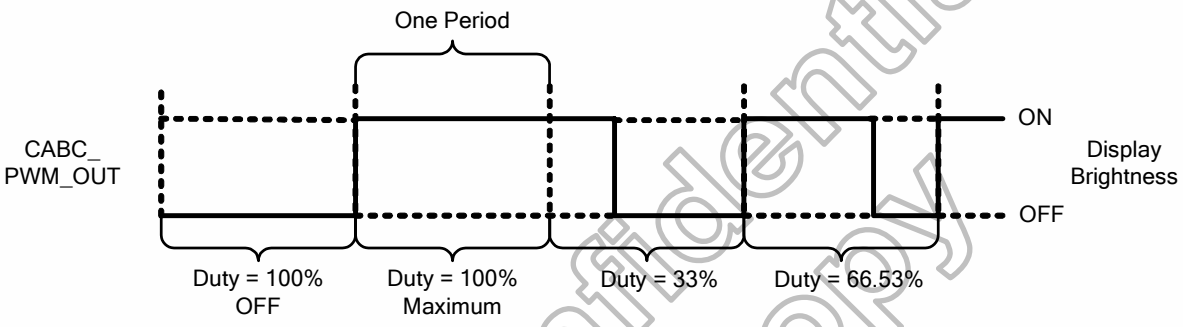

Figure 7.20 CABC_PWM_OUT output duty

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R3Ch) will be read a value as 169_{DEC} ((169)/255≡ 66.27%).

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7.4.3 Minimum brightness setting of CABC function

CABC function automatically reduces backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must cause image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R3Fh) works to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R3D), CABC minimum brightness setting is ignored. Read CABC minimum brightness **CMB[7:0]** (R3Fh) always read the setting value.

7.4.4 Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

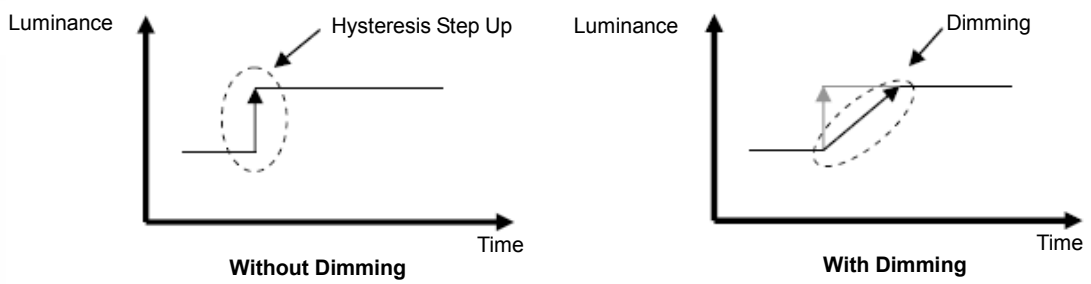

Figure 7.21 Dimming function

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7.5 Scan mode setting

The HX8352-B01 can set internal register SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8352-B01.

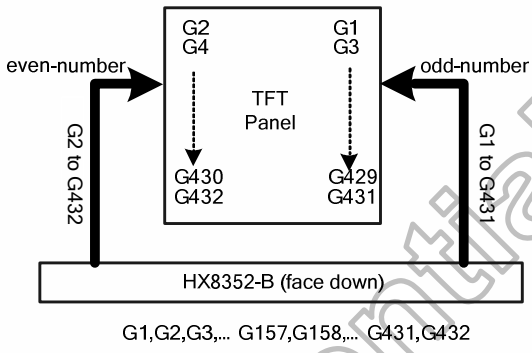
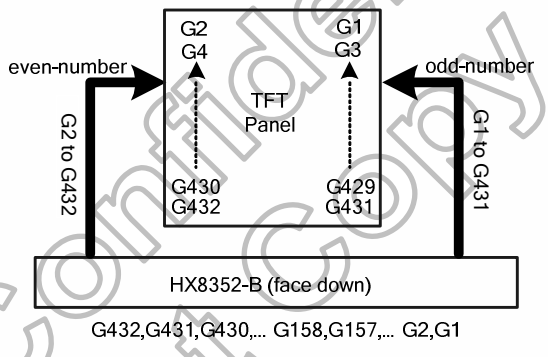
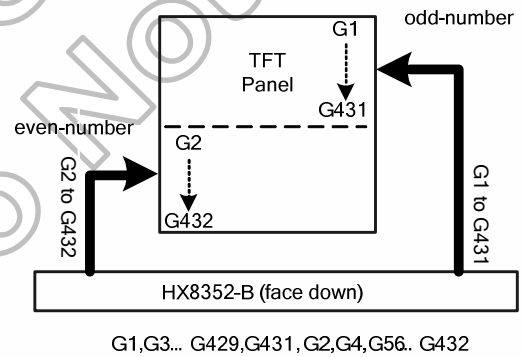
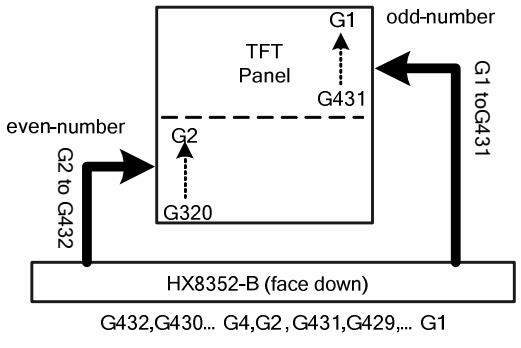
SM_PANEL	GS	Scan direction
0	0	 G1,G2,G3,... G157,G158,... G431,G432
0	1	 G432,G431,G430,... G158,G157,... G2,G1
1	0	 G1,G3... G429,G431, G2,G4,G56.. G432
1	1	 G432,G430... G4,G2 , G431,G429,... G1

Figure 7.22 Gate scan mode

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7.6 System power on/off sequence

IOVCC, VCC, VCI and MDDI_VCC can be applied in any order. IOVCC, VCC, VCI and MDDI_VDD can be powered down in any order. During power off, if LCD is in the Standby Out mode, IOVCC and VCC must be powered down minimum 120msec after NRESET has been released. During power off, if LCD is in the Standby In mode, IOVCC, VCC and VCI can be powered down minimum 0msec after NRESET has been released. NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving STB Out command. Also between receiving STB In command and Power Off Sequence. If NRESET line is not held stable by host during Power On Sequence as defined in Sections 7.6.1 and 7.6.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The system power on/off sequence is illustrated below.

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7.6.1 Case 1 – NRESET line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCC and VCI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

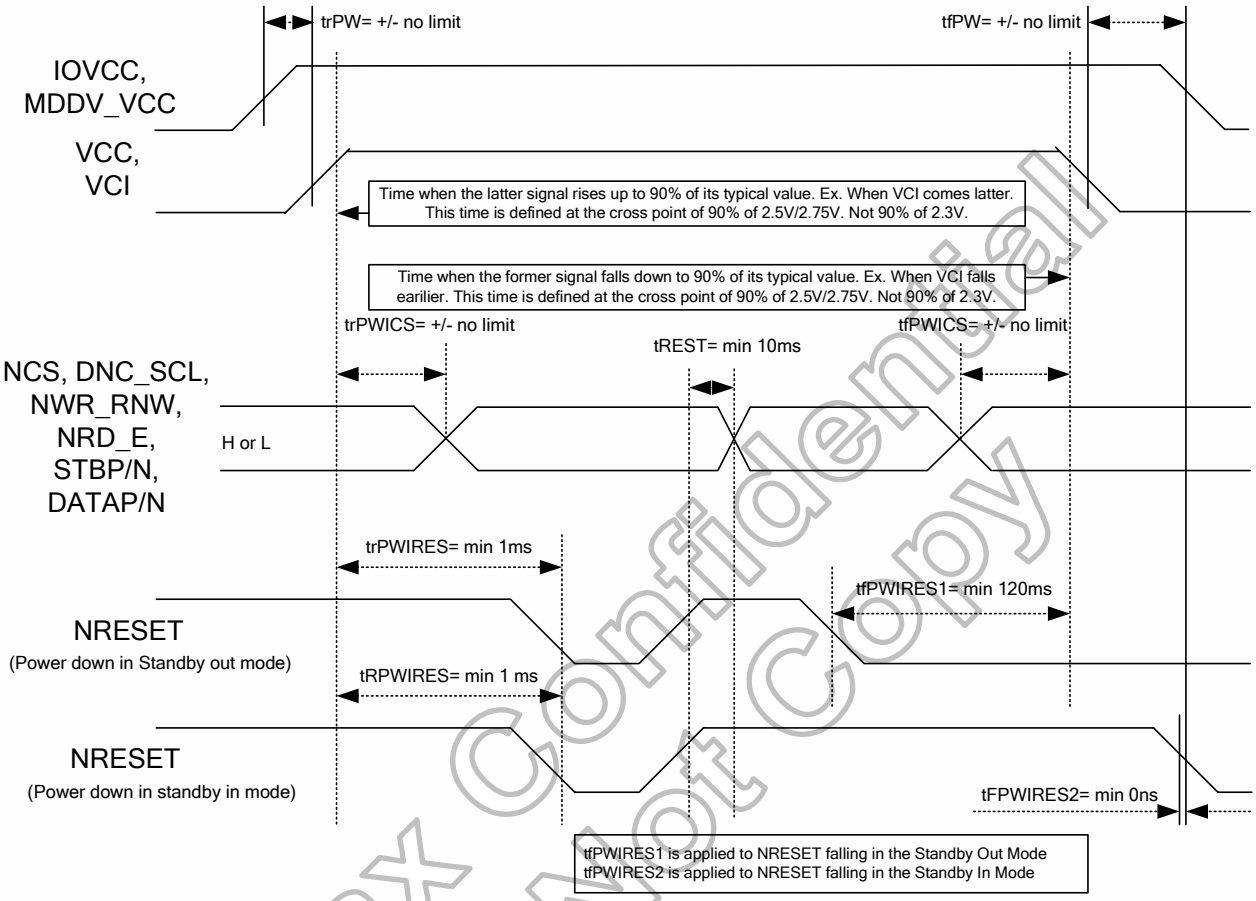

Figure 7.23 Case 1 –NRESET line is held high or unstable by host at power on

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7.6.2 Case 2 – NRESET line is held low by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 5msec after both IOVCC, VCC and VCI have been applied.

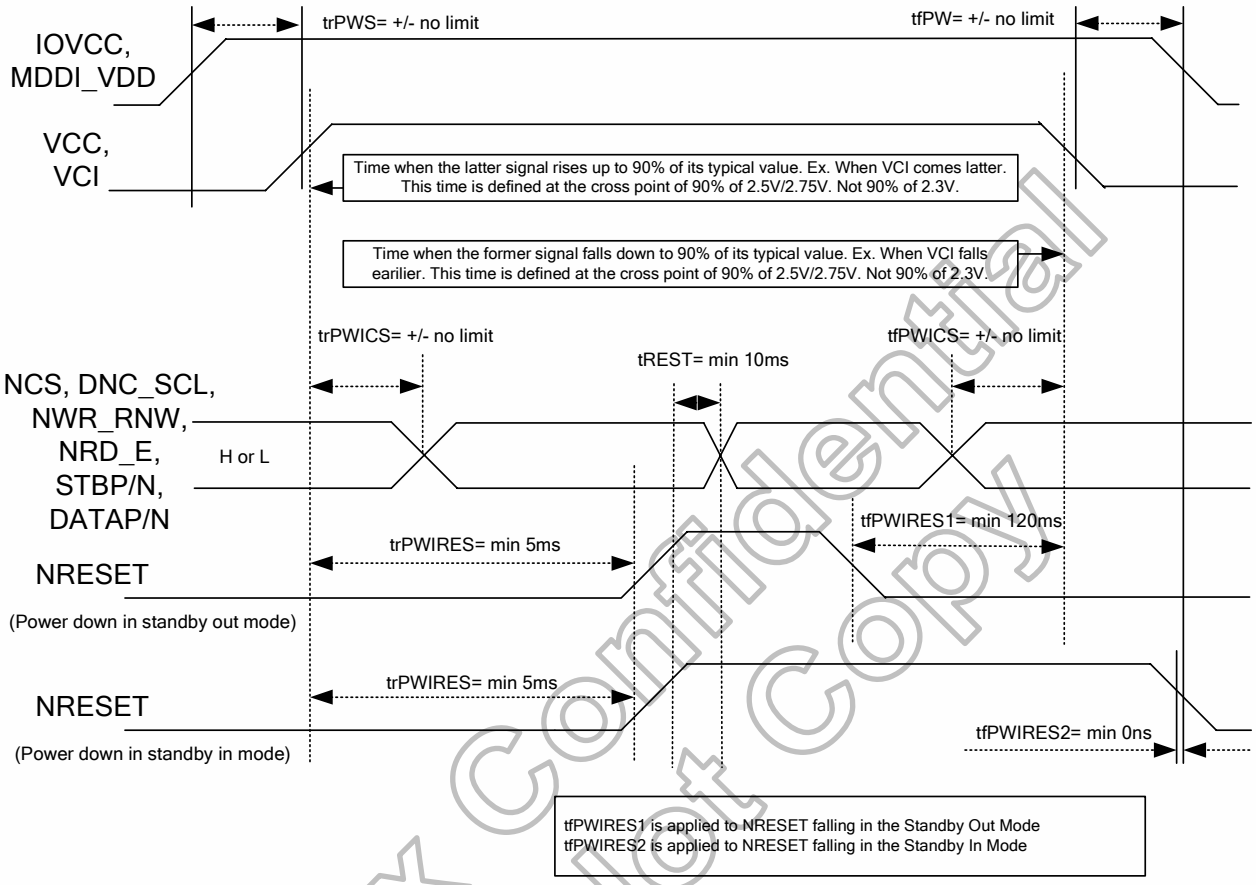

Figure 7.24 Case 2 –NRESET line is held low by host at power on

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7.7 Free running mode specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in, it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Please note that the black and the white pattern are reversed in case of a normally black display.

Parameter	Symbol	Description
Power supply pins	IOVCC, VCI, VCC	All power supply pins
Free running mode	BURN	BURN=1, FR-mode is enabled.
Reset	NRESET	Active low pulse in order to start the FR-mode.
Chip select (1)	NCS	This pin will be left open during FRM mode.
Data enable (1)	ENABLE	This pin will be left open during FRM mode.
Reads/not write (1)	NRD_E, NWR_RNW	This pin will be left open during FRM mode.
Data/not command (1)	DNC_SCL	This pin will be left open during FRM mode.
Horizontal sync (1)	HSYNC	This pin will be left open during FRM mode.
Vertical sync (1)	VSYNC	This pin will be left open during FRM mode.
Data clock	DOTCLK	This pin will be left open during FRM mode.
CPU I/F Data (1)	DB[0..17]	This pin will be left open during FRM mode.
SPI I/F Data (1)	SDI, SDO	This pin will be left open during FRM mode.

Note: (1) The BURN-pin has a pull down resistor inside the driver IC, because this pin will be left open during the normal operation in the application. The BURN-pin must be logical high for longer than 5ms before the driver IC will switch to the FR-mode in order to avoid disturbances during normal operation.
(2) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc must be disabled, all mode select pins like data-not-command, interface-select etc and all data-bus pins must be set to eider logic high or logic low during the FR-mode.

Table 7.28 Pin information of free running mode

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Power-on sequence

The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if it is supported by the driver specification. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP starts to load when Reset leaves low to high.

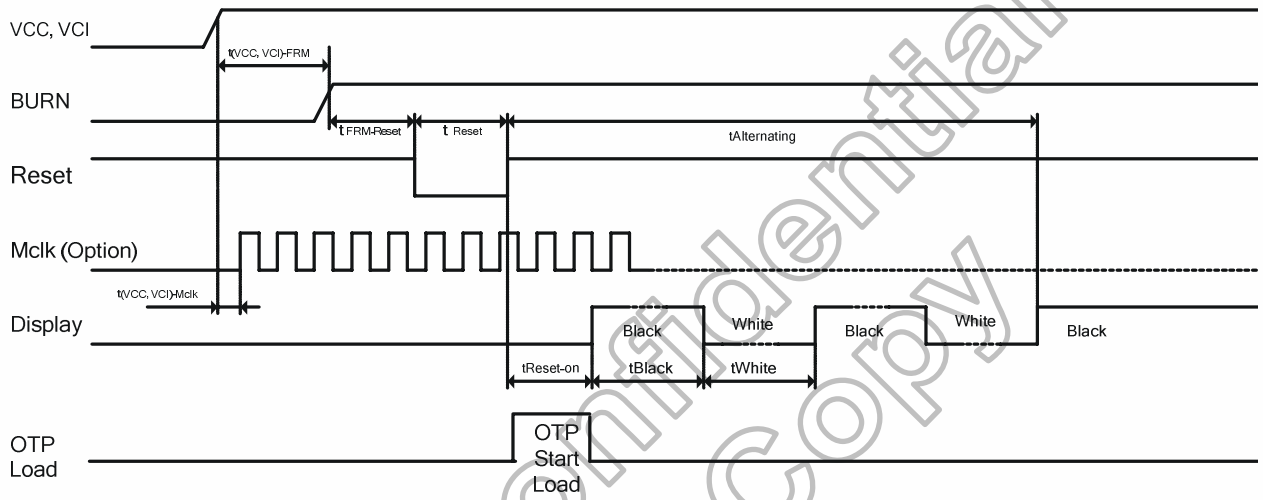

Figure 7.25 Power on sequence of FR-mode (for normally-white panel)

Power off sequence

The power supply can be switched off any time.

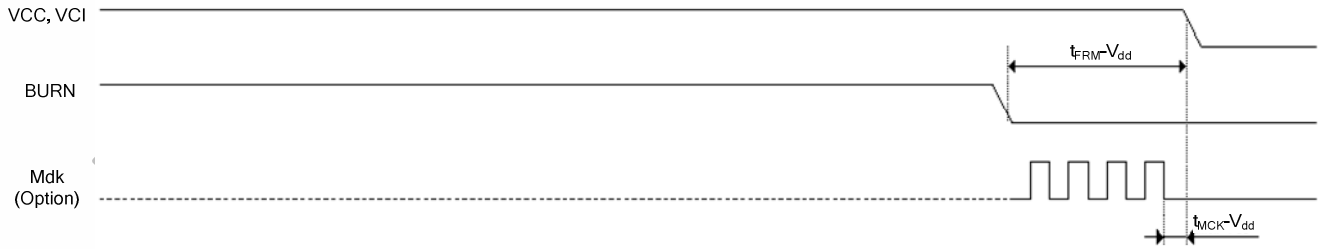

Figure 7.26 Power off sequence of FR-mode

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Free running mode display

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shell be 50%. **The time of the black and white pattern shell be around 1 seconds** in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. **The relationship between VCOM and SOURCE will keep maximum voltage difference after the alternating mode is finished.** Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. It can be between 5 and 100Hz. The frame frequency will be set according to the parameter in the OTP.

Alternating Black and White Pattern	$t_{Alternating}$	-	5	-	min
Master Clock Frequency	f_{Mclk}	-	-	10	MHz

Table 7.29 Frequency definition of free running mode display

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7.8 LCD power generation circuit

7.8.1 Power supply circuit

The power circuit of HX8352-B01 is used to generate supply voltages for LCD panel driving.

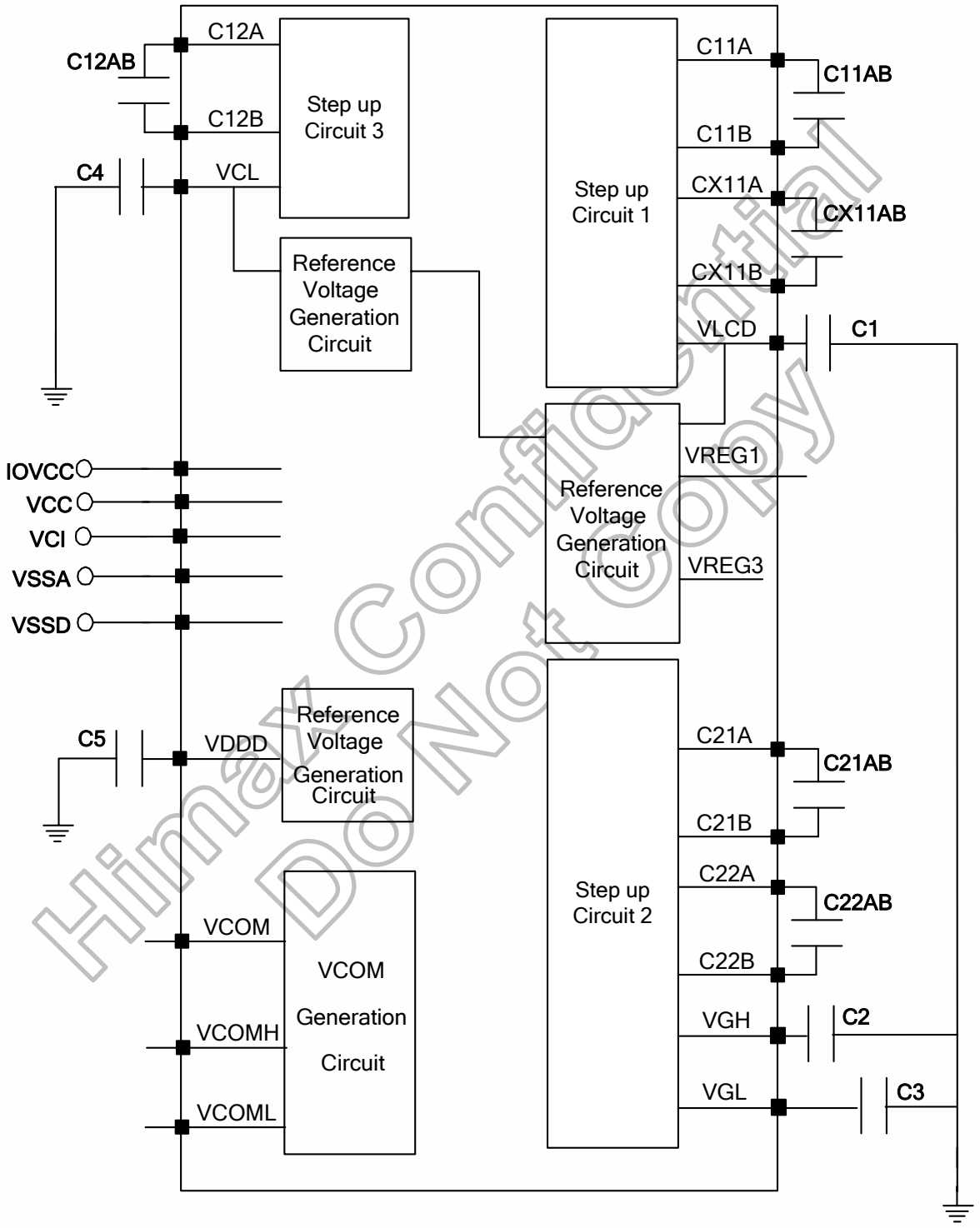

Figure 7.27 Block diagram of HX8352-B01 power circuit

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Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1 (VLCD)	10V	1 μF (B characteristics)
C2 (VGH)	25V	1 μF (B characteristics)
C3 (VGL)	16V	1 μF (B characteristics)
C4 (VCL)	6V	1 μF (B characteristics)
C5(VDDD)	6V	1 μF (B characteristics)
C11AB (C11A/B)	6V	1 μF (B characteristics)
CX11AB (CX11A/B)	6V	1 μF (B characteristics)
C12AB (C12A/B)	6V	1 μF (B characteristics)
C21AB (C21A/B)	10V	1 μF (B characteristics)
C22AB (C22A/B)	10V	1 μF (B characteristics)

Table 7.30 Adoptability of capacitor

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7.8.2 LCD power generation scheme

The boost voltage generated is shown as below.

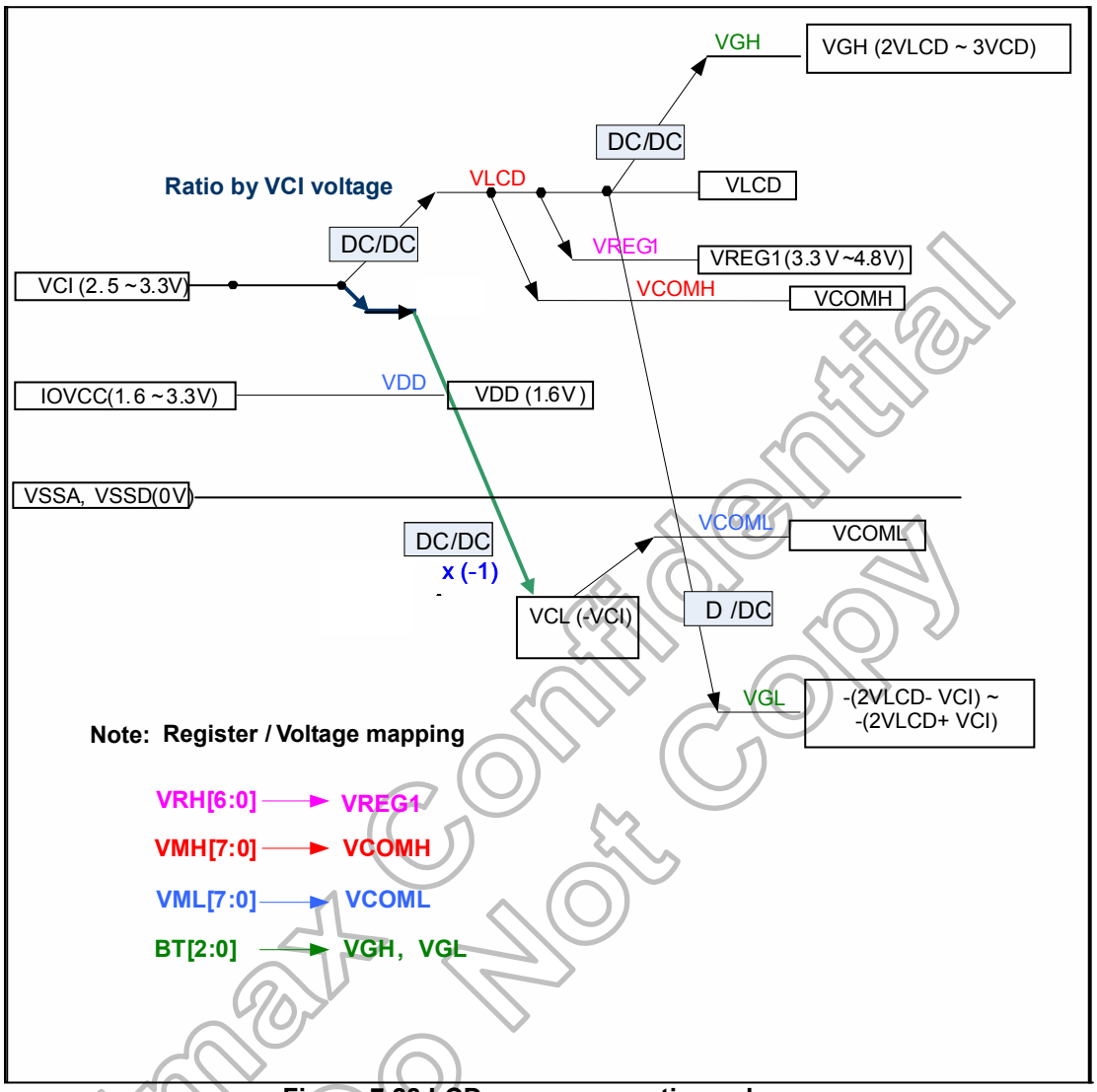

Figure 7.28 LCD power generation scheme

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7.9 Internal power on/off setting sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display on/off set flow

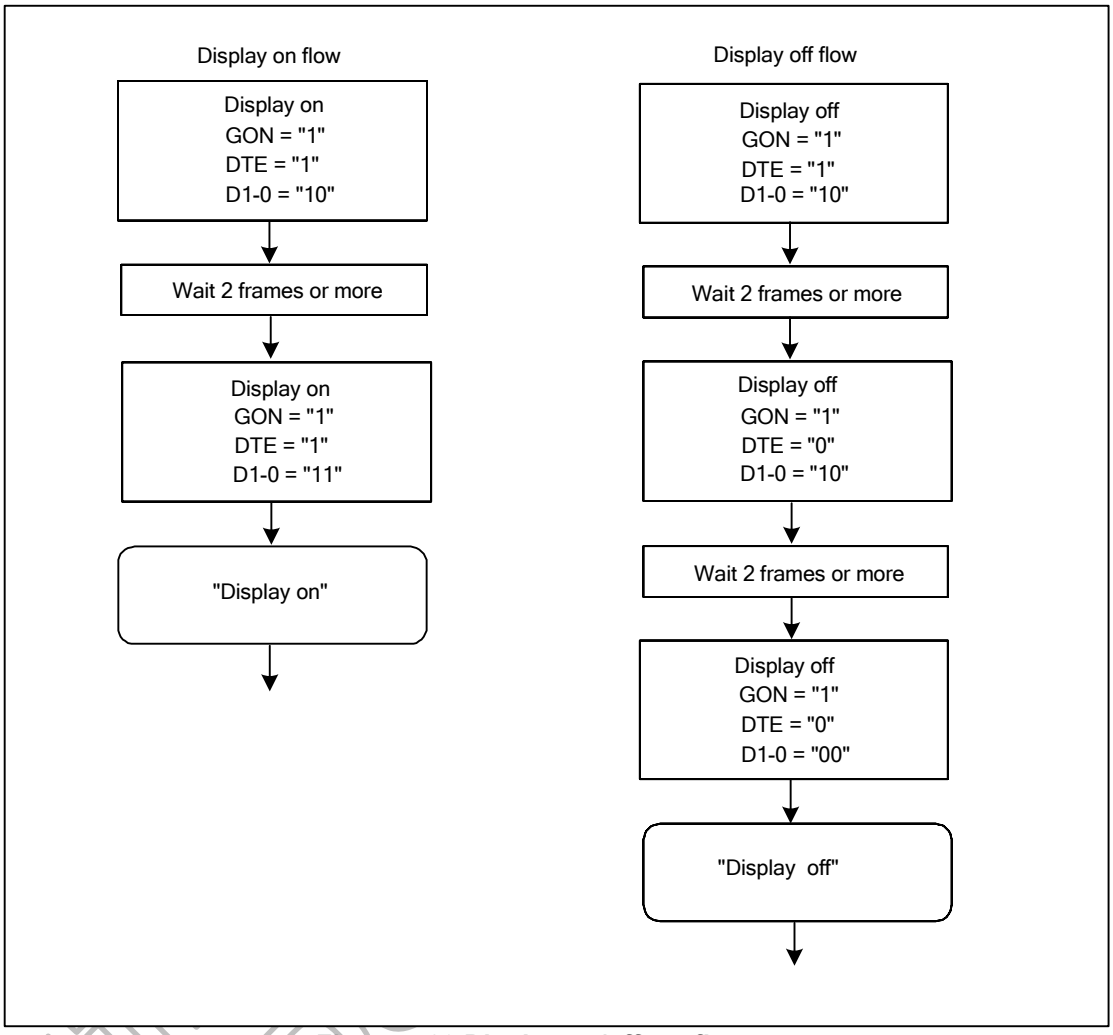

Figure 7.29 Display on/off set flow

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Sleep mode set up flow

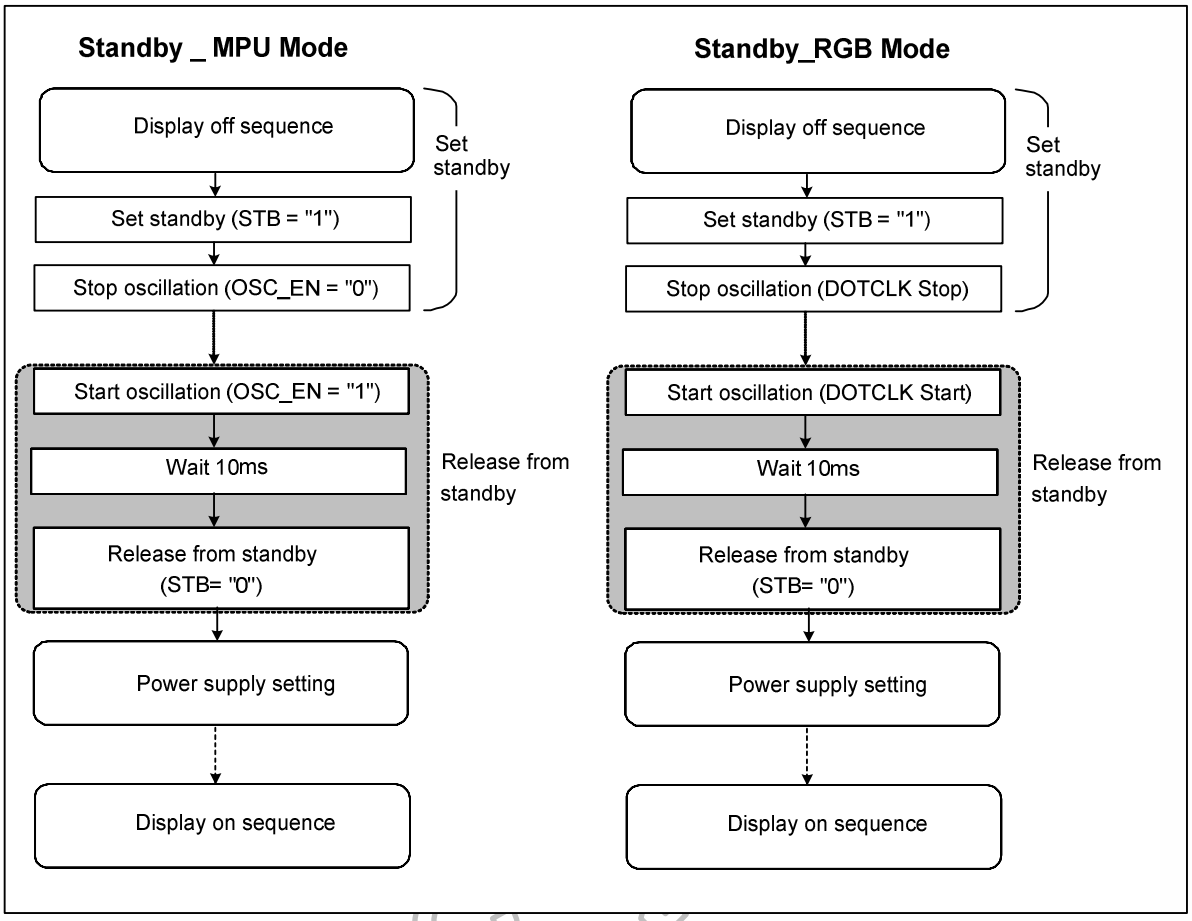

Figure 7.30 Standby mode setting flow

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Power on/off setting up flow

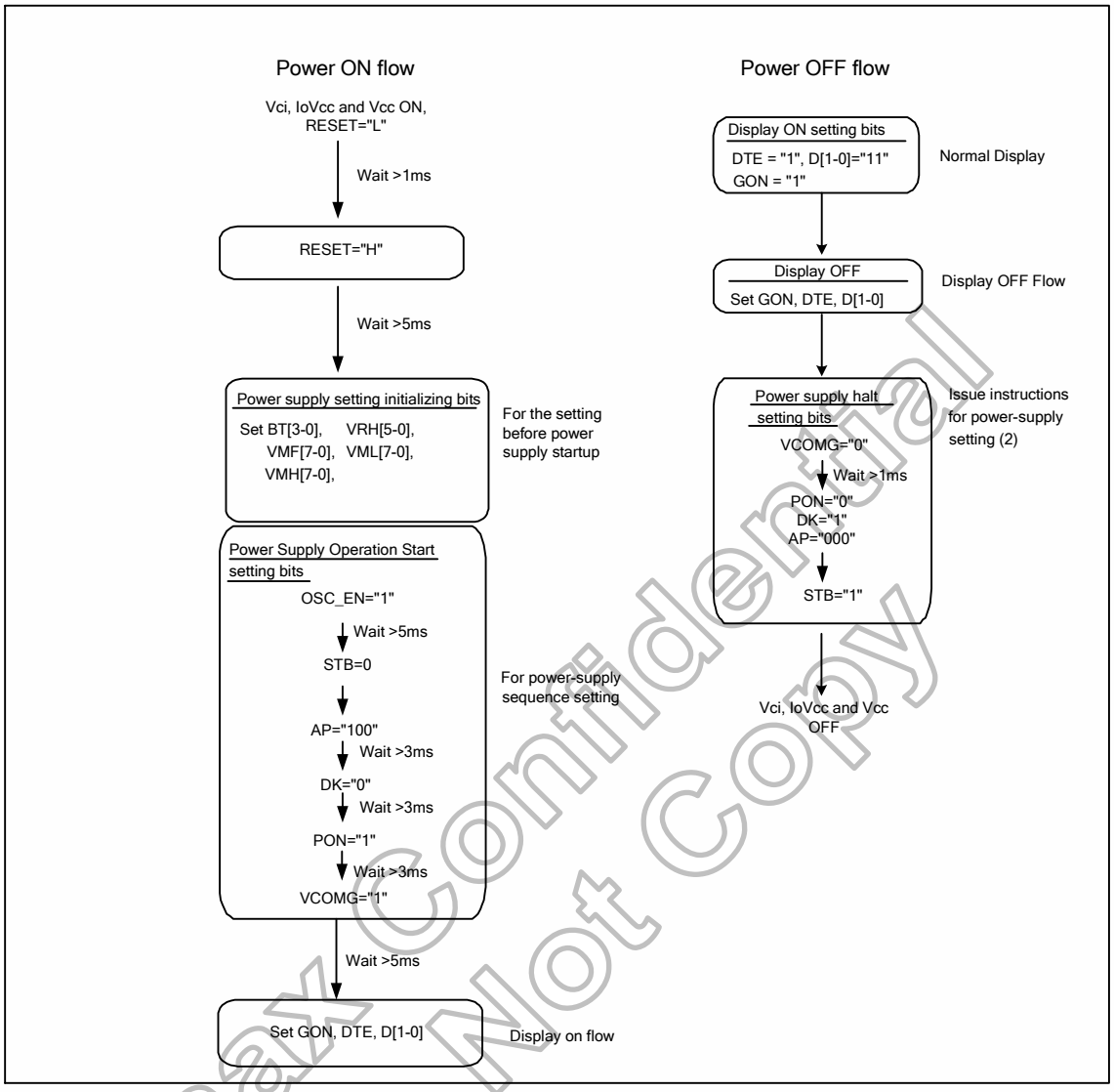

Figure 7.31 Power supply setting flow

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7.10 Input / output pin state

7.10.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
NISD	High	High
PWM_OUT	Low	Low

Table 7.31 Characteristics of output pins

7.10.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
NRESET	Section 11.4.4	Input valid	Input valid	Section 11.34.4
NCS	Input invalid	Input valid	Input valid	Input invalid
NWR_RNW	Input invalid	Input valid	Input valid	Input invalid
NRD_E	Input invalid	Input valid	Input valid	Input invalid
DCX_SCL	Input invalid	Input valid	Input valid	Input invalid
SDI	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DEABLE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
DB[17:0]	Input invalid	Input valid	Input valid	Input invalid
STBP/N	Input Invalid	Input valid	Input valid	Input Invalid
DATAP/N	Input Invalid	Input valid	Input valid	Input Invalid
OSC, BS3,BS2, BS1,BS0, IFSEL0, EXTC	Input invalid	Input valid	Input valid	Input invalid
TEST3-1	Input invalid	Input valid	Input valid	Input invalid
BRUN	Input Invalid	Section 7.7	Section 7.7	Input invaild

Table 7.32 Characteristics of input pins

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8. Command

8.1 Command set

The HX8352-B01 has two pages command set, can setting PAGE_SEL[1:0] to select command set page.

(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
00	Himax ID	R	-	Himax ID (8'bXXXX_XXXX)								-
01	Display Mode control	W/R	-		DP_STBY (0)	-	-	SCROL(0)	IDMON(0)	INVON(0)	PTLON(0)	-
02	Column address start 2	W/R	-	SC[15:8] (8'b0)								-
03	Column address start 1	W/R	-	SC[7:0] (8'b0)								-
04	Column address end 2	W/R	-	EC[15:8] (8'b0)								-
05	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								-
06	Row address start 2	W/R	-	SP[15:8] (8'b0)								-
07	Row address start 1	W/R	-	SP[7:0] (8'b0)								-
08	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								-
09	Row address end 1	W/R	-	EP[7:0] (8'b1010_1111)								-
0A	Partial area start row 2	W/R	-	PSL[15:8] (8'b0)								-
0B	Partial area start row 1	W/R	-	PSL[7:0] (8'b0)								-
0C	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								-
0D	Partial area end row 1	W/R	-	PEL[7:0] (8'b1010_1111)								-
0E	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8](8'b0)								-
0F	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0](8'b0)								-
10	Vertical Scroll height area 2	W/R	-	VSA[15:8](8'b0000_0001)								-
11	Vertical Scroll height area 1	W/R	-	VSA[7:0](8'b1011_0000)								-
12	Vertical Scroll Button area 2	W/R	-	BFA[15:8](8'b0)								-
13	Vertical Scroll Button area 1	W/R	-	BFA[7:0](8'b0)								-
14	Vertical Scroll Start address 2	W/R	-	VSP[15:8](8'b0)								-
15	Vertical Scroll Start address 1	W/R	-	VSP[7:0](8'b0)								-
16	Memory Access control	W/R	-	MY (0)	MX (0)	MV (0)	-	BGR (0)	SM(0)	SS (0)	GS (0)	-
17	COLMOD	W/R	-	CSEL_RGB[2:0](110)				-	CSEL_DBI[2:0](110)			-
18	OSC Control 1	W/R	-	-	I/P RADJ[3:0](1000)			-	N/P RADJ[3:0](1000)			*
19	OSC Control 2	W/R	-	-	-	-	-	-	RNG_EN(0)	OSC_TURBO(0)	OSC_EN (0)	-
1A	Power Control	W/R	-	-	-	-	DCCLK_DISBALE (0)	BT[3:0] (0000)				-
1B	Power Control	W/R	-	-	-	VRH[5:0](01_1000)						-
1C	Power Control	W/R	-	-	-	-	-	-	AP[2:0] (100)			-
1D	Power Control	W/R	-	-	I/PI_FS0[2:0] (010)			-	N/P_FS0[2:0] (010)			-
1E	Power Control	W/R		-	I/PI_FS1[2:0] (001)			-	N/P_FS1[2:0] (001)			-
1F	Power Control 1	W/R	-	GASEN(1)	VCOMG (0)	VPNL_EN(0)	PON (0)	DK (1)	XDK (1)	DDVDH_TRI(0)	STB (1)	-
22	SRAM Control	W/R	SRAM Write/Read									-
23	VCOM Control 1	W/R	-	VMF[7:0] ((8'b1000_0000)								-

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(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
24	VCOM Control 2	W/R	-	VMH[7:0] ((8'b0110_0100)								-
25	VCOM Control 3	W/R	-	VML[7:0] ((8'b0110_0100)								-
26	Display Control 1	W/R	-	I/P_ISC[3:0] (0011)				N/P_ISC[3:0] (0011)				-
27	Display Control 2	W/R	-	PT[1:0] (10)		PTV[1:0](01)		-	(0)	PTG(1)	REF(1)	-
28	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	-
29	Frame Rate control 1	W/R	-	I/PI_RTN[3:0](0000)				N/P_RTN[3:0](0000)				-
2A	Frame Rate Control 2	W/R	-	-	-	I/P_DIV[1:0] (00)		-	-	N/P_DIV[1:0] (00)		-
2B	Frame Rate Control 3	W/R	-	N/P_DUM[7:0](8'b 0001_1110)								-
2h	Frame Rate Control 4	W/R	-	I/PI_DUM[7:0](8'b 0001_1110)								-
2D	Cycle Control 2	W/R	-	GDON[7:0] (8'b0000_0011)								-
2E	Cycle Control 3	W/R	-	GDOF[7:0] (8'b0111_1011)								-
2F	Display inversion	W/R	-	-	I/PI_NW[2:0] (000)			-	N/P_NW[2:0] (001)			-
31	RGB interface control 1	W/R	-	-	-	-	-	-	-	RCM[1:0] (00)		-
32	RGB interface control 2	W/R	-	-	-	-	-	DPL(0)	HSPL(0)	VSPL(0)	EPL(0)	-
33	RGB interface control 3	W/R	-	HBP[7:0] (0000_1000)								-
34	RGB interface control 4	W/R	-	-	VBP[6:0] (00_0010)							-
38	OTP Control 1	W/R	-	OTP_MASK[7:0] (8'b0)								-
39	OTP Control 2	W/R	-	-	OTP_INDEX[6:0] (7'b111_1111)							-
3A	OTP Control 3	W/R	-	OTP_LOAD_DISABLE (0)	OTP_TEST (0)	OTP_POR(0)	OTP_PWE (0)	OTP_PTM[1:0] (00)		VPP_SEL (0)	OTP_PROG (0)	-
3B	OTP Control 4	W/R	-	OTP_DATA[7:0] (8'h00)								-
3C	CABC Control 1	W/R	-	DBV[7:0](8'b0000_0000)								-
3D	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD (0)	BL (0)	-	-	-
3E	CABC Control 3	W/R	-	-	-	-	-	-	-	CABC[1:0] (00)		-
3F	CABC Control 4	W/R	-	CMB[7:0](8'b0000_0000)								-
40	r1 Control (1)	W/R	-	-	-	VRP0[5:0] (6'b00_0000)						-
41	r1 Control (2)	W/R	-	-	-	VRP1[5:0] (6'b00_0000)						-
42	r1 Control (3)	W/R	-	-	-	VRP2[5:0] (6'b00_0000)						-
43	r1 Control (4)	W/R	-	-	-	VRP3[5:0] (6'b00_0000)						-
44	r1 Control (5)	W/R	-	-	-	VRP4[5:0] (6'b00_0000)						-
45	r1 Control (6)	W/R	-	-	-	VRP5[5:0] (6'b00_0000)						-
46	r1 Control (7)	W/R	-	-	PRP0[6:0] (7'b000_0000)							-
47	r1 Control (8)	W/R	-	-	PRP1[6:0] (7'b000_0000)							-
48	r1 Control (9)	W/R	-	-	-	-	PKP0[4:0] (5'b0_0000)					-
49	r1 Control (10)	W/R	-	-	-	-	PKP1[4:0] (5'b0_0000)					-
4A	r1 Control (11)	W/R	-	-	-	-	PKP2[4:0] (5'b0_0000)					-
4B	r1 Control (12)	W/R	-	-	-	-	PKP3[4:0] (5'b0_0000)					-
4C	r1 Control (13)	W/R	-	-	-	-	PKP4[4:0] (5'b0_0000)					-
50	r1 Control (18)	W/R	-	-	-	VRN0[5:0] (6'b00_0000)						-
51	r1 Control (19)	W/R	-	-	-	VRN1[5:0] (6'b00_0000)						-
52	r1 Control (20)	W/R	-	-	-	VRN2[5:0] (6'b00_0000)						-
53	r1 Control (21)	W/R	-	-	-	VRN3[5:0] (6'b00_0000)						-
54	r1 Control (22)	W/R	-	-	-	VRN4[5:0] (6'b00_0000)						-
55	r1 Control (23)	W/R	-	-	-	VRN5[5:0] (6'b00_0000)						-
56	r1 Control (24)	W/R	-	-	PRN0[6:0] (7'b000_0000)							-
57	r1 Control (25)	W/R	-	-	PRN1[6:0] (7'b000_0000)							-
58	r1 Control (26)	W/R	-	-	-	PKN0[4:0] (5'b0_0000)						-
59	r1 Control (27)	W/R	-	-	-	PKN1[4:0] (5'b0_0000)						-
5A	r1 Control (28)	W/R	-	-	-	PKN2[4:0] (5'b0_0000)						-
5B	r1 Control (29)	W/R	-	-	-	PKN3[4:0] (5'b0_0000)						-
5C	r1 Control (30)	W/R	-	-	-	PKN4[4:0] (5'b0_1001)						-
5D	r1 Control (35)	W/R	-	CGMN1[1:0] (2'b00)		CGMN0[1:0] (2'b00)		CGMP1[1:0] (2'b00)		CGMP0[1:0] (2'b00)		-

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(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
60	TE Control	W/R	-	-	-	-	TE_mode (0)	TEON (0)	-	-	-	-
61	ID1	W/R	-	ID1[7:0](8'b0000_0000)								-
62	ID2	W/R	-	ID2[7:0](8'b0000_0000)								-
63	ID3	W/R	-	ID3[7:0](8'b0000_0000)								-
64	ID4	W/R	-	ID4[7:0](8'b0000_0000)								-
68	MDDI Control 4	W/R	-	VWAKE (0)	WKL[8] (0)	-	-	WKF[3:0] (0000)				-
69	MDDI Control 5	W/R	-	WKL[7:0] (8'b0000_0000)								-
6B	GPIO Control 1	W/R	-	GPIO[7:0] (8'b0000_0000)								-
6C	GPIO Control 2	W/R	-	GPIO_CON[7:0] (8'b0000_0000)								-
6D	GPIO Control 3	W/R	-	GPIO_EN[7:0] (8'b0000_0000)								-
6E	GPIO Control 4	W/R	-	GPIO_POL[7:0] (8'b0000_0000)								-
6F	GPIO Control 5	W/R	-	GPIO_CLR[7:0] (8'b0000_0000)								-
70	SUB_PANEL Control 1	W/R	-	SUB_WR[15:8] (8'b0000_0000)								-
71	SUB_PANEL Control 2	W/R	-	SUB_WR[7:0] (8'b0000_0000)								-
72	SUB_PANEL Control 3	W/R	-	SUB_SEL[7:0] (8'b1111_1100)								-
73	SUB_PANEL Control 4	W/R	-	SUB_EN (0)	SUB_RS[1:0] (2'b00)		MPU_MODE (0)	STN_EN (0)	-	SUB_IM[1:0] (2'b00)		-
80	Column address counter 2	W/R	-	-	-	-	-	-	-	-	CAC[8] (0)	-
81	Column address counter 1	W/R	-	CAC[7:0] (8'b0000_0000)								-
82	Row address counter 2	W/R	-	-	-	-	-	-	-	-	RAC[8] (0)	-
83	Row address counter 1	W/R	-	RAC[7:0] (8'b0000_0000)								-
84	TE Output Line2	W/R	-	TSEL15:8] (8'b0)								-
85	TE Output Line2	W/R	-	TSEL[7:0] (8'b0)								-
87	OTP Control 6	W/R	-	OTP_KEY[7:0] (8'b0)								-
E4	Power saving counter 1	W/R	-	EQVCI_M1[7:0] (8'b0000_0000)								-
E5	Power saving counter 2	W/R	-	EQGND_M1[7:0] (8'b0001_1000)								-
E6	Power saving counter 3	W/R	-	EQVCI_M0[7:0] (8'b0000_0000)								-
E7	Power saving counter 4	W/R	-	EQGND_M0[7:0] (8'b0001_1000)								-
FF	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		-

Table 8.1 List table of command set page 0

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(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
00	DGC control	W/R	-	-	-	-	-	-	-	0	DGC_EN (0)	-
01	DGC LUT1	W/R	-	DGC_LUT_R00								-
02	DGC LUT2	W/R	-	DGC_LUT_R01								-
03	DGC LUT3	W/R	-	DGC_LUT_R02								-
04	DGC LUT4	W/R	-	DGC_LUT_R03								-
05	DGC LUT5	W/R	-	DGC_LUT_R04								-
06	DGC LUT6	W/R	-	DGC_LUT_R05								-
07	DGC LUT7	W/R	-	DGC_LUT_R06								-
08	DGC LUT8	W/R	-	DGC_LUT_R07								-
09	DGC LUT9	W/R	-	DGC_LUT_R08								-
0A	DGC LUT10	W/R	-	DGC_LUT_R09								-
0B	DGC LUT11	W/R	-	DGC_LUT_R10								-
0C	DGC LUT12	W/R	-	DGC_LUT_R11								-
0D	DGC LUT13	W/R	-	DGC_LUT_R12								-
0E	DGC LUT14	W/R	-	DGC_LUT_R13								-
0F	DGC LUT15	W/R	-	DGC_LUT_R14								-
10	DGC LUT16	W/R	-	DGC_LUT_R15								-
11	DGC LUT17	W/R	-	DGC_LUT_R16								-
12	DGC LUT18	W/R	-	DGC_LUT_R17								-
13	DGC LUT19	W/R	-	DGC_LUT_R18								-
14	DGC LUT20	W/R	-	DGC_LUT_R19								-
15	DGC LUT21	W/R	-	DGC_LUT_R20								-
16	DGC LUT22	W/R	-	DGC_LUT_R21								-
17	DGC LUT23	W/R	-	DGC_LUT_R22								-
18	DGC LUT24	W/R	-	DGC_LUT_R23								*
19	DGC LUT25	W/R	-	DGC_LUT_R24								-
1A	DGC LUT26	W/R	-	DGC_LUT_R25								-
1B	DGC LUT27	W/R	-	DGC_LUT_R26								-
1C	DGC LUT28	W/R	-	DGC_LUT_R27								-
1D	DGC LUT29	W/R	-	DGC_LUT_R28								-
1E	DGC LUT30	W/R	-	DGC_LUT_R29								-
1F	DGC LUT31	W/R	-	DGC_LUT_R30								-
20	DGC LUT32	W/R	-	DGC_LUT_R31								-
21	DGC LUT33	W/R	-	DGC_LUT_R32								-
22	DGC LUT34	W/R	-	DGC_LUT_R33								-
23	DGC LUT35	W/R	-	DGC_LUT_R34								-
24	DGC LUT36	W/R	-	DGC_LUT_R35								-
25	DGC LUT37	W/R	-	DGC_LUT_R36								-
26	DGC LUT38	W/R	-	DGC_LUT_R37								-
27	DGC LUT39	W/R	-	DGC_LUT_R38								-
28	DGC LUT40	W/R	-	DGC_LUT_R39								-
29	DGC LUT41	W/R	-	DGC_LUT_R40								-
2A	DGC LUT42	W/R	-	DGC_LUT_R41								-
2B	DGC LUT43	W/R	-	DGC_LUT_R42								-
2C	DGC LUT44	W/R	-	DGC_LUT_R43								-
2D	DGC LUT45	W/R	-	DGC_LUT_R44								-
2E	DGC LUT46	W/R	-	DGC_LUT_R45								-
2F	DGC LUT47	W/R	-	DGC_LUT_R46								-
30	DGC LUT48	W/R	-	DGC_LUT_R47								-
31	DGC LUT49	W/R	-	DGC_LUT_R48								-
32	DGC LUT50	W/R	-	DGC_LUT_R49								-
33	DGC LUT51	W/R	-	DGC_LUT_R50								-
34	DGC LUT52	W/R	-	DGC_LUT_R51								-
35	DGC LUT53	W/R	-	DGC_LUT_R52								-
36	DGC LUT54	W/R	-	DGC_LUT_R53								-
37	DGC LUT55	W/R	-	DGC_LUT_R54								-
38	DGC LUT56	W/R	-	DGC_LUT_R55								-
39	DGC LUT57	W/R	-	DGC_LUT_R56								-
3A	DGC LUT58	W/R	-	DGC_LUT_R57								-
3B	DGC LUT59	W/R	-	DGC_LUT_R58								-
3C	DGC LUT60	W/R	-	DGC_LUT_R59								-
3D	DGC LUT61	W/R	-	DGC_LUT_R60								-
3E	DGC LUT62	W/R	-	DGC_LUT_R61								-
3F	DGC LUT63	W/R	-	DGC_LUT_R62								-
40	DGC LUT64	W/R	-	DGC_LUT_R63								-
41	DGC LUT65	W/R	-	DGC_LUT_G00								-

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			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
42	DGC LUT66	W/R	-	DGC_LUT_G01								-
43	DGC LUT67	W/R	-	DGC_LUT_G02								-
44	DGC LUT68	W/R	-	DGC_LUT_G03								-
45	DGC LUT69	W/R	-	DGC_LUT_G04								-
46	DGC LUT70	W/R	-	DGC_LUT_G05								-
47	DGC LUT71	W/R	-	DGC_LUT_G06								-
48	DGC LUT72	W/R	-	DGC_LUT_G07								-
49	DGC LUT73	W/R	-	DGC_LUT_G08								-
4A	DGC LUT74	W/R	-	DGC_LUT_G09								-
4B	DGC LUT75	W/R	-	DGC_LUT_G10								-
4C	DGC LUT76	W/R	-	DGC_LUT_G11								-
4D	DGC LUT77	W/R	-	DGC_LUT_G12								-
4E	DGC LUT78	W/R	-	DGC_LUT_G13								-
4F	DGC LUT79	W/R	-	DGC_LUT_G14								-
50	DGC LUT80	W/R	-	DGC_LUT_G15								-
51	DGC LUT81	W/R	-	DGC_LUT_G16								-
52	DGC LUT82	W/R	-	DGC_LUT_G17								-
53	DGC LUT83	W/R	-	DGC_LUT_G18								-
54	DGC LUT84	W/R	-	DGC_LUT_G19								-
55	DGC LUT85	W/R	-	DGC_LUT_G20								-
56	DGC LUT86	W/R	-	DGC_LUT_G21								-
57	DGC LUT87	W/R	-	DGC_LUT_G22								-
58	DGC LUT88	W/R	-	DGC_LUT_G23								-
59	DGC LUT89	W/R	-	DGC_LUT_G24								-
5A	DGC LUT90	W/R	-	DGC_LUT_G25								-
5B	DGC LUT91	W/R	-	DGC_LUT_G26								-
5C	DGC LUT92	W/R	-	DGC_LUT_G27								-
5D	DGC LUT93	W/R	-	DGC_LUT_G28								-
5E	DGC LUT94	W/R	-	DGC_LUT_G29								-
5F	DGC LUT95	W/R	-	DGC_LUT_G30								-
60	DGC LUT96	W/R	-	DGC_LUT_G31								-
61	DGC LUT97	W/R	-	DGC_LUT_G32								-
62	DGC LUT98	W/R	-	DGC_LUT_G33								-
63	DGC LUT99	W/R	-	DGC_LUT_G34								-
64	DGC LUT100	W/R	-	DGC_LUT_G35								-
65	DGC LUT101	W/R	-	DGC_LUT_G36								-
66	DGC LUT102	W/R	-	DGC_LUT_G37								-
67	DGC LUT103	W/R	-	DGC_LUT_G38								-
68	DGC LUT104	W/R	-	DGC_LUT_G39								-
69	DGC LUT105	W/R	-	DGC_LUT_G40								-
6A	DGC LUT106	W/R	-	DGC_LUT_G41								-
6B	DGC LUT107	W/R	-	DGC_LUT_G42								-
6C	DGC LUT108	W/R	-	DGC_LUT_G43								-
6D	DGC LUT109	W/R	-	DGC_LUT_G44								-
6E	DGC LUT110	W/R	-	DGC_LUT_G45								-
6F	DGC LUT111	W/R	-	DGC_LUT_G46								-
70	DGC LUT112	W/R	-	DGC_LUT_G47								-
71	DGC LUT113	W/R	-	DGC_LUT_G48								-
72	DGC LUT114	W/R	-	DGC_LUT_G49								-
73	DGC LUT115	W/R	-	DGC_LUT_G50								-
74	DGC LUT116	W/R	-	DGC_LUT_G51								-
75	DGC LUT117	W/R	-	DGC_LUT_G52								-
76	DGC LUT118	W/R	-	DGC_LUT_G53								-
77	DGC LUT119	W/R	-	DGC_LUT_G54								-
78	DGC LUT120	W/R	-	DGC_LUT_G55								-
79	DGC LUT121	W/R	-	DGC_LUT_G56								-
7A	DGC LUT122	W/R	-	DGC_LUT_G57								-
7B	DGC LUT123	W/R	-	DGC_LUT_G58								-
7C	DGC LUT124	W/R	-	DGC_LUT_G59								-
7D	DGC LUT125	W/R	-	DGC_LUT_G60								-
7E	DGC LUT126	W/R	-	DGC_LUT_G61								-
7F	DGC LUT127	W/R	-	DGC_LUT_G62								-
80	DGC LUT128	W/R	-	DGC_LUT_G63								-
81	DGC LUT129	W/R	-	DGC_LUT_B00								-
82	DGC LUT130	W/R	-	DGC_LUT_B01								-
83	DGC LUT131	W/R	-	DGC_LUT_B02								-
84	DGC LUT132	W/R	-	DGC_LUT_B03								-
85	DGC LUT133	W/R	-	DGC_LUT_B04								-

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			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
86	DGC LUT134	W/R	-	DGC_LUT_B05								-
87	DGC LUT135	W/R	-	DGC_LUT_B06								-
88	DGC LUT136	W/R	-	DGC_LUT_B07								-
89	DGC LUT137	W/R	-	DGC_LUT_B08								-
8A	DGC LUT138	W/R	-	DGC_LUT_B09								-
8B	DGC LUT139	W/R	-	DGC_LUT_B10								-
8C	DGC LUT140	W/R	-	DGC_LUT_B11								-
8D	DGC LUT141	W/R	-	DGC_LUT_B12								-
8E	DGC LUT142	W/R	-	DGC_LUT_B13								-
8F	DGC LUT143	W/R	-	DGC_LUT_B14								-
90	DGC LUT144	W/R	-	DGC_LUT_B15								-
91	DGC LUT145	W/R	-	DGC_LUT_B16								-
92	DGC LUT146	W/R	-	DGC_LUT_B17								-
93	DGC LUT147	W/R	-	DGC_LUT_B18								-
94	DGC LUT148	W/R	-	DGC_LUT_B19								-
95	DGC LUT149	W/R	-	DGC_LUT_B20								-
96	DGC LUT150	W/R	-	DGC_LUT_B21								-
97	DGC LUT151	W/R	-	DGC_LUT_B22								-
98	DGC LUT152	W/R	-	DGC_LUT_B23								-
99	DGC LUT153	W/R	-	DGC_LUT_B24								-
9A	DGC LUT154	W/R	-	DGC_LUT_B25								-
9B	DGC LUT155	W/R	-	DGC_LUT_B26								-
9C	DGC LUT156	W/R	-	DGC_LUT_B27								-
9D	DGC LUT157	W/R	-	DGC_LUT_B28								-
9E	DGC LUT158	W/R	-	DGC_LUT_B29								-
9F	DGC LUT159	W/R	-	DGC_LUT_B30								-
A0	DGC LUT160	W/R	-	DGC_LUT_B31								-
A1	DGC LUT161	W/R	-	DGC_LUT_B32								-
A2	DGC LUT162	W/R	-	DGC_LUT_B33								-
A3	DGC LUT163	W/R	-	DGC_LUT_B34								-
A4	DGC LUT164	W/R	-	DGC_LUT_B35								-
A5	DGC LUT165	W/R	-	DGC_LUT_B36								-
A6	DGC LUT166	W/R	-	DGC_LUT_B37								-
A7	DGC LUT167	W/R	-	DGC_LUT_B38								-
A8	DGC LUT168	W/R	-	DGC_LUT_B39								-
A9	DGC LUT169	W/R	-	DGC_LUT_B40								-
AA	DGC LUT170	W/R	-	DGC_LUT_B41								-
AB	DGC LUT171	W/R	-	DGC_LUT_B42								-
AC	DGC LUT172	W/R	-	DGC_LUT_B43								-
AD	DGC LUT173	W/R	-	DGC_LUT_B44								-
AE	DGC LUT174	W/R	-	DGC_LUT_B45								-
AF	DGC LUT175	W/R	-	DGC_LUT_B46								-
B0	DGC LUT176	W/R	-	DGC_LUT_B47								-
B1	DGC LUT177	W/R	-	DGC_LUT_B48								-
B2	DGC LUT178	W/R	-	DGC_LUT_B49								-
B3	DGC LUT179	W/R	-	DGC_LUT_B50								-
B4	DGC LUT180	W/R	-	DGC_LUT_B51								-
B5	DGC LUT181	W/R	-	DGC_LUT_B52								-
B6	DGC LUT182	W/R	-	DGC_LUT_B53								-
B7	DGC LUT183	W/R	-	DGC_LUT_B54								-
B8	DGC LUT184	W/R	-	DGC_LUT_B55								-
B9	DGC LUT185	W/R	-	DGC_LUT_B56								-
BA	DGC LUT186	W/R	-	DGC_LUT_B57								-
BB	DGC LUT187	W/R	-	DGC_LUT_B58								-
BC	DGC LUT188	W/R	-	DGC_LUT_B59								-
BD	DGC LUT189	W/R	-	DGC_LUT_B60								-
BE	DGC LUT190	W/R	-	DGC_LUT_B61								-
BF	DGC LUT191	W/R	-	DGC_LUT_B62								-
C0	DGC LUT192	W/R	-	DGC_LUT_B63								-
C3	CABC Control 5	W/R	-	0	PWMDIV[2:0](000)			1	1	INPLUS (1)	1	-
C5	CABC Control 6	W/R	-	PWM_PERIOD[7:0] (8'h2D)								-
C7	CABC Control 7	W/R	-	-	DIM_FRAME[6:0] (20)							-
CB	Gain select register 0	W/R	-	-	DBG0[6:0](40)							-
CC	Gain select register 1	W/R	-	-	DBG1[6:0](3C)							-
CD	Gain select register 2	W/R	-	-	DBG2[6:0](38)							-

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(Hex)	Operation Code	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
CE	Gain select register 3	W/R	-	-	DBG3[6:0](34)							-
CF	Gain select register 4	W/R	-	-	DBG4[6:0](33)							-
D0	Gain select register 5	W/R	-	-	DBG5[6:0](32)							-
D1	Gain select register 6	W/R	-	-	DBG6[6:0](2B)							-
D2	Gain select register 7	W/R	-	-	DBG7[6:0](24)							-
D3	Gain select register 8	W/R	-	-	DBG8[6:0](22)							-
FF	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		-

Table 8.2 List table of command set page 1

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8.2 Index register

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 8.1 Index register

Index register (IR) specifies the Index of register from R00h to RFFh. It sets the register number (ID7-0) in the range from 00000000b to 11111111b in binary form.

8.3 Display mode control register (PAGE0 - R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	1	1	0	0	1	0	1

Figure 8.2 Himax ID register (PAGE0 - R00h)

This command is used to read this IC's ID code. The ID code of this IC is 65h.

8.4 Display mode control register (PAGE0 - R01h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DP_STBY	*	*	SCROL	IDMON	INVON	PLTON
R	1	0	DP_STBY	0	0	SCROL	IDMON	INVON	PLTON

Figure 8.3 Display mode control register (PAGE0 - R01h)

DP_STBY: When DP_STBY = '1', the driver into deep SRAM stand_by mode and, the GRAM data and register content are not retained.
a. Exit the Deep Standby mode (DP_STBY = "0")
b. Start the oscillation
c. Resend GRAM data again before display on.

STB	DP_STB	ModeState
0	0	Normal mode
0	**1**	**Invalid**
1	0	STB Mode
1	1	Deep STB Mode

Note: The relationship between STB and DP_STB

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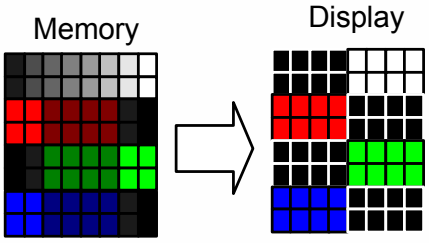
IDMON: This bit is Idle mode (8-color display mode) enable bit. **IDMON** = '1', chip will be into idle mode, and color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

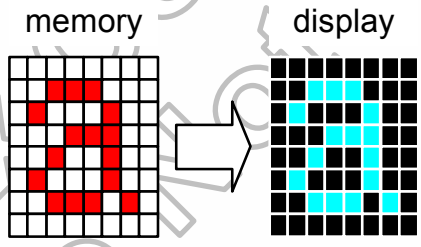
(Idel Mode On Example)



SCROL: This bit turns on scroll mode by setting SCROLL = '1'. The scroll mode window is described by the Vertical Srocll Area command **TFA[15:0], VSA[15:0], BFA[15:0]** and **the Vertical start address VSP[15:0]** (PAGE0 - R0Eh~R15h). To leave scrollmode to normal mode, the **SCROL** bit should be set to '0'.

INVON: This bit is display inversion mode enable bit. **INVON** = '1', chip will be into display inversion mode, and makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

(Example)



PTLON: This command is used for turning on/off Partial mode by setting PTLON=1/0. The Partial mode window is described by the Partial Area command **PSL[15:0], PEL[15:0]** bits(PAGE0 - R0Ah~R0Dh). To leave Partial mode to normal mode, the **PLTON** bit should be set to '0'.
When PTLON=1, display data will come from internal GRAM.

Note: HX8352-B01 do not support SCROL ="1" and PTLON = "1 " together.

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8.5 Column address start register (PAGE0 - R02~03h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 8.4 Column address start register upper byte (PAGE0 - R02h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 8.5 Column address start register low byte (PAGE0 - R03h)

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8.6 Column address end register (PAGE0 - R04~05h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 8.6 Column address end register upper byte (PAGE0 - R04h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 8.7 Column address end register low byte (PAGE0 - R05h)

8.7 Row address start register (PAGE0 - R06~07h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 8.8 Row address start register upper byte (PAGE0 - R06h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 8.9 Row address start register low byte (PAGE0 - R07h)

8.8 Row address end register (PAGE0 - R08~09h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 8.10 Row address end register upper byte (PAGE0 - R08h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 8.11 Row address end register low byte (PAGE0 - R09h)

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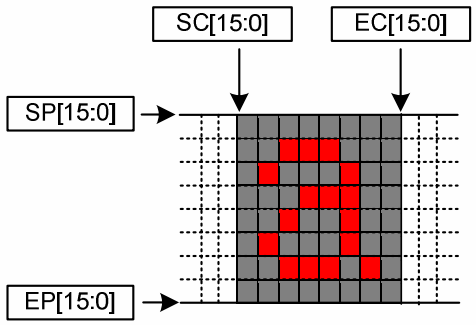
These commands (PAGE0 - R02h~R09h) are used to define area of frame memory where MCU can access. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value of SC[15:0], EC[15:0] represents one column line in the Frame Memory. Each value of SP[15:0], EP[15:0] represents one page line in the Frame Memory.

(Example)



Note: (1) SC[15:0] must always be equal to or less than EC[15:0]
(2) If SC[15:0] or EC[15:0] is greater then the available frame memory then the GRAM write/read will wrong.
(3) SP[15:0] must always be equal to or less than EP[15:0]
(4) If SP[15:0] or EP[15:0] is greater then the available frame memory then the GRAM write/read will worng.

8.9 Partial area start row register (PAGE0 - R0A~0Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 8.12 Partial area start row register upper byte (PAGE0 - R0Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 8.13 Partial area start row register low byte (PAGE0 - R0Bh)

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8.10 Partial area end row register (PAGE0 - R0C~0Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

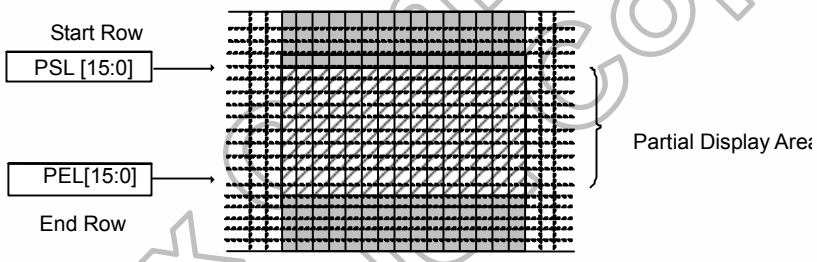
Figure 8.14 Partial area end row register upper byte (PAGE0 - R0Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

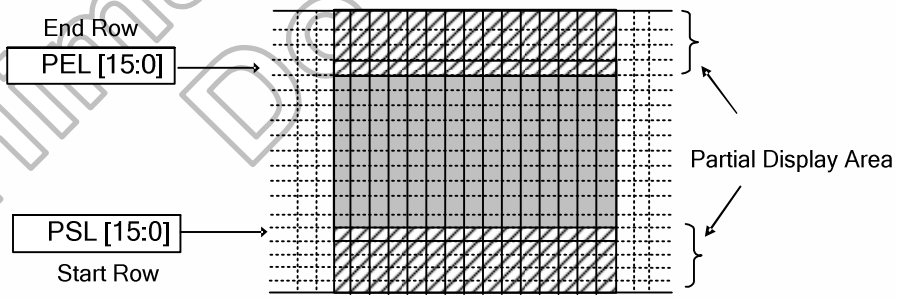
Figure 8.15 Partial area end row register low byte (PAGE0 - R0Dh)

These commands (PAGE0 - R0Ah~~0Dh) define the partial mode's display area. The Start Row (PSL) and the second the End Row (PEL) are illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

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8.11 Vertical scroll top fixed area register (PAGE0 - R0E~0Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 8.16 Vertical scroll top fixed area register upper byte (PAGE0 - R0Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 8.17 Vertical scroll top fixed area register low byte (PAGE0 - R0Fh)

8.12 Vertical scroll height area register (PAGE0 - R10~11h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 8.18 Vertical scroll height area register upper byte (PAGE0 - R10h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 8.19 Vertical scroll height area register low byte (PAGE0 - R11h)

8.13 Vertical scroll button fixed area register (PAGE0 - R12~13h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 8.20 Vertical scroll button fixed area register upper byte (PAGE0 - R12h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 8.21 Vertical scroll button fixed area register low byte (PAGE0 - R13h)

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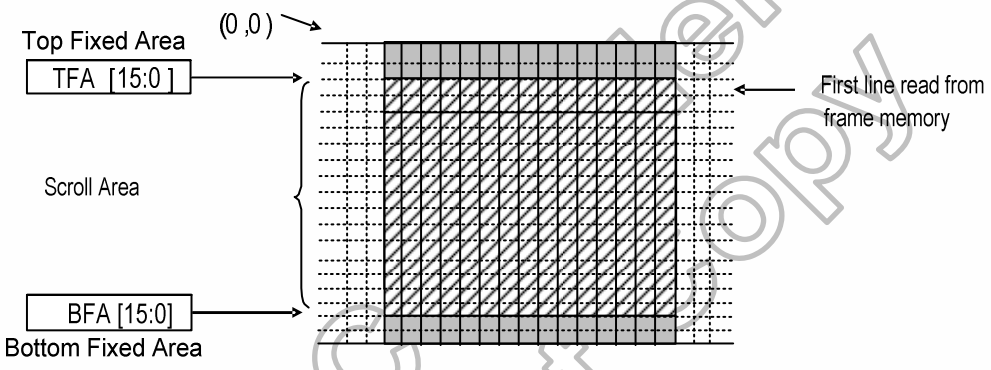
These commands (PAGE0 - R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

TFA[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Please note that (TFA+VSA+BFA) must be set to '432d'(240RGBx432 dot display mode), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, **MV** bit should be set to '0' – this only affects the Frame Memory Write.

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8.14 Vertical scroll start address register (PAGE0 - R14~15h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 8.22 Vertical scroll start address register upper byte (PAGE0 - R14h)

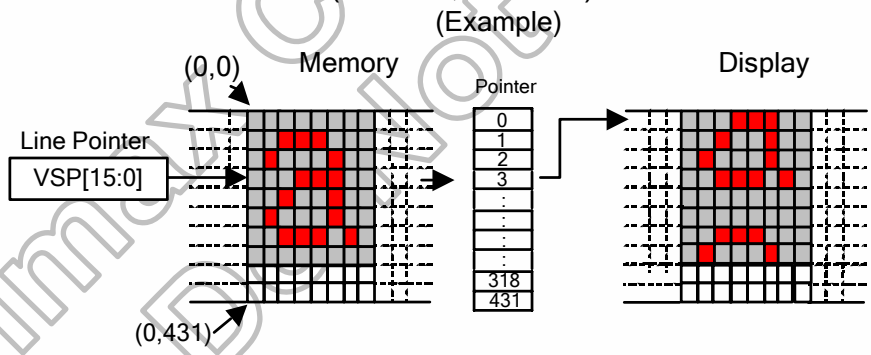
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

Figure 8.23 Vertical scroll start address register low byte (PAGE0 - R15h)

VSP[15:0] is used together with Vertical Scrolling Definition register (PAGE0 - R0Eh~R13h), which describe the scrolling area and the scrolling mode.

VSP[15:0] refers to the Frame Memory line Pointer, and describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '430'd' and VSP = '3d' (**SS** = '0', **GS** = '0')



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

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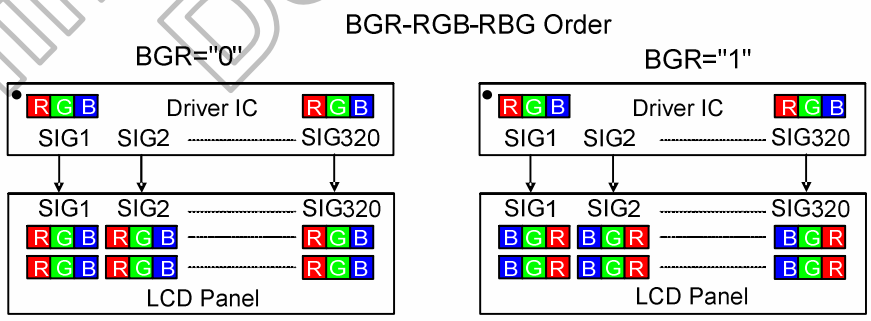
8.15 Memory access control register (PAGE0 - R16h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	MY	MX	MV	*	BGR	SM	SS	GS
R	1	MY	MX	MV	0	BGR	SM	SS	GS

Figure 8.24 Memory access control register (PAGE0 - R16h)

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status. For details, please refer to “6.2.1 System interface to GRAM Write Direction” section.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. “MCU to memory write/read direction”
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) Note : HW pin SRGB=0, BGR color filter SRGB=1, RGB color filter
SS	SOURCE OUTPUT ORDER	The source driver output shift direction selected. When SS = 0, the shift direction don’t reverse(S1 -> S720). When SS = 1, the shift direction will be reversed(S720 -> S1).
GS	GATE OUTPUT ORDER	The gate driver output shift direction selected. When GS = 0, the shift direction don’t reverse(G1 -> G432). When GS = 1, the shift direction will be reversed(G432 -> G1).
SM	GATE SCAN DIRECTION	For detail, please refer section 7.5 scan mode setting.



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8.16 COLMOD control register (PAGE0 - R17h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	CSEL2	CSEL1	CSEL0	*	CESL_ DBI2	CESL_ DBI1	CESL_ DBI0
R	1	0	CSEL2	CSEL1	CSEL0	0	CESL_ DBI2	CESL_ DBI1	CESL_ DBI0

Figure 8.25 COLMOD control register (PAGE0 - R17h)

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface.

Interface Format	CSEL_DBI2	CSEL_DBI1	CSEL_DBI0
Not define	0	0	0
Not define	0	0	1
Not define	0	1	0
12 bit / pixel	0	1	1
18 bit / pixel at 16-bit databus interface (2+16)	1	0	0
16 bit / pixel	1	0	1
18 bit / pixel	1	1	0
18 bit / pixel at 16-bit databus interface (16+2)	1	1	1

Note: Under IFSEL0=1 and (BS="0000" or "0001"), CSEL_DBI [2:0] ="110" is inhibited.

RGB interface

Interface Format	CSEL2	CSEL1	CSEL0
6 bit/pixel	0	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not define	Invalid		

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8.17 OSC control register (PAGE0 - R18h & R19h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_RADJ3	I/P_RADJ2	IP_RADJ1	I/P_RADJ0	N/P_RADJ3	N/P_RADJ2	N/P_RADJ1	N/P_RADJ0
R	1	I/P_RADJ3	I/P_RADJ2	IP_RADJ1	I/P_RADJ0	N/P_RADJ3	N/P_RADJ2	N/P_RADJ1	N/P_RADJ0

Figure 8.26 OSC control 1 register (PAGE0 - R18h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	RNG_EN	OSC_TURBO	OSC_EN
R	1	0	0	0	0	0	RNG_EN	OSC_TURBO	OSC_EN

Figure 8.27 OSC control 2 register (PAGE0 - R19h)

These commands are used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop.

N/P_RADJ[2:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I/PI_RADJ[2:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.
For details, please refer to "7.1 Internal Oscillator" section.

RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency
0	0	0	0	60% x 3.5MHz
0	0	0	1	65% x 3.5MHz
0	0	1	0	70% x 3.5MHz
0	0	1	1	75% x 3.5MHz
0	1	0	0	80% x 3.5MHz
0	1	0	1	85% x 3.5MHz
0	1	1	0	90% x 3.5MHz
0	1	1	1	95% x 3.5MHz
1	0	0	0	100% x 3.5MHz
1	0	0	1	105% x 3.5MHz
1	0	1	0	110% x 3.5MHz
1	0	1	1	115% x 3.5MHz
1	1	0	0	120% x 3.5MHz
1	1	0	1	125% x 3.5MHz
1	1	1	0	130% x 3.5MHz
1	1	1	1	135% x 3.5MHz

Table 8.3 Power control 8 register

OSC_TURBO: Intelnal use, not open
RNG_EN: Intelnal use, not open

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8.18 Power control 1 register (PAGE0 - R1Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	DCCLK_DISABLE	BT3	BT2	BT1	BT0
R	1	*	*	*	DCCLK_DISABLE	BT3	BT2	BT0	BT0

Figure 8.28 Power control 1 register (PAGE0 - R1Ah)

DCCLK_DISABLE: When set DCCLK_DISABLE=1, disable internal pumping Clock. Note: DCCLK_DIASBLE need set as "1" before OTP program value.

BT[3:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT3	BT2	BT1	BT0	VLCD	VCL	VGH	VGL
0	0	0	0	5.3V	-VCI	3VLCD	-VCI-2 VLCD
0	0	0	1	5.3V	-VCI	3VLCD	-2VLCD
0	0	1	0	5.3V	-VCI	3VLCD	VCI-2VLCD
0	0	1	1	5.3V	-VCI	VVCI+2VLCD	-VCI-2VLCD
0	1	0	0	5.3V	-VCI	VCI+2VLCD	-2VLCD
0	1	0	1	5.3V	-VCI	VCI+2VLCD	VCI-2VLCD
0	1	1	0	5.3V	-VCI	2VLCD	-2VLCD
0	1	1	1	5.3V	-VCI	2VLCD	-VCI- VLCD

Note: When VCI = 2.8V

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8.19 Power control 2 register (PAGE0 - R1Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 8.29 Power control 2 register (PAGE0 - R1Bh)

VRH[5:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.VREG1=Decimal(VRH[5:0])x0.05+3.3.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VREG1 (TRI_VDH=0)	VREG1 (TRI_VDH=1)
0	0	0	0	0	0	3.30	3.30
0	0	0	0	0	1	3.35	3.35
0	0	0	0	1	0	3.40	3.40
0	0	0	0	1	1	3.45	3.45
0	0	0	1	0	0	3.50	3.50
0	0	0	1	0	1	3.55	3.55
0	0	0	1	1	0	3.60	3.60
0	0	0	1	1	1	3.65	3.65
0	0	1	0	0	0	3.70	3.70
:	:	:	:	:	:	:	:
0	**1**	**1**	**1**	**1**	**0**	**4.80**	4.80
0	1	1	1	1	1	Inhibited	4.85
1	0	0	0	0	0	:	4.90
1	0	0	0	0	1	:	4.95
1	0	0	0	1	0	:	:
:	:	:	:	:	:	:	:
1	0	1	0	1	0	:	5.40
1	**0**	**1**	**0**	**1**	**1**	:	**5.45**
1	0	1	1	0	0	:	Inhibited
:	:	:	:	:	:	:	:
1	1	1	0	1	1	Inhibited	Inhibited
1	1	1	1	0	1	Inhibited	Inhibited
1	1	1	1	1	0	Inhibited	Inhibited
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.	

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8.20 Power control 3 register (PAGE0 - R1Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	AP2	AP1	AP0

Figure 8.30 Power control 3 register (PAGE0 - R1Ch)

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Medium low
0	1	0	Medium low
0	1	1	Medium low
1	0	0	Medium
1	0	1	Medium high
1	1	0	Large
1	1	1	Setting inhibited

8.21 Power control 4 register (PAGE0 - R1Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_FS02	I/P_FS01	I/P_FS00	*	N/P_FS02	N/P_FS01	N/P_FS00
R	1	*	I/P_FS02	I/P_FS01	I/P_FS00	*	N/P_FS02	N/P_FS01	N/P_FS00

Figure 8.31 Power control 4 register (PAGE0 - R1Dh)

N/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for VLCD voltage generation in Normal / Partial mode.

I/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for VLCD voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

FS02	FS01	FS00	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

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8.22 Power control 5 register (PAGE0 - R1Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_FS12	I/P_FS11	I/P_FS10	*	N/P_FS12	N/P_FS11	N/P_FS10
R	1	*	I/P_FS12	I/P_FS11	I/P_FS10	*	N/P_FS12	N/P_FS11	N/P_FS10

Figure 8.32 Power control 5 register (PAGE0 - R1Eh)

N/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal / Partial mode.

I/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

8.23 Power control 6 register (PAGE0 - R1Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB
R	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB

Figure 8.33 Power control 6 register (PAGE0 - R1Fh)

GASEN: This stands for abnormal power-off supervisal function when the power is off. It’s for monitoring power status by NISD pad when GASEN is set to 1.

VCOMG: When **VCOMG** = ‘1’, VCOML voltage can output to negative voltage (1.0V ~ VCL+0.5V). When VCOMG = ‘0’, VCOML outputs GND and **VML[7:0]** setting are invalid. Then, low power consumption is accomplished.

PON: Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation.
For detail, see the Power On/Off Setting Flow.

PON	Operation of step-up circuit 2
0	OFF
1	ON

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DK: Specify on/off control of step-up circuit 1 for VLCD voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

STB: When **STB** = '1', the HX8352-B01 goes into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

XDK, DDVDH_TRI: Specify the ratio of step-up circuit for VLCD voltage generation.

DDVDH_TRI	XDK	Step up circuit 1	Capacitor connection pins used
0	0	2 x VCI	C11A, C11B
0	1	2 x VCI	C11A, C11B, CX11A, CX11B
1	0	3 x VCI	C11A, C11B, CX11A, CX11B
1	1	Setting inhabited	Setting inhabited

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8.24 Read data register (PAGE0 - R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 8.34 Read data register (PAGE0 - R22h)

WD[17:0] : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

8.25 VCOM control 1~3 register (PAGE0 - R23~25h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0
R	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0

Figure 8.35 Vcom control 1 register (PAGE0 - R23h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0
R	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0

Figure 8.36 Vcom control 2 register (PAGE0 - R24h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0
R	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0

Figure 8.37 Vcom control 3 register (PAGE0 - R25h)

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

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VMH[7:0]: Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5. The default value is 1Ch(28x0.025+2.5=3.2V)

VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	VCOMH (DDVDH_TRI_=0)	VCOMH (DDVDH_TRI=1)
0	0	0	0	0	0	0	0	2.500	2.500
0	0	0	0	0	0	0	1	2.515	2.515
0	0	0	0	0	0	1	0	2.530	2.530
0	0	0	0	0	0	1	1	2.545	2.545
0	0	0	0	0	1	0	0	2.560	2.560
0	0	0	0	0	1	0	1	2.575	2.575
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
1	0	0	1	0	0	1	1	4.705	4.705
1	0	0	1	0	1	0	0	4.720	4.720
1	0	0	1	0	1	0	1	4.735	4.735
1	0	0	1	0	1	1	0	4.750	4.750
1	0	0	1	0	1	1	1	4.765	4.765
1	0	0	1	1	0	0	0	4.780	4.780
1	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**4.795**	4.795
1	0	0	1	1	0	1	0	inhibited	4.810
1	0	0	1	1	0	1	1	:	4.825
1	0	0	1	1	1	0	0	:	4.840
1	0	0	1	1	1	0	1	:	4.855
:	:	:	:	:	:	:	:	:	:
1	**1**	**0**	**0**	**1**	**0**	**0**	**0**	:	**5.500**
:	:	:	:	:	:	:	:	:	inhibited
1	1	1	1	1	1	1	0	inhibited	:
1	1	1	1	1	1	1	1	Setting inhibited	

VML[7:0]: Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5. The default value is 34h(52x0.025-2.5=-1.2V)

VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	0	1	-2.485
0	0	0	0	0	0	1	0	-2.470
0	0	0	0	0	1	0	1	-2.455
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	-0.055
1	0	1	0	0	1	0	0	-0.040
1	0	1	0	0	1	0	1	-0.025
1	0	1	0	0	1	1	0	-0.010
1	0	1	0	0	1	1	1	Setting inhibit
	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Setting inhibit

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VMF[7:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

VMF[7:0]	VCOMH	VCOML
0	"VMH" – 128d	"VML" – 128d
1	"VMH" – 127d	"VML" – 127d
2	"VMH" – 126d	"VML" – 126d
3	"VMH" – 125d	"VML" – 125d
:	:	:
126	"VMH" – 2d	"VML" – 2d
127	"VMH" – 1d	"VML" – 1d
128	"VMH"	"VML"
129	"VMH" + 1d	"VML" + 1d
130	"VMH" + 2d	"VML" + 2d
:	:	:
254	"VMH" + 126d	"VML" + 126d
255	"VMH" + 127d	"VML" + 127d

Note: (1) 0d ≤ (VMH+(VMF-128)) ≤ 153d.(DDVDH_TRI=0)
(2) 0d ≤ (VMH+(VMF-128)) ≤ 200d.(DDVDH_TRI=1)
(3) 0d ≤ (VML+(VMF-128)) ≤ 166d.

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8.26 Display control 1~3 register (PAGE0 - R26h~R28h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_ISC3	I/P_ISC2	I/P_ISC1	I/P_ISC0	N/P_ISC3	N/P_ISC2	N/P_ISC1	N/P_ISC0
R	1	I/P_ISC3	I/P_ISC2	I/P_ISC1	I/P_ISC0	N/P_ISC3	N/P_ISC2	N/P_ISC1	N/P_ISC0

Figure 8.38 Display control 1 register (PAGE0 - R26h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PT1	PT0	PTV1	PTV0	*	0	PTG	REF
R	1	PT1	PT0	PTV1	PTV0	*	0	PTG	REF

Figure 8.39 Display control 2 register (PAGE0 - R27h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	GON	DTE	D1	D0	*	*
R	1	*	*	GON	DTE	D1	D0	0	0

Figure 8.40 Display control 3 register (PAGE0 - R28h)

N/P_ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area for Nornal/ Partial mode. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

I/P_ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area for Idle (8-color) / Partial Idle mode. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	183ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	250ms
1	0	0	0	17 frames	283ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	350ms
1	0	1	1	23 frames	383ms
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

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REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

PT[1:0] : Specify the Non-display area source output in partial display mode.

INVON	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
1	18'h00000 . . 18'h3FFFF	V63P . . V0P	V0N . . V63N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z
0	18'h00000 . . 18'h3FFFF	V0P . . V63P	V63N . . V0N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z

D[1:0]: When D1='1', display is on; when D1='0', display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = '1'. When D1='0', the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8352-B01 can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE.
When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	HX8352-B01 Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	Inhibit	Inhibit	Inhibit
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

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GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	-	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving
1	0	0	-	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving
1	1	0	-	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving

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8.27 Frame control 1~4 register (PAGE0 - R29h~R2Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN2	N/P_RTN1	N/P_RTN0
R	1	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN_2	N/P_RTN1	N/P_RTN0

Figure 8.41 Frame control 1 register (PAGE0 - R29h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0
R	1	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0

Figure 8.42 Frame control 2 register (PAGE0 - R2Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0
R	1	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0

Figure 8.43 Frame control 3 register (PAGE0 - R2Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_DUM7	I/P_DUM6	I/P_DUM5	I/P_DUM4	I/P_DUM3	I/P_DUM2	I/P_DUM1	I/P_DUM0
R	1	I/P_DUM7	I/P_DUM6	I/P_DUM5	I/P_DUM4	I/P_DUM3	I/P_DUM2	I/P_DUM1	I/P_DUM0

Figure 8.44 Frame control 4 register (PAGE0 - R2Ch)

N/P_DIV[1:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **N/P_RTN[3:0]** bits (1H period clock cycle), **N/P_DIV[1:0]**, and **N/P_DUM[7:0]** bits.

I/P_DIV[1:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **I/P_RTN[3:0]** bits(1H period clock cycle), **I/P_DIV[1:0]**, and **I/P_DUM[7:0]** bits.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

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N/P_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation.

I/P_ RTN[3:0]: Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[3:0]	Clock number per Line
4'b0000	127
4'b0001	135
4'b0010	143
4'b0011	151
4'b0100	159
:	:
4'b1110	239
4'b1111	247

N/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.

I/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	1
003d	2
004d	3
:	:
254d	253
255d	254

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (scan Line+DUM)) [Hz]
fosc: RC oscillation frequency

RSO[1:0]	Scan Line
11	Inhibited
10	432
01	400
00	320

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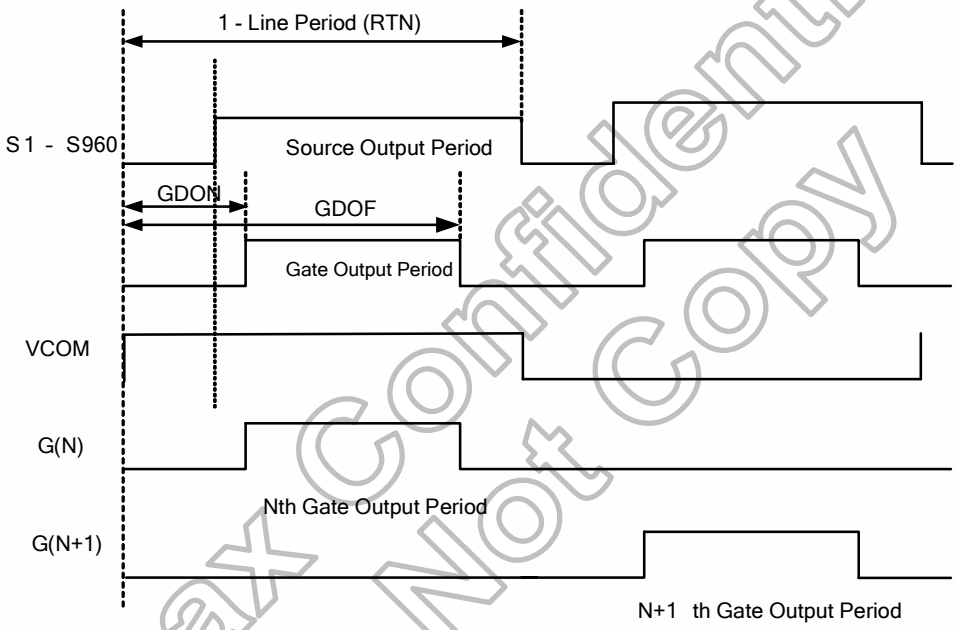
8.28 Cycle control 1~2 register (PAGE0 - R2Dh~R2Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0
R	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0

Figure 8.45 Cycle control 1 register (PAGE0 - R2Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0
R	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0

Figure 8.46 Cycle control 2 register (PAGE0 - R2Eh)



GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited).

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).

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8.29 Display inversion register (PAGE0 - R2Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_ NW2	I/P_ NW1	I/P_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0
R	1	*	I/P_ NW2	I/P_ NW1	I/P_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0

Figure 8.47 Display inversion control register (PAGE0 - R2Fh)

N/P_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I/P_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD driving Inversion type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

8.30 RGB interface control 1~4 register (PAGE0 - R31h~R34h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	RCM 1	RCM 0
R	1	0	0	0	0	0	0	RCM 1	RCM 0

Figure 8.48 RGB interface control 1 register (PAGE0 - R31h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	0	0	DPL	HSPL	VSPL	EPL
R	1	0	0	0	0	DPL	HSPL	VSPL	EPL

Figure 8.49 RGB interface control 2 register (PAGE0 - R32h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 8.50 RGB interface control 3 register (PAGE0 - R33h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R	1	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 8.51 RGB interface control 4 register (PAGE0 - R34h)

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This command is used to set RGB interface related register

RCM[1:0]: Selcet system interface or RGB interface.

RCM[1:0]	Interface Select
0X	System interface
10	RGB Interface(1) (VS+HS+DE)
11	RGB Interface(2) (VS+HS)

EPL: Specify the polarity of ENABLE signal in RGB interface mode. EPL='1', the ENABLE signal is Low active; EPL=0, the ENABLE signal is High active.

VSPL: The polarity of VSYNC pin. When VSPL='0', the VSYNC signal is Low active. When VSPL=1, the VSYNC signal is High active.

HSPL: The polarity of HSYNC pin. When HSPL='0', the HSYNC signal is Low active. When HSPL=1, the HSYNC signal is High active.

DPL: The polarity of PCLK pin. When DPL='0', the data is latched by the chip on the rising edge of PCLK signal. When DPL='1', the data is latched by the chip on the falling edge of PCLK signal.

HBP and **VBP** are used to set vertical and horizontal back porch control in RGB I/F mode 2 (RCM[1:0] = "11")

HBP[7:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2. (RCM[1:0]="11")

HBP[7:0]	No. of clock cycle of DOTCLK
	CSEL="101" or "110" or "000"
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
52d	52
53d	53
Other setting	Setting Inhibited

VBP[6:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2

VBP[6:0]	No. of clock cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
61d	61
62d	62
63d	63

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8.31 OTP contril 1~4 register (PAGE0 - R38h ~ R3Bh)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0
R	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0

Figure 8.52 OTP control 1 register (PAGE0 - R38h)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0
R	1	0	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0

Figure 8.53 OTP control 2 register (PAGE0 - R39h)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG
R	1	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG

Figure 8.54 OTP control 3 register (PAGE0 - R3Ah)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
R	1	OTP_DATA7	OTP_DATA6	OTP_DATA5	OTP_DATA4	OTP_DATA3	OTP_DATA2	OTP_DATA1	OTP_DATA0

Figure 8.55 OTP control 4 register (PAGE0 - R3Bh)

This command is used to set the OTP related setting. Please see OTP flow for detail use.

OTP_MASK[7:0]: Bit programming mask, if 1, means don't programming this bit

OTP_INDEX[6:0]: Set location of OTP to be programmed

OTP_LOAD_DISABLE: When written to 1, auto load from OTP to internal register is disabled, this is used when OTP is not yet programmed

OTP_TEST: Internal use, not open. Please set "0"

OTP_POR: OTP read control bit.

OTP_PWE: Internal use, not open. Please set "0".

OTP_PTM[1:0]: Internal use, not open. Please set "00".

OTP_PROG: When Set OPT_PROG=1, internal register begin written to OTP.

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VPP_SEL: When written to 1, VPP voltage is fed to OTP.

OTP_DATA[7:0]: OTP data of read OTP index.

For details, please refer to Chapter 10. OTP Programming.

8.32 CABC control 1~4 register (PAGE0 - R3Ch~3Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0
R	1	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0

Figure 8.56 CABC control 1 register (PAGE0 - R3Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	BCTRL	*	DD	BL	*	*
R	1	0	0	BCTRL	0	DD	BL	0	0

Figure 8.57 CABC control 2 register (PAGE0 - R3Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	CABC 1	CABC 0
R	1	0	0	0	0	0	0	CABC 1	CABC 0

Figure 8.58 CABC control 3 register (PAGE0 - R3Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0
R	1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0

Figure 8.59 CABC control 4 register (PAGE0 - R3Fh)

These commands are used to set CABC parameter.

DBV[7:0]: Control the backlight PWM pulse output duty.
(PWM_period = DBV[7:0])/255 x CABC_duty).

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BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.

'0' = Off (Equal to DBV[7:0] = '00h')
'1' = On (Brightness registers are active.)

DD: Display Dimming (Only for manual brightness setting)

'0': Display Dimming is off.
'1': Display Dimming is on.

BL: Backlight Control On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)
'1' = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

CABC[1:0]: This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC1	CABC0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

CMB[7:0]: This command is used to set the minimum brightness value of the display for CABC function.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

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8.33 Gamma control 1~35 register (PAGE0 - R40h~5Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 05	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00
R	1	0	0	VRP 05	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00

Figure 8.60 Gamma control 1 register (PAGE0 - R40h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 15	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10
R	1	0	0	VRP 15	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10

Figure 8.61 Gamma control 2 register (PAGE0 - R41h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 25	VRP 24	VRP 23	VRP 22	VRP 21	VRP 20
R	1	0	0	VRP 25	VRP 24	VRP 23	VRP 22	VRP 21	VRP 20

Figure 8.62 Gamma control 3 register (PAGE0 - R42h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 35	VRP 34	VRP 33	VRP 32	VRP 31	VRP 30
R	1	0	0	VRP 35	VRP 34	VRP 33	VRP 32	VRP 31	VRP 30

Figure 8.63 Gamma control 4 register (PAGE0 - R43h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 45	VRP 44	VRP 43	VRP 42	VRP 41	VRP 40
R	1	0	0	VRP 45	VRP 44	VRP 43	VRP 42	VRP 41	VRP 40

Figure 8.64 Gamma control 5 register (PAGE0 - R44h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 55	VRP 54	VRP 53	VRP 52	VRP 51	VRP 50
R	1	0	0	VRP 55	VRP 54	VRP 53	VRP 52	VRP 51	VRP 50

Figure 8.65 Gamma control 6 register (PAGE0 - R45h)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00
R	1	0	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00

Figure 8.66 Gamma control 7 register (PAGE0 - R46h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10
R	1	0	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10

Figure 8.67 Gamma control 8 register (PAGE0 - R47h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00
R	1	0	0	0	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00

Figure 8.68 Gamma control 9 register (PAGE0 - R48h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10
R	1	0	0	0	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10

Figure 8.69 Gamma control 10 register (PAGE0 - R49h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20
R	1	0	0	0	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20

Figure 8.70 Gamma control 11 register (PAGE0 - R4Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30
R	1	0	0	0	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30

Figure 8.71 Gamma control 12 register (PAGE0 - R4Bh)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40
R	1	0	0	0	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40

Figure 8.72 Gamma control 13 register (PAGE0 - R4Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00
R	1	0	0	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

Figure 8.73 Gamma control 17 register (PAGE0 - R50h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10
R	1	0	0	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10

Figure 8.74 Gamma control 18 register (PAGE0 - R51h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20
R	1	0	0	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20

Figure 8.75 Gamma control 19 register (PAGE0 - R52h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30
R	1	0	0	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30

Figure 8.76 Gamma control 20 register (PAGE0 - R53h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40
R	1	0	0	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40

Figure 8.77 Gamma control 21 register (PAGE0 - R54h)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50
R	1	0	0	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50

Figure 8.78 Gamma control 22 register (PAGE0 - R55h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00
R	1	0	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00

Figure 8.79 Gamma control 23 register (PAGE0 - R56h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10
R	1	0	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10

Figure 8.80 Gamma control 24 register (PAGE0 - R57h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00
R	1	0	0	0	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00

Figure 8.81 Gamma control 25 register (PAGE0 - R58h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10
R	1	0	0	0	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10

Figure 8.82 Gamma control 26 register (PAGE0 - R59h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20
R	1	0	0	0	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20

Figure 8.83 Gamma control 27 register (PAGE0 - R5Ah)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30
R	1	0	0	0	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30

Figure 8.84 Gamma control 28 register (PAGE0 - R5Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40
R	1	0	0	0	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40

Figure 8.85 Gamma control 29 register (PAGE0 - R5Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00
R	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00

Figure 8.86 Gamma control 30 register (PAGE0 - R5Dh)

VRP5-0[5:0]: Gamma Offset adjustment registers for positive polarity output
VRN5-0[5:0]: Gamma Offset adjustment registers for negative polarity output
PRP1-0[6:0]: Gamma Center adjustment registers for positive polarity output
PRN1-0[6:0]: Gamma Center adjustment registers for negative polarity output
PKP8-0[4:0]: Gamma Macro adjustment registers for positive polarity output
PKN8-0[4:0]: Gamma Macro adjustment registers for negative polarity output
For details, please refer to Section 7.2 Gamma resister stream and 8 to 1 Selector.

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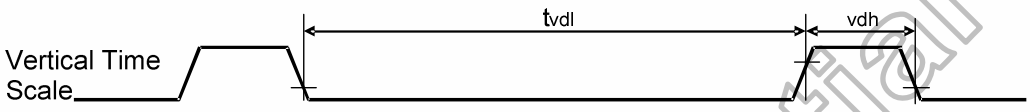
8.34 TE mode control (PAGE0 - R60h)

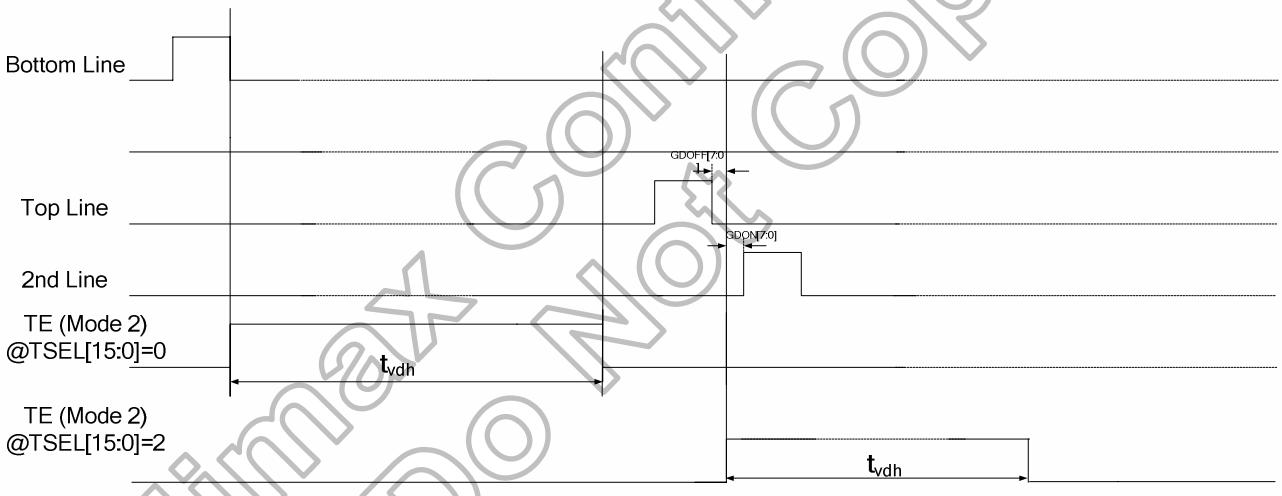
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	TEMODE	TEON	*	*	*
R	1	0	0	0	TEMODE	TEON	0	0	0

Figure 8.87 Mode control register (PAGE0 - R60h)

TEMODE: Specify the Tearing-Effect mode.
When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of V-Blanking information only.



When **TEMODE** ='0': The Tearing Effect Output Line (TE) will output defined by TSEL[15:0] setting.
Example:
(1) TSEL[15:0]=0, then TE signal will output after last Line finished.
(2) TSEL[15:0]=2, then TE signal will output after second Line finished.



Note: During Stand by Mode with Tearing Effect Line On, Tearing Effect Output pin is active low.

TEON: This command is used to turn ON the Tearing Effect output signal from the TE signal line.

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8.35 ID1~4 register (PAGE0 - R61h~64h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 8.88 ID1 register (PAGE0 - R61h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 8.89 ID3 register (PAGE0 - R62h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 8.90 ID3 register (PAGE0 - R63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
R	1	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

Figure 8.91 ID4 register (PAGE0 - R64h)

ID1~4: User can program any value to OTP for module number.

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8.36 MDDI control 4~5 register (PAGE0 - R68h~R69h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VWAKW	WKL8	*	*	WKF3	WKF2	WKF1	WKF0
R	1	VWAKE	WKL8	0	0	WKF3	WKF2	WKF1	WKF0

Figure 8.92 MDDI control 4 register (PAGE0 - R68h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0
R	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0

Figure 8.93 MDDI control 5 register (PAGE0 - R69h)

Set a display position at which to start a wakeup request from the client to the host.

WKF[3:0]: When MDDI applies a client start wakeup, frame WKF[3:0] + 1 is used to release a wakeup request. The range you can set is from the first frame to the 16th frame. (Initial value: "0000")

VWAKE: Setting this bit to “1” will enable a client start wakeup. When the host accepts a wakeup request to clear hibernation, this bit is set automatically to “0.” (Initial value: 0)

WKL[8:0]: When MDDI applies a client start wakeup, a wakeup request is released from line WKL[8:0] + 1 of a frame set by WKF[3:0]. The range you can set is from the first line to the 512th line. (Initial value: "0 0000 0000")

When you set WKL to “0 0000 0001” with WKF set to “0010,” a wakeup request will be started at the second line of the third frame.

8.37 GPIO control 1~5 register (PAGE0 - R6Bh~R6Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R	1	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Figure 8.94 GPIO control 1 register (PAGE0 - R6Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0
R	1	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0

Figure 8.95 GPIO control 2 register (PAGE0 - R6Ch)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
R	1	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0

Figure 8.96 GPIO control 3 register (PAGE0 - R6Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_POL7	GPIO_POL6	GPIO_POL5	GPIO_POL4	GPIO_POL3	GPIO_POL2	GPIO_POL1	GPIO_POL0
R	1	GPIO_POL7	GPIO_POL6	GPIO_POL5	GPIO_POL4	GPIO_POL3	GPIO_POL2	GPIO_POL1	GPIO_POL0

Figure 8.97 GPIO control 4 register (PAGE0 – R6Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_CLR7	GPIO_CLR6	GPIO_CLR5	GPIO_CLR4	GPIO_CLR3	GPIO_CLR2	GPIO_CLR1	GPIO_CLR0
R	1	GPIO_CLR7	GPIO_CLR6	GPIO_CLR5	GPIO_CLR4	GPIO_CLR3	GPIO_CLR2	GPIO_CLR1	GPIO_CLR0

Figure 8.98 GPIO control 5 register (PAGE0 – R6Fh)

GPIO[7:0]: GPIO value. When GPIO is input mode, GPIO value is set to the register.

GPIO_CON[7:0]: Select GPIO I/O mode.

GPIO_CONx	GPIOx pin
0	INPUT
1	OUTPUT

Note: x:7~0

GPIO_EN[7:0]: When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.

GPPOL[7:0]: Interrupt polarity select bit
1: rising edge
0: falling edge

GPIO_CLR[7:0]: Write ’0’, clear interrupt. After Wakeup, this bit is cleared.

For more information about these registers, refer to GPIO CONTROL section

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8.38 SUB_PANEL control 1~4 register (PAGE0 - R70h~R73h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_WR15	SUB_WR14	SUB_WR13	SUB_WR12	SUB_WR11	SUB_WR10	SUB_WR9	SUB_WR8
R	1	SUB_WR15	SUB_WR14	SUB_WR13	SUB_WR12	SUB_WR11	SUB_WR10	SUB_WR9	SUB_WR8

Figure 8.99 SUB_PANEL control 1 register (PAGE0 - R70h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_WR7	SUB_WR6	SUB_WR5	SUB_WR4	SUB_WR3	SUB_WR2	SUB_WR1	SUB_WR0
R	1	SUB_WR7	SUB_WR6	SUB_WR5	SUB_WR4	SUB_WR3	SUB_WR2	SUB_WR1	SUB_WR0

Figure 8.100 SUB_PANEL control 2 register (PAGE0 - R71h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_SEL7	SUB_SEL6	SUB_SEL5	SUB_SEL4	SUB_SEL3	SUB_SEL2	SUB_SEL1	SUB_SEL0
R	1	SUB_SEL7	SUB_SEL6	SUB_SEL5	SUB_SEL4	SUB_SEL3	SUB_SEL2	SUB_SEL1	SUB_SEL0

Figure 8.101 SUB_PANEL control 3 register (PAGE0 - R72h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_EN	SUB_RS1	SUB_RS0	MPU_MODE	STN_EN	*	SUB_IM1	SUB_IM0
R	1	SUB_EN	SUB_RS1	SUB_RS0	MPU_MODE	STN_EN	0	SUB_IM1	SUB_IM0

Figure 8.102 SUB_PANEL control 4 register (PAGE0 - R73h)

SUB_WR[15:0]: SUB_WR is the index of sub panel data write. Initial value of SUB_WR is '202h'. When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 202h), index for GRAM access is automatically transferred before GRAM data transfer. When sub panel driver IC uses other address, 202h address have to be changed. Then user can change SUB_WR value from 202h to other value.

SUB_SEL: SUB_SEL is the index of main/sub panel selection. If SUB_SEL is '01h', then main panel is selected, and if that is "00h", then sub panel is selected. Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_EN: Enables the sub panel interface.

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SUBRS [1:0]: Specifies operation of RS2 terminal when receiving the video stream packet for STN type sub panel control. These register bits are enabled when STN = 1.

SUB_RS1	SUB_RS0	Operation
0	0	Hold (no change)
0	1	High level output
1	0	Low level output
1	1	reserved

MPU_MODE: Selects MPU type for sub panel
If MPU_MODE = 0, then i80-type parallel interface mode is selected.
If MPU_MODE = 1, then M68-type parallel interface mode is selected.

STN_EN: Selects panel type for sub panel.
If STN = 0, then TFT-type sub panel interface is selected.
If STN = 1, then STN-type sub panel interface is selected.

SIM [1:0] : Selects interface mode for sub panel.

SIM1	SIM0	Interface Mode
0	0	18-bit Parallel (1-time transfer)
0	1	9-bit Parallel (2-time transfer)
1	0	16-bit Parallel (1-time transfer)
1	1	8-bit Parallel (2-time transfer)

Note: The HX8352-B01 does not support read operation from sub panel Interface.

8.39 Column address counter 2~1 register (PAGE0 - R80h~R81h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	CAC8
R	1	0	0	0	0	0	0	0	CAC8

Figure 8.103 Column address counter 2 register (PAGE0 - R80h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CAC7	CAC6	CAC5	CAC4	CAC3	CAC2	CAC1	CAC0
R	1	CAC7	CAC6	CAC5	CAC4	CAC3	CAC2	CAC1	CAC0

Figure 8.104 Column address counter 1 register (PAGE0 - R81h)

CAC[8:0]: Set GRAM Column addresses to the address counter (AC) before access to the GRAM. Once the GRAM data is written, the AC is automatically updated according to the MX, MY and MV bits. CAC[8:0] must always be equal to or less than EC[8:0].

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8.40 Row address counter 2~1 register (PAGE0 - R82h~R83h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	RAC8
R	1	0	0	0	0	0	0	0	RAC8

Figure 8.105 Row address counter 2 register (PAGE0 - R82h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
R	1	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0

Figure 8.106 Row address counter 1 register (PAGE0 - R83h)

RAC[8:0]: Set GRAM Row addresses to the address counter (AC) before access to the GRAM. Once the GRAM data is written, the AC is automatically updated according to the MX, MY and MV bits. RAC[8:0] must always be equal to or less than EP[8:0].

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8.41 Set TE output delay line resgiter2~1 (R84~R85h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL 15	TSEL 14	TSEL 13	TSEL 12	TSEL 11	TSEL 10	TSEL 9	TSEL 8
R	1	TSEL 15	TSEL 14	TSEL 13	TSEL 12	TSEL 11	TSEL 10	TSEL 9	TSEL 8

Figure 8.107 Row address counter 2 register (PAGE0 - R84h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL 7	TSEL 6	TSEL 5	TSEL 4	TSEL 3	TSEL 2	TSEL 1	TSEL 0
R	1	TSEL 7	TSEL 6	TSEL 5	TSEL 4	TSEL 3	TSEL 2	TSEL 1	TSEL 0

Figure 8.108 Row address counter 1 register (PAGE0 - R85h)

TSEL[15:0] setting can be used when TEMODE="1" only, otherwise TESL[15:0] setting is invalid.

TSEL[15:0]	Resoultion = 240x320 TE output start Line	Resoultion = 240x400 TE output start Line	Resoultion = 240x432 TE output start Line
0'd	Blanking Area	Blanking Area	Blanking Area
1'd	1-th line	1-th line	1-th line
2'd	2-th line	2-th line	2-th line
3'd	3-th line	3-th line	3-th line
4'd	4-th line	4-th line	4-th line
:	:	:	:
320'd	320-th Line	320-th Line	320-th Line
:	Invalaid	:	:
400'd	Invalaid	400-th Line	400-th Line
:	Invalaid	Invalaid	:
432'd	Invalaid	Invalaid	432-th line
Other setting	Invalaid	Invalaid	Invalaid

Note: The related timing diagram can refer 7.3 Tearing effect output line for detail.

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8.42 OTP Control 5~6 (R87h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0
R	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0

Figure 8.109 OTP Control 6 register (PAGE0 - R87h)

OTP_KEY[7:0]: Control OTP Program mode Enable / Disable

OTP_KEY[7:0]	Description	Note
AAh	Enter OTP Program mode	When Enter OTP program mode, then other ccommend will be blocked unless OTP related commend.
55h	Leave OTP Program mode	-
Other value	Invalid	1. If OTP is in OTP program mode, then keep OTP program mode. 2. If OTP is in non-OTP program mode, then keep non-OTP program mode.

8.43 Command page select register (RFFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	PAGE_SEL1	PAGE_SEL0
R	1	0	0	0	0	0	0	PAGE_SEL1	PAGE_SEL0

Figure 8.110 Command page select 2 register (RFFh)

PAGE_SEL[1:0]: Command set page select.

PAGE_SEL1	PAGE_SEL0	Command Page
0	0	Page 0
0	1	Page 1

8.44 DGC control register (PAGE1 – R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	DGC_EN
R	1	0	0	0	0	0	0	0	DGC_EN

Figure 8.111 DGC control register (PAGE1 – R00h)

DGC_EN: Digital gamma correction enable.
0 : Disable
1 : Enable

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8.45 DGC LUT1~192 register (PAGE1 – R01h~C0h)

For more information about these registers, Please refer to "7.2.2 **Gray Voltage Generator for Digital Gamma Correction"** section.

8.46 CABC control 5~7 register (PAGE1 – RC3h, RC5h, RC7h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	PWM DIV2	PWM DIV1	PWM DIV0	1	1	INPL US	1
R	1	0	PWM DIV2	PWM DIV1	PWM DIV0	1	1	INPL US	1

Figure 8.112 CABC control 5 (PAGE1 – RC3h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PWM_ PERIOD7	PWM_ PERIOD6	PWM_ PERIOD5	PWM_ PERIOD4	PWM_ PERIOD3	PWM_ PERIOD2	PWM_ PERIOD1	PWM_ PERIOD0
R	1	PWM_ PERIOD7	PWM_ PERIOD6	PWM_ PERIOD5	PWM_ PERIOD4	PWM_ PERIOD3	PWM_ PERIOD2	PWM_ PERIOD1	PWM_ PERIOD0

Figure 8.113 CABC control 6 (PAGE1 – RC5h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	DIM_F RAME6	DIM_F RAME5	DIM_F RAME4	DIM_F RAME3	DIM_F RAME2	DIM_F RAME1	DIM_F RAME0
R	1	0	DIM_F RAME6	DIM_F RAME5	DIM_F RAME4	DIM_F RAME3	DIM_F RAME2	DIM_F RAME1	DIM_F RAME0

Figure 8.114 CABC control 7 (PAGE1 – RC7h)

PWM_DIV[2:0]: Internal PWM_CLK divider for CABC clock.

PWM_DIV[2:0]	Divider
0	PWM_CLK/1
1	PWM_CLK/2
2	PWM_CLK/4
3	PWM_CLK/8
4	PWM_CLK/16
5	PWM_CLK/32
6	PWM_CLK/64
7	PWM_CLK/128

Note: PWM_CLK is OSC frequency in any interface

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

PWM_PERIOD[7:0] : The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV)) x (255x(PWM_PERIOD[7:0]+1))

DIM_FRAME[6:0] : Manual brightness setting dimming period.

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8.47 Gain select register 0~8 (PAGE1 – RCBh~D3h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 06	DBG 05	DBG 04	DBG 03	DBG 02	DBG 01	DBG 00
R	1	0	DBG 06	DBG 05	DBG 04	DBG 03	DBG 02	DBG 01	DBG 00

Figure 8.115 Gain select register 0 (PAGE1 – RCBh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 16	DBG 15	DBG 14	DBG 13	DBG 12	DBG 11	DBG 10
R	1	0	DBG 16	DBG 15	DBG 14	DBG 13	DBG 12	DBG 11	DBG 10

Figure 8.116 Gain select register 1 (PAGE1 – RCCh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 26	DBG 25	DBG 24	DBG 23	DBG 22	DBG 21	DBG 20
R	1	0	DBG 26	DBG 25	DBG 24	DBG 23	DBG 22	DBG 21	DBG 20

Figure 8.117 Gain select register 2 (PAGE1 – RCDh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 36	DBG 35	DBG 34	DBG 33	DBG 32	DBG 31	DBG 30
R	1	0	DBG 36	DBG 35	DBG 34	DBG 33	DBG 32	DBG 31	DBG 30

Figure 8.118 Gain select register 3 (PAGE1 – RCEh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 46	DBG 45	DBG 44	DBG 43	DBG 42	DBG 41	DBG 40
R	1	0	DBG 46	DBG 45	DBG 44	DBG 43	DBG 42	DBG 41	DBG 40

Figure 8.119 Gain select register 4 (PAGE1 – RCFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 56	DBG 55	DBG 54	DBG 53	DBG 52	DBG 51	DBG 50
R	1	0	DBG 56	DBG 55	DBG 54	DBG 53	DBG 52	DBG 51	DBG 50

Figure 8.120 Gain select register 5 (PAGE1 – RD0h)

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R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 66	DBG 65	DBG 64	DBG 63	DBG 62	DBG 61	DBG 60
R	1	0	DBG 66	DBG 65	DBG 64	DBG 63	DBG 62	DBG 61	DBG 60

Figure 8.121 Gain select register 6 (PAGE1 – RD1h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 76	DBG 75	DBG 74	DBG 73	DBG 72	DBG 71	DBG 70
R	1	0	DBG 76	DBG 75	DBG 74	DBG 73	DBG 72	DBG 71	DBG 70

Figure 8.122 Gain select register 7 (PAGE1 – RD2h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 86	DBG 85	DBG 84	DBG 83	DBG 82	DBG 81	DBG 80
R	1	0	DBG 86	DBG 85	DBG 84	DBG 83	DBG 82	DBG 81	DBG 80

Figure 8.123 Gain select register 8 (PAGE1 – RD3h)

I

DBG0~8[6:0] : Gain select register 0~8

DBGX	Duty	DBGX	Duty	DBGX	Duty
20	100.00%	30	66.67%	40	49.80%
21	96.86%	31	65.10%		
22	94.12%	32	63.92%		
23	91.37%	33	62.75%		
24	89.02%	34	61.57%		
25	86.27%	35	60.39%		
26	84.31%	36	59.22%		
27	81.96%	37	58.04%		
28	80.00%	38	56.86%		
29	78.04%	39	56.08%		
2A	76.08%	3A	54.90%		
2B	74.51%	3B	54.12%		
2C	72.55%	3C	53.33%		
2D	70.98%	3D	52.16%		
2E	69.41%	3E	51.37%		
2F	67.84%	3F	50.59%		

	UI	ST	MV
DBG0	24	40	40
DBG1	24	3C	3C
DBG2	24	38	38
DBG3	23	34	34
DBG4	23	33	33
DBG5	23	32	32
DBG6	22	2B	2D
DBG7	22	24	2B
DBG8	22	22	28

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8.48 Power saving counter 1~4 (PAGE0 – RE4h~E7h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQVCI_M17	EQVCI_M16	EQVCI_M15	EQVCI_M14	EQVCI_M13	EQVCI_M12	EQVCI_M11	EQVCI_M10
R	1	EQVCI_M17	EQVCI_M16	EQVCI_M15	EQVCI_M14	EQVCI_M13	EQVCI_M12	EQVCI_M11	EQVCI_M10

Figure 8.124 Power saving register 1 (PAGE0 – RE4h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQGNDM17	EQGNDM16	EQGNDM15	EQGNDM14	EQGNDM13	EQGNDM12	EQGNDM11	EQGNDM10
R	1	EQGNDM17	EQGNDM16	EQGNDM15	EQGNDM14	EQGNDM13	EQGNDM12	EQGNDM11	EQGNDM10

Figure 8.125 Power saving register 2 (PAGE0 – RE5h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQVCI_M07	EQVCI_M06	EQVCI_M05	EQVCI_M04	EQVCI_M03	EQVCI_M02	EQVCI_M01	EQVCI_M00
R	1	EQVCI_M07	EQVCI_M06	EQVCI_M05	EQVCI_M04	EQVCI_M03	EQVCI_M02	EQVCI_M01	EQVCI_M00

Figure 8.126 Power saving register 3 (PAGE0 – RE6h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQGNDM07	EQGNDM06	EQGNDM05	EQGNDM04	EQGNDM03	EQGNDM02	EQGNDM01	EQGNDM00
R	1	EQGNDM07	EQGNDM06	EQGNDM05	EQGNDM04	EQGNDM03	EQGNDM02	EQGNDM01	EQGNDM00

Figure 8.127 Power saving register 4 (PAGE0 – RE7h)

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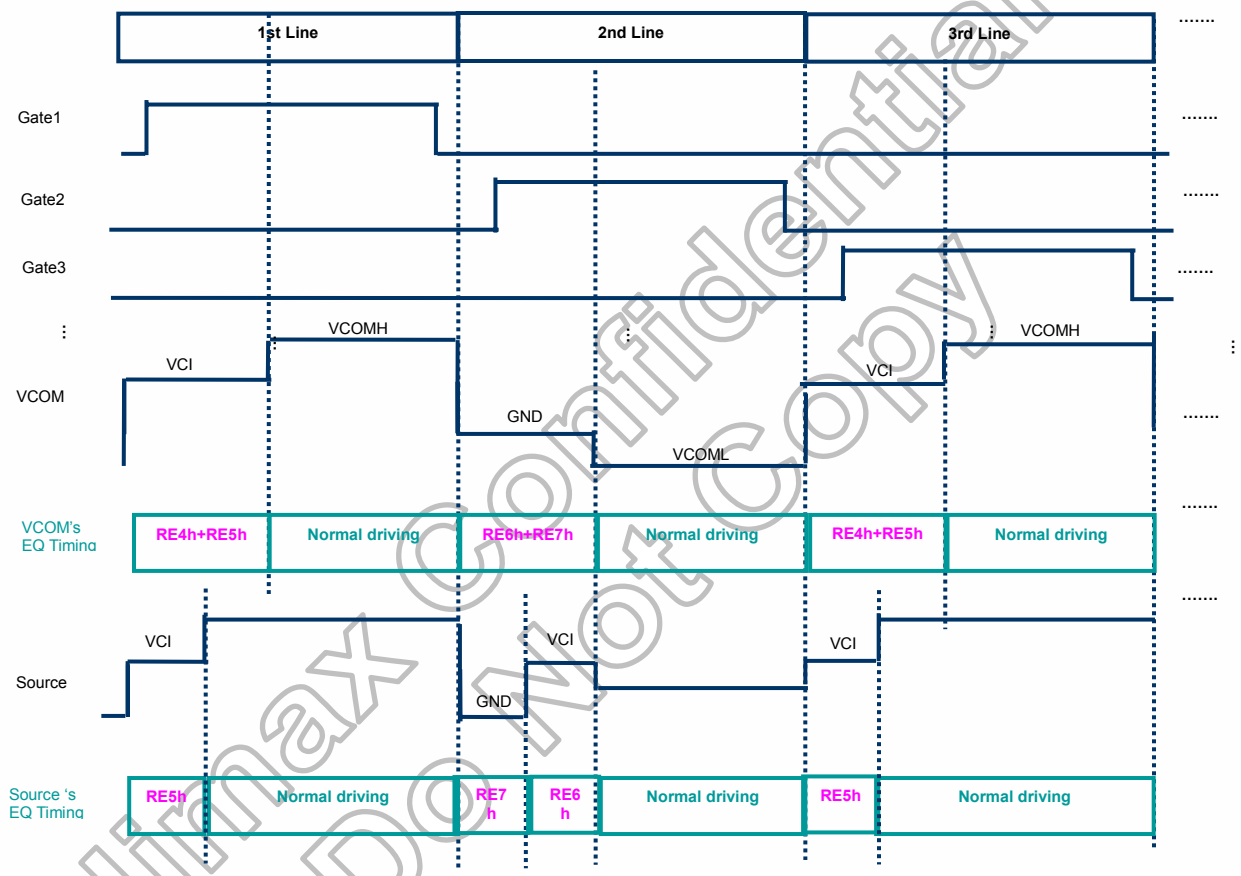
EQVCI_M1[7:0]: used to tuned the timing of EQ function to save power.
EQGND_M1[7:0]: used to tuned the timing of EQ function to save power.
EQVCI_M0[7:0]: used to tuned the timing of EQ function to save power.
EQGND_M0[7:0]: used to tuned the timing of EQ function to save power.

Which,
1) RE4h+RE5h: Conteol EQ_VCI of VCOM during period of VCOMH.
2) RE6h+RE7h: Conteol EQ_GND of VCOM during period of VCOML.
3) RE5h: Conteol EQ_VCI of Source during period of VCOMH.
4) RE6h+RE7h: Conteol (EQ_GND+EQ_VCI) of VCOM during period of VCOML.
   RE6h: Cotrol EQ_GND of Source.
   RE7h: Cotrol EQ_VCI of Source.



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9. Layout Recommendation

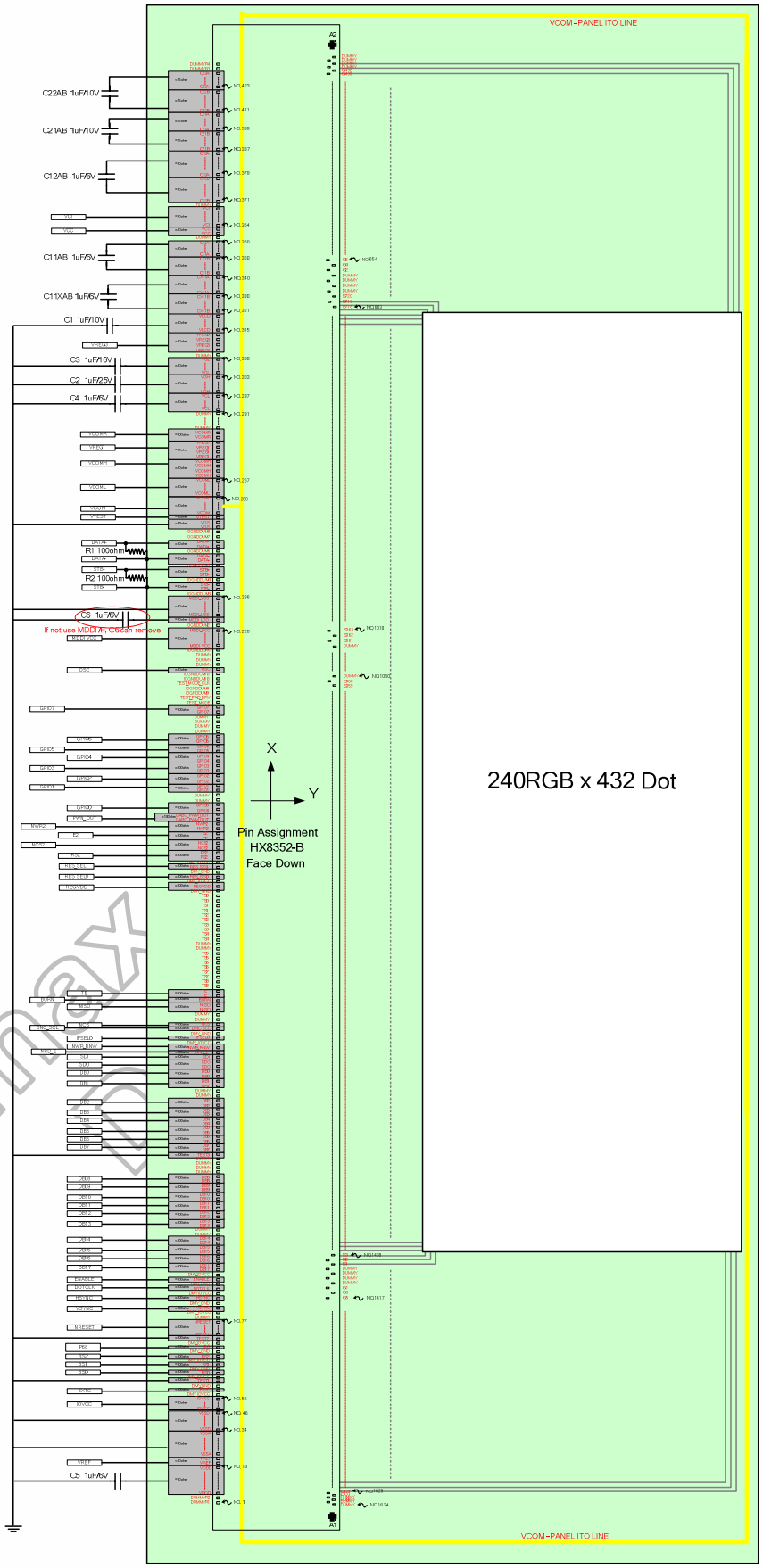

Figure 9.1 ayout Recommendation of HX8352-B01

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9.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
MDDI_VCC	Power supply	10	Ω
MDDI_VSS	Power supply	10	Ω
OSC	Input	100	Ω
BS3, BS[2:0], BURN, REGVDD, RES_SEL[1:0], IFSEL0	Input	100	Ω
nWR_RNW, nRD_E, nCS, nRESET, DNC_SCL, SDI	Input	100	Ω
VSYNC, HSYNC, DOTCLK, ENABLE	Input	100	Ω
STBP, STBN, DATAP, DATAN	Input	10	Ω
VCOMR	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
VLCD	Capacitor connection	10	Ω
VREG1	Output	10	Ω
VREG3	Output	10	Ω
VDDD	Capacitor connection	30	Ω
MDDI_LDO	Capacitor connection	10	Ω
VCOM, VCOMH, VCOML	Output	10	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
NCS2, RS2, NWR2, E2, TE, NISD, SDO PWM_ OUT, VREF, VTESET	Output	100	Ω
GPIO7-0, DB[17:0]	Input/Output	100	Ω

Table 9.1 Maximum layout resistance

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9.2 External components connection

Capacitor	Recommended voltage	Capacity
C1 (VLCD-VSSA)	10V	1 μF (B characteristics)
C2 (VGH-VSSA)	25V	1 μF (B characteristics)
C3 (VGL-VSSA)	16V	1 μF (B characteristics)
C4 (VCL-VSSA)	6V	1 μF (B characteristics)
C5(VDDD-VSSA)	6V	1 μF (B characteristics)
C11AB (C11A/B)	6V	1 μF (B characteristics)
CX11AB (CX11A/B)	6V	1 μF (B characteristics)
C12AB (C12A/B)	6V	1 μF (B characteristics)
C21AB (C21A/B)	10V	1 μF (B characteristics)
C22AB (C22A/B)	10V	1 μF (B characteristics)
C6 (MDDI_LDO-MDDI_VSS)	6V	1 μF (B characteristics)
R1, R2	Resistor	(100 ± 2%) ohm

Note: If MDDI I/F is not used, the C6, R1, R2 can be removed.

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10. OTP Programming

10.1 OTP table

OTP_INDEX	D7	D6	D5	D4	D3	D2	D1	D0
0x00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
0x01h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
0x02h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
0x03h	VMF17	VMF16	VMF15	VMF14	VMF13	VMF12	VMF11	VMF10
0x04h	VMF27	VMF26	VMF25	VMF24	VMF23	VMF22	VMF21	VMF20
0x05h	VMF37	VMF36	VMF35	VMF34	VMF33	VMF32	VMF31	VMF30
0x06h	VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0
0x07h	VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0
0x08h	Vaild_ID	(No used)		Valid_VML	Valid_VMH	Valid_VMF3	Valid_VMF2	Valid_VMF1
0x09h	Valid_panel	(No used)	DDVDH_TRI	Himax internal use (not open)				
0x0Ah	Himax internal use (not open)							
0x0Bh	Himax internal use (not open)							
0x0Ch	Himax internal use (not open)							
0x0Dh	Himax internal use (not open)							
0x0Eh	Himax internal use (not open)							
0x0Fh	Himax internal use (not open)							
0x10h	Himax internal use (not open)							
0x11h	Himax internal use (not open)							
0x12h	Himax internal use (not open)							
0x13h	Himax internal use (not open)							
0x14h	Himax internal use (not open)							
0x15h	Himax internal use (not open)							
0x16h	Himax internal use (not open)							
0x17h	Himax internal use (not open)							
0x18h	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
0x19h	Himax internal use (not open)							
0x1Ah	Himax internal use (not open)							
0x1Bh	Himax internal use (not open)							
0x1Ch	Himax internal use (not open)							
0x1Dh	Himax internal use (not open)							
0x1Eh	Himax internal use (not open)							
0x1Fh	Himax internal use (not open)							
0x20h	Himax internal use (not open)							
0x21h	Himax internal use (not open)							
0x22h	Himax internal use (not open)							

Note: (1) The default value of OTP memory bits are all “1”.

(2) VALID_xxx bit decide the OPT reload Enable/Disable, the default value is “1”. If Valid_xxx correlation OTP_Mask bit is “0” and set OTP_PORG to “1”, the VALID_xxx bit will be changed to “0” automatically and execute the OTP reload.
For example:
Condition 1: Programmed all index of 0x00h ~ 0x2h and 0x18h and Index-0x08h’s bit 7.

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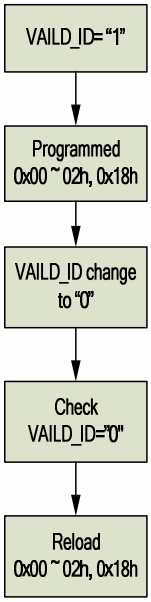
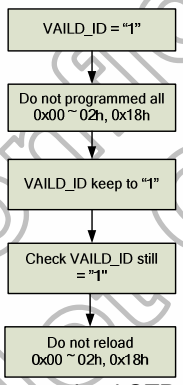


Condition 2: Do not program all index of 0x00h ~ 0x2h and 0x18h



(3) There are some conditions that HX8352-B01 can reload OTP.
1.Hardware reset

(4) VMF can be programed 3 times: Default Valid_VMF1 will be programed when CP.

The value of Valid_VMF3~1	Status of index 0x03h ~ 0x05h
Valid_VMF3~1="111"	Not program any VMF1~3[7:0],
Valid_VMF3~1="110"	Only program VMF1[7:0] and reload VMF1[7:0]
Valid_VMF3~1="101"	Only program VMF2[7:0] and reload VMF2[7:0]
Valid_VMF3~1="100"	Already program VMF1~2[7:0] and reload VMF2[7:0]
Valid_VMF3~1="011"	Only program VMF3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="010"	Already program VMF1[7:0], VMF3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="001"	Already program VMF2~3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="000"	Already program VMF1~3[7:0] and reload VMF3[7:0]

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10.2OTP programming flow

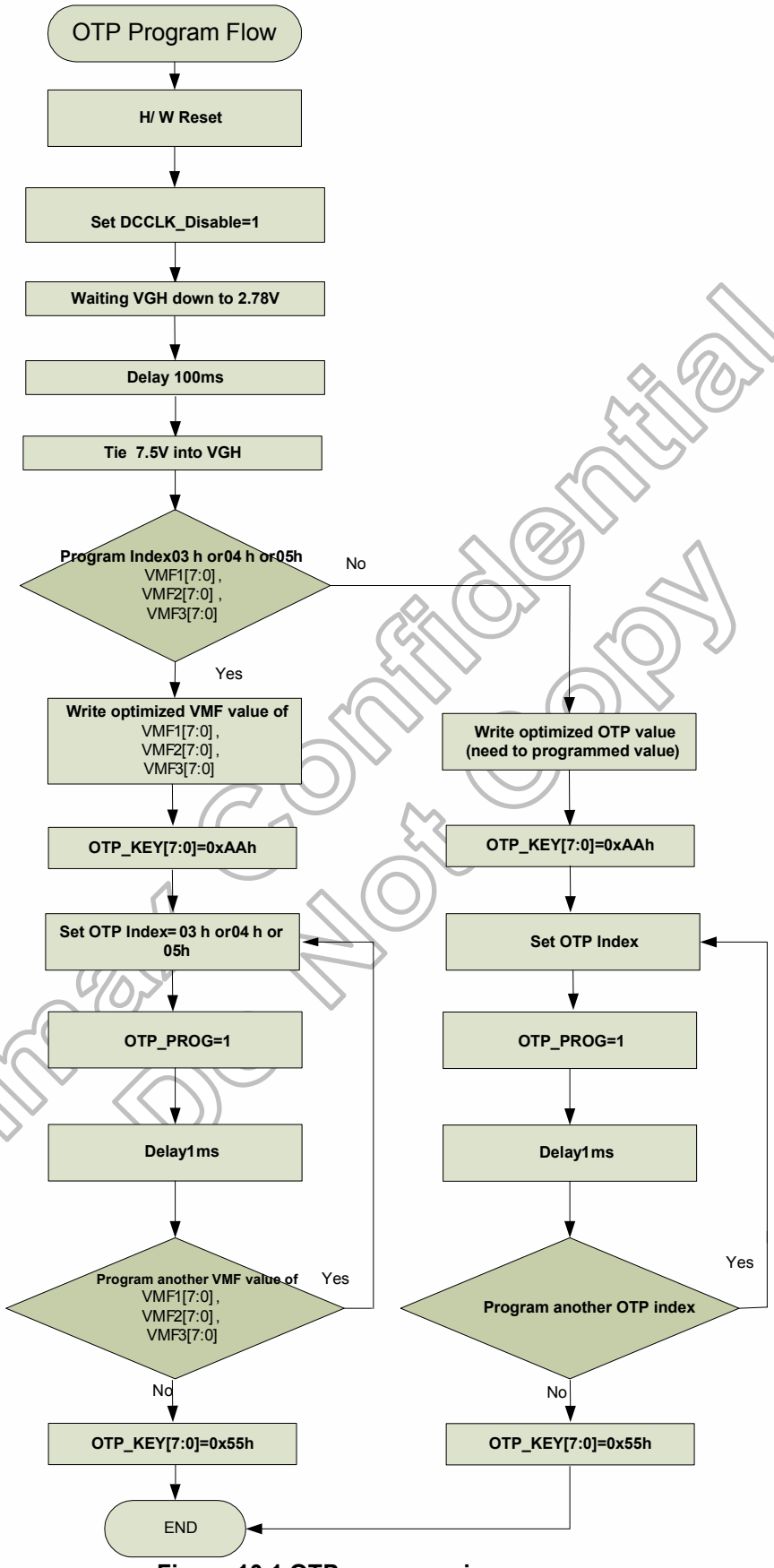

Figure 10.1 OTP programming sequence

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For example: ID1~ID4 programming flow

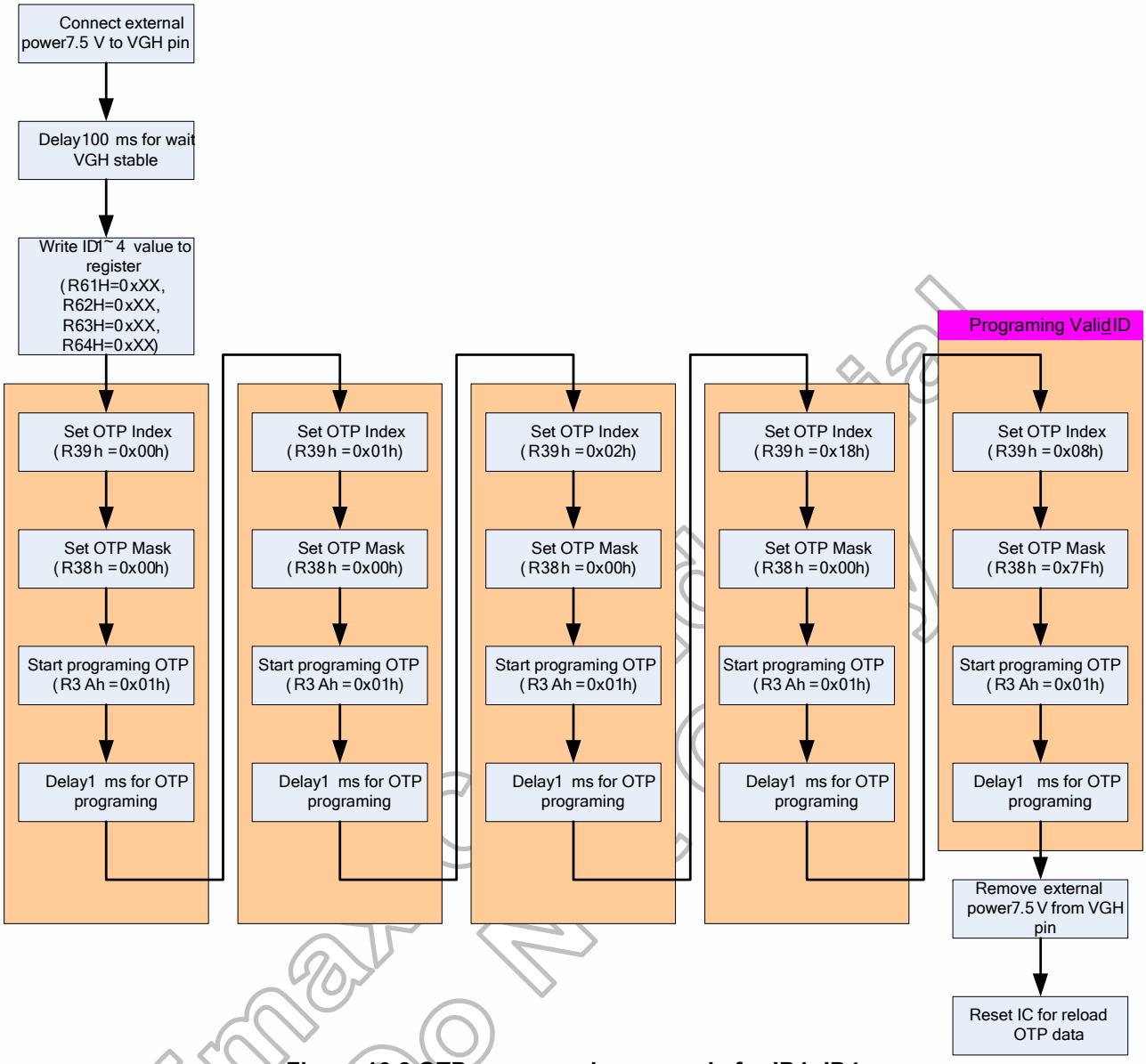

Figure 10.2 OTP programming example for ID1~ID4

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10.3 OTP programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Set DCCLK_DISABLE=1 (Set R1Ah=0x14h)</td></tr>
<tr><td>3</td><td>Connect external power 7.5V to VGH pin</td></tr>
<tr><td>4</td><td>Wait 100ms for VGH stable</td></tr>
<tr><td>5</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td>ID1 (R61h)</td><td>ID1[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID2 (R62h)</td><td>ID2[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID3 (R63h)</td><td>ID3[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>VCOM Control 1 (R23h)</td><td>VMF[7:0],</td><td>Vcom offset voltage for normal mode, Idle mode and Partial Idle mode (High level voltage of VCOM)</td></tr>
<tr><td>VCOM Control 2 (R24h)</td><td>VMH[7:0]</td><td>VcomH voltage for normal mode, Idle mode and Partial Idle mode (High level voltage of VCOM)</td></tr>
<tr><td>VCOM Control 3 (R25h)</td><td>VML[7:0]</td><td>VcomL voltage for normal mode, Idle mode and Partial Idle mode (Low level voltage of VCOM)</td></tr>
<tr><td>ID4 (R64h)</td><td>ID4[7:0]</td><td>LCD module/driver version</td></tr>
</table></td></tr>
<tr><td>6</td><td>Set OTP_KEY[7:0]=0xAAh, Enter OTP program mode.</td></tr>
<tr><td>7</td><td>Specify OTP_index (Note 1)
<table>
<tr><th>OTP_index (Write – For Program)</th><th>Parameter</th></tr>
<tr><td>0x00h</td><td>ID1[7:0]</td></tr>
<tr><td>0x01h</td><td>ID2[7:0]</td></tr>
<tr><td>0x02h</td><td>ID3[7:0]</td></tr>
<tr><td>0x03h</td><td>VMF1[7:0]</td></tr>
<tr><td>0x04h</td><td>VMF2[7:0]</td></tr>
<tr><td>0x05h</td><td>VMF37:0]</td></tr>
<tr><td>0x06h</td><td>VMH[7:0]</td></tr>
<tr><td>0x07h</td><td>VML[7:0]</td></tr>
<tr><td>0x08h</td><td>Vaild_ID, Valid_VML, Valid_VMH, Valid_VMF3, Valid_VMF2, Valid_VMF1</td></tr>
<tr><td>0x18h</td><td>ID4[7:0]</td></tr>
</table></td></tr>
<tr><td>8</td><td>Set OTP_Mask=0x00h, programming the entire bit of one parameter.</td></tr>
<tr><td>9</td><td>Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>10</td><td>Wait 1 ms</td></tr>
<tr><td>11</td><td>Complete programming one parameter to OTP. If continue to programming other parameter, return to step (5). Otherwise, set OTP_KEY[7:0]=0x55h, power off the module and remove the external power on VGH pin.</td></tr>
<tr><td>12</td><td>Remove external power 7.5V from VGH pin</td></tr>
</table>

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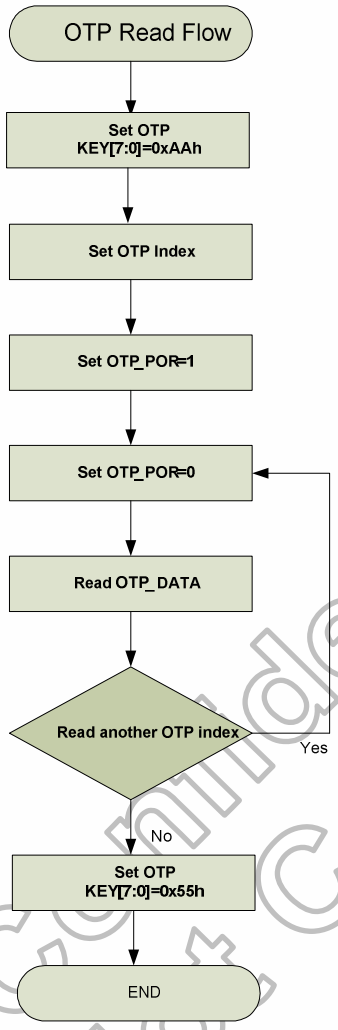
10.4 OTP Read flow



For example: OTP ID1 read flow

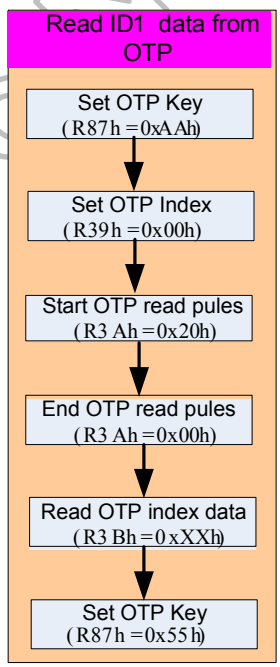


Figure 10.3 OTP read example for ID1

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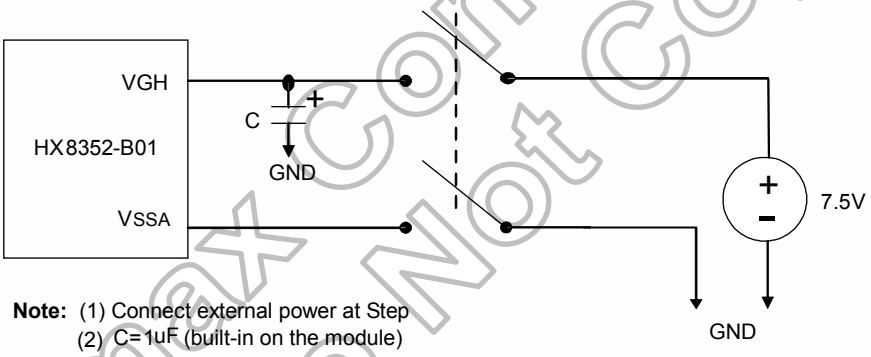
10.5 OTP read sequence

Step	Operation
1	Set OTP_KEY[7:0]=0xAAh (R87h=0xAAh), Enter OTP program mode.
2	Specify OTP_index OTP_index (Read – For get OTP value) / Parameter 0x00h / ID1[7:0] 0x01h / ID2[7:0] 0x02h / ID3[7:0] 0x03h / VMF1[7:0], 0x04h / VMF2[7:0] 0x05h / VMF37:0] 0x06h / VMH[7:0] 0x07h / VML[7:0] 0x08h / Vaild_ID, Valid_VML, Valid_VMH, Valid_VMF3, Valid_VMF2, Valid_VMF1 0x18h / ID4[7:0]
3	Set OTP_POR=1.
4	Set OTP_POR=0.
5	Read OTP_DATA.
6	If OTP read had finished, then Set OTP_KEY[7:0]=0x55h (R87h=0x55h). Leave OTP program mode.

10.6 Programming circuitry



Note: (1) Connect external power at Step
(2) C=1uF (built-in on the module)

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11.Electrical Characteristics

11.1 Absolute maximum ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.8	Note(1),(3)
Power Supply Voltage 3	VCC ~ VSSA	V	-0.3 to +4.8	Note(1),(4)
Power Supply Voltage 4	VLCD ~ VSSA	V	-0.3 to +6.6	Note(5)
Power Supply Voltage 5	VSSA ~ VCL	V	-0.3 to +4.6	Note(6)
Power Supply Voltage 6	VLCD ~ VCL	V	-0.3 to +9	Note(7)
Power Supply Voltage 7	VREG1 ~ VSSA	V	-0.3V to VLCD – 0.5	Note(8)
Power Supply Voltage 8	VREG3 ~ VSSA	V	-03V to VLCD-0.5	Note(9)
Power Supply Voltage 9	VGH ~ VSSA	V	-0.3 to +18.5	Note(9)
Power Supply Voltage 10	VSSA ~ VGL	V	0 to -16.5	Note(10)
Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.3	-
Operating Temperature	Topr	℃	-40 to +85	Note(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure VCC ≥ VSSA.
(5) To make sure VLCD ≥ VSSA.
(6) To make sure VSSA ≥ VCL.
(7) To make sure VLCD ≥ VCL.
(8) To make sure VREG1 <= VLCD-0.5V.
(9) To make sure VREG3 > VSSA.
(10) To make sure VGH ≥ VSSA.
(11) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(10) For die and wafer products, specified up to +85℃.

Table 11.1 Absolute maximum ratings

11.2 ESD protection level

Mode	Test Condition	Protection Level	Unit
Human Body Model	C=100 pF, R=1.5 kΩ	TBD	V
Machine Model	C=200 pF, R=0.0 Ω	TBD	V

Table 11.2 ESD protection level

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11.3 DC characteristics

(VCC=VCI= 2.3 ~ 3.3V, IOVCC = 1.65~3.3V, T_A = -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Spec.			Note
				Min.	Typ.	Max.	
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.7xIOVCC	-	IOVCCc	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVCC	-
Output high voltage (DB17-0 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVCC	-	-	-
Output low voltage (DB17-0Pins)	V_{OL1}	V	IOVcc= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVCC	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ VCC	-1	-	1	-
Current consumption during normal operation (VCI-VSSD)	$I_{OP(VCI)}$	mA	VCI=2.8V VCC =2.8V ,IOVCC=2.8V T_A=25°C , GRAM data = 0000h, Frame rate =60Hz, REV_panel=0, AP=100, FS0=001, FS1=001, BT=0000, VRH=01_1110, VCOMG=1 With standard panel	-	8	-	-
Current consumption during normal operation (VCC– VSSD)	$I_{OP(VCC)}$	uA		-	25	-	-
Current consumption during normal operation (IOVCC-VSSD)	$I_{OP(IOVCC)}$	mA		-	0.55	-	-
Current consumption during standby mode (VCI-VSSD)	$I_{ST(Vci)}$	µA	VCI=2.8V, IOVCC=2.8V , VCC=2.8V T_A =25°C	-	1	5	-
Current consumption during standby mode (VCC– VSSD)	$I_{ST(Vcc)}$	µA		-	2	5	-
Current consumption during standby mode (IOVCC-VSSD)	$I_{ST(IOVcc)}$	µA		-	5	20	-
Current consumption during Deep-standby mode (VCI-VSSD)	$I_{DP-ST(Vci)}$	µA	VCI=2.8V, IOVCC=2.8V , VCC=2.8V T_A =25°C	-	1	5	-
Current consumption during Deep-standby mode (VCC– VSSD)	$I_{DP-ST(Vcc)}$	µA		-	2	5	-
Current consumption during Deep-standby mode (IOVCC-VSSD)	$I_{DP-ST(ioVcc)}$	µA		-	3	10	-
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 11.3 DC characteristics

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(MDDI_VDD= 2.3 ~ 3.3V, T_A = -40 ~ 85 °C)

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	0	50	mV
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic-zero level.	-50	0	-	-
V_{IT+_hib}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	125	175	mV
V_{IT-_hib}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as a logic-zero level.	75	125	-	mV
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0	-	1.65	V

Table 11.4 MDDI DC characteristics

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11.4 AC characteristics

11.4.1 Parallel interface characteristics (8080-series MPU)

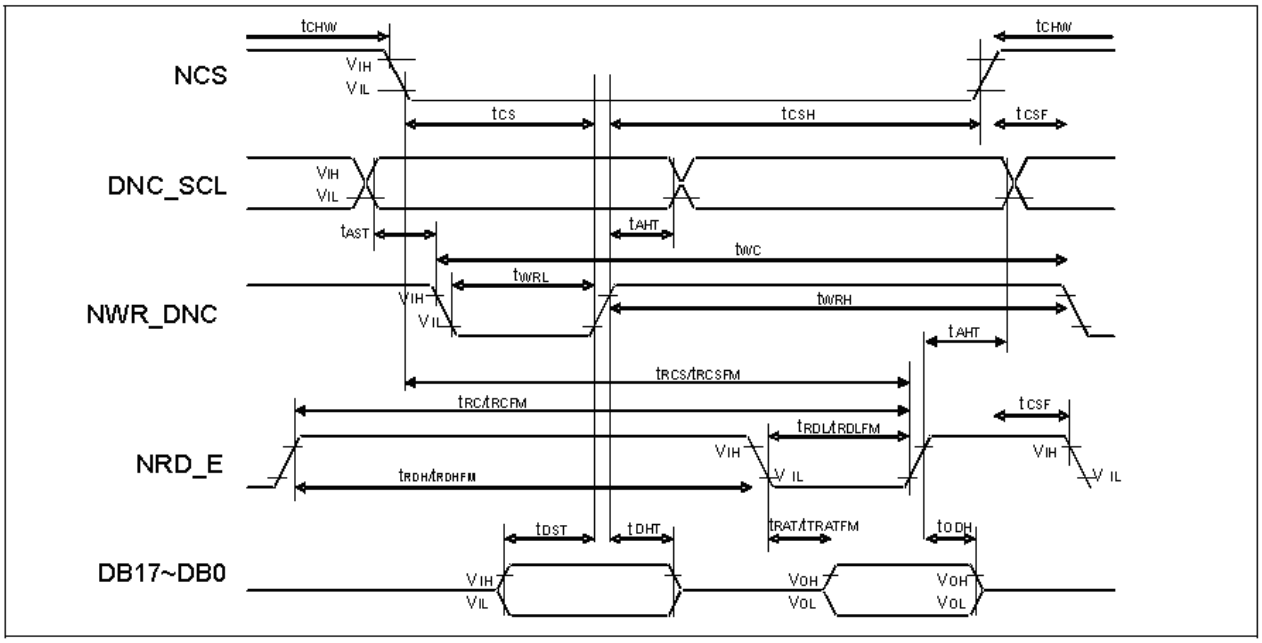


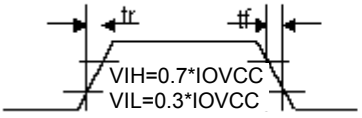
Figure 11.1 Parallel interface characteristics (8080-series MPU)

(T_A = -40 to 85℃)

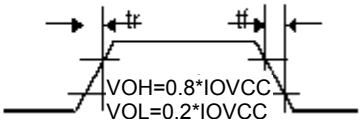
Signal	Symbol	Parameter	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time Chip select wait time (Write/Read) Chip select hold time	0 35 355 10 10	- - - - -	- - - - -	ns	-
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	66 15 15	- - -	- - -	ns	-
NRD_E	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle Control pulse “H” duration Control pulse “L” duration	450 90 355	- - -	- - -	ns	When read from GRAM
DB17-0	t_{DST} t_{DHT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time Output disable time	15 10 - 20(4)	- - - -	- - 340(4) 80(4)	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) t_{RDL} + t_{RD} >= 150ns, t_{RDHFM} + t_{RDLFM} >= 250ns.
(4) t_{RATFM} and t_{ODH} are defined by IOVCC = 1.65V ~ 1.95V.

Input Signal Slope



Output Signal Slope



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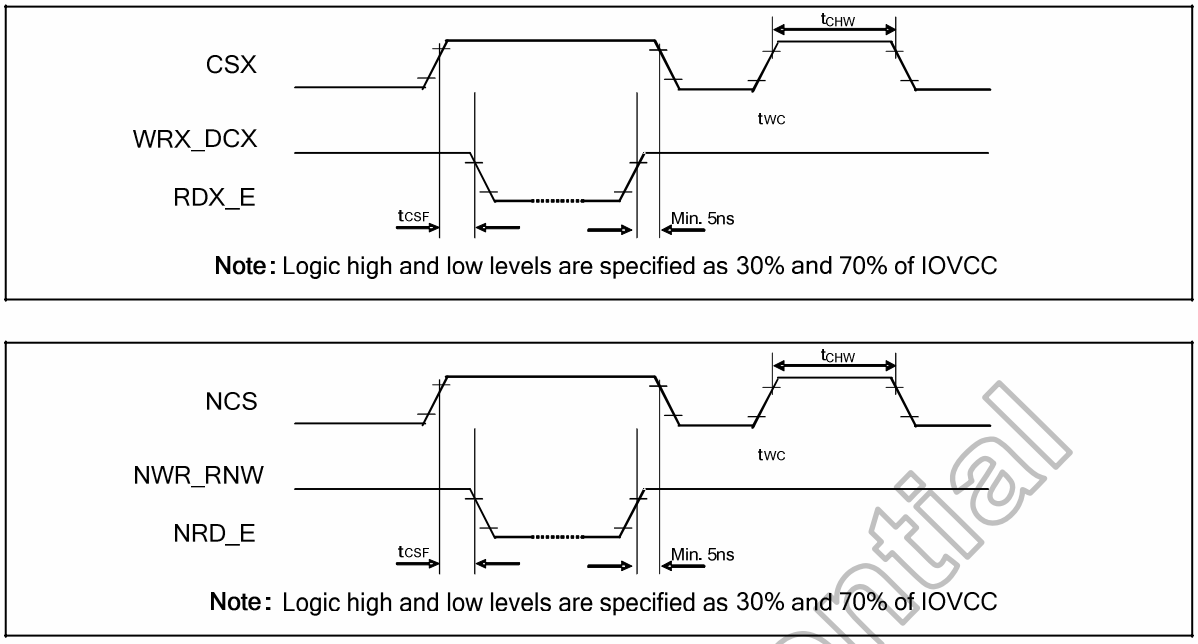

Figure 11.2 Chip select timing

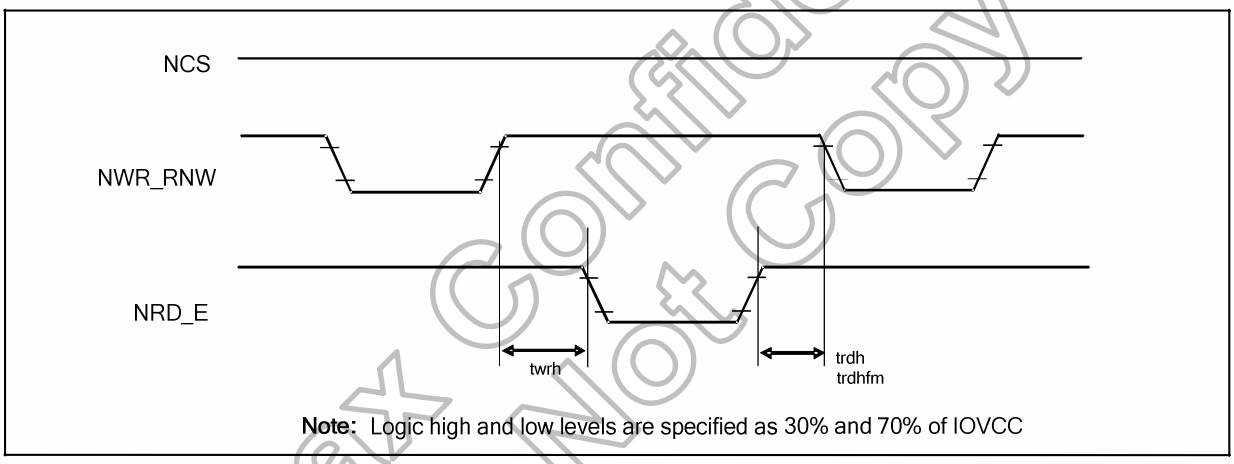

Figure 11.3 Write to read and read to write timing

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11.4.2 Serial interface characteristics

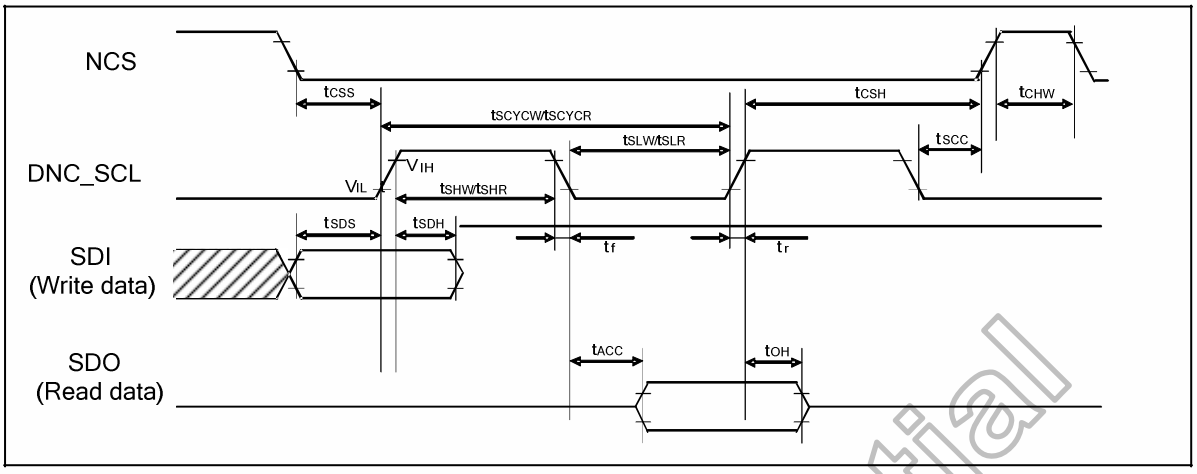


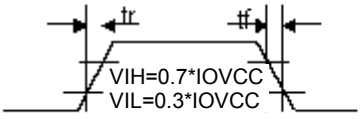
Figure 11.4 Serial interface characteristics

(T_A = -40 to 85℃)

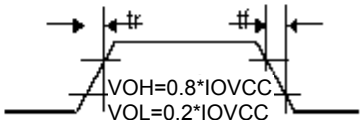
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Serial clock cycle (Write) DNC _SCL "H" pulse width (Write) DNC _SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	DNC_SCL	100 35 35	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDI	30 30	- -	- -	ns
Serial clock cycle (Read) DNC _SCL "H" pulse width (Read) DNC _SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	DNC _SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDA for maximum C_L=30pF For minimum C_L=8pF	45	-	100	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15(3)	-	100(3)	ns
DNC _SCL to Chip select	t_{SCC}	DNC _SCL, NCS	15(3)	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	45	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 65	- -	- -	ns

Note: (1)The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2)Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) t_{ACC} and t_{OH} are defined by IOVCC=1.65V~1.95V.

Input Signal Slope



Output Signal Slope



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11.4.3 RGB interface characteristics

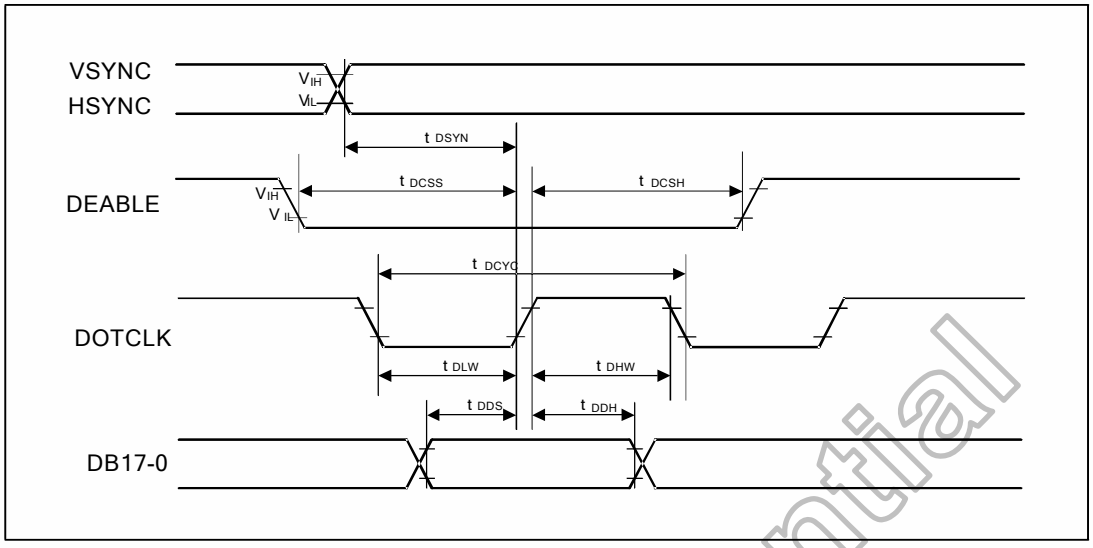
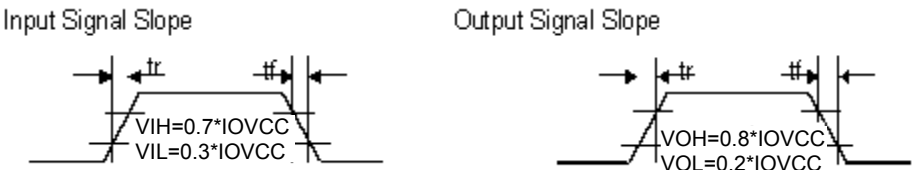


Figure 11.5 RGB interface characteristics

(T_A = -40 to 85℃)

Symbol	Parameter	Conditions	Related Pins	Spec.			Unit
				Min.	Typ.	Max.	
t_{DCYC}	PCLK cycle time	VRR = Min . 50 Hz Max. 65 Hz	PCLK	60(2)	-	226(3)	ns
t_{DLW} t_{CHW}	PCLK Low time PCLK High time	-		15 15	- -	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	PCLK, DB17-DB0	15 15	- -	- -	ns
t_{DCSS} t_{DCSH}	DE setup time DE hold Time	-	DE	15 15	-	-	ns
t_{DSYN}	SYNC setup time	-	PCLK, HS, VS	15	-	-	ns

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) 16.6 MHz
(3) 4.4MHz



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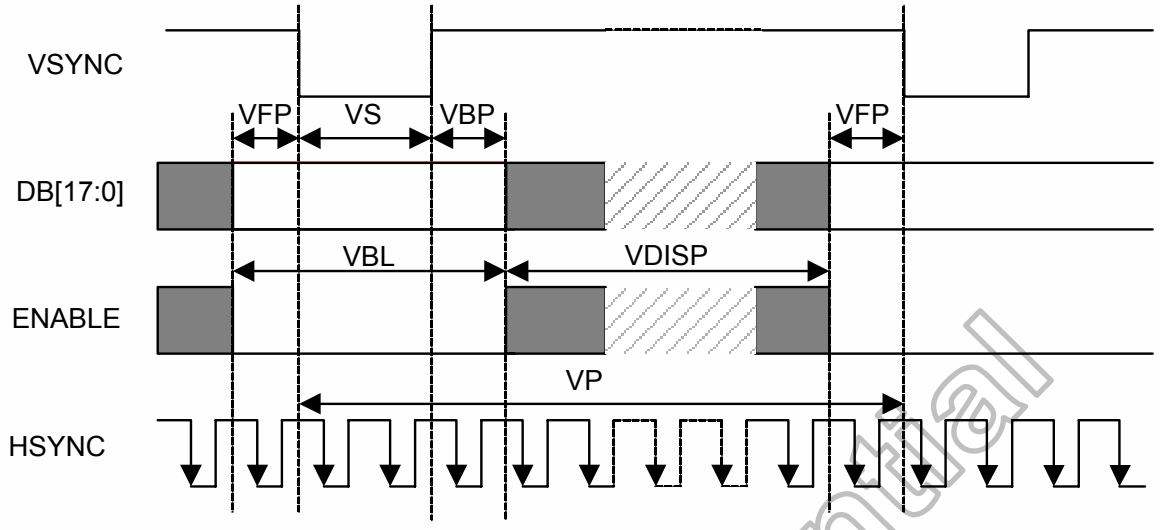
Vertical timings for RGB I/F



(T_A = -40 to 85℃)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
VSYNC Low Pulse Width	VS	-	1	-	16	Line
Vertical Back Porch	VBP	-	1	-	63	Line
Vertical Front Porch	VFP	-	1	-	63	Line
Vertical Blanking period	VBL	VS + VBP + VFP	3	-	142	Line
Vertical Active Area	VDISP	-	320	-	432	Line
VSYNC Cycle	VP	-	323	-	574	Line

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) The frequence of DOTCLK do not limited by frame rate.
(4) The recommmadn setting: Frame rate operate within 55Hz ~ 65Hz.

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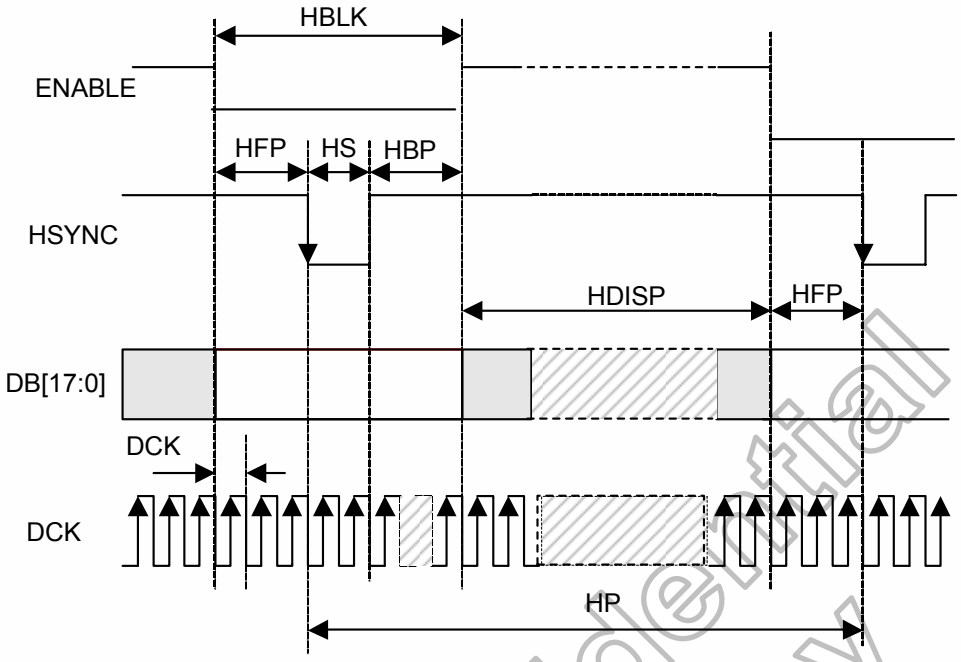
Horizontal timings for RGB I/F



(VSSA=0V, IOVCC=1.65V to 3.3V, VCC=2.3V TO 3.3V, VCI=2.3V to 4.8V, T_A = -40 to 85℃)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
HSYNC Low Pulse Width	HS	R17h=0x5Xh, R17h=0x6Xh.	1	-	53	DCK
		R17h=0x4Xh.	3			
Horizontal Back Porch	HBP	R17h=0x5Xh, R17h=0x6Xh.	1	-	53	DCK
		R17h=0x4Xh.	3			
Horizontal Front Porch	HFP	R17h=0x5Xh, R17h=0x6Xh.	1	-	53	DCK
		R17h=0x4Xh.	3			
Horizontal Blanking period	HBLK (4)	R17h=0x5Xh, R17h=0x6Xh.	3	-	159	DCK
		R17h=0x4Xh.	9			
Horizontal Active Area	HDISP	-	-	240	-	DCK
HSYNC Cycle	HP	R17h=0x5Xh, R17h=0x6Xh.	243	-	399	DCK
		R17h=0x4Xh.	249			

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3)The frequence of DOTCLK do not limited by frame rate.
(4) HBLK = HS + HBP + HFP.

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11.4.4 Reset input timing

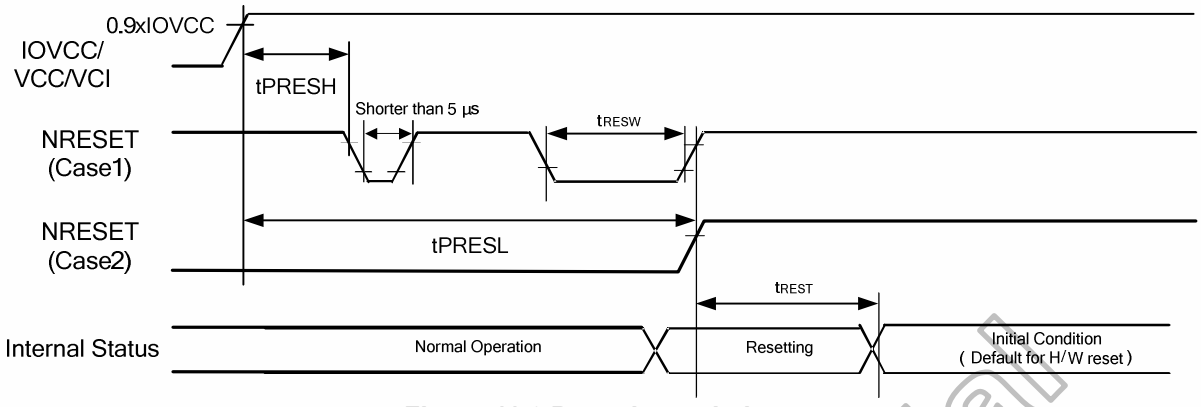


Figure 11.6 Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	10	When reset applied during STB mode	ms
		-	-	-	120	When reset applied during STB mode	ms
tPRESH	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms
tPRESL	Reset goes low level in Power on time	NRESET & IOVCC	5	-	-	Reset goes low level in Power on	ms

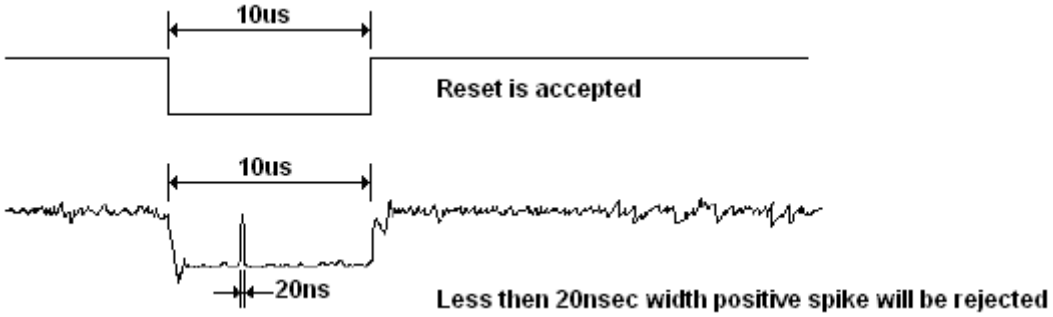
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 10msec after releasing NRESET before sending commands. Also STB Out

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11.4.5 MDDI interface characteristics

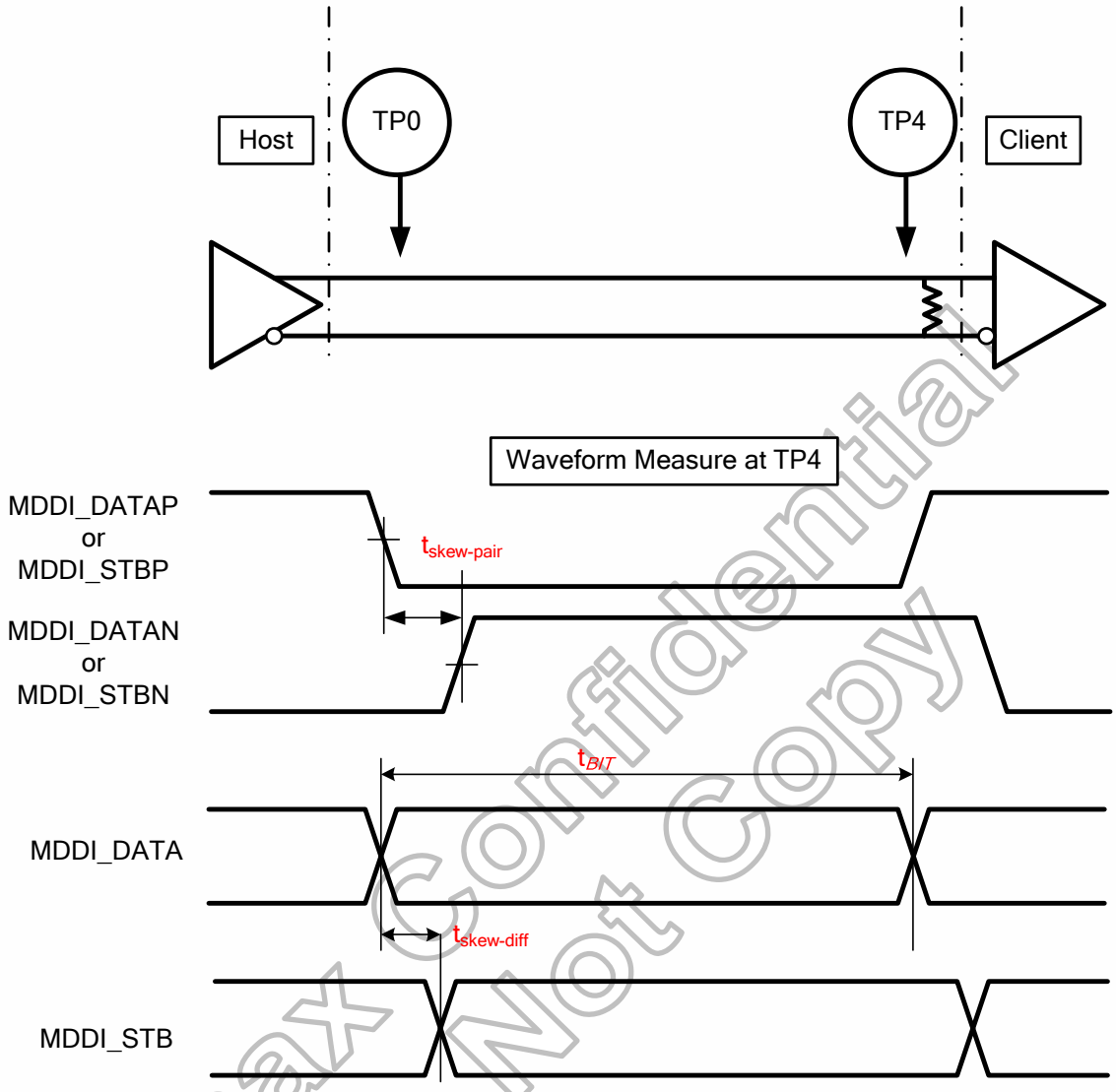

Figure 11.7 MDDI interface characteristics

Symbol	Parameter	Spec.			Unit
		Min	Typ	Max	
$1/t_{BIT}$		-	150	220	Mbps
$t_{skew-pair}$	Skew between positive and negative inputs of the differential receiver of the same differential pair (intra-pair skew)	-0.25	0	0.25	ns
$t_{skew-diff}$	Peak delay skew between one differential pair and any other differential pair	-0.3	0	0.3	ns

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12. Ordering Information

Part No.	Package
HX8352-B01000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 300 μm)

13. Revision History

Version	Date	Description of Changes
01	2009/03/24	New setup
	2009/05/13	1. Modify BS3 pin name as BS3(P68) in P16. 2. Modify PAD coordinates in P21~27. 3. Add 2% torlance for R1, R2 of MDDI IF in P221.1
	2009/07/06	1. Modify Pin description (IFSEL0, BS3-0) in P16. 2. Modify Pin description (VCL, VGL) in P 18~19. 3. Modify defaule value in p163, P165 4. Add notice for R17h in P180. 5. Modify descrotion of R1Ah in P182. 6. Modify description of R1Ch in P184. 7. Updated OTP table in P223. 8. Updated AC characteristics in P233~235. 9. Updated MDDI interface characteristics in P240.

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