# DATA SHEET

*( DOC No. HX8353-C(N)-DS )*

# HX8353-C

132RGB x 162 dot, 262K Color,
with Internal GRAM,
TFT Mobile Single Chip Driver

*Preliminary version 01, February 2008*



**Himax Technologies, Inc.**
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# 1. General Description

This manual describes the Himax's HX8353-C 132RGB*162 dots resolution driving controller. The HX8353-C(N) is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 128RGB*160 dots at maximum.

The HX8353-C can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8353-C also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8353-C is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

## 2. Features

- Single chip solution to drive a TFT panel
- 132RGB x 162-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support resolution:
  - 132RGB x 162-dot: Display with 132 x 18-bits x 162 display RAM (S45AP)
  - 128RGB x 160-dot
    - Type 1: Display with 128 x 18-bits x 160 display RAM (S44AP)
    - Type 2: Display with 132 x 18-bits x 162 display RAM (S43AP)
  - 128RGB x 128-dot
  - 120RGB x 160-dot
  - 96RGB x 68-dot: Display with 96 x 18-bits x 68 display RAM (S31AL)
  - 96RGB x 64-dot
- Internal operation circuit of liquid crystal display:
  - Source channel: 396ch (132RGB)
  - Gate line: 162 Gate output
- Display mode (Color modes):
  - Full colors
    - 262k colours (18bit 6(R):6(G):6(B))
  - Reduce color mode:
    - 65k colours (16bit 5(R):6(G):5(B))
    - 4k colours (12bit 4(R):4(G):4(B))
    - 8 colors (Idle mode on): 8 colors (3 bit binary mode)
- Internal graphics RAM capacity: 132 x 162 x 18-bit = 0.38M bit:
- Support interface mode:
  - I80 System interface: 8-bits / 9-bits / 16-bits / 18bits bus
  - m68 System interface: 8-bits / 9-bits / 16-bits / 18bits bus
  - 3W/4W Serial Data Transfer Interface
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- On chip features:
  - DC/DC converter
  - OTP to store initialization register setting
  - Oscillator for display clock generation

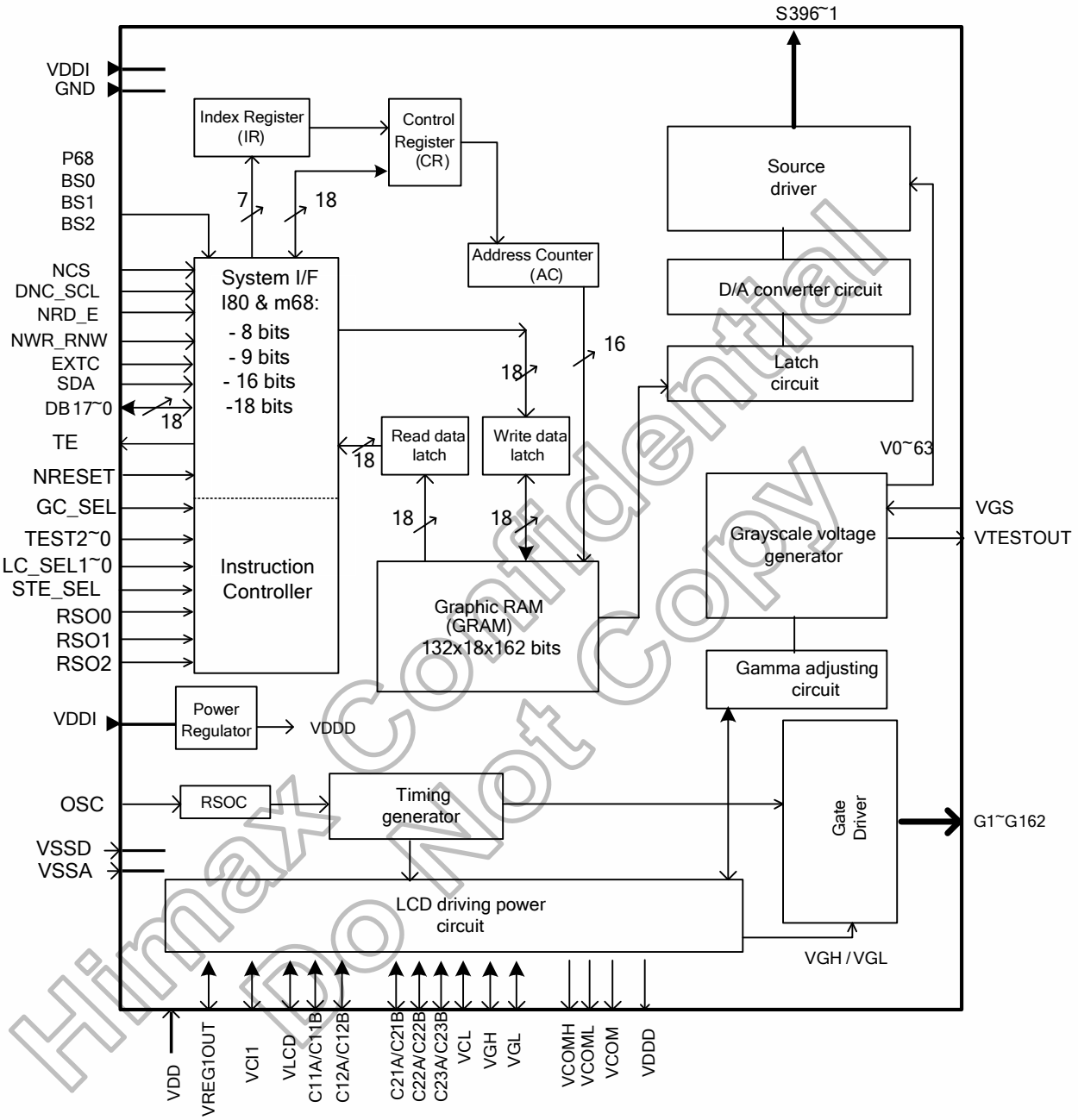
- Line inversion, frame inversion
- OTP to store initialization register setting
- Support default value for factory use

- Low-power consumption architecture supports:
  - Logic supply voltage range for VDDI to VSSD: 1.65 to 3.3V
  - Analog supply voltage range for VDD to VSSA: 2.3 to 3.3V
- Output voltage range:
  - VLCD = 4.0 to 5.5V
  - VCL = -2V to -3.3V
  - VREG1OUT = 3.0 to (VLCD-0.5V) (Source output reference voltage range)
  - VCOMH = 2.5V to 4.5V (Common electrode output high voltage)
  - VCOML = -2V to 0V (Common electrode output low voltage)
  - VGH = +9.0 to +16V (Positive Gate output voltage range)
  - VGL = -9.0 to -16V (Negative Gate output voltage range)

    (note: VDD – VCL ≦ 6V, VGH – VGL ≦ 32V)
- Low power consumption, suitable for battery operated systems
- Suitable for all brand LCM module
  - Command set:
    - 128RGB x 160-dot : DMIF-S43AP-J124 but support LUT table
    - 132RGB x 162-dot : DMIF-S45AP-J12
    - 128RGB x 160-dot : DMIF-S44AP-J12
    - 96RGB x 68-dot : DMIF-S31AL-J124 but support LUT table
  - Himax defined command set
- CMOS compatible inputs
- Optimized layout for COG assembly
- OTP memory to store initialization register settings
- Temperature range: -30 ~ 85℃

**Note:** (1) Blank display means: Normal White Display = White, Normal Black Display = Black.
(2) Timing and voltage level specification apply for the complete display module including LCD glass, Flex cable (FPC) and driver IC. Signal timings and levels are measured on the host interface connector.

# 3. Block Diagram



# 4. Pin Description

## 4.1 Pin Description

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Descriptions</th></tr>
<tr><td>P68, BS2,BS1,BS0</td><td>I</td><td>4</td><td>VSSD/ VDDI</td><td>Select the MPU interface mode as listed below
<table>
<tr><th>P68</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 80-system,</td><td>DB17-DB8:Unused, DB7-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system,</td><td>DB17-DB16:Unused, DB15-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit bus interface, 80-system,</td><td>DB17-DB9:Unused, DB8-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>18-bit bus interface, 80-system,</td><td>DB17-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 68-system,</td><td>DB17-DB8:Unused, DB7-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system,</td><td>DB17-DB16:Unused, DB15-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>9-bit bus interface, 68-system,</td><td>DB17-DB9:Unused, DB8-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>18-bit bus interface, 68-system,</td><td>DB17-DB0: Data</td></tr>
<tr><td>x</td><td>0</td><td>x</td><td>x</td><td>3W/4W Serial interface</td><td>DB17-DB0:Unused SDA: Data input/output</td></tr>
</table>
Note:Must be connected to VSSD or VDDI.(latch type)</td></tr>
<tr><td>SPI_SEL</td><td>I</td><td>1</td><td>MPU</td><td>Interface format select pin (latch type)
<table>
<tr><th>SPI_SEL</th><th>Serial Interface Format Selection</th></tr>
<tr><td>0</td><td>3W Serial Interface (default)</td></tr>
<tr><td>1</td><td>4W Serial Interface</td></tr>
</table></td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.<br>Low: chip can be accessed;<br>High: chip cannot be accessed.<br>Must be connected to VSSD or VDDI if not in use. (latch type)</td></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td>The signal for command or parameter select under parallel mode(i.e. Not serial interface):<br>Low: command. High: parameter.<br>When under serial interface, it servers as SCL.<br>If not used, let it open or connected to VDDI.. (latch type)</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a read signal and read data at the low level.<br>M68 system: 0: Read/Write disable, 1: Read/Write enable.<br>Fix it to VDDI or VSSD level when using serial interface. (latch type)</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a write signal and writes data at the rising edge.<br>M68 system: 0: Write, 1: Read.<br>If not used, let it open or connected to VDDI. (latch type)</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>Extended command set enable. (Only support Command-Parameter Interface mode)<br>Low (VSSD): extended command set is discarded<br>High (VDDI): extended command set is accepted<br>If not used, let it open or connected to VSSD.(weak pull low)</td></tr>
<tr><td>STE_SEL</td><td>I</td><td>1</td><td>MPU</td><td>This Pin is only valid for RSO[2:0]=3’b000.<br>There is a internal pull-high resistor on this pad. (latch type)<br>Low (VSSD): Scrolling function enable and TE lines is meet definition of S45AP (162 lines) → Support document of S45AP.<br>High (VDDI): Scrolling function disable and TE lines is meet definition of S43AP (160 lines) → Support document of S43AP.</td></tr>
<tr><td>GC_SEL</td><td>I</td><td>1</td><td>MPU</td><td>This signal is used to select gamma curve order. (latch type)<br>Low (VSSD): GC0(1.0), GC1(2.5), GC2(2.2), GC3(1.8)<br>High (VDDI): GC0(2.2), GC1(1.8), GC2(2.5), GC3(1.0)</td></tr>
<tr><td>LC_SEL1-0</td><td>I</td><td>2</td><td>MPU</td><td>The selection pins of different liquid crystal type. (latch type)
<table>
<tr><th>LC_SEL1</th><th>LC_SEL0</th><th>Different liquid crystal type Selection</th></tr>
<tr><td>0</td><td>0</td><td>LC type 1</td></tr>
<tr><td>0</td><td>1</td><td>LC type 2</td></tr>
<tr><td>1</td><td>0</td><td>LC type 3</td></tr>
</table></td></tr>
</table>

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | 1 | 1 | LC type 4 |

**Input Parts**

| Signals | I/O | Pin Number | Connected with | Description |
|---|---|---|---|---|
| **RSO0** | I | 1 | MPU | Resolution selection pins. RSO[2:0] is used for selecting resolution. If not used, please let it open. (latch type) |
| **RSO1** | I | 1 | MPU | |
| **RSO2** | I | 1 | MPU | |
| **NRESET** | I | 1 | MPU or reset circuit | Reset pin. Setting this pin low initializes the LSI. Must be reset after power is supplied.<br>Must be connected to VSSD or VDDB1. (latch type) |
| **VDC_ENB** | | | | Input pin to select the logice power. (latch type)<br>VSSD : Enable internal VDDD generator<br>VDDI : Disable internal VDDD generator, VDDD should connect to external 1.65v~1.95v power |
| **SS_PANEL** | I | 1 | MPU | Input pin to select the source driver scan direction on panel module. (1: VDDI, 0: VSSD) (latch type) |
| **GS_PANEL** | I | 1 | MPU | Input pin to select the Gate driver scan direction on panel module. (1: VDDI, 0: VSSD) (latch type) |
| **REV_PANEL** | I | 1 | MPU | Input pin to select the display reversion (1: VDDI, 0: VSSD) (latch type) |
| **BGR_PANEL** | I | 1 | MPU | Input pin to select the color mapping. (1: VDDI, 0: VSSD) (latch type) |
| **TEST1** | I | 1 | VSSD | A test pin. Make sure to fix it to the VSSD level.(weak pull low) |
| **TEST2** | I | 1 | VSSD | A test pin. Make sure to fix it to the VSSD level. (weak pull low) |
| **TEST3** | I | 1 | VSSD | A test pin. Make sure to fix it to the VSSD level. (weak pull low) |
| **OSC** | I | 1 | Open or Connect to VSSD | Oscillator input for test purpose.<br>If not used, please let it open or connected to VSSD. (weak pull low) |

**RSO0 / RSO1 / RSO2 — Resolution**

| RSO2 | RSO1 | RSO0 | Resolution |
|---|---|---|---|
| 0 | 0 | 0 | GRAM resolusion (Size): 132RGBX162<br>Display resolusion:<br>Type1 :132RGBx162 (S1~S396 and G1~G162)→S45AP<br>Type2 :128RGBx160 (S7~S390 and G2~G161)→S43AP |
| 0 | 0 | 1 | GRAM resolusion (Size): 128RGBx128<br>Display resolusion:<br>128RGBx128 (S7~S390 and G2~G129) |
| 0 | 1 | 0 | GRAM resolusion (Size): 120RGBx160<br>Display resolusion:<br>120RGBx160 (S7~S366, G2~G161) |
| 0 | 1 | 1 | GRAM resolusion (Size): 128RGBx160<br>Display resolusion:<br>128RGBx160 (S7~S390 and G2~G161) →S44AP |
| 1 | 0 | 0 | GRAM resolusion: 96RGBx68<br>Display resolusion:<br>96RGBx68 (S55~S342, G1~G68) |
| 1 | 0 | 1 | GRAM resolusion: 96RGBx64<br>Display resolusion:<br>96RGBx64 (S55~S342, G1~G64) |
| 1 | 1 | 0 | Setting disable |
| 1 | 1 | 1 | Setting disable |

**SS_PANEL**

| SS_Panel | Module source output direction | | | |
|---|---|---|---|---|
| | RSO[2:0] =3b'011 | RSO[2:0] =3b'010 | RSO[2:0] =3b'001 | RSO[2:0] =3b'000 |
| 0 | S7 -> S390 | S7 -> S366 | S7 -> S390 | S1 -> S396 |
| 1 | S390 -> S7 | S366 -> S7 | S390 -> S7 | S396 -> S1 |

**GS_PANEL**

| GS_Panel | Module Gate output direction | | | |
|---|---|---|---|---|
| | RSO[2:0] =3b'011 | RSO[2:0] =3b'010 | RSO[2:0] =3b'001 | RSO[2:0] =3b'000 |
| 0 | G2 -> G161 | G2 -> G161 | G2 -> G129 | G1 -> G162 |
| 1 | G161 -> G2 | G161 -> G2 | G129 -> G2 | G162 -> G1 |

**REV_PANEL**

| REV_Panel | Mapping data |
|---|---|
| 0 | "0" to minimum pixel voltage for normal white panel |
| 1 | "0" to maximum pixel voltage for normal black panel |

**BGR_PANEL**

| BGR_panel | Color mapping |
|---|---|
| 0 | R->G->B |
| 1 | B->G->R |

| Input Parts | | | | |
|---|---|---|---|---|
| **BURN** | I | 1 | MPU | Free Running mode (weak pull low)<br>If BURN=Hi, this can enable free running mode for burn in test.<br>The display data alternates between full black and full white independent of input data in free running mode. |

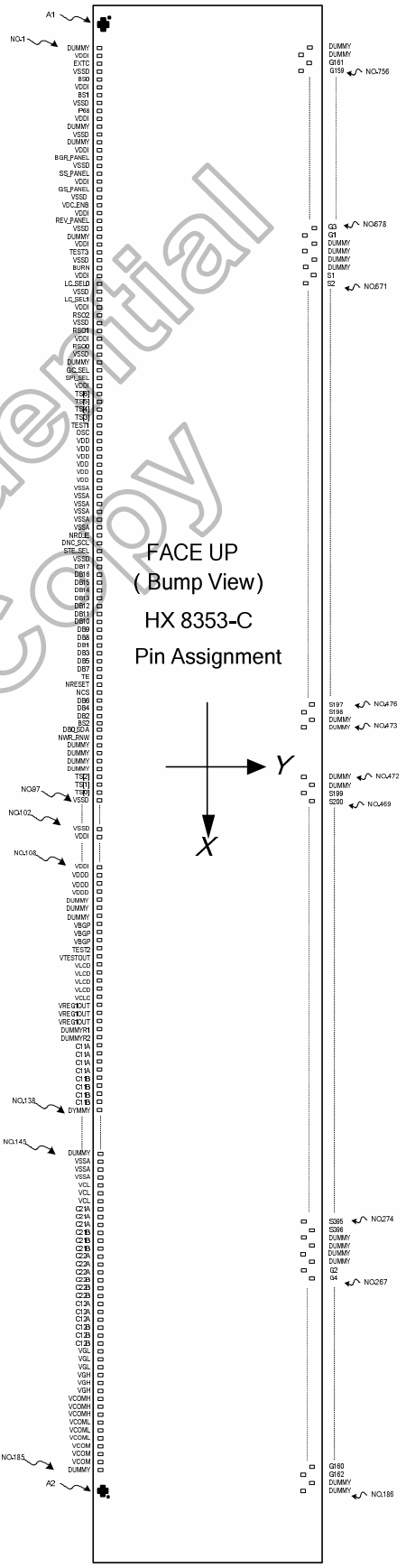
| Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| **S1~396** | O | 396 | LCD | Output voltages applied to the liquid crystal.<br>The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS=0, DATA IN THE ram address “0000” is output from S1.If SS=1, the same data in the ram address “0000” is output from S396.<br>S1,S4,S7,…display red (R),S2,S5,S8,…display green (G),and S3,S6,S9,…display blue(B) (SS=0, BGR=0). |
| **G1~162** | O | 160 | LCD | Output signals from gate lines.<br>VGH: the level to select the gate lines<br>VGL: the level not to select the gate lines |
| **VCOM** | O | 2 | TFT common electrode | The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel. |
| **VCOMH** | O | 1 | Stabilizing capacitor or open | Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation. |
| **VCOML** | O | 1 | Stabilizing capacitor or open | When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VCOML output stops and a capacitor for stabilization is not needed. |
| **VREG1OUT** | O | 1 | Stabilizing capacitor or open | Internal generated stable power for source driver unit .VREG1OUT = 3.0 ~ (VLCD – 0.5)V |
| **VLCD** | O | 1 | Stabilizing capacitor | An output from the step-up circuit1, of twice the VDD level.<br>Connect to a stabilizing capacitor 1uF between VLCD and VSSD.<br>VLCD=4.0 to 5.5V, Connect to VLCDC. |
| **VGL** | O | 1 | Stabilizing capacitor | An output from the step-up circuit2.or -3~-5 time the VDD level.<br>The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor 1uF between VSSD and VGL. Min. VGL = -16V |
| **VCL** | O | 1 | Stabilizing capacitor | A power supply for the VCOML level.<br>Connect to a stabilizing capacitor 1uF between VSSD and VCL.<br>VCL=-2V ~ -3.3V |
| **TE** | O | 1 | MPU or open | A frame start pulse output (amplitude: VDDI-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it |
| **VTESTOUT** | O | 1 | Open | A test pin. Disconnect it. |
| **VDDD** | O | 4 | Stabilizing capacitor | A stabilizing capacitor for logic power.<br>Connect with the capacitor 1uF. |
| **VREF** | 0 | 1 | Open | Reference voltage for power circuit<br>Please open this pads. |
| **VGH** | O | 1 | Stabilizing capacitor | An output from the step-up circuit2.or 4~6 time the VDD level.<br>The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor 1uF between VGH and VSSD. Place a Schottky barrier diode between VDD and VGH. (See “configuration of the power supply”).<br>Max. VGH=16V. |

| Input/Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| **C11A,C11B** | I/O | 2 | Step-up Capacitor | Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used. |
| **C12A, C12B C23A, C23B** | I/O | 2 | Open | Dummy pads. Please open this pin. |
| **C21A, C21B C22A, C22B** | I/O | 8 | Step-up Capacitor | Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them. |
| **DB0_SDA** | I/O | 1 | MPU | When it Operates in system interface mode, This pin (DB0) is used on bi-directional data bus.<br>For serial interface, this pin (SDA) is for serial data pin when operate on serial data transfer interface mode of Command-parameter Interface mode. Data would be latched on the rising edge of the SCL signal. Let it open if this pin is not used. |
| **DB0~17** | I/O | 18 | MPU | When Operates in system interface mode, it is used liked an 18-bit bi-directional data bus.<br>8-bit bus: use DB7-DB0<br>9-bit bus: use DB8-DB0<br>16-bit bus: use DB15-DB0<br>18-bit bus: use DB17-DB0<br>Let unused data pins open. |
| **DUMMY** | - | 16 | Open | Dummy pads. Disconnect them. |
| **DUMMYR1~R2** | - | 2 | - | Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. |

| Power Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| **VDDI** | P | 1 | Power supply | Power supply for interface pin. VDDI = 1.65 ~3.3 V. |
| **VSSD** | P | 1 | Power supply | Ground for the logic side. VSSD = 0V |
| **VSSA** | P | 1 | Power supply | Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise. |
| **VDD** | P | 1 | Power supply | A power supply for the analog circuit. VDD = 2.3 ~ 3.3V |

## 4.2 Pin assignment

- Chip size : 9900um x 670um
  Including : Seal-ring : 15um*2
  Scribe line : 40um*2
- Chip thickness : 300 um( typ.) / 400 um
- Pad coordinate : PAD center
- Coordinate Origin : Chip Center
- Au Bump Size
  Bump height tolerance +/- 3um
  Bump size tolerance:
  Output bump width: 16 +/- 2um
  Output bump length: 98 +/- 3um
  Input bump width: 35/40 +/- 3um
  Input bump length: 90 +/- 3um
- Au bump height : 15 um +/- 3um
- Numbers in the figure corresponds to pad coordinate numbers .
- Alignment Mark
  Arrangement : Two places
  A1: Coordinate ( X,Y ) = ( -4841 , -220 )
  A2: Coordinate ( X,Y ) = ( 4841 , -220 )



## 4.3 PAD Coordinate

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 1 | Dummy | -4750 | -231 | 35 X 90 | Input |
| 2 | IOVCC | -4700 | -231 | 35 X 90 | Input |
| 3 | EXTC | -4650 | -231 | 35 X 90 | Input |
| 4 | VSSD | -4600 | -231 | 35 X 90 | Input |
| 5 | BS0 | -4550 | -231 | 35 X 90 | Input |
| 6 | IOVCC | -4500 | -231 | 35 X 90 | Input |
| 7 | BS1 | -4450 | -231 | 35 X 90 | Input |
| 8 | VSSD | -4400 | -231 | 35 X 90 | Input |
| 9 | P68 | -4350 | -231 | 35 X 90 | Input |
| 10 | IOVCC | -4300 | -231 | 35 X 90 | Input |
| 11 | Dummy | -4250 | -231 | 35 X 90 | Input |
| 12 | VSSD | -4200 | -231 | 35 X 90 | Input |
| 13 | Dummy | -4150 | -231 | 35 X 90 | Input |
| 14 | IOVCC | -4100 | -231 | 35 X 90 | Input |
| 15 | BGR_PANE | -4050 | -231 | 35 X 90 | Input |
| 16 | VSSD | -4000 | -231 | 35 X 90 | Input |
| 17 | SS_PANEL | -3950 | -231 | 35 X 90 | Input |
| 18 | IOVCC | -3900 | -231 | 35 X 90 | Input |
| 19 | GS_PANEL | -3850 | -231 | 35 X 90 | Input |
| 20 | VSSD | -3800 | -231 | 35 X 90 | Input |
| 21 | VDCENB | -3750 | -231 | 35 X 90 | Input |
| 22 | IOVCC | -3700 | -231 | 35 X 90 | Input |
| 23 | REV_PANE | -3650 | -231 | 35 X 90 | Input |
| 24 | VSSD | -3600 | -231 | 35 X 90 | Input |
| 25 | Dummy | -3550 | -231 | 35 X 90 | Input |
| 26 | IOVCC | -3500 | -231 | 35 X 90 | Input |
| 27 | TEST3 | -3450 | -231 | 35 X 90 | Input |
| 28 | VSSD | -3400 | -231 | 35 X 90 | Input |
| 29 | BURN | -3350 | -231 | 35 X 90 | Input |
| 30 | IOVCC | -3300 | -231 | 35 X 90 | Input |
| 31 | LC_SEL0 | -3250 | -231 | 35 X 90 | Input |
| 32 | VSSD | -3200 | -231 | 35 X 90 | Input |
| 33 | LC_SEL1 | -3150 | -231 | 35 X 90 | Input |
| 34 | IOVCC | -3100 | -231 | 35 X 90 | Input |
| 35 | RSO2 | -3050 | -231 | 35 X 90 | Input |
| 36 | VSSD | -3000 | -231 | 35 X 90 | Input |
| 37 | RSO1 | -2950 | -231 | 35 X 90 | Input |
| 38 | IOVCC | -2900 | -231 | 35 X 90 | Input |
| 39 | RSO0 | -2850 | -231 | 35 X 90 | Input |
| 40 | VSSD | -2800 | -231 | 35 X 90 | Input |
| 41 | Dummy | -2750 | -231 | 35 X 90 | Input |
| 42 | GC_SEL | -2700 | -231 | 35 X 90 | Input |
| 43 | SPI_SEL | -2650 | -231 | 35 X 90 | Input |
| 44 | IOVCC | -2600 | -231 | 35 X 90 | Input |
| 45 | TS[6] | -2550 | -231 | 35 X 90 | Input |
| 46 | TS[5] | -2500 | -231 | 35 X 90 | Input |
| 47 | TS[4] | -2450 | -231 | 35 X 90 | Input |
| 48 | TS[3] | -2400 | -231 | 35 X 90 | Input |
| 49 | TEST1 | -2350 | -231 | 35 X 90 | Input |
| 50 | OSC | -2300 | -231 | 35 X 90 | Input |
| 51 | VCI | -2250 | -231 | 35 X 90 | Input |
| 52 | VCI | -2200 | -231 | 35 X 90 | Input |
| 53 | VCI | -2150 | -231 | 35 X 90 | Input |
| 54 | VCI | -2100 | -231 | 35 X 90 | Input |
| 55 | VCI | -2050 | -231 | 35 X 90 | Input |
| 56 | VCI | -2000 | -231 | 35 X 90 | Input |
| 57 | VSSA | -1950 | -231 | 35 X 90 | Input |
| 58 | VSSA | -1900 | -231 | 35 X 90 | Input |
| 59 | VSSA | -1850 | -231 | 35 X 90 | Input |
| 60 | VSSA | -1800 | -231 | 35 X 90 | Input |
| 61 | VSSA | -1750 | -231 | 35 X 90 | Input |
| 62 | VSSA | -1700 | -231 | 35 X 90 | Input |
| 63 | NRD_E | -1630 | -231 | 40 X 90 | Input |
| 64 | DNC_SCL | -1570 | -231 | 40 X 90 | Input |
| 65 | STE_SEL | -1510 | -231 | 40 X 90 | Input |
| 66 | VSSD | -1450 | -231 | 40 X 90 | Input |
| 67 | DB17 | -1390 | -231 | 40 X 90 | Input |
| 68 | DB16 | -1330 | -231 | 40 X 90 | Input |
| 69 | DB15 | -1270 | -231 | 40 X 90 | Input |
| 70 | DB14 | -1210 | -231 | 40 X 90 | Input |
| 71 | DB13 | -1150 | -231 | 40 X 90 | Input |
| 72 | DB12 | -1090 | -231 | 40 X 90 | Input |
| 73 | DB11 | -1030 | -231 | 40 X 90 | Input |
| 74 | DB10 | -970 | -231 | 40 X 90 | Input |
| 75 | DB9 | -910 | -231 | 40 X 90 | Input |
| 76 | DB8 | -850 | -231 | 40 X 90 | Input |
| 77 | DB1 | -790 | -231 | 40 X 90 | Input |
| 78 | DB3 | -730 | -231 | 40 X 90 | Input |
| 79 | DB5 | -670 | -231 | 40 X 90 | Input |
| 80 | DB7 | -610 | -231 | 40 X 90 | Input |
| 81 | TE | -550 | -231 | 40 X 90 | Input |
| 82 | NRESET | -490 | -231 | 40 X 90 | Input |
| 83 | NCS | -430 | -231 | 40 X 90 | Input |
| 84 | DB6 | -370 | -231 | 40 X 90 | Input |
| 85 | DB4 | -310 | -231 | 40 X 90 | Input |
| 86 | DB2 | -250 | -231 | 40 X 90 | Input |
| 87 | BS2 | -190 | -231 | 40 X 90 | Input |
| 88 | DB0_SDA | -130 | -231 | 40 X 90 | Input |
| 89 | NWR_RNW | -70 | -231 | 40 X 90 | Input |
| 90 | Dummy | 0 | -231 | 35 X 90 | Input |
| 91 | Dummy | 50 | -231 | 35 X 90 | Input |
| 92 | Dummy | 100 | -231 | 35 X 90 | Input |
| 93 | Dummy | 150 | -231 | 35 X 90 | Input |
| 94 | TS[2] | 200 | -231 | 35 X 90 | Input |
| 95 | TS[1] | 250 | -231 | 35 X 90 | Input |
| 96 | TS[0] | 300 | -231 | 35 X 90 | Input |
| 97 | VSSD | 350 | -231 | 35 X 90 | Input |
| 98 | VSSD | 400 | -231 | 35 X 90 | Input |
| 99 | VSSD | 450 | -231 | 35 X 90 | Input |
| 100 | VSSD | 500 | -231 | 35 X 90 | Input |
| 101 | VSSD | 550 | -231 | 35 X 90 | Input |
| 102 | VSSD | 600 | -231 | 35 X 90 | Input |
| 103 | IOVCC | 650 | -231 | 35 X 90 | Input |
| 104 | IOVCC | 700 | -231 | 35 X 90 | Input |
| 105 | IOVCC | 750 | -231 | 35 X 90 | Input |
| 106 | IOVCC | 800 | -231 | 35 X 90 | Input |
| 107 | IOVCC | 850 | -231 | 35 X 90 | Input |
| 108 | IOVCC | 900 | -231 | 35 X 90 | Input |
| 109 | VDDD | 950 | -231 | 35 X 90 | Output |
| 110 | VDDD | 1000 | -231 | 35 X 90 | Output |
| 111 | VDDD | 1050 | -231 | 35 X 90 | Output |
| 112 | Dummy | 1100 | -231 | 35 X 90 | Input |
| 113 | Dummy | 1150 | -231 | 35 X 90 | Input |
| 114 | Dummy | 1200 | -231 | 35 X 90 | Input |
| 115 | VREF | 1250 | -231 | 35 X 90 | Output |
| 116 | VREF | 1300 | -231 | 35 X 90 | Output |
| 117 | VREF | 1350 | -231 | 35 X 90 | Output |
| 118 | TEST2 | 1400 | -231 | 35 X 90 | Input |
| 119 | VTESTOUT | 1450 | -231 | 35 X 90 | Output |
| 120 | VLCD(DDVI | 1500 | -231 | 35 X 90 | Output |
| 121 | VLCD(DDVI | 1550 | -231 | 35 X 90 | Output |
| 122 | VLCD(DDVI | 1600 | -231 | 35 X 90 | Output |
| 123 | VLCD(DDVI | 1650 | -231 | 35 X 90 | Output |
| 124 | VLCD(DDVI | 1700 | -231 | 35 X 90 | Output |
| 125 | VREG1OUT | 1750 | -231 | 35 X 90 | Output |
| 126 | VREG1OUT | 1800 | -231 | 35 X 90 | Output |
| 127 | VREG1OUT | 1850 | -231 | 35 X 90 | Output |
| 128 | DUMMYR1 | 1900 | -231 | 35 X 90 | Input |
| 129 | DUMMYR2 | 1950 | -231 | 35 X 90 | Input |
| 130 | C11A | 2000 | -231 | 35 X 90 | Input |
| 131 | C11A | 2050 | -231 | 35 X 90 | Input |
| 132 | C11A | 2100 | -231 | 35 X 90 | Input |
| 133 | C11A | 2150 | -231 | 35 X 90 | Input |
| 134 | C11B | 2200 | -231 | 35 X 90 | Input |
| 135 | C11B | 2250 | -231 | 35 X 90 | Input |
| 136 | C11B | 2300 | -231 | 35 X 90 | Input |
| 137 | C11B | 2350 | -231 | 35 X 90 | Input |
| 138 | Dummy | 2400 | -231 | 35 X 90 | Input |
| 139 | Dummy | 2450 | -231 | 35 X 90 | Input |
| 140 | Dummy | 2500 | -231 | 35 X 90 | Input |
| 141 | Dummy | 2550 | -231 | 35 X 90 | Input |
| 142 | Dummy | 2600 | -231 | 35 X 90 | Input |
| 143 | Dummy | 2650 | -231 | 35 X 90 | Input |
| 144 | Dummy | 2700 | -231 | 35 X 90 | Input |
| 145 | Dummy | 2750 | -231 | 35 X 90 | Input |
| 146 | VSSA | 2800 | -231 | 35 X 90 | Input |
| 147 | VSSA | 2850 | -231 | 35 X 90 | Input |
| 148 | VSSA | 2900 | -231 | 35 X 90 | Input |
| 149 | VCL | 2950 | -231 | 35 X 90 | Output |
| 150 | VCL | 3000 | -231 | 35 X 90 | Output |
| 151 | VCL | 3050 | -231 | 35 X 90 | Output |
| 152 | C21A | 3100 | -231 | 35 X 90 | Input |
| 153 | C21A | 3150 | -231 | 35 X 90 | Input |
| 154 | C21A | 3200 | -231 | 35 X 90 | Input |
| 155 | C21B | 3250 | -231 | 35 X 90 | Input |
| 156 | C21B | 3300 | -231 | 35 X 90 | Input |
| 157 | C21B | 3350 | -231 | 35 X 90 | Input |
| 158 | C22A | 3400 | -231 | 35 X 90 | Input |
| 159 | C22A | 3450 | -231 | 35 X 90 | Input |
| 160 | C22A | 3500 | -231 | 35 X 90 | Input |
| 161 | C22B | 3550 | -231 | 35 X 90 | Input |
| 162 | C22B | 3600 | -231 | 35 X 90 | Input |
| 163 | C22B | 3650 | -231 | 35 X 90 | Input |
| 164 | C12A | 3700 | -231 | 35 X 90 | Input |
| 165 | C12A | 3750 | -231 | 35 X 90 | Input |
| 166 | C12A | 3800 | -231 | 35 X 90 | Input |
| 167 | C12B | 3850 | -231 | 35 X 90 | Input |
| 168 | C12B | 3900 | -231 | 35 X 90 | Input |
| 169 | C12B | 3950 | -231 | 35 X 90 | Input |
| 170 | VGL | 4000 | -231 | 35 X 90 | Output |
| 171 | VGL | 4050 | -231 | 35 X 90 | Output |
| 172 | VGL | 4100 | -231 | 35 X 90 | Output |
| 173 | VGH | 4150 | -231 | 35 X 90 | Output |
| 174 | VGH | 4200 | -231 | 35 X 90 | Output |
| 175 | VGH | 4250 | -231 | 35 X 90 | Output |
| 176 | VCOMH | 4300 | -231 | 35 X 90 | Output |
| 177 | VCOMH | 4350 | -231 | 35 X 90 | Output |
| 178 | VCOMH | 4400 | -231 | 35 X 90 | Output |
| 179 | VCOML | 4450 | -231 | 35 X 90 | Output |
| 180 | VCOML | 4500 | -231 | 35 X 90 | Output |
| 181 | VCOML | 4550 | -231 | 35 X 90 | Output |
| 182 | VCOM | 4600 | -231 | 35 X 90 | Output |
| 183 | VCOM | 4650 | -231 | 35 X 90 | Output |
| 184 | VCOM | 4700 | -231 | 35 X 90 | Output |
| 185 | DUMMY | 4750 | -231 | 35 X 90 | Output |
| 186 | DUMMY | 4772 | 110 | 16 X 98 | Output |
| 187 | DUMMY | 4756 | 227 | 16 X 98 | Output |
| 188 | G162 | 4740 | 110 | 16 X 98 | Output |
| 189 | G160 | 4724 | 227 | 16 X 98 | Output |
| 190 | G158 | 4708 | 110 | 16 X 98 | Output |
| 191 | G156 | 4692 | 227 | 16 X 98 | Output |
| 192 | G154 | 4676 | 110 | 16 X 98 | Output |
| 193 | G152 | 4660 | 227 | 16 X 98 | Output |
| 194 | G150 | 4644 | 110 | 16 X 98 | Output |
| 195 | G148 | 4628 | 227 | 16 X 98 | Output |
| 196 | G146 | 4612 | 110 | 16 X 98 | Output |
| 197 | G144 | 4596 | 227 | 16 X 98 | Output |
| 198 | G142 | 4580 | 110 | 16 X 98 | Output |
| 199 | G140 | 4564 | 227 | 16 X 98 | Output |
| 200 | G138 | 4548 | 110 | 16 X 98 | Output |
| 201 | G136 | 4532 | 227 | 16 X 98 | Output |
| 202 | G134 | 4516 | 110 | 16 X 98 | Output |
| 203 | G132 | 4500 | 227 | 16 X 98 | Output |
| 204 | G130 | 4484 | 110 | 16 X 98 | Output |
| 205 | G128 | 4468 | 227 | 16 X 98 | Output |
| 206 | G126 | 4452 | 110 | 16 X 98 | Output |
| 207 | G124 | 4436 | 227 | 16 X 98 | Output |
| 208 | G122 | 4420 | 110 | 16 X 98 | Output |
| 209 | G120 | 4404 | 227 | 16 X 98 | Output |
| 210 | G118 | 4388 | 110 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 211 | G116 | 4372 | 227 | 16 X 98 | Output |
| 212 | G114 | 4356 | 110 | 16 X 98 | Output |
| 213 | G112 | 4340 | 227 | 16 X 98 | Output |
| 214 | G110 | 4324 | 110 | 16 X 98 | Output |
| 215 | G108 | 4308 | 227 | 16 X 98 | Output |
| 216 | G106 | 4292 | 110 | 16 X 98 | Output |
| 217 | G104 | 4276 | 227 | 16 X 98 | Output |
| 218 | G102 | 4260 | 110 | 16 X 98 | Output |
| 219 | G100 | 4244 | 227 | 16 X 98 | Output |
| 220 | G98 | 4228 | 110 | 16 X 98 | Output |
| 221 | G96 | 4212 | 227 | 16 X 98 | Output |
| 222 | G94 | 4196 | 110 | 16 X 98 | Output |
| 223 | G92 | 4180 | 227 | 16 X 98 | Output |
| 224 | G90 | 4164 | 110 | 16 X 98 | Output |
| 225 | G88 | 4148 | 227 | 16 X 98 | Output |
| 226 | G86 | 4132 | 110 | 16 X 98 | Output |
| 227 | G84 | 4116 | 227 | 16 X 98 | Output |
| 228 | G82 | 4100 | 110 | 16 X 98 | Output |
| 229 | G80 | 4084 | 227 | 16 X 98 | Output |
| 230 | G78 | 4068 | 110 | 16 X 98 | Output |
| 231 | G76 | 4052 | 227 | 16 X 98 | Output |
| 232 | G74 | 4036 | 110 | 16 X 98 | Output |
| 233 | G72 | 4020 | 227 | 16 X 98 | Output |
| 234 | G70 | 4004 | 110 | 16 X 98 | Output |
| 235 | G68 | 3988 | 227 | 16 X 98 | Output |
| 236 | G66 | 3972 | 110 | 16 X 98 | Output |
| 237 | G64 | 3956 | 227 | 16 X 98 | Output |
| 238 | G62 | 3940 | 110 | 16 X 98 | Output |
| 239 | G60 | 3924 | 227 | 16 X 98 | Output |
| 240 | G58 | 3908 | 110 | 16 X 98 | Output |
| 241 | G56 | 3892 | 227 | 16 X 98 | Output |
| 242 | G54 | 3876 | 110 | 16 X 98 | Output |
| 243 | G52 | 3860 | 227 | 16 X 98 | Output |
| 244 | G50 | 3844 | 110 | 16 X 98 | Output |
| 245 | G48 | 3828 | 227 | 16 X 98 | Output |
| 246 | G46 | 3812 | 110 | 16 X 98 | Output |
| 247 | G44 | 3796 | 227 | 16 X 98 | Output |
| 248 | G42 | 3780 | 110 | 16 X 98 | Output |
| 249 | G40 | 3764 | 227 | 16 X 98 | Output |
| 250 | G38 | 3748 | 110 | 16 X 98 | Output |
| 251 | G36 | 3732 | 227 | 16 X 98 | Output |
| 252 | G34 | 3716 | 110 | 16 X 98 | Output |
| 253 | G32 | 3700 | 227 | 16 X 98 | Output |
| 254 | G30 | 3684 | 110 | 16 X 98 | Output |
| 255 | G28 | 3668 | 227 | 16 X 98 | Output |
| 256 | G26 | 3652 | 110 | 16 X 98 | Output |
| 257 | G24 | 3636 | 227 | 16 X 98 | Output |
| 258 | G22 | 3620 | 110 | 16 X 98 | Output |
| 259 | G20 | 3604 | 227 | 16 X 98 | Output |
| 260 | G18 | 3588 | 110 | 16 X 98 | Output |
| 261 | G16 | 3572 | 227 | 16 X 98 | Output |
| 262 | G14 | 3556 | 110 | 16 X 98 | Output |
| 263 | G12 | 3540 | 227 | 16 X 98 | Output |
| 264 | G10 | 3524 | 110 | 16 X 98 | Output |
| 265 | G8 | 3508 | 227 | 16 X 98 | Output |
| 266 | G6 | 3492 | 110 | 16 X 98 | Output |
| 267 | G4 | 3476 | 227 | 16 X 98 | Output |
| 268 | G2 | 3460 | 110 | 16 X 98 | Output |
| 269 | DUMMY | 3444 | 227 | 16 X 98 | Output |
| 270 | DUMMY | 3428 | 110 | 16 X 98 | Output |
| 271 | DUMMY | 3412 | 227 | 16 X 98 | Output |
| 272 | DUMMY | 3396 | 110 | 16 X 98 | Output |
| 273 | S396 | 3380 | 227 | 16 X 98 | Output |
| 274 | S395 | 3364 | 110 | 16 X 98 | Output |
| 275 | S394 | 3348 | 227 | 16 X 98 | Output |
| 276 | S393 | 3332 | 110 | 16 X 98 | Output |
| 277 | S392 | 3316 | 227 | 16 X 98 | Output |
| 278 | S391 | 3300 | 110 | 16 X 98 | Output |
| 279 | S390 | 3284 | 227 | 16 X 98 | Output |
| 280 | S389 | 3268 | 110 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 281 | S388 | 3252 | 227 | 16 X 98 | Output |
| 282 | S387 | 3236 | 110 | 16 X 98 | Output |
| 283 | S386 | 3220 | 227 | 16 X 98 | Output |
| 284 | S385 | 3204 | 110 | 16 X 98 | Output |
| 285 | S384 | 3188 | 227 | 16 X 98 | Output |
| 286 | S383 | 3172 | 110 | 16 X 98 | Output |
| 287 | S382 | 3156 | 227 | 16 X 98 | Output |
| 288 | S381 | 3140 | 110 | 16 X 98 | Output |
| 289 | S380 | 3124 | 227 | 16 X 98 | Output |
| 290 | S379 | 3108 | 110 | 16 X 98 | Output |
| 291 | S378 | 3092 | 227 | 16 X 98 | Output |
| 292 | S377 | 3076 | 110 | 16 X 98 | Output |
| 293 | S376 | 3060 | 227 | 16 X 98 | Output |
| 294 | S375 | 3044 | 110 | 16 X 98 | Output |
| 295 | S374 | 3028 | 227 | 16 X 98 | Output |
| 296 | S373 | 3012 | 110 | 16 X 98 | Output |
| 297 | S372 | 2996 | 227 | 16 X 98 | Output |
| 298 | S371 | 2980 | 110 | 16 X 98 | Output |
| 299 | S370 | 2964 | 227 | 16 X 98 | Output |
| 300 | S369 | 2948 | 110 | 16 X 98 | Output |
| 301 | S368 | 2932 | 227 | 16 X 98 | Output |
| 302 | S367 | 2916 | 110 | 16 X 98 | Output |
| 303 | S366 | 2900 | 227 | 16 X 98 | Output |
| 304 | S365 | 2884 | 110 | 16 X 98 | Output |
| 305 | S364 | 2868 | 227 | 16 X 98 | Output |
| 306 | S363 | 2852 | 110 | 16 X 98 | Output |
| 307 | S362 | 2836 | 227 | 16 X 98 | Output |
| 308 | S361 | 2820 | 110 | 16 X 98 | Output |
| 309 | S360 | 2804 | 227 | 16 X 98 | Output |
| 310 | S359 | 2788 | 110 | 16 X 98 | Output |
| 311 | S358 | 2772 | 227 | 16 X 98 | Output |
| 312 | S357 | 2756 | 110 | 16 X 98 | Output |
| 313 | S356 | 2740 | 227 | 16 X 98 | Output |
| 314 | S355 | 2724 | 110 | 16 X 98 | Output |
| 315 | S354 | 2708 | 227 | 16 X 98 | Output |
| 316 | S353 | 2692 | 110 | 16 X 98 | Output |
| 317 | S352 | 2676 | 227 | 16 X 98 | Output |
| 318 | S351 | 2660 | 110 | 16 X 98 | Output |
| 319 | S350 | 2644 | 227 | 16 X 98 | Output |
| 320 | S349 | 2628 | 110 | 16 X 98 | Output |
| 321 | S348 | 2612 | 227 | 16 X 98 | Output |
| 322 | S347 | 2596 | 110 | 16 X 98 | Output |
| 323 | S346 | 2580 | 227 | 16 X 98 | Output |
| 324 | S345 | 2564 | 110 | 16 X 98 | Output |
| 325 | S344 | 2548 | 227 | 16 X 98 | Output |
| 326 | S343 | 2532 | 110 | 16 X 98 | Output |
| 327 | S342 | 2516 | 227 | 16 X 98 | Output |
| 328 | S341 | 2500 | 110 | 16 X 98 | Output |
| 329 | S340 | 2484 | 227 | 16 X 98 | Output |
| 330 | S339 | 2468 | 110 | 16 X 98 | Output |
| 331 | S338 | 2452 | 227 | 16 X 98 | Output |
| 332 | S337 | 2436 | 110 | 16 X 98 | Output |
| 333 | S336 | 2420 | 227 | 16 X 98 | Output |
| 334 | S335 | 2404 | 110 | 16 X 98 | Output |
| 335 | S334 | 2388 | 227 | 16 X 98 | Output |
| 336 | S333 | 2372 | 110 | 16 X 98 | Output |
| 337 | S332 | 2356 | 227 | 16 X 98 | Output |
| 338 | S331 | 2340 | 110 | 16 X 98 | Output |
| 339 | S330 | 2324 | 227 | 16 X 98 | Output |
| 340 | S329 | 2308 | 110 | 16 X 98 | Output |
| 341 | S328 | 2292 | 227 | 16 X 98 | Output |
| 342 | S327 | 2276 | 110 | 16 X 98 | Output |
| 343 | S326 | 2260 | 227 | 16 X 98 | Output |
| 344 | S325 | 2244 | 110 | 16 X 98 | Output |
| 345 | S324 | 2228 | 227 | 16 X 98 | Output |
| 346 | S323 | 2212 | 110 | 16 X 98 | Output |
| 347 | S322 | 2196 | 227 | 16 X 98 | Output |
| 348 | S321 | 2180 | 110 | 16 X 98 | Output |
| 349 | S320 | 2164 | 227 | 16 X 98 | Output |
| 350 | S319 | 2148 | 110 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 351 | S318 | 2132 | 227 | 16 X 98 | Output |
| 352 | S317 | 2116 | 110 | 16 X 98 | Output |
| 353 | S316 | 2100 | 227 | 16 X 98 | Output |
| 354 | S315 | 2084 | 110 | 16 X 98 | Output |
| 355 | S314 | 2068 | 227 | 16 X 98 | Output |
| 356 | S313 | 2052 | 110 | 16 X 98 | Output |
| 357 | S312 | 2036 | 227 | 16 X 98 | Output |
| 358 | S311 | 2020 | 110 | 16 X 98 | Output |
| 359 | S310 | 2004 | 227 | 16 X 98 | Output |
| 360 | S309 | 1988 | 110 | 16 X 98 | Output |
| 361 | S308 | 1972 | 227 | 16 X 98 | Output |
| 362 | S307 | 1956 | 110 | 16 X 98 | Output |
| 363 | S306 | 1940 | 227 | 16 X 98 | Output |
| 364 | S305 | 1924 | 110 | 16 X 98 | Output |
| 365 | S304 | 1908 | 227 | 16 X 98 | Output |
| 366 | S303 | 1892 | 110 | 16 X 98 | Output |
| 367 | S302 | 1876 | 227 | 16 X 98 | Output |
| 368 | S301 | 1860 | 110 | 16 X 98 | Output |
| 369 | S300 | 1844 | 227 | 16 X 98 | Output |
| 370 | S299 | 1828 | 110 | 16 X 98 | Output |
| 371 | S298 | 1812 | 227 | 16 X 98 | Output |
| 372 | S297 | 1796 | 110 | 16 X 98 | Output |
| 373 | S296 | 1780 | 227 | 16 X 98 | Output |
| 374 | S295 | 1764 | 110 | 16 X 98 | Output |
| 375 | S294 | 1748 | 227 | 16 X 98 | Output |
| 376 | S293 | 1732 | 110 | 16 X 98 | Output |
| 377 | S292 | 1716 | 227 | 16 X 98 | Output |
| 378 | S291 | 1700 | 110 | 16 X 98 | Output |
| 379 | S290 | 1684 | 227 | 16 X 98 | Output |
| 380 | S289 | 1668 | 110 | 16 X 98 | Output |
| 381 | S288 | 1652 | 227 | 16 X 98 | Output |
| 382 | S287 | 1636 | 110 | 16 X 98 | Output |
| 383 | S286 | 1620 | 227 | 16 X 98 | Output |
| 384 | S285 | 1604 | 110 | 16 X 98 | Output |
| 385 | S284 | 1588 | 227 | 16 X 98 | Output |
| 386 | S283 | 1572 | 110 | 16 X 98 | Output |
| 387 | S282 | 1556 | 227 | 16 X 98 | Output |
| 388 | S281 | 1540 | 110 | 16 X 98 | Output |
| 389 | S280 | 1524 | 227 | 16 X 98 | Output |
| 390 | S279 | 1508 | 110 | 16 X 98 | Output |
| 391 | S278 | 1492 | 227 | 16 X 98 | Output |
| 392 | S277 | 1476 | 110 | 16 X 98 | Output |
| 393 | S276 | 1460 | 227 | 16 X 98 | Output |
| 394 | S275 | 1444 | 110 | 16 X 98 | Output |
| 395 | S274 | 1428 | 227 | 16 X 98 | Output |
| 396 | S273 | 1412 | 110 | 16 X 98 | Output |
| 397 | S272 | 1396 | 227 | 16 X 98 | Output |
| 398 | S271 | 1380 | 110 | 16 X 98 | Output |
| 399 | S270 | 1364 | 227 | 16 X 98 | Output |
| 400 | S269 | 1348 | 110 | 16 X 98 | Output |
| 401 | S268 | 1332 | 227 | 16 X 98 | Output |
| 402 | S267 | 1316 | 110 | 16 X 98 | Output |
| 403 | S266 | 1300 | 227 | 16 X 98 | Output |
| 404 | S265 | 1284 | 110 | 16 X 98 | Output |
| 405 | S264 | 1268 | 227 | 16 X 98 | Output |
| 406 | S263 | 1252 | 110 | 16 X 98 | Output |
| 407 | S262 | 1236 | 227 | 16 X 98 | Output |
| 408 | S261 | 1220 | 110 | 16 X 98 | Output |
| 409 | S260 | 1204 | 227 | 16 X 98 | Output |
| 410 | S259 | 1188 | 110 | 16 X 98 | Output |
| 411 | S258 | 1172 | 227 | 16 X 98 | Output |
| 412 | S257 | 1156 | 110 | 16 X 98 | Output |
| 413 | S256 | 1140 | 227 | 16 X 98 | Output |
| 414 | S255 | 1124 | 110 | 16 X 98 | Output |
| 415 | S254 | 1108 | 227 | 16 X 98 | Output |
| 416 | S253 | 1092 | 110 | 16 X 98 | Output |
| 417 | S252 | 1076 | 227 | 16 X 98 | Output |
| 418 | S251 | 1060 | 110 | 16 X 98 | Output |
| 419 | S250 | 1044 | 227 | 16 X 98 | Output |
| 420 | S249 | 1028 | 110 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 421 | S248 | 1012 | 227 | 16 X 98 | Output |
| 422 | S247 | 996 | 110 | 16 X 98 | Output |
| 423 | S246 | 980 | 227 | 16 X 98 | Output |
| 424 | S245 | 964 | 110 | 16 X 98 | Output |
| 425 | S244 | 948 | 227 | 16 X 98 | Output |
| 426 | S243 | 932 | 110 | 16 X 98 | Output |
| 427 | S242 | 916 | 227 | 16 X 98 | Output |
| 428 | S241 | 900 | 110 | 16 X 98 | Output |
| 429 | S240 | 884 | 227 | 16 X 98 | Output |
| 430 | S239 | 868 | 110 | 16 X 98 | Output |
| 431 | S238 | 852 | 227 | 16 X 98 | Output |
| 432 | S237 | 836 | 110 | 16 X 98 | Output |
| 433 | S236 | 820 | 227 | 16 X 98 | Output |
| 434 | S235 | 804 | 110 | 16 X 98 | Output |
| 435 | S234 | 788 | 227 | 16 X 98 | Output |
| 436 | S233 | 772 | 110 | 16 X 98 | Output |
| 437 | S232 | 756 | 227 | 16 X 98 | Output |
| 438 | S231 | 740 | 110 | 16 X 98 | Output |
| 439 | S230 | 724 | 227 | 16 X 98 | Output |
| 440 | S229 | 708 | 110 | 16 X 98 | Output |
| 441 | S228 | 692 | 227 | 16 X 98 | Output |
| 442 | S227 | 676 | 110 | 16 X 98 | Output |
| 443 | S226 | 660 | 227 | 16 X 98 | Output |
| 444 | S225 | 644 | 110 | 16 X 98 | Output |
| 445 | S224 | 628 | 227 | 16 X 98 | Output |
| 446 | S223 | 612 | 110 | 16 X 98 | Output |
| 447 | S222 | 596 | 227 | 16 X 98 | Output |
| 448 | S221 | 580 | 110 | 16 X 98 | Output |
| 449 | S220 | 564 | 227 | 16 X 98 | Output |
| 450 | S219 | 548 | 110 | 16 X 98 | Output |
| 451 | S218 | 532 | 227 | 16 X 98 | Output |
| 452 | S217 | 516 | 110 | 16 X 98 | Output |
| 453 | S216 | 500 | 227 | 16 X 98 | Output |
| 454 | S215 | 484 | 110 | 16 X 98 | Output |
| 455 | S214 | 468 | 227 | 16 X 98 | Output |
| 456 | S213 | 452 | 110 | 16 X 98 | Output |
| 457 | S212 | 436 | 227 | 16 X 98 | Output |
| 458 | S211 | 420 | 110 | 16 X 98 | Output |
| 459 | S210 | 404 | 227 | 16 X 98 | Output |
| 460 | S209 | 388 | 110 | 16 X 98 | Output |
| 461 | S208 | 372 | 227 | 16 X 98 | Output |
| 462 | S207 | 356 | 110 | 16 X 98 | Output |
| 463 | S206 | 340 | 227 | 16 X 98 | Output |
| 464 | S205 | 324 | 110 | 16 X 98 | Output |
| 465 | S204 | 308 | 227 | 16 X 98 | Output |
| 466 | S203 | 292 | 110 | 16 X 98 | Output |
| 467 | S202 | 276 | 227 | 16 X 98 | Output |
| 468 | S201 | 260 | 110 | 16 X 98 | Output |
| 469 | S200 | 244 | 227 | 16 X 98 | Output |
| 470 | S199 | 228 | 110 | 16 X 98 | Output |
| 471 | DUMMY | 212 | 227 | 16 X 98 | Output |
| 472 | DUMMY | 196 | 110 | 16 X 98 | Output |
| 473 | DUMMY | -196 | 110 | 16 X 98 | Output |
| 474 | DUMMY | -212 | 227 | 16 X 98 | Output |
| 475 | S198 | -228 | 110 | 16 X 98 | Output |
| 476 | S197 | -244 | 227 | 16 X 98 | Output |
| 477 | S196 | -260 | 110 | 16 X 98 | Output |
| 478 | S195 | -276 | 227 | 16 X 98 | Output |
| 479 | S194 | -292 | 110 | 16 X 98 | Output |
| 480 | S193 | -308 | 227 | 16 X 98 | Output |
| 481 | S192 | -324 | 110 | 16 X 98 | Output |
| 482 | S191 | -340 | 227 | 16 X 98 | Output |
| 483 | S190 | -356 | 110 | 16 X 98 | Output |
| 484 | S189 | -372 | 227 | 16 X 98 | Output |
| 485 | S188 | -388 | 110 | 16 X 98 | Output |
| 486 | S187 | -404 | 227 | 16 X 98 | Output |
| 487 | S186 | -420 | 110 | 16 X 98 | Output |
| 488 | S185 | -436 | 227 | 16 X 98 | Output |
| 489 | S184 | -452 | 110 | 16 X 98 | Output |
| 490 | S183 | -468 | 227 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 491 | S182 | -484 | 110 | 16 X 98 | Output |
| 492 | S181 | -500 | 227 | 16 X 98 | Output |
| 493 | S180 | -516 | 110 | 16 X 98 | Output |
| 494 | S179 | -532 | 227 | 16 X 98 | Output |
| 495 | S178 | -548 | 110 | 16 X 98 | Output |
| 496 | S177 | -564 | 227 | 16 X 98 | Output |
| 497 | S176 | -580 | 110 | 16 X 98 | Output |
| 498 | S175 | -596 | 227 | 16 X 98 | Output |
| 499 | S174 | -612 | 110 | 16 X 98 | Output |
| 500 | S173 | -628 | 227 | 16 X 98 | Output |
| 501 | S172 | -644 | 110 | 16 X 98 | Output |
| 502 | S171 | -660 | 227 | 16 X 98 | Output |
| 503 | S170 | -676 | 110 | 16 X 98 | Output |
| 504 | S169 | -692 | 227 | 16 X 98 | Output |
| 505 | S168 | -708 | 110 | 16 X 98 | Output |
| 506 | S167 | -724 | 227 | 16 X 98 | Output |
| 507 | S166 | -740 | 110 | 16 X 98 | Output |
| 508 | S165 | -756 | 227 | 16 X 98 | Output |
| 509 | S164 | -772 | 110 | 16 X 98 | Output |
| 510 | S163 | -788 | 227 | 16 X 98 | Output |
| 511 | S162 | -804 | 110 | 16 X 98 | Output |
| 512 | S161 | -820 | 227 | 16 X 98 | Output |
| 513 | S160 | -836 | 110 | 16 X 98 | Output |
| 514 | S159 | -852 | 227 | 16 X 98 | Output |
| 515 | S158 | -868 | 110 | 16 X 98 | Output |
| 516 | S157 | -884 | 227 | 16 X 98 | Output |
| 517 | S156 | -900 | 110 | 16 X 98 | Output |
| 518 | S155 | -916 | 227 | 16 X 98 | Output |
| 519 | S154 | -932 | 110 | 16 X 98 | Output |
| 520 | S153 | -948 | 227 | 16 X 98 | Output |
| 521 | S152 | -964 | 110 | 16 X 98 | Output |
| 522 | S151 | -980 | 227 | 16 X 98 | Output |
| 523 | S150 | -996 | 110 | 16 X 98 | Output |
| 524 | S149 | -1012 | 227 | 16 X 98 | Output |
| 525 | S148 | -1028 | 110 | 16 X 98 | Output |
| 526 | S147 | -1044 | 227 | 16 X 98 | Output |
| 527 | S146 | -1060 | 110 | 16 X 98 | Output |
| 528 | S145 | -1076 | 227 | 16 X 98 | Output |
| 529 | S144 | -1092 | 110 | 16 X 98 | Output |
| 530 | S143 | -1108 | 227 | 16 X 98 | Output |
| 531 | S142 | -1124 | 110 | 16 X 98 | Output |
| 532 | S141 | -1140 | 227 | 16 X 98 | Output |
| 533 | S140 | -1156 | 110 | 16 X 98 | Output |
| 534 | S139 | -1172 | 227 | 16 X 98 | Output |
| 535 | S138 | -1188 | 110 | 16 X 98 | Output |
| 536 | S137 | -1204 | 227 | 16 X 98 | Output |
| 537 | S136 | -1220 | 110 | 16 X 98 | Output |
| 538 | S135 | -1236 | 227 | 16 X 98 | Output |
| 539 | S134 | -1252 | 110 | 16 X 98 | Output |
| 540 | S133 | -1268 | 227 | 16 X 98 | Output |
| 541 | S132 | -1284 | 110 | 16 X 98 | Output |
| 542 | S131 | -1300 | 227 | 16 X 98 | Output |
| 543 | S130 | -1316 | 110 | 16 X 98 | Output |
| 544 | S129 | -1332 | 227 | 16 X 98 | Output |
| 545 | S128 | -1348 | 110 | 16 X 98 | Output |
| 546 | S127 | -1364 | 227 | 16 X 98 | Output |
| 547 | S126 | -1380 | 110 | 16 X 98 | Output |
| 548 | S125 | -1396 | 227 | 16 X 98 | Output |
| 549 | S124 | -1412 | 110 | 16 X 98 | Output |
| 550 | S123 | -1428 | 227 | 16 X 98 | Output |
| 551 | S122 | -1444 | 110 | 16 X 98 | Output |
| 552 | S121 | -1460 | 227 | 16 X 98 | Output |
| 553 | S120 | -1476 | 110 | 16 X 98 | Output |
| 554 | S119 | -1492 | 227 | 16 X 98 | Output |
| 555 | S118 | -1508 | 110 | 16 X 98 | Output |
| 556 | S117 | -1524 | 227 | 16 X 98 | Output |
| 557 | S116 | -1540 | 110 | 16 X 98 | Output |
| 558 | S115 | -1556 | 227 | 16 X 98 | Output |
| 559 | S114 | -1572 | 110 | 16 X 98 | Output |
| 560 | S113 | -1588 | 227 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 561 | S112 | -1604 | 110 | 16 X 98 | Output |
| 562 | S111 | -1620 | 227 | 16 X 98 | Output |
| 563 | S110 | -1636 | 110 | 16 X 98 | Output |
| 564 | S109 | -1652 | 227 | 16 X 98 | Output |
| 565 | S108 | -1668 | 110 | 16 X 98 | Output |
| 566 | S107 | -1684 | 227 | 16 X 98 | Output |
| 567 | S106 | -1700 | 110 | 16 X 98 | Output |
| 568 | S105 | -1716 | 227 | 16 X 98 | Output |
| 569 | S104 | -1732 | 110 | 16 X 98 | Output |
| 570 | S103 | -1748 | 227 | 16 X 98 | Output |
| 571 | S102 | -1764 | 110 | 16 X 98 | Output |
| 572 | S101 | -1780 | 227 | 16 X 98 | Output |
| 573 | S100 | -1796 | 110 | 16 X 98 | Output |
| 574 | S99 | -1812 | 227 | 16 X 98 | Output |
| 575 | S98 | -1828 | 110 | 16 X 98 | Output |
| 576 | S97 | -1844 | 227 | 16 X 98 | Output |
| 577 | S96 | -1860 | 110 | 16 X 98 | Output |
| 578 | S95 | -1876 | 227 | 16 X 98 | Output |
| 579 | S94 | -1892 | 110 | 16 X 98 | Output |
| 580 | S93 | -1908 | 227 | 16 X 98 | Output |
| 581 | S92 | -1924 | 110 | 16 X 98 | Output |
| 582 | S91 | -1940 | 227 | 16 X 98 | Output |
| 583 | S90 | -1956 | 110 | 16 X 98 | Output |
| 584 | S89 | -1972 | 227 | 16 X 98 | Output |
| 585 | S88 | -1988 | 110 | 16 X 98 | Output |
| 586 | S87 | -2004 | 227 | 16 X 98 | Output |
| 587 | S86 | -2020 | 110 | 16 X 98 | Output |
| 588 | S85 | -2036 | 227 | 16 X 98 | Output |
| 589 | S84 | -2052 | 110 | 16 X 98 | Output |
| 590 | S83 | -2068 | 227 | 16 X 98 | Output |
| 591 | S82 | -2084 | 110 | 16 X 98 | Output |
| 592 | S81 | -2100 | 227 | 16 X 98 | Output |
| 593 | S80 | -2116 | 110 | 16 X 98 | Output |
| 594 | S79 | -2132 | 227 | 16 X 98 | Output |
| 595 | S78 | -2148 | 110 | 16 X 98 | Output |
| 596 | S77 | -2164 | 227 | 16 X 98 | Output |
| 597 | S76 | -2180 | 110 | 16 X 98 | Output |
| 598 | S75 | -2196 | 227 | 16 X 98 | Output |
| 599 | S74 | -2212 | 110 | 16 X 98 | Output |
| 600 | S73 | -2228 | 227 | 16 X 98 | Output |
| 601 | S72 | -2244 | 110 | 16 X 98 | Output |
| 602 | S71 | -2260 | 227 | 16 X 98 | Output |
| 603 | S70 | -2276 | 110 | 16 X 98 | Output |
| 604 | S69 | -2292 | 227 | 16 X 98 | Output |
| 605 | S68 | -2308 | 110 | 16 X 98 | Output |
| 606 | S67 | -2324 | 227 | 16 X 98 | Output |
| 607 | S66 | -2340 | 110 | 16 X 98 | Output |
| 608 | S65 | -2356 | 227 | 16 X 98 | Output |
| 609 | S64 | -2372 | 110 | 16 X 98 | Output |
| 610 | S63 | -2388 | 227 | 16 X 98 | Output |
| 611 | S62 | -2404 | 110 | 16 X 98 | Output |
| 612 | S61 | -2420 | 227 | 16 X 98 | Output |
| 613 | S60 | -2436 | 110 | 16 X 98 | Output |
| 614 | S59 | -2452 | 227 | 16 X 98 | Output |
| 615 | S58 | -2468 | 110 | 16 X 98 | Output |
| 616 | S57 | -2484 | 227 | 16 X 98 | Output |
| 617 | S56 | -2500 | 110 | 16 X 98 | Output |
| 618 | S55 | -2516 | 227 | 16 X 98 | Output |
| 619 | S54 | -2532 | 110 | 16 X 98 | Output |
| 620 | S53 | -2548 | 227 | 16 X 98 | Output |
| 621 | S52 | -2564 | 110 | 16 X 98 | Output |
| 622 | S51 | -2580 | 227 | 16 X 98 | Output |
| 623 | S50 | -2596 | 110 | 16 X 98 | Output |
| 624 | S49 | -2612 | 227 | 16 X 98 | Output |
| 625 | S48 | -2628 | 110 | 16 X 98 | Output |
| 626 | S47 | -2644 | 227 | 16 X 98 | Output |
| 627 | S46 | -2660 | 110 | 16 X 98 | Output |
| 628 | S45 | -2676 | 227 | 16 X 98 | Output |
| 629 | S44 | -2692 | 110 | 16 X 98 | Output |
| 630 | S43 | -2708 | 227 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 631 | S42 | -2724 | 110 | 16 X 98 | Output |
| 632 | S41 | -2740 | 227 | 16 X 98 | Output |
| 633 | S40 | -2756 | 110 | 16 X 98 | Output |
| 634 | S39 | -2772 | 227 | 16 X 98 | Output |
| 635 | S38 | -2788 | 110 | 16 X 98 | Output |
| 636 | S37 | -2804 | 227 | 16 X 98 | Output |
| 637 | S36 | -2820 | 110 | 16 X 98 | Output |
| 638 | S35 | -2836 | 227 | 16 X 98 | Output |
| 639 | S34 | -2852 | 110 | 16 X 98 | Output |
| 640 | S33 | -2868 | 227 | 16 X 98 | Output |
| 641 | S32 | -2884 | 110 | 16 X 98 | Output |
| 642 | S31 | -2900 | 227 | 16 X 98 | Output |
| 643 | S30 | -2916 | 110 | 16 X 98 | Output |
| 644 | S29 | -2932 | 227 | 16 X 98 | Output |
| 645 | S28 | -2948 | 110 | 16 X 98 | Output |
| 646 | S27 | -2964 | 227 | 16 X 98 | Output |
| 647 | S26 | -2980 | 110 | 16 X 98 | Output |
| 648 | S25 | -2996 | 227 | 16 X 98 | Output |
| 649 | S24 | -3012 | 110 | 16 X 98 | Output |
| 650 | S23 | -3028 | 227 | 16 X 98 | Output |
| 651 | S22 | -3044 | 110 | 16 X 98 | Output |
| 652 | S21 | -3060 | 227 | 16 X 98 | Output |
| 653 | S20 | -3076 | 110 | 16 X 98 | Output |
| 654 | S19 | -3092 | 227 | 16 X 98 | Output |
| 655 | S18 | -3108 | 110 | 16 X 98 | Output |
| 656 | S17 | -3124 | 227 | 16 X 98 | Output |
| 657 | S16 | -3140 | 110 | 16 X 98 | Output |
| 658 | S15 | -3156 | 227 | 16 X 98 | Output |
| 659 | S14 | -3172 | 110 | 16 X 98 | Output |
| 660 | S13 | -3188 | 227 | 16 X 98 | Output |
| 661 | S12 | -3204 | 110 | 16 X 98 | Output |
| 662 | S11 | -3220 | 227 | 16 X 98 | Output |
| 663 | S10 | -3236 | 110 | 16 X 98 | Output |
| 664 | S9 | -3252 | 227 | 16 X 98 | Output |
| 665 | S8 | -3268 | 110 | 16 X 98 | Output |
| 666 | S7 | -3284 | 227 | 16 X 98 | Output |
| 667 | S6 | -3300 | 110 | 16 X 98 | Output |
| 668 | S5 | -3316 | 227 | 16 X 98 | Output |
| 669 | S4 | -3332 | 110 | 16 X 98 | Output |
| 670 | S3 | -3348 | 227 | 16 X 98 | Output |
| 671 | S2 | -3364 | 110 | 16 X 98 | Output |
| 672 | S1 | -3380 | 227 | 16 X 98 | Output |
| 673 | DUMMY | -3396 | 110 | 16 X 98 | Output |
| 674 | DUMMY | -3412 | 227 | 16 X 98 | Output |
| 675 | DUMMY | -3428 | 110 | 16 X 98 | Output |
| 676 | DUMMY | -3444 | 227 | 16 X 98 | Output |
| 677 | G1 | -3460 | 110 | 16 X 98 | Output |
| 678 | G3 | -3476 | 227 | 16 X 98 | Output |
| 679 | G5 | -3492 | 110 | 16 X 98 | Output |
| 680 | G7 | -3508 | 227 | 16 X 98 | Output |
| 681 | G9 | -3524 | 110 | 16 X 98 | Output |
| 682 | G11 | -3540 | 227 | 16 X 98 | Output |
| 683 | G13 | -3556 | 110 | 16 X 98 | Output |
| 684 | G15 | -3572 | 227 | 16 X 98 | Output |
| 685 | G17 | -3588 | 110 | 16 X 98 | Output |
| 686 | G19 | -3604 | 227 | 16 X 98 | Output |
| 687 | G21 | -3620 | 110 | 16 X 98 | Output |
| 688 | G23 | -3636 | 227 | 16 X 98 | Output |
| 689 | G25 | -3652 | 110 | 16 X 98 | Output |
| 690 | G27 | -3668 | 227 | 16 X 98 | Output |
| 691 | G29 | -3684 | 110 | 16 X 98 | Output |
| 692 | G31 | -3700 | 227 | 16 X 98 | Output |
| 693 | G33 | -3716 | 110 | 16 X 98 | Output |
| 694 | G35 | -3732 | 227 | 16 X 98 | Output |
| 695 | G37 | -3748 | 110 | 16 X 98 | Output |
| 696 | G39 | -3764 | 227 | 16 X 98 | Output |
| 697 | G41 | -3780 | 110 | 16 X 98 | Output |
| 698 | G43 | -3796 | 227 | 16 X 98 | Output |
| 699 | G45 | -3812 | 110 | 16 X 98 | Output |
| 700 | G47 | -3828 | 227 | 16 X 98 | Output |

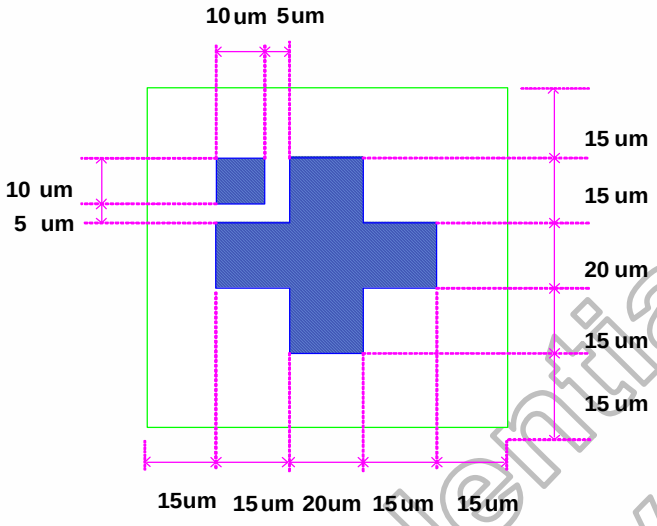
| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|
| 701 | G49 | -3844 | 110 | 16 X 98 | Output |
| 702 | G51 | -3860 | 227 | 16 X 98 | Output |
| 703 | G53 | -3876 | 110 | 16 X 98 | Output |
| 704 | G55 | -3892 | 227 | 16 X 98 | Output |
| 705 | G57 | -3908 | 110 | 16 X 98 | Output |
| 706 | G59 | -3924 | 227 | 16 X 98 | Output |
| 707 | G61 | -3940 | 110 | 16 X 98 | Output |
| 708 | G63 | -3956 | 227 | 16 X 98 | Output |
| 709 | G65 | -3972 | 110 | 16 X 98 | Output |
| 710 | G67 | -3988 | 227 | 16 X 98 | Output |
| 711 | G69 | -4004 | 110 | 16 X 98 | Output |
| 712 | G71 | -4020 | 227 | 16 X 98 | Output |
| 713 | G73 | -4036 | 110 | 16 X 98 | Output |
| 714 | G75 | -4052 | 227 | 16 X 98 | Output |
| 715 | G77 | -4068 | 110 | 16 X 98 | Output |
| 716 | G79 | -4084 | 227 | 16 X 98 | Output |
| 717 | G81 | -4100 | 110 | 16 X 98 | Output |
| 718 | G83 | -4116 | 227 | 16 X 98 | Output |
| 719 | G85 | -4132 | 110 | 16 X 98 | Output |
| 720 | G87 | -4148 | 227 | 16 X 98 | Output |
| 721 | G89 | -4164 | 110 | 16 X 98 | Output |
| 722 | G91 | -4180 | 227 | 16 X 98 | Output |
| 723 | G93 | -4196 | 110 | 16 X 98 | Output |
| 724 | G95 | -4212 | 227 | 16 X 98 | Output |
| 725 | G97 | -4228 | 110 | 16 X 98 | Output |
| 726 | G99 | -4244 | 227 | 16 X 98 | Output |
| 727 | G101 | -4260 | 110 | 16 X 98 | Output |
| 728 | G103 | -4276 | 227 | 16 X 98 | Output |
| 729 | G105 | -4292 | 110 | 16 X 98 | Output |
| 730 | G107 | -4308 | 227 | 16 X 98 | Output |
| 731 | G109 | -4324 | 110 | 16 X 98 | Output |
| 732 | G111 | -4340 | 227 | 16 X 98 | Output |
| 733 | G113 | -4356 | 110 | 16 X 98 | Output |
| 734 | G115 | -4372 | 227 | 16 X 98 | Output |
| 735 | G117 | -4388 | 110 | 16 X 98 | Output |
| 736 | G119 | -4404 | 227 | 16 X 98 | Output |
| 737 | G121 | -4420 | 110 | 16 X 98 | Output |
| 738 | G123 | -4436 | 227 | 16 X 98 | Output |
| 739 | G125 | -4452 | 110 | 16 X 98 | Output |
| 740 | G127 | -4468 | 227 | 16 X 98 | Output |
| 741 | G129 | -4484 | 110 | 16 X 98 | Output |
| 742 | G131 | -4500 | 227 | 16 X 98 | Output |
| 743 | G133 | -4516 | 110 | 16 X 98 | Output |
| 744 | G135 | -4532 | 227 | 16 X 98 | Output |
| 745 | G137 | -4548 | 110 | 16 X 98 | Output |
| 746 | G139 | -4564 | 227 | 16 X 98 | Output |
| 747 | G141 | -4580 | 110 | 16 X 98 | Output |
| 748 | G143 | -4596 | 227 | 16 X 98 | Output |
| 749 | G145 | -4612 | 110 | 16 X 98 | Output |
| 750 | G147 | -4628 | 227 | 16 X 98 | Output |
| 751 | G149 | -4644 | 110 | 16 X 98 | Output |
| 752 | G151 | -4660 | 227 | 16 X 98 | Output |
| 753 | G153 | -4676 | 110 | 16 X 98 | Output |
| 754 | G155 | -4692 | 227 | 16 X 98 | Output |
| 755 | G157 | -4708 | 110 | 16 X 98 | Output |
| 756 | G159 | -4724 | 227 | 16 X 98 | Output |
| 757 | G161 | -4740 | 110 | 16 X 98 | Output |
| 758 | DUMMY | -4756 | 227 | 16 X 98 | Output |
| 759 | DUMMY | -4772 | 110 | 16 X 98 | Output |

| No. | PAD NAME | X | Y | Bump Size | I/O Pad |
|---|---|---|---|---|---|

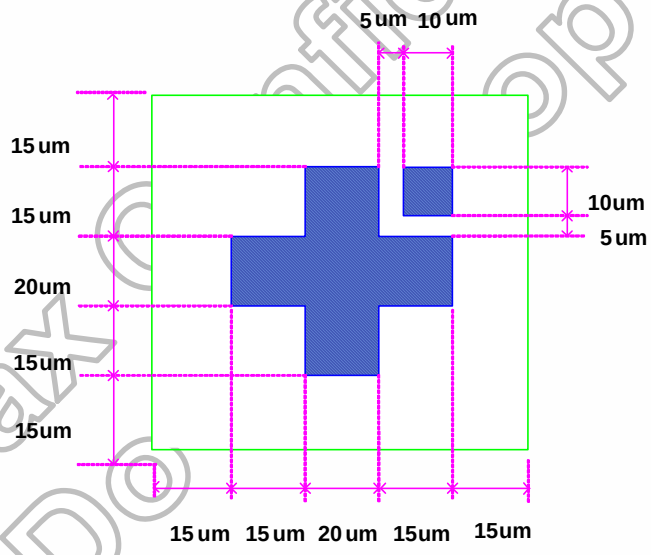
| Alignment mark | X | Y |
|---|---|---|
| A1 | -4841 | -220 |
| A2 | 4841 | -220 |

## 4.4 Alignment mark

A_MARK (A1)

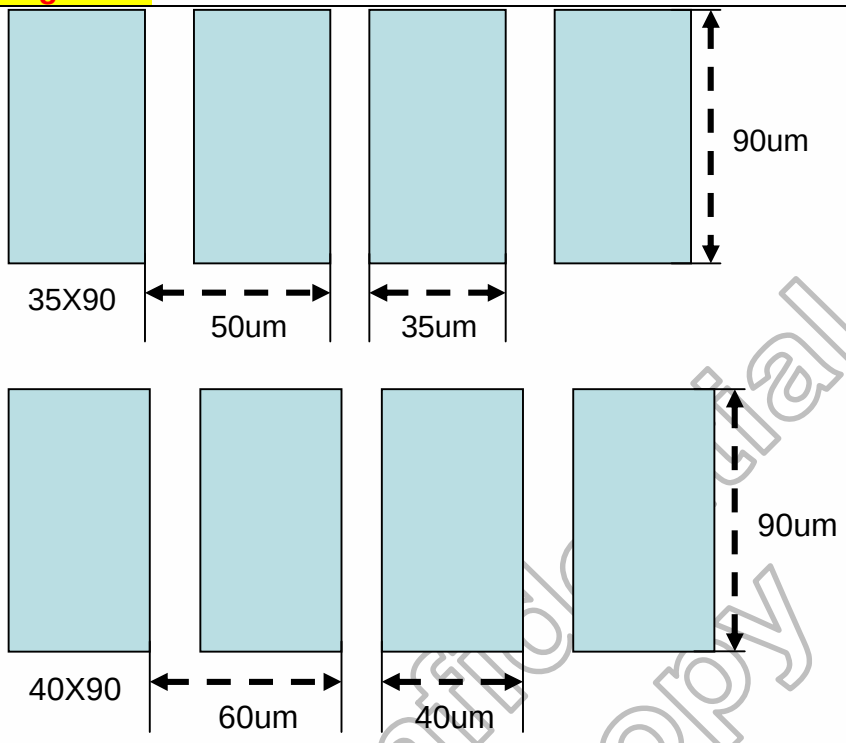



A_MARK (A2)



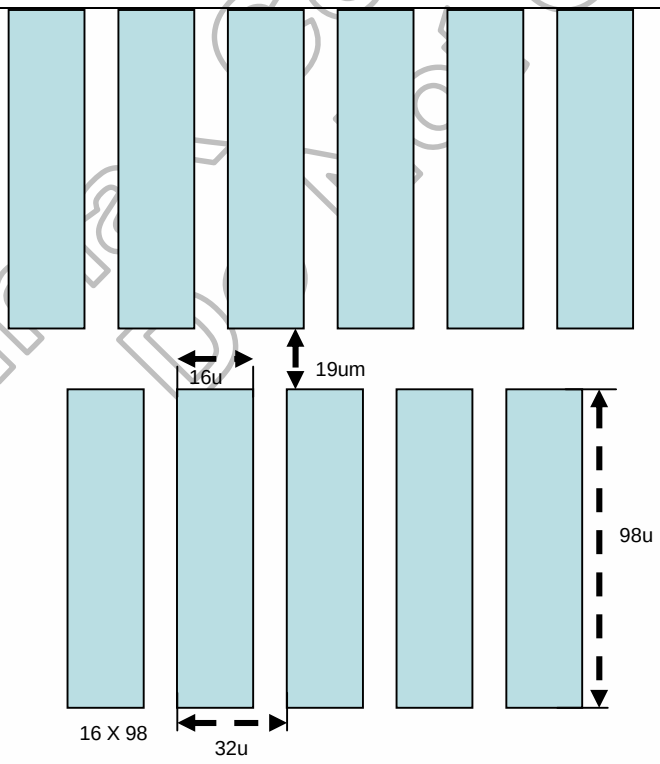
## 4.5 Bump arrangement

Input/Output PAD




Note: 35X90 : Pad no. 1~62
Pad no. 90~185
40X90: pad no. 63~89

Output PAD




Note: 16X98 : Pad no.186~759

# 5. Function Description

## 5.1 System Interface

The HX8353-C **supports parallel 80-system and 68-system 18-/16-/9-/8-bits bus bus interface mode and 3W/4W serial interface mode.** When NCS = "L", the parallel and serial bus system interface of the HX8353-C become active and data transfer through the interface circuit is available. The DNC_ SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS(2-0). For selecting the format of input bus, please refer to Table 5.1 and Table 5.2.

HX8353-C includes command code and the following parameter and GRAM data. The command code can be written through data bus by setting DNC_ SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_ SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

| SPI_SEL | P68 | BS2 | BS1 | BS0 | Interface |
|---|---|---|---|---|---|
| x | 0 | 1 | 0 | 0 | 80-system 8-bit Parallel |
| x | 0 | 1 | 0 | 1 | 80-system 16-bit Parallel |
| x | 0 | 1 | 1 | 0 | 80-system 9-bit Parallel |
| x | 0 | 1 | 1 | 1 | 80-system 18-bit Parallel |
| x | 1 | 1 | 0 | 0 | 68-system 8-bit Parallel |
| x | 1 | 1 | 0 | 1 | 68-system 16-bit Parallel |
| x | 1 | 1 | 1 | 0 | 68-system 9-bit Parallel |
| x | 1 | 1 | 1 | 1 | 68-system 18-bit Parallel |
| 0 | x | 0 | x | x | 3 wire serial Interface only |
| 1 | x | 0 | x | x | 4 wire serial Interface only |

**Table 5. 1 Interface selection**

| Interface | E_NRD | RW_NWR | DNC_SCL | SDA | DB17 – DB0 |
|---|---|---|---|---|---|
| 80-system 8-bit Parallel | NRD | NWR | DNC | Unused | DB17-DB8: Unused,<br>DB7-DB0: 8 bit data bus |
| 80-system 9-bit Parallel | NRD | NWR | DNC | Unused | DB17-DB9: Unused,<br>DB8-DB0: 9 bit data bus |
| 80-system 16-bit Parallel | NRD | NWR | DNC | Unused | DB17-DB16: Unused,<br>DB15-DB0: 16 bit data bus |
| 80-system 18-bit Parallel | NRD | NWR | DNC | Unused | DB17-DB0: 18 bit data bus |
| 3 wire serial Interface | Unused | -- | SCL | SDA | Unused |
| 68-system 8-bit Parallel | E | RW | DNC | Unused | DB17-DB8: Unused,<br>DB7-DB0: 8 bit data bus |
| 68-system 9-bit Parallel | E | RW | DNC | Unused | DB17-DB9: Unused,<br>DB8-DB0: 9 bit data bus |
| 68-system 16-bit Parallel | E | RW | DNC | Unused | DB17-DB16: Unused,<br>DB15-DB0: 16 bit data bus |
| 68-system 18-bit Parallel | E | RW | DNC | Unused | DB17-DB0: 18 bit data bus |
| 4 wire serial Interface | Unused | DNC | SCL | SDA | Unused |

**Table 5. 2 Interface Mode Selection**

### 5.1.1 Parallel Bus System Interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface as listed in Table 5.3 and Table 5.4.

| Operations | NWR_RNW | NRD_E | DNC_SCL |
|---|---|---|---|
| Writes command code | 0 | 1 | 0 |
| Reads internal status | 1 | 0 | 0 |
| Writes parameter into command or data into GRAM | 0 | 1 | 1 |
| Reads parameter from command or data from GRAM | 1 | 0 | 1 |

**Table 5. 3 Data Pin Function for I80 Series CPU**

| Operations | NWR_RNW | NRD_E | DNC_SCL |
|---|---|---|---|
| Writes command code | 1 | 0 | 0 |
| Reads internal status | 1 | 1 | 0 |
| Writes parameter into command or data into GRAM | 1 | 0 | 1 |
| Reads parameter from command or data from GRAM | 1 | 1 | 1 |

**Table 5. 4 Data Pin Function for M68 Series CPU**

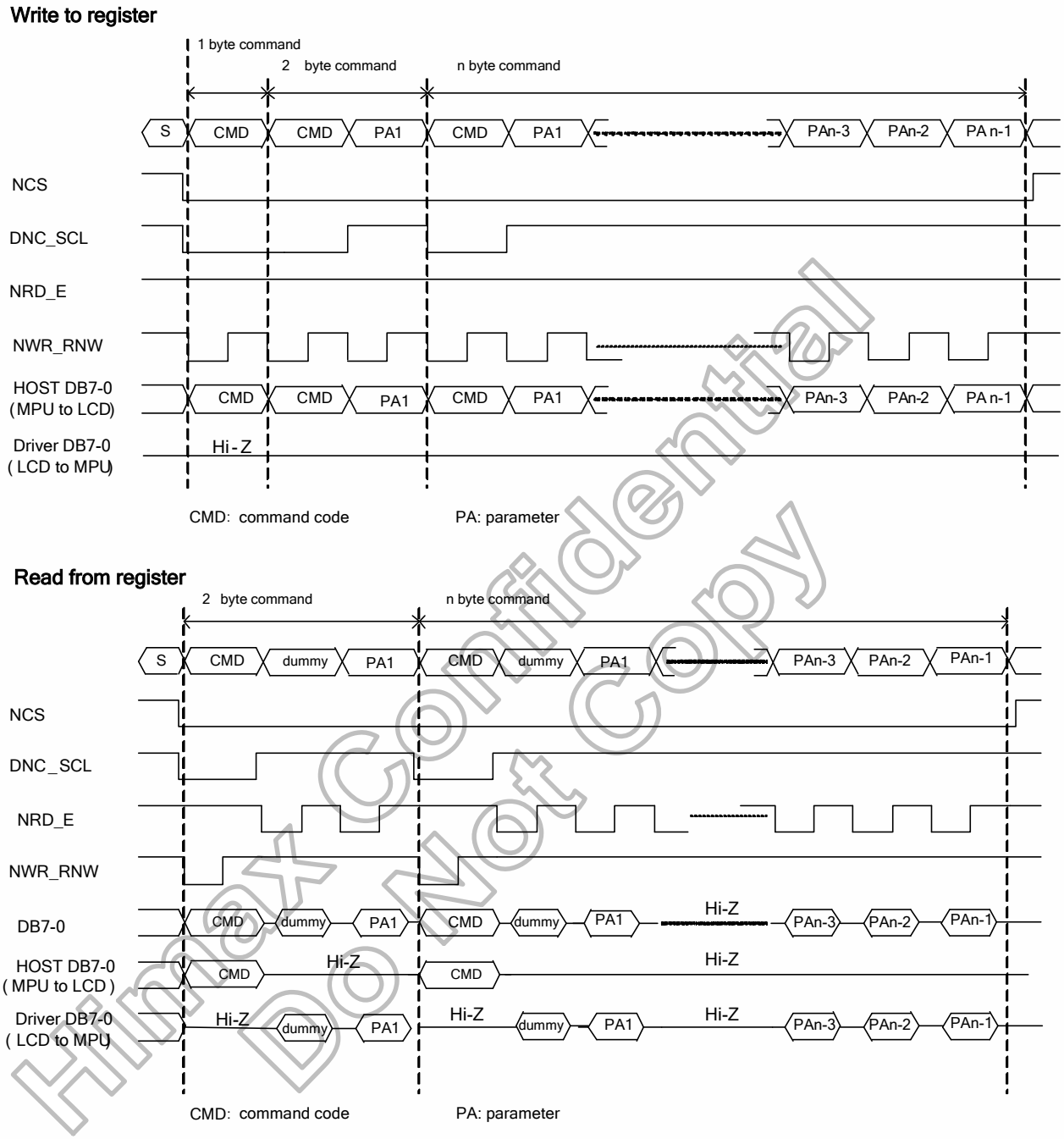



**Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 series MPU)**

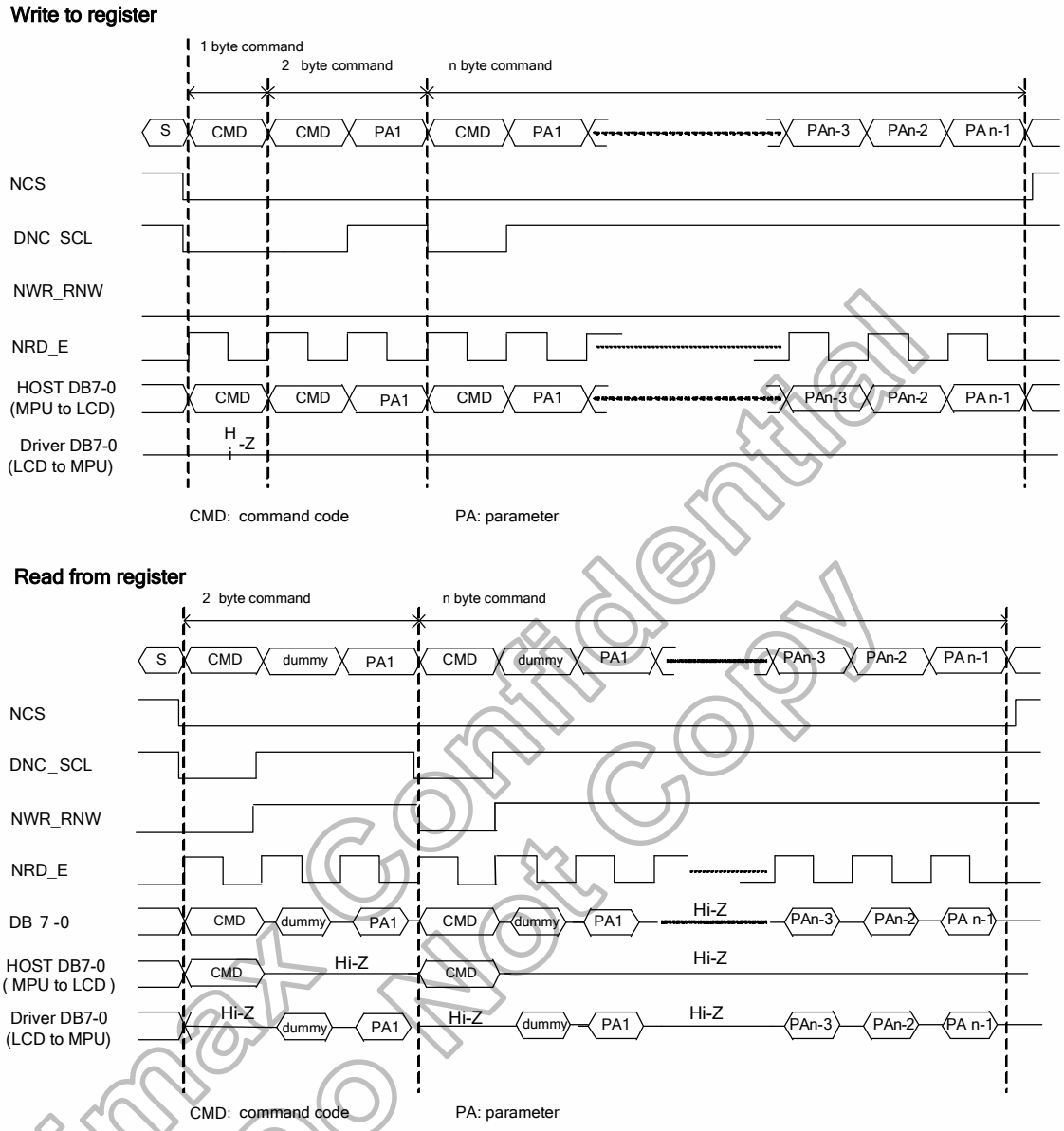
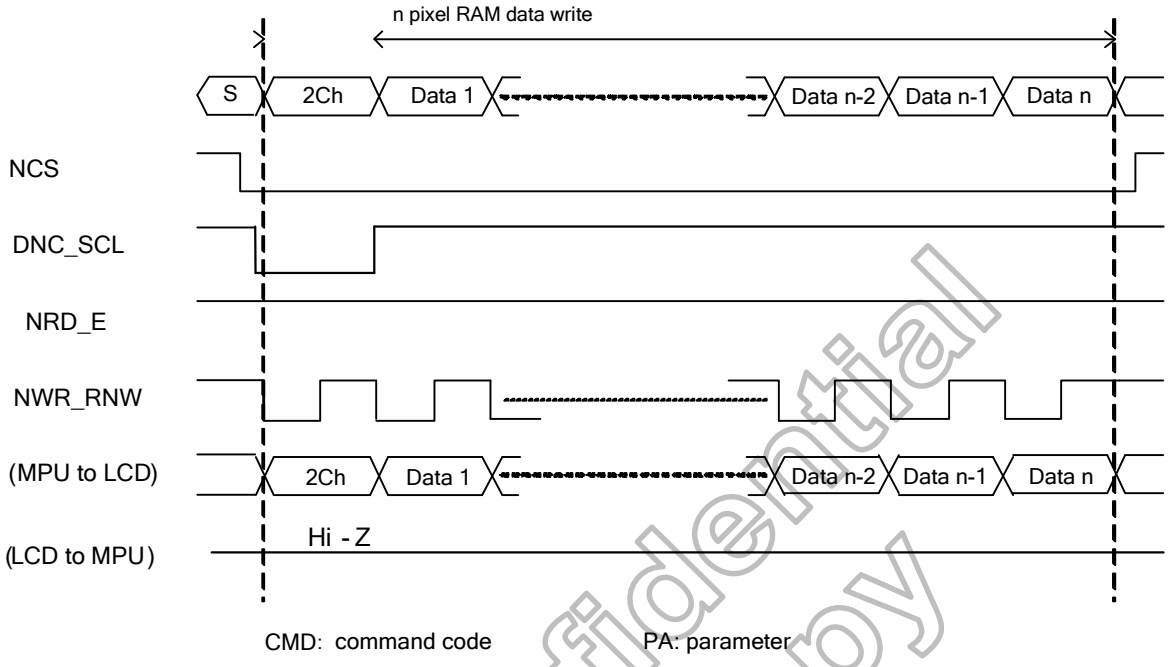



**Figure 5. 2 Register Read/Write Timing in Parallel Bus System Interface (for M68 series MPU)**

### Write to GRAM




### Read from GRAM

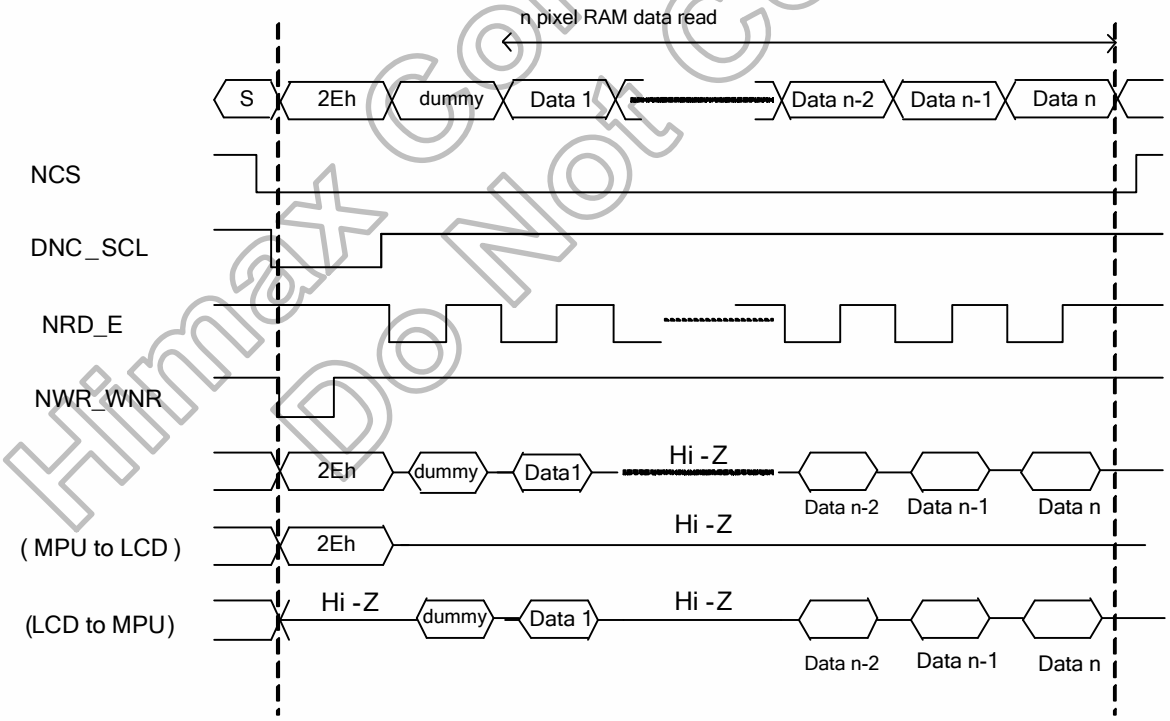
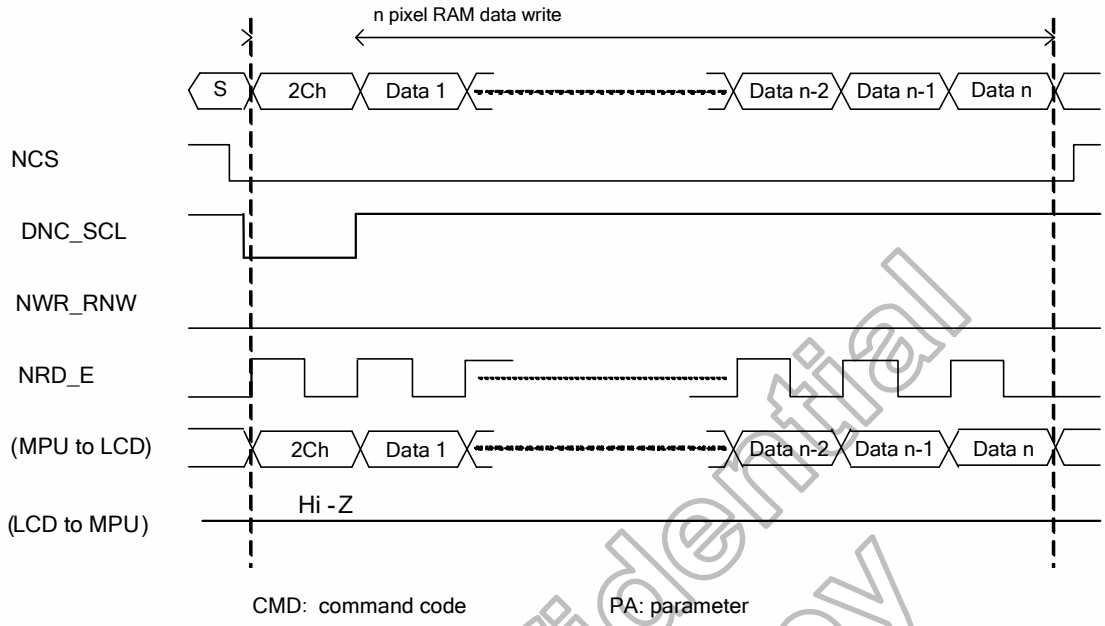



**Figure 5. 3 GRAM Read/Write Timing in Parallel Bus System Interface (for I80 series MPU)**

**Write to GRAM**




**Read from GRAM**

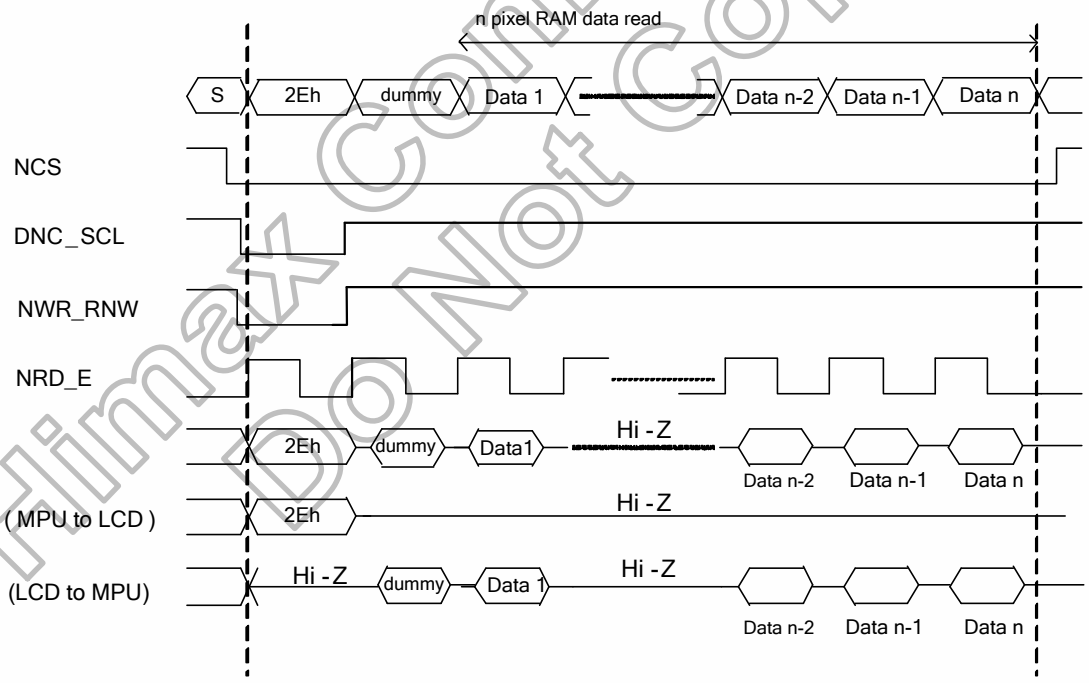



**Figure 5. 4 GRAM Read/Write Timing in Parallel Bus System Interface (for M68 series MPU)**

### 8-bit bus Interface

The I80-system 8-bit parallel bus interface can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0100”. And the M68-system 8-bit parallel bus interface can be used by setting “P68, BS2, BS1, and BS0” pins to “1100”. Figure 5.5 is the example of interface with I80/M68 microcomputer system interface and Figure 5.6 ~Figure 5.9 is bit format per pixel color order.

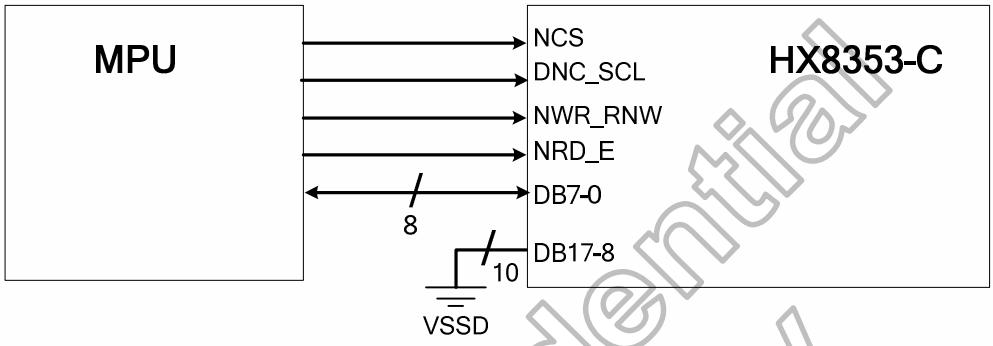



**Figure 5. 5 Example of 80- / 68- System 8-bit bus Interface**

The data format of write display data at 8-bit bus Interface. See Figure 5.6 ~Figure 5.9.

| 262k Color Data | DNC/ RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R15 | R14 | R13 | R12 | R11 | R10 | x | x | - |
| 2nd write | 1 | G15 | G14 | G13 | G12 | G11 | G10 | x | x | - |
| 3rd write | 1 | B15 | B14 | B13 | B12 | B11 | B10 | x | x | 1st pixel (R1/G1/B1) |
| 4th write | 1 | R25 | R24 | R23 | R22 | R21 | R20 | x | x | - |
| 5th write | 1 | G25 | G24 | G23 | G22 | G21 | G20 | x | x | - |
| 6th write | 1 | B25 | B24 | B23 | B22 | B21 | B20 | x | x | 2nd pixel (R2/G2/B2) |

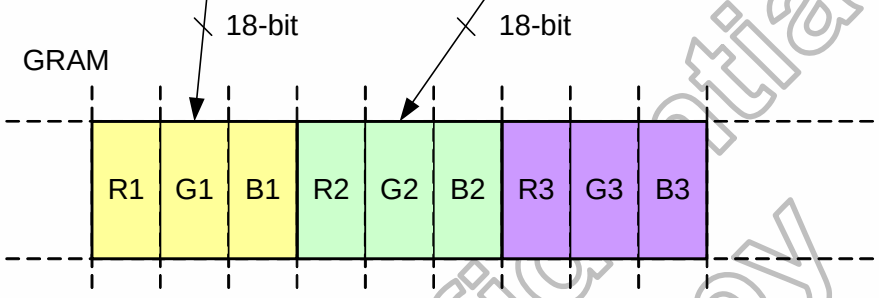
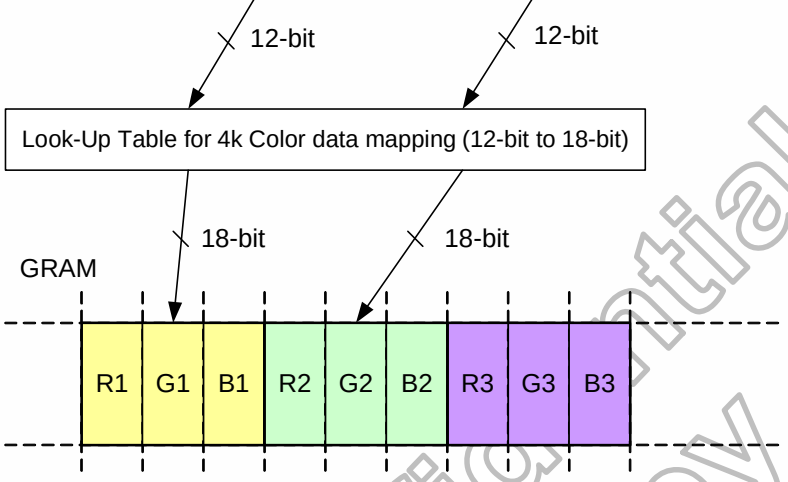



**Figure 5. 6 Write data for RGB 6-6-6-bits input (support DMIF-S43AP-J124 and LUT_EN=1)**

| 4k Color Data | DNC/ RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R13 | R12 | R11 | R10 | G13 | G12 | G11 | G10 | - |
| 2nd write | 1 | B13 | B12 | B11 | B10 | R23 | R22 | R21 | R20 | 1st pixel (R1/G1/B1) |
| 3rd write | 1 | G23 | G22 | G21 | G20 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |




| 4k Color Data | DNC/ RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R13 | R12 | R11 | R10 | G13 | G12 | G11 | G10 | - |
| 2nd write | 1 | B13 | B12 | B11 | B10 | R23 | R22 | R21 | R20 | 1st pixel (R1/G1/B1) |
| MEMWR | 0 | The other command | | | | | | | | - |
| MEMWR | 0 | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R23 | R22 | R21 | R20 | G23 | G22 | G21 | G20 | - |
| 2nd write | 1 | B23 | B22 | B21 | B20 | R33 | R32 | R31 | R30 | 2nd pixel (R2/G2/B2) |
| 3rd write | 1 | G33 | G32 | G31 | G30 | B33 | B32 | B31 | B30 | 3rd pixel (R3/G3/B3) |

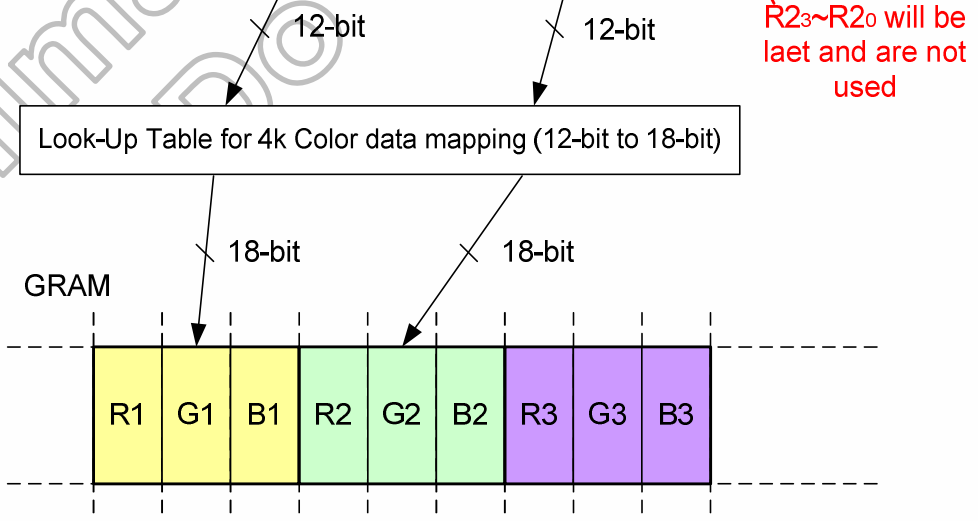





**Figure 5. 7 Write data for RGB 4-4-4-bits input (support Look-up table and LUT_EN=0)**

| 65k Color Data | DNC/ RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | - |
| 2nd write | 1 | G12 | G11 | G10 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 3rd write | 1 | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | - |
| 4th write | 1 | G22 | G21 | G20 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

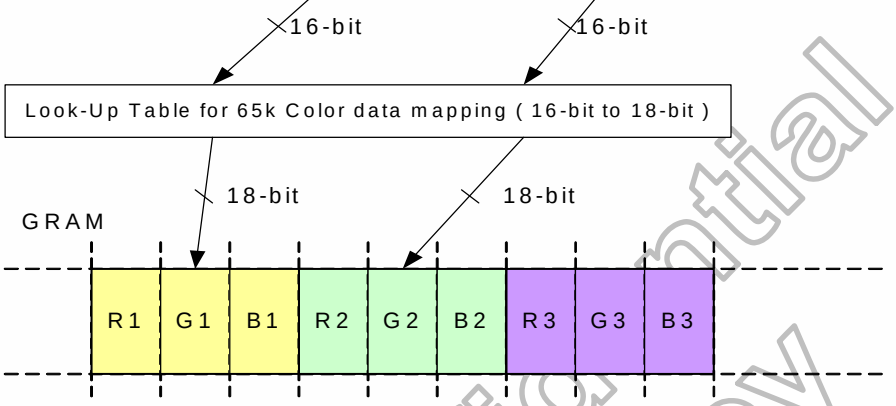



**Figure 5. 8 Write data for RGB 5-6-5-bits input (support Look-up table and LUT_EN=0)**

## 16-bit Parallel Bus System Interface

The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0101”. And the M68-system 16-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1” pins to “1101”. The Figure 5.9 is the example of interface with I80/M68 microcomputer system interface. There are three types of data format to write display data at 18-bit bus Interface. See Figure 5.10 Figure 5.12.

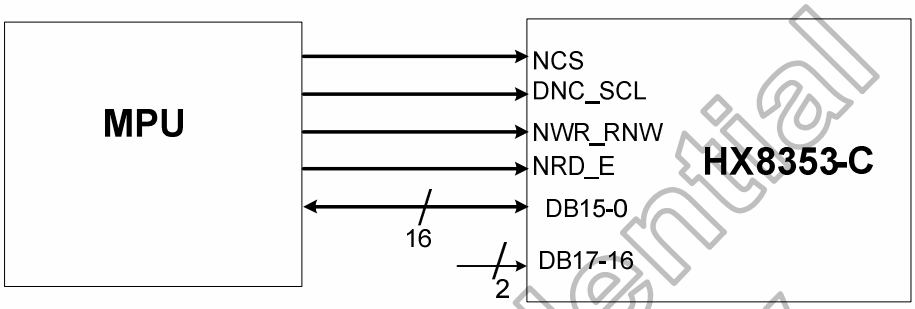



**Figure 5. 9 Example of I80- / M68- System 16-bit Parallel Bus Interface**

| | DNC_SCL | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | x | x | x | x | x | x | x | x | GRAM Write command code (2Ch) | | | | | | | | - |
| 1 st write | 1 | R15 | R14 | R13 | R12 | R11 | R10 | x | x | G15 | G14 | G13 | G12 | G11 | G10 | x | x | - |
| 2 nd write | 1 | B15 | B14 | B13 | B12 | B11 | B10 | x | x | R25 | R24 | R23 | R22 | R21 | R20 | x | x | 1st pixel (R1/G1/B1) |
| 3 rd write | 1 | G25 | G24 | G23 | G22 | G21 | G20 | x | x | B25 | B24 | B23 | B22 | B21 | B20 | x | x | 2nd pixel (R2/G2/B2) |

X : Don’t care

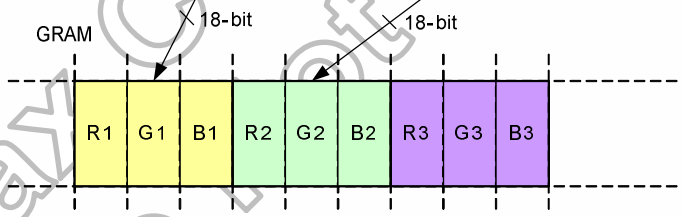



**Figure 5. 10 GRAM Write Data for RGB 6-6-6-(262k colours) bits input (LUT_EN=1)**

| 4k Color Data | DNC/RS | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | | | | | | | | - |
| 1st write | 1 | x | x | x | x | R13 | R12 | R11 | R10 | G13 | G12 | G11 | G10 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 2nd write | 1 | x | x | x | x | R23 | R22 | R21 | R20 | G23 | G22 | G21 | G20 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

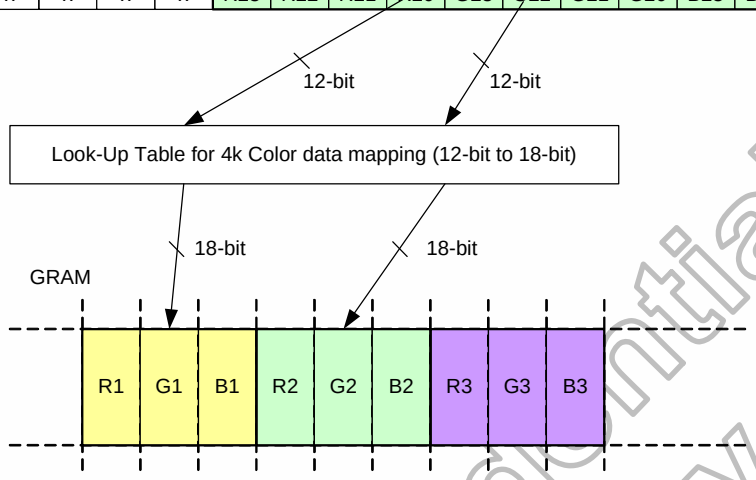



**Figure 5. 11 Write data for RGB 4-4-4 (4k colours) bits input on 16-bit parallel Interface (when support Look-up table and LUT_EN=0)**

| 65k Color Data | DNC/RS | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | x | x | x | x | x | x | x | x | GRAM Write command code | | | | | | | | - |
| 1st write | 1 | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | G12 | G11 | G10 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 2nd write | 1 | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | G22 | G21 | G20 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

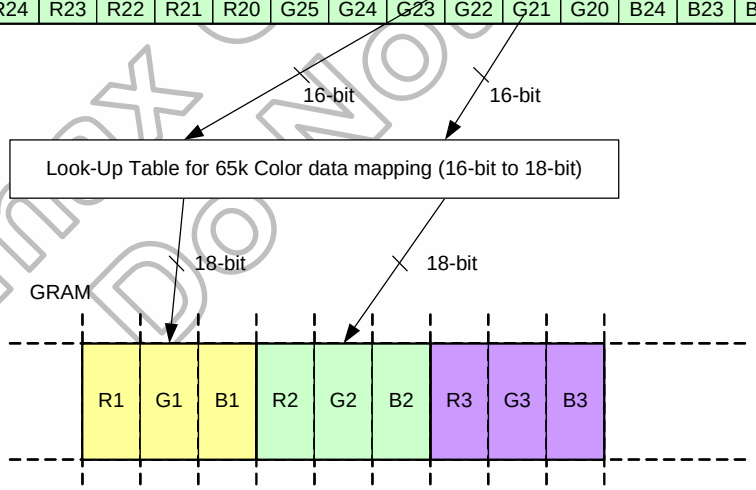



**Figure 5. 12 Write data for RGB 5-6-5 (65k colours) bits input on 16-bit parallel Interface (when support Look-up table and LUT_EN=0)**

## 18-bit Parallel Bus System Interface

The I80-system 18-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0111”. And the M68-system 18-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1111”. The Figure5.13 is the example of interface with I80/M68 microcomputer system
interface.

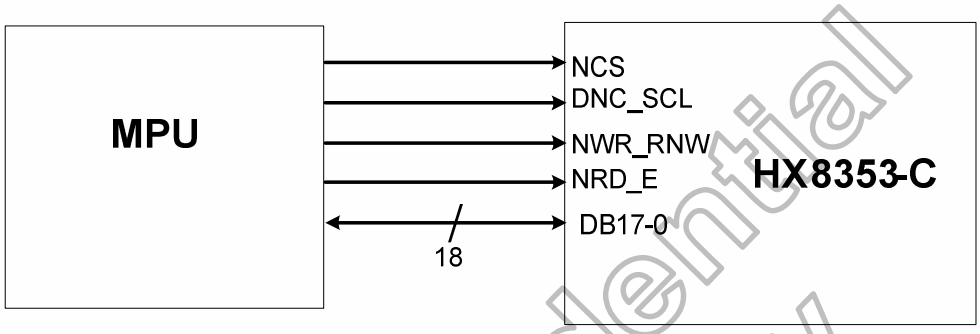



**Figure 5. 13 Example of I80- / M68- System 18-bit Parallel Bus Interface**

There are three types of data format to write display data at 18-bit bus Interface. See Figure 5.14 ~ Figure 5. 16.

| 4k Color Data | DNC/ RS | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | | | | | | | | | | - |
| 1st write | 1 | x | x | x | x | x | x | $R1_3$ | $R1_2$ | $R1_1$ | $R1_0$ | $G1_3$ | $G1_2$ | $G1_1$ | $G1_0$ | $B1_3$ | $B1_2$ | $B1_1$ | $B1_0$ | 1st pixel (R1/G1/B1) |
| 2nd write | 1 | x | x | x | x | x | x | $R2_3$ | $R2_2$ | $R2_1$ | $R2_0$ | $G2_3$ | $G2_2$ | $G2_1$ | $G2_0$ | $B2_3$ | $B2_2$ | $B2_1$ | $B2_0$ | 2nd pixel (R2/G2/B2) |

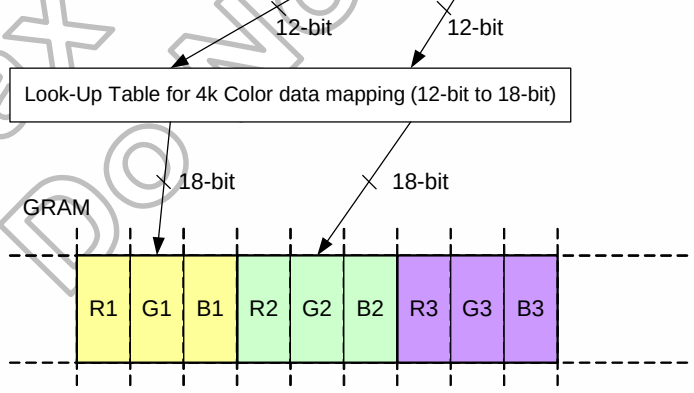



**Figure 5. 14 Write data for RGB 4-4-4 (4k colours) bits input in 18-bit parallel Interface (when support Look-up table and LUTENB=0)**

| 65k Color Data | DNC/RS | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | | | | | | | | | | - |
| 1st write | 1 | x | x | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | G12 | G11 | G10 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 2nd write | 1 | x | x | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | G22 | G21 | G20 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

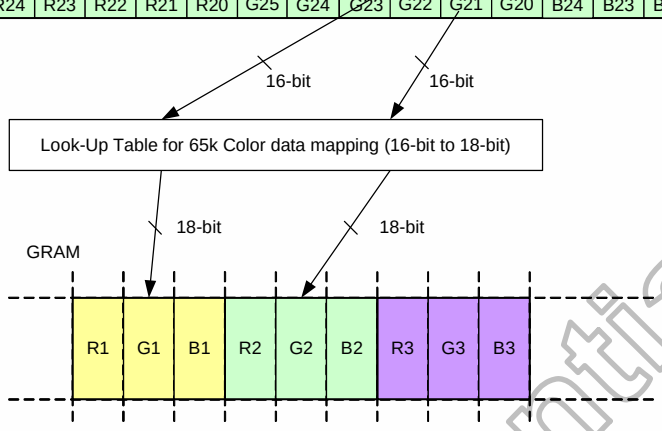



**Figure 5. 15 Write data for RGB 5-6-5 (65k colours) bits input in 18-bit parallel Interface (when support Look-up table and LUT_EN=0)**

| 262k Color Data | DNC/RS | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | | | | | | | | | | - |
| 1st write | 1 | R15 | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | G12 | G11 | G10 | B15 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 2nd write | 1 | R25 | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | G22 | G21 | G20 | B25 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

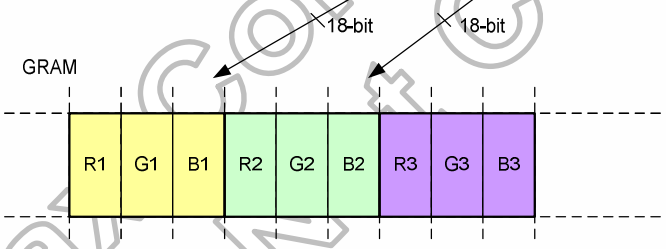



**Figure 5. 16 Write data for RGB 6-6-6(262k colours) bits input in 18-bit parallel Interface (LUT_EN=1)**

### 9-bit Bus Interface

The I80-system 9-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0110”. And the M68-system 9-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1110”. The Figure5.13 is the example of interface with I80/M68 microcomputer system interface.

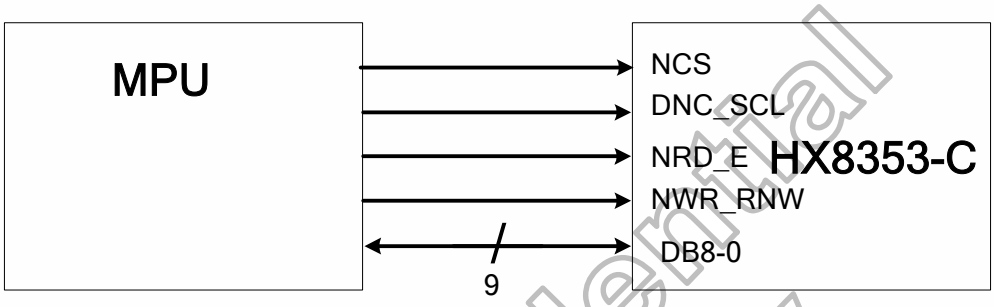



**Figure 5. 17 Example of 80- / 68- System 9-bit bus Interface**

There are five types data format to write display data at 9-bit bus Interface. See Figure 5. 18 ~ Figure 5. 22

| 4k Color Data | DNC | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | - |
| 1st write | 1 | x | R13 | R12 | R11 | R10 | G13 | G12 | G11 | G10 | - |
| 2nd write | 1 | x | B13 | B12 | B11 | B10 | R23 | R22 | R21 | R20 | 1st pixel (R1/G1/B1) |
| 3rd write | 1 | x | G23 | G22 | G21 | G20 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

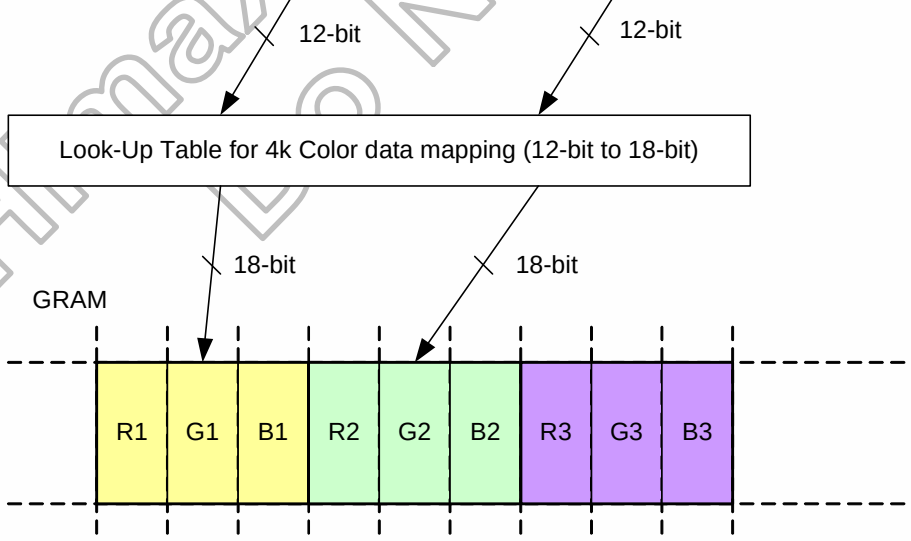



**Figure 5. 18 Write data for RGB 4-4-4 (4k colours) bits input in 9-bit parallel Interface (when support Look-up table and LUT_EN=0)**

| 65k Color Data | DNC | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | - |
| 1st write | 1 | x | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | - |
| 2nd write | 1 | x | G12 | G11 | G10 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 3rd write | 1 | x | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | - |
| 4th write | 1 | x | G22 | G21 | G20 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

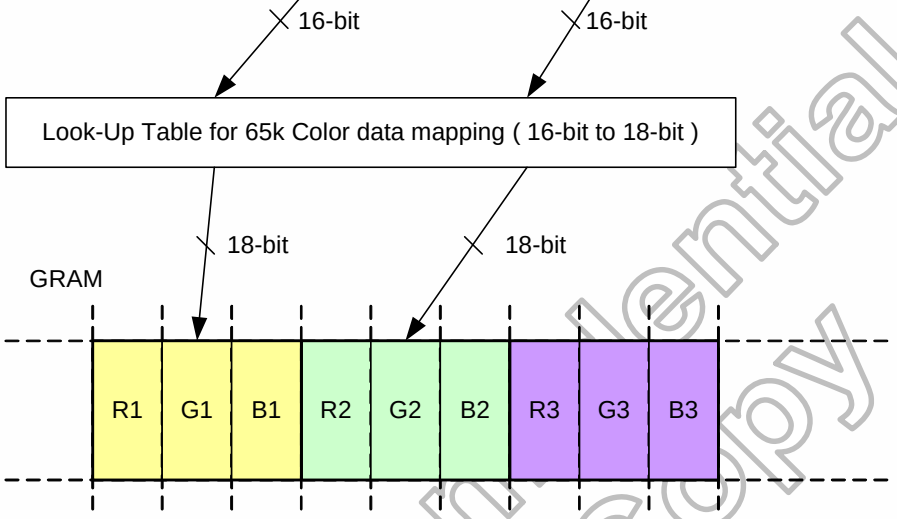



**Figure 5. 19 Write data for RGB 5-6-5(65k colours) bits input in 9-bit parallel Interface (when support Look-up table and LUT_EN=0)**

| 262k Color Data | DNC | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | GRAM Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MEMWR | 0 | GRAM Write command code | | | | | | | | | - |
| 1st write | 1 | R15 | R14 | R13 | R12 | R11 | R10 | G15 | G14 | G13 | - |
| 2nd write | 1 | G12 | G11 | G10 | B15 | B14 | B13 | B12 | B11 | B10 | 1st pixel (R1/G1/B1) |
| 3rd write | 1 | R25 | R24 | R23 | R22 | R21 | R20 | G25 | G24 | G23 | - |
| 4th write | 1 | G22 | G21 | G20 | B25 | B24 | B23 | B22 | B21 | B20 | 2nd pixel (R2/G2/B2) |

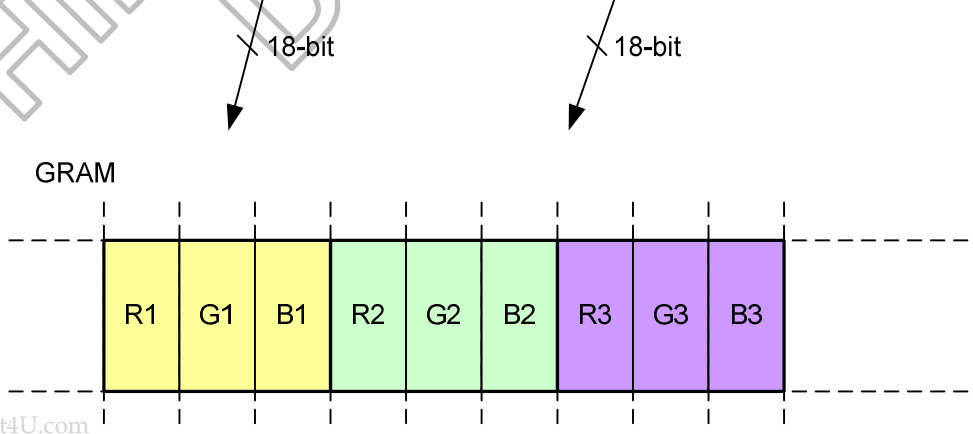





**Figure 5. 20 Write data for RGB 6-6-6-bits (262kcolours) input in 9-bit parallel Interface (LUT_EN=1)**

### 5.1.2 Serial Interface

The HX8353-C supports serial data transfer interface. The interface selection by setting BS2=0 for serial interface mode. The 3 wires serial bus and 4 wires serial bus is select by SPI_SEL pin. When SPI_SEL pin is low (VSSD), it is selected by 3 wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC _SCL). When SPI_SEL pin is high (VDDI), it is selected by 4 wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC _SCL) and NWR_RNW.

**Serial data write mode**

The 3-Pin serial data packet contains a control bit DNC and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by NWR_RNW pin. If NWR_RNW is low, the transmission byte is command byte. If NWR_RNW is high, the transmission byte is stored to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, DNC_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

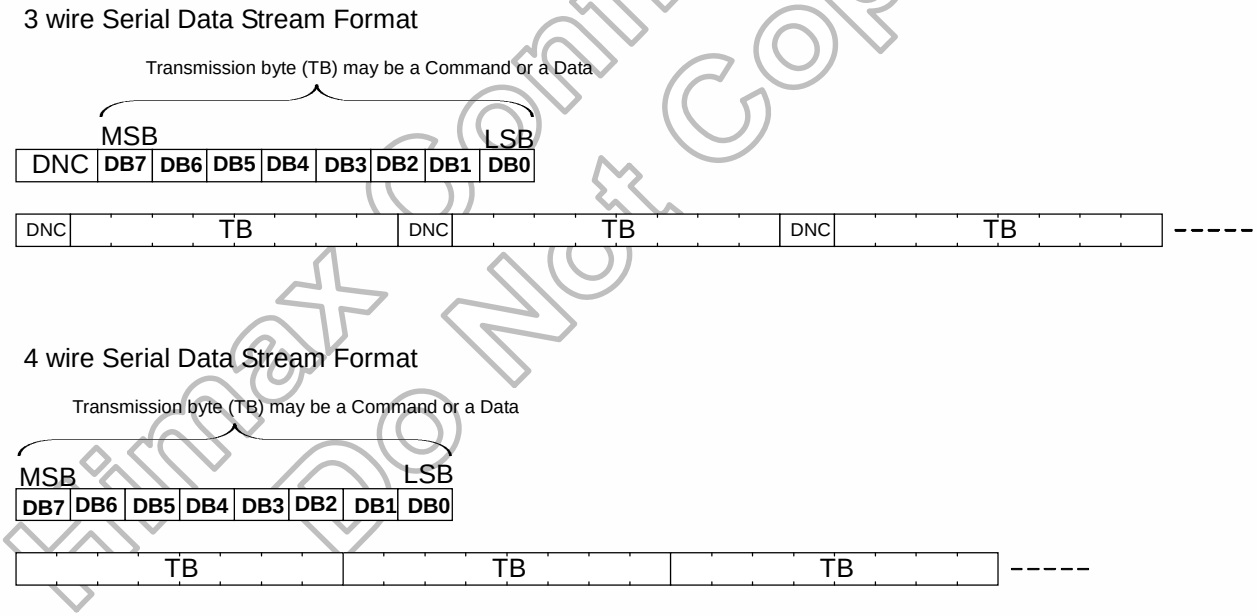



**Figure 5. 21 Serial Interface protocol data stream format**

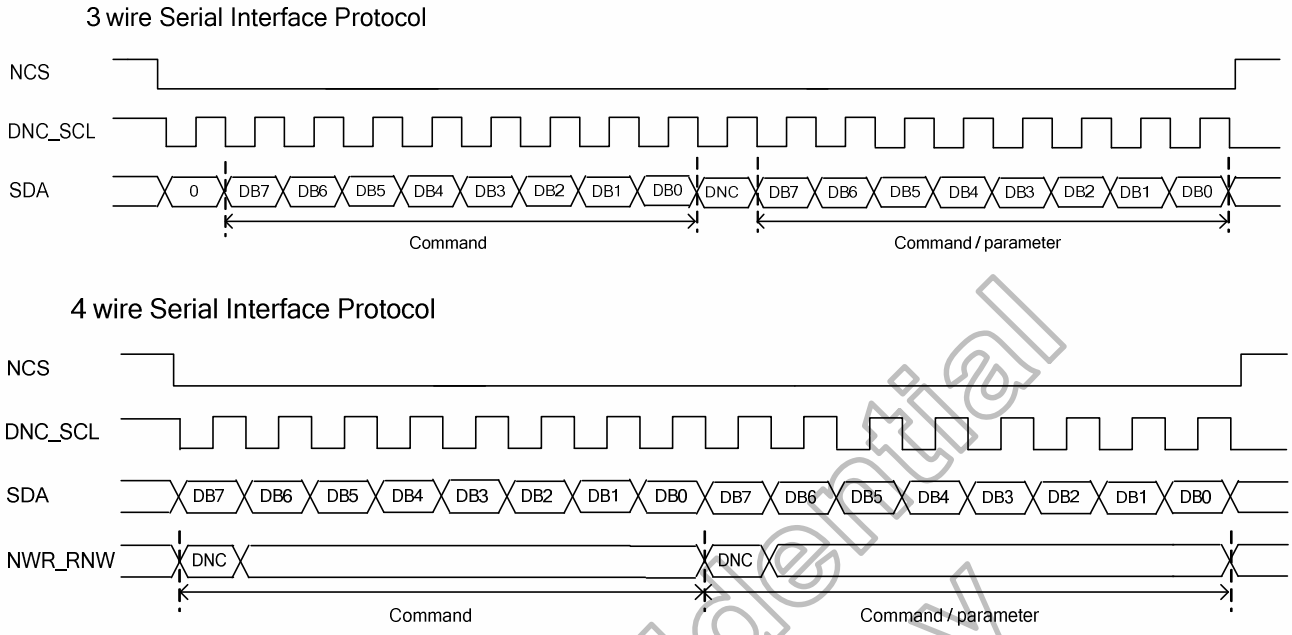



**Figure 5. 22 Serial Interface protocol 3 wire/4 wire, write mode**

## Serial data read mode

The micro controller first has to send a command and then the following byte is transmitted in the opposite direction. The read mode has three type command data transmitted (8- / 24- / 32-bit) is according command code.

3 Wires Serial Interface Protocol

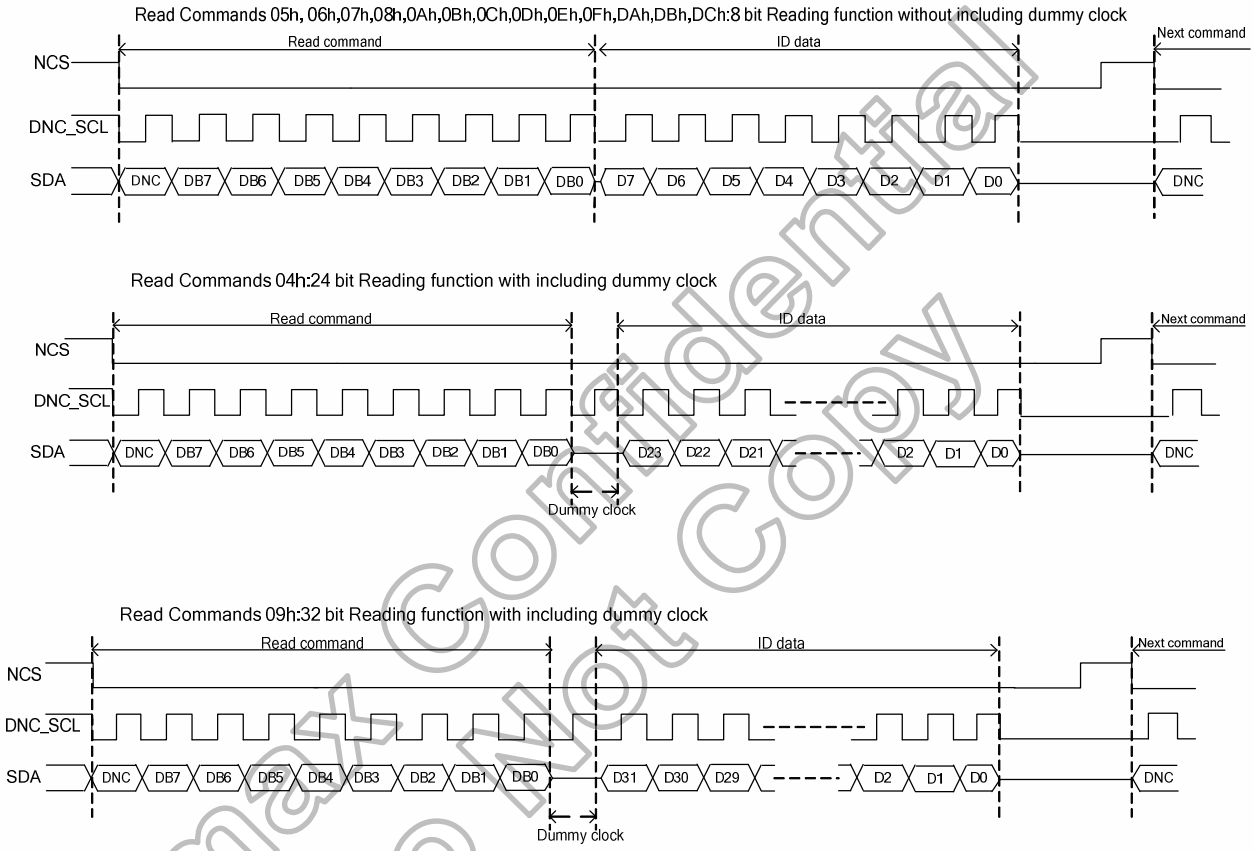



**Figure 5. 23 3 Wires Serial Interface protocol, read mode**

## 4 Wires Serial Interface Protocol

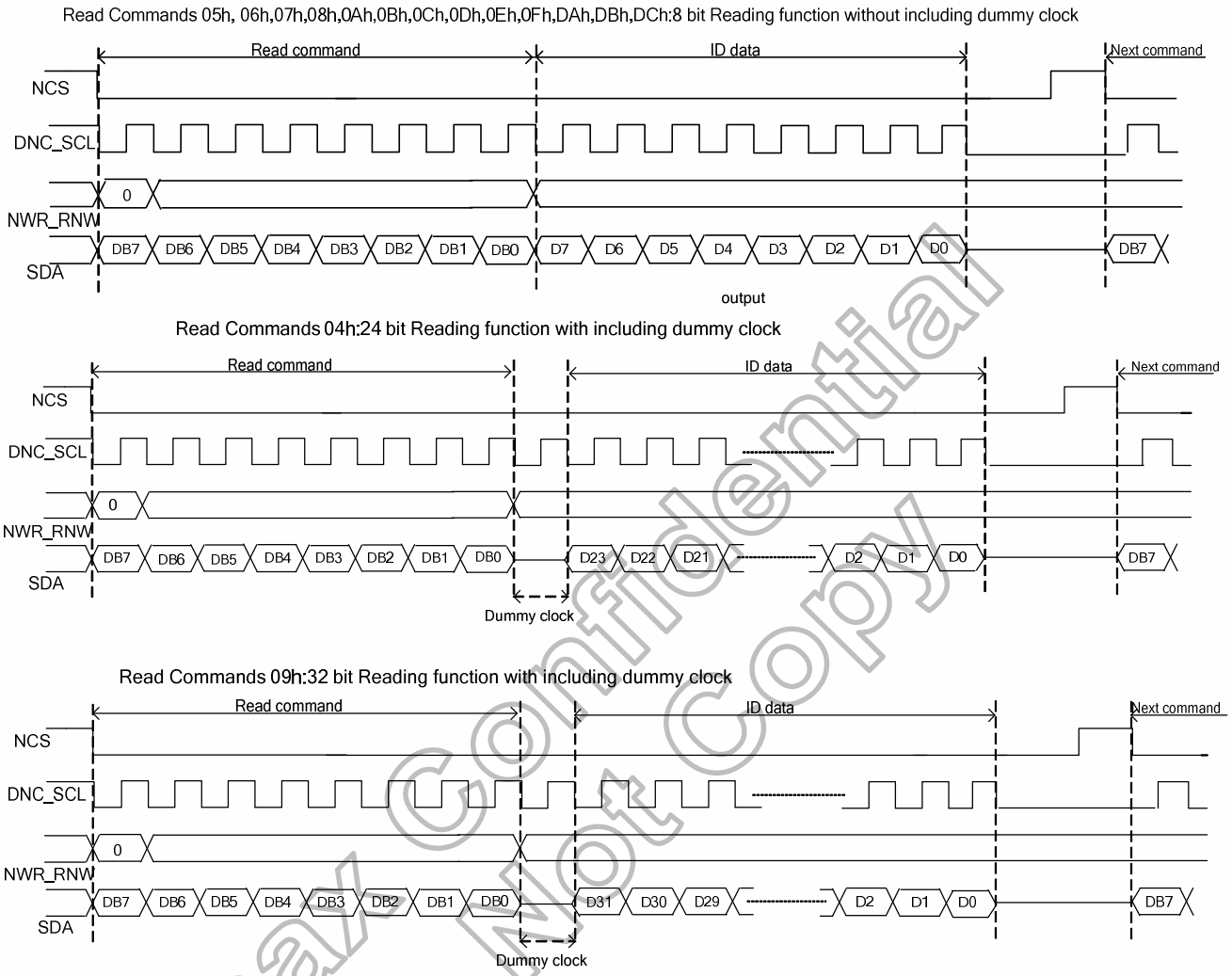



**Figure 5. 24 4 wire Serial Interface protocol, read mode**

There are four types of data format to write display data at Serial data bus Interface and it is the same as 8-bit bus Interface.

The data format that write display data to SRAM at Serial data bus Interface is shown as Figure5. 25 ~ Figure5. 30.

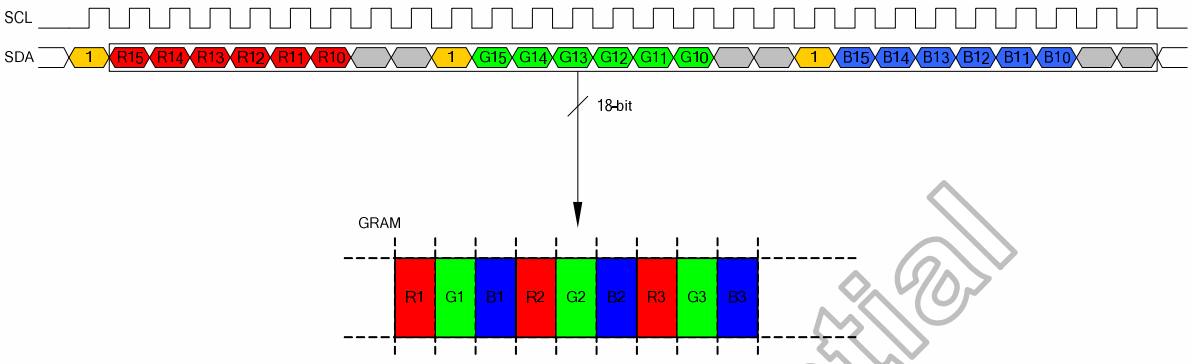



**Figure 5. 25 3W Serial write data for RGB (6-6-6) bits input (LUT_EN=1)**

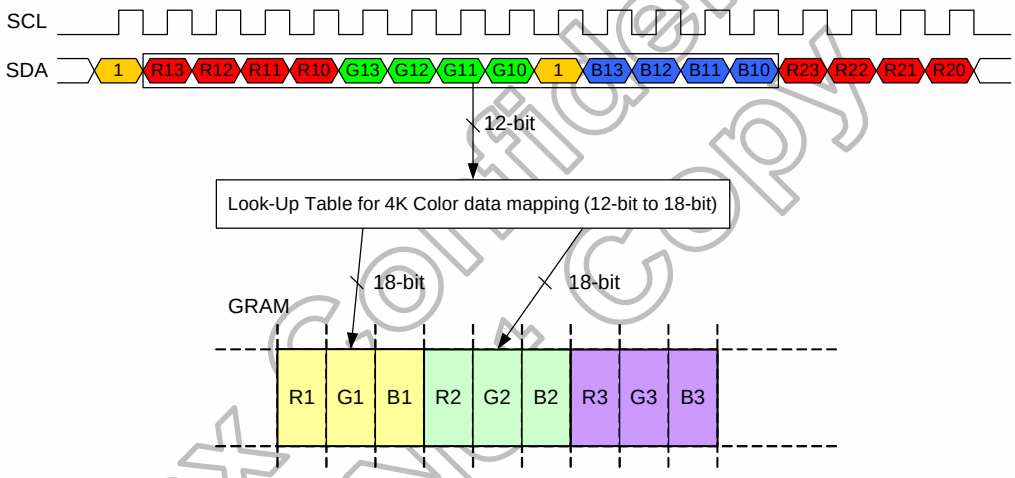



**Figure 5. 26 3W Serial write data for RGB 4-4-4-bits input (support Look-up table and LUT_EN=0)**

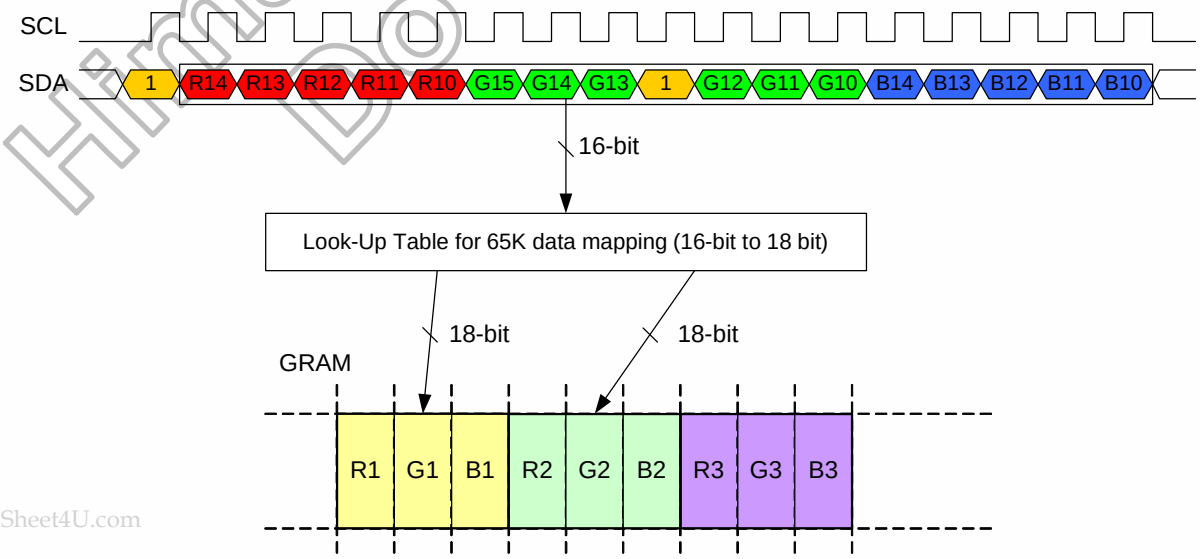



**Figure 5. 27 3W Serial write data for RGB 5-6-5-bits input (support Look-up table and LUT_EN=0)**

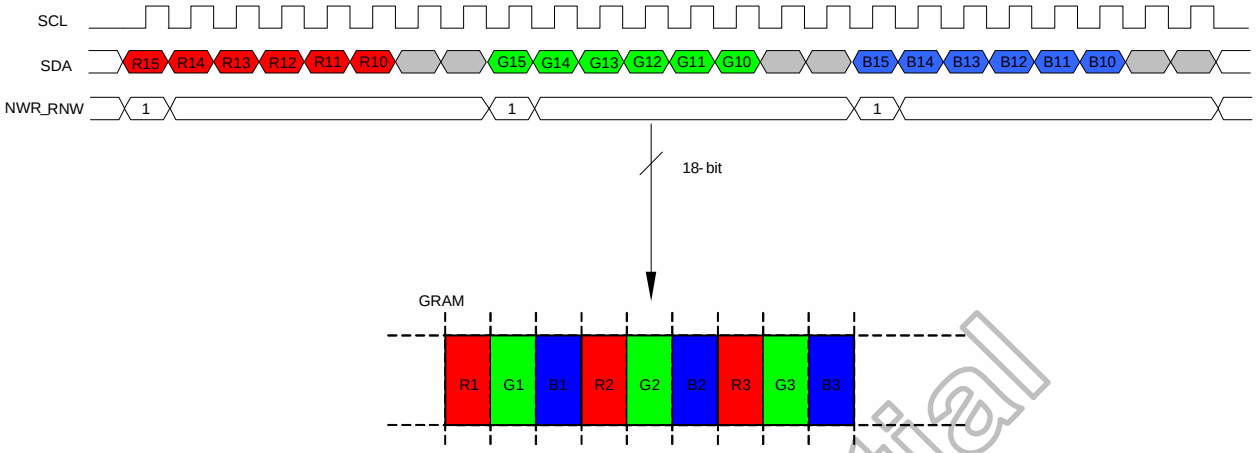



**Figure 5. 28 4W Serial write data for RGB (6-6-6) bits input (LUT_EN=1)**

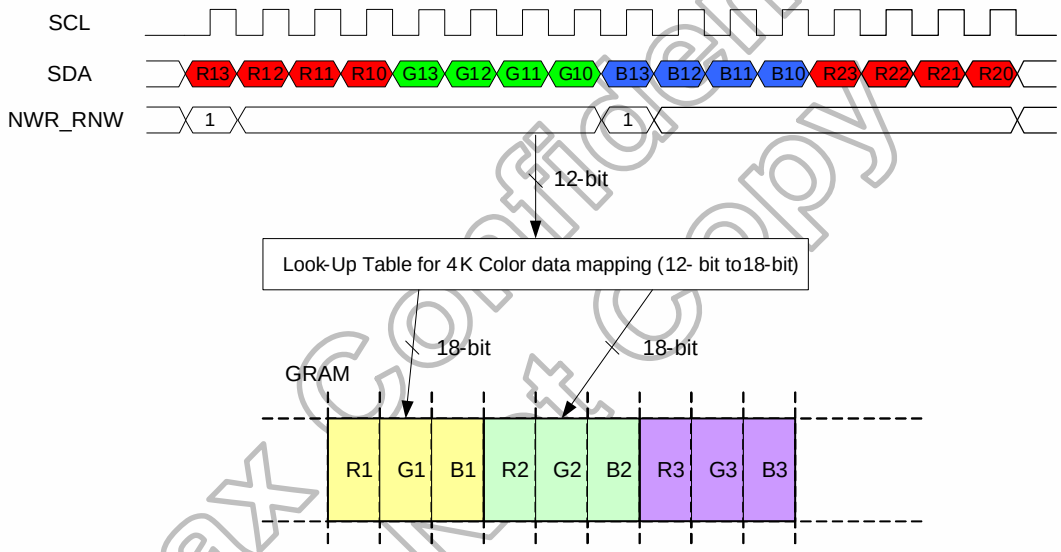



**Figure 5. 29 4W Serial write data for RGB 4-4-4-bits input (support Look-up table and LUT_EN=0)**

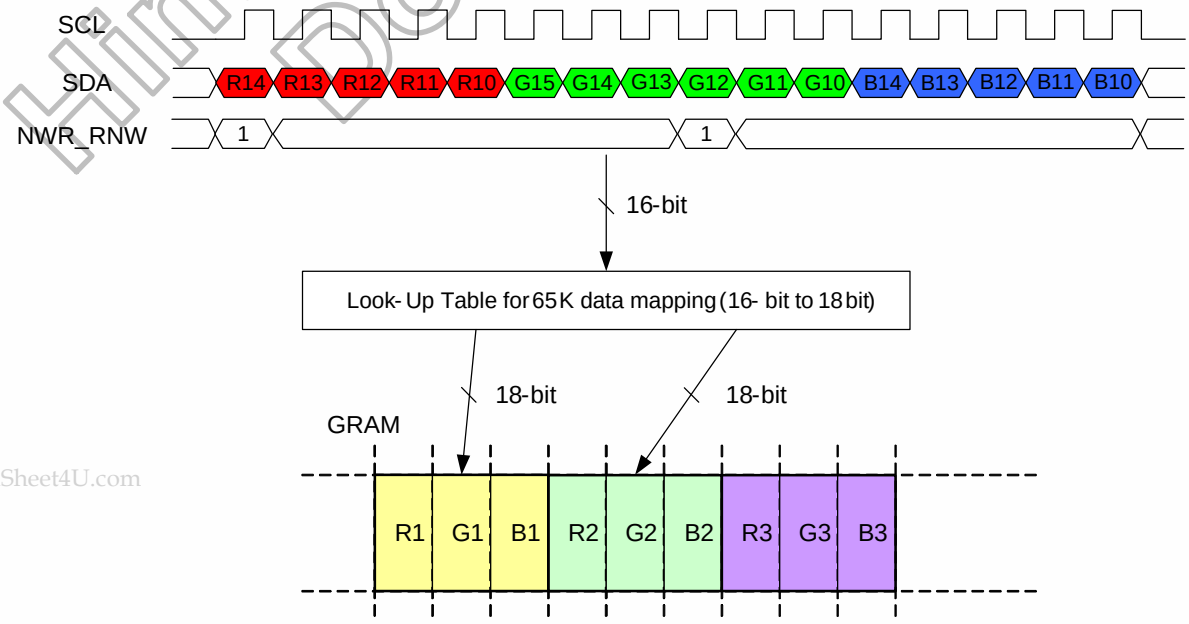



**Figure 5. 30 4W Serial write data for RGB 5-6-5-bits input (support Look-up table and LUT_EN=0)**

### 5.1.3 Display Module Data Transfer Recovery

If there is a break on data transmission when transmitting a command before a whole byte has been completed, then the display module will reset the interface so that it will be ready to receive the same byte re-transmitted when the chip select line (NCS) is next activated. See the following figure.

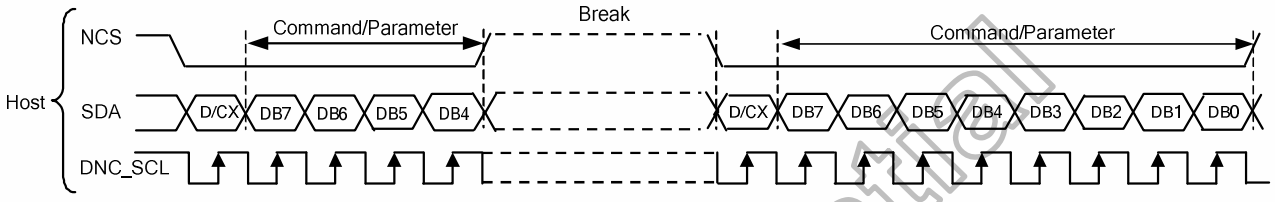
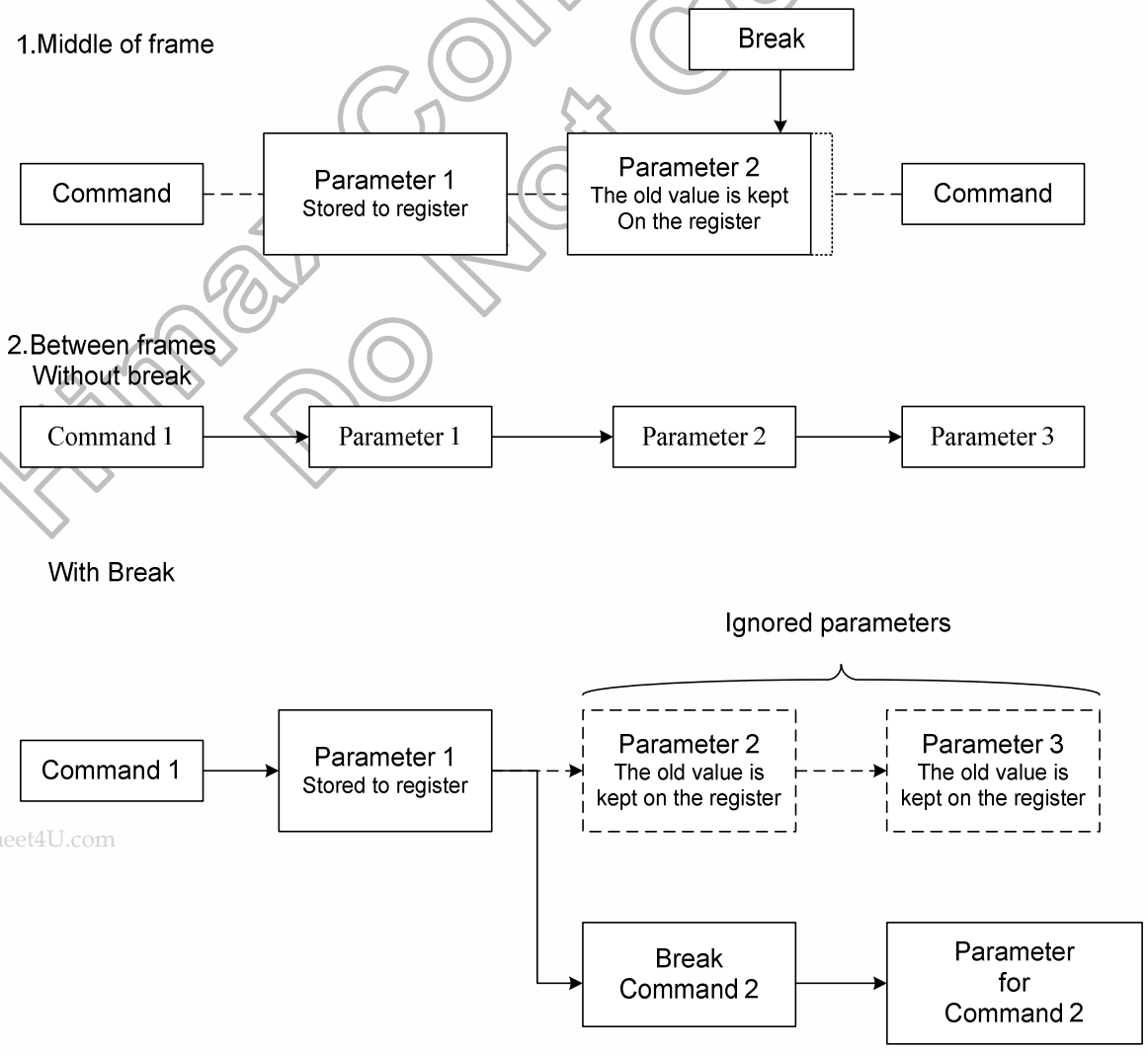



**Figure 5. 31 Display Module Data Transfer Recovery**

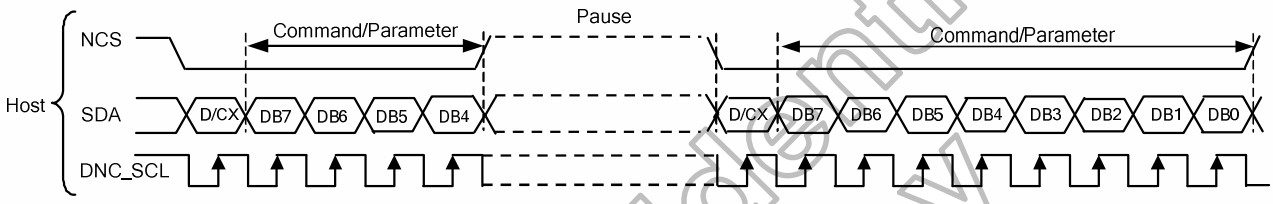
If 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:



### 5.1.4 Display Module Data Transfer Pause

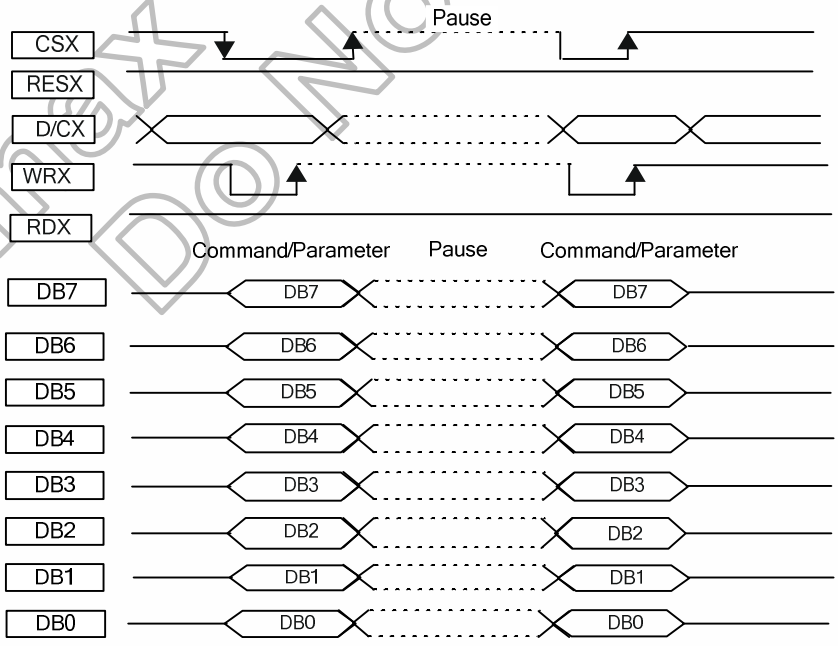
It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

**Serial Interface Pause**




This applies to the following 4 conditions:
a. Command-Pause-Command
b. Command-Pause-Parameter
c. Parameter-Pause-Command
d. Parameter-Pause-Parameter

**Parallel Interface Pause**



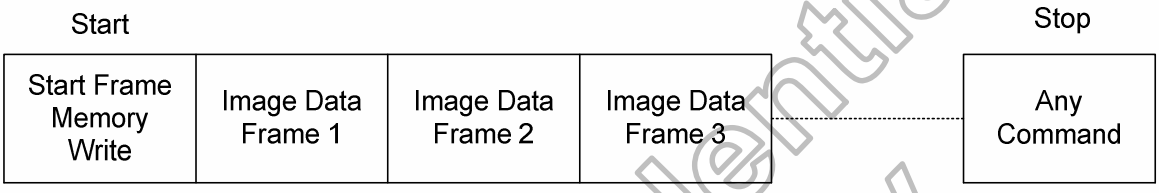



This applies to the following 4 conditions:
a. Command-Pause-Command
b. Command-Pause-Parameter
c. Parameter-Pause-Command
d. Parameter-Pause-Parameter

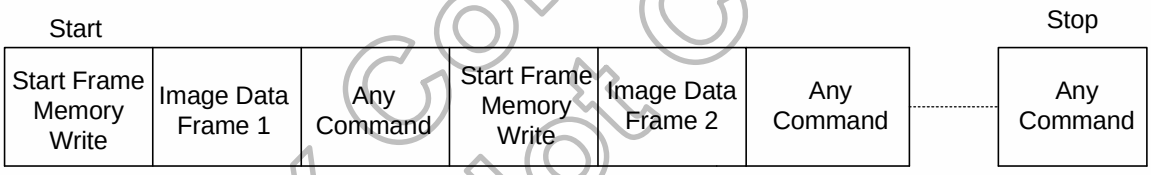
### 5.1.5 Display Module Data Transfer Modes

The Module has three colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1:
The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.




Method 2:
Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.




**Note:** (1) These apply to all Data Transfer Colour modes on both Serial and Parallel interfaces.
(2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

### 5.2 Address Counter (AC)

The HX8353-C contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range X=0~131d (0~83h) and Y=0~161d (0~A1h).
Every time when a pixel data is written/read the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.
To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: SC, end: EC) or the vertical address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

### 5.2.1 MCU to memory write/read direction

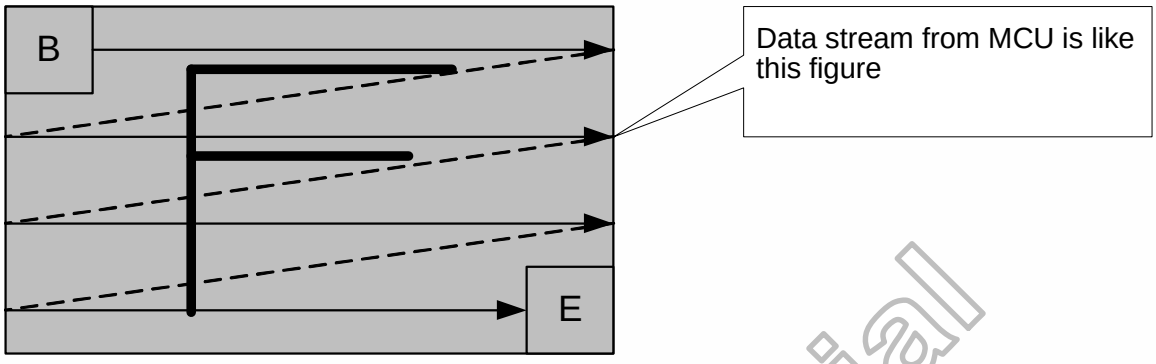



**Figure 5. 32 MCU to memory write/read direction**

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits MY, MX, MV as described below.

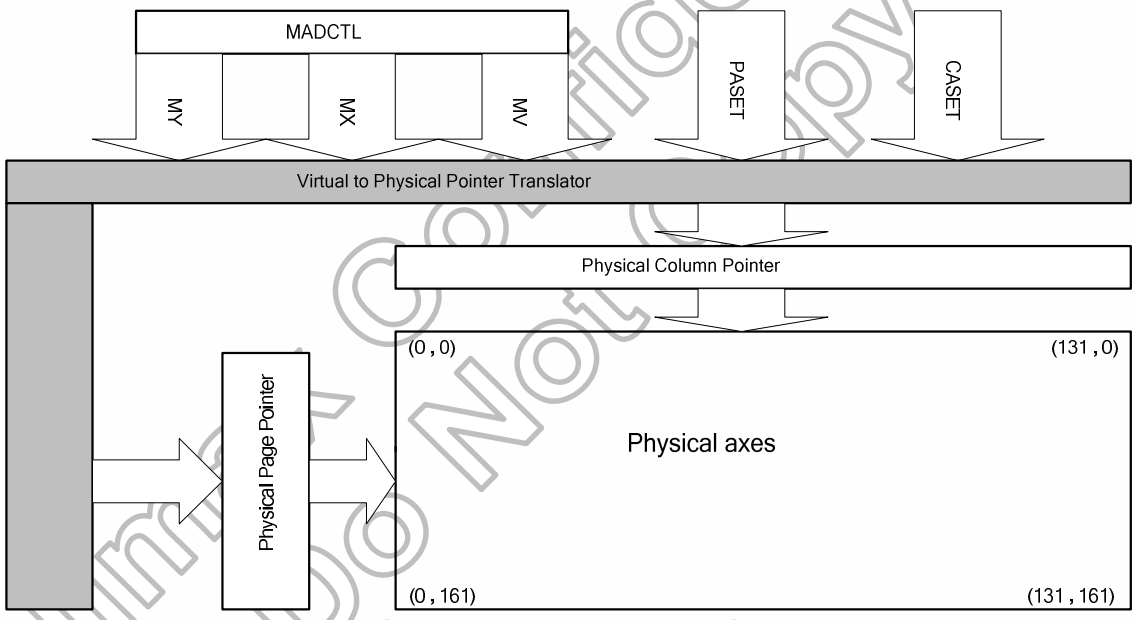



**Figure 5. 33 MY, MX, MV Setting**

| MV | MX | MY | CASET | PASET |
|---|---|---|---|---|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Page Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (161-Physical Page Pointer)<br>Direct to (131-Physical Page Pointer) |
| 0 | 1 | 0 | Direct to (131-Physical Column Pointer) | Direct to Physical Page Pointer |
| 0 | 1 | 1 | Direct to (131-Physical Column Pointer) | Direct to (161-Physical Page Pointer)<br>Direct to (131-Physical Page Pointer) |
| 1 | 0 | 0 | Direct to Physical Page Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (161-Physical Page Pointer)<br>Direct to (131-Physical Page Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Page Pointer | Direct to (131-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (161-Physical Page Pointer)<br>Direct to (131-Physical Page Pointer) | Direct to (131-Physical Column Pointer) |

**Table 5. 5 MY, MX, MV Setting**

The following figure depicts the update method with MV, MX and MY bit

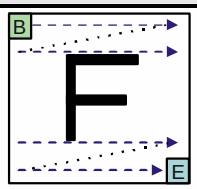
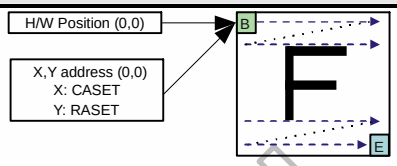
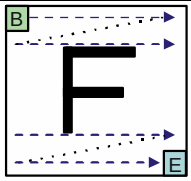
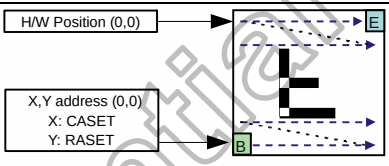
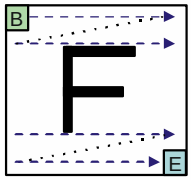
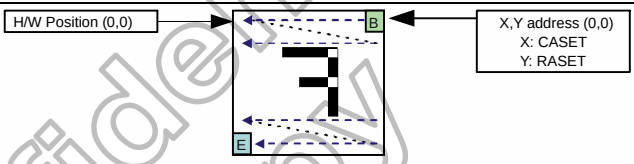
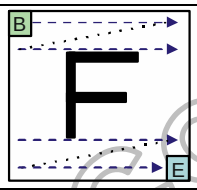
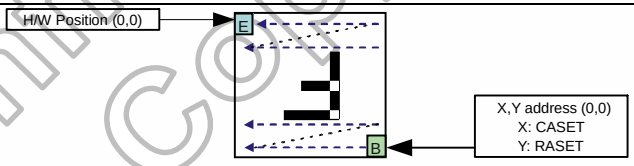
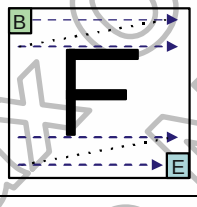
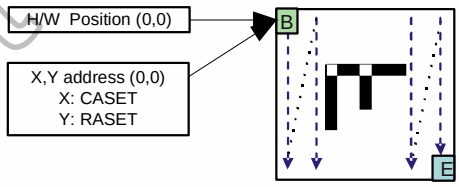
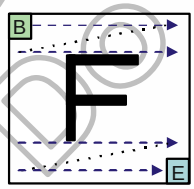
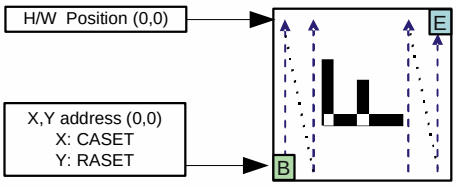
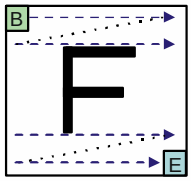
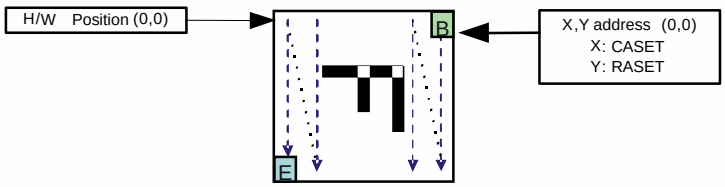
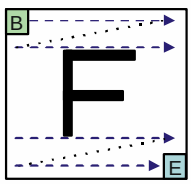
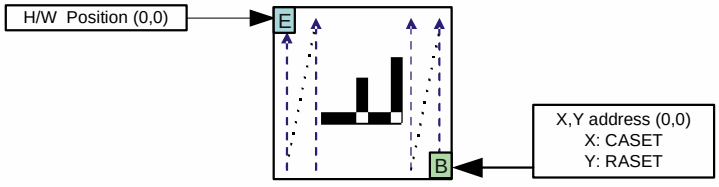
| Display Data Direction | MADCTR parameter | | | Image in the Host | Image in the Driver (GRAM) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 |  |  |
| X-Y Exchange X-Mirror | 1 | 1 | 0 |  |  |
| X-Y Exchange X-Mirror Y-Mirror | 1 | 1 | 1 |  |  |



**Figure 5. 34 Address Direction Settings**

## 5.3 Source, Gate and Memory Map

### 5.3.1 When using 132 x 162 GRAM resolution, display resolution 132RGB x 162 and support S45AP spec (RSO[2:0]=3'b000 & STE_SEL=0)


| Source Out | S1 | S2 | S3 | S4 | S5 | S6 | ---------- | S391 | S392 | S393 | S394 | S395 | S396 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RGB Order —— :RGB=0 ----- :RGB=1 | | | | | | |

| RA | | | | | | | | | | | | | | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MY=0 | MY=1 | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| 0 | 161 | $R0_{5-0}$ | $G0_{5-0}$ | $B0_{5-0}$ | $R1_{5-0}$ | $G1_{5-0}$ | $B1_{5-0}$ | – | $R130_{5-0}$ | $G130_{5-0}$ | $B130_{5-0}$ | $R131_{5-0}$ | $G131_{5-0}$ | $B131_{5-0}$ | 0 | 161 | G1 | G162 |
| 1 | 160 | | | | | | | – | | | | | | | 1 | 160 | G2 | G161 |
| 2 | 159 | | | | | | | – | | | | | | | 2 | 159 | G3 | G160 |
| 3 | 158 | | | | | | | – | | | | | | | 3 | 158 | G4 | G159 |
| 4 | 157 | | | | | | | – | | | | | | | 4 | 157 | G5 | G158 |
| 5 | 156 | | | | | | | – | | | | | | | 5 | 156 | G6 | G157 |
| 6 | 155 | | | | | | | – | | | | | | | 6 | 155 | G7 | G156 |
| 7 | 154 | | | | | | | – | | | | | | | 7 | 154 | G8 | G155 |
| 8 | 153 | | | | | | | – | | | | | | | 8 | 153 | G9 | G154 |
| 9 | 152 | | | | | | | – | | | | | | | 9 | 152 | G10 | G153 |
| 10 | 151 | | | | | | | – | | | | | | | 10 | 151 | G11 | G152 |
| 11 | 150 | | | | | | | – | | | | | | | 11 | 150 | G12 | G151 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : | : | : |
| 154 | 7 | | | | | | | – | | | | | | | 154 | 7 | G155 | G8 |
| 155 | 6 | | | | | | | – | | | | | | | 155 | 6 | G156 | G7 |
| 156 | 5 | | | | | | | – | | | | | | | 156 | 5 | G157 | G6 |
| 157 | 4 | | | | | | | – | | | | | | | 157 | 4 | G158 | G5 |
| 158 | 3 | | | | | | | – | | | | | | | 158 | 3 | G159 | G4 |
| 159 | 2 | | | | | | | – | | | | | | | 159 | 2 | G160 | G3 |
| 160 | 1 | | | | | | | – | | | | | | | 160 | 1 | G161 | G2 |
| 161 | 0 | | | | | | | – | | | | | | | 161 | 0 | G162 | G1 |

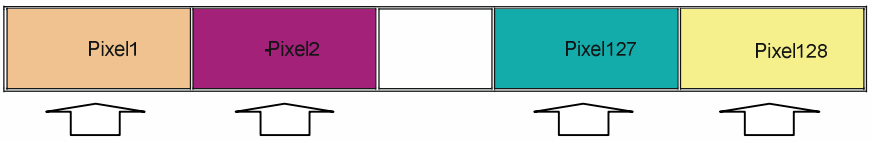
| CA | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MX=0 | 0 | | | 1 | | | 130 | | | 131 | | | |
| | MX=1 | 131 | | | 130 | | | 1 | | | 0 | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 35 Memory Map, 132 x 162 GRAM resolution, display resolution 132RGB x 162**

### 5.3.2 When using 132 x 162 GRAM resolution, display resolution 128RGB x 160 and support S43AP spec (RSO[2:0]=3'b000 & STE_SEL=1)



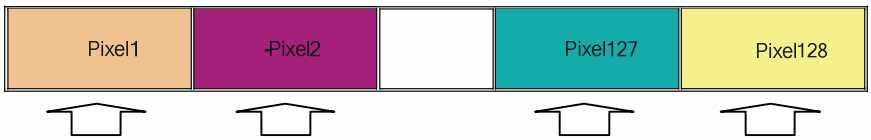

| Source Out | | S7 | S8 | S9 | S10 | S11 | S12 | RGB Order —— :RGB=0 ----- :RGB=1 | S385 | S386 | S387 | S388 | S389 | S390 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| MY=0 | MY=1 | | | | | | | | | | | | | | | | | |
| 0 | 161 | $R0_{5-0}$ | $G0_{5-0}$ | $B0_{5-0}$ | $R1_{5-0}$ | $G1_{5-0}$ | $B1_{5-0}$ | – | $R126_{5-0}$ | $G126_{5-0}$ | $B126_{5-0}$ | $R127_{5-0}$ | $G127_{5-0}$ | $B127_{5-0}$ | 0 | 161 | G2 | G161 |
| 1 | 160 | | | | | | | – | | | | | | | 1 | 160 | G3 | G160 |
| 2 | 159 | | | | | | | – | | | | | | | 2 | 159 | G4 | G159 |
| 3 | 158 | | | | | | | – | | | | | | | 3 | 158 | G5 | G158 |
| 4 | 157 | | | | | | | – | | | | | | | 4 | 157 | G6 | G157 |
| 5 | 156 | | | | | | | – | | | | | | | 5 | 156 | G7 | G156 |
| 6 | 155 | | | | | | | – | | | | | | | 6 | 155 | G8 | G155 |
| 7 | 154 | | | | | | | – | | | | | | | 7 | 154 | G9 | G154 |
| 8 | 153 | | | | | | | – | | | | | | | 8 | 153 | G10 | G153 |
| 9 | 152 | | | | | | | – | | | | | | | 9 | 152 | G11 | G152 |
| 10 | 151 | | | | | | | – | | | | | | | 10 | 151 | G12 | G151 |
| 11 | 150 | | | | | | | – | | | | | | | 11 | 150 | G13 | G150 |
| : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| 154 | 7 | | | | | | | – | | | | | | | 154 | 7 | G154 | G9 |
| 155 | 6 | | | | | | | – | | | | | | | 155 | 6 | G155 | G8 |
| 156 | 5 | | | | | | | – | | | | | | | 156 | 5 | G156 | G7 |
| 157 | 4 | | | | | | | – | | | | | | | 157 | 4 | G157 | G6 |
| 158 | 3 | | | | | | | – | | | | | | | 158 | 3 | G158 | G5 |
| 159 | 2 | | | | | | | – | | | | | | | 159 | 2 | G159 | G4 |
| 160 | 1 | | | | | | | – | | | | | | | 160 | 1 | G160 | G3 |
| 161 | 0 | | | | | | | – | | | | | | | 161 | 0 | G161 | G2 |
| CA | MX=0 | 0 | | | 1 | | | | 126 | | | 127 | | | | | | |
| | MX=1 | 127 | | | 126 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 36 Memory Map, 132 x 162 GRAM resolution ,display resolution 128RGB x 160**

### 5.3.3 When using 128 x 160 GRAM resolution, display resolution 128RGB x 160 and support S44AP spec (RSO[2:0]=3'b011)



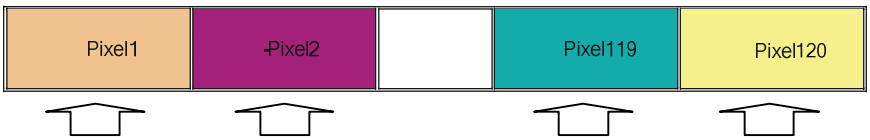

| Source Out | | S7 | S8 | S9 | S10 | S11 | S12 | RGB Order —— :RGB=0 ----- :RGB=1 | S385 | S386 | S387 | S388 | S389 | S390 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | | | | |
| MY=0 | MY=1 | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| 0 | 159 | $R0_{5-0}$ | $G0_{5-0}$ | $B0_{5-0}$ | $R1_{5-0}$ | $G1_{5-0}$ | $B1_{5-0}$ | – | $R126_{5-0}$ | $G126_{5-0}$ | $B126_{5-0}$ | $R127_{5-0}$ | $G127_{5-0}$ | $B127_{5-0}$ | 0 | 159 | G2 | G161 |
| 1 | 158 | | | | | | | – | | | | | | | 1 | 158 | G3 | G160 |
| 2 | 157 | | | | | | | – | | | | | | | 2 | 157 | G4 | G159 |
| 3 | 156 | | | | | | | – | | | | | | | 3 | 156 | G5 | G158 |
| 4 | 155 | | | | | | | – | | | | | | | 4 | 155 | G6 | G157 |
| 5 | 154 | | | | | | | – | | | | | | | 5 | 154 | G7 | G156 |
| 6 | 153 | | | | | | | – | | | | | | | 6 | 153 | G8 | G155 |
| 7 | 152 | | | | | | | – | | | | | | | 7 | 152 | G9 | G154 |
| 8 | 151 | | | | | | | – | | | | | | | 8 | 151 | G10 | G153 |
| 9 | 150 | | | | | | | – | | | | | | | 9 | 150 | G11 | G152 |
| 10 | 149 | | | | | | | – | | | | | | | 10 | 149 | G12 | G151 |
| 11 | 148 | | | | | | | – | | | | | | | 11 | 148 | G13 | G150 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| 152 | 7 | | | | | | | – | | | | | | | 152 | 7 | G154 | G9 |
| 153 | 6 | | | | | | | – | | | | | | | 153 | 6 | G155 | G8 |
| 154 | 5 | | | | | | | – | | | | | | | 154 | 5 | G156 | G7 |
| 155 | 4 | | | | | | | – | | | | | | | 155 | 4 | G157 | G6 |
| 156 | 3 | | | | | | | – | | | | | | | 156 | 3 | G158 | G5 |
| 157 | 2 | | | | | | | – | | | | | | | 157 | 2 | G159 | G4 |
| 158 | 1 | | | | | | | – | | | | | | | 158 | 1 | G160 | G3 |
| 159 | 0 | | | | | | | – | | | | | | | 159 | 0 | G161 | G2 |
| CA | MX=0 | 0 | | | 1 | | | | 126 | | | 127 | | | | | | |
| | MX=1 | 127 | | | 126 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 37 Memory Map, 128 x 160 GRAM resolution, display resolution 128RGB x 160**

### 5.3.4 When using 120 x 160 GRAM resolution, display resolution 120RGB x 160 (RSO[2:0]=3'b010)



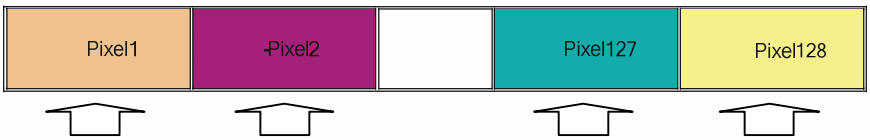

| Source Out | | S7 | S8 | S9 | S10 | S11 | S12 | RGB Order —— :RGB=0 ----- :RGB=1 | S361 | S362 | S363 | S364 | S365 | S366 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| MY=0 | MY=1 | | | | | | | | | | | | | | | | | |
| 0 | 159 | R0$_{5-0}$ | G0$_{5-0}$ | B0$_{5-0}$ | R1$_{5-0}$ | G1$_{5-0}$ | B1$_{5-0}$ | – | R118$_{5-0}$ | G118$_{5-0}$ | B118$_{5-0}$ | R119$_{5-0}$ | G119$_{5-0}$ | B119$_{5-0}$ | 0 | 159 | G2 | G161 |
| 1 | 158 | | | | | | | – | | | | | | | 1 | 158 | G3 | G160 |
| 2 | 157 | | | | | | | – | | | | | | | 2 | 157 | G4 | G159 |
| 3 | 156 | | | | | | | – | | | | | | | 3 | 156 | G5 | G158 |
| 4 | 155 | | | | | | | – | | | | | | | 4 | 155 | G6 | G157 |
| 5 | 154 | | | | | | | – | | | | | | | 5 | 154 | G7 | G156 |
| 6 | 153 | | | | | | | – | | | | | | | 6 | 153 | G8 | G155 |
| 7 | 152 | | | | | | | – | | | | | | | 7 | 152 | G9 | G154 |
| 8 | 151 | | | | | | | – | | | | | | | 8 | 151 | G10 | G153 |
| 9 | 150 | | | | | | | – | | | | | | | 9 | 150 | G11 | G152 |
| 10 | 149 | | | | | | | – | | | | | | | 10 | 149 | G12 | G151 |
| 11 | 148 | | | | | | | – | | | | | | | 11 | 148 | G13 | G150 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| 152 | 7 | | | | | | | – | | | | | | | 152 | 7 | G154 | G9 |
| 153 | 6 | | | | | | | – | | | | | | | 153 | 6 | G155 | G8 |
| 154 | 5 | | | | | | | – | | | | | | | 154 | 5 | G156 | G7 |
| 155 | 4 | | | | | | | – | | | | | | | 155 | 4 | G157 | G6 |
| 156 | 3 | | | | | | | – | | | | | | | 156 | 3 | G158 | G5 |
| 157 | 2 | | | | | | | – | | | | | | | 157 | 2 | G159 | G4 |
| 158 | 1 | | | | | | | – | | | | | | | 158 | 1 | G160 | G3 |
| 159 | 0 | | | | | | | – | | | | | | | 159 | 0 | G161 | G2 |
| CA | MX=0 | 0 | | | 1 | | | | 118 | | | 119 | | | | | | |
| | MX=1 | 119 | | | 118 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 38 Memory Map, 120 x 160 GRAM resolution, display resolution 120RGB x 160**

### 5.3.5 When using 128 x 128 GRAM resolution, display resolution 128RGB x 128 (RSO[2:0]=3'b001)




| Source Out | | S7 | S8 | S9 | S10 | S11 | S12 | RGB Order —— :RGB=0 ----- :RGB=1 | S385 | S386 | S387 | S388 | S389 | S390 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| MY=0 | MY=1 | | | | | | | | | | | | | | | | | |
| 0 | 127 | R0 5-0 | G0 5-0 | B0 5-0 | R1 5-0 | G1 5-0 | B1 5-0 | – | R126 5-0 | G126 5-0 | B126 5-0 | R127 5-0 | G127 5-0 | B127 5-0 | 0 | 127 | G2 | G129 |
| 1 | 126 | | | | | | | – | | | | | | | 1 | 126 | G3 | G128 |
| 2 | 125 | | | | | | | – | | | | | | | 2 | 125 | G4 | G127 |
| 3 | 124 | | | | | | | – | | | | | | | 3 | 124 | G5 | G126 |
| 4 | 123 | | | | | | | – | | | | | | | 4 | 123 | G6 | G125 |
| 5 | 122 | | | | | | | – | | | | | | | 5 | 122 | G7 | G124 |
| 6 | 121 | | | | | | | – | | | | | | | 6 | 121 | G8 | G123 |
| 7 | 120 | | | | | | | – | | | | | | | 7 | 120 | G9 | G122 |
| 8 | 119 | | | | | | | – | | | | | | | 8 | 119 | G10 | G121 |
| 9 | 118 | | | | | | | – | | | | | | | 9 | 118 | G11 | G120 |
| 10 | 117 | | | | | | | – | | | | | | | 10 | 117 | G12 | G119 |
| 11 | 116 | | | | | | | – | | | | | | | 11 | 116 | G13 | G118 |
| : | : | : | : | : | : | : | : | – | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| 120 | 7 | | | | | | | – | | | | | | | 120 | 7 | G122 | G9 |
| 121 | 6 | | | | | | | – | | | | | | | 121 | 6 | G123 | G8 |
| 122 | 5 | | | | | | | – | | | | | | | 122 | 5 | G124 | G7 |
| 123 | 4 | | | | | | | – | | | | | | | 123 | 4 | G125 | G6 |
| 124 | 3 | | | | | | | – | | | | | | | 124 | 3 | G126 | G5 |
| 125 | 2 | | | | | | | – | | | | | | | 125 | 2 | G127 | G4 |
| 126 | 1 | | | | | | | – | | | | | | | 126 | 1 | G128 | G3 |
| 127 | 0 | | | | | | | – | | | | | | | 127 | 0 | G129 | G2 |
| CA | MX=0 | 0 | | | 1 | | | | 126 | | | 127 | | | | | | |
| | MX=1 | 127 | | | 126 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 39 Memory Map, 128 x 128 GRAM resolution, display resolution 128RGB x 128**

### 5.3.6 When using 96 x 68 GRAM resolution, display resolution 96RGB x 68 (RSO[2:0]=3'b100)


| Source Out | | S55 | S56 | S57 | S58 | S59 | S60 | RGB Order :RGB=0 :RGB=1 | S337 | S338 | S339 | S340 | S341 | S342 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| MY=0 | MY=1 | | | | | | | | | | | | | | | | | |
| 0 | 67 | R0 5-0 | G0 5-0 | B0 5-0 | R1 5-0 | G1 5-0 | B1 5-0 | – | R94 5-0 | G94 5-0 | B94 5-0 | R95 5-0 | G95 5-0 | B95 5-0 | 0 | 67 | G1 | G68 |
| 1 | 66 | | | | | | | – | | | | | | | 1 | 66 | G2 | G67 |
| 2 | 65 | | | | | | | – | | | | | | | 2 | 65 | G3 | G66 |
| 3 | 64 | | | | | | | – | | | | | | | 3 | 64 | G4 | G65 |
| 4 | 63 | | | | | | | – | | | | | | | 4 | 63 | G5 | G64 |
| 5 | 62 | | | | | | | – | | | | | | | 5 | 62 | G6 | G63 |
| 6 | 61 | | | | | | | – | | | | | | | 6 | 61 | G7 | G62 |
| 7 | 60 | | | | | | | – | | | | | | | 7 | 60 | G8 | G61 |
| 8 | 59 | | | | | | | – | | | | | | | 8 | 59 | G9 | G60 |
| 9 | 58 | | | | | | | – | | | | | | | 9 | 58 | G10 | G59 |
| 10 | 57 | | | | | | | – | | | | | | | 10 | 57 | G11 | G58 |
| 11 | 56 | | | | | | | – | | | | | | | 11 | 56 | G12 | G57 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| 60 | 7 | | | | | | | – | | | | | | | 60 | 7 | G61 | G8 |
| 61 | 6 | | | | | | | – | | | | | | | 61 | 6 | G62 | G7 |
| 62 | 5 | | | | | | | – | | | | | | | 62 | 5 | G63 | G6 |
| 63 | 4 | | | | | | | – | | | | | | | 63 | 4 | G64 | G5 |
| 64 | 3 | | | | | | | – | | | | | | | 64 | 3 | G65 | G4 |
| 65 | 2 | | | | | | | – | | | | | | | 65 | 2 | G66 | G3 |
| 66 | 1 | | | | | | | – | | | | | | | 66 | 1 | G67 | G2 |
| 67 | 0 | | | | | | | – | | | | | | | 67 | 0 | G68 | G1 |
| CA | MX=0 | 0 | | | 1 | | | | 94 | | | 95 | | | | | | |
| | MX=1 | 95 | | | 94 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 40 Memory Map, 96 x 68 GRAM resolution, display resolution 96RGB x 68**

### 5.3.7 When using 96 x 64 GRAM resolution, display resolution 96RGB x 64 (RSO[2:0]=3'b101)


| Source Out | | S55 | S56 | S57 | S58 | S59 | S60 | RGB Order —— :RGB=0 ----- :RGB=1 | S337 | S338 | S339 | S340 | S341 | S342 | SA | | Gate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | | | | | | | | ML=0 | ML=1 | ML=0 | ML=1 |
| MY=0 | MY=1 | | | | | | | | | | | | | | | | | |
| 0 | 63 | R0 5-0 | G0 5-0 | B0 5-0 | R1 5-0 | G1 5-0 | B1 5-0 | – | R94 5-0 | G94 5-0 | B94 5-0 | R95 5-0 | G95 5-0 | B95 5-0 | 0 | 63 | G1 | G64 |
| 1 | 62 | | | | | | | – | | | | | | | 1 | 62 | G2 | G63 |
| 2 | 61 | | | | | | | – | | | | | | | 2 | 61 | G3 | G62 |
| 3 | 60 | | | | | | | – | | | | | | | 3 | 60 | G4 | G61 |
| 4 | 59 | | | | | | | – | | | | | | | 4 | 59 | G5 | G60 |
| 5 | 58 | | | | | | | – | | | | | | | 5 | 58 | G6 | G59 |
| 6 | 57 | | | | | | | – | | | | | | | 6 | 57 | G7 | G58 |
| 7 | 56 | | | | | | | – | | | | | | | 7 | 56 | G8 | G57 |
| 8 | 55 | | | | | | | – | | | | | | | 8 | 55 | G9 | G56 |
| 9 | 54 | | | | | | | – | | | | | | | 9 | 54 | G10 | G55 |
| 10 | 53 | | | | | | | – | | | | | | | 10 | 53 | G11 | G54 |
| 11 | 52 | | | | | | | – | | | | | | | 11 | 52 | G12 | G53 |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : | : | : | : | : |
| 56 | 7 | | | | | | | – | | | | | | | 56 | 7 | G57 | G8 |
| 57 | 6 | | | | | | | – | | | | | | | 57 | 6 | G58 | G7 |
| 58 | 5 | | | | | | | – | | | | | | | 58 | 5 | G59 | G6 |
| 59 | 4 | | | | | | | – | | | | | | | 59 | 4 | G60 | G5 |
| 60 | 3 | | | | | | | – | | | | | | | 60 | 3 | G61 | G4 |
| 61 | 2 | | | | | | | – | | | | | | | 61 | 2 | G62 | G3 |
| 62 | 1 | | | | | | | – | | | | | | | 62 | 1 | G63 | G2 |
| 63 | 0 | | | | | | | – | | | | | | | 63 | 0 | G64 | G1 |
| CA | MX=0 | 0 | | | 1 | | | | 94 | | | 95 | | | | | | |
| | MX=1 | 95 | | | 94 | | | | 1 | | | 0 | | | | | | |



**Note:** RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

**Figure 5. 41 Memory Map, 96 x 64 GRAM resolution, display resolution 96RGB x 64**

### 5.3.8 Normal Display On or Partial Display On

The HX8353-C has an internal GRAM that store 48,114 bytes bit pattern data, where one pixel is expressed by 18 bits.

#### 5.3.8.1 132X162 GRAM resolution (Size) (display resolution 132RGB x 162 and support S45AP spec (RSO[2:0]=3'b000 & STE_SEL=0)

**(a)Normal Display On**

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | ---------<br>--------- | 80h<br>DB---DB 17 ---0 | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A180H | A181H | A182H | A183H |

| LCD panel S/G pins | S1 | S2 | S3 | --------- | S394 | S395 | S396 |
|---|---|---|---|---|---|---|---|
| G1 | 0000H | | | --------- | 0083H | | |
| G2 | 0100H | | | --------- | 0183H | | |
| G3 | 0200H | | | --------- | 0283H | | |
| G4 | 0300H | | | --------- | 0383H | | |
| G5 | 0400H | | | --------- | 0483H | | |
| G6 | 0500H | | | --------- | 0583H | | |
| ⋮ | ⋮ | | | --------- | ⋮ | | |
| G157 | 9C00H | | | --------- | 9C83H | | |
| G158 | 9DB00H | | | --------- | 9DB83H | | |
| G159 | 9E00H | | | --------- | 9E83H | | |
| G160 | 9F00H | | | --------- | 9F83H | | |
| G161 | A000H | | | --------- | A083H | | |
| G162 | A100H | | | --------- | A183H | | |



**Table 5. 6**

### (b)Partial Display On

PSL[15:0]=02h, PEL[15:0]=9Fh, ML=0.

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | ---------<br>--------- | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A180H | A181H | A182H | A183H |

| | LCD panel S/G pins | S1 | S2 | S3 | --------- | S394 | S395 | S396 |
|---|---|---|---|---|---|---|---|---|
| non-display area 2 lines | G1 | 0000H | | | --------- | 0083H | | |
| | G2 | 0100H | | | --------- | 0183H | | |
| Display area 158 lines | G3 | 0200H | | | --------- | 0283H | | |
| | G4 | 0300H | | | --------- | 0383H | | |
| | G5 | 0400H | | | --------- | 0483H | | |
| | G6 | 0500H | | | --------- | 0583H | | |
| | ⋮ | ⋮ | | | --------- | ⋮ | | |
| | G157 | 9C00H | | | --------- | 9C83H | | |
| | G158 | 9DB00H | | | --------- | 9DB83H | | |
| Non-display area 2 lines | G159 | 9E00H | | | --------- | 9E83H | | |
| | G160 | 9F00H | | | --------- | 9F83H | | |
| | G161 | A000H | | | --------- | A083H | | |
| | G162 | A100H | | | --------- | A183H | | |

**Table 5. 7**

### 5.3.8.2 132X162 GRAM resolution (Size) (display resolution 128RGB x 160 and support S43AP spec (RSO[2:0]=3'b000 & STE_SEL=1)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h | 01h | 02h | 03h | --------- | 80h | 81h | 82h | 83h |
|---|---|---|---|---|---|---|---|---|---|
| | DB---DB 17 ---0 | DB---DB 17 ---0 | DB---DB 17 ---0 | DB---DB 17 ---0 | --------- | DB---DB 17 ---0 | DB---DB 17 ---0 | DB---DB 17 ---0 | DB---DB 17 ---0 |
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A180H | A181H | A182H | A183H |

| LCD panel S/G pins | S7 | S8 | S9 | --------- | S388 | S389 | S390 |
|---|---|---|---|---|---|---|---|
| G2 | 0000H | | | --------- | 0181H | | |
| G3 | 0100H | | | --------- | 0281H | | |
| G4 | 0200H | | | --------- | 0381H | | |
| G5 | 0300H | | | --------- | 0481H | | |
| G6 | 0400H | | | --------- | 0581H | | |
| G7 | 0500H | | | --------- | 0681H | | |
| ⋮ | ⋮ | | | --------- | ⋮ | | |
| G158 | 9C00H | | | --------- | 9DB81H | | |
| G159 | 9DB00H | | | --------- | 9E81H | | |
| G160 | 9E00H | | | --------- | 9F81H | | |
| G161 | 9F00H | | | --------- | A081H | | |

**Table 5. 8**

### (b)Partial Display On

PSL[15:0]=03h, PEL[15:0]=9Eh, ML=0.

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | ---------<br>--------- | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|
| **00h** | 0000H | 0001H | 0002H | 0003H | --------- | 0080H | 0081H | 0082H | 0083H |
| **01h** | 0100H | 0101H | 0102H | 0103H | --------- | 0180H | 0181H | 0182H | 0183H |
| **02h** | 0200H | 0201H | 0202H | 0203H | --------- | 0280H | 0281H | 0282H | 0283H |
| **03h** | 0300H | 0301H | 0302H | 0303H | --------- | 0380H | 0381H | 0382H | 0383H |
| **04h** | 0400H | 0401H | 0402H | 0403H | --------- | 0480H | 0481H | 0482H | 0483H |
| **05h** | 0500H | 0501H | 0502H | 0503H | --------- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ |
| **9Ch** | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C80H | 9C81H | 9C82H | 9C83H |
| **9Dh** | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| **9Eh** | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E80H | 9E81H | 9E82H | 9E83H |
| **9Fh** | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F80H | 9F81H | 9F82H | 9F83H |
| **A0h** | A000H | A001H | A002H | A003H | --------- | A080H | A081H | A082H | A083H |
| **A1h** | A100H | A101H | A102H | A103H | --------- | A180H | A181H | A182H | A183H |

| | LCD panel S/G pins | S7 | S8 | S9 | --------- | S388 | S389 | S390 |
|---|---|---|---|---|---|---|---|---|
| non-display area 2 lines | **G2** | 0102H | | | --------- | 0181H | | |
| | **G3** | 0202H | | | --------- | 0281H | | |
| Display area 156 lines | **G4** | 0302H | | | --------- | 0381H | | |
| | **G5** | 0402H | | | --------- | 0481H | | |
| | **G6** | 0502H | | | --------- | 0581H | | |
| | **G7** | 0602H | | | --------- | 0681H | | |
| | ⋮ | ⋮ | | | --------- | ⋮ | | |
| Non-display area 2 lines | **G158** | 9DB02H | | | --------- | 9DB81H | | |
| | **G159** | 9E02H | | | --------- | 9E81H | | |
| | **G160** | 9F02H | | | --------- | 9F81H | | |
| | **G161** | A002H | | | --------- | A081H | | |

**Table 5. 9**

### 5.3.8.3 128X160 GRAM resolution (Size) (display resolution 128RGB x 160 and support S44AP spec (RSO[2:0]=3'b011)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | ---------<br>--------- | 7Fh<br>DB---DB<br>17 ---0 | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 007FH | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 017FH | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 027FH | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 037FH | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 047FH | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 057FH | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C7FH | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB7FH | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E7FH | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F7FH | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A07FH | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A17FH | A180H | A181H | A182H | A183H |

| LCD panel S/G pins | S7 | S8 | S9 | --------- | S388 | S389 | S390 |
|---|---|---|---|---|---|---|---|
| G2 | 0000H | | | --------- | 007FH | | |
| G3 | 0100H | | | --------- | 017FH | | |
| G4 | 0200H | | | --------- | 027FH | | |
| G5 | 0300H | | | --------- | 037FH | | |
| G6 | 0400H | | | --------- | 047FH | | |
| G7 | 0500H | | | --------- | 057FH | | |
| ⋮ | ⋮ | | | --------- | ⋮ | | |
| G158 | 9C00H | | | --------- | 9C7FH | | |
| G159 | 9DB00H | | | --------- | 9DB7FH | | |
| G160 | 9E00H | | | --------- | 9E7FH | | |
| G161 | 9F00H | | | --------- | 9F7FH | | |

**Table 5. 10**

### (b)Partial Display On

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | ---------<br>--------- | 7Fh<br>DB---DB 17 ---0 | 80h<br>DB---DB 17 ---0 | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 007FH | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 017FH | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 027FH | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 037FH | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 047FH | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 057FH | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C7FH | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB7FH | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E7FH | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F7FH | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A07FH | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A17FH | A180H | A181H | A182H | A183H |

| | LCD panel S/G pins | S7 | S8 | S9 | --------- | S388 | S389 | S390 |
|---|---|---|---|---|---|---|---|---|
| non-display area 2 lines | G2 | 0000H | | | --------- | 007FH | | |
| | G3 | 0100H | | | --------- | 017FH | | |
| Display area 156 lines | G4 | 0200H | | | --------- | 027FH | | |
| | G5 | 0300H | | | --------- | 037FH | | |
| | G6 | 0400H | | | --------- | 047FH | | |
| | G7 | 0500H | | | --------- | 057FH | | |
| | ⋮ | ⋮ | | | --------- | ⋮ | | |
| | G158 | 9C00H | | | --------- | 9C7FH | | |
| Non-display area 2 lines | G159 | 9DB00H | | | --------- | 9DB7FH | | |
| | G160 | 9E00H | | | --------- | 9E7FH | | |
| | G161 | 9F00H | | | --------- | 9F7FH | | |

**Table 5. 11**

### 5.3.8.4 120X160 GRAM resolution (Size) (display resolution 120RGB x 160 → RSO[2:0]=3'b001)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | --------- | 77h<br>DB---DB 17 ---0 | --------- | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 0077H | --------- | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 0177H | --------- | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 0277H | --------- | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 0377H | --------- | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 0477H | --------- | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 0577H | --------- | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C77H | --------- | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB77H | --------- | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E77H | --------- | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F77H | --------- | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A077H | --------- | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A177H | --------- | A181H | A182H | A183H |

| LCD panel S/G pins | S7 | S8 | S9 | --------- | S364 | S365 | S366 |
|---|---|---|---|---|---|---|---|
| G2 | 0000H | | | --------- | 0077H | | |
| G3 | 0100H | | | --------- | 0177H | | |
| G4 | 0200H | | | --------- | 0277H | | |
| G5 | 0300H | | | --------- | 0377H | | |
| G6 | 0400H | | | --------- | 0477H | | |
| G7 | 0500H | | | --------- | 0577H | | |
| ⋮ | ⋮ | | | --------- | ⋮ | | |
| G158 | 9C00H | | | --------- | 9C77H | | |
| G159 | 9DB00H | | | --------- | 9DB77H | | |
| G160 | 9E00H | | | --------- | 9E77H | | |
| G161 | 9F00H | | | --------- | 9F77H | | |

**Table 5. 12**

### (b)Partial Display On

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | --------- | 77h<br>DB---DB 17 ---0 | --------- | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 0077H | --------- | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 0177H | --------- | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 0277H | --------- | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 0377H | --------- | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 0477H | --------- | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 0577H | --------- | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C77H | --------- | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB77H | --------- | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E77H | --------- | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F77H | --------- | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A077H | --------- | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A177H | --------- | A181H | A182H | A183H |

| | LCD panel S/G pins | S7 | S8 | S9 | --------- | S364 | S365 | S366 |
|---|---|---|---|---|---|---|---|---|
| non-display area 2 lines | G2 | 0000H | | | --------- | 0077H | | |
| | G3 | 0100H | | | --------- | 0177H | | |
| Display area 156 lines | G4 | 0200H | | | --------- | 0277H | | |
| | G5 | 0300H | | | --------- | 0377H | | |
| | G6 | 0400H | | | --------- | 0477H | | |
| | G7 | 0500H | | | --------- | 0577H | | |
| | ⋮ | ⋮ | | | --------- | ⋮ | | |
| | G158 | 9C00H | | | --------- | 9C77H | | |
| Non-display area 2 lines | G159 | 9DB00H | | | --------- | 9DB77H | | |
| | G160 | 9E00H | | | --------- | 9E77H | | |
| | G161 | 9F00H | | | --------- | 9F77H | | |

**Table 5. 13**

### 5.3.7.5 128X128 GRAM resolution (Size) (display resolution 128RGB x 128 → RSO[2:0]=3'b010)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 7Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | --------- | 7Fh<br>DB---DB 17 ---0 | --------- | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --------- | 007FH | --------- | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --------- | 017FH | --------- | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --------- | 027FH | --------- | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --------- | 037FH | --------- | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --------- | 047FH | --------- | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --------- | 057FH | --------- | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| 7Eh | 7E00H | 7E01H | 7E02H | 7E03H | --------- | 7E7FH | --------- | 7E81H | 7E82H | 7E83H |
| 7Fh | 7F00H | 7F01H | 7F02H | 7F03H | --------- | 7E7FH | --------- | 7F81H | 7F82H | 7F83H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C7FH | --------- | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB7FH | --------- | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E7FH | --------- | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F7FH | --------- | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --------- | A07FH | --------- | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --------- | A17FH | --------- | A181H | A182H | A183H |

| LCD panel S/G pins | S7 | S8 | S9 | --------- | S388 | S389 | S390 |
|---|---|---|---|---|---|---|---|
| G2 | 0000H | | | --------- | 007FH | | |
| G3 | 0100H | | | --------- | 017FH | | |
| G4 | 0200H | | | --------- | 027FH | | |
| G5 | 0300H | | | --------- | 037FH | | |
| G6 | 0400H | | | --------- | 047FH | | |
| G7 | 0500H | | | --------- | 057FH | | |
| ⋮ | ⋮ | | | --------- | ⋮ | | |
| G126 | 9C00H | | | --------- | 9C7FH | | |
| G127 | 9DB00H | | | --------- | 9DB7FH | | |
| G128 | 9E00H | | | --------- | 9E7FH | | |
| G129 | 9F00H | | | --------- | 9F7FH | | |

**Table 5. 14**

### (b)Partial Display On

PSL[15:0]=02h, PEL[15:0]=7Dh, ML=0.

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | --------- | 7Fh<br>DB---DB 17 ---0 | --------- | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **00h** | 0000H | 0001H | 0002H | 0003H | --------- | 007FH | --------- | 0081H | 0082H | 0083H |
| **01h** | 0100H | 0101H | 0102H | 0103H | --------- | 017FH | --------- | 0181H | 0182H | 0183H |
| **02h** | 0200H | 0201H | 0202H | 0203H | --------- | 027FH | --------- | 0281H | 0282H | 0283H |
| **03h** | 0300H | 0301H | 0302H | 0303H | --------- | 037FH | --------- | 0381H | 0382H | 0383H |
| **04h** | 0400H | 0401H | 0402H | 0403H | --------- | 047FH | --------- | 0481H | 0482H | 0483H |
| **05h** | 0500H | 0501H | 0502H | 0503H | --------- | 057FH | --------- | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| **7Eh** | 7E00H | 7E01H | 7E02H | 7E03H | --------- | 7E7FH | --------- | 7E81H | 7E82H | 7E83H |
| **7Fh** | 7F00H | 7F01H | 7F02H | 7F03H | --------- | 7E7FH | --------- | 7F81H | 7F82H | 7F83H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --------- | ⋮ | --------- | ⋮ | ⋮ | ⋮ |
| **9Ch** | 9C00H | 9C01H | 9C02H | 9C03H | --------- | 9C7FH | --------- | 9C81H | 9C82H | 9C83H |
| **9Dh** | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --------- | 9DB7FH | --------- | 9DB81H | 9DB82H | 9DB83H |
| **9Eh** | 9E00H | 9E01H | 9E02H | 9E03H | --------- | 9E7FH | --------- | 9E81H | 9E82H | 9E83H |
| **9Fh** | 9F00H | 9F01H | 9F02H | 9F03H | --------- | 9F7FH | --------- | 9F81H | 9F82H | 9F83H |
| **A0h** | A000H | A001H | A002H | A003H | --------- | A07FH | --------- | A081H | A082H | A083H |
| **A1h** | A100H | A101H | A102H | A103H | --------- | A17FH | --------- | A181H | A182H | A183H |

| | LCD panel S/G pins | S7 | S8 | S9 | --------- | S387 | S389 | S390 |
|---|---|---|---|---|---|---|---|---|
| non-display area 2 lines | **G2** | 0000H | | | --------- | 007FH | | |
| | **G3** | 0100H | | | --------- | 017FH | | |
| Display area 124 lines | **G4** | 0200H | | | --------- | 027FH | | |
| | **G5** | 0300H | | | --------- | 037FH | | |
| | **G6** | 0400H | | | --------- | 047FH | | |
| | **G7** | 0500H | | | --------- | 057FH | | |
| | ⋮ | ⋮ | | | --------- | ⋮ | | |
| Non-display area 2 lines | **G158** | 7C00H | | | --------- | 7C7FH | | |
| | **G159** | 7DB00H | | | --------- | 7DB7FH | | |
| | **G160** | 7E00H | | | --------- | 7E7FH | | |
| | **G161** | 7F00H | | | --------- | 7F7FH | | |

**Table 5. 15**

### 5.3.8.6 96x68 resolution (RSO[2:0]=3'b100)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | --- | 5Dh<br>DB---DB<br>17 ---0 | 5Eh<br>DB---DB<br>17 ---0 | 5Fh<br>DB---DB<br>17 ---0 | --- | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **00h** | 0000H | 0001H | 0002H | 0003H | --- | 005DH | 005EH | 005FH | --- | 0080H | 0081H | 0082H | 0083H |
| **01h** | 0100H | 0101H | 0102H | 0103H | --- | 015DH | 015EH | 015FH | --- | 0180H | 0181H | 0182H | 0183H |
| **02h** | 0200H | 0201H | 0202H | 0203H | --- | 025DH | 025EH | 025FH | --- | 0280H | 0281H | 0282H | 0283H |
| **03h** | 0300H | 0301H | 0302H | 0303H | --- | 035DH | 035EH | 035FH | --- | 0380H | 0381H | 0382H | 0383H |
| **04h** | 0400H | 0401H | 0402H | 0403H | --- | 045DH | 045EH | 045FH | --- | 0480H | 0481H | 0482H | 0483H |
| **05h** | 0500H | 0501H | 0502H | 0503H | --- | 055DH | 055EH | 055FH | --- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **41h** | 4100H | 4101H | 4102H | 4103H | --- | 415DH | 415EH | 415FH | --- | 4180H | 4181H | 4182H | 4183H |
| **42h** | 4200H | 4201H | 4102H | 4103H | --- | 425DH | 425EH | 425FH | --- | 4280H | 4281H | 4282H | 4283H |
| **43h** | 4300H | 4301H | 4302H | 4303H | --- | 435DH | 435EH | 435FH | --- | 4380H | 4381H | 4382H | 4383H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **9Ch** | 9C00H | 9C01H | 9C02H | 9C03H | --- | 9C5DH | 9C5EH | 9C5FH | --- | 9C80H | 9C81H | 9C82H | 9C83H |
| **9Dh** | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --- | 9DB5DH | 9DB5EH | 9DB5FH | --- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| **9Eh** | 9E00H | 9E01H | 9E02H | 9E03H | --- | 9E5DH | 9E5EH | 9E5FH | --- | 9E80H | 9E81H | 9E82H | 9E83H |
| **9Fh** | 9F00H | 9F01H | 9F02H | 9F03H | --- | 9F5DH | 9F5EH | 9F5FH | --- | 9F80H | 9F81H | 9F82H | 9F83H |
| **A0h** | A000H | A001H | A002H | A003H | --- | A05DH | A05EH | A05FH | --- | A080H | A081H | A082H | A083H |
| **A1h** | A100H | A101H | A102H | A103H | --- | A15DH | A15EH | A15FH | --- | A180H | A181H | A182H | A183H |

| LCD panel S/G pins | S55 | S56 | S57 | | S340 | S341 | S342 |
|---|---|---|---|---|---|---|---|
| **G1** | 0000H | | | --------- | 005FH | | |
| **G2** | 0100H | | | --------- | 015FH | | |
| **G3** | 0200H | | | --------- | 025FH | | |
| **G4** | 0300H | | | --------- | 035FH | | |
| **G5** | 0400H | | | --------- | 045FH | | |
| **G6** | 0500H | | | --------- | 055FH | | |
| ⋮ | ⋮ | | | ⋮ | ⋮ | | |
| **G67** | 4200H | | | --------- | 425FH | | |
| **G68** | 4300H | | | --------- | 435FH | | |

**Table 5. 16**

### (b)Partial Display On

PSL[15:0]=02, PEL[15:0]=41, ML=0.

| GRAM | 00h<br>DB---DB 17 ---0 | 01h<br>DB---DB 17 ---0 | 02h<br>DB---DB 17 ---0 | 03h<br>DB---DB 17 ---0 | ---<br>--- | 5Dh<br>DB---DB 17 ---0 | 5Eh<br>DB---DB 17 ---0 | 5Fh<br>DB---DB 17 ---0 | ---<br>--- | 80h<br>DB---DB 17 ---0 | 81h<br>DB---DB 17 ---0 | 82h<br>DB---DB 17 ---0 | 83h<br>DB---DB 17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 0000H | 0001H | 0002H | 0003H | --- | 005DH | 005EH | 005FH | --- | 0080H | 0081H | 0082H | 0083H |
| 01h | 0100H | 0101H | 0102H | 0103H | --- | 015DH | 015EH | 015FH | --- | 0180H | 0181H | 0182H | 0183H |
| 02h | 0200H | 0201H | 0202H | 0203H | --- | 025DH | 025EH | 025FH | --- | 0280H | 0281H | 0282H | 0283H |
| 03h | 0300H | 0301H | 0302H | 0303H | --- | 035DH | 035EH | 035FH | --- | 0380H | 0381H | 0382H | 0383H |
| 04h | 0400H | 0401H | 0402H | 0403H | --- | 045DH | 045EH | 045FH | --- | 0480H | 0481H | 0482H | 0483H |
| 05h | 0500H | 0501H | 0502H | 0503H | --- | 055DH | 055EH | 055FH | --- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| 41h | 4100H | 4101H | 4102H | 4103H | --- | 415DH | 415EH | 415FH | --- | 4180H | 4181H | 4182H | 4183H |
| 42h | 4200H | 4201H | 4202H | 4203H | --- | 425DH | 425EH | 425FH | --- | 4280H | 4281H | 4282H | 4283H |
| 43h | 4300H | 4301H | 4302H | 4303H | --- | 435DH | 435EH | 435FH | --- | 4380H | 4381H | 4382H | 4383H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| 9Ch | 9C00H | 9C01H | 9C02H | 9C03H | --- | 9C5DH | 9C5EH | 9C5FH | --- | 9C80H | 9C81H | 9C82H | 9C83H |
| 9Dh | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --- | 9DB5DH | 9DB5EH | 9DB5FH | --- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| 9Eh | 9E00H | 9E01H | 9E02H | 9E03H | --- | 9E5DH | 9E5EH | 9E5FH | --- | 9E80H | 9E81H | 9E82H | 9E83H |
| 9Fh | 9F00H | 9F01H | 9F02H | 9F03H | --- | 9F5DH | 9F5EH | 9F5FH | --- | 9F80H | 9F81H | 9F82H | 9F83H |
| A0h | A000H | A001H | A002H | A003H | --- | A05DH | A05EH | A05FH | --- | A080H | A081H | A082H | A083H |
| A1h | A100H | A101H | A102H | A103H | --- | A15DH | A15EH | A15FH | --- | A180H | A181H | A182H | A183H |

| | LCD panel S/G pins | S55 | S56 | S57 | | S340 | S341 | S342 |
|---|---|---|---|---|---|---|---|---|
| Non-display area 2 lines | G1 | 0000H | | | --------- | | 005FH | |
| | G2 | 0100H | | | --------- | | 015FH | |
| Display area 64 lines | G3 | 0200H | | | --------- | | 025FH | |
| | G4 | 0300H | | | --------- | | 035FH | |
| | G5 | 0400H | | | --------- | | 045FH | |
| | G6 | 0500H | | | --------- | | 055FH | |
| | ⋮ | ⋮ | | | ⋮ | | ⋮ | |
| | G66 | 4100H | | | --------- | | 415FH | |
| Non-display area 2 lines | G67 | 4200H | | | --------- | | 425FH | |
| | G68 | 4300H | | | --------- | | 435FH | |

**Table 5. 17**

### 5.3.8.7 96x64 resolution (RSO[2:0]=3'b101)

#### (a)Normal Display On

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | --- | 5Dh<br>DB---DB<br>17 ---0 | 5Eh<br>DB---DB<br>17 ---0 | 5Fh<br>DB---DB<br>17 ---0 | --- | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **00h** | 0000H | 0001H | 0002H | 0003H | --- | 005DH | 005EH | 005FH | --- | 0080H | 0081H | 0082H | 0083H |
| **01h** | 0100H | 0101H | 0102H | 0103H | --- | 015DH | 015EH | 015FH | --- | 0180H | 0181H | 0182H | 0183H |
| **02h** | 0200H | 0201H | 0202H | 0203H | --- | 025DH | 025EH | 025FH | --- | 0280H | 0281H | 0282H | 0283H |
| **03h** | 0300H | 0301H | 0302H | 0303H | --- | 035DH | 035EH | 035FH | --- | 0380H | 0381H | 0382H | 0383H |
| **04h** | 0400H | 0401H | 0402H | 0403H | --- | 045DH | 045EH | 045FH | --- | 0480H | 0481H | 0482H | 0483H |
| **05h** | 0500H | 0501H | 0502H | 0503H | --- | 055DH | 055EH | 055FH | --- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **3Fh** | 3F00H | 3F01H | 3F02H | 3F03H | --- | 3F5DH | 3F5EH | 3F5FH | --- | 3F80H | 3F81H | 3F82H | 3F83H |
| **40h** | 4000H | 4001H | 4002H | 4003H | --- | 405DH | 405EH | 405FH | --- | 4080H | 4081H | 4082H | 4083H |
| **41h** | 4100H | 4101H | 4102H | 4103H | --- | 415DH | 415EH | 415FH | --- | 4180H | 4181H | 4182H | 4183H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **9Ch** | 9C00H | 9C01H | 9C02H | 9C03H | --- | 9C5DH | 9C5EH | 9C5FH | --- | 9C80H | 9C81H | 9C82H | 9C83H |
| **9Dh** | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --- | 9DB5DH | 9DB5EH | 9DB5FH | --- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| **9Eh** | 9E00H | 9E01H | 9E02H | 9E03H | --- | 9E5DH | 9E5EH | 9E5FH | --- | 9E80H | 9E81H | 9E82H | 9E83H |
| **9Fh** | 9F00H | 9F01H | 9F02H | 9F03H | --- | 9F5DH | 9F5EH | 9F5FH | --- | 9F80H | 9F81H | 9F82H | 9F83H |
| **A0h** | A000H | A001H | A002H | A003H | --- | A05DH | A05EH | A05FH | --- | A080H | A081H | A082H | A083H |
| **A1h** | A100H | A101H | A102H | A103H | --- | A15DH | A15EH | A15FH | --- | A180H | A181H | A182H | A183H |

| LCD panel S/G pins | S55 | S56 | S57 | | S340 | S341 | S342 |
|---|---|---|---|---|---|---|---|
| **G1** | 0000H | | | --------- | 005FH | | |
| **G2** | 0100H | | | --------- | 015FH | | |
| **G3** | 0200H | | | --------- | 025FH | | |
| **G4** | 0300H | | | --------- | 035FH | | |
| **G5** | 0400H | | | --------- | 045FH | | |
| **G6** | 0500H | | | --------- | 055FH | | |
| ⋮ | ⋮ | | | ⋮ | ⋮ | | |
| **G63** | 3E00H | | | --------- | 3E5FH | | |
| **G64** | 3F00H | | | --------- | 3F5FH | | |

**Table 5. 18**

### (b)Partial Display On

PSL[15:0]=02, PEL[15:0]=3D, ML=0.

| GRAM | 00h<br>DB---DB<br>17 ---0 | 01h<br>DB---DB<br>17 ---0 | 02h<br>DB---DB<br>17 ---0 | 03h<br>DB---DB<br>17 ---0 | --- | 5Dh<br>DB---DB<br>17 ---0 | 5Eh<br>DB---DB<br>17 ---0 | 5Fh<br>DB---DB<br>17 ---0 | --- | 80h<br>DB---DB<br>17 ---0 | 81h<br>DB---DB<br>17 ---0 | 82h<br>DB---DB<br>17 ---0 | 83h<br>DB---DB<br>17 ---0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **00h** | 0000H | 0001H | 0002H | 0003H | --- | 005DH | 005EH | 005FH | --- | 0080H | 0081H | 0082H | 0083H |
| **01h** | 0100H | 0101H | 0102H | 0103H | --- | 015DH | 015EH | 015FH | --- | 0180H | 0181H | 0182H | 0183H |
| **02h** | 0200H | 0201H | 0202H | 0203H | --- | 025DH | 025EH | 025FH | --- | 0280H | 0281H | 0282H | 0283H |
| **03h** | 0300H | 0301H | 0302H | 0303H | --- | 035DH | 035EH | 035FH | --- | 0380H | 0381H | 0382H | 0383H |
| **04h** | 0400H | 0401H | 0402H | 0403H | --- | 045DH | 045EH | 045FH | --- | 0480H | 0481H | 0482H | 0483H |
| **05h** | 0500H | 0501H | 0502H | 0503H | --- | 055DH | 055EH | 055FH | --- | 0580H | 0581H | 0582H | 0583H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **3Fh** | 3F00H | 3F01H | 3F02H | 3F03H | --- | 3F5DH | 3F5EH | 3F5FH | --- | 3F80H | 3F81H | 3F82H | 3F83H |
| **40h** | 4000H | 4001H | 4002H | 4003H | --- | 405DH | 405EH | 405FH | --- | 4080H | 4081H | 4082H | 4083H |
| **41h** | 4100H | 4101H | 4102H | 4103H | --- | 415DH | 415EH | 415FH | --- | 4180H | 4181H | 4182H | 4183H |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | --- | ⋮ | ⋮ | ⋮ | ⋮ |
| **9Ch** | 9C00H | 9C01H | 9C02H | 9C03H | --- | 9C5DH | 9C5EH | 9C5FH | --- | 9C80H | 9C81H | 9C82H | 9C83H |
| **9Dh** | 9DB00H | 9DB01H | 9DB02H | 9DB03H | --- | 9DB5DH | 9DB5EH | 9DB5FH | --- | 9DB80H | 9DB81H | 9DB82H | 9DB83H |
| **9Eh** | 9E00H | 9E01H | 9E02H | 9E03H | --- | 9E5DH | 9E5EH | 9E5FH | --- | 9E80H | 9E81H | 9E82H | 9E83H |
| **9Fh** | 9F00H | 9F01H | 9F02H | 9F03H | --- | 9F5DH | 9F5EH | 9F5FH | --- | 9F80H | 9F81H | 9F82H | 9F83H |
| **A0h** | A000H | A001H | A002H | A003H | --- | A05DH | A05EH | A05FH | --- | A080H | A081H | A082H | A083H |
| **A1h** | A100H | A101H | A102H | A103H | --- | A15DH | A15EH | A15FH | --- | A180H | A181H | A182H | A183H |

| | LCD panel S/G pins | S55 | S56 | S57 | | S340 | S341 | S342 |
|---|---|---|---|---|---|---|---|---|
| Non-display area 2 lines | **G1** | 0000H | | | --------- | | 005FH | |
| | **G2** | 0100H | | | --------- | | 015FH | |
| Display area 60 lines | **G3** | 0200H | | | --------- | | 025FH | |
| | **G4** | 0300H | | | --------- | | 035FH | |
| | **G5** | 0400H | | | --------- | | 045FH | |
| | **G6** | 0500H | | | --------- | | 055FH | |
| | ⋮ | ⋮ | | | ⋮ | | ⋮ | |
| Non-display area 2 lines | **G63** | 3E00H | | | --------- | | 3E5FH | |
| | **G64** | 3F00H | | | --------- | | 3F5FH | |

**Table 5. 19**

## 5.4 Vertical Scrolling Display

The vertical scrolling display is specified by SCRLAR instruction (R33h) and VSCSAD instruction (R37h). The Vertical scrolling is only enable when using 132 x 162 GRAM resolution, display resolution 132RGB x 162 and support S45AP spec (RSO[2:0]=3'b000 & STE_SEL=0)

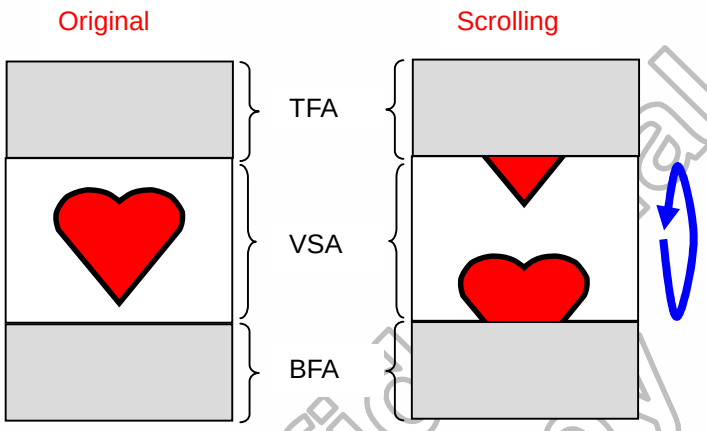



**Figure 5. 42**

**RSO[2:0]=3'b000 (132RGBx162)**

When RSO[2:0]=3'b000(132RGB x 162) and Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=162 (other setting is prohibited). In this case, scrolling is applied as shown below.

**Example 1: RSO=2'b00(132RGB x 162), TFA =3, VSA=157, BFA=2, VSP=4, MADCTR(ML)=0: Scrolling**

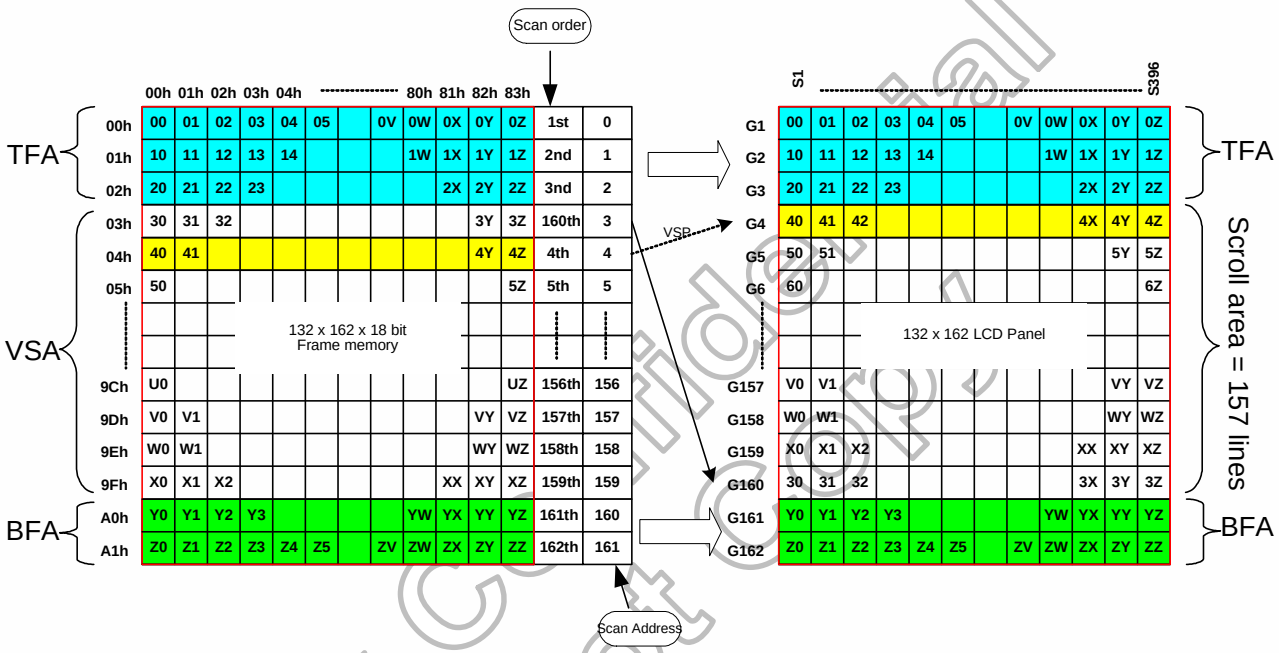



**Figure 5. 43**

**Example 2: RSO=2'b00(132RGB x 162), TFA =3, VSA=157, BFA=2, SSA=4, MADCTR (ML)=1: Scrolling (TFA and BFA are exchanged)**

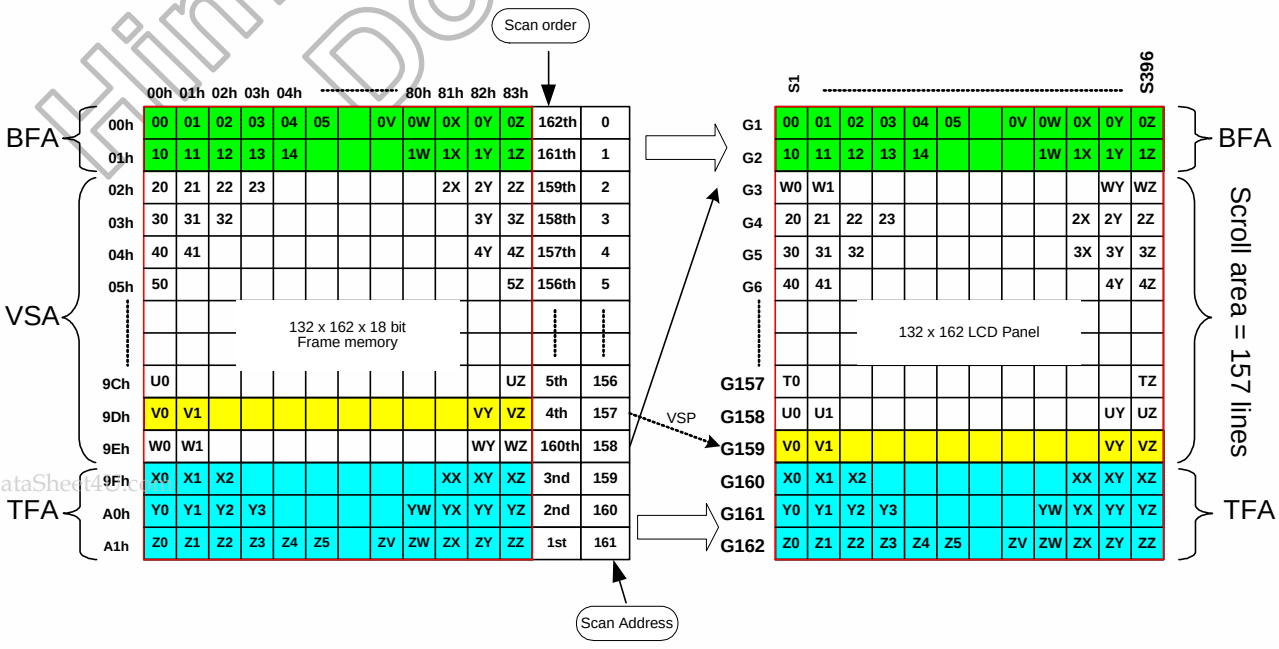



**Figure 5. 44**

## 5.5 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

### 5.5.1 Tearing Effect Line Modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:

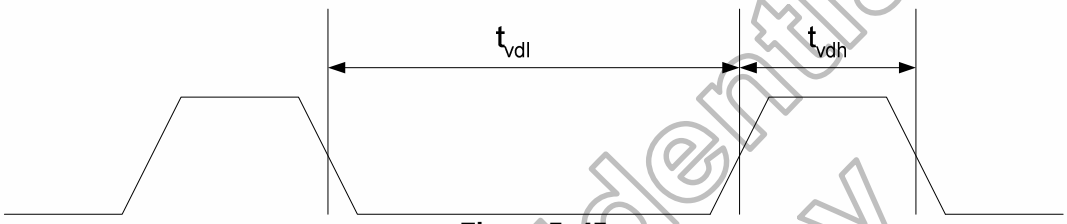
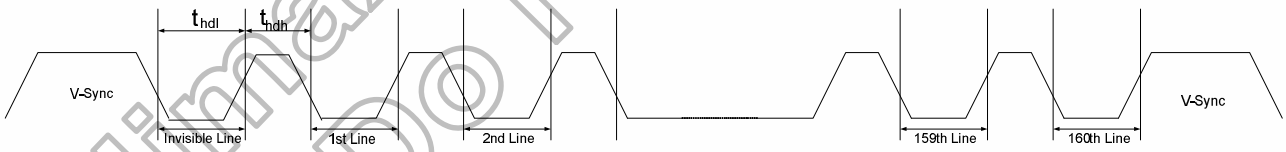



**Figure 5. 45**

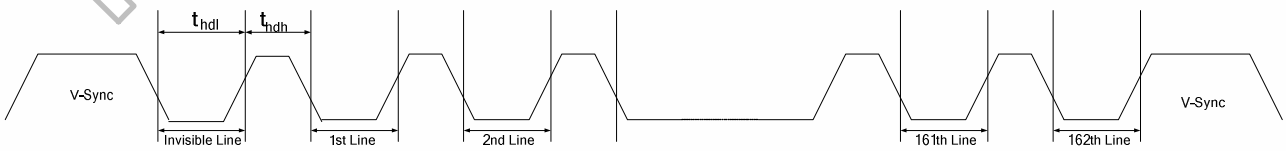
$t_{VREG1}$= The LCD display is not updated from the Frame Memory
$t_{vdl}$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field on different resolution.

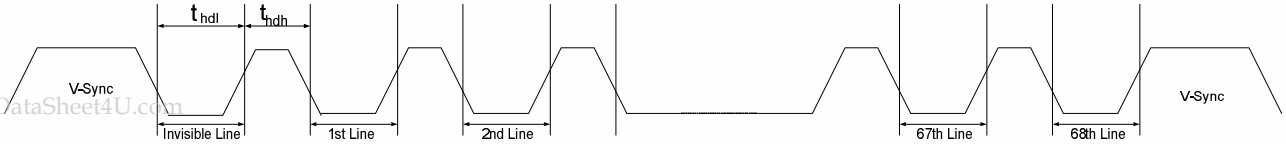
128RGBx160 (Support S43AP and S44AP): N=160




132RGBx162 (Support S45AP): N=162




96x68: N=68



96x64: N=64

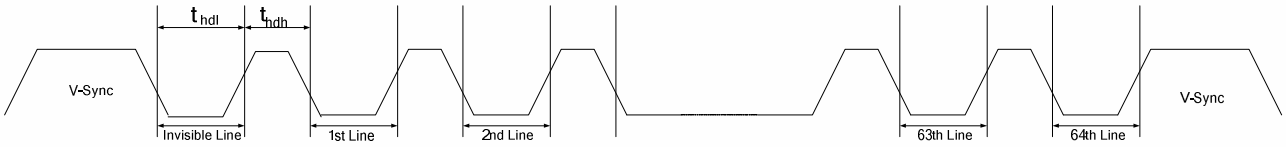
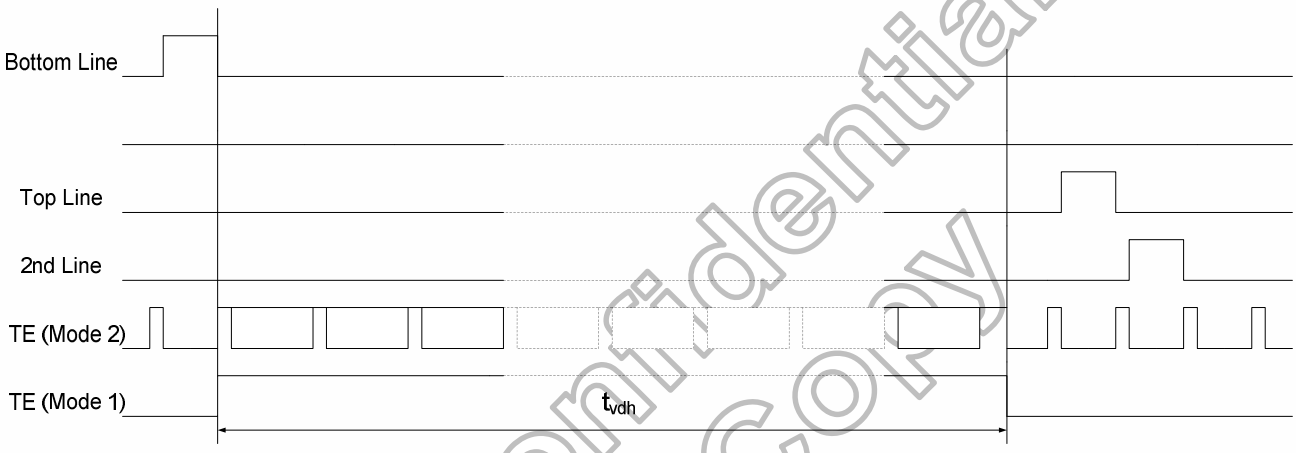



**Figure 5. 46**

$t_{hdh}$= The LCD display is not updated from the Frame Memory

$t_{hdl}$= The LCD display is updated from the Frame Memory (except Invisible Line – see above.)




**Note:** During Sleep In Mode, the Tearing Output Pin is active Low

**Figure 5. 47**

### 5.5.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.

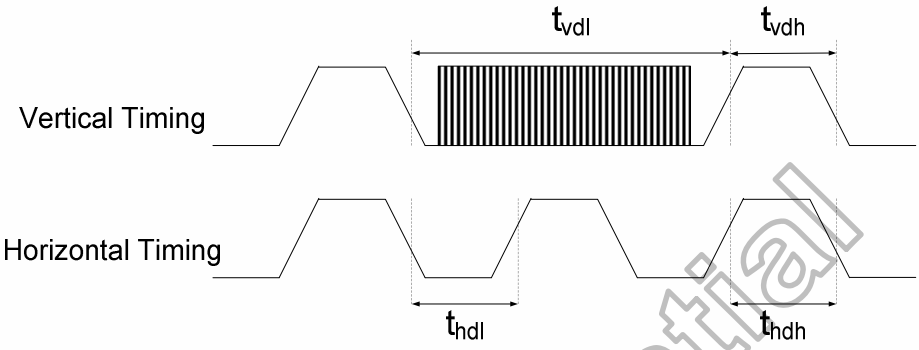



**Figure 5. 48**

Idle Mode Off (Frame Rate = TBDHz)

| Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|
| tvdl | Vertical Timing Low Duration | TBD | - | ms | - |
| tVREG1 | Vertical Timing High Duration | 1000 | - | us | - |
| thdl | Horizontal Timing Low Duration | TBD | - | us | - |
| thdh | Horizontal Timing High Duration | TBD | 500 | us | - |

**Note:** The timings in Table 5.12 apply when MADCTL ML=0 and ML=1

**Table 5. 20 AC characteristics of Tearing Effect Signal**

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

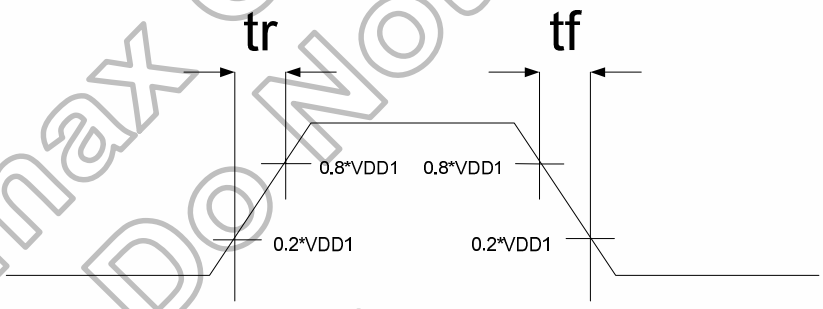



**Figure 5. 49**

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

### 5.5.3 Example 1: MPU Write is faster than Panel Read

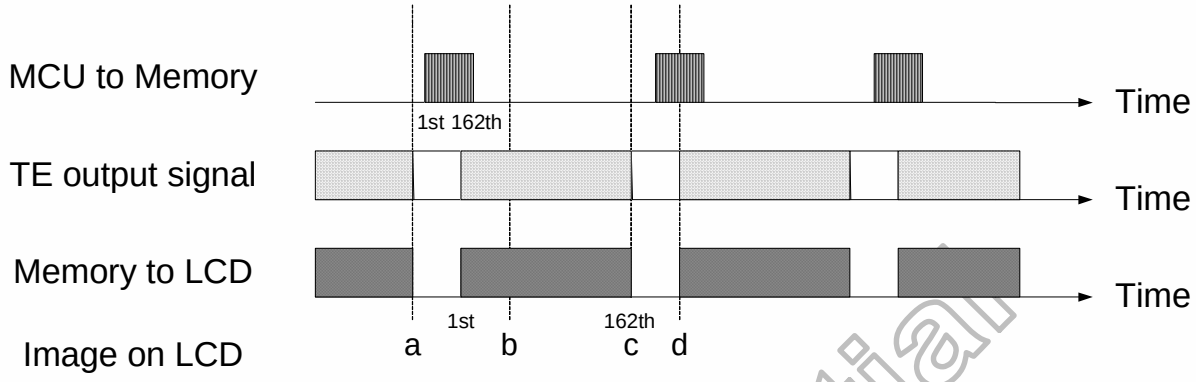



**Figure 5. 50**

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

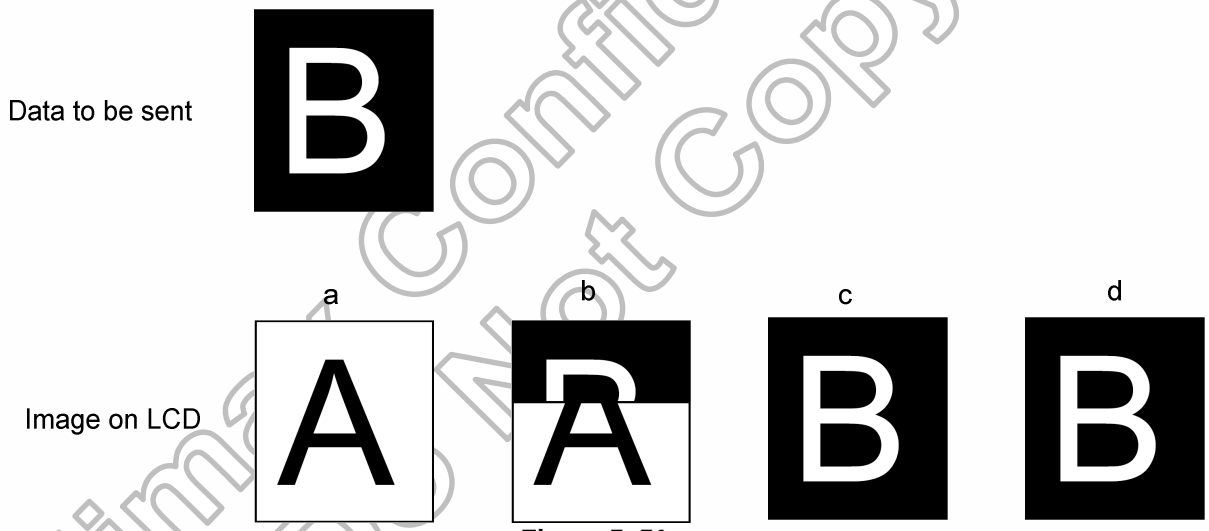



**Figure 5. 51**

### 5.5.4 Example 2: MPU Write is slower than Panel Read

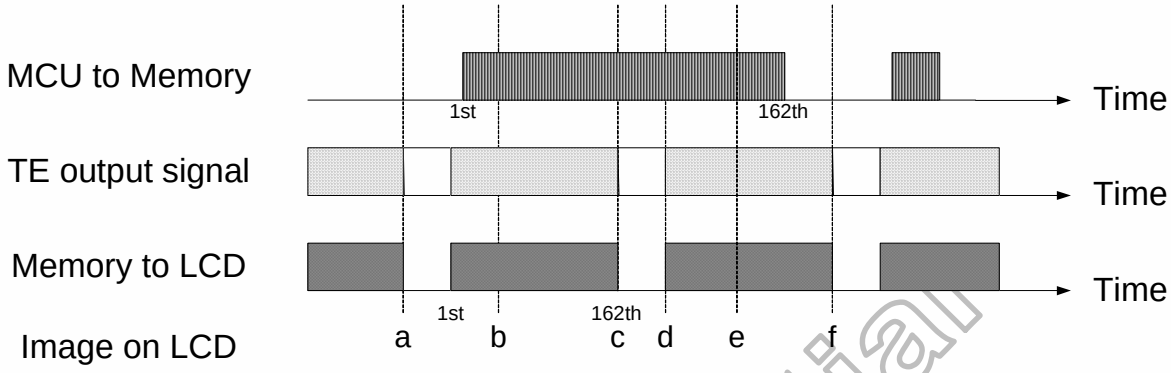
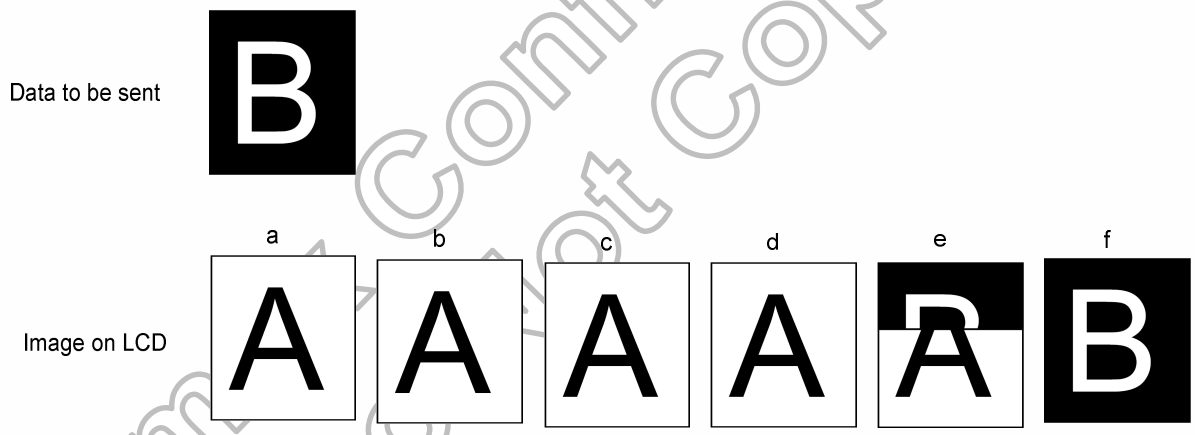



**Figure 5. 52**

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



## 5.6 Color Depth Conversion Look-up Tables

| R input (4bit)<br>12 bit/pixel -mode<br>4,096 colours | R input (5 bit)<br>16 bit/pixel -mode<br>65,536 colours | R output (6bit)<br>18 bit/pixel -mode<br>262,144 colours | RGBSET Parameter |
|---|---|---|---|
| 0000 | 00000 | $R_{005}R_{004}$ $R_{003}$ $R_{002}$ $R_{001}$ $R_{000}$ | 1 |
| 0001 | 00001 | $R_{015}R_{014}$ $R_{013}$ $R_{012}$ $R_{011}$ $R_{010}$ | 2 |
| 0010 | 00010 | $R_{025}R_{024}$ $R_{023}$ $R_{022}$ $R_{021}$ $R_{020}$ | 3 |
| 0011 | 00011 | $R_{035}R_{034}$ $R_{033}$ $R_{032}$ $R_{031}$ $R_{030}$ | 4 |
| 0100 | 00100 | $R_{045}R_{044}$ $R_{043}$ $R_{042}$ $R_{041}$ $R_{040}$ | 5 |
| 0101 | 00101 | $R_{055}R_{054}$ $R_{053}$ $R_{052}$ $R_{051}$ $R_{050}$ | 6 |
| 0110 | 00110 | $R_{065}R_{064}$ $R_{063}$ $R_{062}$ $R_{061}$ $R_{060}$ | 7 |
| 0111 | 00111 | $R_{075}R_{074}$ $R_{073}$ $R_{072}$ $R_{071}$ $R_{070}$ | 8 |
| 1000 | 01000 | $R_{085}R_{084}$ $R_{083}$ $R_{082}$ $R_{081}$ $R_{080}$ | 9 |
| 1001 | 01001 | $R_{095}R_{094}$ $R_{093}$ $R_{092}$ $R_{091}$ $R_{090}$ | 10 |
| 1010 | 01010 | $R_{105}R_{104}$ $R_{103}$ $R_{102}$ $R_{101}$ $R_{100}$ | 11 |
| 1011 | 01011 | $R_{115}R_{114}$ $R_{113}$ $R_{112}$ $R_{111}$ $R_{110}$ | 12 |
| 1100 | 01100 | $R_{125}R_{124}$ $R_{123}$ $R_{122}$ $R_{121}$ $R_{120}$ | 13 |
| 1101 | 01101 | $R_{135}R_{134}$ $R_{133}$ $R_{132}$ $R_{131}$ $R_{130}$ | 14 |
| 1110 | 01110 | $R_{145}R_{144}$ $R_{143}$ $R_{142}$ $R_{141}$ $R_{140}$ | 15 |
| 1111 | 01111 | $R_{155}R_{154}$ $R_{153}$ $R_{152}$ $R_{151}$ $R_{150}$ | 16 |
| No Input | 10000 | $R_{165}R_{164}$ $R_{163}$ $R_{162}$ $R_{161}$ $R_{160}$ | 17 |
| No Input | 10001 | $R_{175}R_{174}$ $R_{173}$ $R_{172}$ $R_{171}$ $R_{170}$ | 18 |
| No Input | 10010 | $R_{185}R_{184}$ $R_{183}$ $R_{182}$ $R_{181}$ $R_{180}$ | 19 |
| No Input | 10011 | $R_{195}R_{194}$ $R_{193}$ $R_{192}$ $R_{191}$ $R_{190}$ | 20 |
| No Input | 10100 | $R_{205}R_{204}$ $R_{203}$ $R_{202}$ $R_{201}$ $R_{200}$ | 21 |
| No Input | 10101 | $R_{215}R_{214}$ $R_{213}$ $R_{212}$ $R_{211}$ $R_{210}$ | 22 |
| No Input | 10110 | $R_{225}R_{224}$ $R_{223}$ $R_{222}$ $R_{221}$ $R_{220}$ | 23 |
| No Input | 10111 | $R_{235}R_{234}$ $R_{233}$ $R_{232}$ $R_{231}$ $R_{230}$ | 24 |
| No Input | 11000 | $R_{245}R_{244}$ $R_{243}$ $R_{242}$ $R_{241}$ $R_{240}$ | 25 |
| No Input | 11001 | $R_{255}R_{254}$ $R_{253}$ $R_{252}$ $R_{251}$ $R_{250}$ | 26 |
| No Input | 11010 | $R_{265}R_{264}$ $R_{263}$ $R_{262}$ $R_{261}$ $R_{260}$ | 27 |
| No Input | 11011 | $R_{275}R_{274}$ $R_{273}$ $R_{272}$ $R_{271}$ $R_{270}$ | 28 |
| No Input | 11100 | $R_{285}R_{284}$ $R_{283}$ $R_{282}$ $R_{281}$ $R_{280}$ | 29 |
| No Input | 11101 | $R_{295}R_{294}$ $R_{293}$ $R_{292}$ $R_{291}$ $R_{290}$ | 30 |
| No Input | 11110 | $R_{305}R_{304}$ $R_{303}$ $R_{302}$ $R_{301}$ $R_{300}$ | 31 |
| No Input | 11111 | $R_{315}R_{314}$ $R_{313}$ $R_{312}$ $R_{311}$ $R_{310}$ | 32 |

| G input (4bit)<br>12 bit/pixel -mode<br>4,096 colours | G input (6 bit)<br>16 bit/pixel -mode<br>65,536 colours | G output (6bit)<br>18 bit/pixel -mode<br>262,144 colours | RGBSET Parameter |
|---|---|---|---|
| 0000 | 000000 | $G_{005}G_{004}$ $G_{003}$ $G_{002}$ $G_{001}$ $G_{000}$ | 33 |
| 0001 | 000001 | $G_{015}G_{014}$ $G_{013}$ $G_{012}$ $G_{011}$ $G_{010}$ | 34 |
| 0010 | 000010 | $G_{025}G_{024}$ $G_{023}$ $G_{022}$ $G_{021}$ $G_{020}$ | 35 |
| 0011 | 000011 | $G_{035}G_{034}$ $G_{033}$ $G_{032}$ $G_{031}$ $G_{030}$ | 36 |
| 0100 | 000100 | $G_{045}G_{044}$ $G_{043}$ $G_{042}$ $G_{041}$ $G_{040}$ | 37 |
| 0101 | 000101 | $G_{055}G_{054}$ $G_{053}$ $G_{052}$ $G_{051}$ $G_{050}$ | 38 |
| 0110 | 000110 | $G_{065}G_{064}$ $G_{063}$ $G_{062}$ $G_{061}$ $G_{060}$ | 39 |
| 0111 | 000111 | $G_{075}G_{074}$ $G_{073}$ $G_{072}$ $G_{071}$ $G_{070}$ | 40 |
| 1000 | 001000 | $G_{085}G_{084}$ $G_{083}$ $G_{082}$ $G_{081}$ $G_{080}$ | 41 |
| 1001 | 001001 | $G_{095}G_{094}$ $G_{093}$ $G_{092}$ $G_{091}$ $G_{090}$ | 42 |
| 1010 | 001010 | $G_{105}G_{104}$ $G_{103}$ $G_{102}$ $G_{101}$ $G_{100}$ | 43 |
| 1011 | 001011 | $G_{115}G_{114}$ $G_{113}$ $G_{112}$ $G_{111}$ $G_{110}$ | 44 |
| 1100 | 001100 | $G_{125}G_{124}$ $G_{123}$ $G_{122}$ $G_{121}$ $G_{120}$ | 45 |
| 1101 | 001101 | $G_{135}G_{134}$ $G_{133}$ $G_{132}$ $G_{131}$ $G_{130}$ | 46 |
| 1110 | 001110 | $G_{145}G_{144}$ $G_{143}$ $G_{142}$ $G_{141}$ $G_{140}$ | 47 |
| 1111 | 001111 | $G_{155}G_{154}$ $G_{153}$ $G_{152}$ $G_{151}$ $G_{150}$ | 48 |
| No Input | 010000 | $G_{165}G_{164}$ $G_{163}$ $G_{162}$ $G_{161}$ $G_{160}$ | 49 |
| No Input | 010001 | $G_{175}G_{174}$ $G_{173}$ $G_{172}$ $G_{171}$ $G_{170}$ | 50 |
| No Input | 010010 | $G_{185}G_{184}$ $G_{183}$ $G_{182}$ $G_{181}$ $G_{180}$ | 51 |
| No Input | 010011 | $G_{195}G_{194}$ $G_{193}$ $G_{192}$ $G_{191}$ $G_{190}$ | 52 |
| No Input | 010100 | $G_{205}G_{204}$ $G_{203}$ $G_{202}$ $G_{201}$ $G_{200}$ | 53 |
| No Input | 010101 | $G_{215}G_{214}$ $G_{213}$ $G_{212}$ $G_{211}$ $G_{210}$ | 54 |
| No Input | 010110 | $G_{225}G_{224}$ $G_{223}$ $G_{222}$ $G_{221}$ $G_{220}$ | 55 |
| No Input | 010111 | $G_{235}G_{234}$ $G_{233}$ $G_{232}$ $G_{231}$ $G_{230}$ | 56 |
| No Input | 011000 | $G_{245}G_{244}$ $G_{243}$ $G_{242}$ $G_{241}$ $G_{240}$ | 57 |
| No Input | 011001 | $G_{255}G_{254}$ $G_{253}$ $G_{252}$ $G_{251}$ $G_{250}$ | 58 |
| No Input | 011010 | $G_{265}G_{264}$ $G_{263}$ $G_{262}$ $G_{261}$ $G_{260}$ | 59 |
| No Input | 011011 | $G_{275}G_{274}$ $G_{273}$ $G_{272}$ $G_{271}$ $G_{270}$ | 60 |
| No Input | 011100 | $G_{285}G_{284}$ $G_{283}$ $G_{282}$ $G_{281}$ $G_{280}$ | 61 |
| No Input | 011101 | $G_{295}G_{294}$ $G_{293}$ $G_{292}$ $G_{291}$ $G_{290}$ | 62 |
| No Input | 011110 | $G_{305}G_{304}$ $G_{303}$ $G_{302}$ $G_{301}$ $G_{300}$ | 63 |
| No Input | 011111 | $G_{315}G_{314}$ $G_{313}$ $G_{312}$ $G_{311}$ $G_{310}$ | 64 |

| G input (4bit)<br>12 bit/pixel -mode<br>4,096 colours | G input (6 bit)<br>16 bit/pixel -mode<br>65,536 colours | G output (6bit)<br>18 bit/pixel -mode<br>262,144 colours | RGBSET Parameter |
|---|---|---|---|
| No Input | 100000 | $G_{325}$ $G_{324}$ $G_{323}$ $G_{322}$ $G_{321}$ $G_{320}$ | 65 |
| No Input | 100001 | $G_{335}$ $G_{334}$ $G_{333}$ $G_{332}$ $G_{331}$ $G_{330}$ | 66 |
| No Input | 100010 | $G_{345}$ $G_{344}$ $G_{343}$ $G_{342}$ $G_{341}$ $G_{340}$ | 67 |
| No Input | 100011 | $G_{355}$ $G_{354}$ $G_{353}$ $G_{352}$ $G_{351}$ $G_{350}$ | 68 |
| No Input | 100100 | $G_{365}$ $G_{364}$ $G_{363}$ $G_{362}$ $G_{361}$ $G_{360}$ | 69 |
| No Input | 100101 | $G_{375}$ $G_{374}$ $G_{373}$ $G_{372}$ $G_{371}$ $G_{370}$ | 70 |
| No Input | 100110 | $G_{385}$ $G_{384}$ $G_{383}$ $G_{382}$ $G_{381}$ $G_{380}$ | 71 |
| No Input | 100111 | $G_{395}$ $G_{394}$ $G_{393}$ $G_{392}$ $G_{391}$ $G_{390}$ | 72 |
| No Input | 101000 | $G_{405}$ $G_{404}$ $G_{403}$ $G_{402}$ $G_{401}$ $G_{400}$ | 73 |
| No Input | 101001 | $G_{415}$ $G_{414}$ $G_{413}$ $G_{412}$ $G_{411}$ $G_{410}$ | 74 |
| No Input | 101010 | $G_{425}$ $G_{424}$ $G_{423}$ $G_{422}$ $G_{421}$ $G_{420}$ | 75 |
| No Input | 101011 | $G_{435}$ $G_{434}$ $G_{433}$ $G_{432}$ $G_{431}$ $G_{430}$ | 76 |
| No Input | 101100 | $G_{445}$ $G_{444}$ $G_{443}$ $G_{442}$ $G_{441}$ $G_{440}$ | 77 |
| No Input | 101101 | $G_{455}$ $G_{454}$ $G_{453}$ $G_{452}$ $G_{451}$ $G_{450}$ | 78 |
| No Input | 101110 | $G_{465}$ $G_{464}$ $G_{463}$ $G_{462}$ $G_{461}$ $G_{460}$ | 79 |
| No Input | 101111 | $G_{475}$ $G_{474}$ $G_{473}$ $G_{472}$ $G_{471}$ $G_{470}$ | 80 |
| No Input | 110000 | $G_{485}$ $G_{484}$ $G_{483}$ $G_{482}$ $G_{481}$ $G_{480}$ | 81 |
| No Input | 110001 | $G_{495}$ $G_{494}$ $G_{493}$ $G_{492}$ $G_{491}$ $G_{490}$ | 82 |
| No Input | 110010 | $G_{505}$ $G_{504}$ $G_{503}$ $G_{502}$ $G_{501}$ $G_{500}$ | 83 |
| No Input | 110011 | $G_{515}$ $G_{514}$ $G_{513}$ $G_{512}$ $G_{511}$ $G_{510}$ | 84 |
| No Input | 110100 | $G_{525}$ $G_{524}$ $G_{523}$ $G_{522}$ $G_{521}$ $G_{520}$ | 85 |
| No Input | 110101 | $G_{535}$ $G_{534}$ $G_{533}$ $G_{532}$ $G_{531}$ $G_{530}$ | 86 |
| No Input | 110110 | $G_{545}$ $G_{544}$ $G_{543}$ $G_{542}$ $G_{541}$ $G_{540}$ | 87 |
| No Input | 110111 | $G_{555}$ $G_{554}$ $G_{553}$ $G_{552}$ $G_{551}$ $G_{550}$ | 88 |
| No Input | 111000 | $G_{565}$ $G_{564}$ $G_{563}$ $G_{562}$ $G_{561}$ $G_{560}$ | 89 |
| No Input | 111001 | $G_{575}$ $G_{574}$ $G_{573}$ $G_{572}$ $G_{571}$ $G_{570}$ | 90 |
| No Input | 111010 | $G_{585}$ $G_{584}$ $G_{583}$ $G_{582}$ $G_{581}$ $G_{580}$ | 91 |
| No Input | 111011 | $G_{595}$ $G_{594}$ $G_{593}$ $G_{592}$ $G_{591}$ $G_{590}$ | 92 |
| No Input | 111100 | $G_{605}$ $G_{604}$ $G_{603}$ $G_{602}$ $G_{601}$ $G_{600}$ | 93 |
| No Input | 111101 | $G_{615}$ $G_{614}$ $G_{613}$ $G_{612}$ $G_{611}$ $G_{610}$ | 94 |
| No Input | 111110 | $G_{625}$ $G_{624}$ $G_{623}$ $G_{622}$ $G_{621}$ $G_{620}$ | 95 |
| No Input | 111111 | $G_{635}$ $G_{634}$ $G_{533}$ $G_{632}$ $G_{631}$ $G_{630}$ | 96 |

| B input (4bit)<br>12 bit/pixel -mode<br>4,096 colours | B input (5 bit)<br>16 bit/pixel -mode<br>65,536 colours | B output (6bit)<br>18 bit/pixel -mode<br>262,144 colours | RGBSET Parameter |
|---|---|---|---|
| 0000 | 00000 | $B_{005}B_{004}$ $B_{003}$ $B_{002}$ $B_{001}$ $B_{000}$ | 97 |
| 0001 | 00001 | $B_{015}B_{014}$ $B_{013}$ $B_{012}$ $B_{011}$ $B_{010}$ | 98 |
| 0010 | 00010 | $B_{025}B_{024}$ $B_{023}$ $B_{022}$ $B_{021}$ $B_{020}$ | 99 |
| 0011 | 00011 | $B_{035}B_{034}$ $B_{033}$ $B_{032}$ $B_{031}$ $B_{030}$ | 100 |
| 0100 | 00100 | $B_{045}B_{044}$ $B_{043}$ $B_{042}$ $B_{041}$ $B_{040}$ | 101 |
| 0101 | 00101 | $B_{055}B_{054}$ $B_{053}$ $B_{052}$ $B_{051}$ $B_{050}$ | 102 |
| 0110 | 00110 | $B_{065}B_{064}$ $B_{063}$ $B_{062}$ $B_{061}$ $B_{060}$ | 103 |
| 0111 | 00111 | $B_{075}B_{074}$ $B_{073}$ $B_{072}$ $B_{071}$ $B_{070}$ | 104 |
| 1000 | 01000 | $B_{085}B_{084}$ $B_{083}$ $B_{082}$ $B_{081}$ $B_{080}$ | 105 |
| 1001 | 01001 | $B_{095}B_{094}$ $B_{093}$ $B_{092}$ $B_{091}$ $B_{090}$ | 106 |
| 1010 | 01010 | $B_{105}B_{104}$ $B_{103}$ $B_{102}$ $B_{101}$ $B_{100}$ | 107 |
| 1011 | 01011 | $B_{115}B_{114}$ $B_{113}$ $B_{112}$ $B_{111}$ $B_{110}$ | 108 |
| 1100 | 01100 | $B_{125}B_{124}$ $B_{123}$ $B_{122}$ $B_{121}$ $B_{120}$ | 109 |
| 1101 | 01101 | $B_{135}B_{134}$ $B_{133}$ $B_{132}$ $B_{131}$ $B_{130}$ | 110 |
| 1110 | 01110 | $B_{145}B_{144}$ $B_{143}$ $B_{142}$ $B_{141}$ $B_{140}$ | 111 |
| 1111 | 01111 | $B_{155}B_{154}$ $B_{153}$ $B_{152}$ $B_{151}$ $B_{150}$ | 112 |
| No Input | 10000 | $B_{165}B_{164}$ $B_{163}$ $B_{162}$ $B_{161}$ $B_{160}$ | 113 |
| No Input | 10001 | $B_{175}B_{174}$ $B_{173}$ $B_{172}$ $B_{171}$ $B_{170}$ | 114 |
| No Input | 10010 | $B_{185}B_{184}$ $B_{183}$ $B_{182}$ $B_{181}$ $B_{180}$ | 115 |
| No Input | 10011 | $B_{195}B_{194}$ $B_{193}$ $B_{192}$ $B_{191}$ $B_{190}$ | 116 |
| No Input | 10100 | $B_{205}B_{204}$ $B_{203}$ $B_{202}$ $B_{201}$ $B_{200}$ | 117 |
| No Input | 10101 | $B_{215}B_{214}$ $B_{213}$ $B_{212}$ $B_{211}$ $B_{210}$ | 118 |
| No Input | 10110 | $B_{225}B_{224}$ $B_{223}$ $B_{222}$ $B_{221}$ $B_{220}$ | 119 |
| No Input | 10111 | $B_{235}B_{234}$ $B_{233}$ $B_{232}$ $B_{231}$ $B_{230}$ | 120 |
| No Input | 11000 | $B_{245}B_{244}$ $B_{243}$ $B_{242}$ $B_{241}$ $B_{240}$ | 121 |
| No Input | 11001 | $B_{255}B_{254}$ $B_{253}$ $B_{252}$ $B_{251}$ $B_{250}$ | 122 |
| No Input | 11010 | $B_{265}B_{264}$ $B_{263}$ $B_{262}$ $B_{261}$ $B_{260}$ | 123 |
| No Input | 11011 | $B_{275}B_{274}$ $B_{273}$ $B_{272}$ $B_{271}$ $B_{270}$ | 124 |
| No Input | 11100 | $B_{285}B_{284}$ $B_{283}$ $B_{282}$ $B_{281}$ $B_{280}$ | 125 |
| No Input | 11101 | $B_{295}B_{294}$ $B_{293}$ $B_{292}$ $B_{291}$ $B_{290}$ | 126 |
| No Input | 11110 | $B_{305}B_{304}$ $B_{303}$ $B_{302}$ $B_{301}$ $B_{300}$ | 127 |
| No Input | 11111 | $B_{315}B_{314}$ $B_{313}$ $B_{312}$ $B_{311}$ $B_{310}$ | 128 |

### 5.7 Oscillator

The HX8353-C has an internal oscillator without extra external components that provide a source for system clock generator.

### 5.8 Source Driver

The HX8353-C contains a 396 channels of source driver (S1~S396) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 396 channels and generates corresponding gray scale voltage output, which can realize a 262,144 colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately output from each channel.

### 5.9 Gate Driver

The HX8353-C contains a 160 gate channels of gate driver (G1~G160) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

## 5.10 LCD POWER GENERATION CIRCUIT

### 5.10.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

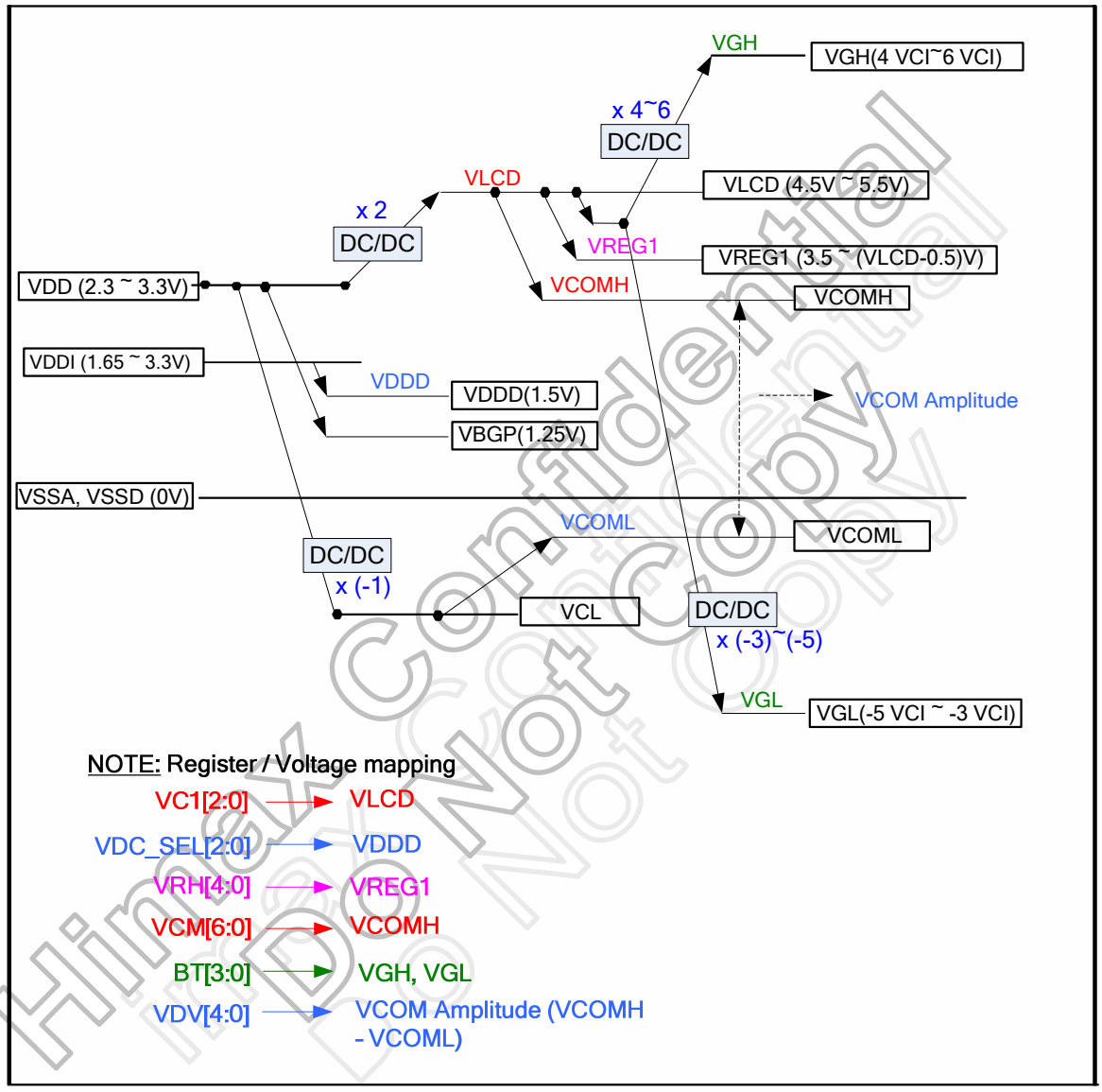



**Figure 5. 53 LCD power generation scheme**

### 5.10.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

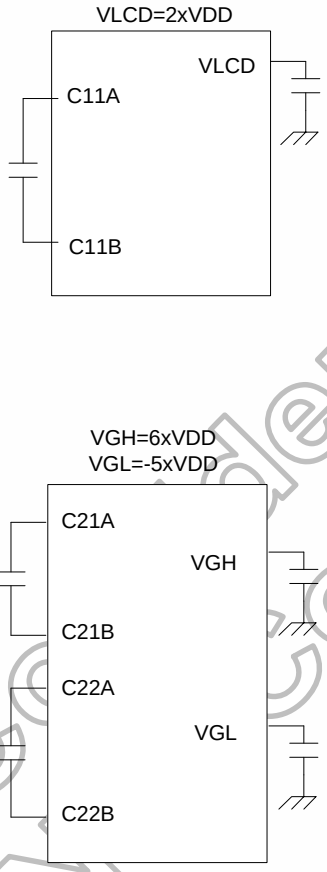



**Figure 5. 54 Block Diagram of Power Supply Circuit**

## 5.11 Gray Voltage Generator for Source Driver

The HX8353-C incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

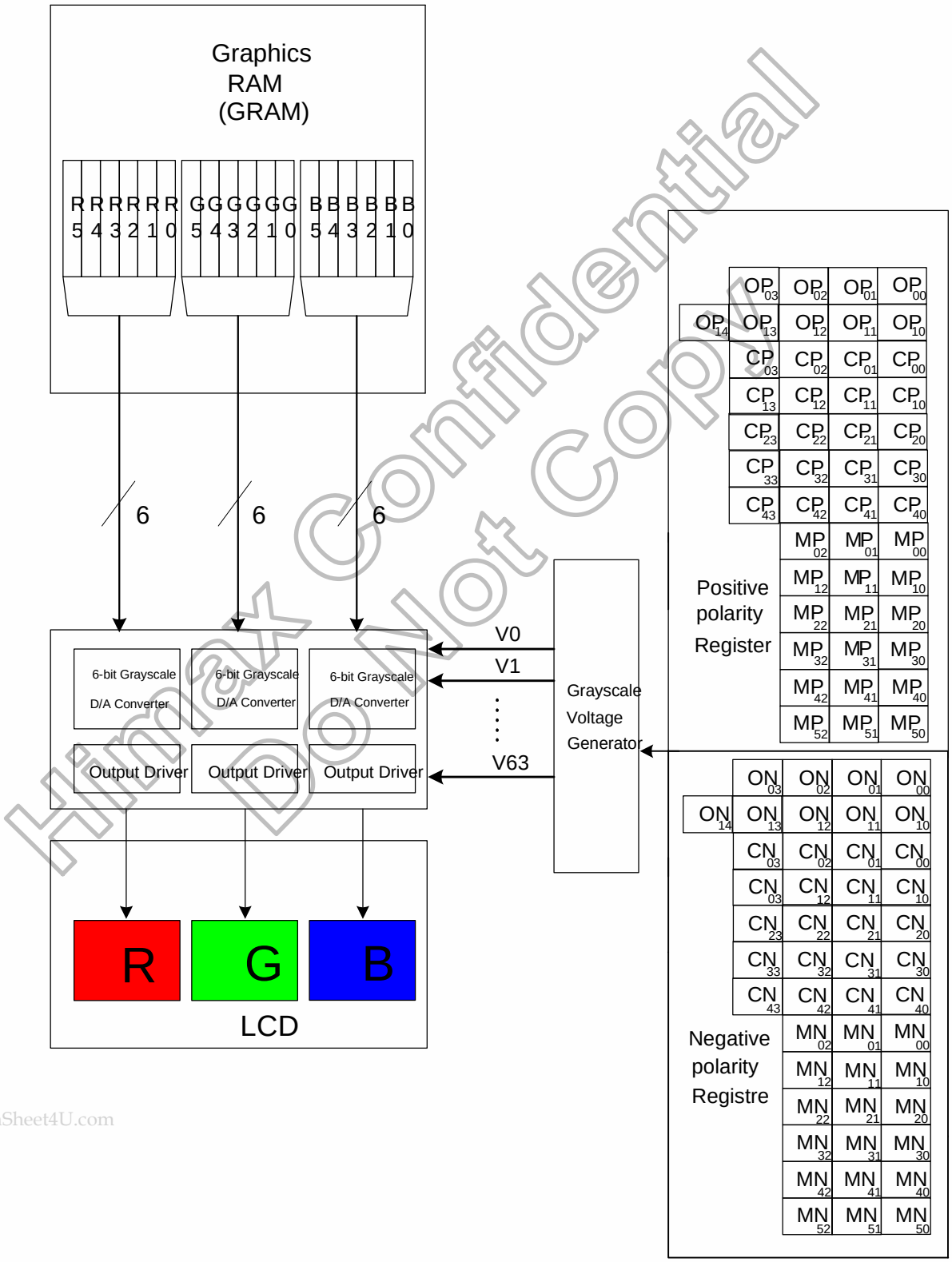



**Figure 5. 55 Grayscale Control**

### 5.11.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel.

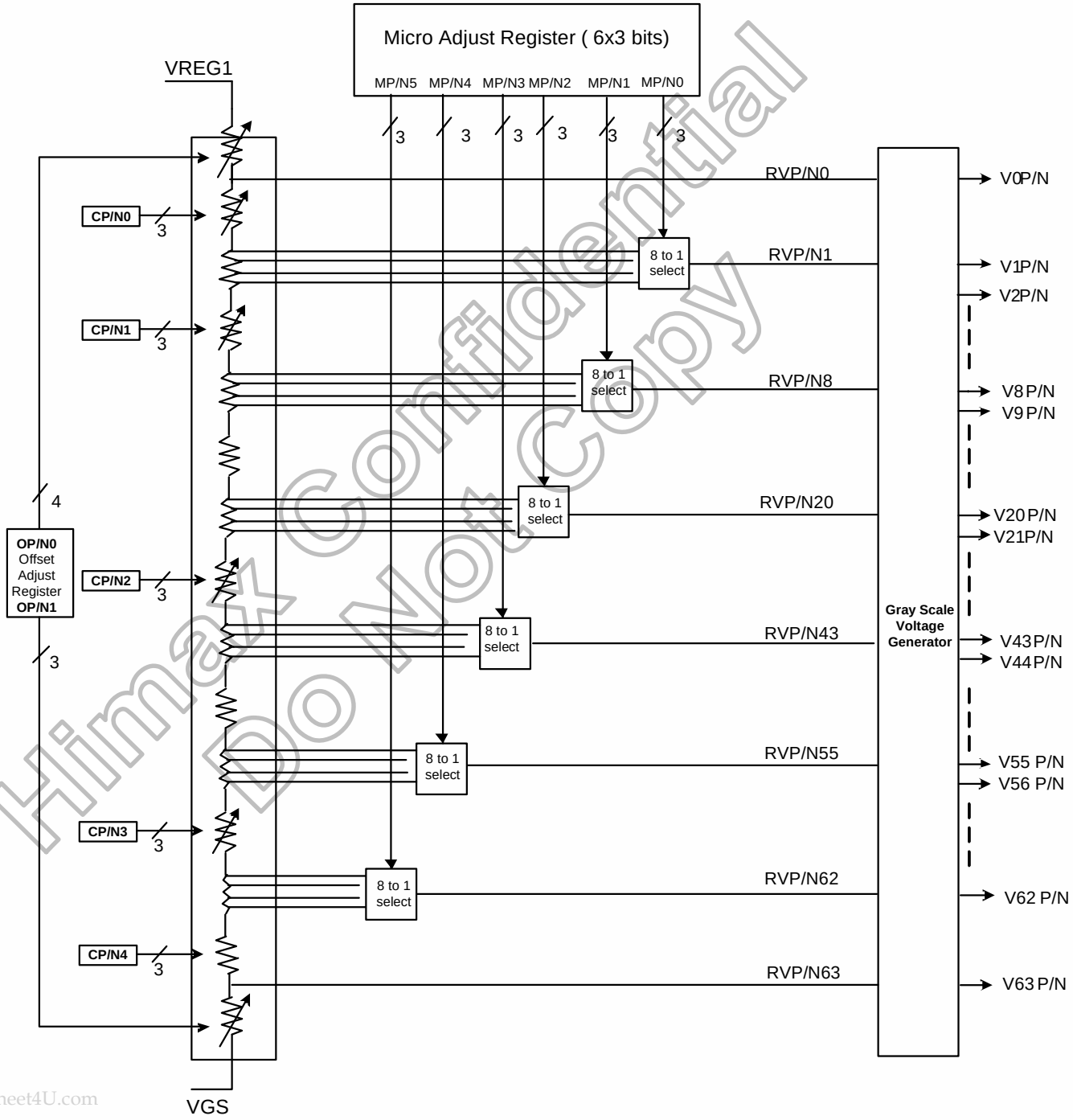



**Figure 5. 56 Structure of Grayscale Voltage Generator**

### 5.11.2 Gamma-Characteristics Adjustment Register

This HX8353-C has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

#### 5.11.2.1 Offset Adjustment Registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

#### 5.11.2.2 Gamma Center Adjustment Registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

### 5.11.3 Gamma Macro Adjustment Registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (RVP/N 0, 1, 8, 20, 44, 56, 63, 64). These registers are available for both positive and negative polarities.

| Register Groups | Positive Polarity | Description |
|---|---|---|
| Center Adjustment | CP/N0 3-0 | Variable resistor (VRTP/N) for center adjustment |
| | CP/N1 3-0 | Variable resistor (VRCP/N0)for center adjustment |
| | CP/N2 3-0 | Variable resistor (VRMP/N) for center adjustment |
| | CP/N3 3-0 | Variable resistor (VRCP/N1)for center adjustment |
| | CP/N4 3-0 | Variable resistor (VRBP/N)for center adjustment |
| Macro Adjustment | MP/N0 2-0 | 8-to-1 selector (reference voltage level of grayscale 1) |
| | MP/N1 2-0 | 8-to-1 selector (reference voltage level of grayscale 8) |
| | MP/N2 2-0 | 8-to-1 selector (reference voltage level of grayscale 20) |
| | MP/N3 2-0 | 8-to-1 selector (reference voltage level of grayscale 43) |
| | MP/N4 2-0 | 8-to-1 selector (reference voltage level of grayscale 55) |
| | MP/N5 2-0 | 8-to-1 selector (reference voltage level of grayscale 62) |
| Offset Adjustment | OP/N0 3-0 | Variable resistor (VRP/N0)for offset adjustment |
| | OP/N1 4-0 | Variable resistor (VRP/N1)for offset adjustment |

**Table 5. 21 Gamma-Adjustment Registers**

### 5.11.4 Gamma Resister Stream and 8 to 1 Selector

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.

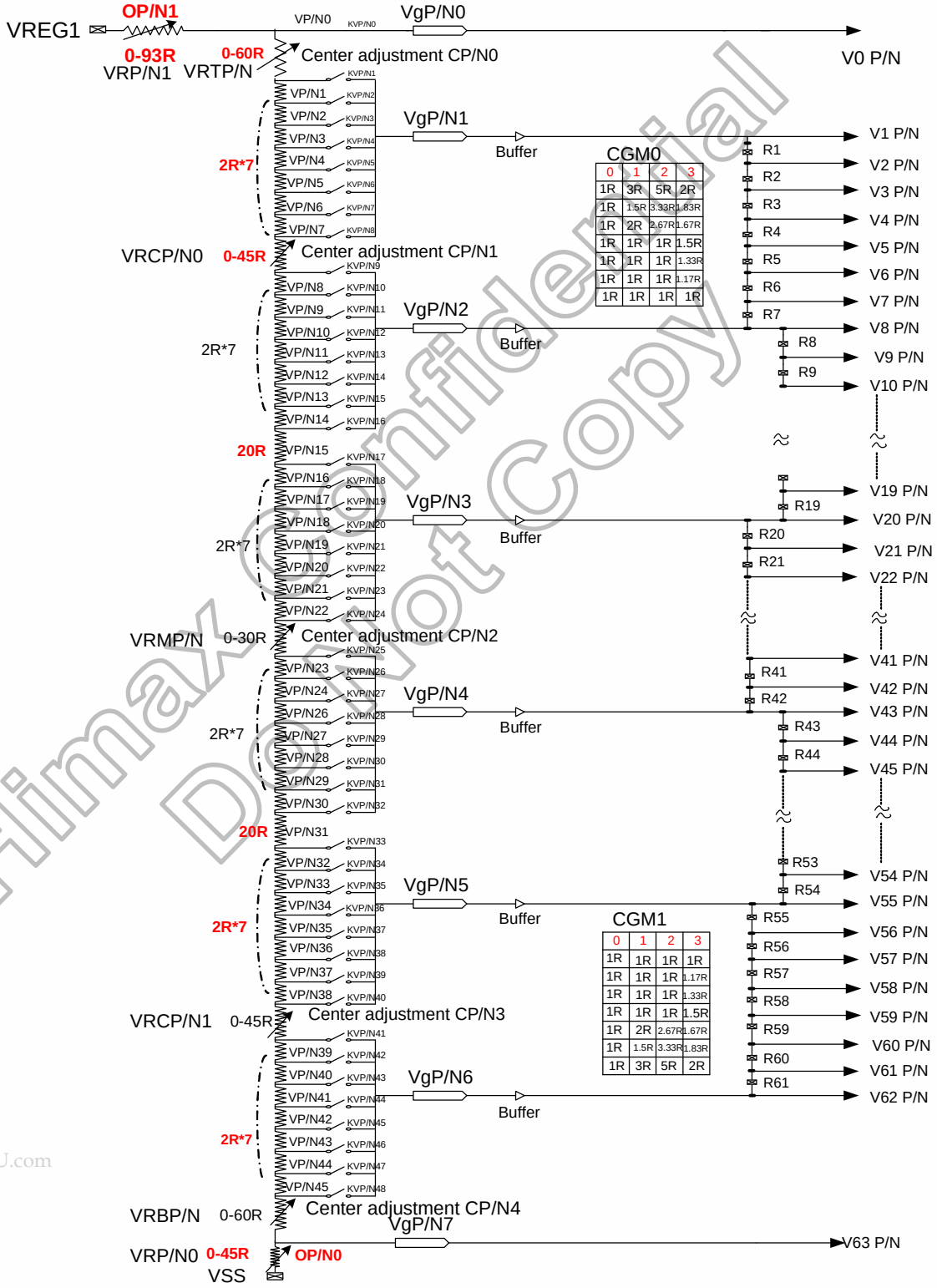



**Figure 5. 57 Gamma Resister Stream and Gamma Reference Voltage**

### 5.11.5 Variable Resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

| Value in Register OP/N0 3-0 | Resistance VRP/N0 |
|---|---|
| 0000 | **0R** |
| 0001 | **3R** |
| 0010 | **6R** |
| • • | • • |
| 1101 | **39R** |
| 1110 | **42R** |
| 1111 | **45R** |

**Table 5. 22 Offset Adjustment 0**

| Value in Register OP/N1 4-0 | Resistance VRP/N1 |
|---|---|
| 00000 | **0R** |
| 00001 | **3R** |
| 00010 | **6R** |
| • • | • • |
| 11101 | **87R** |
| 11110 | **90R** |
| 11111 | **93R** |

**Table 5. 23 Offset Adjustment 1**

| Value in Register CP/N0 3-0 | Resistance VRTP/N | Value in Register CP/N4 3-0 | Resistance VRBP/N | Value in Register CP/N2 3-0 | Resistance VRMP/N0 |
|---|---|---|---|---|---|
| 0000 | **0R** | 0000 | 0R | 0000 | 0R |
| 0001 | **4R** | 0001 | 4R | 0001 | 2R |
| 0010 | **8R** | 0010 | 8R | 0010 | 4R |
| • • | • | • • | • • | • • | • • |
| 1100 | • | 1100 | 48R | 1100 | 24R |
| 1101 | **52R** | 1101 | 52R | 1101 | 26R |
| 1110 | **56R** | 1110 | 56R | 1110 | 28R |
| 1111 | **60R** | 1111 | 60R | 1111 | 30R |

| Value in Register CP/N3 3-0 | Resistance VRCP/N1 |
|---|---|
| 0000 | 0R |
| 0001 | 3R |
| 0010 | 6R |
| • • | • • |
| 1100 | 36R |
| 1101 | 39R |
| 1110 | 42R |
| 1111 | 45R |

| Value in Register CP/N1 3-0 | Resistance VRCP/N0 |
|---|---|
| 0000 | **0R** |
| 0001 | **3R** |
| 0010 | **6R** |
| • • | • • |
| 1100 | **36R** |
| 1101 | **39R** |
| 1110 | **42R** |
| 1111 | **45R** |

**Table 5. 24 Center Adjustment**

### 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

| Value in Register | Voltage level | | | | | |
|---|---|---|---|---|---|---|
| M(P/N) 2-0 | Vg(P/N) 1 | Vg(P/N) 2 | Vg(P/N) 3 | Vg(P/N) 4 | Vg(P/N) 5 | Vg(P/N) 6 |
| 000 | VP(N)1 | VP(N)9 | VP(N)17 | VP(N)25 | VP(N)33 | VP(N)41 |
| 001 | VP(N)2 | VP(N)10 | VP(N)18 | VP(N)26 | VP(N)34 | VP(N)42 |
| 010 | VP(N)3 | VP(N)11 | VP(N)19 | VP(N)27 | VP(N)35 | VP(N)43 |
| 011 | VP(N)4 | VP(N)12 | VP(N)20 | VP(N)28 | VP(N)36 | VP(N)44 |
| 100 | VP(N)5 | VP(N)13 | VP(N)21 | VP(N)29 | VP(N)37 | VP(N)45 |
| 101 | VP(N)6 | VP(N)14 | VP(N)22 | VP(N)30 | VP(N)38 | VP(N)46 |
| 110 | VP(N)7 | VP(N)15 | VP(N)23 | VP(N)31 | VP(N)39 | VP(N)47 |
| 111 | VP(N)8 | VP(N)16 | VP(N)24 | VP(N)32 | VP(N)40 | VP(N)48 |

**Table 5. 25 Output Voltage of 8 to 1 Selector**

The grayscale levels are determined by the following formulas.

| Reference Voltage | Formula | | Pin |
|---|---|---|---|
| VgP/N0 | ---- | VREG1-VD*VRP/N0 /sumRP/N | KVP0/KVN49 |
| VgP1/VgN7 | MP/N0 2-0=000 | VREG1 –VD((VRP/N0+VRTP/N) /sumRP/N | KVP1/KVN48 |
| | MP/N0 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N +2R) /sumRP/N | KVP2/ KVN47 |
| | MP/N0 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N +4R) /sumRP/N | KVP3/ KVN46 |
| | MP/N0 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N +6R) /sumRP/N | KVP4/ KVN45 |
| | MP/N0 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N +8R) /sumRP/N | KVP5/ KVN44 |
| | MP/N0 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N +10R) /sumRP/N | KVP6/ KVN43 |
| | MP/N0 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N +12R) /sumRP/N | KVP7/ KVN42 |
| | MP/N0 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N +14R) /sumRP/N | KVP8/ KVN41 |
| VgP2/VgN2 | MP/N1 2-0=000 | VREG1 –VD((VRP/N0+ VRTP/N +14R+VRCP/N0) /sumRP/N | KVP9/ KVN40 |
| | MP/N1 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N +16R+VRCP/N0) /sumRP/N | KVP10/ KVN39 |
| | MP/N1 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N +18R+VRCP/N0) /sumRP/N | KVP11/ KVN38 |
| | MP/N1 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N +20R+VRCP/N0) /sumRP/N | KVP12/ KVN37 |
| | MP/N1 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N +22R+VRCP/N0) /sumRP/N | KVP13/ KVN36 |
| | MP/N1 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N +24R+VRCP/N0) /sumRP/N | KVP14/ KVN35 |
| | MP/N1 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N +26R+VRCP/N0) /sumRP/N | KVP15/ KVN34 |
| | MP/N1 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N +28R+VRCP/N0) /sumRP/N | KVP16/ KVN33 |
| VgP3/VgN3 | MP/N2 2-0=000 | VREG1 –VD((VRP/N0+ VRTP/N+48R+VRCP/N0) /sumRP/N | KVP17/ KVN32 |
| | MP/N2 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N+50R+VRCP/N0) /sumRP/N | KVP18/ KVN31 |
| | MP/N2 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N+52R+VRCP/N0) /sumRP/N | KVP19/ KVN30 |
| | MP/N2 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N+54R+VRCP/N0) /sumRP/N | KVP20/KVN29 |
| | MP/N2 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N+56R+VRCP/N0) /sumRP/N | KVP21/KVN28 |
| | MP/N2 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N+58R+VRCP/N0) /sumRP/N | KVP22/ KVN27 |
| | MP/N2 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N+60R+VRCP/N0) /sumRP/N | KVP23/ KVN26 |
| | MP/N2 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N+62R+VRCP/N0) /sumRP/N | KVP24/ KVN25 |
| VgP4/VgN4 | MP/N3 2-0=000 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +62R+VRCP/N0) /sumRP/N | KVP25/ KVN24 |
| | MP/N3 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +64R+VRCP/N0) /sumRP/N | KVP26/ KVN23 |
| | MP/N3 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +66R+VRCP/N0) /sumRP/N | KVP27/ KVN22 |
| | MP/N3 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +68R+VRCP/N0) /sumRP/N | KVP28/ KVN21 |
| | MP/N3 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +70R+VRCP/N0) /sumRP/N | KVP29/ KVN20 |
| | MP/N3 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +72R+VRCP/N0) /sumRP/N | KVP30/ KVN19 |
| | MP/N3 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +74R+VRCP/N0) /sumRP/N | KVP31/ KVN18 |
| | MP/N3 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +76R+VRCP/N0) /sumRP/N | KVP32/ KVN17 |
| VgP5Vg/N5 | MP/N4 2-0=000 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +96R+VRCP/N0) /sumRP/N | KVP33/ KVN16 |
| | MP/N4 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +98R+VRCP/N0) /sumRP/N | KVP34/ KVN15 |
| | MP/N4 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +100R+VRCP/N0) /sumRP/N | KVP35/ KVN14 |
| | MP/N4 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +102R+VRCP/N0) /sumRP/N | KVP36/ KVN13 |
| | MP/N4 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +104R+VRCP/N0) /sumRP/N | KVP37/ KVN12 |
| | MP/N4 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +106R+VRCP/N0) /sumRP/N | KVP38/ KVN11 |
| | MP/N4 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +108R+VRCP/N0) /sumRP/N | KVP39/ KVN10 |
| | MP/N4 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +110R+VRCP/N0) /sumRP/N | KVP40/ KVN9 |
| VgP6/VgN6 | MP/N5 2-0=000 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N+110R+VRCP/N0 +VRCP/N1) /sumRP/N | KVP41/ KVN8 |
| | MP/N5 2-0=001 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +112R+VRCP/N0+VRCP/N1) /sumRP/N | KVP42/ KVN7 |
| | MP/N5 2-0=010 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +114R+VRCP/N0+VRCP/N1) /sumRP/N | KVP43/ KVN6 |
| | MP/N5 2-0=011 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +116R+VRCP/N0+VRCP/N1) /sumRP/N | KVP44/ KVN5 |
| | MP/N5 2-0=100 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +118R+VRCP/N0+VRCP/N1) /sumRP/N | KVP45/ KVN4 |
| | MP/N5 2-0=101 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +120R+VRCP/N0+VRCP/N1) /sumRP/N | KVP46/ KVN3 |
| | MP/N5 2-0=110 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +122R+VRCP/N0+VRCP/N1) /sumRP/N | KVP47/ KVN2 |
| | MP/N5 2-0=111 | VREG1 –VD((VRP/N0+ VRTP/N+ VRMP/N +124R+VRCP/N0+VRCP/N1) /sumRP/N | KVP48/ KVN1 |
| VgP7/VgN7 | ---- | VREG1 –VD((VRP/N0+ VRBP/N+ VRTP/N+ VRMP/N +104R+VRCP/N0+VRCP/N1) /sumRP/N | KVP49/ KVN0 |

SumRP=124R+VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
SumRN=124R+ VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
VD=(VREG1–VSS)

**Table 5. 26 Voltage Calculation Formula**

| Grayscale Voltage | Formula | Grayscale Voltage | Formula |
|---|---|---|---|
| V0P/V63N | VgP/N0 | V32P/V31N | VgP/N4+(VgP/N3-VgP/N4)*(11/23) |
| V1P/V62N | VgP/N1 | V33P/V30N | VgP/N4+(VgP/N3-VgP/N4)*(10/23) |
| V2P/V61N | VgP/N2+(VgP/N1-VgP/N2)*CT1 | V34P/V29N | VgP/N4+(VgP/N3-VgP/N4)*(9/23) |
| V3P/V60N | VgP/N2+(VgP/N1-VgP/N2)*CT2 | V35P/V28N | VgP/N4+(VgP/N3-VgP/N4)*(8/23) |
| V4P/V59N | VgP/N2+(VgP/N1-VgP/N2)*CT3 | V36P/V27N | VgP/N4+(VgP/N3-VgP/N4)*(7/23) |
| V5P/V58N | VgP/N2+(VgP/N1-VgP/N2)*CT4 | V37P/V26N | VgP/N4+(VgP/N3-VgP/N4)*(6/23) |
| V6P/V57N | VgP/N2+(VgP/N1-VgP/N2)*CT5 | V38P/V25N | VgP/N4+(VgP/N3-VgP/N4)*(5/23) |
| V7P/V56N | VgP/N2+(VgP/N1-VgP/N2)*CT6 | V39P/V24N | VgP/N4+(VgP/N3-VgP/N4)*(4/23) |
| V8P/V55N | VgP/N2 | V40P/V23N | VgP/N4+(VgP/N3-VgP/N4)*(3/23) |
| V9P/V54N | VgP/N3+(VgP/N2-VgP/N3)*(22/24) | V41P/V22N | VgP/N4+(VgP/N3-VgP/N4)*(2/23) |
| V10P/V53N | VgP/N3+(VgP/N2-VgP/N3)*(20/24) | V42P/V21N | VgP/N4+(VgP/N3-VgP/N4)*(1/23) |
| V11P/V52N | VgP/N3+(VgP/N2-VgP/N3)*(18/24) | V43P/V20N | VgP/N4 |
| V12P/V51N | VgP/N3+(VgP/N2-VgP/N3)*(16/24) | V44P/V19N | VgP/N5+(VgP/N4-VgP/N5)*(22/24) |
| V13P/V50N | VgP/N3+(VgP/N2-VgP/N3)*(14/24) | V45P/V18N | VgP/N5+(VgP/N4-VgP/N5)*(20/24) |
| V14P/V49N | VgP/N3+(VgP/N2-VgP/N3)*(12/24) | V46P/V17N | VgP/N5+(VgP/N4-VgP/N5)*(18/24) |
| V15P/V48N | VgP/N3+(VgP/N2-VgP/N3)*(10/24) | V47P/V16N | VgP/N5+(VgP/N4-VgP/N5)*(16/24) |
| V16P/V47N | VgP/N3+(VgP/N2-VgP/N3)*(8/24) | V48P/V15N | VgP/N5+(VgP/N4-VgP/N5)*(14/24) |
| V17P/V46N | VgP/N3+(VgP/N2-VgP/N3)*(6/24) | V49P/V14N | VgP/N5+(VgP/N4-VgP/N5)*(12/24) |
| V18P/V45N | VgP/N3+(VgP/N2-VgP/N3)*(4/24) | V50P/V13N | VgP/N5+(VgP/N4-VgP/N5)*(10/24) |
| V19P/V44N | VgP/N3+(VgP/N2-VgP/N3)*(2/24) | V51P/V12N | VgP/N5+(VgP/N4-VgP/N5)*(8/24) |
| V20P/V43N | VgP/N3 | V52P/V11N | VgP/N5+(VgP/N4-VgP/N5)*(6/24) |
| V21P/V42N | VgP/N4+(VgP/N3-VgP/N4)*(22/23) | V53P/V10N | VgP/N5+(VgP/N4-VgP/N5)*(4/24) |
| V22P/V41N | VgP/N4+(VgP/N3-VgP/N4)*(21/23) | V54P/V9N | VgP/N5+(VgP/N4-VgP/N5)*(2/24) |
| V23P/V40N | VgP/N4+(VgP/N3-VgP/N4)*(20/23) | V55P/V8N | VgP/N5 |
| V24P/V39N | VgP/N4+(VgP/N3-VgP/N4)*(19/23) | V56P/V7N | VgP/N6+(VgP/N5-VgP/N6)*CB1 |
| V25P/V38N | VgP/N4+(VgP/N3-VgP/N4)*(18/23) | V57P/V6N | VgP/N6+(VgP/N5-VgP/N6)*CB2 |
| V26P/V37N | VgP/N4+(VgP/N3-VgP/N4)*(17/23) | V58P/V5N | VgP/N6+(VgP/N5-VgP/N6)*CB3 |
| V27P/V36N | VgP/N4+(VgP/N3-VgP/N4)*(16/23) | V59P/V4N | VgP/N6+(VgP/N5-VgP/N6)*CB4 |
| V28P/V35N | VgP/N4+(VgP/N3-VgP/N4)*(15/23) | V60P/V3N | VgP/N6+(VgP/N5-VgP/N6)*CB5 |
| V29P/V34N | VgP/N4+(VgP/N3-VgP/N4)*(14/23) | V61P/V2N | VgP/N6+(VgP/N5-VgP/N6)*CB6 |
| V30P/V33N | VgP/N4+(VgP/N3-VgP/N4)*(13/23) | V62P/V1N | VgP/N6 |
| V31P/V32N | VgP/N4+(VgP/N3-VgP/N4)*(12/23) | V63P/V0N | VgP/N7 |

**Table 5. 27 Voltage Calculation Formula of Grayscale Voltage**

| CGM0[1:0] | "00" | "01" | "10" | "11" |
|---|---|---|---|---|
| CT1 | 6/7 | 7.5/10.5 | 10/15 | 8.5/10.5 |
| CT2 | 5/7 | 6/10.5 | 6.67/15 | 6.67/10.5 |
| CT3 | 4/7 | 4/10.5 | 4/15 | 5.0/10.5 |
| CT4 | 3/7 | 3/10.5 | 3/15 | 3.5/10.5 |
| CT5 | 2/7 | 2/10.5 | 2/15 | 2.17/10.5 |
| CT6 | 1/7 | 1/10.5 | 1/15 | 1/10.5 |

| CGM1[1:0] | "00" | "01" | "10" | "11" |
|---|---|---|---|---|
| CB1 | 6/7 | 9.5/10.5 | 14/15 | 9.5/10.5 |
| CB2 | 5/7 | 8.5/10.5 | 13/15 | 8.33/10.5 |
| CB3 | 4/7 | 7.5/10.5 | 12/15 | 7.0/10.5 |
| CB4 | 3/7 | 6.5/10.5 | 11/15 | 5.5/10.5 |
| CB5 | 2/7 | 4.5/10.5 | 8.33/15 | 3.83/10.5 |
| CB6 | 1/7 | 3.0/10.5 | 5/15 | 2.0/10.5 |

**Note:** Negative gamma don't have CGM0/CGM1 setting, the ratio V2~V7 and V56~V61 is automatically mapping from positive side.

**Table 5. 28 Voltage Calculation Formula of Grayscale Voltage V2~V7 and V56~V61**

**Relationship between GRAM Data and Output Level (REV = "0")**

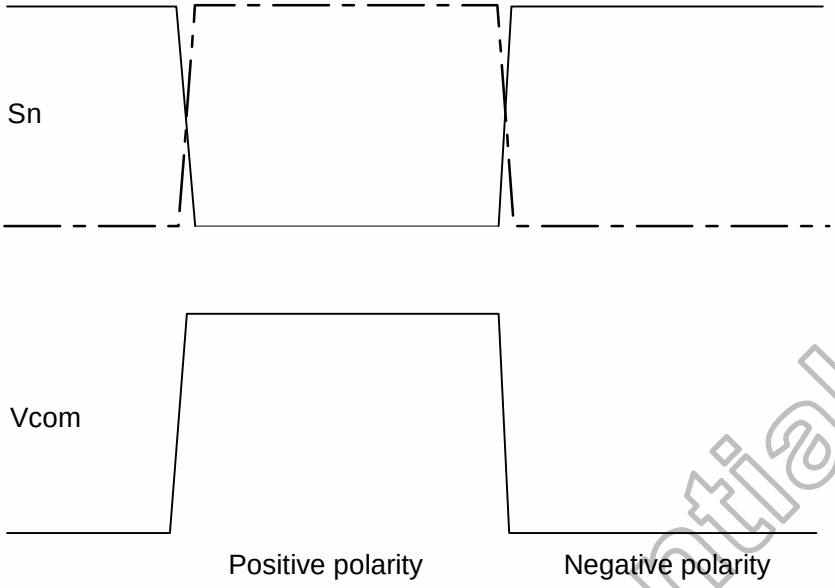
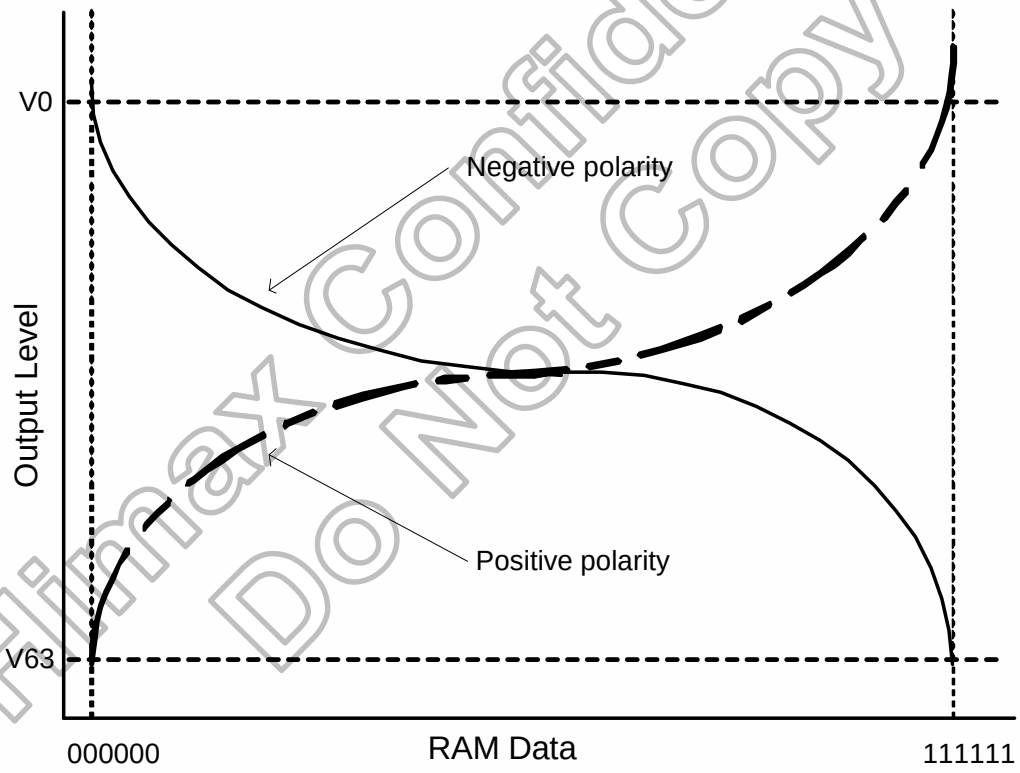



**Figure 5. 58 Relationship between Source Output and Vcom**




(Same characteristic for each RGB)

**Figure 5. 59 Relationship between GRAM Data and Output Level**

### 5.11.6 Gamma Curve Control

There are four kind of Gamma Curve is selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

GC_SEL= Low(VSSD):

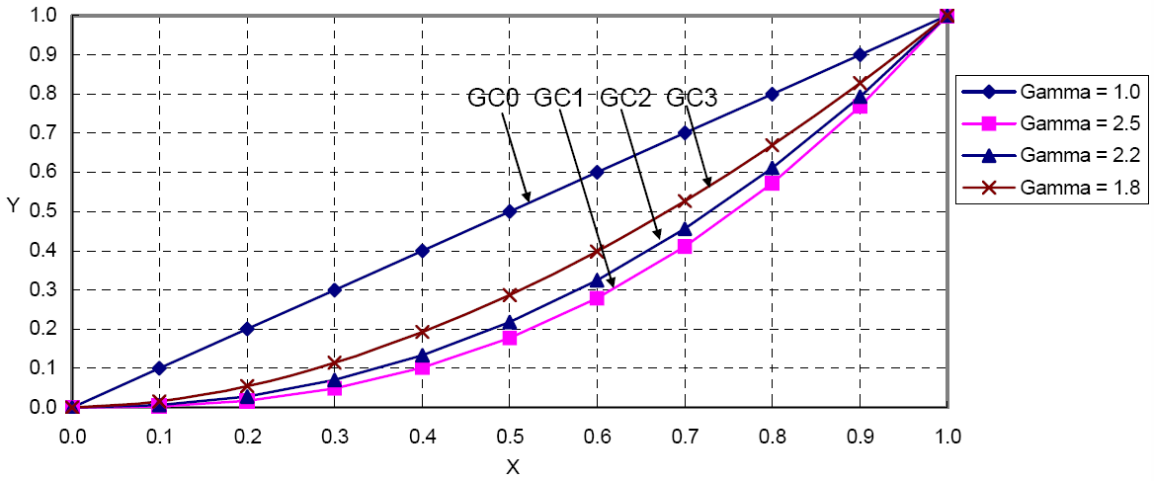
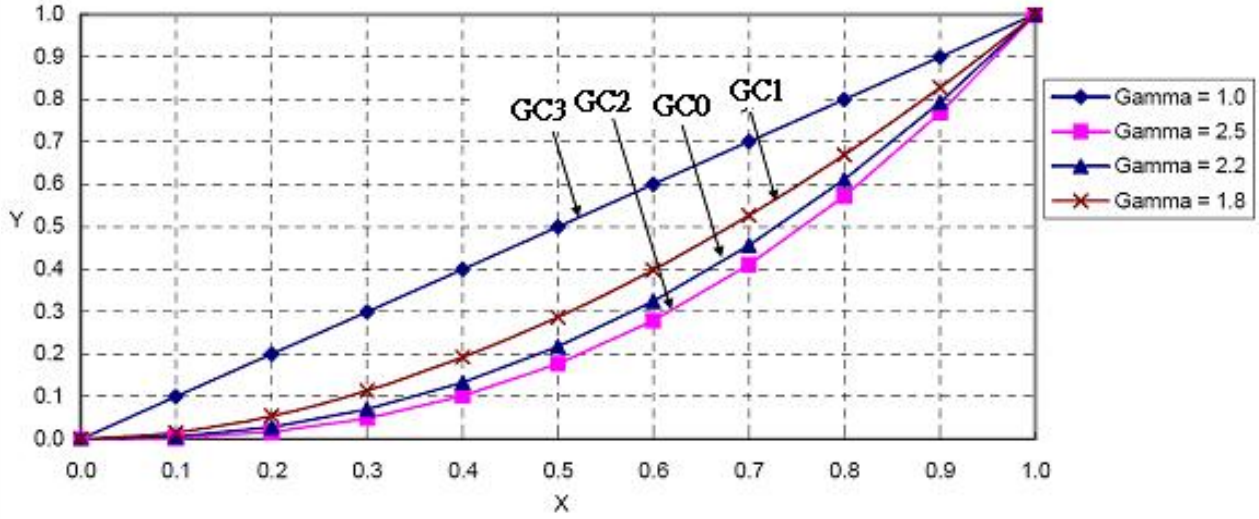



**Figure 5. 60 Gamma Curve according to the GC0 to GC3 bit (GC_SEL=low)**

GC_SEL= high (VDDI):



## 5.12 Oscillator

The HX8353-C can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the CADJ[3:0] and RADJ[2:0] internal register. Please refer to extended command set B0h. The default frequency is 1.5MHz.

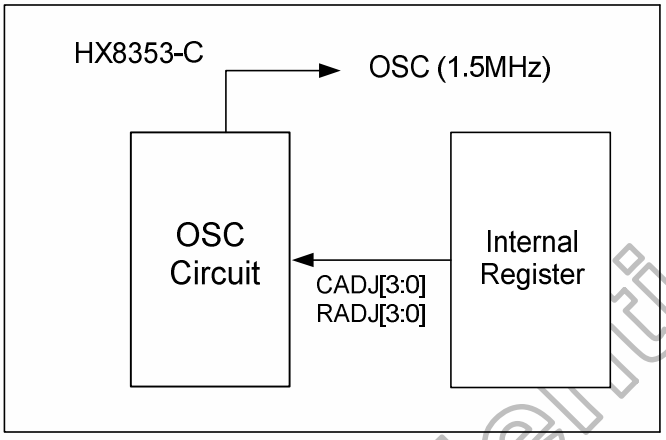



**Figure 5. 61 Oscillation Circuit**

## 5.13 Power On/Off Sequence

VDDI, VDD can be applied in any order. VDDI and VDD can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDDI and VDD must be powered down minimum 120msec after NRESET has been released. During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after NRESET has been released. NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If NRESET line is not held stable by host during Power On Sequence as defined in Sections 5.16.1 and 5.16.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below:

### 5.13.1 Case 1 – NRESET line is hold High or Unstable by Host at Power On

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied - otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

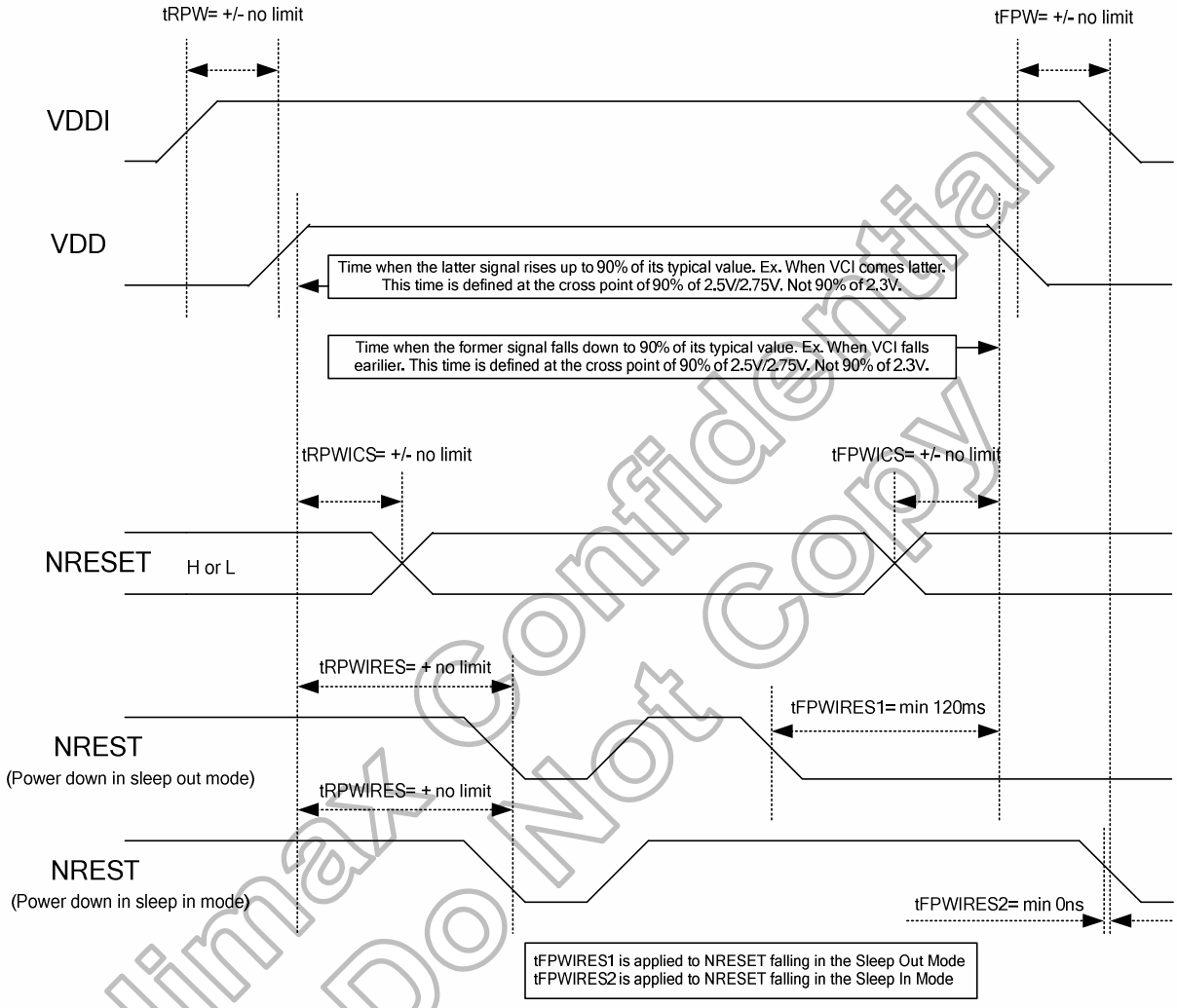



**Figure 5. 62 Case 1 – NRESET line is hold High or Unstable by Host at Power On**

### 5.13.2 Case 2 – NRESET line is held Low by host at Power On

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after both VDD and VDDI have been applied.

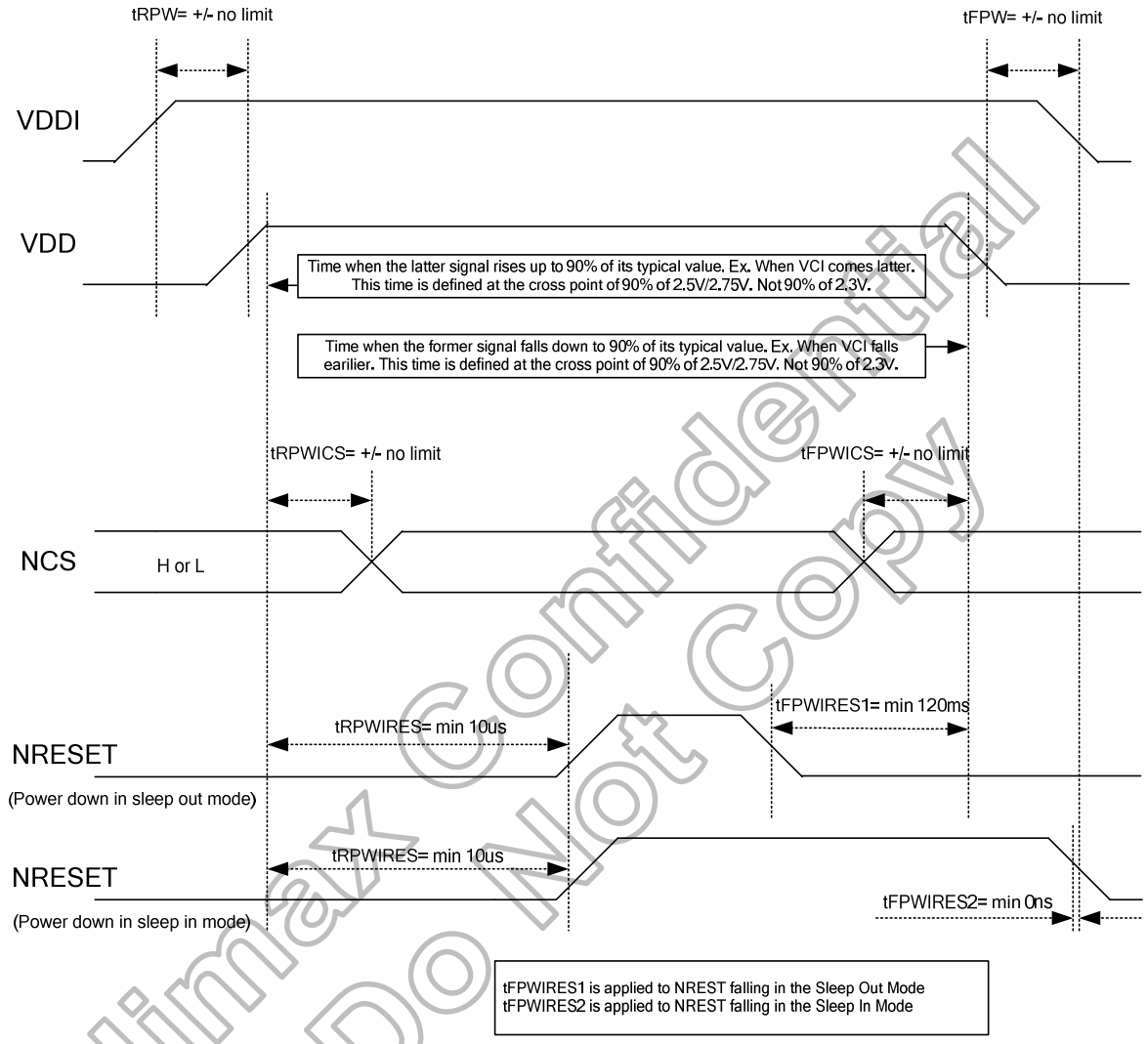



**Figure 5. 63 NRESET line is held Low by host at Power On**

## 5.14 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

## 5.15 Power Flow Chart for Different Power Mode

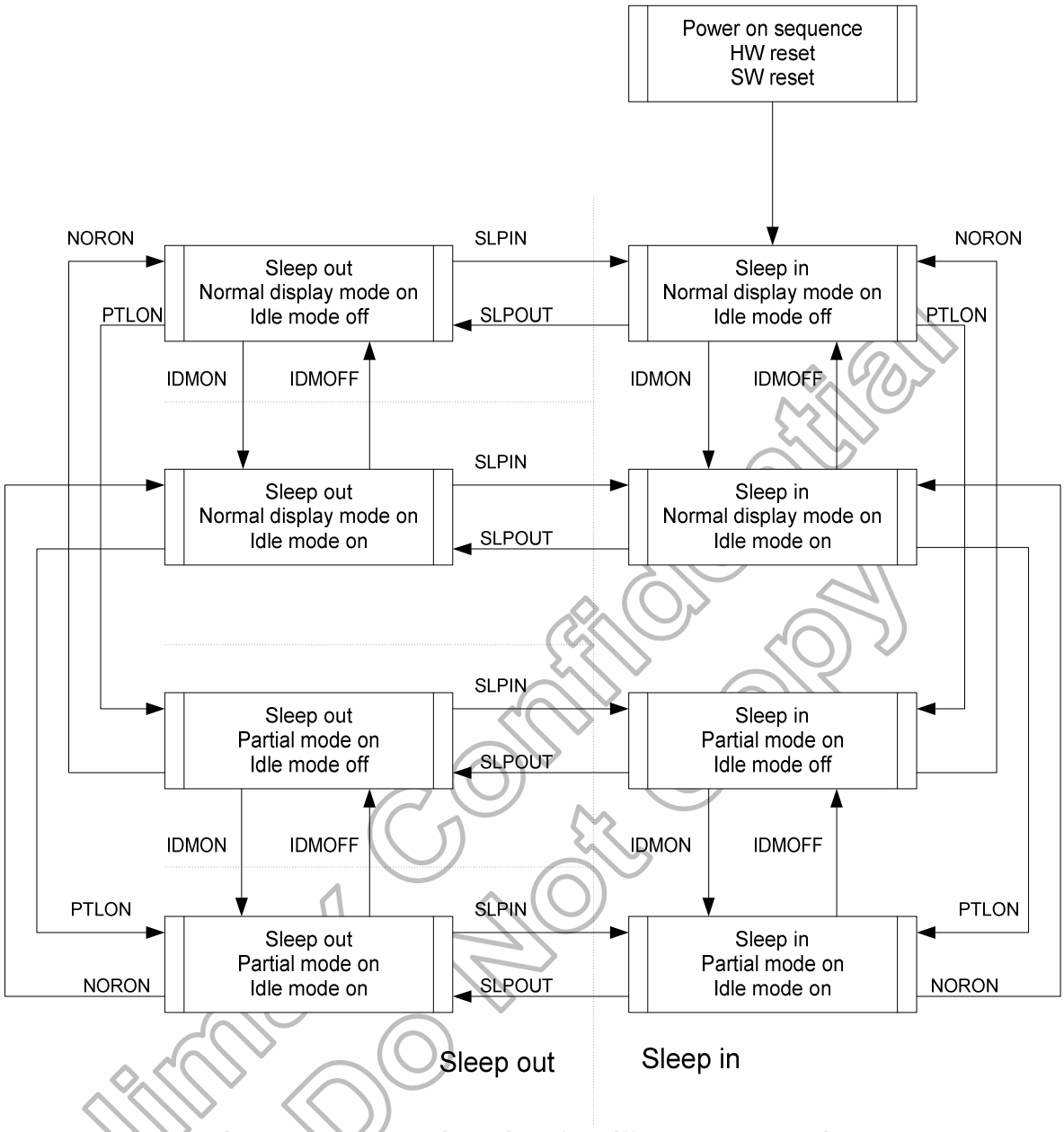



**Figure 5. 64 Power Flow Chart for Different Power Modes**

## 5.16 Input/Output Pin State

### 5.16.1 Output or Bi-directional (I/O) Pins

| Output or Bi-directional pins | After Power On | After Hardware Reset | After Software Reset |
|---|---|---|---|
| TE | Low | Low | Low |
| DB17 to DB0 (Output driver) | High-Z (Inactive) | High-Z (Inactive) | High-Z (Inactive) |
| VTESTOUT | Low | Low | Low |

**Note:** There will be no output from DB17-DB0 during Power On/Off sequence, Hardware Reset and Software Reset.

**Table 5. 29 The State of Output or Bi-directional (I/O) Pins**

### 5.16.2 Input Pins

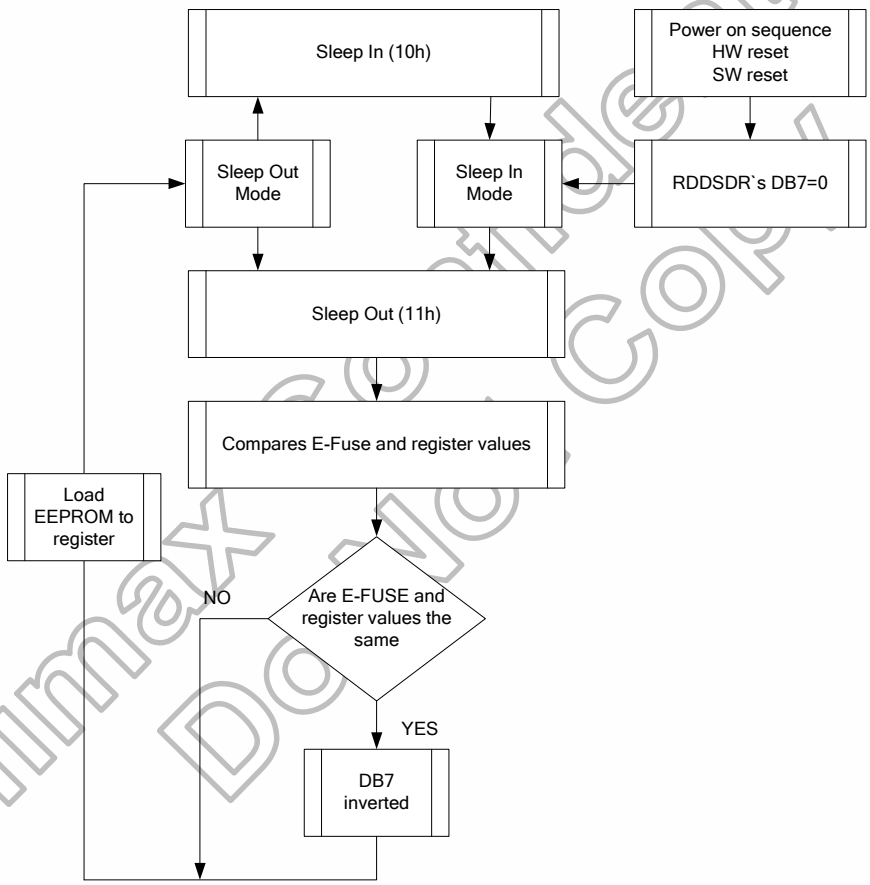
| Input pins | During Power On Process | After Power On | After Hardware Reset | After Software Reset | During Power Off Process |
|---|---|---|---|---|---|
| NRESET | See Section 5.17 | Input valid | Input valid | Input valid | See Section 5.17 |
| NCS | Input valid | Input valid | Input valid | Input valid | Input valid |
| SPI_SEL | Input valid | Input valid | Input valid | Input valid | Input valid |
| GC_SEL | Input valid | Input valid | Input valid | Input valid | Input valid |
| LC_SEL0, LC_SEL1 | Input valid | Input valid | Input valid | Input valid | Input valid |
| DNC_SCL | Input valid | Input valid | Input valid | Input valid | Input valid |
| NWR_RNW | Input valid | Input valid | Input valid | Input valid | Input valid |
| NRD_E | Input valid | Input valid | Input valid | Input valid | Input valid |
| DB17 to DB0 | Input valid | Input valid | Input valid | Input valid | Input valid |
| OSC,P68,BS1,BS2,BS0 | Input valid | Input valid | Input valid | Input valid | Input valid |
| EXTC | Input valid | Input valid | Input valid | Input valid | Input valid |
| TEST1 | Input valid | Input valid | Input valid | Input valid | Input valid |
| TEST2 | Input valid | Input valid | Input valid | Input valid | Input valid |
| TEST3 | Input valid | Input valid | Input valid | Input valid | Input valid |
| RSO0 | Input valid | Input valid | Input valid | Input valid | Input valid |
| RSO1 | Input valid | Input valid | Input valid | Input valid | Input valid |
| RSO2 | Input valid | Input valid | Input valid | Input valid | Input valid |

**Table 5. 30 The State of Input Pins**

## 5.17 Sleep Out – Command and Self-Diagnostic Functions of the Display Module

### 5.17.1 Register loading Detection

Sleep Out-command (See section 6.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly.
There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.2.10 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is DB7). If those both values are not same, this bit (DB7) is not inverted (= increased by 1).
The flow chart for this internal function is following:

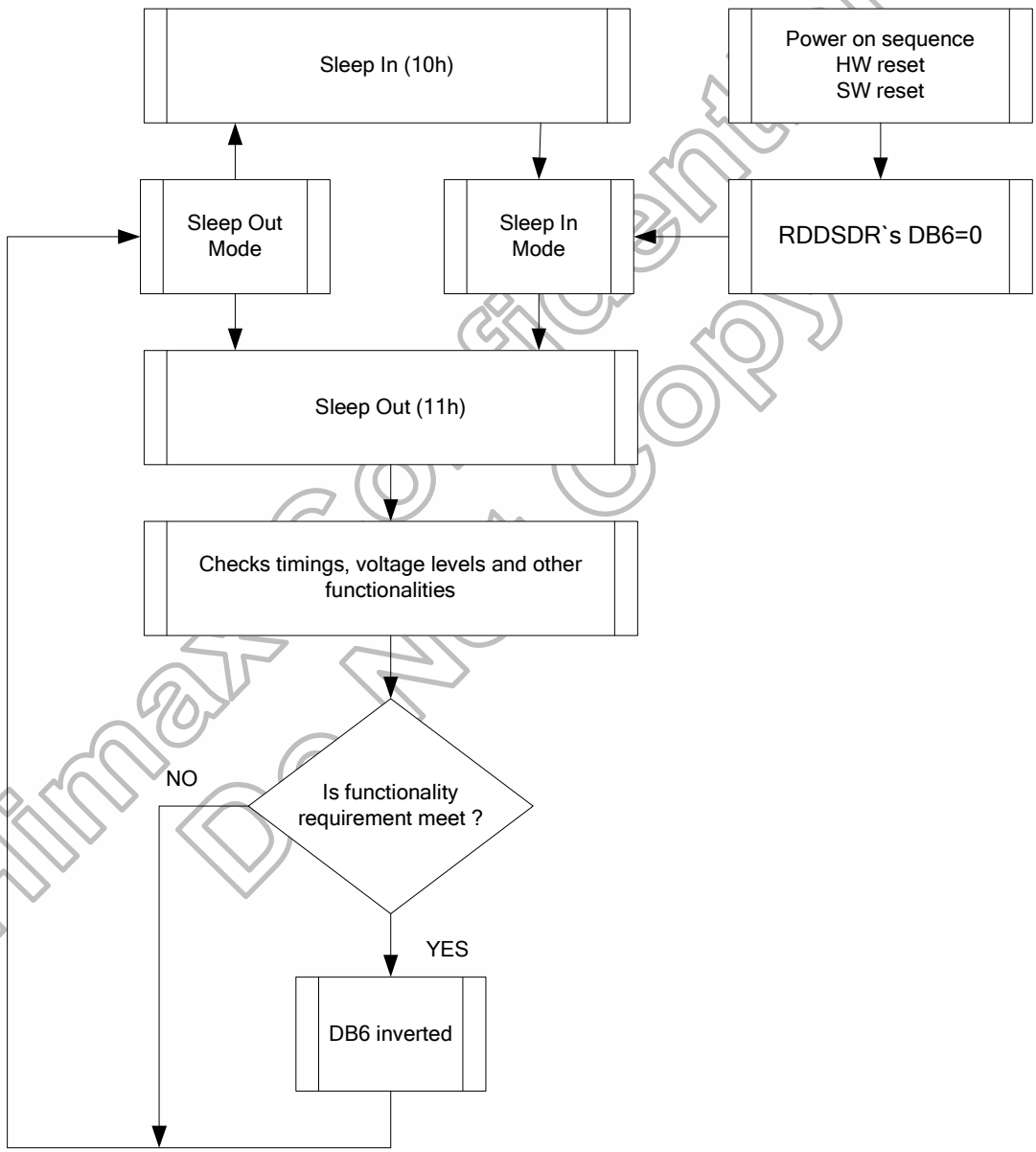



**Note:** There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

**Figure 5. 65 Register loading Detection Flow**

### 5.17.2 Functionality Detection

Sleep Out-command (See section 6.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.
The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 6.2.10 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is DB6). If functionality requirement is not same, this bit (DB6) is not inverted (= increased by 1). The flow chart for this internal function is following:






**Note:** There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s DB6 is valid. Otherwise, there is 5msec delay for DB6’s value, when Sleep Out –command is sent in Sleep Out -mode.

**Figure 5. 66 Functionality Detection Flow**

## 5.18 OTP Programming

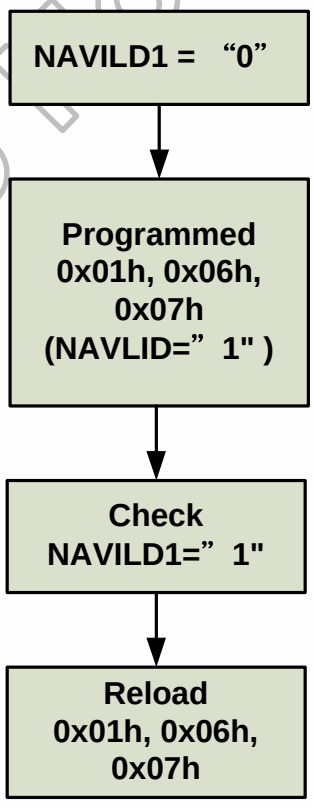
| OTP index | [7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | CADJ[3] | CADJ[2] | CADJ[1] | CADJ[0] | BGP[3] | BGP[2] | BGP[1] | BGP[0] |
| 1 | IDB1[7] | IDB1[6] | IDB1[5] | IDB1[4] | IDB1[3] | IDB1[2] | IDB1[1] | IDB1[0] |
| 2 | NVALID_VCM0 | VCM0[6] | VCM0[5] | VCM0[4] | VCM0[3] | VCM0[2] | VCM0[1] | VCM0[0] |
| 3 | NVALID_VCM1 | VCM1[6] | VCM1[5] | VCM1[4] | VCM1[3] | VCM1[2] | VCM1[1] | VCM1[0] |
| 4 | NVALID_VCM2 | VCM2[6] | VCM2[5] | VCM2[4] | VCM2[3] | VCM2[2] | VCM2[1] | VCM2[0] |
| 5 | LUT_EN | RADJ[1] | RADJ[0] | VDV[4] | VDV[3] | VDV[2] | VDV[1] | VDV[0] |
| 6 | NVALIDB1 | IDB2[6] | IDB2[5] | IDB2[4] | IDB2[3] | IDB2[2] | IDB2[1] | IDB2[0] |
| 7 | IDB3[7] | IDB3[6] | IDB3[5] | IDB3[4] | IDB3[3] | IDB3[2] | IDB3[1] | IDB3[0] |

**Table 5. 31 OTP memory table**

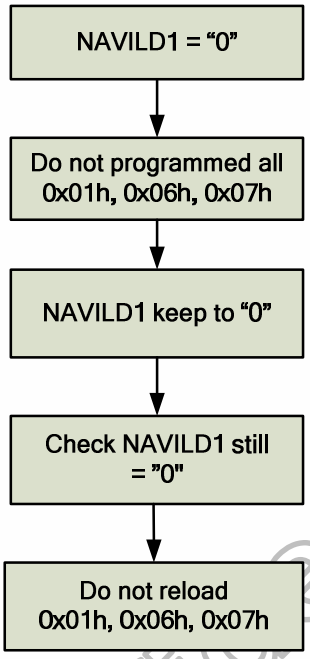
For OSC adjust and BGAP voltage adjust are valid only Himax provide)
For Module suplier program
For Module suplier program
For Module suplier program
For Module suplier program

**Note:** (1) The default value of OTP memory bits are all “0”.
(2) NAVLIDB1, NVALID_VCM[2:0] bit decide the OPT reload Enable/Disable, the default value is “0”. If the own OTP area of NAVILD bit had been programmed, the NAVILD bit will be changed to “1” automatically and execute the OTP reload.

For example:
Condition 1: Programmed all index of 0X01h, 0X06h and 0X07h



Condition 2: Do not program all index of 0X01h, 0X06h and 0X07h




(3) There are some conditions that HX8353-C can reload OTP.
1. Hardware reset
2. Software reset
3. SLPOUT command.

(4) User can use GETOTP command to read back the OTP values. Similarly, the user also can use GETOTP to read the index 0x02h, 0x03h and 0x04h that is defined the NVALID bit for VCM0, VCM1 and VCM2 (NVALID_VCM0, NAVLID_VCM1 and NAVLID_VCM2). User can read back the NVALID_VCM0, NAVLID_VCM1 and NAVLID_VCM2 (use GETOTP command to know how many times of VCM had programmed on OTP.

| | NVALID_VCM2 | NVALID_VCM1 | NVALID_VCM0 |
|---|---|---|---|
| Programed 0 time | 0 | 0 | 0 |
| Programed 1 time | 0 | 0 | 1 |
| Programed 2 times | 0 | 1 | 1 |
| Programed 3 times | 1 | 1 | 1 |

## Programming Flow

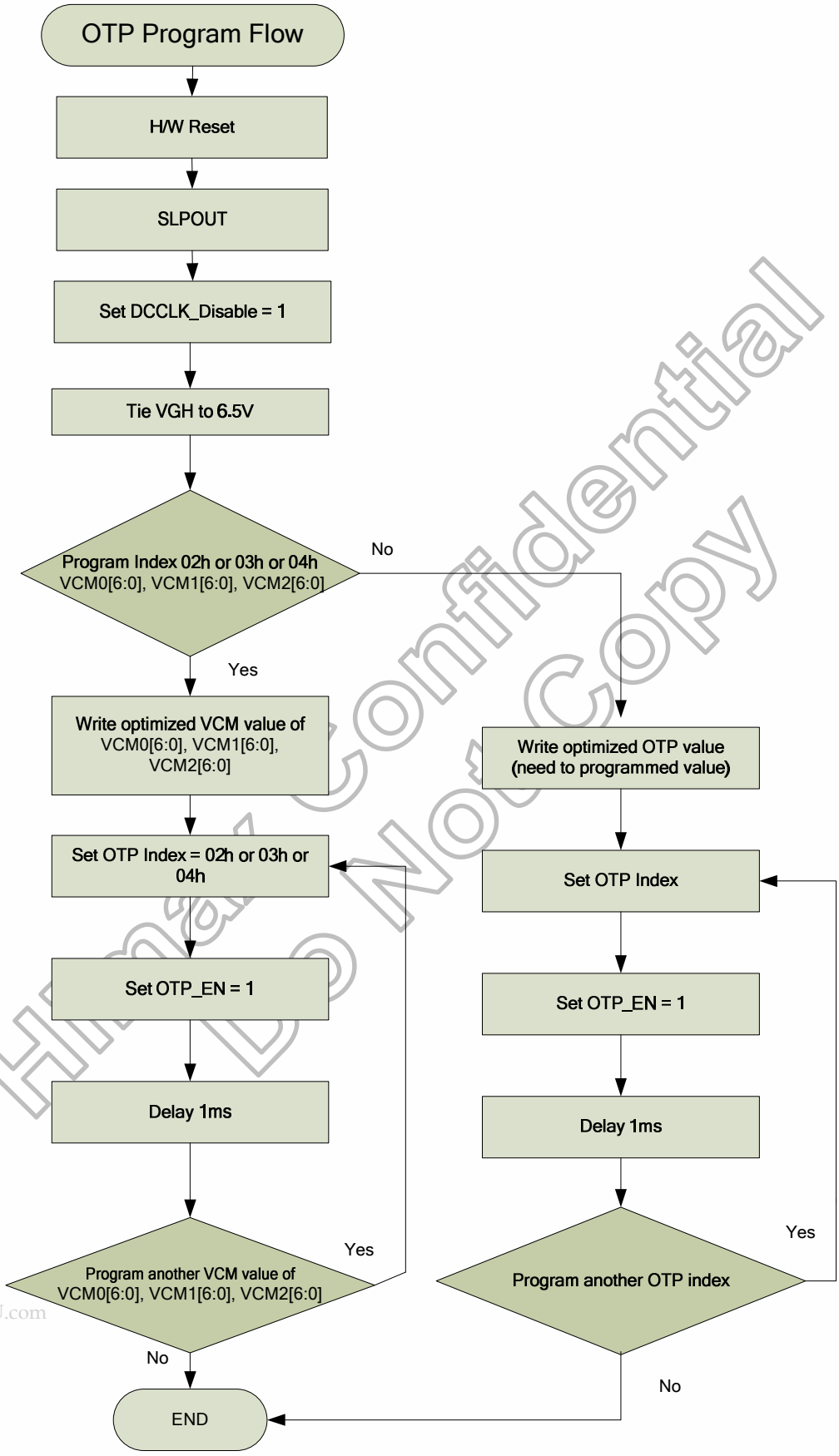
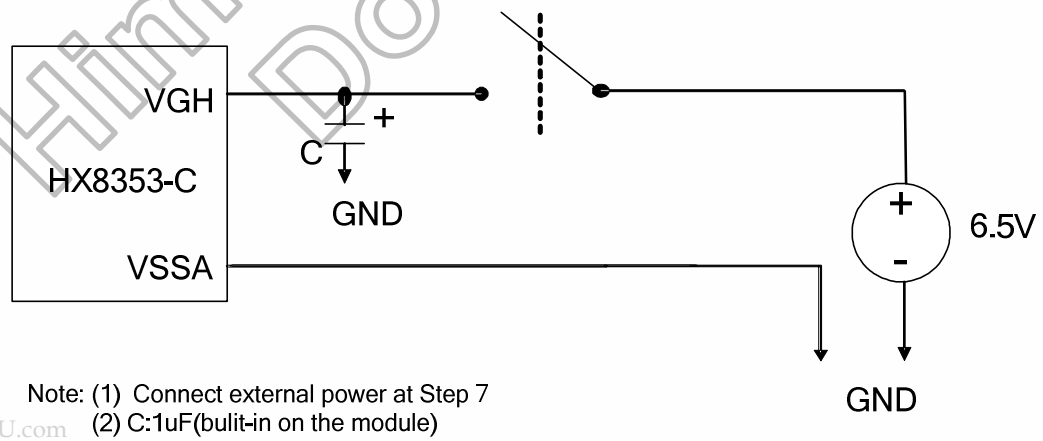



**Figure 5. 67 OTP Programming Flow**

## Programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Set OTP_LOAD_DISABLE=1, disable the auto-loading function.</td></tr>
<tr><td>3</td><td>SLPOUT command (11h)</td></tr>
<tr><td>4</td><td>Wait 120ms</td></tr>
<tr><td>5</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td rowspan="2">SETVCOM (B6h)</td><td>VCM[6:0]</td><td>VcomH voltage for normal mode, Idle mode and Partial Idle mode<br>(High level voltage of VCOM)</td></tr>
<tr><td>VDV[4:0]</td><td>Vcom amplitude (VcomL = VcomH – Vcom amplitude, VcomL ≥ VCL+0.5V)</td></tr>
<tr><td rowspan="3">SETID (C4h)</td><td>IDB1[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>IDB2[6:0]</td><td>LCD module/driver version</td></tr>
<tr><td>IDB3[7:0]</td><td>Identifies the LCD module/driver</td></tr>
</table></td></tr>
<tr><td>6</td><td>Set OTP_ DCCLK_DISABLE=1, disable internal pumping clock.</td></tr>
<tr><td>7</td><td>Connect external power 6.5V to VGH pin</td></tr>
<tr><td>8</td><td>Wait 100ms for external power 6.5V to stabilize.</td></tr>
<tr><td>9</td><td>Specify OTP_index
<table>
<tr><th>OTP_index<br>(Write – For Program)</th><th>OTP_index<br>(Read – For get OTP value)</th><th>Parameter</th></tr>
<tr><td>0x05h</td><td>0x05h</td><td>VDV[4:0],</td></tr>
<tr><td>0x06h</td><td>0x06h</td><td>IDB2[6:0]</td></tr>
<tr><td>0x07h</td><td>0x07h</td><td>IDB3[7:0]</td></tr>
<tr><td>0x01h</td><td>0x01h</td><td>IDB1[7:0]</td></tr>
<tr><td>0x02h</td><td>0x02h</td><td>VCM0[6:0]</td></tr>
<tr><td>0x03h</td><td>0x03h</td><td>VCM1[6:0]</td></tr>
<tr><td>0x04h</td><td>0x04h</td><td>VCM2[6:0]</td></tr>
</table></td></tr>
<tr><td>10</td><td>Set OTP_Mask=0x00h, programming the entire bit of one parameter.</td></tr>
<tr><td>11</td><td>Set OTP_EN=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>12</td><td>Wait 1 ms</td></tr>
<tr><td>13</td><td>Complete programming one parameter to OTP. If continue to programming other parameter, return to step (9). Otherwise, power off the module and remove the external power on VGH pin.</td></tr>
</table>

## Programming circuitry




Note: (1) Connect external power at Step 7
(2) C:1uF(bulit-in on the module)

## 5.19 Free Running Mode Specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in, it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Please note that the black and the white pattern are reversed in case of a normally black display.

| Parameter | Symbol | Description |
|---|---|---|
| Power supply pins | VDDI, VDD | All power supply pins |
| Free running mode | BURN | BURN=1, FR-mode is enabled. |
| Reset | NRESET | Active low pulse in order to start the FR-mode. |
| Chip select(1) | NCS | This pin will be left open during FRM mode. |
| Reads/not write(1) | NWR_RNW | This pin will be left open during FRM mode. |
| Data/not command(1) | DNC_SCL | This pin will be left open during FRM mode. |
| SPI I/F select(1) | SPI_SEL | This pin will be left open during FRM mode. |
| TE select | STE_SEL | This pin will be left open during FRM mode. |
| CPU I/F Data(1) | D[0..17] | This pin will be left open during FRM mode. |
| SPI I/F | SCL | This pin will be left open during FRM mode. |

**Note:** (1) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc, must be disabled, all modes select pins like data-not-command, interface-select etc and all data-bus pins must be set to either logic high or logic low during the FR-mode.

**Table 5. 32 Pin Information**

## Power-on Sequence of Free Running Mode

The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if it is supported by the driver specification. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP starts to load when Reset leaves low to high.

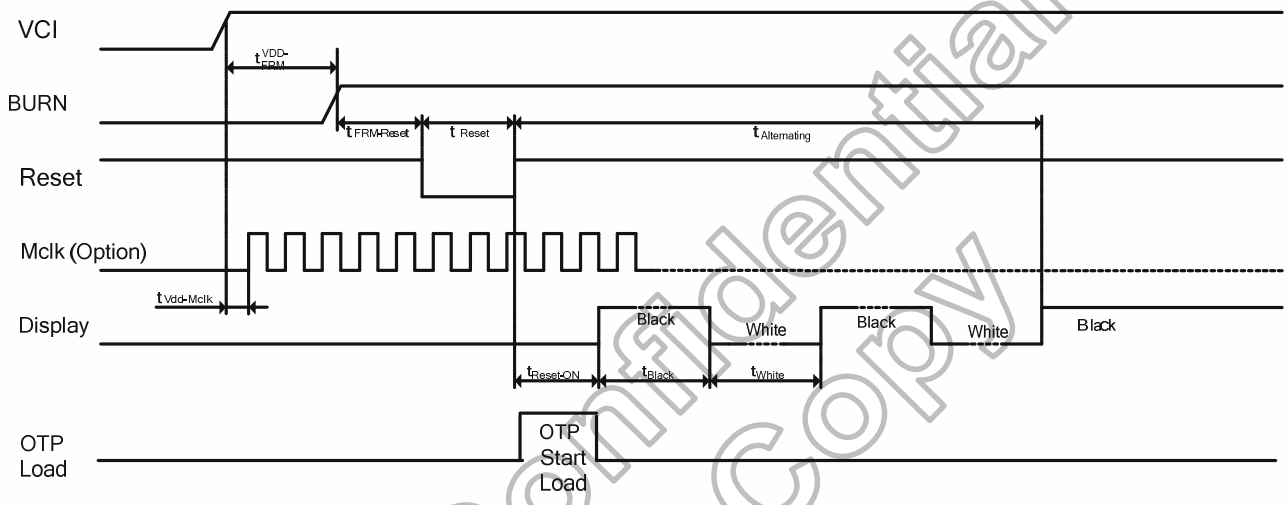



**Figure 5. 68 Power On Sequence of FR-mode (for Normally–White Panel)**

## Power off Sequence of Free Running Mode

The power supply can be switched off any time.

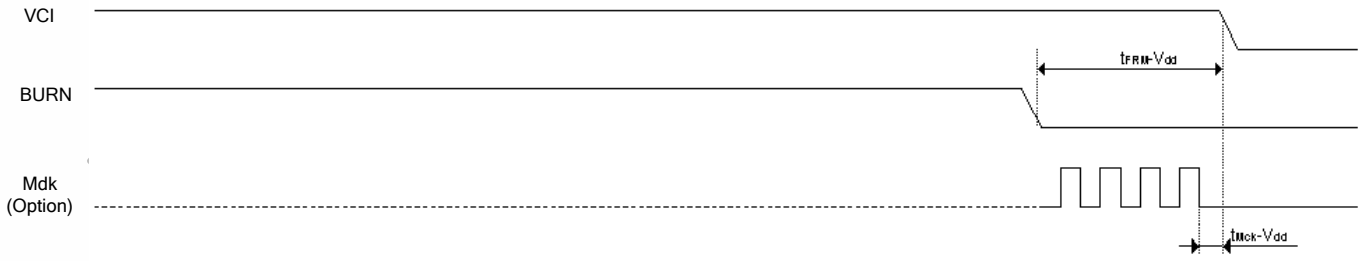



**Figure 5. 69 Power Off Sequence of FR-mode**

## Free Running Mode Display

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shell be 50%/50%. The time of the black and white pattern shell is around 1 second in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. The display is switched to a static black pattern after the alternating mode is finished. Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. The frame frequency will be set according to the parameter in the OTP.

| | | | | | |
|---|---|---|---|---|---|
| **Alternating Black and White Pattern** | $t_{Alternating}$ | - | 5 | - | min |
| **Master Clock Frequency** | $f_{Mclk}$ | - | - | 1.5 | MHz |

**Table 5. 33 Frequency Definition of Free Running Mode Display**

# 6. Command

## 6.1 Command Compare Table

**Table 6. 1 MPU Interface Command Set**

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | NOP | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No Operation |
| 01 | SWRESET | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software reset |
| 04 | RDDIDIF | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Read Display Identification Information |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | xx | xx | xx | xx | xx | xx | xx | xx | IDB1 read |
| | | 1 | 1 | ↑ | - | 1 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | IDB2 read |
| | | 1 | 1 | ↑ | - | xx | xx | xx | xx | xx | xx | xx | xx | IDB3 read |
| 09 | RDDST | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Read Display Status |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[31:24] | | | | | | | | |
| | | 1 | 1 | ↑ | - | D[23:16] | | | | | | | | |
| | | 1 | 1 | ↑ | - | D[15:8] | | | | | | | | |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0A | RDDPM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Read Display Power Mode |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0B | RDDMADCTL | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Read Display MADCTL |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0C | RDDCOLMOD | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Read Display Pixel Format |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0D | RDDIM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | Read Display Image Mode |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0E | RDDSM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Read Display Signal Mode |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |
| 0F | RDDSDR | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Read Display Self-Diagnostic Result |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | D[7:0] | | | | | | | | |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | SLPIN | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Sleep in and charge-pump off |
| 11 | SLPOUT | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Sleep out and charge-pump on |
| 12 | PTLON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Partial Mode On |
| 13 | NORON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Normal Display Mode On |
| 20 | INVOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Display Inversion Off |
| 21 | INVON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Display Inversion On |
| 26 | GAMSET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | Gamma Set |
| | | 1 | ↑ | 1 | - | GC[7:0] | | | | | | | | |
| 28 | DISPOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Display off |
| 29 | DISPON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Display on |
| 2A | CASET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Read Display Status |
| | | 1 | ↑ | 1 | - | SC[15:8] | | | | | | | | Column address start |
| | | 1 | ↑ | 1 | - | SC[7:0] | | | | | | | | Column address start |
| | | 1 | ↑ | 1 | - | EC[15:8] | | | | | | | | Column address end |
| | | 1 | ↑ | 1 | - | EC[7:0] | | | | | | | | Column address end |
| 2B | PASET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Row address set |
| | | 1 | ↑ | 1 | - | SP[15:8] | | | | | | | | Row address start |
| | | 1 | ↑ | 1 | - | SP[7:0] | | | | | | | | Row address start |
| | | 1 | ↑ | 1 | - | EP[15:8] | | | | | | | | Row address end |
| | | 1 | ↑ | 1 | - | EP[7:0] | | | | | | | | Row address end |
| 2C | RAMWR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Memory write |
| | | 1 | ↑ | 1 | | D[15:0] | | | | | | | | Write data |
| 2D | Colour set | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Colour set |
| | | 1 | ↑ | 1 | - | X | X | R005 | R004 | R003 | R002 | R001 | R000 | Total 128 parameters |
| | | 1 | ↑ | 1 | - | X | X | Rnn5 | Rnn4 | Rnn3 | Rnn2 | Rnn1 | Rnn0 | |
| | | 1 | ↑ | 1 | - | X | X | R315 | R314 | R313 | R312 | R311 | R310 | |
| | | 1 | ↑ | 1 | - | X | X | G005 | G004 | G003 | G002 | G001 | G000 | |
| | | 1 | ↑ | 1 | - | X | X | Gnn5 | Gnn4 | Gnn3 | Gnn2 | Gnn1 | Gnn0 | |
| | | 1 | ↑ | 1 | - | X | X | G635 | G634 | G633 | G632 | G631 | G630 | |
| | | 1 | ↑ | 1 | - | X | X | B005 | B004 | B003 | B002 | B001 | B000 | |
| | | 1 | ↑ | 1 | - | X | X | B315 | B314 | B313 | B312 | B311 | B310 | |
| 2E | RAMRD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Memory read |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | D[15:0] | | | | | | | | | Read data |
| 30 | PLTAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Partial start end address set |
| | | 1 | ↑ | 1 | - | SR[15:8] | | | | | | | | Start row |
| | | 1 | ↑ | 1 | - | SR[7:0] | | | | | | | | Start row |
| | | 1 | ↑ | 1 | - | ER[15:8] | | | | | | | | End row |
| | | 1 | ↑ | 1 | - | ER[7:0] | | | | | | | | End row |
| 33 | VSCRDEF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Vertical Scrolling Definition |
| | | 1 | ↑ | 1 | - | TFA15 | TFA14 | TFA13 | TFA12 | TFA11 | TFA10 | TFA9 | TFA8 | |
| | | 1 | ↑ | 1 | - | TFA7 | TFA6 | TFA5 | TFA4 | TFA3 | TFA2 | TFA1 | TFA0 | |
| | | 1 | ↑ | 1 | - | VSA15 | VSA14 | VSA13 | VSA12 | VSA11 | VSA10 | VSA9 | VSA8 | |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | ↑ | 1 | - | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 | |
| | | 1 | ↑ | 1 | - | BFA15 | BFA14 | BFA13 | BFA12 | BFA11 | BFA10 | BFA9 | BFA8 | |
| | | 1 | ↑ | 1 | - | BFA7 | BFA6 | BFA5 | BFA4 | BFA3 | BFA2 | BFA1 | BFA0 | |
| 34 | TEOFF | 0 | ↑ | 1 | | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Tear Effect On/Off |
| 35 | TEON | 0 | ↑ | 1 | | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Tear Effect Mode |
| | | 1 | ↑ | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M(0) | |
| 36 | MADCTL | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Memory Access Control |
| | | 0 | ↑ | 1 | - | MY (0) | MX (0) | MV (0) | ML (0) | BGR (0) | SS (0) | 0 | 0 | |
| 37 | VSCRSADD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Vertical Scrolling Start Address |
| | | 1 | ↑ | 1 | - | VSP15 | VSP14 | VSP13 | VSP12 | VSP11 | VSP10 | VSP9 | VSP8 | |
| | | 1 | ↑ | 1 | - | VSP7 | VSP6 | VSP5 | VSP4 | VSP3 | VSP2 | VSP1 | VSP0 | |
| 38 | IDMOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Idle Mode off |
| 39 | IDMON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Idle Mode on |
| 3A | COLMOD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Interface Pixel Format |
| | | 1 | ↑ | 1 | - | - | CSEL_RGB[2:0] | | | - | CSEL[2:0] | | | |
| DA | RDIDB1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Read IDB1 |
| | | 0 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | module's manufacturer[7:0] | | | | | | | | |
| DB | RDIDB2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | Read IDB2 |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | 1 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | |
| DC | RDIDB3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Read IDB3 |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | Dummy read |
| | | 1 | 1 | ↑ | - | LCD module/driver ID[7:0] | | | | | | | | |

## 6.2 User Define Command List Table

User define command list is available only under “EXTC=1” or enable PASSWDEN command (even EXTC = low), if EXTC=0 (No enable PASSWDEN command )all user define write command is seen as “NOP”, of Hi-Z data bus if any user defined read command.

### 6.2.1 Command List

**Table 6. 2 User Command Set**

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B0 | SETOSC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Set Internal Oscillator |
| | | 1 | ↑ | 1 | - | CADJ[3:0](1000) | | | | UADJ[2:0](001) | | | - | |
| | | 1 | ↑ | 1 | | - | - | - | - | - | - | RADJ[1:0](01) | | |
| | | 1 | ↑ | 1 | - | - | - | - | OSC_EN_CON(0) | - | - | OSC_EN (0) | - | |
| B1 | SETPOWER | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Set power |
| | | 1 | ↑ | 1 | - | GASENB (0) | - | - | PON (0) | DK (1) | - | - | STB(0) | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | AP[2:0] (000) | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | VC1[2:0] (011) | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | VRH[3:0](0100) | | | | |
| | | 1 | ↑ | 1 | - | BT[3:0] (0011) | | | | - | - | - | - | |
| | | 1 | ↑ | 1 | - | - | - | FS1[1:0] (01) | | - | - | FS0[1:0] (00) | | |
| | | 1 | ↑ | 1 | - | N_DC[7:0] (0100_1010) | | | | | | | | |
| | | 1 | ↑ | 1 | - | E_DC[7:0](0100_1010) | | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | DCCLK_SYNC (1) | |
| B2 | SETDISP | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Set display related register |
| | | 1 | ↑ | 1 | - | PT[1:0] (00) | | GON (1) | DTE (0) | D[1:0] (00) | | - | - | |
| | | 1 | ↑ | 1 | - | - | - | - | - | N_BP[3:0] (1101) | | | | |
| | | 1 | ↑ | 1 | | - | - | - | - | N_FP[3:0] (1010) | | | | |
| | | 1 | ↑ | 1 | SAP[7:0] | | | | | | | | | |
| | | 1 | ↑ | 1 | EQS[7:0] | | | | | | | | | |
| | | 1 | ↑ | 1 | EQP[7:0] | | | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | GEN_OFF[3:0] | | | | |
| | | 1 | ↑ | 1 | - | - | - | PTG[1:0] (10) | | ISC[3:0] (0010) | | | | |
| | | 1 | ↑ | 1 | SAP_I[7:0] | | | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | OPTION_DISP(0) | |
| B3 | SETLUT | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (P/H default) |
| | | 1 | 1 | ↑ | - | - | - | LUT_ENB(0) | - | - | - | - | - | |
| B4 | SETCYC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Set Display cycles |
| | | 1 | ↑ | 1 | - | N_RTN[3:0] (1101) | | | | - | N_NW[2:0] (001) | | | |
| | | 1 | ↑ | 1 | - | E_RTN[3:0] (1101) | | | | - | E_NW[2:0] (000) | | | |
| | | 1 | ↑ | 1 | - | - | - | DIV_E[1:0] (00) | | - | - | - | - | |
| | | 1 | ↑ | 1 | - | SON[7:0] (0001_1001) | | | | | | | | |
| | | 1 | ↑ | 1 | - | GDON[7:0] (0001_1110) | | | | | | | | |
| | | 1 | ↑ | 1 | - | GDOF[7:0] (0111_1000) | | | | | | | | |
| B5 | SETBGP | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Set BGP Voltage |
| | | 1 | ↑ | 1 | - | - | - | - | - | BGP[3:0] (1000) | | | | |
| B6 | SETVCOM | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Set VCOM Voltage |
| | | 1 | ↑ | 1 | - | VCOMG (0) | - | - | - | - | - | - | - | |
| | | 1 | ↑ | 1 | - | - | VCMN [6:0] (100_0100) | | | | | | | |
| | | 1 | ↑ | 1 | - | - | - | - | VDV[4:0] (0_1101) | | | | | |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | SETGAMMA | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Set Gamma |
| | | 1 | ↑ | 1 | - | -- | MP1[2:0](101) | | | -- | MP0[2:0](000) | | | |
| | | 1 | ↑ | 1 | - | -- | MP3[2:0](101) | | | -- | MP2[2:0](101) | | | |
| | | 1 | ↑ | 1 | - | -- | MP5[2:0](000) | | | -- | MP4[2:0](101) | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CP0[3:0](0010) | | | | |
| | | 1 | ↑ | 1 | - | CP2[3:0](1001) | | | | CP1[3:0](1111) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CP3[3:0](0101) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CP4[3:0](0010) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | OP0[3:0](0010) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | OP1[4:0](0_0110) | | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CGM1[1:0](10) | | CGM0[1:0](10) | | |
| | | 1 | ↑ | 1 | - | -- | MN1[2:0](111) | | | -- | MN0[2:0](101) | | | |
| | | 1 | ↑ | 1 | - | -- | MN3[2:0](001) | | | -- | MN2[2:0](000) | | | |
| | | 1 | ↑ | 1 | - | -- | MN5[2:0](100) | | | -- | MN4[2:0](000) | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CN0[3:0](0011) | | | | |
| | | 1 | ↑ | 1 | - | CN2[3:0](1000) | | | | CN1[3:0](0011) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CN3[3:0](1111) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | CN4[3:0](0000) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | -- | ON0[3:0](0001) | | | | |
| | | 1 | ↑ | 1 | - | -- | -- | -- | ON1[4:0](1_0111) | | | | | |
| B9 | PASSWDEN | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Pass word enable command |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |
| | | 1 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17H |
| BA | PASSWDDISAB | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Pass word disable command |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BB | SETOTP | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Set OTP |
| | | 1 | ↑ | 1 | - | OTP_ MASK[7:0] (0000_0000) | | | | | | | | |
| | | 1 | ↑ | 1 | - | OTP_INDEX[7:0] (1111_1111) | | | | | | | | |
| | | 1 | ↑ | 1 | - | OTP_LOAD_DISABLE (0) | DCCLK_DISABLE (0) | OTP_POR (0) | OTP_PWE (0) | OTP_EN (0) | OTPTEST_EN(0) | VPP_SEL(0) | OTP_PROG(0) | |
| | | 1 | ↑ | 1 | - | - | - | - | - | OTP_PTM[1:0](00) | | OTP_VRADJ[1:0](00) | | |
| BC | SETVDC | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | Set internal digital and GRAM voltage |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | VDC_SEL[2:0] (010) | | | |
| BD | SETSPULSE | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | Set SRAM Arbiter pulse |
| | | 1 | ↑ | 1 | - | RTBA[13:8](000000) | | | | | | | | |
| | | 1 | ↑ | 1 | - | RTBA[7:0](1101_1011) | | | | | | | | |
| BE | SETPROBE | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | TEST_MODE(0) | TEST_OE(0) | |
| | | 1 | ↑ | 1 | - | PROB[7:0] (8'b0) | | | | | | | | |
| BF | SETPTBA | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | 1 | ↑ | 1 | - | PTBA[15:8] (00100100) | | | | | | | | |
| | | 1 | ↑ | 1 | - | PTBA[7:0] (00000100) | | | | | | | | |
| C0 | SETSTBA | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | ↑ | 1 | - | | | | | | | | STBA[8](1) | |
| | | 1 | ↑ | 1 | - | STBA[7:0] (1000_1011) | | | | | | | | |
| | | 1 | ↑ | 1 | - | VTESTSEL[3:0] (0000) | | | | STESTOE[1:0](00) | | - | - | |
| C1 | SETPFUSE | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | PFUSE(0) | |
| C4 | SETID | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | |
| | | 1 | ↑ | 1 | - | IDB1[7:0] (0100_0111) | | | | | | | | |
| | | 1 | ↑ | 1 | - | - | IDB2[6:0] (000_0001) | | | | | | | |
| | | 1 | ↑ | 1 | - | IDB3[7:0] (0000_0000) | | | | | | | | |
| C6 | SETECO | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | |
| | | | | | | ECO0[7:0] (0000_0000) | | | | | | | | |
| | | 1 | ↑ | 1 | - | ECO1[7:0] (0000_0000) | | | | | | | | |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA | SETMREV | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | |
| | | 1 | ↑ | 1 | - | - | - | - | - | - | - | SFULL(0) | - | For Free Running Mode |
| CB | SETIOOPT | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| | | 1 | ↑ | 1 | - | IO_OPT[7:0] (0101_0101) | | | | | | | | |
| | | 1 | ↑ | 1 | - | IO_OPT2[7:0] (0000_0000) | | | | | | | | IO_OPT2[7:6]=> SDI |
| CC | SETPANEL | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | |
| | | 1 | ↑ | 1 | - | | | | SM_PANEL(0) | SS_PANEL(0) | - | - | - | Set Panel characteristics |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E0 | GETOSC | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Get Internal Oscillator |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | CADJ[3:0] (1000) | | | | UADJ[2:0] (011) | | | - | |
| | | 1 | 1 | ↑ | - | | | | | - | RADJ[2:0] | | | |
| | | 1 | 1 | ↑ | - | - | - | - | OSC_EN_CON (1) | - | - | OSC_EN(0) | - | |
| E1 | GETPOWER | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Get power |
| | | 1 | 1 | ↑ | | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | GASEB(0) | - | - | PON(0) | DK(1) | -- | -- | STB(0) | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | AP[2:0] (000) | | | |
| | | 1 | 1 | ↑ | - | - | | | | - | VC1[2:0] (011) | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | VRH[3:0] (0010) | | | | |
| | | 1 | 1 | ↑ | - | BT[3:0] (0011) | | | | - | - | - | - | |
| | | 1 | 1 | ↑ | - | - | - | FS1[1:0] | | - | - | FS01[1:0] (00) | | |
| | | 1 | 1 | ↑ | - | N_DC[7:0] (0011_0111) | | | | | | | | |
| | | 1 | 1 | ↑ | - | E_DC[7:0] (0011_0111) | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | DCCLK_SYNC(1) | |
| E2 | GETDISP | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Get display related register |
| | | 1 | 1 | ↑ | | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | PT[1:0](00) | | GON(1) | DTE(0) | D[1:0](00) | | 0 | 0 | |
| | | 1 | 1 | ↑ | - | - | - | - | - | N_BP[3:0](1101) | | | | |
| | | 1 | 1 | ↑ | | - | - | - | - | N_FP[3:0] (1010) | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | SAP [7:0] | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | EQS[7:0] | | | | |
| | | 1 | 1 | ↑ | | - | - | - | - | EQP[7:0] | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | GEN_OFF[3:0] | | | | |
| | | 1 | 1 | ↑ | - | | | PTG[1:0](10) | | ISC[3:0] (0010) | | | | |
| | | 1 | 1 | ↑ | | SAP_I[7:0] | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | PTG[1:0] | | ISC[3:0] | | | | |
| | | 1 | 1 | ↑ | - | | | | | | | | OPTION_DISP(0) | |
| E3 | GETLUT | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Get LUT interface related register |
| | | 1 | 1 | ↑ | | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | LUT_EN(0) | - | - | - | - | - | |
| E4 | GETCYC | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Get Display waveform cycle |
| | | 1 | 1 | ↑ | | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | N_RTN[3:0](1101) | | | | - | N_NW[2:0] (001) | | | |
| | | 1 | 1 | ↑ | - | E_RTN[3:0] (1101) | | | | - | E_NW[2:0] (000) | | | |
| | | 1 | 1 | ↑ | - | - | - | DIV_E[1:0] | | | | | | |
| | | 1 | 1 | ↑ | - | SON[7:0](0001_1001) | | | | | | | | |
| | | 1 | 1 | ↑ | - | GDON[7:0] (0001_1110) | | | | | | | | |
| | | 1 | 1 | ↑ | - | GDOF[7:0] (0111_1000) | | | | | | | | |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E5 | GETBGP | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Get BGP Voltage |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | BGP[3:0](1000) | | | | |
| E6 | GETVCOM | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | Get VCOM Voltage |
| | | 1 | 1 | ↑ | - | VCOMG(0) | - | - | - | - | - | - | - | |
| | | 1 | 1 | ↑ | - | - | VCMPN[6:0](101_0101) | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | VDV[4:0] (1_0000) | | | | | |
| E7 | GETGAMMA | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | Get Gamma |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | MP12 | MP11 | MP10 | -- | MP02 | MP01 | MP00 | |
| | | 1 | 1 | ↑ | - | - | MP32 | MP31 | MP30 | -- | MP22 | MP21 | MP20 | |
| | | 1 | 1 | ↑ | - | - | MP52 | MP51 | MP50 | -- | MP42 | MP41 | MP40 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CP03 | CP02 | CP01 | CP00 | |
| | | 1 | 1 | ↑ | - | CP23 | CP22 | CP21 | CP20 | CP13 | CP12 | CP11 | CP10 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CP33 | CP32 | CP31 | CP30 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CP43 | CP42 | CP41 | CP40 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | OP03 | OP02 | OP01 | OP00 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | OP14 | OP13 | OP12 | OP11 | OP10 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CGM1[1:0] | | CGM0[1:0] | | |
| | | 1 | 1 | ↑ | - | - | MN12 | MN11 | MN10 | -- | MN02 | MN01 | MN00 | |
| | | 1 | 1 | ↑ | - | - | MN32 | MN31 | MN30 | -- | MN22 | MN21 | MN20 | |
| | | 1 | 1 | ↑ | - | - | MN52 | MN51 | MN50 | -- | MN42 | MN41 | MN40 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CN03 | CN02 | CN01 | CN00 | |
| | | 1 | 1 | ↑ | - | CN23 | CN22 | CN21 | CN20 | CN13 | CN12 | CN11 | CN10 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | -- | CN32 | CN31 | CN30 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | CN43 | CN42 | CN49 | CN40 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | ON03 | ON02 | ON01 | ON00 | |
| | | 1 | 1 | ↑ | - | - | -- | -- | ON14 | ON13 | ON12 | ON11 | ON10 | |
| E8 | GETCPCRC | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Get CPCRC |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | CPCRC7:0] | | | | | | | | |
| EB | GETOTP | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Get OTP |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | OTP_ MASK[7:0] | | | | | | | | |
| | | 1 | 1 | ↑ | - | OTP_INDEX[7:0] | | | | | | | | |
| | | 1 | 1 | ↑ | - | OTP_LOAD_DISABLE | DCCLK_DISABLE | OTP_POR | OTP_PWE | OTP_EN | OTPEST_ENB | VPP_SEL | OTP_PROG | |
| | | 1 | 1 | ↑ | - | - | -- | -- | -- | OTP_PTM[1:0](00) | | OTP_VRADJ[1:0](00) | | |
| | | 1 | 1 | ↑ | - | OTP_DATA[7:0] | | | | | | | | |
| EC | GETVDC | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | Get internal digital and GRAM voltage |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | VDC_SEL[2:0] | | | |
| ED | GETSPULSE | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | Get SRAM Arbiter pulse |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | RTBA[15:8] | | | | | | | | - |
| | | 1 | 1 | ↑ | | RTBA[7:0] | | | | | | | | |
| EE | GETPROBE | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | TEST_MODE(0) | TEST_OE(0) | |
| | | 1 | 1 | ↑ | - | PROB[7:0](8'b0) | | | | | | | | |
| EF | GETPTBA | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | PTBA[15:8](0010_0100) | | | | | | | | |
| | | 1 | 1 | ↑ | - | PTBA[7:0] (0000_0100) | | | | | | | | |

| (Hex) | Operation Code | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F0 | GETSTBA | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Get Source option |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | | | | | | | | STBA[8] | |
| | | 1 | 1 | ↑ | - | STBA[7:0](1000_1011) | | | | | | | | |
| | | 1 | 1 | ↑ | - | VTESTSEL[3:0](0000) | | | | STESTOE[1:0](00) | | | | |
| | | 1 | 1 | ↑ | - | | | | | | | | | |
| F1 | GETPFUSE | 0 | ↑ | 1 | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | 1 | 1 | ↑ | | - | - | - | - | - | - | - | PFUSE(0) | Get internal OTP |
| F4 | GETHXID | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | Get Himax ID |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | ID_version[7:0](53h) | | | | | | | | |
| | | 1 | 1 | ↑ | | IDB2_version [7:0](0Ch) | | | | | | | | |
| | | 1 | 1 | ↑ | - | VersionID[7:0](00h) | | | | | | | | |
| F6 | GETECO | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | |
| | | 1 | ↑ | 1 | | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | ↑ | 1 | - | ECO0[7:0](8'b0) | | | | | | | | |
| | | 1 | ↑ | 1 | - | ECO1[7:0] (8'b0) | | | | | | | | |
| | | 1 | ↑ | 1 | - | | | | | | | | | |
| FA | GETMREV | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | - | - | - | SFULL(0) | - | For Free Running Mode |
| FB | GETIOOPT | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | IO_OPT[7:0] (0101_0101) | | | | | | | | |
| | | 1 | 1 | ↑ | - | IO_OPT2[7:0] (0000_0000) | | | | | | | | IO_OPT2[7:6]=>SDI |
| FC | GETPANEL | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | GET_PANEL |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | 1 | ↑ | - | - | - | - | SM_PANEL | SS_PANEL | - | - | - | |
| FE | GETWINDOW | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | 1 | ↑ | 1 | | SC[7:0] | | | | | | | | It is for internal use, not open. |
| | | 1 | ↑ | 1 | - | EC[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | SP[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | EP[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | PSL[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | PEL[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | TFA[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | VSA[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | BFA[7:0] | | | | | | | | |
| | | 1 | ↑ | 1 | - | VSP[7:0] | | | | | | | | |
| FF | GETTS | 0 | ↑ | 1 | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | 1 | 1 | ↑ | - | Dummy Read or Dummy Clock | | | | | | | | |
| | | | | | | - | TS[6:0] | | | | | | | It is for internal use, not open. |

**Note**: (1) Undefined commands are treated as NOP (00H) command.
(2) B0 to DB9 and DE to FF are for factory use of display module supplier. User can decide if these commands are available or they are treated as NOP (00H) commands before shipped to User. Default value is NOP(00H). If pin EXTC is tied to high, B0 to DB9 and DE to FF extended command sets are accepted, other extended command sets are discarded.
(3) Commands 10H, 12H, 13H, 20H, 21H, 26H, 28H, 29H, 30H, 36H (Bit B4 only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09H), Read Display Power Mode (0AH), Read Display MADCTL (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In Mode and Sleep Out Mode.
(4) SETGAMMA and GETGAMMA can't be set at the same time.

## 6.3 Command Description

### 6.3.1 NOP

<table>
<tr><td>00 H</td><td colspan="12">NOP (No Operation)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td></td><td colspan="12">This command is an empty command; it does not have any effect on the display module.</td></tr>
<tr><td>Description</td><td colspan="12">However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"></td></tr>
</table>

### 6.3.2 Software Reset (01h)

| 01 H | SWRESET (Software Reset) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command | | | | | | | | | | | |
| | It will be necessary to wait 5msec before sending new command following software reset. | | | | | | | | | | | |
| Restriction | The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence. | | | | | | | | | | | |

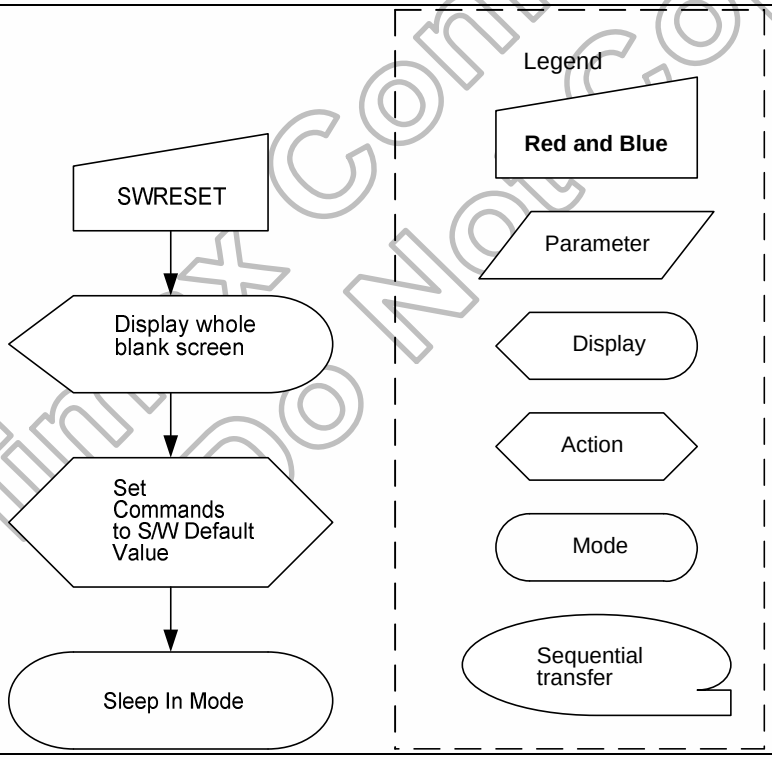
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | N/A |
| S/W Reset | N/A |
| H/W Reset | N/A |

Flow Chart



### 6.3.3 Read Display Identification Information (04h)

| 04 H | RDDIDIF (Read Display Identification Information) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 1st parameter | 1 | 1 | ↑ | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | - |
| 2nd parameter | 1 | 1 | ↑ | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | - |
| 3rd parameter | 1 | 1 | ↑ | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | - |

**Description**

This read byte returns 24-bit display identification information.
The 1st Parameter is dummy read. The 2nd Parameter identifies the LCD module's manufacturer. It is specified by Nokia and for xx is defined as xxHEX.
The 3rd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Color). Bits 6...0 are used to track the LCD module/driver version. It is defined by display supplier (with Nokia's agreement) and it changes each time a revision is made to the display, material or construction specifications. See Table:

| ID Byte Value V[7:0] | Version | Changes |
|---|---|---|
| 80h | | |
| 81h | | |
| 82h | | |
| 83h | | |
| 84h | | |
| 85h | | |

The 4th parameter identifies the LCD module/driver. It is specified by Nokia and for this LCD project module is defined as xxHEX.

**Restriction**

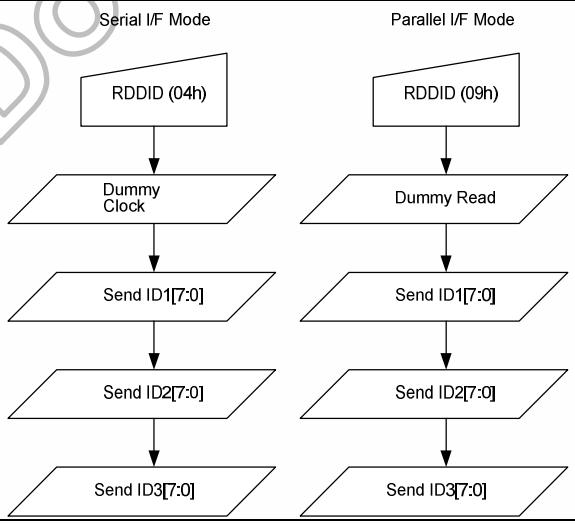
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | See Description |
| S/W Reset | See Description |

**Flow Chart**



### 6.3.4 Read Display Status (09h)

| 09 H | RDDST (Read Display Status) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | - |
| 3rd parameter | 1 | 1 | ↑ | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | - |
| 4th parameter | 1 | 1 | ↑ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | - |
| 5th parameter | 1 | 1 | ↑ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |

Description

This command indicates the current status of the display as described in the table below:

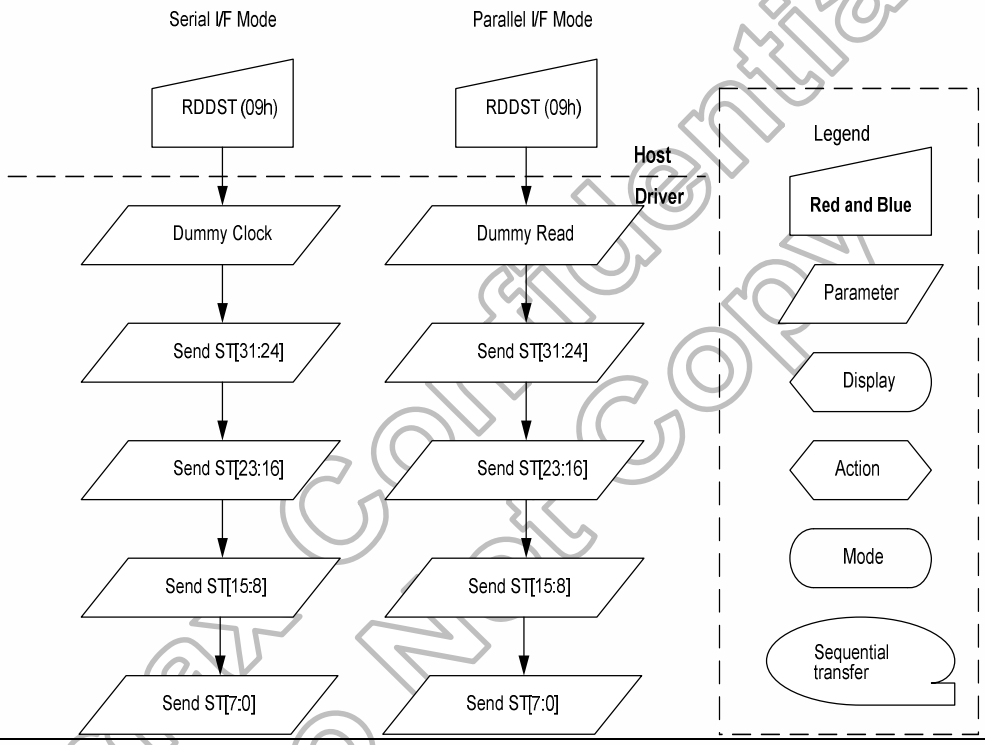
| Bit | Description | Comment |
|---|---|---|
| D31 | Booster Voltage Status | |
| D30 | Page Address Order | |
| D29 | Column Address Order | |
| D28 | Page/Column Order | |
| D27 | Vertical Order | |
| D26 | RGB/BGR Order | |
| D25 | Horizontal Order | |
| D24 | Switching between Segment outputs and RAM | Set to '0' |
| D23 | Switching between Common outputs and RAM | Set to '0' |
| D22 | Interface Color Pixel Format Definition | Set to '1' |
| D21 | | Set to '1' |
| D20 | | Set to '0' |
| D19 | Idle Mode On/Off | |
| D18 | Partial Mode On/Off | |
| D17 | Sleep In/Out | |
| D16 | Display Normal Mode On/Off | |
| D15 | Vertical Scrolling Status | |
| D14 | Horizontal Scrolling Status | Set to '0' |
| D13 | Inversion Status | |
| D12 | All Pixels On | Set to '0' |
| D11 | All Pixels Off | Set to '0' |
| D10 | Display On/Off | |
| D9 | Tearing Effect Line On/Off | |
| D8 | Gamma Curve Selection | |
| D7 | | |
| D6 | | |
| D5 | Tearing Effect Output Line Mode | |
| D4 | For Future Use | Set to '0' |
| D3 | For Future Use | Set to '0' |
| D2 | For Future Use | Set to '0' |
| D1 | For Future Use | Set to '0' |
| D0 | For Future Use | Set to '0' |

Bit Values are explained overleaf.

Bit D31 – Booster Voltage Status
'0' = Booster Off.
'1' = Booster On.
Bit D30 – Page Address Order
'0' = Top to Bottom (When MADCTL DB7='0').
'1' = Bottom to Top (When MADCTL DB7='1').

‘0’ = Left to Right (When MADCTL DB6=’0’).
‘1’ = Right to Left (When MADCTL DB6=’1’).
Bit D28 - Page/Column Order
‘0’ = Normal Mode (When MADCTL B5=’0’).
‘1’ = Reverse Mode (When MADCTL B5=’1’).
Bit D27 – Line Address Order
‘0’ = LCD Refresh Top to Bottom (When MADCTL B4=’0’).
‘1’ = LCD Refresh Bottom to Top (When MADCTL B4=’1’).
Bit D26 – RGB/BGR Order
‘0’ = RGB (When MADCTL B3=’0’).
‘1’ = BGR (When MADCTL B3=’1’).
Note: For Bits DB27, DB26, also refer to Section 9.3.23.
Bit D25 – Display Data Latch Data Order (if this bit is not available, so it is set to ‘0’)
‘0’ = LCD Refresh Left to Right (When MADCTL B2=’0’).
‘1’ = LCD Refresh Right to Left (When MADCTL B2=’1’).
Bit D24 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to ‘0’
Bit D23 – Switching Between Common Outputs and RAM
‘This bit is not applicable for this project, so it is set to ‘0’
Bits D22, DB21, DB20 – Interface Color Pixel Format Definition
Bit D19 – Idle Mode On/Off
‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.
Bit D18 – Partial Mode On/Off
‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.
Bit D17 – Sleep In/Out
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.
Bit D16 – Display Normal Mode On/Off
‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.
Bit D15 – Vertical Scrolling On/Off
‘0’ = Vertical Scrolling is Off.
‘1’ = Vertical Scrolling is On.
Bit D14 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to ‘0’
Bit D13 – Inversion On/Off
‘0’ = Inversion is Off.
‘1’ = Inversion is On.
Bit D12 – All Pixels On
This bit is not applicable for this project, so it is set to ‘0’
Bit D11 – All Pixels Off
This bit is not applicable for this project, so it is set to ‘0’
Bit D10 – Display On/Off
‘0’ = Display is Off.
‘1’ = Display is On.
Bit D9 – Tearing Effect Line On/Off
‘0’ =Tearing Effect Line Off.
‘1’ = Tearing Effect On.
Bits D8, D7, D6 – Gamma Curve Selection

| Gamma Curve Selected | D8 | D7 | D6 | Gamma Set (26h) Parameter |
|---|---|---|---|---|
| Gamma Curve 1 | 0 | 0 | 0 | GC0 |
| Gamma Curve 2 | 0 | 0 | 1 | GC1 |
| Gamma Curve 3 | 0 | 1 | 0 | GC2 |
| Gamma Curve 4 | 0 | 1 | 1 | GC3 |
| Not Defined | 1 | 0 | 0 | Not Defined |
| Not Defined | 1 | 0 | 1 | Not Defined |
| Not Defined | 1 | 1 | 0 | Not Defined |
| Not Defined | 1 | 1 | 1 | Not Defined |

<table>
<tr><td></td><td>Bit D5 – Tearing Effect Line Output Mode.<br>‘0’ = Mode 1, V-Blanking only.<br>‘1’ = Mode 2, both H-Blanking and V-Blanking.<br>Bits D4, D3, D2, D1, D0 are for future use and are set to ‘0’.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>See Description</td></tr>
<tr><td>S/W Reset</td><td>See Description</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

### 6.3.5 Read Display Power Mode (0Ah)

| 0A H | RDDPM (Read Display Power Mode) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | - |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| DB7 | Booster Voltage Status | |
| DB6 | Idle Mode On/Off | |
| DB5 | Partial Mode On/Off | |
| DB4 | Sleep In/Out | |
| DB 3 | Display Normal Mode On/Off | |
| DB2 | Display On/Off | |
| DB1 | Not Defined | Set to '0' |
| DB0 | Not Defined | Set to '0' |

Bit DB7 – Booster Voltage Status
'0' = Booster Off or has a fault.
'1' = Booster On and working OK (Meets Nokia's optical requirements).
Bit DB6 - Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit DB5 – Partial Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit DB4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit DB3 – Display Normal Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
Bit DB2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.

Restrictions

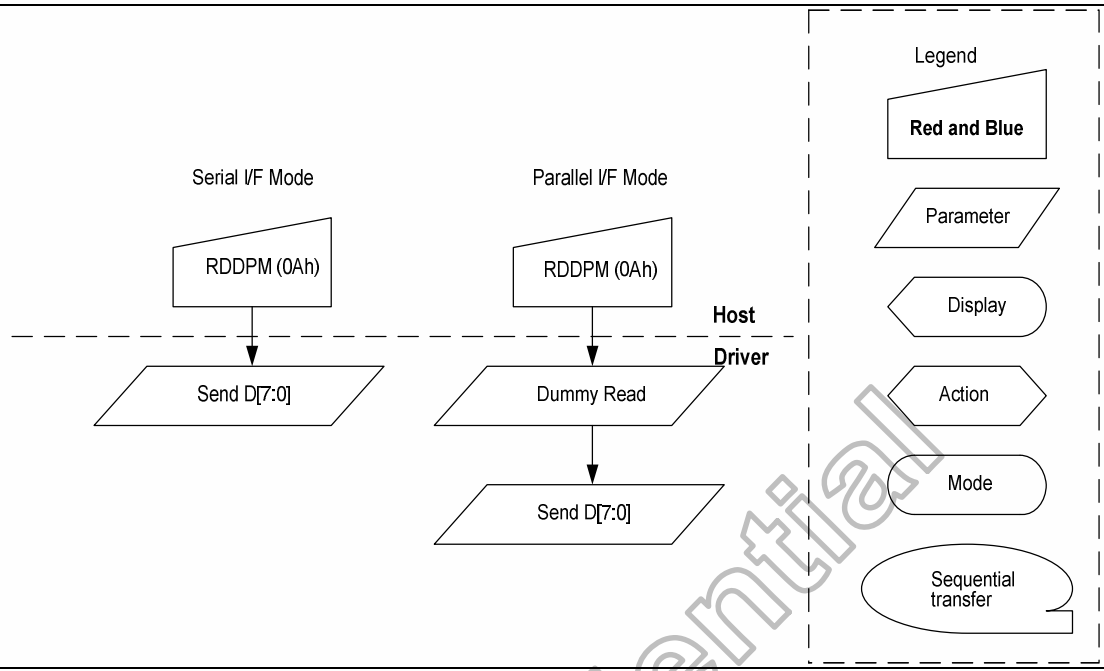
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 08HEX |
| S/W Reset | 08HEX |
| H/W Reset | 08HEX |

Flow Chart



### 6.3.6 Read Display MADCTL (0Bh)

| 0B H | RDDMADCTL (Read Display MADCTL) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| 1st parameter | 1 | 1 | ↑ | xx | xx | xx | xx | xx | xx | xx | xx | xx |
| 2nd parameter | 1 | 1 | ↑ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | 0 | 0 | xx |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| DB7 | Page Address Order | |
| DB6 | Column Address Order | |
| DB5 | Page/Column Order | |
| DB4 | Line Address Order | |
| DB3 | RGB/BGR Order | |
| DB2 | Display Data Latch Order | |
| DB1 | Switching between Segment outputs and RAM | Set to '0' |
| DB0 | Switching between Common outputs and RAM | Set to '0' |

Bit DB7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit DB6 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit DB5 - Page/Column Order
'0' = Normal Mode (When MADCTL B5='0').
'1' = Reverse Mode (When MADCTL B5='1').
Note: For Bits DB7 to DB5, also refer to Section 8.2.3 MCU to memory write/read direction.
Bit DB4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit DB3 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').
Note: For Bits DB4 and DB3 also refer to 9.2.29 Memory Access Control (36h).
Bit DB2 – Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit DB1 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to '0'
Bit DB0 – Switching Between Common Outputs and RAM

**Restrictions**

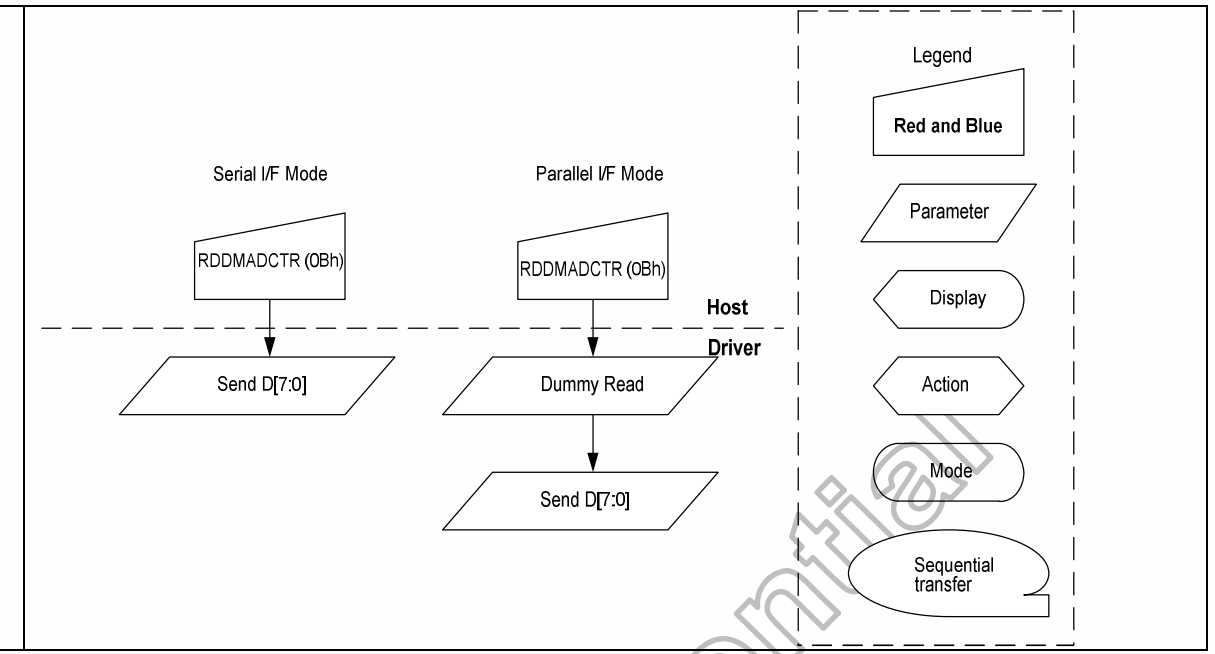
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00HEX |
| S/W Reset | No Change |
| H/W Reset | 00HEX |

Flow Chart



### 6.3.7 Read Display Pixel Format (0Ch)

| 0C H | RDDCOLMOD (Read Display COLMOD) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | - |

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Comment |
|---|---|---|
| DB7 | RGB Interface Colour Format | Set to '0' |
| DB6 | | Set to '0' |
| DB5 | | Set to '0' |
| DB4 | | Set to '0' |
| DB3 | Control Interface Colour Format | |
| DB2 | | |
| DB1 | | |
| DB0 | | |

Bit DB7 – RGB Interface Colour Format Selection
This bit is not applicable for this project, so it is set to '0'.
Bits DB6, DB5, DB4 – RGB Interface Colour Pixel Format Definition
These bits are not applicable for this project, so they are set to '0's.
Bit DB3 – Control Interface Colour Format Selection
This bit is not applicable for this project, so it is set to '0'.
Bit DB2, DB1, DB0 – Control Interface Colour Pixel Format Definition.
These bits are not applicable for this project, so they are set to '110'.

**Restrictions**

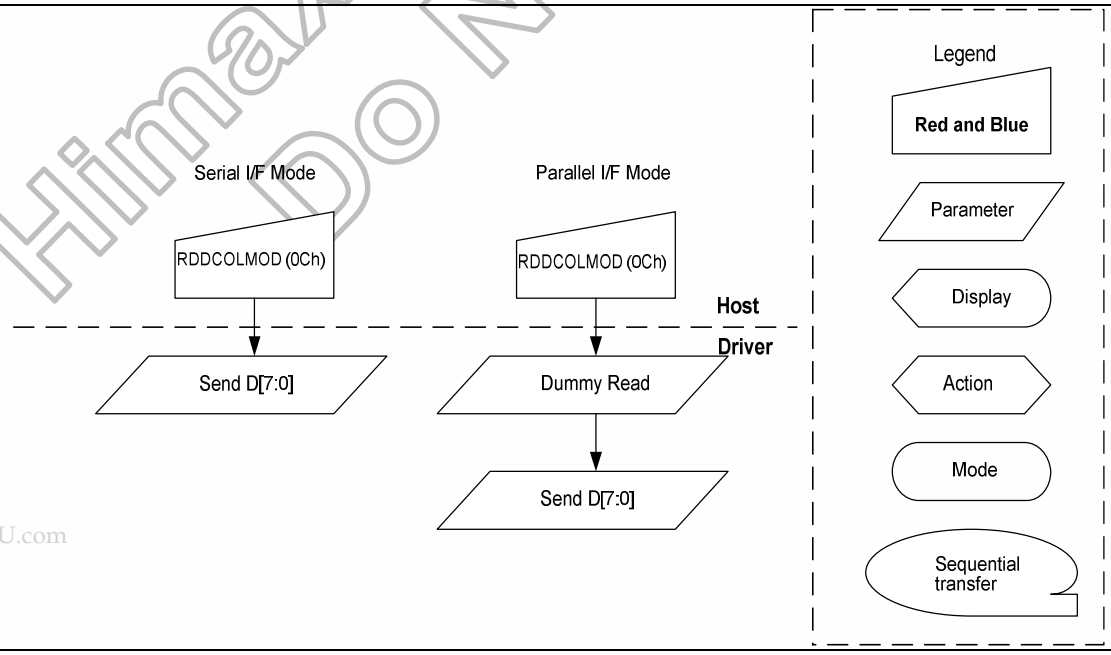
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 16 bit/pixel |
| S/W Reset | No Change |

**Flow Chart**



### 6.3.8 Read Display Image Mode (0Dh)

| 0D H | RDDIM (Read Display Image Mode) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | - |

**Description**

This command indicates the current status of the display as described in the table below:

- Bit DB7 – Vertical Scrolling On/Off
  ‘0’ = Vertical Scrolling is Off.
  ‘1’ = Vertical Scrolling is On.
- Bit DB6 – Horizontal Scrolling Status
  This bit is not applicable for this project, so it is set to ‘0’
- Bit DB5 – Inversion On/Off
  ‘0’ = Inversion is Off.
  ‘1’ = Inversion is On.
- Bit DB4 – All Pixels On
  This bit is not applicable for this project, so it is set to ‘0’
- Bit DB3 – All Pixels Off
  This bit is not applicable for this project, so it is set to ‘0’
- Bits DB2, DB1, DB0 – Gamma Curve Selection

| Gamma Curve Selected | DB 2 | DB 1 | DB 0 | Gamma Set (26h) Parameter |
|---|---|---|---|---|
| Gamma Curve 1 | 0 | 0 | 0 | GC0 |
| Gamma Curve 2 | 0 | 0 | 1 | GC1 |
| Gamma Curve 3 | 0 | 1 | 0 | GC2 |
| Gamma Curve 4 | 0 | 1 | 1 | GC3 |
| Not Defined | 1 | 0 | 0 | Not Defined |
| Not Defined | 1 | 0 | 1 | Not Defined |
| Not Defined | 1 | 1 | 0 | Not Defined |

**Restrictions**

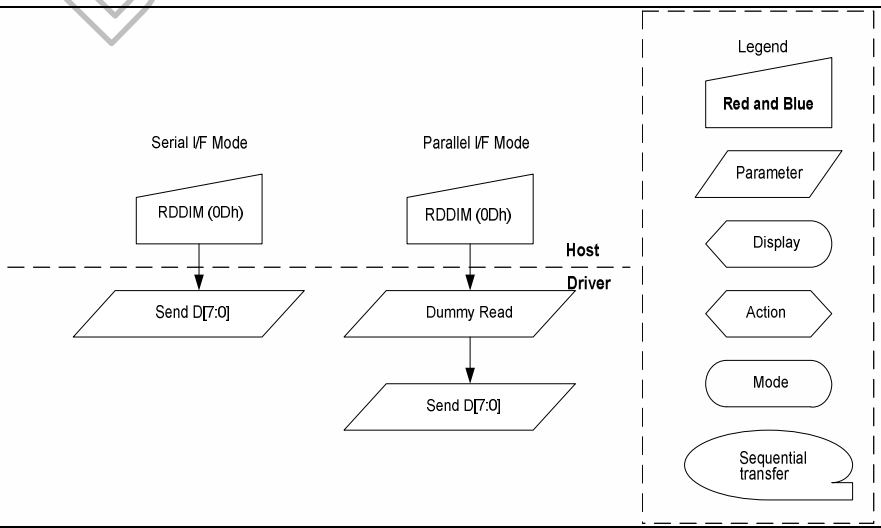
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00HEX |
| S/W Reset | 00HEX |

**Flow Chart**



### 6.3.9 Read Display Signal Mode (0Eh)

| 0E H | RDDSM (Read Display Signal Mode) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | - |

**Description**

This command indicates the current status of the display as described in the table below:

- Bit DB7 – Tearing Effect Line On/Off
  - '0' = Tearing Effect Line Off.
  - '1' = Tearing Effect On.
- Bit DB6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions.
  - '0' = Mode 1.
  - '1' = Mode 2.
- Bit DB5 – Horizontal Sync. (RGB I/F) On/Off
  - This bit is not applicable for this project, so it is set to '0'
- Bit DB4 – Vertical Sync. (RGB I/F) On/Off
  - This bit is not applicable for this project, so it is set to '0'
- Bit DB3 – Pixel Clock (PCLK, RGB I/F) On/Off
  - This bit is not applicable for this project, so it is set to '0'
- Bit DB2 – Data Enable (DE, RGB I/F)) On/Off
  - This bit is not applicable for this project, so it is set to '0'
- DB1 are DB0 - are for future use and are set to '0'.

**Restrictions**

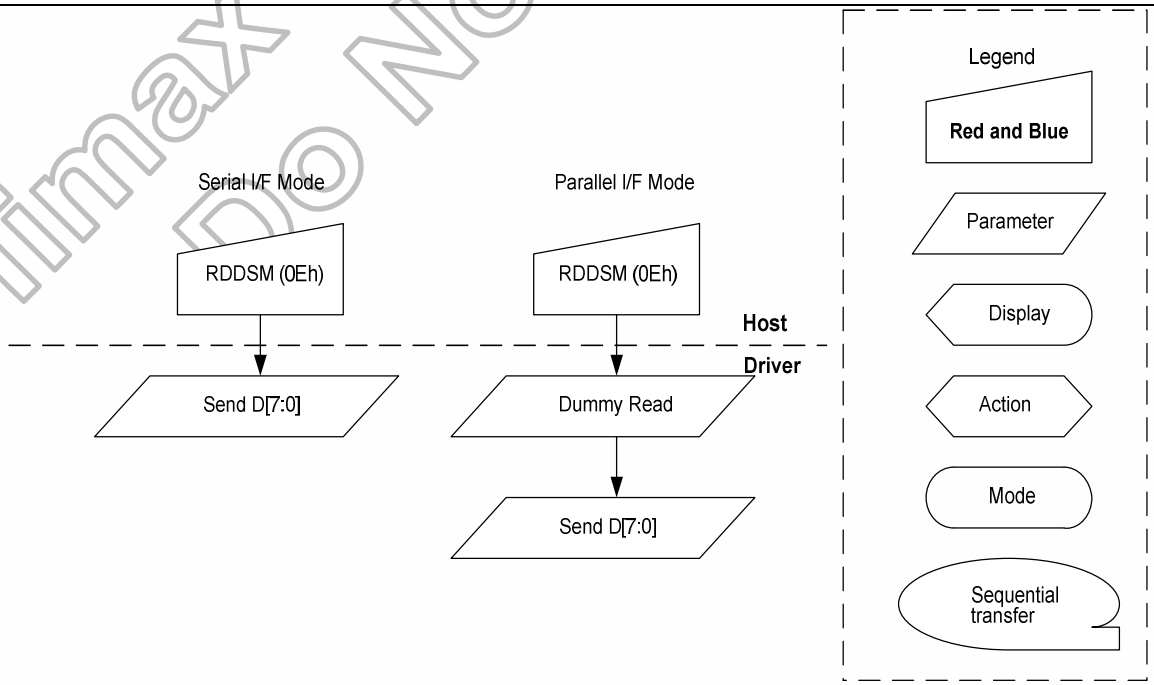
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00HEX |
| S/W Reset | 00HEX |

**Flow Chart**



### 6.3.10 Read Display Self-Diagnostic Result (0Fh)

| 0F H | RDDSDR (Read Display Self-Diagnostic Result) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 1st parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | ↑ | 1 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | - |
| | This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below: | | | | | | | | | | | |
| Description | ■ Bit DB7 – Register Loading Detection See section 5.17.1<br>■ Bit DB6 – Functionality Detection See section 5.17.2.<br>■ Bit DB5 – Chip Attachment Detection Set bit DB5 to '0', if this function is not implemented.<br>■ Bit DB4 – Display Glass Break Detection. Set bit DB4 to '0', if this function is not implemented.<br>■ Bits DB3, DB2, DB1 and DB0 are for future use and are set to '0'. | | | | | | | | | | | |
| Restrictions | | | | | | | | | | | | |

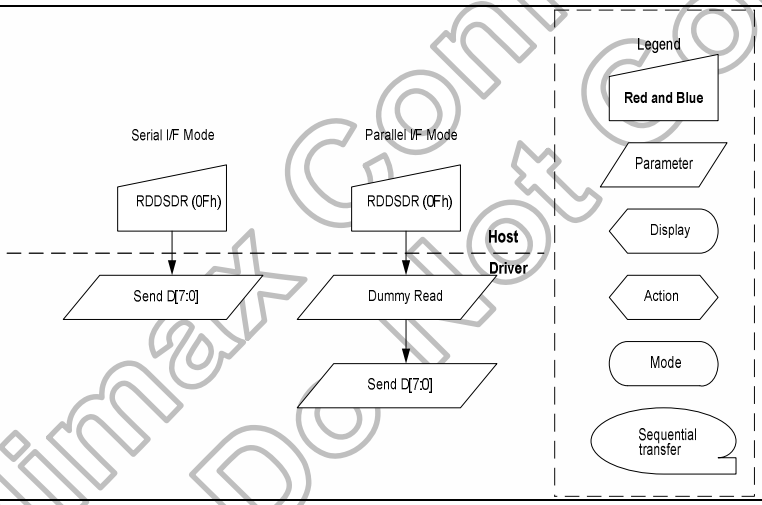
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

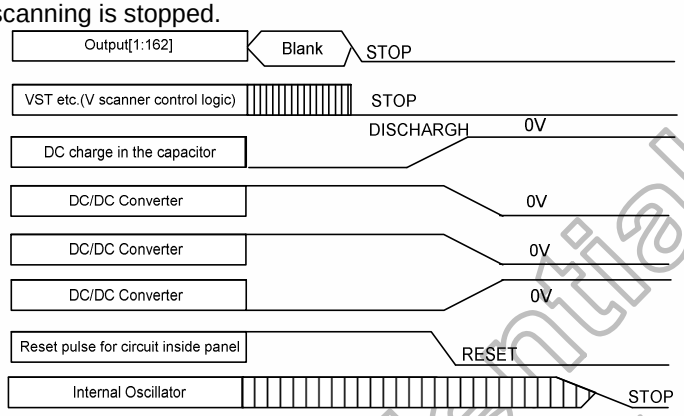
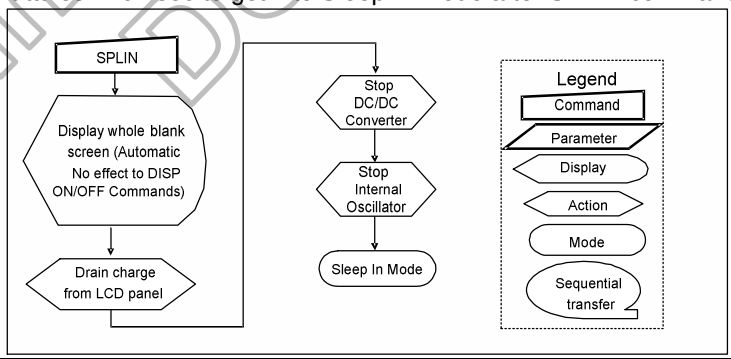
Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00HEX |
| S/W Reset | 00HEX |
| H/W Reset | 00HEX |

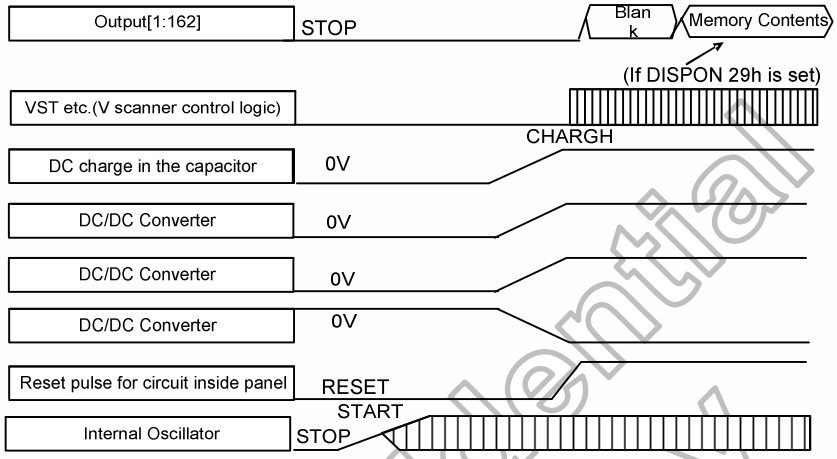
Flow Chart

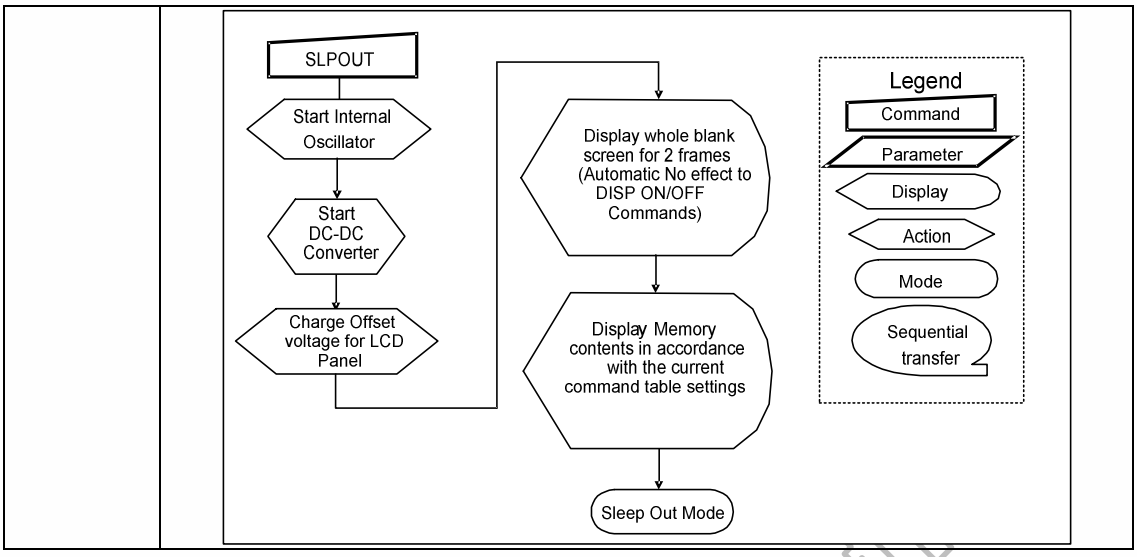


### 6.3.11 Sleep In (10h)

| 10 H | SLPIN (Sleep In) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.<br>  <br><br>MCU interface and memory are still working and the memory keeps its contents.<br>See also section 5.13. | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).<br>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.<br>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. | | | | | | | | | | | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In or Booster Off: Yes | | | | | | | | | | | |
| Default | Status / Default Value<br>Power On Sequence: Sleep in mode<br>S/W Reset: Sleep in mode<br>H/W Reset: Sleep in mode | | | | | | | | | | | |
| Flow Chart | It takes 120msec to get into Sleep In mode after SLPIN command issued.<br>  <br> | | | | | | | | | | | |

### 6.3.12 Sleep Out (11h)

| 11 H | SLPOUT (Sleep Out) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command turns off sleep mode.<br>In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.<br>  <br><br>See also section 5.13 | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).<br>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.<br>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.<br>The display module is doing self-diagnostic functions during this 5msec. See also section 8.10.<br>It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent. | | | | | | | | | | | |
| Register Availability | Status | Availability | | | | | | | | | | |
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | |
| | Sleep In or Booster Off | Yes | | | | | | | | | | |
| Default | Status | Default Value | | | | | | | | | | |
| | Power On Sequence | Sleep In Mode | | | | | | | | | | |
| | S/W Reset | Sleep In Mode | | | | | | | | | | |
| Flow Chart | It takes 120msec to become Sleep Out mode after SLPOUT command issued. | | | | | | | | | | | |



### 6.3.13 Partial Mode On (12h)

| **12 H** | PTLON (Partial Mode On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.<br>See also section 8.6.2. | | | | | | | | | | | |
| Restrictions | This command has no effect when Partial mode is active. | | | | | | | | | | | |
| Register Availability | Status | Availability | | | | | | | | | | |
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes | | | | | | | | | | |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes | | | | | | | | | | |
| Default | Status | Default Value | | | | | | | | | | |
| | Power On Sequence | Normal Mode On | | | | | | | | | | |
| | S/W Reset | Normal Mode On | | | | | | | | | | |
| Flow Chart | See Partial Area (30h) | | | | | | | | | | | |

### 6.3.14 Normal Display Mode On (13h)

| **13 H** | NORON (Normal Display Mode On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. | | | | | | | | | | | |
| Restriction | This command has no effect when Normal Display mode is active. | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | |

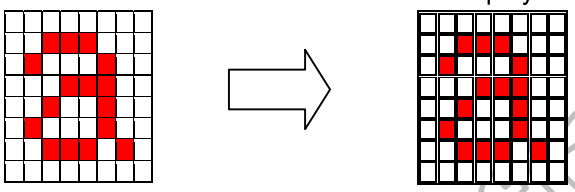
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Normal Mode On |
| S/W Reset | Normal Mode On |

| Flow Chart | See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command. |
|---|---|

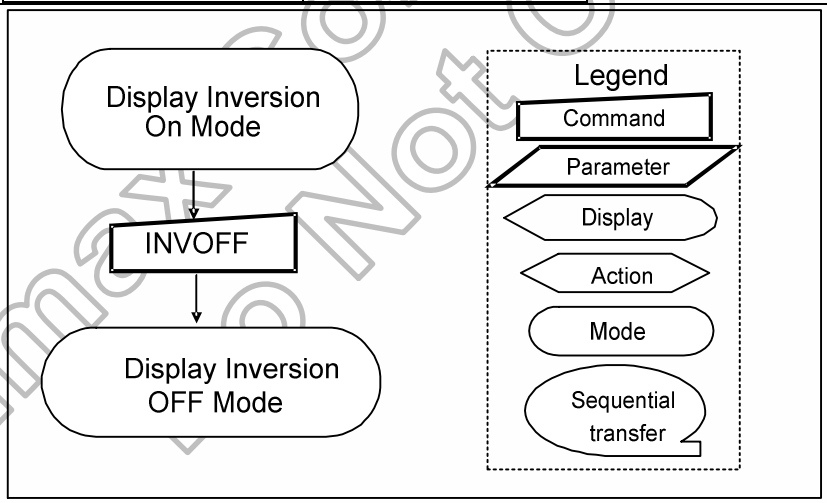
### 6.3.15 Display Inversion Off (20h)

| 20 H | INVOFF (Display Inversion Off) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command is used to recover from display inversion mode.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>(Example)<br>Memory → Display  | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in inversion off mode. | | | | | | | | | | | |

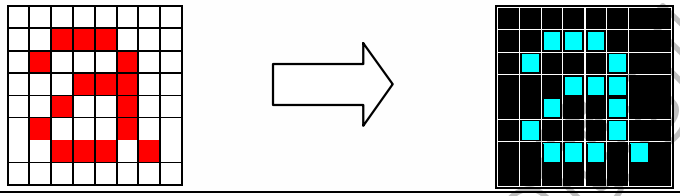
| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In or Booster Off | Yes |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display Inversion off |
| | S/W Reset | Display Inversion off |
| | H/W Reset | Display Inversion off |

Flow Chart



### 6.3.16 Display Inversion On (21h)

| 21 H | INVON (Display Inversion On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command is used to enter into display inversion mode.<br>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.<br>This command does not change any other status.<br>Memory (Example) Display<br>  | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in inversion on mode. | | | | | | | | | | | |

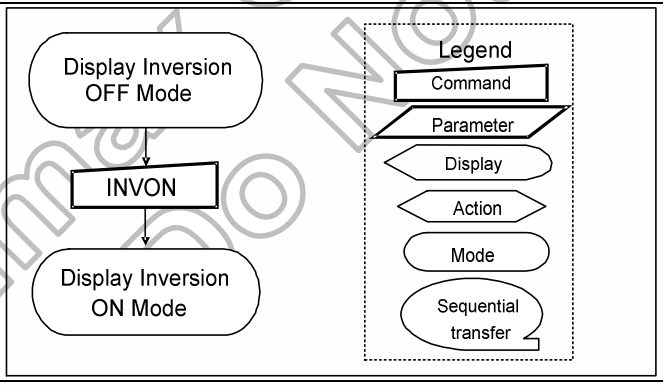
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| S/W Reset | Display Inversion off |
| H/W Reset | Display Inversion off |

Flow Chart



### 6.3.17 Gamma Set (26h)

| 26 H | GAMSET (Gamma Set) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 |
| Parameter | 1 | ↑ | 1 | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 | - |

**Description**

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

| GC[7..0] | Parameter | Curve Selected |
|---|---|---|
| 01h | GC0 | Gamma Curve 1 |
| 02h | GC1 | Gamma Curve 2 |
| 04h | GC2 | Gamma Curve 3 |
| 08h | GC3 | Gamma Curve 4 |

**Restriction**

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

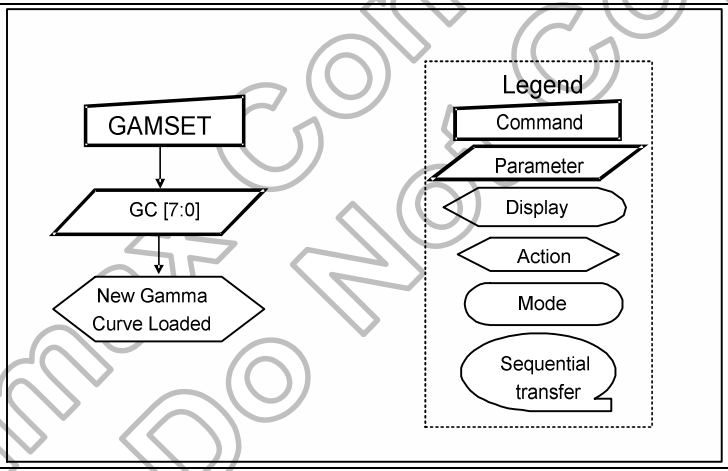
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 01h |
| S/W Reset | 01h |

**Flow Chart**



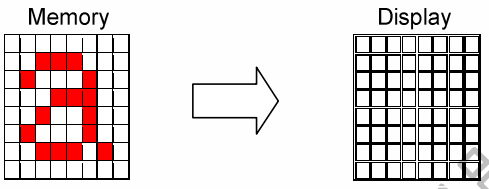
### 6.3.18 Display Off(28h)

| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 |
| Parameter | NO PARAMETER | | | | | | | | | | | |

**Description**

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

Example




**Restriction**

This command has no effect when module is already in display off mode.

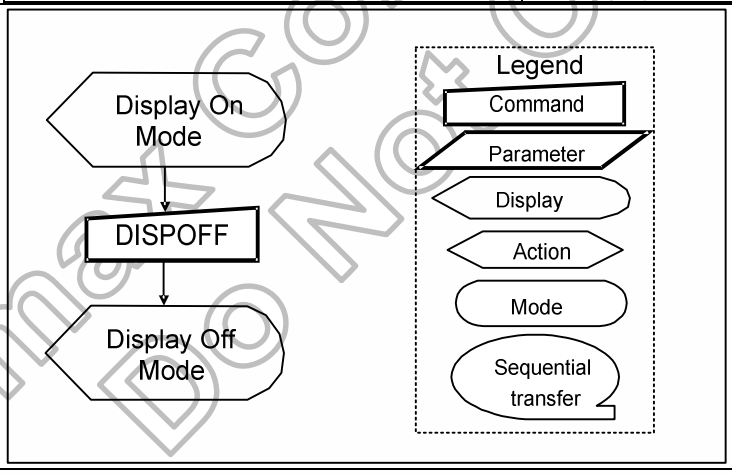
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

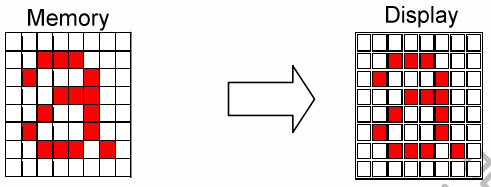
**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display off |
| S/W Reset | Display off |
| H/W Reset | Display off |

**Flow Chart**



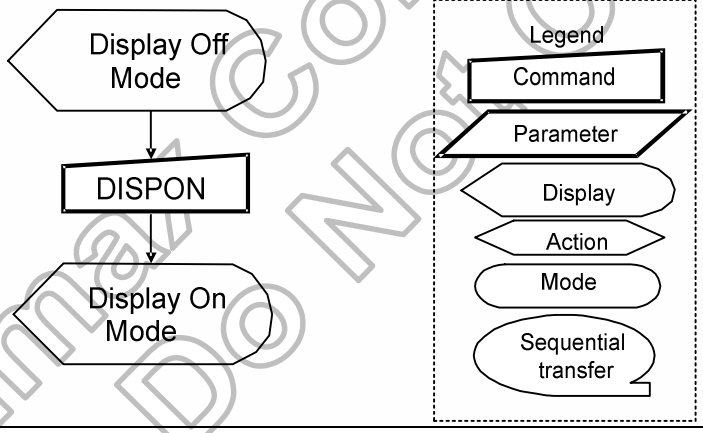
### 6.3.19 Display On (29h)

| 29 H | DISPON (Display On) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| Description | This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.<br>(Example)<br>  | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display on mode. | | | | | | | | | | | |

| Register Availability | Status | Availability |
|---|---|---|
| | Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| | Normal Mode On, Idle Mode On, Sleep Out | Yes |
| | Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| | Partial Mode On, Idle Mode On, Sleep Out | Yes |
| | Sleep In or Booster Off | Yes |

| Default | Status | Default Value |
|---|---|---|
| | Power On Sequence | Display off |
| | S/W Reset | Display off |
| | H/W Reset | Display off |

Flow Chart



### 6.3.20 Column Address Set (2Ah)

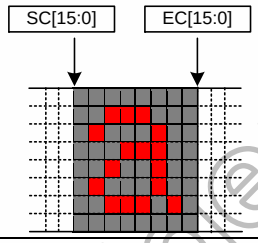
| 2A H | CASET (Column Address Set) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A |
| parameter 1st | 1 | ↑ | 1 | SC15 | SC14 | SC13 | SC12 | SC11 | SC10 | SC9 | SC8 | - |
| parameter 2nd | 1 | ↑ | 1 | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | - |
| parameter3rd | 1 | ↑ | 1 | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 | - |
| parameter4th | 1 | ↑ | 1 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | |

**Description**

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)

(Example)




**Restriction**

SC[15:0] always must be equal to or less than EC[15:0]
Note 1: When SC[15:0] or EC[15:0] is greater than 83h (when MADCTL's B5=0) or A1h (when MADCTL's B5=1), data of out of range will be ignored

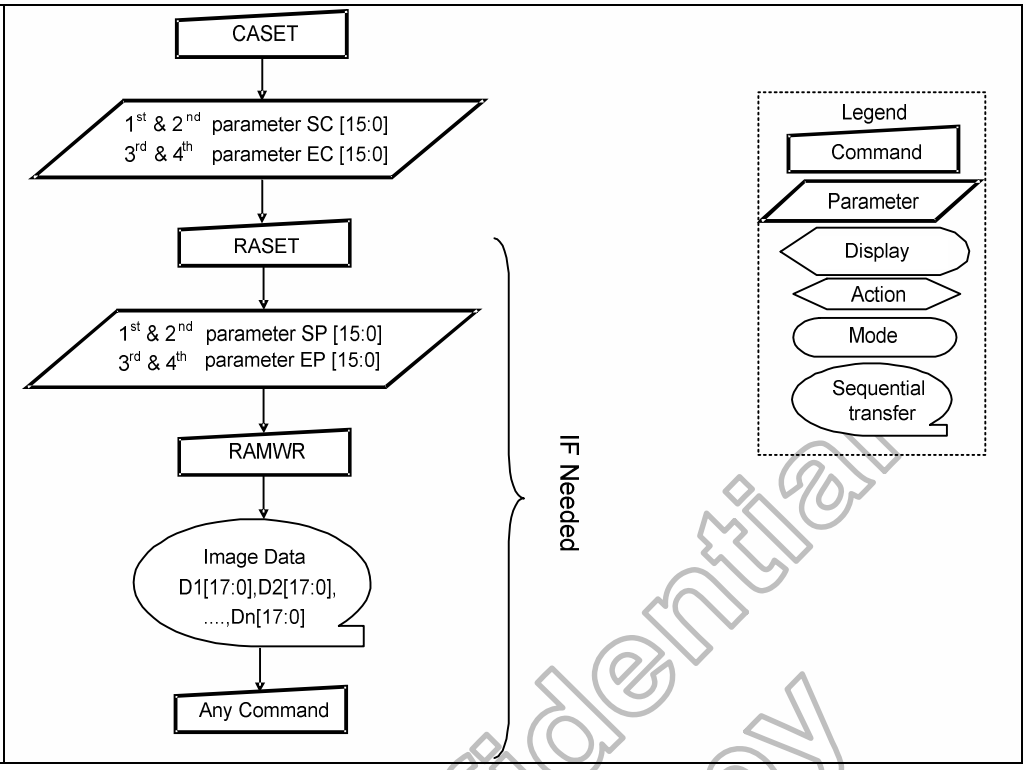
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SC[15:0]=0000 | EC[15:0]=0083 |
| S/W Reset | When MADCTL's B5=0: | When MADCTL's B5=0: |
| | SC[15:0]=0000 | EC[15:0]=0083 |
| | When MADCTL's B5=1: | When MADCTL's B5=1: |
| | SC[15:0]=0000 | EC[15:0]=00A1 |
| H/W Reset | SC[15:0]=0000 | EC[15:0]=0083 |

Flow Chart



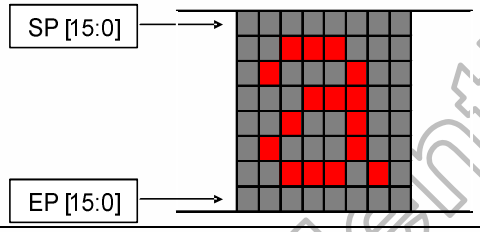
## 6.3.21 Page Address Set (2Bh)

| 2B H | PASET (Page Address Set) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B |
| parameter 1st | 1 | ↑ | 1 | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | 00.. |
| parameter 2nd | 1 | ↑ | 1 | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | Note 1 |
| parameter3rd | 1 | ↑ | 1 | EP15 | EP14 | EP13 | EP12 | EP11 | EP10 | EP9 | EP8 | 00.. Note 1 |
| parameter4th | 1 | ↑ | 1 | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | |

**Description**

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.

(Example)




**Restriction**

SP[15:0] always must be equal to or less than EP[15:0]
Note 1: When SP[15:0] or EP[15:0] is greater than A1h (When MADCTL's B5=0) or 83h (When MADCTL's B5=1), data of out of range will be ignored.

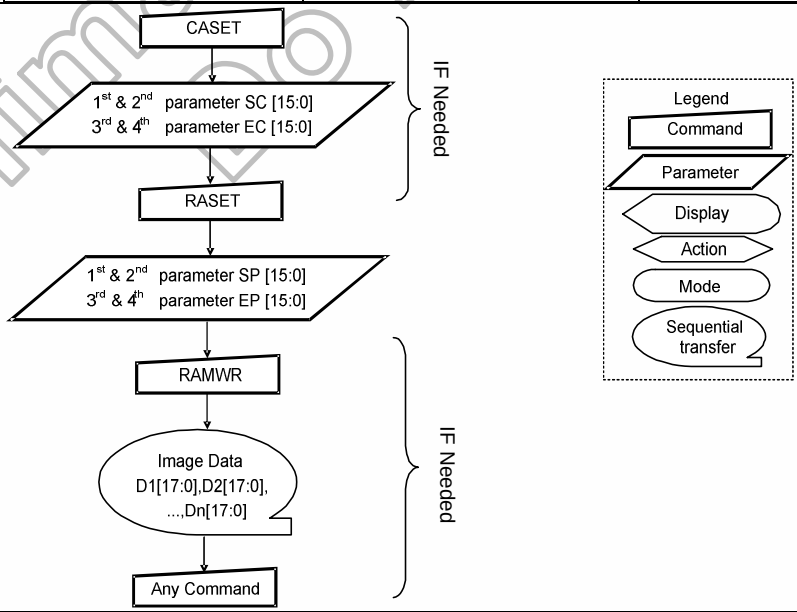
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| Power On Sequence | SP[15:0]=0000 | EP[15:0]=00A1 |
| S/W Reset | When MADCTL's B5=0: | When MADCTL's B5=0: |
| | SP[15:0]=0000 | EP[15:0]=00A1 |
| | When MADCTL's B5=1: | When MADCTL's B5=1: |
| | SP[15:0]=0000 | EP[15:0]=0083 |
| H/W Reset | SP[15:0]=0000 | EP[15:0]=00A1 |

**Flow Chart**



### 6.3.22 Memory Write (2Ch)

| 2C H | RAMWR (Memory Write) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C |
| 1st parameter | 1 | ↑ | 1 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00..FF |

**Description**

This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See follow table) Then DB[7:0] is stored in frame memory and the column register and the page register incremented as follow table.

| Condition | Column Counter | Page Counter |
|---|---|---|
| When RAMWR/RAMRD command is accepted | Return to "Start Column" | Return to "Start Page" |
| Complete Pixel Read/Write action | Increment by 1 | No change |
| The Column counter value is larger than "End column" | Return to "Start Column" | Increment by 1 |
| The Page counter value is larger than "End page" | Return to "Start Column" | Return to "Start Page" |

**Restriction**

In all color modes, there is no restriction on length of parameters.

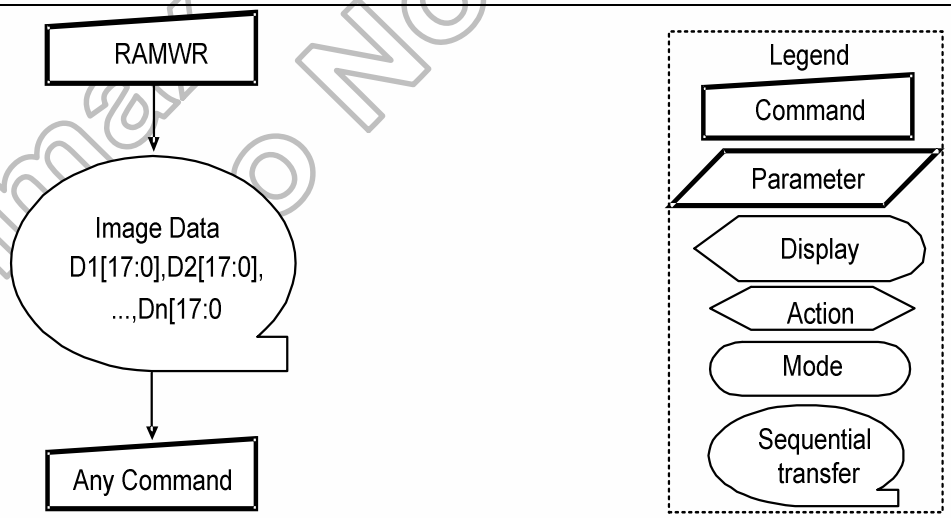
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |

**Flow Chart**



### 6.3.23 Colour Set (2Dh)

| 2D H | RGBSET (Color Set) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| 1st parameter | 0 | 1 | ↑ | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D |
| : | 1 | 1 | ↑ | X | X | R005 | R004 | R003 | R002 | R001 | R000 | 00..FF |
| 16th parameter | 1 | 1 | ↑ | X | X | Rnn5 | Rnn4 | Rnn3 | Rnn2 | Rnn1 | Rnn0 | 00..FF |
| 17th parameter | 1 | 1 | ↑ | X | X | R315 | R314 | R313 | R312 | R311 | R310 | 00..FF |
| 33rd parameter | 1 | 1 | ↑ | X | X | G005 | G004 | G003 | G002 | G001 | G000 | 00..FF |
| .. | 1 | 1 | ↑ | X | X | Gnn5 | Gnn4 | Gnn3 | Gnn2 | Gnn1 | Gnn0 | 00..FF |
| 96th parameter | 1 | 1 | ↑ | X | X | G635 | G634 | G633 | G632 | G631 | G630 | 00..FF |
| 97th parameter | 1 | 1 | ↑ | X | X | B005 | B004 | B003 | B002 | B001 | B000 | 00..FF |
| 128th parameter | 1 | 1 | ↑ | X | X | B315 | B314 | B313 | B312 | B311 | B310 | 00..FF |
| Description | This command is used to define the LUT for 12bit-to-18bit/16bit-to-18bit color depth conversions. (See also section 8.9) 128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 8.9 are referred. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to. | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | |

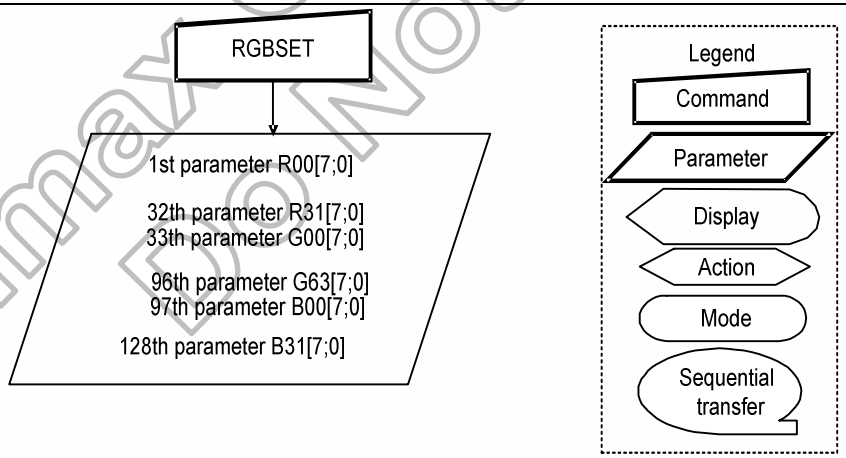
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Random values |
| S/W Reset | Contents of the look-up table protected |
| H/W Reset | Random values |

Flow Chart



## 6.3.24 Memory Read (2Eh)

| 2E H | RAMRD (Memory Read) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB 7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | - |

**Description**

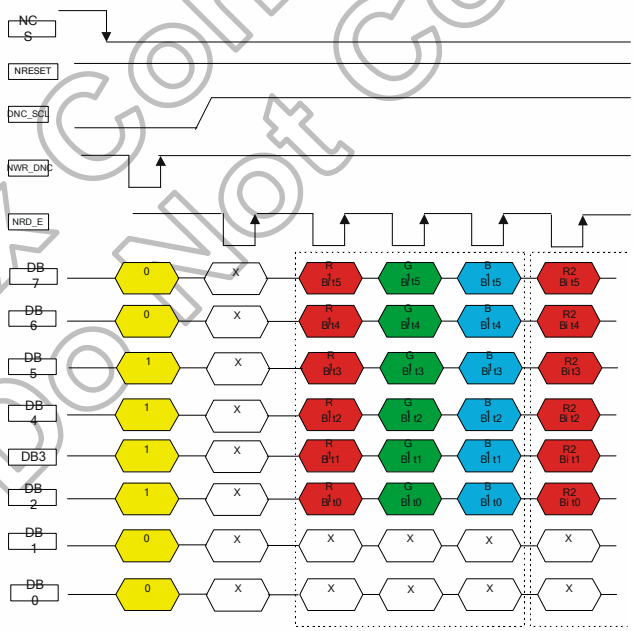
This command is used to transfer data from frame memory to MCU. See section 9.1 This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See follow table) Then DB[7:0] is read back from the frame memory and the column register and the page register incremented as follow table.

| Condition | Column Counter | Page Counter |
|---|---|---|
| When RAMWR/RAMRD command is accepted | Return to "Start Column" | Return to "Start Page" |
| Complete Pixel Read/Write action | Increment by 1 | No change |
| The Column counter value is larger than "End column" | Return to "Start Column" | Increment by 1 |
| The Page counter value is larger than "End page" | Return to "Start Column" | Return to "Start Page" |

Frame Read can be stopped by sending any other command.

**Restriction**

In all color modes, the Frame Read is always like figure below. There is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.

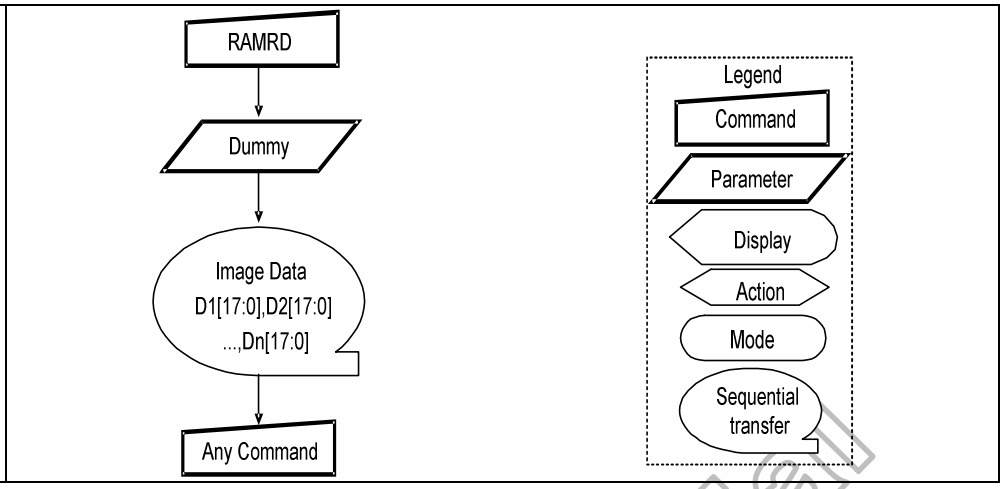



**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |

| | |
|---|---|
| Flow Chart |  |

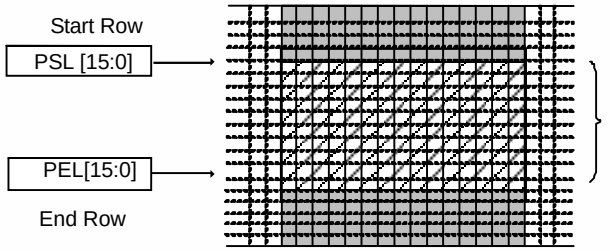
### 6.3.25 Partial Area (30h)

| 30 H | PLTAR (Partial Area) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 |
| 1st Parameter | 1 | ↑ | 1 | PSL15 | PSL14 | PSL13 | PSL12 | PSL11 | PSL10 | PSL9 | PSL8 | 00 …A1 |
| 2nd Parameter | 1 | ↑ | 1 | PSL7 | PSL6 | PSL5 | PSL4 | PSL3 | PSL2 | PSL1 | PSL0 | |
| 3rd Parameter | 1 | ↑ | 1 | PEL15 | PEL14 | PEL13 | PEL12 | PEL11 | PEL10 | PEL9 | PEL8 | 00 ...A1 |
| 4th Parameter | 1 | ↑ | 1 | PEL7 | PEL6 | PEL5 | PEL4 | PEL3 | PEL2 | PEL1 | PEL0 | |

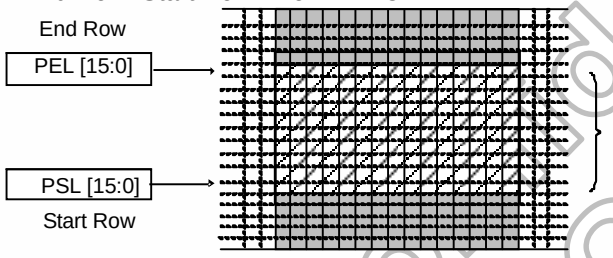
**Description**

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

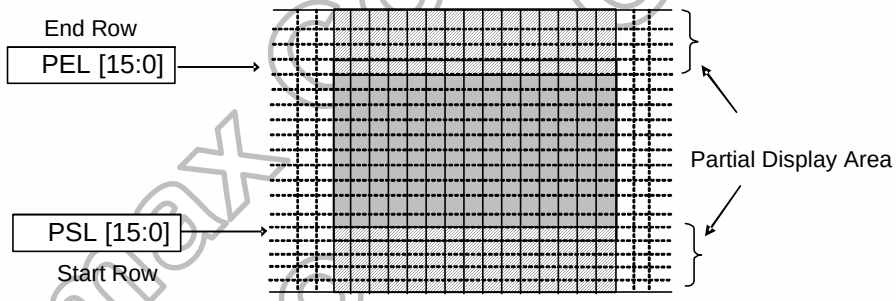
If End Row>Start Row when MADCTL B4=0:-




If End Row>Start Row when MADCTL B4=1:-




If End Row<Start Row when MADCTL B4=0:-




If End Row = Start Row then the Partial Area will be one row deep.

**Restriction**

SR[15...0] and ER[15...0] cannot be greater than A1h.

**Register Availability**

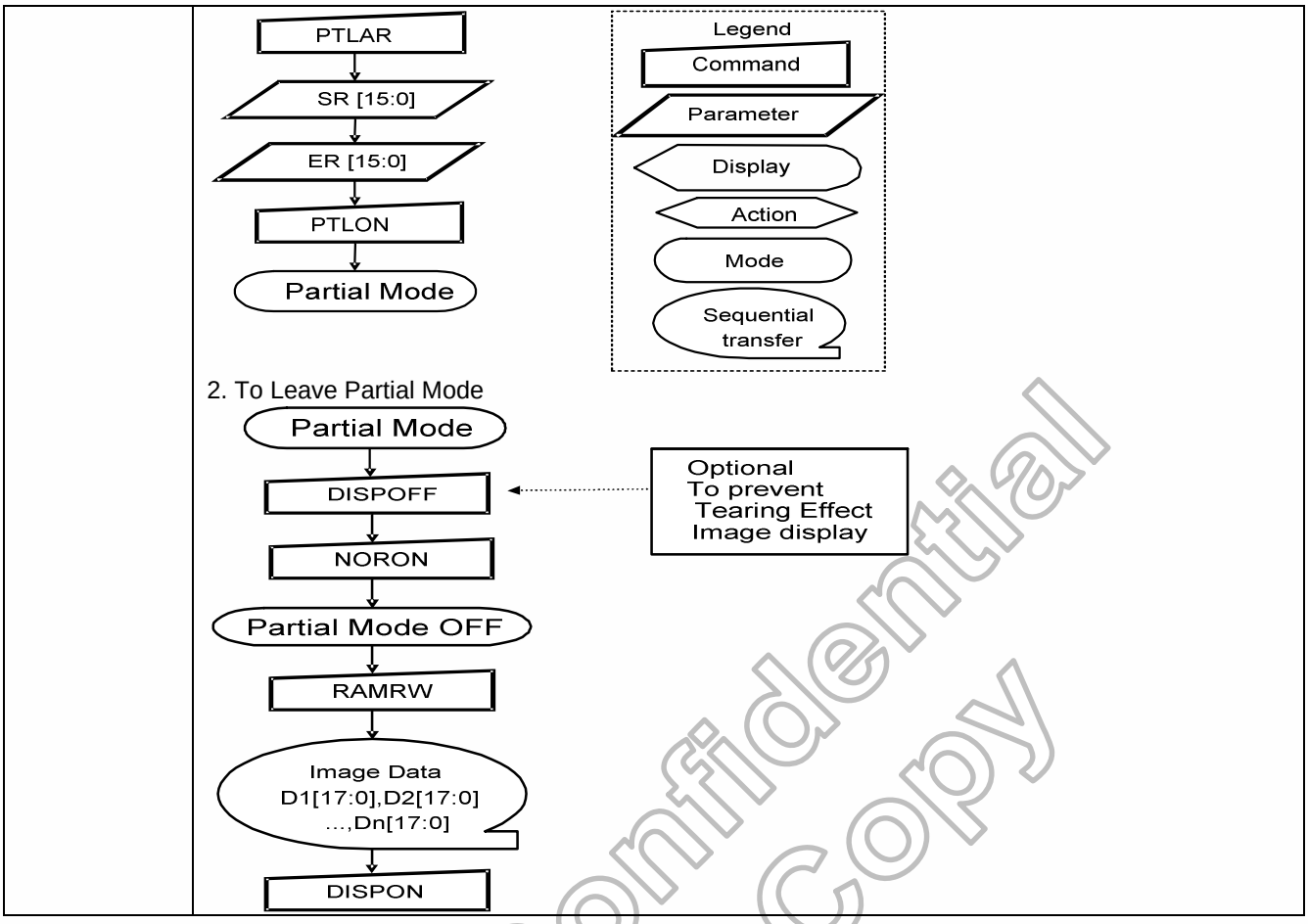
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

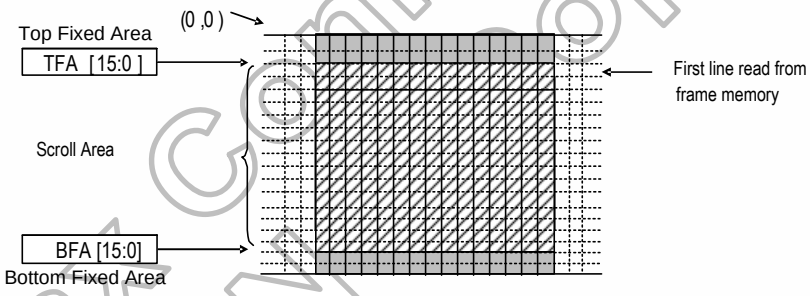
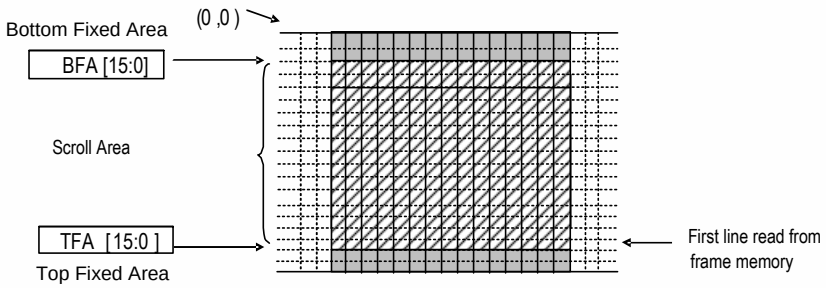
| Status | Default Value | |
|---|---|---|
| Power On Sequence | SR[15..0]=00 | ER[15..0]=A1 |
| S/W Reset | SR[15..0]=00 | ER[15..0]=A1 |

**Flow Chart**

1. To Enter Partial Mode:-



## 6.3.26 Vertical Scrolling Definition (33h)

| 33 H | VSCRDEF (Vertical Scrolling Definition) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 |
| 1st parameter | 1 | 1 | ↑ | TFA 15 | TFA 14 | TFA 13 | TFA 12 | TFA 11 | TFA 10 | TFA 9 | TFA 8 | 00..A2 |
| 2nd parameter | 1 | 1 | ↑ | TFA 7 | TFA 6 | TFA 5 | TFA 4 | TFA 3 | TFA 2 | TFA 1 | TFA 0 | |
| 3rd parameter | 1 | 1 | ↑ | VSA 15 | VSA 14 | VSA 13 | VSA 12 | VSA 11 | VSA 10 | VSA 9 | VSA 8 | 00..A2 |
| 4th parameter | 1 | 1 | ↑ | VSA 7 | VSA 6 | VSA 5 | VSA 4 | VSA 3 | VSA 2 | VSA 1 | VSA 0 | |
| 5th parameter | 1 | 1 | ↑ | BFA 15 | BFA 14 | BFA 13 | BFA 12 | BFA 11 | BFA 10 | BFA 9 | BFA 8 | 00..A2 |
| 6th parameter | 1 | 1 | ↑ | BFA 7 | BFA 6 | BFA 5 | BFA 4 | BFA 3 | BFA 2 | BFA 1 | BFA 0 | |
| Description | This command defines the Vertical Scrolling Area of the display.<br>When MADCTL B4=0<br>The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).<br>The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.<br>The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).<br>TFA, VSA and BFA refer to the Frame Memory Line Pointer.<br>  <br><br>When MADCTL B4=1<br>The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).<br>The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.<br>The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).<br>  <br><br>See also Section 8.2.2.2 for details of the Memory to Display mappings. | | | | | | | | | | | |
| Restriction | The condition is (TFA+VSA+BFA)=162, otherwise Scrolling mode is undefined.<br>In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write. | | | | | | | | | | | |

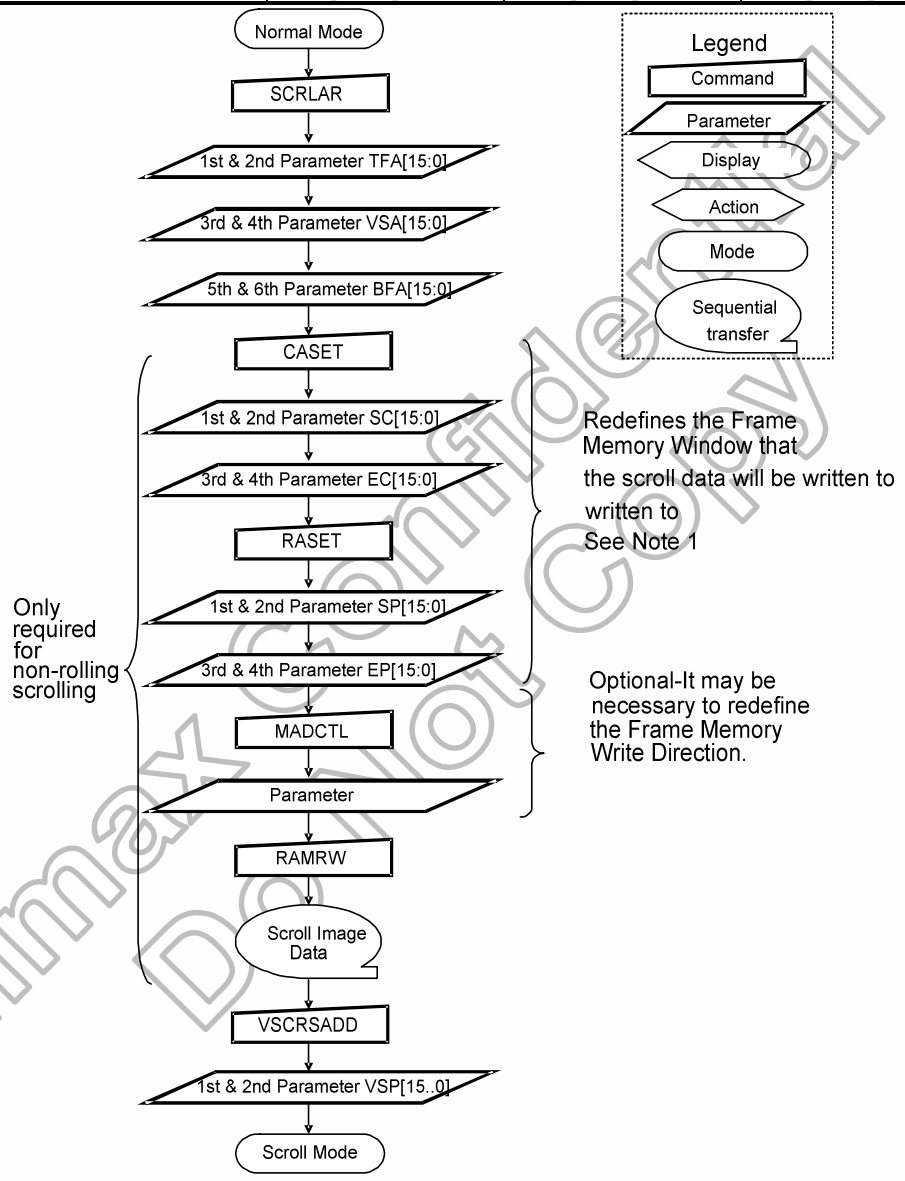
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

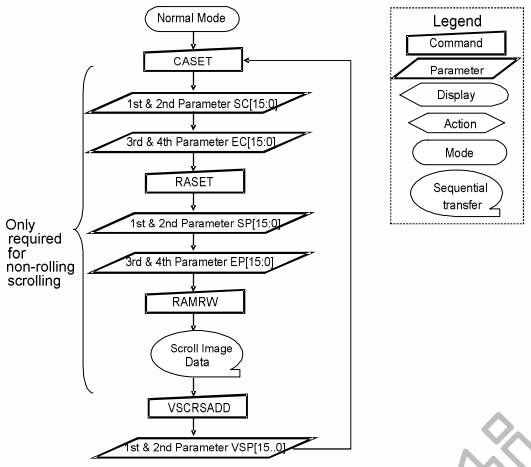
| Status | Default Value | | |
|---|---|---|---|
| Power On Sequence | TFA[15..0]=0000 | VSA[15..0]=00A2 | BFA[15..0]=0000 |
| S/W Reset | TFA[15..0]=0000 | VSA[15..0]=00A2 | BFA[15..0]=0000 |
| H/W Reset | TFA[15..0]=0000 | VSA[15..0]=00A2 | BFA[15..0]=0000 |

**Flow Charts**

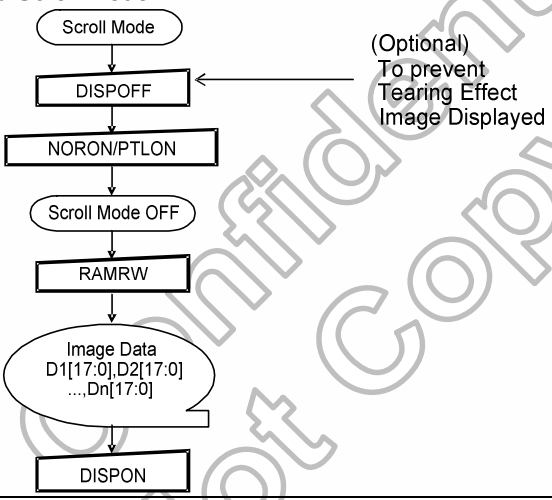



Note
The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:




3. To Leave Vertical Scroll Mode:



### 6.3.27 Tearing Effect Line Off (34h)

| **34 H** | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 |
| Description | This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. | | | | | | | | | | | |
| Restriction | This command has no effect when Tearing Effect output is already OFF. | | | | | | | | | | | |

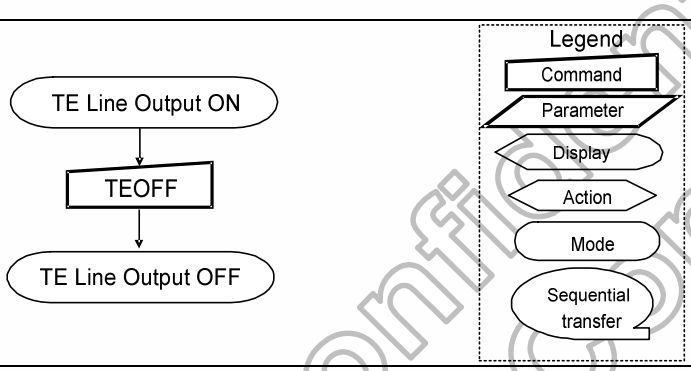
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Off |
| S/W Reset | Off |

Flow Chart



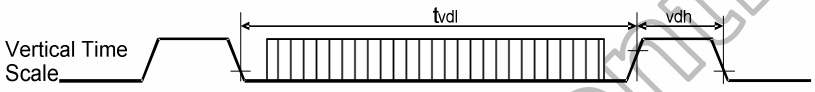
### 6.3.28 Tearing Effect Line On (35h)

| 35 H | TEON (Tearing Effect Line ON) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 |
| Parameter | 1 | ↑ | 1 | - | - | - | - | - | - | - | M | - |

**Description**

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:


When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:




Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

**Restriction**

This command has no effect when Tearing Effect output is already ON.

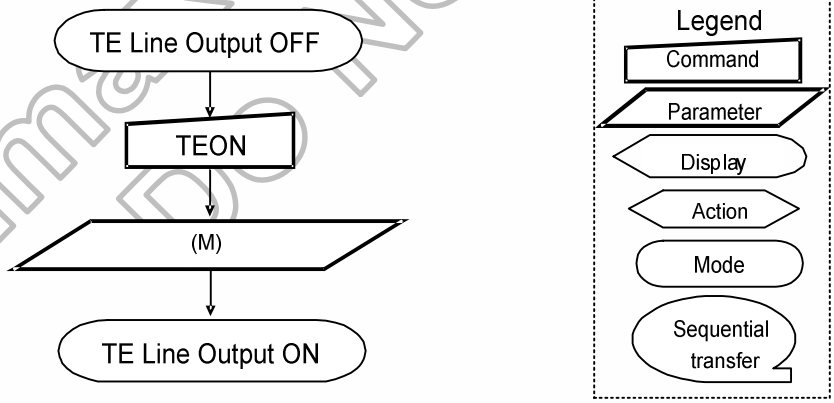
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Off |
| S/W Reset | Off |

**Flow Chart**



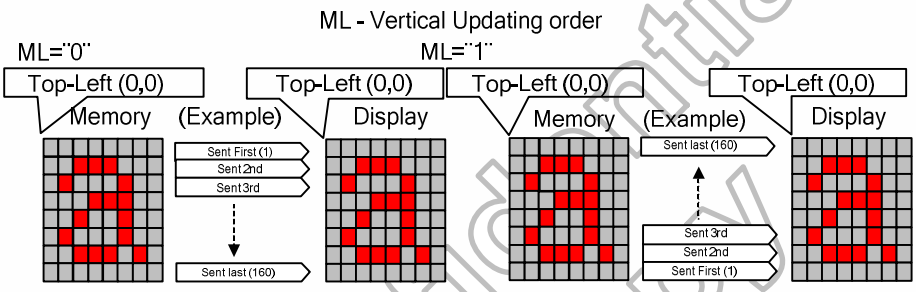
## 6.3.29 Memory Access Control (36h)

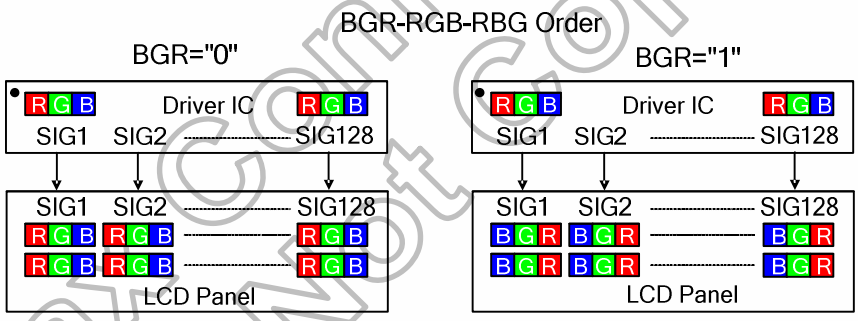
| 36 H | MADCTL (Memory Access Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 |
| 1st parameter | 1 | ↑ | 1 | MY | MX | MV | ML | BGR | SS | - | - | XX |

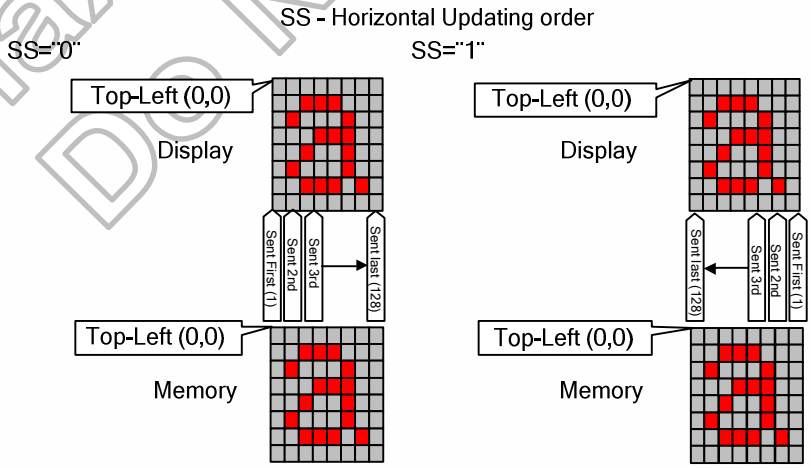
**Description**

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment

| BIT | NAME | DESCRIPTION |
|---|---|---|
| MY | PAGE ADDRESS ORDER | These 3 bits controls MCU to memory write/read direction. |
| MX | COLUMN ADDRESS ORDER | |
| MV | PAGE/COLUMN SELECTION | |
| ML | Vertical ORDER | LCD vertical refresh direction control |
| BGR | RGB-BGR ORDER | Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) |
| SS | Horizontal ORDER | LCD horizontal refresh direction control |





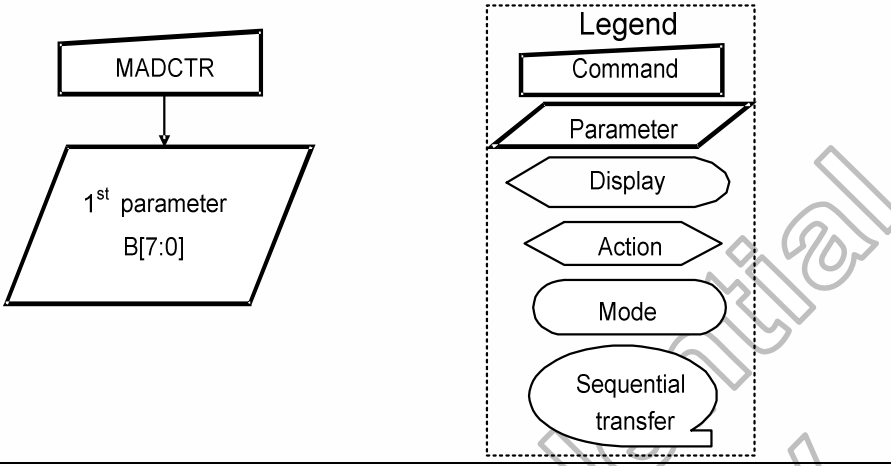



**Restriction**

DB1 and DB0 are set to '00' internally. DB2 is implemented if the LCD is updating pixel-by-pixel.
DB2 is set to '0' internally if the LCD is updating line-by-line.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |

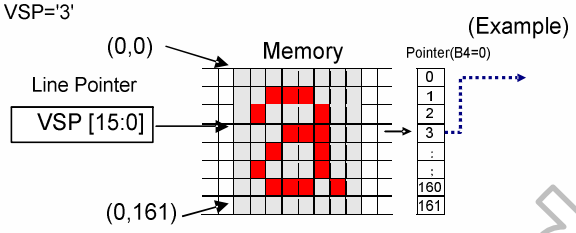
<table>
<tr><td></td><td>
<table>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>MY=0,MX=0,MV=0,ML=0,BGR=0,SS=0,B1=0,B0=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

## 6.3.30 Vertical Scrolling Start Address (37h)

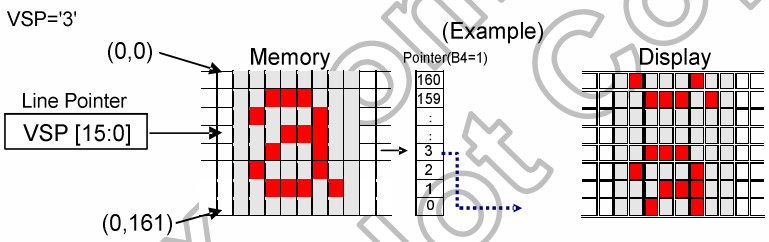
| 37 H | VSCRSADD (Vertical Scrolling Start Address) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | NRD DNC | NW R | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 10 | ↑ | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37 |
| 1st parameter | 11 | ↑ | VSP 15 | VSP 14 | VSP 13 | VSP 12 | VSP 11 | VSP 10 | VSP 9 | VSP 8 | 00 .. A1 |
| 2nd parameter | 11 | ↑ | VSP 7 | VSP 6 | VSP 5 | VSP 4 | VSP 3 | VSP 2 | VSP 1 | VSP 0 | |

**Description**

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'




When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'




. When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
. VSP refers to the Frame Memory line Pointer.

**Restriction**

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | No |
| Partial Mode On, Idle Mode On, Sleep Out | No |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 0000 |
| S/W Reset | 0000 |
| H/W Reset | 0000 |

**Flow Chart**

See Vertical Scrolling Definition (33h) description.

### 6.3.31 Idle Mode Off (38h)

| **38 H** | IDMOFF (Idle mode off) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 |
| Parameter | NO PARAMETER | | | | | | | | | | | |
| | This command is used to recover from Idle mode on. | | | | | | | | | | | |
| Description | In the idle off mode, LCD can display maximum 262,144 colors. See also section 8.6.2. | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in idle off mode. | | | | | | | | | | | |

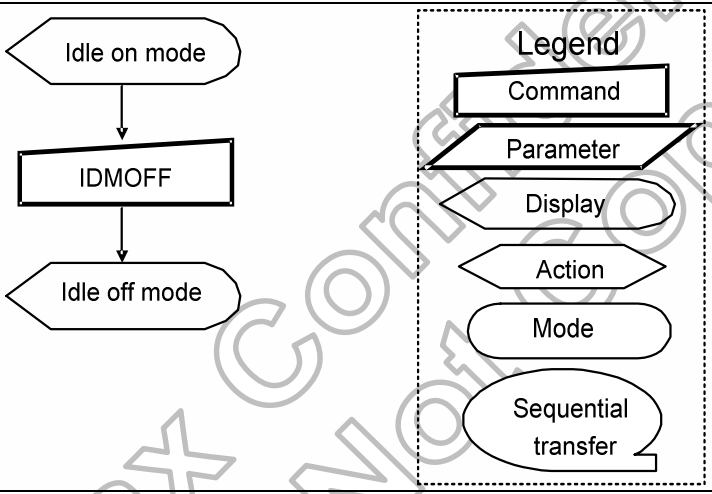
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Idle off mode |
| S/W Reset | Idle off mode |

Flow Chart



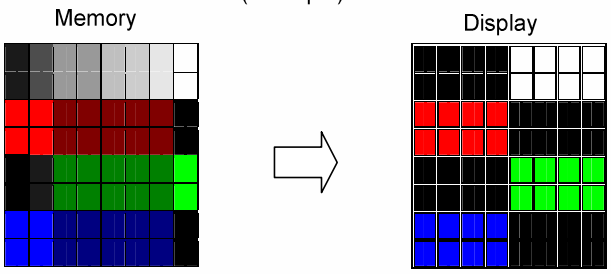
### 6.3.32 Idle Mode On (39h)

| 39 H | IDMON (Idle mode on) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 |
| Parameter | NO PARAMETER | | | | | | | | | | | |

**Description**

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Example)




Memory contents vs. Display Color

| | R4 R3 R2 R1 R0 | G5 G4 G3 G2 G1 G0 | B4 B3 B2 B1 B0 |
|---|---|---|---|
| Black | 0XXXX | 0XXXXX | 0XXXX |
| Blue | 0XXXX | 0XXXXX | 1XXXX |
| Red | 1XXXX | 0XXXXX | 0XXXX |
| Magenta | 1XXXX | 0XXXXX | 1XXXX |
| Green | 0XXXX | 1XXXXX | 0XXXX |
| Cyan | 0XXXX | 1XXXXX | 1XXXX |
| Yellow | 1XXXX | 1XXXXX | 0XXXX |
| White | 1XXXX | 1XXXXX | 1XXXX |

X=don't care
See also section 8.6.2.

**Restriction**

This command has no effect when module is already in idle on mode.

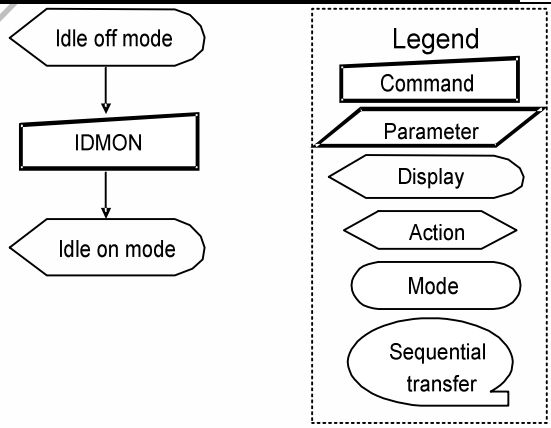
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Idle off mode |
| S/W Reset | Idle off mode |
| H/W Reset | Idle off mode |

**Flow Chart**



## 6.3.33 Interface Pixel Format (3Ah)

| 3A H | COLMOD (Interface Pixel Format) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A |
| 1st parameter | 1 | 1 | ↑ | XX | XX | XX | XX | XX | CSEL2 | CSEL1 | CSEL0 | 011,101 |

**Description**

This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:-

| Interface Format (system interface) | CSEL2 | CSEL1 | CSEL0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| 12 Bit/Pixel | 0 | 1 | 1 |
| Not Defined | 1 | 0 | 0 |
| 16 Bit/Pixel | 1 | 0 | 1 |
| 18 Bit/Pixel | 1 | 1 | 0 |
| Not Defined | 1 | 1 | 1 |

Note: In 8, 12, 16 &18 Bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

**Restriction**

There is no visible effect until the Frame Memory is written to.

**Register Availability**

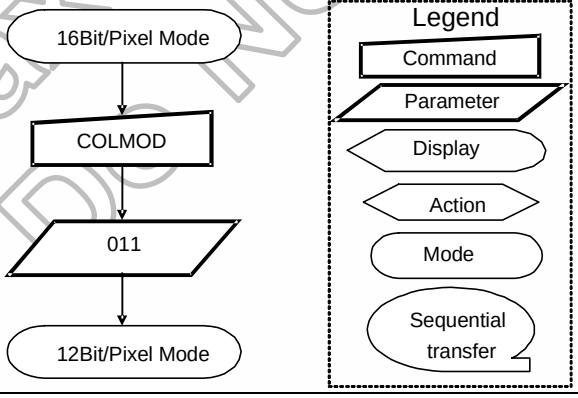
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 18 Bit/Pixel |
| S/W Reset | No Change |
| H/W Reset | 18 Bit/Pixel |

**Flow Chart**

Example:



### 6.3.34 Read IDB1 (DAh)

| DA H | RDIDB1 (Read IDB1) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | Module's manufacturer[7:0] | | | | | | | | xx |
| Description | This read byte identifies the LCD module's manufacturer. It is specified by Nokia and for xx is defined as xxHEX. | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | |

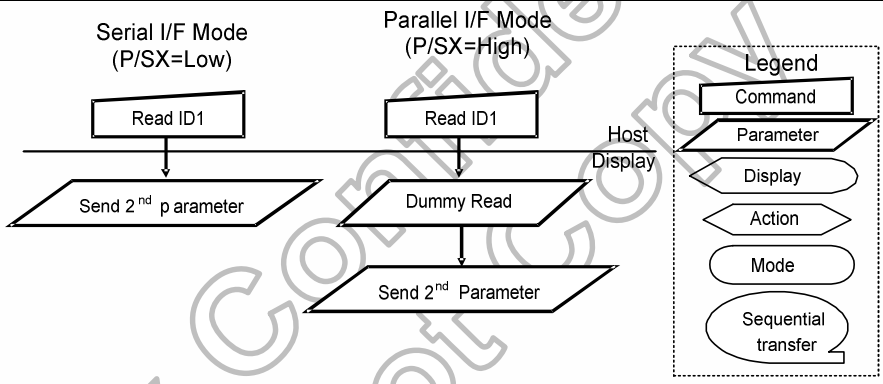
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | xxHEX |
| S/W Reset | xxHEX |

Flow Chart



### 6.3.35 Read IDB2 (DBh)

| DB H | RDIDB2 (Read IDB2) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | - | V6 | V5 | V4 | V3 | V2 | V1 | V0 | - |

**Description**

This read byte is used to track the LCD module/driver version. It is defined by display supplier (with Nokia's agreement) and changes each time a revision is made to the display, material or construction specifications. See Table:

| ID Byte Value V[7:0] | Version | Changes |
|---|---|---|
| 80h | | |
| 81h | | |
| 82h | | |
| 83h | | |
| 84h | | |
| 85h | | |

**Restrictions**

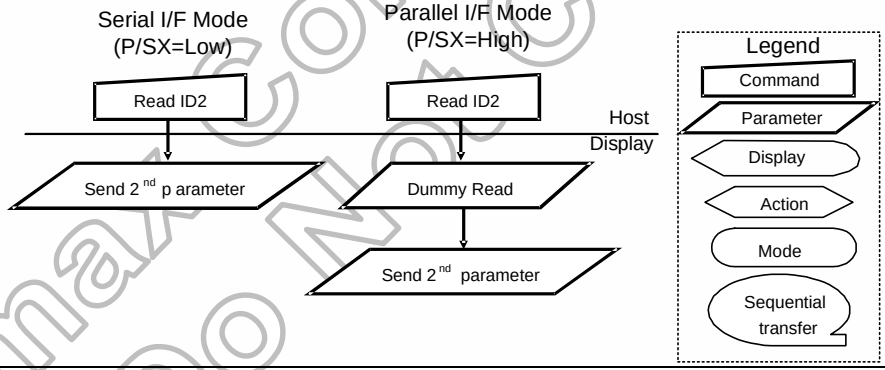
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | See Description |
| S/W Reset | See Description |

**Flow Chart**



### 6.3.36 Read IDB3 (DCh)

| DC H | RDIDB3 (Read IDB3) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC |
| 1st parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - |
| 2nd parameter | 1 | 1 | ↑ | LCD module/driver ID [7:0] | | | | | | | | - |
| Description | This read byte identifies the LCD module/driver. It is specified by Nokia and for this LCD project module is defined as xxHEX. | | | | | | | | | | | |
| Restrictions | | | | | | | | | | | | |

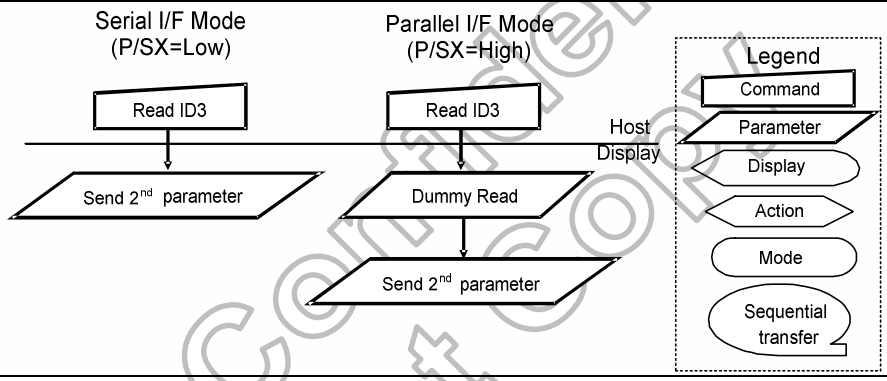
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | TBDHEX |
| S/W Reset | TBDHEX |

Flow Chart



## 6.4 Himax Command

### 6.4.1 SETOSC: Set Internal Oscillator (B0h)

| B0 H | SETOSC( Set Internal Oscillator) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0 |
| 1st parameter | 1 | ↑ | 1 | -- | CADJ[3:0] | | | | UADJ[2:0] | | | - | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | RADJ[1:0] | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | OSC_EN_CON(0) | -- | -- | OSC_EN(1) | -- | -- |

**Description**

This command is used to set internal oscillator related setting.
**OSC_EN**: Enable internal oscillator, High active
**CADJ[3:0]**, **RADJ[3:0]:** for Internal test.
**UADJ[2:0]:** Internal oscillator frequency, default is 1.5MHz.

| UADJ2 | UADJ1 | UADJ0 | frequency |
|---|---|---|---|
| 0 | 0 | 0 | 128% |
| 0 | 0 | 1 | 119% |
| 0 | 1 | 0 | 110% |
| 0 | 1 | 1 | 100% |
| 1 | 0 | 0 | 91% |
| 1 | 0 | 1 | 81% |
| 1 | 1 | 0 | 71% |
| 1 | 1 | 1 | 61% |

**OSC_EN_CON**: OSC_EN status control bit,1: OSC_EN in fix state,0: OSC_EN in changed state

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | OSC_TEST=0; OSC_EN=0, CADJ[3:0]=OTP value, RADJ=OTP value, UADJ[2:0]=3'b011. |
| S/W Reset | OSC_EN=0h, if OPT is programmed, CADJ[3:0] =OTP value, RADJ=OTP value, else no change |
| H/W Reset | OSC_TEST=0; OSC_EN=0, CADJ[3:0] =OTP value, RADJ=OTP value, UADJ[2:0]=3'b011 |

**Flow Chart**

### 6.4.2 SETPOWER: Set Power (B1h)

| B1 H | SETPOWER( Set power related setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B1 |
| 1st parameter | 1 | ↑ | 1 | -- | GASENB(0) | -- | -- | PON(0) | DK(1) | -- | -- | STB(0) | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | AP[2:0](000) | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | VC1[2:0](110) | | | -- |
| 4th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | VRH[3:0](0100) | | | | -- |
| 5th parameter | 1 | ↑ | 1 | -- | BT[3:0](0011) | | | | -- | -- | -- | -- | -- |
| 6th parameter | 1 | ↑ | 1 | -- | -- | -- | FS11 | FS10 | -- | -- | FS01 | FS00 | -- |
| 7th parameter | 1 | ↑ | 1 | -- | N_DC[7:0] | | | | | | | | -- |
| 8th parameter | 1 | ↑ | 1 | -- | E_DC[7:0] | | | | | | | | -- |
| 9th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | -- | DCCLK_SYNC(1) | -- |

Description

**GASENB:** This stands for abnormal power-off supervise function when the power is off. It's for monitoring power status by NISD pad when GASENB is set to 0.

**PON:** Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation.
For detail, see the Power Supply Setting Sequence.

| PON | Operation of step-up circuit 2 |
|---|---|
| 0 | OFF |
| 1 | ON |

**DK:** Specify on/off control of step-up circuit 1 for VLCD voltage generation. For detail, see the Power Supply Setting Sequence.

| DK | Operation of step-up circuit 1 |
|---|---|
| 0 | ON |
| 1 | OFF |

**STB:** When STB = "1", the HX8353-C into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0") ,
b. Start the oscillation

In the standby mode, the GRAM data and register content may be lost. For preventing this, they have to reset again after the standby mode cancel.

**AP(2-0):**
Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. AP(2-0) can be set as "000" when display is off, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

| AP2 | AP1 | AP0 | Constant Current of Operational Amplifier |
|---|---|---|---|
| 0 | 0 | 0 | Power Circuit Off |
| 0 | 0 | 1 | Ignore |
| 0 | 1 | 0 | Ignore |

| | | | |
|---|---|---|---|
| 0 | 1 | 1 | Ignore |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1.25 |
| 1 | 1 | 0 | 1.5 |
| 1 | 1 | 1 | Ignore |

**VC1(2-0):**
Specify the ratio for VLCD voltage adjusting.

| VC12 | VC11 | VC10 | VLCD |
|---|---|---|---|
| 0 | 0 | 0 | 5.47 |
| 0 | 0 | 1 | 5.29 |
| 0 | 1 | 0 | 5.12 |
| 0 | 1 | 1 | 4.95 |
| 1 | 0 | 0 | 4.76 |
| 1 | 0 | 1 | 4.59 |
| 1 | 1 | 0 | 4.46 |
| 1 | 1 | 1 | 4.23 |

**VRH(3-0):**
Set the magnification of amplification for VREG1 voltage for gamma voltage setting. It allows magnify the amplification of VREF from 2.8 to 4.8 times.

| VRH3 | VRH2 | VRH1 | VRH0 | VREG1 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VREFx 1.87 |
| 0 | 0 | 0 | 1 | VREF x 2.00 |
| 0 | 0 | 1 | 0 | VREF x 2.13 |
| 0 | 0 | 1 | 1 | VREF x 2.20 |
| 0 | 1 | 0 | 0 | VREF x 2.27 |
| 0 | 1 | 0 | 1 | VREF x 2.33 |
| 0 | 1 | 1 | 0 | VREF x 2.4 |
| 0 | 1 | 1 | 1 | VREF x 2.47 |
| 1 | 0 | 0 | 0 | VREF x 2.53 |
| 1 | 0 | 0 | 1 | VREF x2.6 |
| 1 | 0 | 1 | 0 | VREF x 2.67 |
| 1 | 0 | 1 | 1 | VREF x 2.8 |
| 1 | 1 | 0 | 0 | VREF x 2.93 |
| 1 | 1 | 0 | 1 | VREF x 3.07 |
| 1 | 1 | 1 | 0 | VREF x 3.2 |
| 1 | 1 | 1 | 1 | Inhibited |

**Note:** VREF is the internal reference voltage equals to 1.8V.

**BT(3-0):**
Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.



| BT3 | BT2 | BT1 | BT0 | VCL | VGH | VGL | | Capacitor Connection Pins |
|---|---|---|---|---|---|---|---|---|
| | | | | | | VCOMG=1 | VCOMG=0 | |
| 0 | 0 | 0 | 0 | -1x VDD | VLCD x 3 [x 6] | -(VLCDx2)+VCL [x -5] | -(VLCDX2) [x -4] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 0 | 0 | 1 | -1x VDD | VLCD x 3 [x 6] | -(VLCDX2) [x -4] | -(VLCDX2) [x -4] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 0 | 1 | 0 | -1x VDD | VLCD x 3 [x 6] | -(VLCDx2)+VDD [x -3] | -(VLCDx2)+VDD [x -3] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | -1x VDD | VLCD x 2+VDD [x 5] | -(VLCDX2)+VCL [x -5] | -(VLCDX2) [x -4] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 1 | 0 | 0 | -1x VDD | VLCD x 2+VDD [x 5] | -(VLCDX2) [x -4] | -(VLCDX2) [x -4] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 1 | 0 | 1 | -1x VDD | VLCD x 2+VDD [x 5] | -(VLCDx2)+VDD [x -3] | -(VLCDx2)+VDD [x -3] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 1 | 1 | 0 | -1x VDD | VLCD X 2 [x 4] | -(VLCDX2) [x -4] | -(VLCDX2) [x -4] | VCL, VGH, VGL C11 A/B, C21 A/B, C22A/B |
| 0 | 1 | 1 | 1 | -1x VDD | Inhibited | | | |
| 1 | 0 | 0 | 0 | -1x VDD | VLCD X 2 [x 4] | -(VLCDX1)+VCL [x-3] | -(VLCDX1) [x-2] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 0 | 0 | 1 | -1x VDD | VLCD X 2 [x 4] | -(VLCDX1) [x-2] | -(VLCDX1) [x-2] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 0 | 1 | 0 | -1x VDD | VLCD X 2 [x 4] | -(VLCDX1)+VDD [x-1] | -(VLCDX1)+VDD [x-1] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 0 | 1 | 1 | -1x VDD | VLCD X 1 +VDD [x3] | -(VLCDX1)+VCL [x-3] | -(VLCDX1) [x-2] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 1 | 0 | 0 | -1x VDD | VLCD X1 + VDD [x3] | -(VLCDX1) [x-2] | -(VLCDX1) [x-2] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 1 | 0 | 1 | -1x VDD | VLCDX1+ VDD [x3] | -(VLCDX1)+VDD [x-1] | -(VLCDX1)+VDD [x-1] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 1 | 1 | 0 | -1x VDD | VLCDX1 [x2] | -(VLCDX1) [x-2] | -(VLCDX1) [x-2] | VCL, VGH, VGL C11 A/B, C21 A/B, |
| 1 | 1 | 1 | 1 | Inhibited | | | | |

**Note:** 1. The conditions of VLCD ≦ 6V, VCL ≦ -3.3V, VGH-VGL ≦ 32V must be satisfied.
2. If VCOMG=0, VCL output is floating.
3. C22 option : VGH and VGL can share the same pump capacitor when operate on special pumping condition →BT[3:0]=1XXX (On this condition, C22 can be removed).

**FS0(1-0):**

Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for VLCD voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

| FS01 | FS0 | Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1 |
|---|---|---|
| 0 | 0 | DCDCf / 1 |
| 0 | 1 | DCDCf / 2 |
| 1 | 0 | DCDCf / 4 |
| 1 | 1 | DCDCf / 8 |

**FS1(1-0):**

Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

| FS11 | FS10 | Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3 |
|---|---|---|
| 0 | 0 | DCDCf / 1 |
| 0 | 1 | DCDCf / 2 |
| 1 | 0 | DCDCf / 4 |
| 1 | 1 | DCDCf / 8 |

**Note:** Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

**N_DC:** Normal mode
**E_DC:** Idle mode
**DCCLK_SYNC:** Internal use, not open.

<table>
<tr><td>Restrictions</td><td>If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>GASENB=1’b0, PON=1’b0, XDK=1’b0, VLCD_TRI=1’b0, STB=1’b1, AP[2:0]=3’b000, VC1[2:0]=3’b110, VC3[2:0]=3’b110, VRH[3:0]=4’b0010, BT[3:0]=4’b0011, FS1[1:0]=2’b01, FS0[1:0]=2’b00, N_DC[7:0]=8’b0110_1110, PE_DC[7:0]=8’b0110_1110, E_DC[7:0]=8’b0110_1110, PI_PRE_REFRESH[1:0]=2’b00, BLANK_DIV[3:0]=4’b0000, DCCLK_SYNC=1’b1</td></tr>
<tr><td>S/W Reset</td><td>GASENB=1’b0, PON=1’b0, XDK=1’b0, VLCD_TRI=1’b0, STB=1’b1, AP[2:0]=3’b000, VC1[2:0]=3’b110, VC3[2:0]=3’b110, VRH[3:0]=4’b0010, BT[3:0]=4’b0011, FS1[1:0]=2’b01, FS0[1:0]=2’b00, N_DC[7:0]=8’b0110_1110, PE_DC[7:0]=8’b0110_1110, E_DC[7:0]=8’b0110_1110, PI_PRE_REFRESH[1:0]=2’b00, BLANK_DIV[3:0]=4’b0000, DCCLK_SYNC=1’b1</td></tr>
<tr><td>H/W Reset</td><td>GASENB=1’b0, PON=1’b0, XDK=1’b0, VLCD_TRI=1’b0, STB=1’b1, AP[2:0]=3’b000, VC1[2:0]=3’b110, VC3[2:0]=3’b110, VRH[3:0]=4’b0010, BT[3:0]=4’b0011, FS1[1:0]=2’b01, FS0[1:0]=2’b00, N_DC[7:0]=8’b0110_1110, PE_DC[7:0]=8’b0110_1110, E_DC[7:0]=8’b0110_1110, PI_PRE_REFRESH[1:0]=2’b00, BLANK_DIV[3:0]=4’b0000, DCCLK_SYNC=1’b1</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

### 6.4.3 SETDISP: Set Display Related Register (B2h)

| B2 H | SETDISP( Set display related register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2 |
| 1st parameter | 1 | ↑ | 1 | -- | PT[1:0] | | GON | DTE | D[1:0] | | -- | -- | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | N_BP[3:0] | | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | N_FP[3:0] | | | | -- |
| 4th parameter | 1 | ↑ | 1 | SAP[7:0] | | | | | | | | | -- |
| 5th parameter | 1 | ↑ | 1 | EQS[7:0] | | | | | | | | | -- |
| 6th parameter | 1 | ↑ | 1 | EQP[7:0] | | | | | | | | | -- |
| 7th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | GEN_OFF[3:0] | | | | -- |
| 8th parameter | 1 | ↑ | 1 | -- | -- | -- | PTG[1:0] | | ISC[3:0] | | | | -- |
| 9th parameter | 1 | ↑ | 1 | SAP_I[7:0] | | | | | | | | | -- |
| 10th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | -- | OPTION_DISP(0) | -- |

Description

This command is used to set display related register

**DB1–0:** When DB1 = 1, display is on; when DB1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting DB1 = 1. When DB1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8353-C can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE. When DB1–0 = 01, the internal display of the HX8353-C is performed although the actual display is off. When DB1-0 = 00, the internal display operation halts and the display is off.

| DB 1 | DB 0 | Source Output | HX8353-C Internal Display Operations | Gate-Driver Control Signals (CPV, FLM, M) |
|---|---|---|---|---|
| 0 | 0 | VSSD | Halt | Halt |
| 0 | 1 | VSSD | Operate | Operate |
| 1 | 0 | Non-lit display | Operate | Operate |
| 1 | 1 | Display | Operate | Operate |

**GON, DTE:**

| GON | DTE | Gate Output |
|---|---|---|
| 0 | X | VGH |
| 1 | 0 | VGL |
| 1 | 1 | VGH/VGL |

**PT[1:0] :** Non-display area source output control

| Source Output Level | | | | | |
|---|---|---|---|---|---|
| REV | GRAM Data | Display area | Non-display Area | | |
| | | | PT1-0=(0,*) | PT1-0=(1,0) | PT1-0=(1,1) |

| | | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 18'h00000<br>.<br>.<br>18'h3FFFF | V63<br>.<br>.<br>V0 | V0<br>.<br>.<br>V63 | V63 | V0 | VSSD | VSSD | Hi-z | Hi-z |
| 1 | 18'h00000<br>.<br>.<br>18'h3FFFF | V0<br>.<br>.<br>V63 | V63<br>.<br>.<br>V0 | V63 | V0 | VSSD | VSSD | Hi-z | Hi-z |

**FP[3:0]:** Specify the amount of scan line for front porch (FP).
**BP[3:0]:** Specify the amount of scan line for back porch(BP).
**N_FP[3:0], N_BP[3:0]:** Normal mode

| FP3<br>BP3 | FP2<br>BP2 | FP1<br>BP1 | FP0<br>BP0 | Number of FP Line | Number of BP Line |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Ignore | |
| 0 | 0 | 0 | 1 | Ignore | |
| 0 | 0 | 1 | 0 | 2 lines | |
| 0 | 0 | 1 | 1 | 3 lines | |
| 0 | 1 | 0 | 0 | 4 lines | |
| 0 | 1 | 0 | 1 | 5 lines | |
| 0 | 1 | 1 | 0 | 6 lines | |
| 0 | 1 | 1 | 1 | 7 lines | |
| 1 | 0 | 0 | 0 | 8 lines | |
| 1 | 0 | 0 | 1 | 9 lines | |
| 1 | 0 | 1 | 0 | 10 lines | |
| 1 | 0 | 1 | 1 | 11 lines | |
| 1 | 1 | 0 | 0 | 12 lines | |
| 1 | 1 | 0 | 1 | 13 lines | |
| 1 | 1 | 1 | 0 | 14 lines | |
| 1 | 1 | 1 | 1 | Ignore | |

| Operation Mode | BP | FP |
|---|---|---|
| System Interface | ≥2 lines | ≥2 lines |

**EQS[7:0]:** Internal use, not open.
**EQP[7:0]:** Internal use, not open.
**GEN_OFF:** Internal use, not open.
**PTG[1:0]:** Specify the scan mode of gate driver in non-display area.

| PTG1 | PTG0 | Gate Outputs in Non-display Area |
|---|---|---|
| 0 | 0 | Normal Drive |
| 0 | 1 | Fixed VGL |
| 1 | 0 | Interval scan |
| 1 | 1 | Ignore |



**ISC[3:0]:** Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

| ISC3 | ISC2 | ISC1 | ISC0 | Scan Cycle | $f_{FLM}$ = 60Hz |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 frame | - |
| 0 | 0 | 0 | 1 | 3 frames | 50 ms |
| 0 | 0 | 1 | 0 | 5 frames | 84 ms |

| | | | | | |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 7 frames | 117 ms |
| 0 | 1 | 0 | 0 | 9 frames | 150 ms |
| 0 | 1 | 0 | 1 | 11 frames | 184 ms |
| 0 | 1 | 1 | 0 | 13 frames | 217 ms |
| 0 | 1 | 1 | 1 | 15 frames | 251 ms |
| 1 | 0 | 0 | 0 | 17 frames | 284 ms |
| 1 | 0 | 0 | 1 | 19 frames | 317 ms |
| 1 | 0 | 1 | 0 | 21 frames | 351 ms |
| 1 | 0 | 1 | 1 | 23 frames | 384 ms |
| 1 | 1 | 0 | 0 | 25 frames | 418 ms |
| 1 | 1 | 0 | 1 | 27 frames | 451 ms |
| 1 | 1 | 1 | 0 | 29 frames | 484 ms |
| 1 | 1 | 1 | 1 | 31 frames | 518 ms |

**SAP[7-0]:** Normal mode, Internal use, not open.
**SAP_I[7-0]:** Idle mode, Internal use, not open.

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | PT[1:0]=2'b00, GON=1, DTE=0, DB1-0=2'b00, N_FP[3:0]=4'b1101, N_BP[3:0]=4'b1010, PE_FP[3:0]=4'b1101, PE_BP[3:0]=4'b1010, E_FP[3:0]=4'b1101, E_BP[3:0]=4'b1010, SAP[7:0]=8'b0001_0100, EQS=8'b0001_1001, EQP=8'b0001_1001, GEN_OFF=8'b0001_0100, PTG[1:0]=2'b10, ISC[3:0]=4'b010, SAP_I[7:0]= 8'b0000_1010,, PTG[1:0]=2'b10 |
| S/W Reset | PT[1:0]=2'b00, GON=1, DTE=0, DB1-0=2'b00, N_FP[3:0]=4'b1101, N_BP[3:0]=4'b1010, PE_FP[3:0]=4'b1101, PE_BP[3:0]=4'b1010, E_FP[3:0]=4'b1101, E_BP[3:0]=4'b1010, SAP[7:0]=8'b0001_0100, EQS=8'b0001_1001, EQP=8'b0001_1001, GEN_OFF=8'b0001_0100, PTG[1:0]=2'b10, ISC[3:0]=4'b010, SAP_I[7:0]= 8'b0000_1010,, PTG[1:0]=2'b10 |
| H/W Reset | PT[1:0]=2'b00, GON=1, DTE=0, DB1-0=2'b00, N_FP[3:0]=4'b1101, N_BP[3:0]=4'b1010, PE_FP[3:0]=4'b1101, PE_BP[3:0]=4'b1010, E_FP[3:0]=4'b1101, E_BP[3:0]=4'b1010, SAP[7:0]=8'b0001_0100, EQS=8'b0001_1001, EQP=8'b0001_1001, GEN_OFF=8'b0001_0100, PTG[1:0]=2'b10, ISC[3:0]=4'b010, SAP_I[7:0]= 8'b0000_1010,, PTG[1:0]=2'b10 |

**Flow Chart**

### 6.4.4 SETLUT: Set LUT Enable Related Register (B3h)

| B3 H | SETLUT(Set LUT Enable Related Register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B3 |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | LUT_ENB | -- | -- | -- | -- | -- | -- |
| Description | This command is used to set LUTenable related register<br>**LUT_ENB:** Enable/Disable the look up table.<br>0: Enable the look up table.<br>1: Disable the look up table. | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes | | | | | | | | | | | | |
| Default | Status: Power On Sequence — Default Value: LUT_EN=OTP value,<br>Status: S/W Reset — Default Value: LUT_EN= No change ,<br>Status: H/W Reset — Default Value: LUT_EN=OTP value, | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

### 6.4.5 SETCYC: Set Display Waveform Cycles (B4h)

| B4H | SETCYC( Set display waveform cycles) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B4 |
| 1st parameter | 1 | ↑ | 1 | -- | N_RTN[3:0] | | | | -- | N_NW[2:0] | | | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | E_RTN[3:0] | | | | -- | E_NW[2:0] | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | -- | DIV_E[1:0] | | -- | -- | -- | -- | -- |
| 4th parameter | 1 | ↑ | 1 | -- | SON[7:0] | | | | | | | | -- |
| 5th parameter | 1 | ↑ | 1 | -- | GDON[7:0] | | | | | | | | -- |
| 6th parameter | 1 | ↑ | 1 | -- | GDOF[7:0] | | | | | | | | -- |

Description

This command is used to set display waveform cycles

**NW[2:0]**: Frame Inversion and N-line inversion control

| NW[2:0] | Inversion Type |
|---|---|
| 0 | Frame inversion |
| 1 | 1-line inversion |
| 2 | 2-line inversion |
| 3 | 3-line inversion |
| .. | .. |
| 7 | 7-line inversion |

**RTN[3:0]:** Set the 1-line period in a clock unit.

Clock cycles=1/internal operation clock frequency

| RTN[3:0] | Clock Cycles per Line |
|---|---|
| 4'b0000 | 138 |
| 4'b0001 | 139 |
| 4'b0010 | 140 |
| 4'b0011 | 141 |
| …. | …. |
| 4'b1110 | 153 |
| 4'b1111 | 154 |

DIV_E: only use in Idle mode

**DIV_E[1:0]:**The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN3-0). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

| DIV_E1 | DIV_E0 | Division Ratio | Internal Operation Clock Frequency |
|---|---|---|---|
| 0 | 0 | 1 | fosc / 1 |
| 0 | 1 | 2 | fosc / 2 |
| 1 | 0 | 4 | fosc / 4 |
| 1 | 1 | 8 | fosc / 8 |

**Formula for the Frame Frequency:**

Frame frequency = fosc/( RTN × DIV × (NL+BP+FP) ) [HZ]

fosc: RC oscillation frequency

RTN bit: Clocks per line

DIV bit: Division ratio

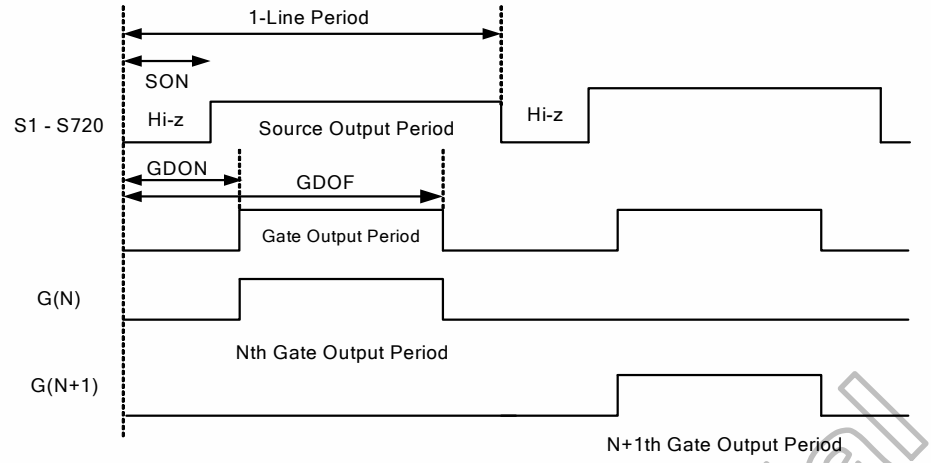
NL: The number of lines

FP: Number of lines for front porch

BP: Number of lines for back porch

BP+FP≦16

**The HX8353-C can control the display operation period time for LCD panel driving as follow:**




**SON7-0**: Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number. (Please note that the setting "00h" and "01h" is inhibited).

**GDON7-0**: Specify the valid gate output start time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the setting "00h", "01h", "02h" is inhibited).

**GDOF7-0**: Specify the gate output end time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the GDOF7-0 ≤ HCK-1).

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | N_NW[3:0]=3'b001, N_RTN[3:0]=4'b1101, PE_NW[3:0]=3'b000, E_NW[3:0]=3'b000, E_RTN[3:0]=4'b1101, DIV_E[1:0]=OTP Value, DIV_PE[1:0]=OTP Value , DIV_N[1:0]=OTP Value, SON[7:0]=8'h19, GDON[7:0]=8'h1E, GDOF[7:0]=8'h78. |
| S/W Reset | N_NW[3:0]=3'b001, N_RTN[3:0]=4'b1101, PE_NW[3:0]=3'b000, E_NW[3:0]=3'b000, E_RTN[3:0]=4'b1101, DIV_E[1:0]= No change, DIV_PE[1:0]= No change , DIV_N[1:0]=No change, SON[7:0]=8'h19, GDON[7:0]=8'h1E, GDOF[7:0]=8'h78. |
| H/W Reset | N_NW[3:0]=3'b001, N_RTN[3:0]=4'b1101, PE_NW[3:0]=3'b000, E_NW[3:0]=3'b000, E_RTN[3:0]=4'b1101, DIV_E[1:0]=OTP Value, DIV_PE[1:0]=OTP Value , DIV_N[1:0]=OTP Value, SON[7:0]=8'h19, GDON[7:0]=8'h1E, GDOF[7:0]=8'h78. |

**Flow Chart**

### 6.4.6 SETBGP: Set BGP Voltage (B5h)

| B5 H | SETBGP( Set Band Gap Voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B5 |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | BGP[3:0] | | | | - |

**Description**

This command is used to set BandGap Voltage

**BGP[3:0]: band gap voltage control**

| BGP[3:0] | VREF output |
|---|---|
| 4'b0000 | X 0.936 |
| 4'b0001 | X 0.944 |
| 4'b0010 | X 0.952 |
| 4'b0011 | X 0.96 |
| 4'b0100 | X 0.968 |
| 4'b0101 | X 0.976 |
| 4'b0110 | X 0.984 |
| 4'b0111 | X 0.992 |
| 4'b1000 | X 1.000 |
| 4'b1001 | X 1.008 |
| 4'b1010 | X 1.016 |
| 4'b1011 | X 1.024 |
| 4'b1100 | X 1.032 |
| 4'b1101 | X 1.040 |
| 4'b1110 | X 1.048 |
| 4'b1111 | X 1.056 |

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | BGP[3:0]=OTP value |
| S/W Reset | BGP[3:0]=No Change |
| H/W Reset | BGP[3:0]=OTP value |

**Flow Chart**

### 6.4.7 SETVCOM: Set VCOM Voltage (B6h)

| B6 H | SETVCOM( Set VCOM Voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6 |
| 1st parameter | 1 | ↑ | 1 | -- | VCOMG | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | VCMN[6:0] | | | | | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | -- | -- | VDV[4:0] | | | | | -- |

Description

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

**VCOMG:** When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ -VDD +0.5V ). When VCOMG = 0, VCOML voltage becomes VSSD and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished.

**VDV(4-0):** Specify the VCOM amplitude factors for panel common driving (VCOML = VCOMH – VCOM amplitude). It is possible to setup from 0.6 to 1.23 times of VREG1. When VCOMG0 = 0, the VDV(4-0) setup is invalid and VCOML is output VSSA.

| VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | VCOM Amplitude |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | VREG1*0.6 |
| 0 | 0 | 0 | 0 | 1 | VREG1*0.63 |
| 0 | 0 | 0 | 1 | 0 | VREG1*0.66 |
| 0 | 0 | 0 | 1 | 1 | VREG1*0.69 |
| 0 | 0 | 1 | 0 | 0 | VREG1*0.72 |
| 0 | 0 | 1 | 0 | 1 | VREG1*0.75 |
| 0 | 0 | 1 | 1 | 0 | VREG1*0.78 |
| 0 | 0 | 1 | 1 | 1 | VREG1*0.81 |
| 0 | 1 | 0 | 0 | 0 | VREG1*0.84 |
| 0 | 1 | 0 | 0 | 1 | VREG1*0.87 |
| 0 | 1 | 0 | 1 | 0 | VREG1*0.9 |
| 0 | 1 | 0 | 1 | 1 | VREG1*0.93 |
| 0 | 1 | 1 | 0 | 0 | VREG1*0.96 |
| 0 | 1 | 1 | 0 | 1 | VREG1*0.99 |
| 0 | 1 | 1 | 1 | 0 | VREG1*1.02 |
| 0 | 1 | 1 | 1 | 1 | Inhibit |
| 1 | 0 | 0 | 0 | 0 | VREG1*1.05 |
| 1 | 0 | 0 | 0 | 1 | VREG1*1.08 |
| 1 | 0 | 0 | 1 | 0 | VREG1*1.11 |
| 1 | 0 | 0 | 1 | 1 | VREG1*1.14 |
| 1 | 0 | 1 | 0 | 0 | VREG1*1.17 |
| 1 | 0 | 1 | 0 | 1 | VREG1*1.2 |
| 1 | 0 | 1 | 1 | 0 | VREG1*1.23 |
| 1 | 0 | 1 | 1 | 1 | Inhibit |
| 1 | 1 | 0 | 0 | 0 | Inhibit |
| 1 | 1 | 0 | 0 | 1 | Inhibit |
| 1 | 1 | 0 | 1 | 0 | Inhibit |
| 1 | 1 | 0 | 1 | 1 | Inhibit |
| 1 | 1 | 1 | 0 | 0 | Inhibit |
| 1 | 1 | 1 | 0 | 1 | Inhibit |
| 1 | 1 | 1 | 1 | 0 | Inhibit |
| 1 | 1 | 1 | 1 | 1 | Inhibit |

**Note: VCOML >= (VCL + 0.3), VCOMH <= (VLCD - 0.3) when set VDV[4:0]**

**VCMN(6-0):** Set the VCOMH voltage on normal mode. It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage.

| VCMN6 | VCMN5 | VCMN4 | VCMN3 | VCMN2 | VCMN1 | VCMN0 | VCOMH |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.405 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.41 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.415 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.42 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.425 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.43 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.435 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.44 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.445 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.45 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.455 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.46 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.465 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.47 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.475 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.48 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.485 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.49 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.495 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.5 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.505 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.51 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.515 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.52 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.525 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.53 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.535 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.54 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.545 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.55 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | VREG1 * 0.555 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.56 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.565 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.57 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.575 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.58 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.585 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.59 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.595 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.6 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.605 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.61 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.615 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.62 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.625 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.63 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.635 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.64 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.645 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.65 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.655 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.66 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.665 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.67 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.675 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.68 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.685 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.69 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.695 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.7 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.705 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.71 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | inhibit |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.715 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.72 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.725 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.73 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.735 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.74 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.745 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.75 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.755 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.76 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.765 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.77 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.78 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.785 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.79 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.795 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.8 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.805 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.81 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.815 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.82 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.825 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.83 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.835 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.84 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.845 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.85 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.855 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.86 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.865 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | VREG1 * 0.87 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.875 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.88 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.885 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.89 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.895 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.9 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.905 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.91 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.915 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.92 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.925 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.93 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.935 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.94 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.945 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.95 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.955 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.96 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.965 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.97 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.975 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.98 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | inhibit |

| | |
|---|---|
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |

<table>
<tr><td></td><td>
<table>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>VCOMG=1’b0, VDV[4:0]=OTP value, VCMN[5:0]=OTP value, VCME[5:0]=OTP value, VCMPE[5:0]=OTP value</td></tr>
<tr><td>S/W Reset</td><td>VCOMG=1’b0, VDV[4:0]= OTP value, VCMN[5:0]= OTP value, VCME[5:0]= OTP value, VCMPE[5:0]= OTP value</td></tr>
<tr><td>H/W Reset</td><td>VCOMG=1’b0, VDV[4:0]= OTP value, VCMN[5:0]= OTP value, VCME[5:0]= OTP value, VCMPE[5:0]= OTP value</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

## 6.4.8 SETGAMMA: Set Gamma Curve Related Setting (B7)

| B7H | SETGAMMA1( Set Gamma Curve1 Related Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7 |
| 1st parameter | 1 | ↑ | 1 | -- | -- | MP12 | MP11 | MP10 | -- | MP02 | MP01 | MP00 | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | MP32 | MP31 | MP30 | -- | MP22 | MP21 | MP20 | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | -- | MP52 | MP51 | MP50 | -- | MP42 | MP41 | MP40 | -- |
| 4th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CP03 | CP02 | CP01 | CP00 | -- |
| 5th parameter | 1 | ↑ | 1 | -- | CP23 | CP22 | CP21 | CP20 | CP13 | CP12 | CP11 | CP10 | -- |
| 6th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CP33 | CP32 | CP31 | CP30 | -- |
| 7th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CP43 | CP42 | CP41 | CP40 | -- |
| 8th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | OP03 | OP02 | OP01 | OP00 | -- |
| 9th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | OP14 | OP13 | OP12 | OP11 | OP10 | |
| 10th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CGM1[1:0] | | CGM0[1:0] | | -- |
| 11th parameter | 1 | ↑ | 1 | -- | -- | MN12 | MN11 | MN10 | -- | MN02 | MN01 | MN00 | -- |
| 12th parameter | 1 | ↑ | 1 | -- | -- | MN32 | MN31 | MN30 | -- | MN22 | MN21 | MN20 | -- |
| 13th parameter | 1 | ↑ | 1 | -- | -- | MN52 | MN51 | MN50 | -- | MN42 | MN41 | MN40 | -- |
| 14th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CN03 | CN02 | CN01 | CN00 | |
| 15th parameter | 1 | ↑ | 1 | -- | CN23 | CN22 | CN21 | CN20 | CN13 | CN12 | CN11 | CN10 | |
| 16th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CN33 | CN32 | CN31 | CN30 | |
| 17th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | CN43 | CN42 | CN41 | CN40 | |
| 18th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | ON03 | ON02 | ON01 | ON00 | |
| 19th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | ON14 | ON13 | ON12 | ON11 | ON10 | |

**Description**

This command is used to set Gamma Curve 1 Related Setting

| Register Groups | Positive Polarity | Description |
|---|---|---|
| Center Adjustment | CP/N0 3-0 | Variable resistor (VRTP/N) for center adjustment |
| | CP/N1 3-0 | Variable resistor (VRCP/N0)for center adjustment |
| | CP/N2 3-0 | Variable resistor (VRMP/N) for center adjustment |
| | CP/N3 3-0 | Variable resistor (VRCP/N1)for center adjustment |
| | CP/N4 3-0 | Variable resistor (VRBP/N)for center adjustment |
| Macro Adjustment | MP/N0 2-0 | 8-to-1 selector (reference voltage level of grayscale 1) |
| | MP/N1 2-0 | 8-to-1 selector (reference voltage level of grayscale 8) |
| | MP/N2 2-0 | 8-to-1 selector (reference voltage level of grayscale 20) |
| | MP/N3 2-0 | 8-to-1 selector (reference voltage level of grayscale 43) |
| | MP/N4 2-0 | 8-to-1 selector (reference voltage level of grayscale 55) |
| | MP/N5 2-0 | 8-to-1 selector (reference voltage level of grayscale 62) |
| Offset Adjustment | OP/N0 3-0 | Variable resistor (VROP/N0)for offset adjustment |
| | OP/N1 4-0 | Variable resistor (VROP/N1)for offset adjustment |

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | OTP value |
| S/W Reset | No change |
| H/W Reset | OTP value |

**Flow Chart**

### 6.4.9 PASSWDEN: Set Password enable command (B9h)

| B9 H | PASSWDEN( Set Password enable command) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB17-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9 |
| 1st parameter | 1 | ↑ | 1 | -- | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |
| 2nd parameter | 1 | ↑ | 1 | -- | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17h |

**Description**

This command is used to set extended command set access enable.

| Extend cmd | Command description |
|---|---|
| Enable | After command (B9h), must write 2 parameters (04h, 17h) by order, then can enable the extended command (Himax command) |
| Disable(default) | After command(BAh), the extended command (Himax command) can not be accessed |

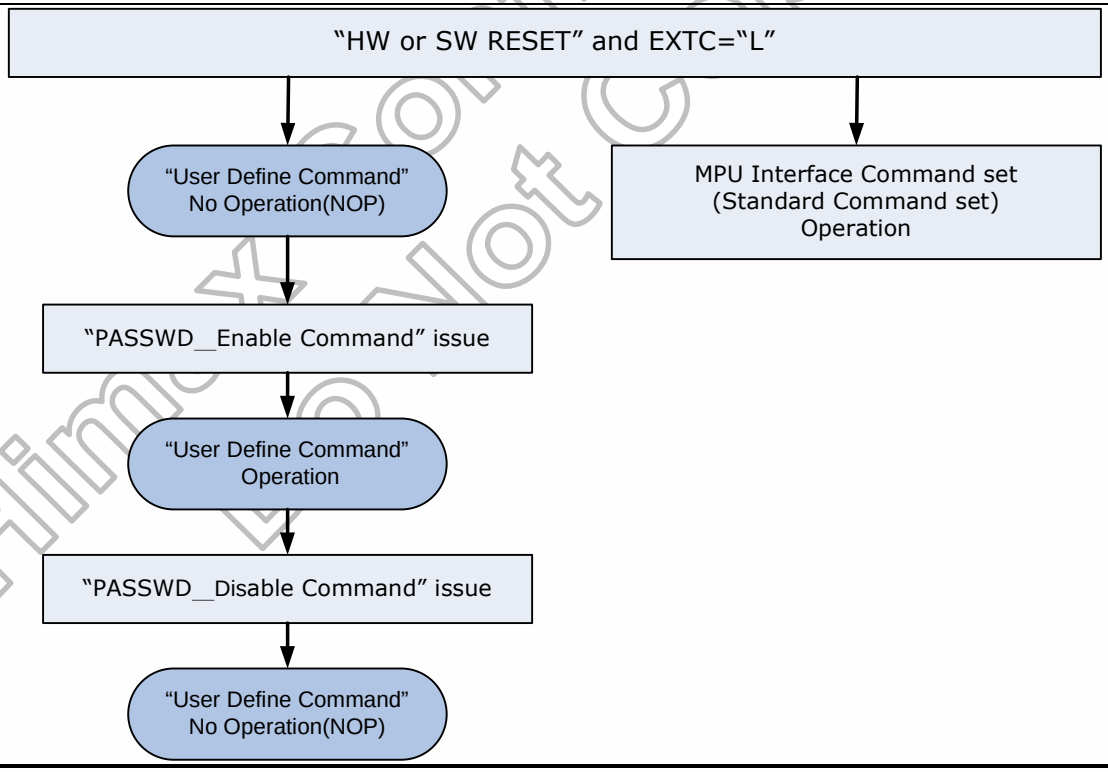
As PASSWDEN command has been written, the external pin EXTC control is invalid, and extended command can access.

**Restrictions**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |

**Flow Chart**



### 6.4.10 PASSWDDISAB: Password Disable command (BAh)

| BAH | PASSWDDISAB(Password Disable command) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB17-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BA |

**Description**

This command is used to set extended command set access enable.

| Extend cmd | Command description |
|---|---|
| Enable | After command (B9h), must write 2 parameters (17h, CCh) by order, then can enable the extended command (Himax command) |
| Disable(default) | After command(BAh), the extended command (Himax command) can not be accessed |

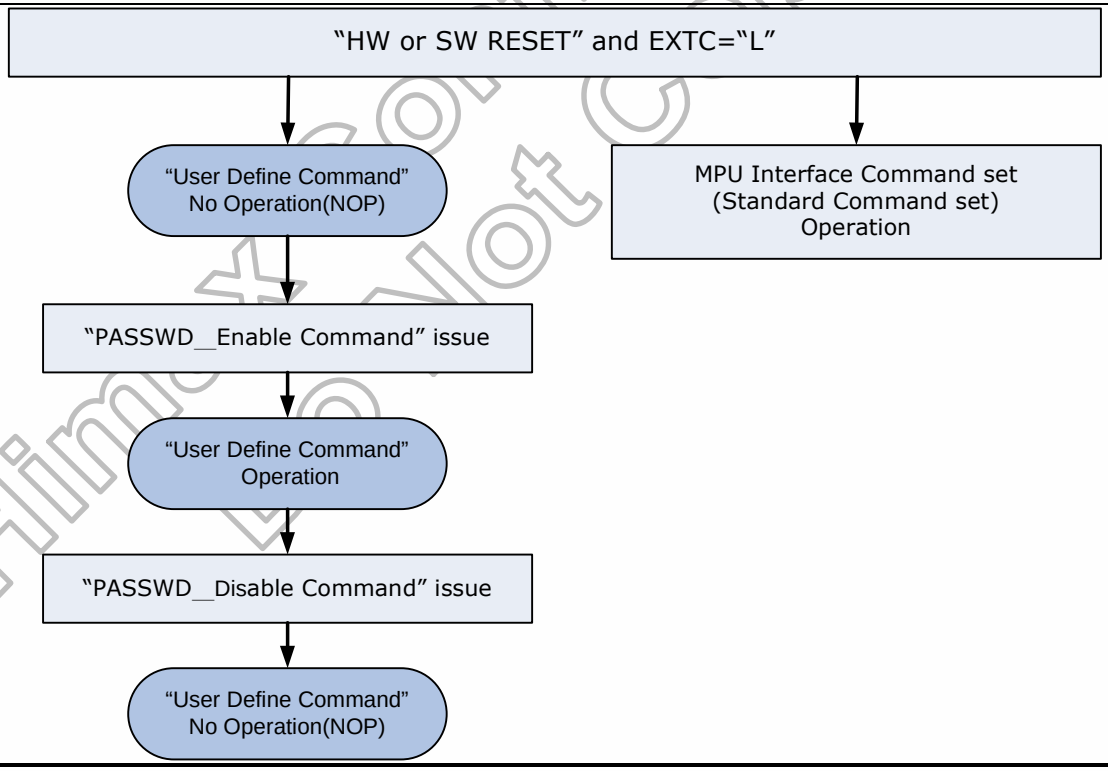
As PASSWDDISAB command has been written, it will be disable PASSWDEN command and the extended command can not be accessed.

**Restrictions**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In or Booster Off | Yes |

**Flow Chart**



### 6.4.11 SETOTP: Set OTP Related Setting (BBh)

| BB H | SETOTP( Set OTP Related Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BB |
| 1st parameter | 1 | ↑ | 1 | -- | OTP_MASK[7:0] | | | | | | | | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | OTP_INDEX[7:0] | | | | | | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | OTP_LOAD_DISABLE | DCCLK_DISABLE | OTP_POR | OTP_PWE | OTP_EN | OTPTEST_EN | VPP_SEL | OTP_PROG | -- |
| 4th parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | OTP_PTM[1:0] | | OTP_VRADJ[1:0] | | -- |
| Description | This command is used to set OTP Related Setting<br>**OTP_MASK7~OTP_MASK0:** Bit programming mask, if 1, means don't programming this bit<br>**OTP_INDEX7~OTP_INDEX0:** Set location of OTP to be programmed<br>**OTP_EN:** When written to 1, internal register begin written to OTP<br>**VPP_SEL:** When written to 1, PVSS voltage is fed to OTP<br>**OTP_LOAD_DISABLE**: When written to 1, auto load from OTP to internal register when SLPOUT command received is disabled, this is used when OTP is not yet programmed<br>**DCCLK_DISABLE:** Disable Pumping Clock<br>**OTPEST_EN:**<br>0 : normal mode, automatic OTP programming mode (by internal state machine)<br>1 : manual mode<br>0 is the default value | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes | | | | | | | | | | | | |
| Default | Status: Default Value<br>Power On Sequence: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00<br>S/W Reset: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00<br>H/W Reset: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00 | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

### 6.4.12 SETVDC: Set Internal Digital Voltage (BCh)

| **BC H** | SETVDC( Set internal digital voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BC |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | VDC_SEL[2:0] | | | -- |
| Description | This command is used to set internal digital voltage for digital circuit and GRAM<br>**VDC_SEL[1:0]:** Not open | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | VDC_SEL[2:0]=3'b110 |
| S/W Reset | VDC_SEL[2:0]=3'b110 |
| H/W Reset | VDC_SEL[2:0]=3'b110 |

Flow Chart

### 6.4.13 SETSPULSE: Set Arbiter Pulse Width (BDh)

| **BD H** | SETSPULSE( Set Arbiter Pulse Width) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | BD |
| 1st parameter | 1 | 1 | ↑ | RTBA[13:8] | | | | | | | | -- |
| 2nd parameter | 1 | 1 | ↑ | RTBA[7:0] | | | | | | | | -- |
| Description | This command is used to set GRAM arbiter pulse width, it is for internal use. | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SPULSE_ERD[2:0]=3'b100, SPULSE_EWR[2:0]=3'b100, SPULSE_IRD[2:0]=3'b100, ARBMODE_SEL=0, LPLW_EN =0, REFBL_EN[1:0]=2'b00, RPULSE [2:0]=3'b100, DPULSE [2:0]=3'b000 |
| S/W Reset | No change |
| H/W Reset | SPULSE_ERD[2:0]=3'b100, SPULSE_EWR[2:0]=3'b100, SPULSE_IRD[2:0]=3'b100, ARBMODE_SEL=0, LPLW_EN =0, REFBL_EN[1:0]=2'b00, RPULSE [2:0]=3'b100, DPULSE [2:0]=3'b000 |

Flow Chart

### 6.4.14 SETPROBE: Set Probe Signal Group (BEh)

| BE H | SETPROBE ( Set Probe Signal Group) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BE |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | TEST_MODE(0) | TEST_OE(0) | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | PROB[7:0] | | | | | | | | -- |
| Description | This command is used to set which group of signals to be observed<br>**PROBE[7:0]: Internal use**<br>TEST_MODE: Internal use<br>TEST_OE: Internal use | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes | | | | | | | | | | | | |
| Default | Status: Power On Sequence — Default Value: PROBE[7:0]=8'h00, TEST_MODE =0, TEST_OE=0<br>Status: S/W Reset — Default Value: PROBE[7:0]=8'h00, TEST_MODE =0, TEST_OE=0<br>Status: H/W Reset — Default Value: PROBE[7:0]=8'h00, TEST_MODE =0, TEST_OE=0 | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

### 6.4.15 SETPTBA: Set Power Option (BFh)

| **BF H** | SETPTBA ( Set Power Option) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BF |
| 1st parameter | 1 | ↑ | 1 | -- | PTBA[15:8] | | | | | | | | - |
| 2nd parameter | 1 | ↑ | 1 | -- | PTBA[7:0] | | | | | | | | - |
| Description | This command is used to set power circuit option<br>PTBA[15:0]: **Internal use** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PTBA[15:0]=16'h0000 |
| S/W Reset | PTBA[15:0]=16'h0000 |
| H/W Reset | PTBA[15:0]=16'h0000 |

Flow Chart

### 6.4.16 SETSTBA: Set Source Option (C0h)

| C0 H | SETSTBA ( Set Source Option) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 |
| 1st parameter | 0 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | -- | STBA[8] | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | STBA[7:0] | | | | | | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | VTESTSEL[3:0] | | | | STESTOE[1:0] | | -- | -- | -- |
| Description | This command is used to set source circuit option<br>**STBA[8:0]: Not open**<br>**VTESTSEL[3:0]:** Not open<br>**STESTOE:** Not open | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | STBA[15:0]=16'h0149; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; TLADD[7:0]=8'b0000_0000 |
| S/W Reset | STBA[15:0]=16'h0149; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; TLADD[7:0]=8'b0000_0000 |
| H/W Reset | STBA[15:0]=16'h0149; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; TLADD[7:0]=8'b0000_0000 |

Flow Chart

### 6.4.17 SETID: Set ID (C4h)

| C4 H | SETID ( Set ID) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 |
| 1st parameter | 1 | ↑ | 1 | -- | IDB1[7:0] | | | | | | | | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | -- | IDB2[6:0] | | | | | | | -- |
| 3rd parameter | 1 | ↑ | 1 | -- | IDB3[7:0] | | | | | | | | -- |
| Description | This command is used to timing controller internal test | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OTP value |
| S/W Reset | No Change |
| H/W Reset | OTP value |

Flow Chart

### 6.4.18 SETECO: Set ECO (C6h)

| C6 H | SETROMT ( Set ECO) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6 |
| 1st parameter | 1 | ↑ | 1 | -- | ECO0[7:0] (8'b0) | | | | | | | | |
| 2nd parameter | 1 | ↑ | 1 | -- | ECO1[7:0] (8'b0) | | | | | | | | |
| Description | This command is used for internal test | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |
| Default | | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

### 6.4.19 SETMREV: Set Free Running Mode (CAh)

| CA H | SETMREV ( Set Free Running Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CA |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | -- | -- | -- | -- | SFULL | -- | -- |
| Description | **The command is internal use, not open.** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SFULL=1'b0 |
| S/W Reset | SFULL=1'b0 |
| H/W Reset | SFULL=1'b0 |

Flow Chart

### 6.4.20 SETIOOPT: Set IO_OPT (CBh)

| CB H | SETIOOPT ( Set IO_OPT) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CB |
| 1st parameter | 1 | ↑ | 1 | -- | IO_OPT[7:0] | | | | | | | | -- |
| 2nd parameter | 1 | ↑ | 1 | -- | IO_OPT2[7:0] | | | | | | | | |
| Description | **This command is used for internal test** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | IO_OPT[7:0]=8b'01010101 |
| S/W Reset | IO_OPT[7:0]=8b'01010101 |
| H/W Reset | IO_OPT[7:0]=8b'01010101 |

Flow Chart

### 6.4.21 SETPANEL: Set PANEL (CCh)

| CC H | SETPANEL ( Set PANEL) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC |
| 1st parameter | 1 | ↑ | 1 | -- | -- | -- | -- | SM_PANEL | SS_PANEL | -- | -- | -- | -- |
| Description | Compensate for Panel type, layout and color filter order. | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SM_PANEL=0, SS_PANEL=0, |
| S/W Reset | SM_PANEL=0, SS_PANEL=0, |
| H/W Reset | SM_PANEL=0, SS_PANEL=0, |

Flow Chart

## 6.4.22 GETOSC: Read Internal Oscillator (E0h)

| **E0 H** | GETOSC( Read Internal oscillator setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 |
| 1st parameter | xx | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | CADJ[3:0] | | | | UADJ[2:0] | | | -- | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | -- | | | | -- | -- | RADJ[2:0] | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | OSC_EN_CON(0) | -- | -- | OSC_EN(0) | | -- |
| Description | This command is used to read internal oscillator related setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OSC_TEST=0; OSC_EN=0, CADJ[3:0]=OTP value, RADJ=OTP value, UADJ[2:0]=3'b011. |
| S/W Reset | OSC_EN=0h, if OPT is programmed, CADJ[3:0] =OTP value, RADJ=OTP value, else no change |
| H/W Reset | OSC_TEST=0; OSC_EN=0, CADJ[3:0] =OTP value, RADJ=OTP value, UADJ[2:0]=3'b011 |

Flow Chart

### 6.4.23 GETPOWER: Read Power (E1h)

| E1 H | GETPOWER( Read power related setting) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | GASENB | -- | -- | PON | DK | -- | -- | STB | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | AP[2:0] | | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | | | | -- | VC1[2:0] | | | -- |
| 5th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | VRH[3:0] | | | | -- |
| 6th parameter | 1 | 1 | ↑ | BT[3:0] | | | | -- | -- | -- | -- | -- |
| 7th parameter | 1 | 1 | ↑ | -- | -- | FS1[1:0] | | -- | -- | FS0[1:0] | | -- |
| 8th parameter | 1 | 1 | ↑ | N_DC[7:0] | | | | | | | | -- |
| 9th parameter | 1 | 1 | ↑ | E_DC[7:0] | | | | | | | | -- |
| 10th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | DCCLK_ SYNC | |
| Description | This command is used to read power related register. | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PON=1'b0, DK=1'b0, STB=1'b0, AP[2:0]=3'b000, VR2[2:0]=3'b000, VRH[3:0]=4'b0000, BT[3:0]=4'b0000, VDV[4:0]=5'b00000, VCM[5:0]=6'b000000, FS0[1:0]=2'b00, FS1[1:0]=2'b00, DC[7:0]=8'b00000000 |
| S/W Reset | PON=1'b0, DK=1'b0, STB=1'b0, AP[2:0]=3'b000, VR2[2:0]=3'b000, VRH[3:0]=4'b0000, BT[3:0]=4'b0000, VDV[4:0]=5'b00000, VCM[5:0]=6'b000000, FS0[1:0]=2'b00, FS1[1:0]=2'b00, DC[7:0]=8'b00000000 |
| H/W Reset | PON=1'b0, DK=1'b0, STB=1'b0, AP[2:0]=3'b000, VR2[2:0]=3'b000, VRH[3:0]=4'b0000, BT[3:0]=4'b0000, VDV[4:0]=5'b00000, VCM[5:0]=6'b000000, FS0[1:0]=2'b00, FS1[1:0]=2'b00, DC[7:0]=8'b00000000 |

Flow Chart

### 6.4.24 GETDISP: Read Display Related Register (E2h)

| E2 H | GETDISP( Read display related register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | PT[1:0] | | GON | DTE | D[1:0] | | -- | -- | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | N_BP[3:0] | | | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | N_FP[3:0] | | | | -- |
| 5th parameter | 1 | 1 | ↑ | -- | SAP[7:0] | | | | | | | | -- |
| 6th parameter | 1 | 1 | ↑ | -- | EQS[7:0] | | | | | | | | -- |
| 7th parameter | 1 | 1 | ↑ | -- | EQP[7:0] | | | | | | | | -- |
| 8th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | GEN_OFF[3:0] | | | | -- |
| 9th parameter | 1 | 1 | ↑ | -- | -- | -- | PTG[1:0] | | ISC[3:0] | | | | -- |
| 10th parameter | 1 | 1 | ↑ | -- | SAP_I[7:0] | | | | | | | | -- |
| 11th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | TION_DISP(0) | |
| Description | This command is used to read display related register | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | DB1-0=2'b00, GON=0, DTE=0, PT[1:0]=2'b00, P[3:0]=4'b1000, BP[3:0]=4'b1000, ISC[3:0]=4'b000, SAP[7:0]=8'h04, SAP2[7:0]=8'h04, PTG[1:0]=2'b00 |
| S/W Reset | DB1-0=2'b00, GON=0, DTE=0, PT[1:0]=No change, FP[3:0]=No change, BP[3:0]= No change, ISC[3:0]= No change, SAP[7:0]= No change, SAP2[7:0]= No change, PTG[1:0]= No change |
| H/W Reset | DB1-0=2'b00, GON=0, DTE=0, PT[1:0]=2'b00, FP[3:0]=4'b1000, BP[3:0]=4'b1000, ISC[3:0]=4'b000, SAP[7:0]=8'h04, SAP2[7:0]=8'h04, PTG[1:0]=2'b00 |

Flow Chart

### 6.4.25 GETLUT: ReadLUT Enable Related Register (E3h)

| **E3 H** | GETRGBIF( Read RGB interface related register) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | LUT_ ENB | -- | -- | -- | -- | -- | -- |
| Description | This command is used to read RGB interface related register | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | LUT_EN=OTP value, |
| S/W Reset | LUT_EN= No change , |
| H/W Reset | LUT_EN=OTP value, |

Flow Chart

### 6.4.26 GETCYC: Read Display Waveform Cycle(E4h)

| E4H | GETCYC( Read display waveform cycles) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | E47 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | N_RTN[3:0] | | | | -- | N_NW[2:0] | | | -- |
| 3th parameter | 1 | 1 | ↑ | -- | E_RTN[3:0] | | | | -- | E_NW[2:0] | | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | -- | -- | DIV_E[1:0] | | -- | -- | -- | -- | -- |
| 5th parameter | 1 | 1 | ↑ | -- | SON[7:0] | | | | | | | | -- |
| 6th parameter | 1 | 1 | ↑ | -- | GDON[7:0] | | | | | | | | -- |
| 7th parameter | 1 | 1 | ↑ | -- | GDOF[7:0] | | | | | | | | -- |
| Description | This command is used to read display waveform cycles | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | NW[3:0]=4'b0000, RTN[3:0]=4'b0000, DIV_N[1:0]=2'b00, DIV_PE=2'b00, DIV_E=2'b00, SON[7:0]=8'h00, GON[7:0]=8'h00 |
| S/W Reset | NW[3:0]=No change, RTN[3:0]= No change, DIV_N[1:0]= No change, SON [7:0]= No change, GON [7:0]= No change, GOF [7:0]= No change |
| H/W Reset | NW[3:0]=4'b0000, RTN[3:0]=4'b0000, DIV[1:0]=2'b00, DIV_PE=2'b00, DIV_E=2'b00, SON[7:0]=8'h00, GON[7:0]=8'h00 |

Flow Chart

### 6.4.27 GETBGP: Read BGP Voltage Setting (E5h)

| **E5 H** | GETBGP( Get BandGap Voltage Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | BGP[3:0] | | | | -- |
| Description | This command is used to read BandGap Voltage setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | BGP[3:0]=OTP value |
| S/W Reset | BGP[3:0]=No Change |
| H/W Reset | BGP[3:0]= OTP value |

Flow Chart

### 6.4.28 GETVCOM: Read VCOM Voltage Setting (E6h)

| **E6 H** | GETVCOM( Read VCOM Voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | E6 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | VCOMG | -- | -- | -- | -- | -- | -- | -- | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | -- | VCMN[6:0] | | | | | | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | -- | | | VDV[4:0] | | | | | -- |
| Description | This command is used to read VCOM Low and VCOM High Voltage setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | VCOMG=1'b0, VDV[4:0]= OTP value, VCMN[5:0]= OTP value, VCME[5:0]= OTP value, VCMPE[5:0]= OTP value |
| S/W Reset | VCOMG=1'b0, VDV[4:0]= OTP value, VCMN[5:0]= OTP value, VCME[5:0]= OTP value, VCMPE[5:0]= OTP value |
| H/W Reset | VCOMG=1'b0, VDV[4:0]= OTP value, VCMN[5:0]= OTP value, VCME[5:0]= OTP value, VCMPE[5:0]= OTP value |

Flow Chart

## 6.4.29 GETGAMMA: Read Gamma Curve Related Setting (E7h)

| E7 H | GETGAMMA1( Read Gamma Curve1 Related Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | E7 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | MP12 | MP11 | MP10 | -- | MP02 | MP01 | MP00 | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | -- | MP32 | MP31 | MP30 | -- | MP22 | MP21 | MP20 | -- |
| 4th parameter | 1 | 1 | ↑ | -- | -- | MP52 | MP51 | MP50 | -- | MP42 | MP41 | MP40 | -- |
| 5th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CP03 | CP02 | CP01 | CP00 | -- |
| 6th parameter | 1 | 1 | ↑ | -- | CP23 | CP22 | CP21 | CP20 | CP13 | CP12 | CP11 | CP10 | -- |
| 7th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CP33 | CP32 | CP31 | CP30 | -- |
| 8th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CP43 | CP42 | CP41 | CP40 | -- |
| 9th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | OP03 | OP02 | OP01 | OP00 | -- |
| 10th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | OP14 | OP13 | OP12 | OP11 | OP10 | |
| 11th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CGM1[1:0] | | CGM0[1:0] | | -- |
| 12th parameter | 1 | 1 | ↑ | -- | -- | MN12 | MN11 | MN10 | -- | MN02 | MN01 | MN00 | -- |
| 13th parameter | 1 | 1 | ↑ | -- | -- | MN32 | MN31 | MN30 | -- | MN22 | MN21 | MN20 | -- |
| 14th parameter | 1 | 1 | ↑ | -- | -- | MN52 | MN51 | MN50 | -- | MN42 | MN41 | MN40 | -- |
| 15th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CN03 | CN02 | CN01 | CN00 | |
| 16th parameter | 1 | 1 | ↑ | -- | CN23 | CN22 | CN21 | CN20 | CN13 | CN12 | CN11 | CN10 | |
| 17th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CN33 | CN32 | CN31 | CN30 | |
| 18th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | CN43 | CN42 | CN41 | CN40 | |
| 19th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | ON03 | ON02 | ON01 | ON00 | |
| 20th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | ON14 | ON13 | ON12 | ON11 | ON10 | |
| Description | This command is used to read Gamma Curve Related Setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OTP value |
| S/W Reset | No change |
| H/W Reset | OTP value |

Flow Chart

### 6.4.30 GETOTP: Read OTP Related Setting (EBh)

| EB H | GETOTP( Read OTP Related Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EB |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | OTP_MASK[7:0] | | | | | | | | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | OTP_INDEX[7:0] | | | | | | | | --- |
| 4th parameter | 1 | 1 | ↑ | -- | OTP_LOAD_DISABLE | DCCLK_DISABLE | OTP_POR | OTP_PWE- | OTP_PTM | OTPEST_EN | VPP_SEL | OTP_PROG | --- |
| 5th parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | OTP_PTM[1:0] | | OTP_VRADJ[1:0] | | |
| 6th parameter | 1 | 1 | ↑ | -- | OTP_DATA[7:0] | | | | | | | | --- |

**Description**

This command is used to set OTP Related Setting
**OTP_MASK7~OTP_MASK0:** Bit programming mask, if 1, means don't programming this bit
**OTP_INDEX7~OTP_INDEX0:** Set location of OTP to be programmed
**OTP_EN:** When written to 1, internal register begin written to OTP
**VPP_SEL:** When written to 1, PVSS voltage is fed to OTP
**OTP_LOAD_DISABLE**: When written to 1, auto load from OTP to internal register when SLPOUT command received is disabled, this is used when OTP is not yet programmed
**DCCLK_DISABLE:** Disable Pumping Clock
**OTPEST_EN:**
0 : normal mode, automatical OTP programming mode (by internal state machine)
1 : manual mode
0 is the default value

**Restrictions**

If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00 |
| S/W Reset | OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00 |
| H/W Reset | OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'hff, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, VPP_SEL=0, OTP_PROG=0, OTPEST_EN=0, OTP_EN=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0] =2'b00 |

**Flow Chart**

### 6.4.31 GETVDC: Read Internal Digital Voltage Setting (ECh)

| EC H | GETVDC( Read internal digital voltage) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | EC |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | VDC_SEL[2:0] | | | -- |
| Description | **This command is used to read internal digital voltage setting** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | VDC_SEL[1:0]=2'b00 |
| S/W Reset | VDC_SEL[1:0]=2'b00 |
| H/W Reset | VDC_SEL[1:0]=2'b00 |

Flow Chart

### 6.4.32 GETSPULSE: Read Arbiter Pulse Width (EDh)

| **ED H** | GETSPULSE( Get Arbiter Pulse Width) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NRD | NWR | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | 1 | ↑ | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ED |
| 1st parameter | 1 | 1 | ↑ | RTBA[13:8] | | | | | | | | - |
| 2nd parameter | 1 | 1 | ↑ | RTBA[7:0] | | | | | | | | |
| Description | This command is used to get GRAM arbiter pulse width, it is for internal use. | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SPULSE_ERD[2:0]=3'b011, SPULSE_EWR[2:0]=3'b001, SPULSE_IRD[2:0]=3'b011, ARBMODE_SEL=0, LPLW_EN =0, REFBL_EN[1:0]=2'b00 RPULSE [2:0]=3'b011, DPULSE [2:0]=3'b001 |
| S/W Reset | No change |
| H/W Reset | SPULSE_ERD[2:0]=3'b011, SPULSE_EWR[2:0]=3'b001, SPULSE_IRD[2:0]=3'b011, ARBMODE_SEL=0, LPLW_EN =0, REFBL_EN[1:0]=2'b00, RPULSE [2:0]=3'b011, DPULSE [2:0]=3'b001 |

Flow Chart

### 6.4.33 GETPROBE: Read Probe Signal Group (EEh)

| EE H | GETPROBE ( Read Probe Signal Group) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | EE |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | TEST_MODE | TEST_OE | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | PROB[7:0] | | | | | | | | -- |
| Description | **This command is used to read which group of signals to be observed** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PROBE[7:0]=8'h00, TEST_MODE=1'b0, TEST_OE=1'b0 |
| S/W Reset | PROBE[7:0]=8'h00, TEST_MODE=1'b0, TEST_OE=1'b0 |
| H/W Reset | PROBE[7:0]=8'h00, TEST_MODE=1'b0, TEST_OE=1'b0 |

Flow Chart

### 6.4.34 GETPTBA: Read Power Option (EFh)

| **EF H** | GETPTBA ( Read Power Option) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | EF |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | PTBA[15:8] | | | | | | | | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | PTBA[7:0] | | | | | | | | -- |
| Description | This command is used to read power circuit option setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PTBA[15:0]=16'h0000; |
| S/W Reset | PTBA[15:0]=16'h0000; |
| H/W Reset | PTBA[15:0]=16'h0000; |

Flow Chart

### 6.4.35 GETSTBA: Read Source Option (F0h)

| F0 H | GETSTBA ( Read Source Option) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | | | | | | | | STBA [8] | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | STBA[7:0] | | | | | | | | -- |
| 4th parameter | 1 | 1 | ↑ | -- | VTESTSEL[3:0] | | | | STESTOE[1:0] | | | | -- |
| Description | This command is used to read source circuit option setting | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | STBA[15:0]=16'h0081; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; |
| S/W Reset | STBA[15:0]=16'h0081; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; |
| H/W Reset | STBA[15:0]=16'h0081; VTESTSEL[3:0]=4'b0000; STESTOE1=1'b0, STESTOE0=1'b0, GAOE=1'b0; GMA=1'b0; |

Flow Chart

### 6.4.36 GETPFUSE: Get Internal OTP (F1h)

| F1 H | GETPFUSE ( Set internal Efuse) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1 |
| 1st parameter | 1 | ↑ | 1 | -- | - | - | - | - | - | - | - | PFUSE | |
| Description | This command is used to set source circuit option<br>**PFUSE: Internal use for OTP programming. This pad is only for internal use, not open.** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | PFUSE=0 |
| S/W Reset | PFUSE=0 |
| H/W Reset | PFUSE=0 |

Flow Chart

### 6.4.37 GETHXID: Read Himax ID (F4h)

| F4 H | GETHXID ( Read) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | ID_version[7:0](8'h53) | | | | | | | | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | IDB2_version [7:0](0Ch) | | | | | | | | |
| 4rd parameter | 1 | 1 | ↑ | -- | VersionID[7:0](00h) | | | | | | | | -- |
| Description | It is for internal use, not open. | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | |
| Normal Mode On, Idle Mode On, Sleep Out | |
| Partial Mode On, Idle Mode Off, Sleep Out | |
| Partial Mode On, Idle Mode On, Sleep Out | |
| Sleep In | |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | |
| S/W Reset | |
| H/W Reset | |

Flow Chart

### 6.4.38 GETECO: Read ECO(F6h)

| F6H | GETECO ( Read ) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6 |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | ECO0[7:0] | | | | | | | | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | ECO1[7:0] | | | | | | | | -- |
| Description | It is for internal use, not open. | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |
| Register Availability | Status | Availability | | | | | | | | | | | |
| | Normal Mode On, Idle Mode Off, Sleep Out | | | | | | | | | | | | |
| | Normal Mode On, Idle Mode On, Sleep Out | | | | | | | | | | | | |
| | Partial Mode On, Idle Mode Off, Sleep Out | | | | | | | | | | | | |
| | Partial Mode On, Idle Mode On, Sleep Out | | | | | | | | | | | | |
| | Sleep In | | | | | | | | | | | | |
| Default | Status | Default Value | | | | | | | | | | | |
| | Power On Sequence | | | | | | | | | | | | |
| | S/W Reset | | | | | | | | | | | | |
| | H/W Reset | | | | | | | | | | | | |
| Flow Chart | | | | | | | | | | | | | |

### 6.4.39 GETMREV: Get Free Running Mode (FAh)

| FA H | GETMREV ( Get Free Running Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15 -8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | FA |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | SFULL | -- | -- |
| Description | **It is for internal use, not open.** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | |
| Normal Mode On, Idle Mode On, Sleep Out | |
| Partial Mode On, Idle Mode Off, Sleep Out | |
| Partial Mode On, Idle Mode On, Sleep Out | |
| Sleep In | |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SFULL=0 |
| S/W Reset | SFULL=0 |
| H/W Reset | SFULL=0 |

Flow Chart

### 6.4.40 GETIOOPT: Get IO_OPT (FBh)

| FB H | GETIOOPT ( Get IO_OPT) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | FB |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | IO_OPT[7:0](0101_0101) | | | | | | | | -- |
| 3rd parameter | 1 | 1 | ↑ | -- | IO_OPT2[7:0] (0000_0000) | | | | | | | | |
| Description | **It is for internal use, not open.** | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | |
| Normal Mode On, Idle Mode On, Sleep Out | |
| Partial Mode On, Idle Mode Off, Sleep Out | |
| Partial Mode On, Idle Mode On, Sleep Out | |
| Sleep In | |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | IO_OPT[7:0]=8b'00000000 |
| S/W Reset | IO_OPT[7:0]=8b'00000000 |
| H/W Reset | IO_OPT[7:0]=8b'00000000 |

Flow Chart

### 6.4.41 GETPANEL: Get PANEL (FCh)

| FC H | SETPANEL ( Set PANEL) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DNC | NWR | NRD | DB15-8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | HEX |
| Command | 0 | ↑ | 1 | -- | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FC |
| 1st parameter | 1 | 1 | ↑ | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| 2nd parameter | 1 | 1 | ↑ | -- | -- | -- | -- | SM_PANEL | SS_PANEL | -- | -- | -- | -- |
| Description | Compensate for Panel type, layout and color filter order. | | | | | | | | | | | | |
| Restrictions | If EXTC is high or enable PASSWDEN command (even EXTC = low) can enable this command | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | |
| Normal Mode On, Idle Mode On, Sleep Out | |
| Partial Mode On, Idle Mode Off, Sleep Out | |
| Partial Mode On, Idle Mode On, Sleep Out | |
| Sleep In | |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | SM_PANEL=0, SS_PANEL=0, |
| S/W Reset | SM_PANEL=0, SS_PANEL=0, |
| H/W Reset | SM_PANEL=0, SS_PANEL=0, |

Flow Chart

# 7. Electrical Characteristic

## 7.1 Absolute Maximum Ratings

(VSS = 0V)

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage 1 | VDD | - 0.3 ~ + 3.7 | V |
| Supply voltage 2 | VDDI | - 0.3 ~ + 3.7 | V |
| Drive Supply Voltage | VGH – VGL | - 0.3 ~ + 32.0 | V |
| Input voltage range | VIN | - 0.3 ~ VDDI + 0.3 | V |
| Output voltage range | VO | - 0.3 ~ VDDI+ 0.3 | V |
| Operating temperature range | TOPR | - 40 ~ + 85 | °C |
| Storage temperature range | TSTG | - 55 ~ + 125 | °C |

**Table 7. 1 Absolute Maximum Ratings**

## 7.2 ESD Protection Level

| Mode | Test Condition | Protection Level | Unit |
|---|---|---|---|
| Human Body Model | C=100 pF, R=1.5kΩ | > 3000 | V |
| Machine Model | C=200 pF, R=0.0Ω | > 300 | V |

**Table 7. 2 ESD Protection Level**

## 7.3 Maximum Series Resistance

| Name | Type | Maximum Series Resistance | Unit |
|---|---|---|---|
| VDD | Power supply | 10 | Ω |
| VDDI | Power supply | 10 | Ω |
| VSSA | Power supply | 10 | Ω |
| VSSD | Power supply | 10 | Ω |
| OSC | Input | 100 | Ω |
| EXTC | Input | 100 | Ω |
| P68, BS2, BS1, BS0 | Input | 100 | Ω |
| STE_SEL, GC_SEL, SPI_SEL | Input | 100 | Ω |
| RSO0, RSO1, RSO2 | Input | 100 | Ω |
| LC_SEL0, LC_SEL1, BURN | Input | 100 | Ω |
| NRESET, NCS, DNC_SCL | Input | 100 | Ω |
| NWR_RNW, NRD_E | Input | 100 | Ω |
| TEST[3:1], VDC_ENB | Input | 100 | Ω |
| SS_PANEL, GS_PANEL, REV_PANEL, BGR_PANEL | Input | 100 | Ω |
| DUMMYR1,DummyR2, | Input | 100 | Ω |
| DB0_SDA, DB17 ~ DB1 | Input / Output | 100 | Ω |
| VGH | Capacitor connection | 10 | Ω |
| VGL | Capacitor connection | 10 | Ω |
| C11A, C11B | Capacitor connection | 10 | Ω |
| C22A, C22B | Capacitor connection | 10 | Ω |
| C21A, C21B | Capacitor connection | 10 | Ω |
| VDDD | Capacitor connection | 20 | Ω |
| VLCD | Capacitor connection | 10 | Ω |
| VCL | Capacitor connection | 10 | Ω |
| TE | Output | 100 | Ω |
| VCOMH, VCOML | Output | 50 | Ω |
| VREGIOUT | Output | 50 | Ω |
| VREF | Output | 50 | Ω |
| VTESTOUT | Output | 50 | Ω |
| VCOM | Output | 50 | Ω |

**Table 7. 3**

## 7.4 DC Characteristics

### 7.4.1 DC Characteristics List

| Parameter | Symbol | Conditions | Related Pins | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Power & Operating Voltages** | | | | | | | |
| IO Operating voltage | VDDI | - | VDDI(2) | 1.65 | 1.8 | 1.95 | V |
| Analog & Logic Operating voltage | VDD,VDDI | - | VDD,VDDI (2) | 2.3 | 2.5/2.75 | 2.9 | |
| Source Drive Voltage | VS | - | VS(3) | 3.0 | 4.5 | 5.0 | |
| Gate Drive High Voltage | VGH | - | VGH(3) | 9.0 | 14.0 | 16. | |
| Drive Supply Voltage | VGH-VGL | - | VGH, VGL(3) | 15.0 | 27.0 | 30 | |
| **Input / Output** | | | | | | | |
| High level input voltage | VIH | - | Note(1),(2) | 0.7VDDI | - | VDDI | V |
| Low level input voltage | VIL | - | Note(1),(2) | VSSA | - | 0.3VDDI | |
| High level output voltage | VOH | IOH = -1.0mA | DB17 to DB0, TE, TEST1(2) | 0.8VDDI | - | VDDI | |
| Low level output voltage | VOL | IOL = +1.0mA | | VSSA | - | 0.2VDDI | |
| Input leakage current | IIL | VIN = VDDI or VSSA | Note(1),(2) | -1.0 | - | +1.0 | µA |

**Note:** (1) OSC, P68, BS1, BS0, NRESET, DNC_SCL, NWR_RNW, NRD_E, and DB17 to DB0 pins
(2), (3) When the measurement are performed with LCD module, Measurement Points are like below

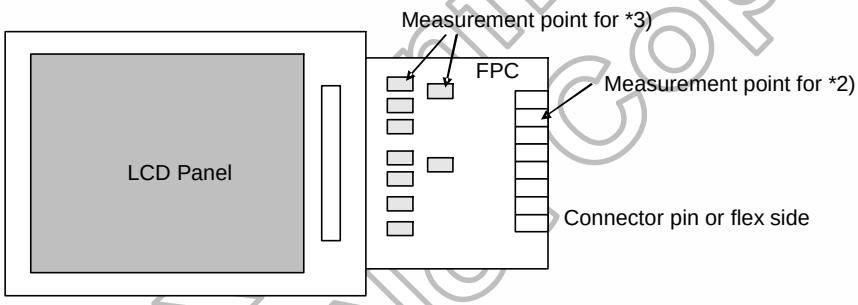



**Table 7. 4 DC Characteristics 1**

| Parameter | Symbol | Conditions | Related Pins | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **VCOM Generator** | | | | | | | |
| VCOM amplitude | VCOMA | No load | VCOMH VCOML | 2.5 | -- | 5 | V |
| VCOM output high resistance | RVCOMH | VCOM output = High IVCOM = 1mA | VCOM | - | 100 | - | Ω |
| VCOM output low resistance | RVCOML | VCOM output = Low IVCOM = 1mA | VCOM | - | 100 | - | |
| **Source Driver** | | | | | | | |
| Gray scale resistance | Rgray | Rap~Rjp, Ran~Rjn, R0~R62 of gray voltage generator | S1 to S396 | 0.7*Rx | Rx | 1.3*Rx | Ω |
| Drive output current(1),(2) | IVOSH | VS=4.25V, VSO=V0 at positive, VOUT=V0-2V | S1 to S396 | - | -200 | -100 | µA |
| | IVOSL | VS=4.25V, VSO=V0 at negative, VOUT=V0-2V | S1 to S396 | 100 | 200 | - | µA |
| Output voltage deviation | DVOS | VSSD+1.0 ~ VS-1.0 | S1 to 396 | - | ±10 | ±20 | mV |
| | | VSSD+0.1V ~ VSSD+1.0 VS-1.0 ~ VS-0.1V | S1 to 396 | - | ±30 | ±50 | mV |
| Output voltage range | VOS | - | S1 to 396 | 0.1 | - | VS-0.1 | V |
| **Gate Driver** | | | | | | | |
| Output ON resistance(3) | RONG | Ta = 25°C | G1 to G162 | - | 2 | 3 | kΩ |

**Note:** (1) VSO is the output voltage of source output pins S1 to S396.
(2) VOUT is the applied voltage to source output pins S1 to S396.
(3) Resistance value when -0.1[mA] is applied during the ON status of the gate output pin G0 to G160.
RON [ ] = V [V] / 0.1[mA] ( V: Voltage change when –0.1[mA] is applied in the on status.)

**Table 7. 5 DC Characteristics 2**

### 7.4.2 Current Consumption

| Host I/F | Mode of operation | Frame Frequency | Inversion Mode | Image | Memory Data Access Control (MY:MX:MV) | Current consumption | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Typical | | Worst case | |
| | | | | | | VDD (mA) | VDDI (mA) | VDD (mA) | VDDI (mA) |
| Host interface NOT active | - Normal Mode On<br>- Partial Mode Off<br>- Idle Mode Off<br>- Sleep Out Mode | 60Hz | TBD | Note(1) | X;X;X | TBD | TBD | TBD | TBD |
| | | | TBD | Note(2) | X;X;X | TBD | TBD | TBD | TBD |
| | | | TBD | Note(3) | X;X;X | TBD | TBD | TBD | TBD |
| | | | TBD | Note(4) | X;X;X | TBD | TBD | TBD | TBD |
| | | | TBD | Note(5) | X;X;X | TBD | TBD | TBD | TBD |
| | - Normal Mode On<br>- Partial Mode Off<br>- Idle Mode On<br>- Sleep Out Mode | 60Hz | TBD | Note(5) | X;X;X | TBD | TBD | TBD | TBD |
| | - Normal Mode Off<br>- Partial Mode On<br>(32 lines)<br>- Idle Mode Off<br>- Sleep Out Mode | 60Hz | TBD | Grey Levels | X;X;X | TBD | TBD | TBD | TBD |
| | - Normal Mode Off<br>- Partial Mode On<br>(32 lines)<br>- Idle Mode On<br>- Sleep Out Mode | 60Hz | TBD | Note(6) | X;X;X | TBD | TBD | TBD | TBD |
| | | | TBD | Note(7) | X;X;X | TBD | TBD | TBD | TBD |
| | - Sleep In Mode | N/A | N/A | N/A | X;X;X | TBD | | TBD | |
| Host interface active | - Normal Mode On<br>- Partial Mode Off<br>- Idle Mode Off<br>- Sleep Out Mode | 60Hz | TBD | 262k Colors(8)<br>CPU Access @ 15fps | 0;0;0 | TBD | TBD | TBD | TBD |
| | | | | | 0;0;1 | TBD | TBD | TBD | TBD |
| | | | | | 0;1;0 | TBD | TBD | TBD | TBD |
| | | | | | 0;1;1 | TBD | TBD | TBD | TBD |
| | | | | | 1;0;0 | TBD | TBD | TBD | TBD |
| | | | | | 1;0;1 | TBD | TBD | TBD | TBD |
| | | | | | 1;1;0 | TBD | TBD | TBD | TBD |
| | | | | | 1;1;1 | TBD | TBD | TBD | TBD |
| | | | | 262k Colors(8)<br>CPU Access @ 25fps | 0;0;0 | TBD | TBD | TBD | TBD |
| | | | | | 0;0;1 | TBD | TBD | TBD | TBD |
| | | | | | 0;1;0 | TBD | TBD | TBD | TBD |
| | | | | | 0;1;1 | TBD | TBD | TBD | TBD |
| | | | | | 1;0;0 | TBD | TBD | TBD | TBD |
| | | | | | 1;0;1 | TBD | TBD | TBD | TBD |
| | | | | | 1;1;0 | TBD | TBD | TBD | TBD |
| | | | | | 1;1;1 | TBD | TBD | TBD | TBD |

Typical Case:
TA = 25oC
VDDB2 = 2.75V
VDDB1 = 1.8V

Worst Case:
TA = -30 to70oC
VDDB2 = 2.5V to 2.9V
VDDB1 = 1.65V to 2.5V
Includes Process Variance.

**Note:** X Do not care
(1) All pixels black
(2) Checker board one by one
(3) Checker board 4 by 4
(4) Grey-scale from top to bottom
(5) 20% Black, 80%White
(6) Black & White Checker board 8 by 8.
(7) Absolute Worst Case Patterns: Defined by Display Supplier
(8) Absolute Worst Case Patterns and Sequences: Defined by Display Supplier
(9) Absolute worst case VDD current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.
(10) Absolute worst case VDDI current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.
(11) Inrush currents are not included in current consumption values

**Table 7. 6 Current Consumption**

## 7.5 AC CHARACTERISTICS

### 7.5.1 Parallel Interface Characteristics (8080-series MPU)

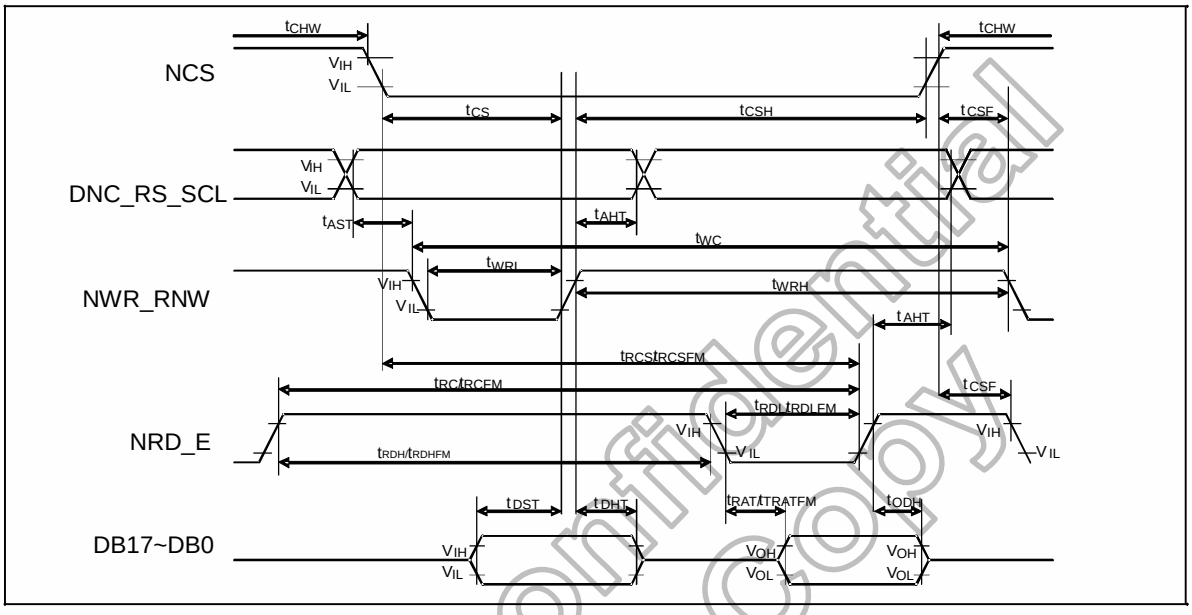


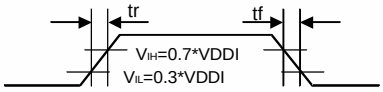

**Figure 7. 1 Parallel Interface characteristics (8080-series MPU)**

(VSSA=0V, VDDI=1.65V to 2.50V, VDD=2.3V to 2.9V,Ta = -30 to 70°C)

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| DNC_RS_SCL | $t_{AST}$ | Address setup time | 0 | - | ns | - |
| | $t_{AHT}$ | Address hold time (Write/Read) | 10 | - | | |
| NCS | $t_{CHW}$ | Chip select "H" pulse width | 0 | - | ns | - |
| | $t_{CS}$ | Chip select setup time (Write) | 15 | - | | |
| | $t_{RCS}$ | Chip select setup time (Read ID) | 45 | - | | |
| | $t_{RCSFM}$ | Chip select setup time (Read FM) | 355 | - | | |
| | $t_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | | |
| NWR_RNW | $t_{WC}$ | Write cycle | 66 | - | ns | - |
| | $t_{WRH}$ | Control pulse "H" duration | 15 | - | | |
| | $t_{WRL}$ | Control pulse "L" duration | 15 | - | | |
| NRD_E (ID) | $t_{RC}$ | Read cycle (ID) | 160 | - | ns | When read ID data |
| | $t_{RDH}$ | Control pulse "H" duration (ID) | 90 | - | | |
| | $t_{RDL}$ | Control pulse "L" duration (ID) | 45 | - | | |
| NRD_E (FM) | $t_{RCFM}$ | Read cycle (FM) | 450 | - | ns | When read from frame memory |
| | $t_{RDHFM}$ | Control pulse "H" duration (FM) | 90 | - | | |
| | $t_{RDLFM}$ | Control pulse "L" duration (FM) | 355 | - | | |
| DB17 to DB0 | $t_{DST}$ | Data setup time | 10 | - | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| | $t_{DHT}$ | Data hold time | 10 | - | | |
| | $t_{RAT}$ | Read access time (ID) | - | 40 | | |
| | $t_{RATFM}$ | Read access time (FM) | - | 340 | | |
| | $t_{ODH}$ | Output disable time | 20 | 80 | | |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDB1 for Input signals.

Input Signal Slope




Output Signal Slope

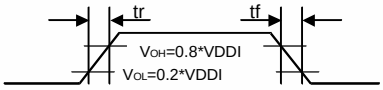



**Table 7. 7 Parallel Interface characteristics (8080-series MPU)**

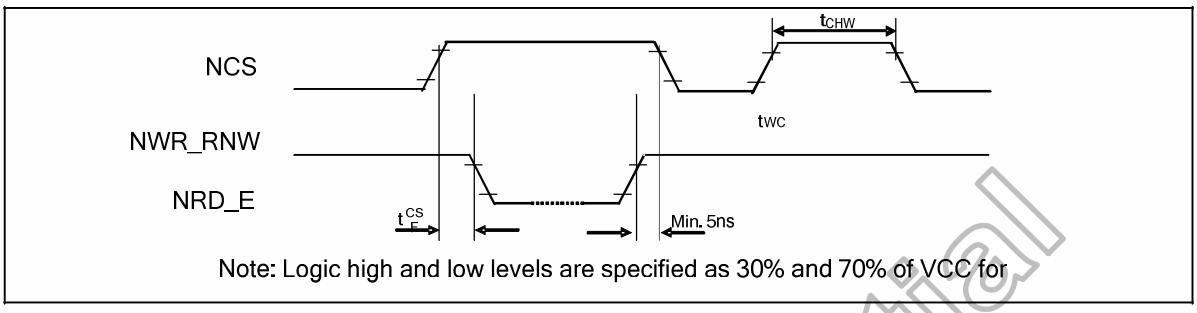



**Figure 7. 2 Chip select timing**

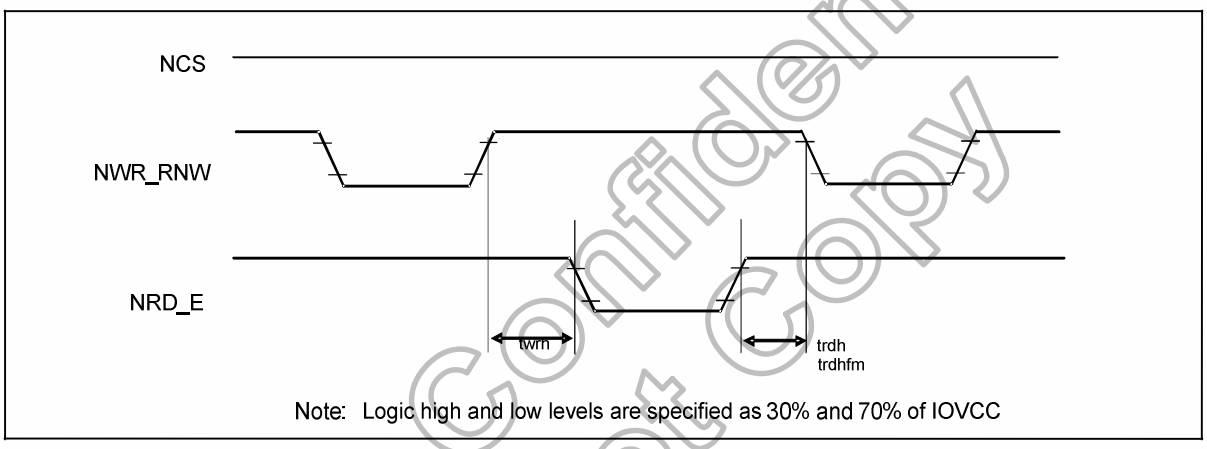



**Figure 7. 3 Write to read and read to write timing**

## 7.5.2 Serial Interface Characteristics

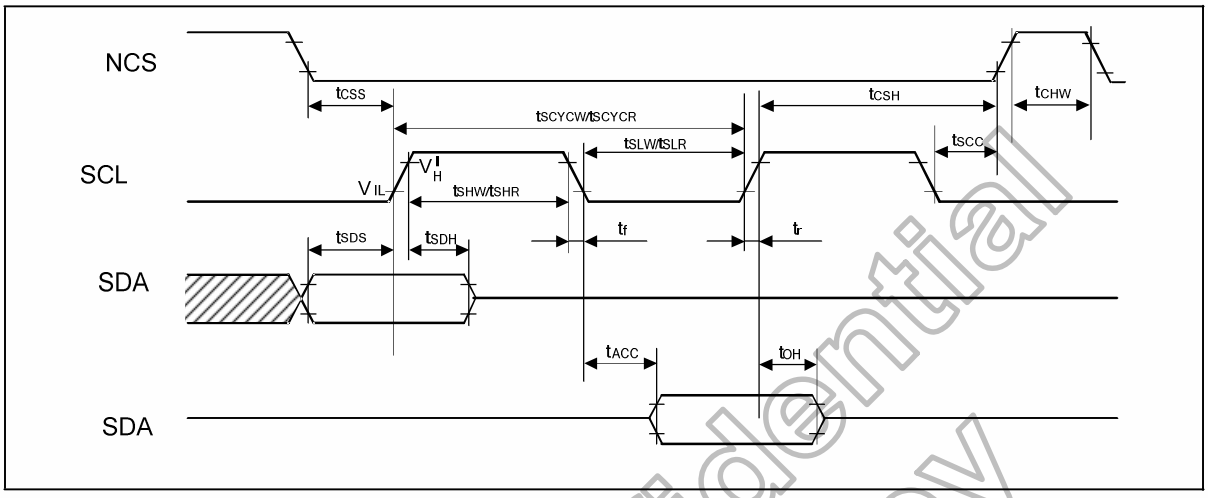


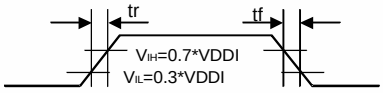

**Figure 7. 4 Serial Interface Characteristics**

(VSSA=0V, VDDI=1.65V to 2.50V, VDD=2.5V to 2.9V,Ta = -30 to 70°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Serial clock cycle (Write)<br>SCL "H" pulse width (Write)<br>SCL "L" pulse width (Write) | $t_{SCYCW}$<br>$t_{SHW}$<br>$t_{SLW}$ | SCL | 66<br>15<br>15 | -<br>-<br>- | -<br>-<br>- | ns |
| Data setup time (Write)<br>Data hold time (Write) | $t_{SDS}$<br>$t_{SDH}$ | SDA | 10<br>10 | -<br>- | -<br>- | ns |
| Serial clock cycle (Read)<br>SCL "H" pulse width (Read)<br>SCL "L" pulse width (Read) | $t_{SCYCR}$<br>$t_{SHR}$<br>$t_{SLR}$ | SCL | 150<br>60<br>60 | -<br>-<br>- | -<br>-<br>- | ns |
| Access Time | $t_{ACC}$ | SDA For maximum $C_L$=30pF<br>For maximum $C_L$=8pF | 10 | - | 50 | ns |
| Output disable time | $t_{OH}$ | SDA For maximum $C_L$=30pF<br>For maximum $C_L$=8pF | 15 | - | 50 | ns |
| NCS "H" pulse width | $t_{CHW}$ | NCS | 40 | - | - | ns |
| NCS-SCL time (write)<br>NCS-SCL time (write) | $t_{CSS}$<br>$t_{CSH}$ | NCS | 15<br>15 | -<br>- | -<br>- | ns |
| NCS-SCL time (Read)<br>NCS-SCL time (Read) | $t_{CSS}$<br>$t_{CSH}$ | NCS | 60<br>65 | -<br>- | -<br>- | ns |

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDB1 for Input signals. For output, see Section 7.7.6.2

Input Signal Slope




Output Signal Slope

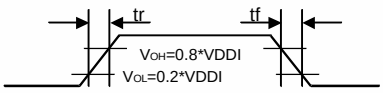



**Table 7. 8 Serial Interface Characteristics**

### 7.5.3 Reset Input Timing

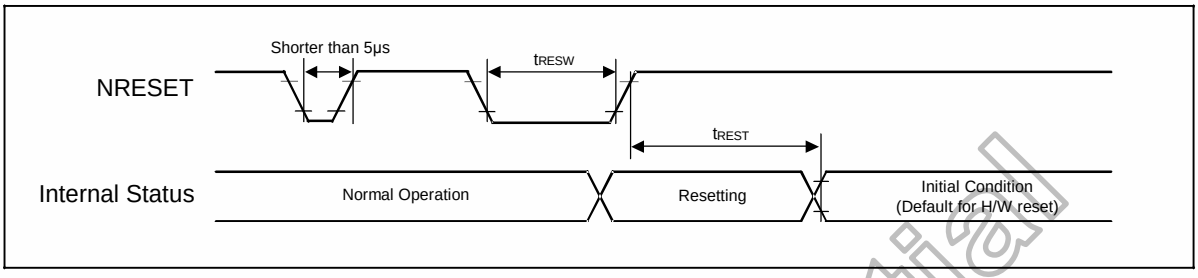


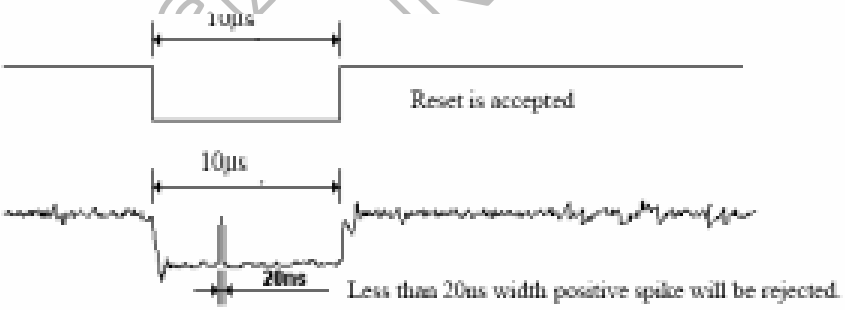

**Figure 7. 5 Reset input timing**

| Symbol | Parameter | Related Pins | Min. | Typ. | Max. | Note | Unit |
|---|---|---|---|---|---|---|---|
| $t_{RESW}$ | Reset low pulse width(1) | NRESET | 10 | - | - | - | µs |
| $t_{REST}$ | Reset complete time(2) | - | - | - | 5 | When reset applied during Sleep In mode | ms |
| | | - | | - | 120 | When reset applied during Sleep Out mode | ms |

**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

| NRESET Pulse | Action |
|---|---|
| Shorter than 5µs | Reset Rejected |
| Longer than 10µs | Reset |
| Between 5 µs and 10µs | Reset Start |

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, IDB2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



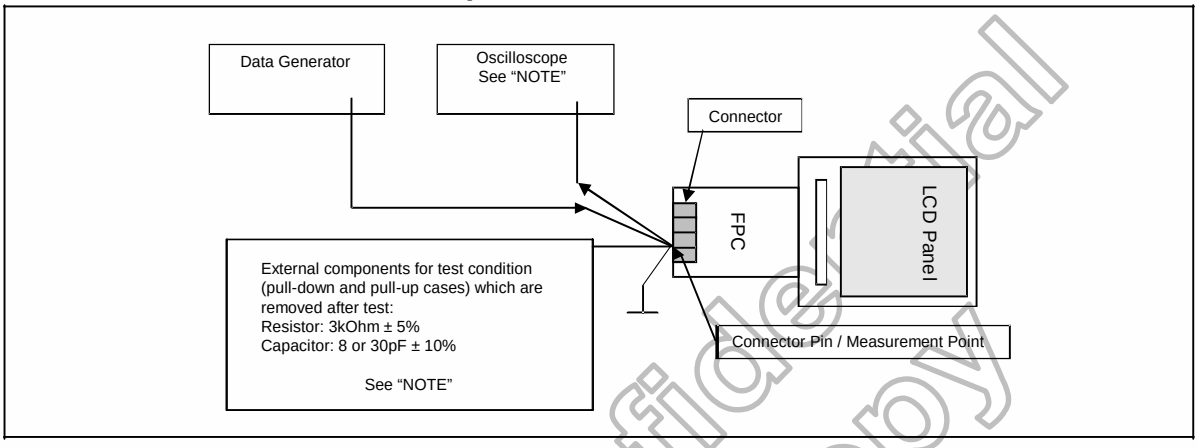

(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

**Table 7. 9**

## 7.5.4 Measurement Conditions

### 7.5.4.1 tRATFM, tODH Measurement Condition

#### Measurement Condition Set-up




**Note:** Capacitances and resistances of the oscilloscope's probe must be included externals components in these Measurements

**Figure 7. 6**

#### Minimum Value Measurement

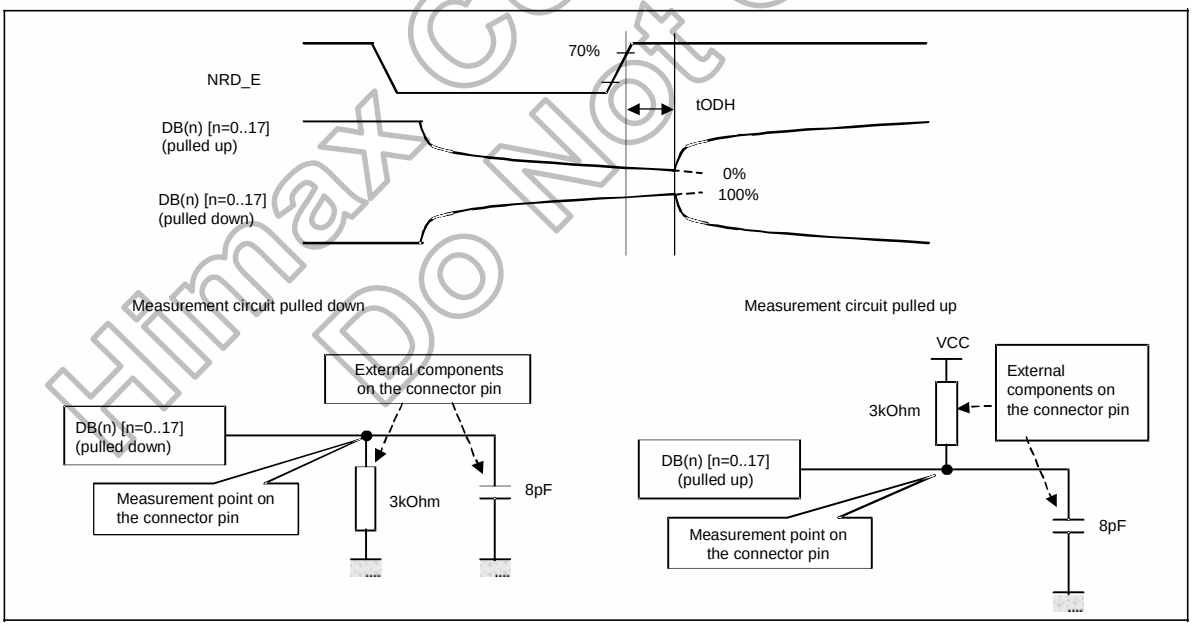



**Figure 7. 7**

## Maximum Value Measurement

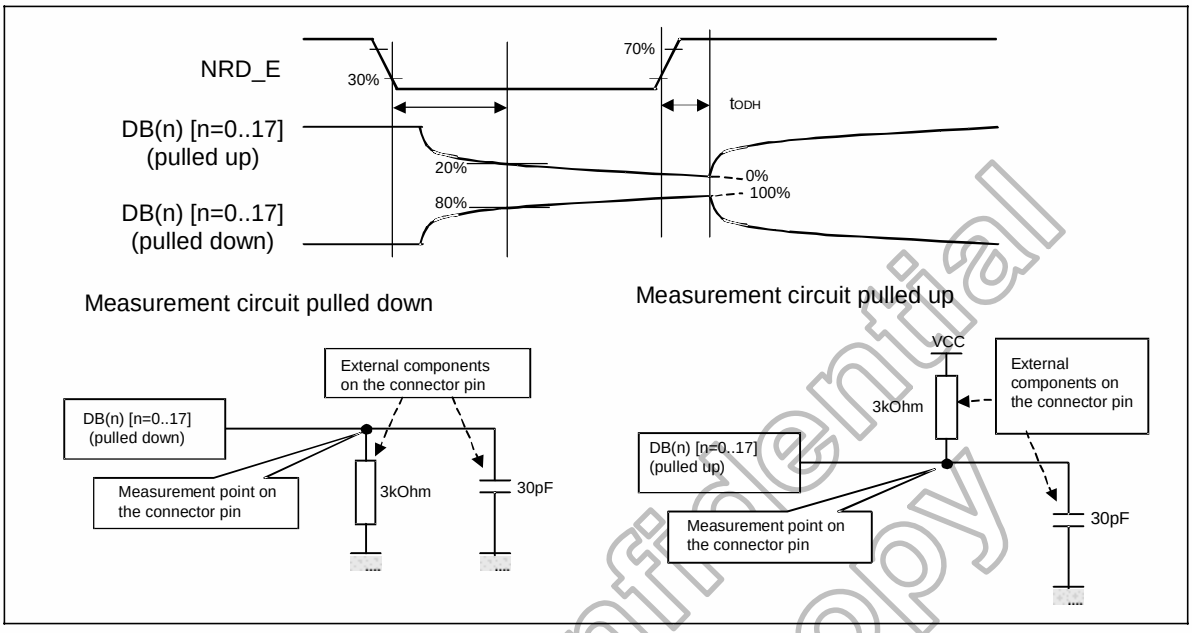
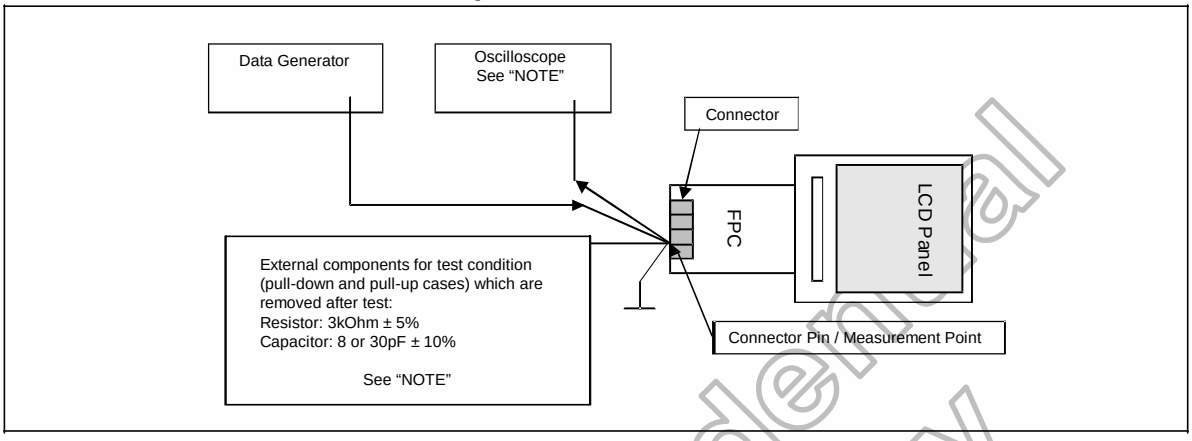



**Figure 7. 8**

### 7.5.4.2 tACC, tOH Measurement Condition

#### Measurement Condition Set-up




**Note:** Capacitances and resistances of the oscilloscope's probe must be included externals components in these Measurements

**Figure 7. 9**

#### Minimum Value Measurement

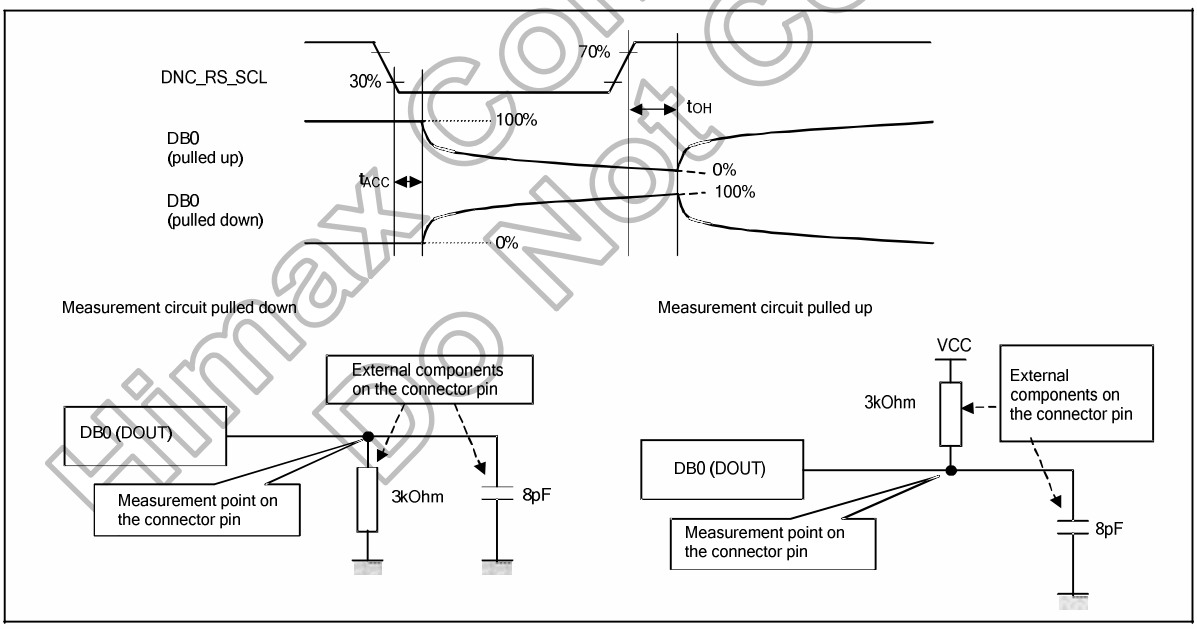



**Figure 7. 10**

## Maximum Value Measurement

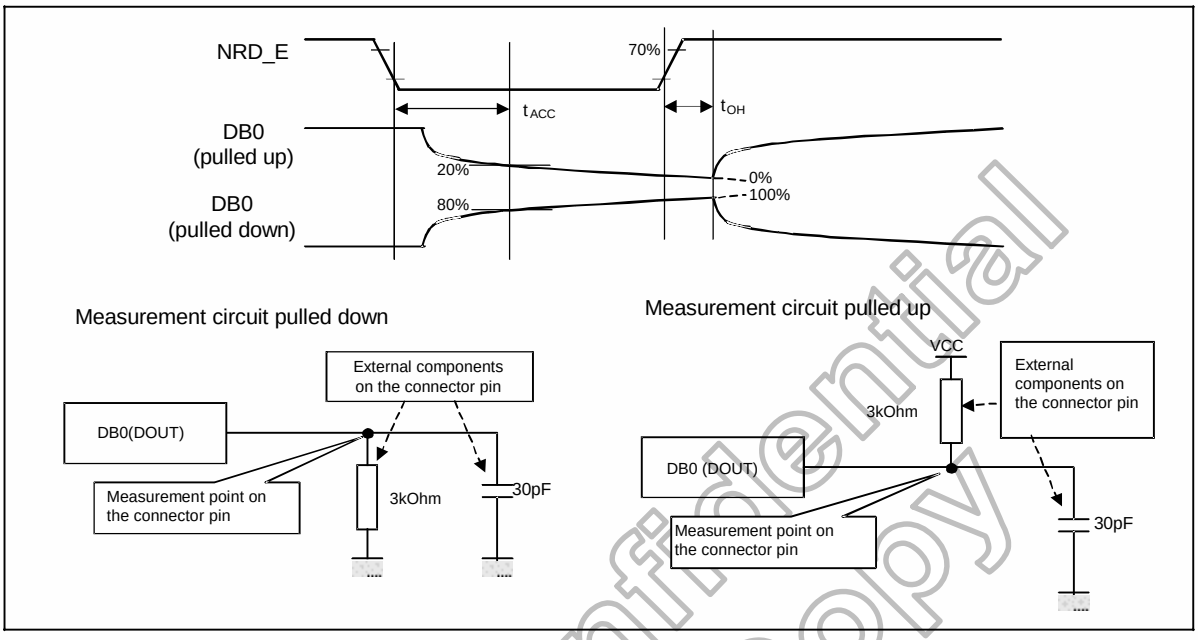



**Figure 7. 11**

# 8. Reference Application

## 8.1 Example Connection with Panel

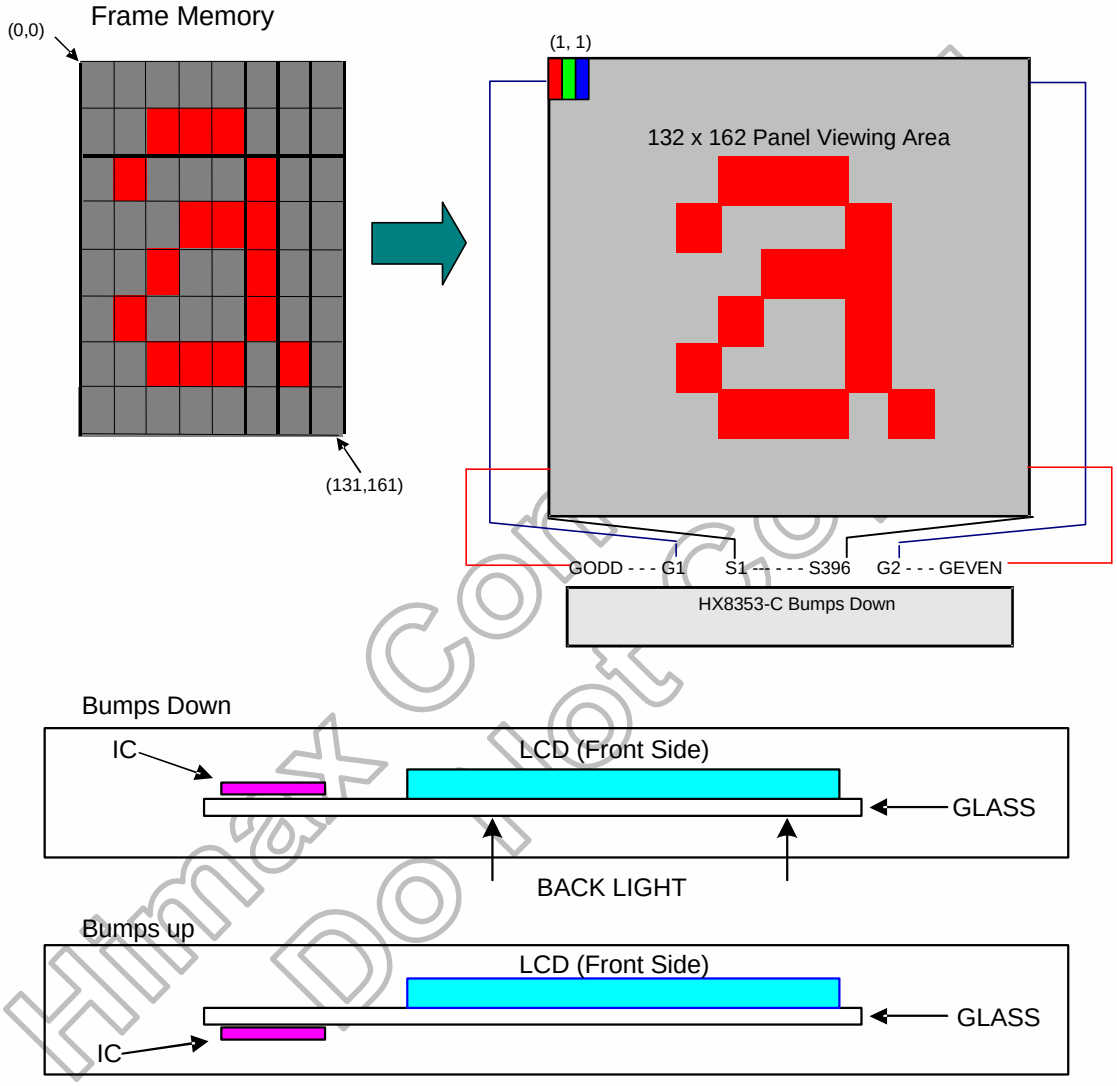
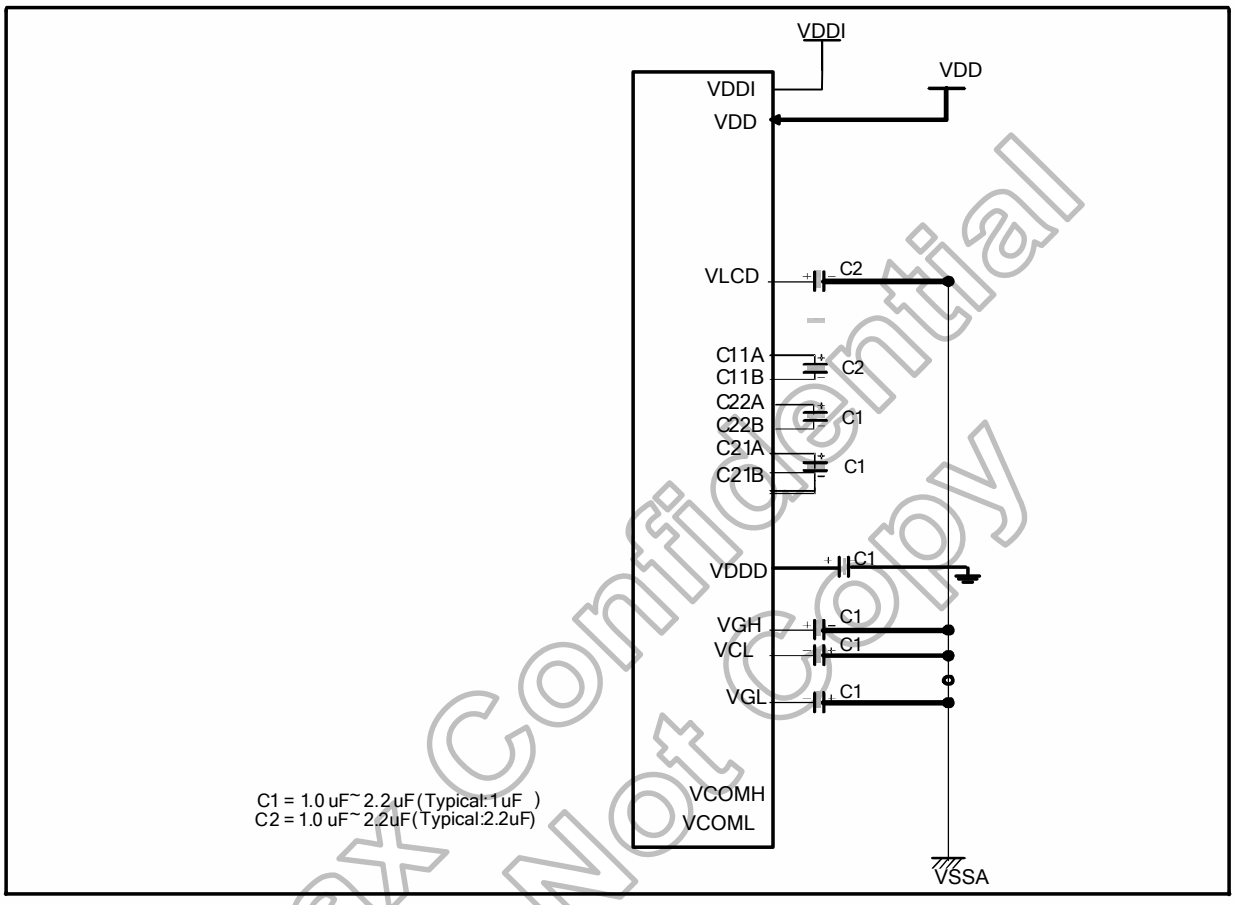



**Figure 8. 1**

## 8.2 Connection Example with External Components




**Note1: C22 option : VGH and VGL can share the same pump capacitor when operate on special pumping condition → VGH<4xVDD, VGL>-3xVDD (On this condition, C22 can be removed).**
**Note2: If need to remove capacitor of VDDD connection : when VDDI = 1.65~1.95v, VDDD can connect to VDDI on FPC directly**

**Figure 8. 2 Example connection with external components**

## 8.3 External Components

| Pad Name | Connection | Typical capacitance value |
|---|---|---|
| VGL | Connect to Capacitor (Max 16V): VGL ---(-)----\| \|--- (+)----- VSSA | 1.0µF |
| VCL | Connect to Capacitor (Max 5V): VCL ---(-)----\| \|--- (+)----- VSSA | 1.0µF |
| VDDD | Connect to Capacitor (Max 5V): VDDD ---(+)----\| \|--- (-)----- VSSA | 1.0µF |
| VGH | Connect to Capacitor (Max 21V): VGH ---(+)----\| \|--- (-)----- VSSA | 1.0µF |
| C21A, C21B | Connect to Capacitor (Max 7V): C21A ---(+)----\| \|--- (-)-----C21B | 1.0µF |
| C22A, C22B | Connect to Capacitor (Max 7V): C22A,---(+)----\| \|--- (-)----C22B | 1.0µF |
| C11A, C11B | Connect to Capacitor (Max 5V): C11A ---(+)----\| \|--- (-)-----C11B | 2.2µF |
| VLCD | Connect to Capacitor (Max 6V): VLCD ---(+)----\| \|--- (-)-----VSSA | 1.0µF |
| **VDD** | **VDD (Analogue Power)** | Optional |
| **VSSD** | **Connect to VSSD** | **-** |
| **VDDI** | **VDDI (Digital Power)** | Optional |
| **VSSD** | **VSSA (Ground)** | **-** |

**Table 8. 1 Example capacitor connection**

| Pins connection | Recommended voltage | Capacity |
|---|---|---|
| VDD, VDDI, VCL, C11A/B, VDDD | 6V | 1 µFor 2.2uF (B characteristics) |
| VLCD, C21A/B, C22A/B, | 10V | 1 µF |
| VGH, VGL | 25V | 1 µF |

**Table 8. 2 Adoptability of Capacitor**

| Reusable | Pins to connect |
|---|---|
| > 200 kΩ | VcomR |

**Table 8. 3 Adoptability of Variable resistor**

# 9. Layout Recommedacation

TBD

# 10. Ordering Information

| Part No. | Package |
|---|---|
| HX8353-C000PDxxx | TBD. |

# 11. Revision History

| Version | Date | Description of Changes |
|---|---|---|
| 01 | 2008/02/25 | New setup |
| | 2008/4/17 | 1. Modify the 8.2 Connection Example with External Components (page 231)<br>2. Modify the 7.3 Maximum Series Resistance (page 219)<br>3. Mody the setting of VC1[2:0] and BT[3:0] (page 171 and page 172) |
| | 2008/4/21 | 1. Modify the 7.3 Maximum Series Resistance (page 219)<br>2. Add the voltage range of VCOMH, VCOML (page10) |
| | 2008/4/22 | 1. Modify the 4.5 Bump arrangement (page 22)<br>2. Modify the seal-ing =15um * 2 (page 16) |
| | 2008/4/25 | 1. Modify the Pin Coordinate,add description of input and output pin (page 18~21)<br>2. Modify the Bump arrangement,add pin number of input and output pin (page 23) |
| | 2008/4/29 | 1. Modify Fig.5.53 BT[2:0] to BT[3:0] (page 85)<br>2. Modify table5.33 Master clock Frequency 10M to 1.5M (page 113)<br>3. Modify B2H(ISC) $f_{FLM}$ =70Hz to $f_{FLM}$ =60Hz (page 176)<br>4. Modify B4H(RTN,clock cycles perline) (page 179)<br>5. Modify address and resolution unmatch<br>5.3.1 SA,ML=1(page 52)<br>5.3.2 SA,RA(page 53)<br>5.3.6 SA,RA(page 57)<br>5.3.7 SA,RA(page 58)<br>6. Modify Alignment mark A1 and A2 (page17,page21)<br>7. Modify table 6.2 E7 and 6.4.29 E7 parameter (page 121, page206) |
| | 2008/4/30 | 1. Add description of input PIN (page 13 ,page 14)<br>2. Add description of BURN (page15) |
| | 2008/5/07 | 1. Modify VRH[3:0] setting (page 171, page 172)<br>2. Modify “Serial interface”(5.12) , when SPI_SEL pin high is 4 wire (page 40)<br>3. Modify Fig5.55 (page 86)<br>4. Modify Fig5.57 gamma stream,Table5.22, Table 5.23 and Table5.24 (page 90, page91)<br>5. Add 2nd parametet of C6h(page118, page196)<br>6. Modify register of B2h and E2h (page 175, page 201)<br>7. Remove bit5 function in B5h,E5h(page 181,page 204)<br>8. Remove E8h and F5h(page 199) |

| | | |
|---|---|---|
| | | 9. Modify parameter4 of E0h<br>10. Modify table6.2 (page117~page122) |
| | 2008/5/16 | 1. Modify 8.1Example Connection with Panel(page 228)<br>2. Modify “Voltage Calculation Formula”, SumRP(SumRN)=124+….(page 92) |
| | 2008/5/20 | 1. Modify “Page top” 132RGBx162 dot |
| | 2008/5/21 | 1. 5.18 OTP Programming, in note2 ”,…. NAVILD bit will be changed to 1 “ (page 106)<br>2. Programming seruence step9,modify “Specify OTP_index” read and write (page 109)<br>3. Modify B9H and BAH flow chart (page 186 and page187) |
| | 2008/6/16 | 1. Feature,Page4 VDDI and VDD change<br>2. Modify bit number of RADJ in B0H/E0H ,page168 |
| | 2008/6/18 | 1. Modify the formula of VGH ,in B1H ,page170<br>2. B9H passward set is (04,17) ,page 185 |
| | 2008/7/03 | 1. Pin Description DB0~DB17 (page 16)<br>2. Pin description VDDB1 updata VDDI (page 13) |
| | 2008/7/10 | 1. REV_PANEL define (page 14)<br>0→ for normal white panel<br>1→ for normal black panel |
| | 2008/7/15 | 1. Modify VREG1OUT description (page 15)<br>2. Add description of DIV_E ,only use in idle mode (page 178) |
| | 2008/7/24 | 1.Modify 5.10.1 LCD Power Generation Scheme (page 84) |