



DATA SHEET

(DOC No. HX8353-E-DS)

HX8353-E

132RGB x 162 dots, 262K color,
with Internal GRAM,
TFT Mobile Single Chip Driver
Version 0.1 April, 2012

List of Contents

April, 2012

1. General Description	5
2. Features.....	6
3. Block Diagram	8
4. Pin Description	9
4.1 Pin description	9
4.2 Pin assignment	13
4.3 PAD coordinates	14
4.4 Alignment mark.....	17
4.5 Bump size	18
5. Interface.....	19
5.1 System interface.....	19
5.1.1 Parallel bus system interface.....	20
5.1.2 MCU data color coding	27
5.1.3 Serial Interface	36
5.1.4 Display module data transfer recovery.....	40
5.1.5 Display module data transfer pause	41
5.1.6 Display module data transfer modes	42
5.2 Color depth conversion.....	43
6. Display Data GRAM	47
6.1 Display data GRAM mapping	47
6.2 Address counter (AC) of GRAM	47
6.2.1 System interface to GRAM write direction.....	48
6.3 Source, gate and memory map	53
6.3.1 When using 132 x 162 GRAM resolution, display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0).....	53
6.3.2 When using 132 x 162 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b000 & STE_SEL=1).....	54
6.3.3 When using 128 x 128 GRAM resolution, display resolution 128RGB x 128 (RSO[2:0]=3'b001)	55
6.3.4 When using 120 x 160 GRAM resolution, display resolution 120RGB x 160 (RSO[2:0]=3'b010).....	56
6.3.5 When using 128 x 160 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b011)	57
6.3.6 When using 96 x 68 GRAM resolution, display resolution 96RGB x 68 (RSO[2:0]=3'b100).....	58
6.3.7 When using 96 x 64 GRAM resolution, display resolution 96RGB x 64 (RSO[2:0]=3'b101).....	59
6.3.8 Normal display on or partial display on	60
6.4 Vertical scrolling display	74
7. Functional Description	76
7.1 Internal Oscillator.....	76
7.2 Gamma characteristic correction function	77
7.2.1 Structure of grayscale voltage generator.....	78
7.2.2 Gamma-characteristics adjustment register.....	79
7.2.3 Gamma resister stream and 8 to 1 selector	80
7.2.4 Variable resister	83
7.3 Tearing effect output line	89
7.3.1 Tearing effect line modes.....	89
7.3.2 Tearing effect line timing.....	91
7.3.3 Example 1: MPU write is faster than panel read	92
7.3.4 Example 2: MPU write is slower than panel read.....	93
7.4 Scan Mode Setting	93
7.5 LCD power generation circuit	94
7.5.1 Power supply circuit.....	94
7.5.2 LCD power generation scheme.....	95
7.6 Power function	96



7.6.1	Power on/off sequence	96
7.6.2	Power levels definition	99
7.6.3	Deep standby mode set up flow	100
7.7	Sleep out – command and self-diagnostic functions of display module	101
7.7.1	Register loading detection	101
7.7.2	Functionality detection	102
7.8	Input / output pin state	103
7.8.1	Output pins	103
7.8.2	Input pins	103
8.	Command Set	104
8.1	Command set list	104
8.2	Command description	109
8.2.1	NOP	109
8.2.2	Software reset (01h)	110
8.2.3	Read display identification information (04h)	111
8.2.4	Read display status (09h)	112
8.2.5	Read display power mode (0Ah)	115
8.2.6	Read display MADCTL (0Bh)	117
8.2.7	Read display pixel format (0Ch)	119
8.2.8	Read display image mode (0Dh)	121
8.2.9	Read display signal mode (0Eh)	123
8.2.10	Read display self-diagnostic result (0Fh)	124
8.2.11	Sleep in (10h)	125
8.2.12	Sleep out (11h)	126
8.2.13	Partial mode on (12h)	128
8.2.14	Normal display mode on (13h)	129
8.2.15	Display inversion off (20h)	130
8.2.16	Display inversion on (21h)	131
8.2.17	Gamma set (26h)	132
8.2.18	Display off (28h)	133
8.2.19	Display on (29h)	134
8.2.20	Column address set (2Ah)	135
8.2.21	Page address set (2Bh)	137
8.2.22	Memory write (2Ch)	139
8.2.23	Color set (2Dh)	140
8.2.24	Memory read (2Eh)	141
8.2.25	Partial area (30h)	142
8.2.26	Vertical scrolling definition (33h)	144
8.2.27	Tearing effect line off (34h)	147
8.2.28	Tearing effect line on (35h)	148
8.2.29	Memory access control (36h)	149
8.2.30	Vertical scrolling start address (37h)	151
8.2.31	Idle mode off (38h)	152
8.2.32	Idle mode on (39h)	153
8.2.33	Interface pixel format (3Ah)	154
8.2.34	Read ID1 (DAh)	155
8.2.35	Read ID2 (DBh)	156
8.2.36	Read ID3 (DCh)	157
8.2.37	SETOSC: set internal oscillator (B0h)	158
8.2.38	SETPOWER: set power (B1h)	159
8.2.39	SETDISPLAY: set display related register (B2h)	162
8.2.40	SETCYC: set display cycle register (B4h)	164
8.2.41	SETBGP: set internal reference voltage register (B5h)	167
8.2.42	SETCOM: set VCOM voltage related register (B6h)	169
8.2.43	SETEXTC: enable extension command (B9h)	170



Himax Technologies, Inc.
<http://www.himax.com.tw>

8.2.44	SETOTP: set OTP setting (BBh)	171
8.2.45	SETSTBA: set Source option related register (C0h)	172
8.2.46	SETTID: set ID (C3h)	175
8.2.47	SETPANEL: set panel characteristic (CCh)	176
8.2.48	GETHID: Read Himax Internal ID (D0h)	177
8.2.49	SETGAMMA: set gamma curve (E0h)	178
8.2.50	SET SPI READ: Set SPI read address (FEh)	179
8.2.51	GET SPI READ: Get SPI read address (FFh)	180
9.	Layout Recommendation	181
10.	OTP Programming	183
10.1	Programming flow (Internal OTP power programming sequence)	185
10.2	Programming flow (External OTP power programming sequence)	186
11.	Electrical Characteristic	187
11.1	Absolute maximum ratings	187
11.2	ESD protection level	187
11.3	DC characteristics	188
11.3.1	Current consumption	189
11.4	AC characteristics	190
11.4.1	Parallel interface characteristics (8080-series MPU)	190
11.4.2	Serial interface characteristics	192
11.4.3	Reset input timing	193
11.5	tACC, tOH Measurement Condition	194
11.6	1 st Pixel is at right-bottom of the panel & RGB filter order = RGB	196
11.7	1 st Pixel is at left-top of the panel & RGB filter order = BGR	197
11.8	Application of connection with Different resolution	198
12.	Ordering Information	212
13.	Revision History	212

>> **HX8353-E**

132RGB x 162 dot, 262K Color, with Internal GRAM, TFT Mobile Single Chip Driver



Himax Technologies, Inc.
<http://www.himax.com.tw>

Preliminary Version 0.1

April, 2012

1. General Description

This manual describes the Himax's HX8353-E 132RGB*162 dots resolution driving controller. The HX8353-E is designed to provide a single-chip solution that combined a gate driver, a source driver, **power supply circuit**, and internal graphics RAM for **262,144 colors** to drive a TFT panel with 132RGB*162 dots at maximum.

The HX8353-E can be operated in low-voltage condition to the interface and integrated internal boosters that produce the liquid crystal voltage, **breeder resistance** and the voltage follower circuit for liquid crystal driver. In addition, The HX8353-E also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8353-E is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

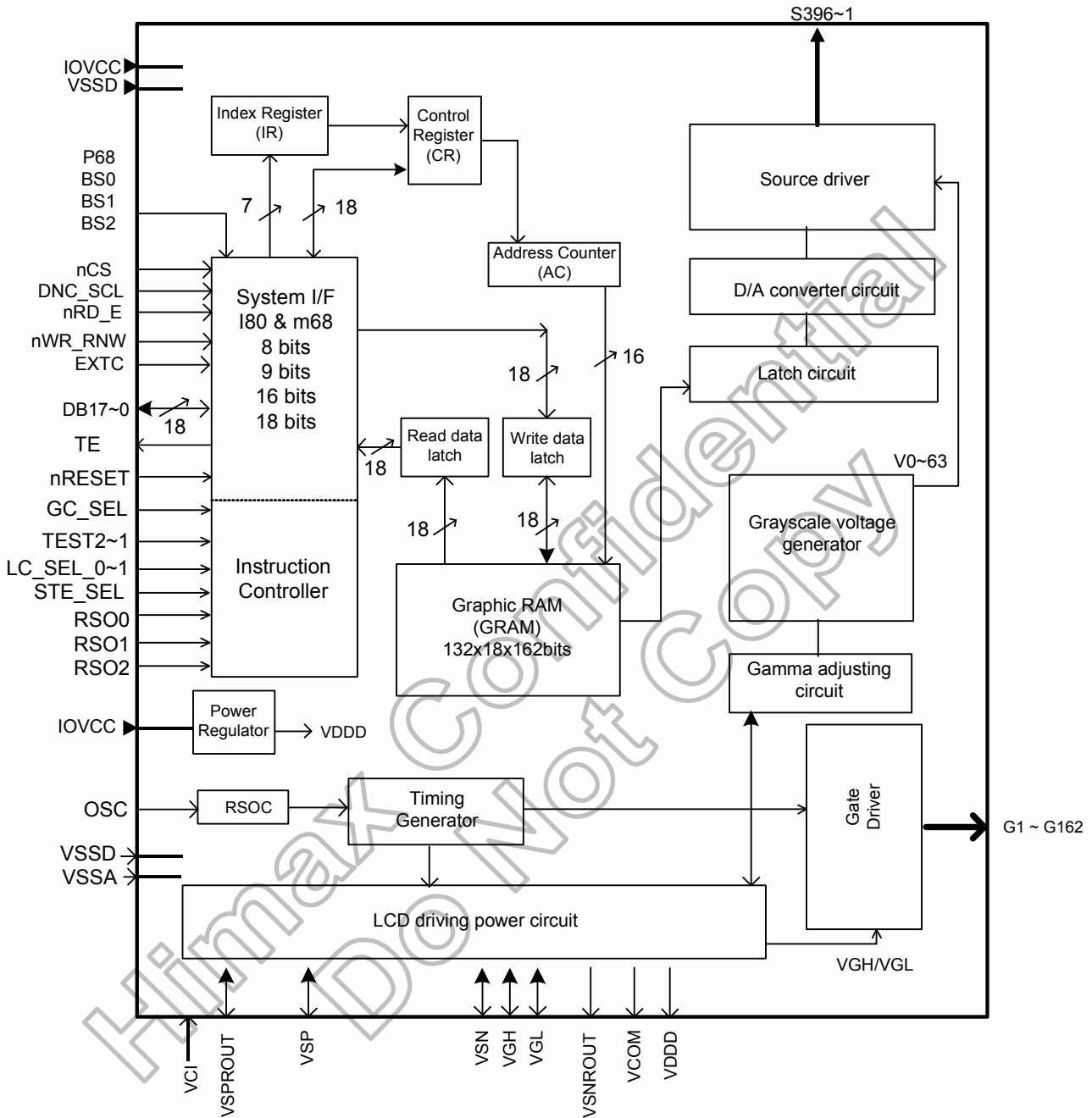
Himax Confidential
Do Not Copy

2. Features

- Single chip solution to drive a TFT panel
- 132RGB x 162-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support resolution:
 - 132RGB x 162-dot: Display with 132 x 18-bits x 162 display RAM
 - 128RGB x 160-dot
 - Type 1: Display with 128 x 18-bits x 160 display RAM
 - Type 2: Display with 132 x 18-bits x 162 display RAM
 - 128RGB x 128-dot
 - 120RGB x 160-dot
 - 96RGB x 68-dot: Display with 96 x 18-bits x 68 display RAM
 - 96RGB x 64-dot
- Internal operation circuit of liquid crystal display:
 - Source channel: 396ch (132RGB)
 - Gate line: 162 Gate output
- Display mode (Color modes):
 - Full colors
 - 262k colors (18bit 6(R):6(G):6(B))
 - Reduce color mode:
 - 65k colors (16bit 5(R):6(G):5(B))
 - 4k colors (12bit 4(R):4(G):4(B))
 - 8 colors (Idle mode on): 8 colors (3 bit binary mode)
- Internal graphics RAM capacity: 132 x 162 x 18-bit = 0.38M bit:
- Support interface mode:
 - I80 System interface: 8-/9-/16-/18-bits bus
 - M68 System interface: 8-/9-/16- /18-bits bus
 - 3-/4- Wires Serial Data Transfer Interface
- Display features
 - Area scrolling
 - Partial display mode
 - Software programmable color depth mode
- On chip features:
 - DC/DC converter
 - OTP to store initialization register setting and MTP (Multi-time-programming)

- non-volatile memory to store for VCOM setting
- Oscillator for display clock generation
 - 1-dot/2-dot/4-dot inversion, column inversion
 - Support default value for factory use
 - Low-power consumption architecture supports:
 - Logic supply voltage range for IOVCC to VSSD: 1.65 to 3.3V
 - Analog supply voltage range for VCI to VSSA: 2.5 to 3.3V
 - Output voltage range:
 - VSP = 5.0V (VCI=2.8V) for dual pump (Power supply for driver circuit range)
 - VSN = -5.0 V for dual pump (Power supply for driver circuit range)
 - VSPROUT =3.3V to 4.6V (Positive Source output voltage range)
 - VSNROUT = -3.3V to -4.6V (Negative Source output voltage range)
 - VGH = +9.0 to +15V (Positive Gate output voltage range)
 - VGL = -6.0 to -12.5V (Negative Gate output voltage range)
 - VCOM=-2.5V to 0V
 - Low power consumption, suitable for battery operated systems
 - Suitable for all brand LCM module
 - Command set:
 - 128RGB x 160-dot
 - 132RGB x 162-dot
 - 120RGB x 160-dot
 - 96RGB x 68-dot
 - 96RGB x 64-dot
 - Himax defined command set
 - CMOS compatible inputs
 - Optimized layout for COG assembly
 - Temperature range: -30°C ~ 80°C

3. Block Diagram



4. Pin Description

4.1 Pin description

				Input Part					
Signals	I/O	Pin Number	Connected with	Description					
P68, BS2,BS1,BS0	I	4	VSSD/IOVCC	Select the MPU interface mode as listed below					
				P68	BS2	BS1	BS0	Interface mode	DB pins
				0	1	0	0	8-bit bus interface, 80-system	DB17-DB8:Unused DB7-DB0: Data
				0	1	0	1	16-bit bus interface, 80-system	DB17-DB16:Unused DB15-DB0: Data
				0	1	1	0	9-bit bus interface, 80-system	DB17-DB9:Unused DB8-DB0: Data
				0	1	1	1	18-bit bus interface, 80-system	DB17-DB0: Data
				1	1	0	0	8-bit bus interface, 68-system	DB17-DB8:Unused DB7-DB0: Data
				1	1	0	1	16-bit bus interface, 68-system	DB17-DB16:Unused DB15-DB0: Data
				1	1	1	0	9-bit bus interface, 68-system	DB17-DB9:Unused DB8-DB0: Data
				1	1	1	1	18-bit bus interface, 68-system	DB17-DB0: Data
X	0	X	X	3-/4- wire serial interface	DB17-DB0:Unused SDA: Data input/output				
Must be connected to VSSD or IOVCC.									
SPI_SEL	I	1	VSSD/IOVCC	Interface format select pin					
				SPI_SEL	Serial Interface Format Selection				
				0	3-wire serial interface (default)				
1	4-wire serial interface								
If not used, connect it to VSSD.									
NCS	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.					
DNC_SCL	I	1	MPU	The signal for command or parameter select under parallel mode(i.e. Not serial interface): Low: command. High: parameter. When under serial interface, it servers as SCL.					
NRD_E	I	1	MPU	I80 system: Serves as a read signal and read data at the low level. M68 system: 0: Read/Write disable, 1: Read/Write enable. If not used, connected to IOVCC.					
NWR_RNW	I	1	MPU	I80 system: Serves as a write signal and writes data at the rising edge. M68 system: 0: Write, 1: Read. 4-wire SPI interface: 0: Command, 1: Data. If not used, connected to IOVCC.					
EXTC	I	1	VSSD/IOVCC	Extended command set enable. Low (VSSD): extended command set is discarded High (IOVCC): extended command set is accepted If not used, let it open or connected to VSSD.(weak pull low)					
STE_SEL	I	1	VSSD/IOVCC	This Pin is only valid for RSO[2:0]=3'b000. Low (VSSD): Scrolling function enable and TE lines (162 lines) High (IOVCC): Scrolling function disable and TE lines (160 lines) Must be connected to VSSD or IOVCC.					
GC_SEL	I	1	VSSD/IOVCC	This signal is used to select gamma curve order. Low (VSSD): GC0(1.0), GC1(2.5), GC2(2.2), GC3(1.8) High (IOVCC): GC0(2.2), GC1(1.8), GC2(2.5), GC3(1.0) Must be connected to VSSD or IOVCC.					

Input Part																																								
Signals	I/O	Pin Number	Connected with	Description																																				
RSO0~2	I	3	VSSD/ IOVCC	Resolution selection pins. RSO[2:0] is used for selecting resolution. Must be connected to VSSD or IOVCC.																																				
				<table border="1"> <thead> <tr> <th>RSO2</th> <th>RSO1</th> <th>RSO0</th> <th>Resolution</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>GRAM resolution (Size): 132RGBx162 Display resolution: Type1 :132RGBx162 (S1~S396 and G1~G162) Type2 :128RGBx160 (S7~S390 and G2~G161)</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>GRAM resolution (Size): 128RGBx128 Display resolution: 128RGBx128 (S7~S390 and G2~G129)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>GRAM resolution (Size): 120RGBx160 Display resolution: 120RGBx160 (S7~S366, G2~G161)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>GRAM resolution (Size): 128RGBx160 Display resolution: 128RGBx160 (S7~S390 and G2~G161)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>GRAM resolution: 96RGBx68 Display resolution: 96RGBx68 (S55~S342, G1~G68)</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>GRAM resolution: 96RGBx64 Display resolution: 96RGBx64 (S55~S342, G1~G64)</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Setting disable</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Setting disable</td> </tr> </tbody> </table>	RSO2	RSO1	RSO0	Resolution	0	0	0	GRAM resolution (Size): 132RGBx162 Display resolution: Type1 :132RGBx162 (S1~S396 and G1~G162) Type2 :128RGBx160 (S7~S390 and G2~G161)	0	0	1	GRAM resolution (Size): 128RGBx128 Display resolution: 128RGBx128 (S7~S390 and G2~G129)	0	1	0	GRAM resolution (Size): 120RGBx160 Display resolution: 120RGBx160 (S7~S366, G2~G161)	0	1	1	GRAM resolution (Size): 128RGBx160 Display resolution: 128RGBx160 (S7~S390 and G2~G161)	1	0	0	GRAM resolution: 96RGBx68 Display resolution: 96RGBx68 (S55~S342, G1~G68)	1	0	1	GRAM resolution: 96RGBx64 Display resolution: 96RGBx64 (S55~S342, G1~G64)	1	1	0	Setting disable	1	1	1	Setting disable
				RSO2	RSO1	RSO0	Resolution																																	
				0	0	0	GRAM resolution (Size): 132RGBx162 Display resolution: Type1 :132RGBx162 (S1~S396 and G1~G162) Type2 :128RGBx160 (S7~S390 and G2~G161)																																	
				0	0	1	GRAM resolution (Size): 128RGBx128 Display resolution: 128RGBx128 (S7~S390 and G2~G129)																																	
				0	1	0	GRAM resolution (Size): 120RGBx160 Display resolution: 120RGBx160 (S7~S366, G2~G161)																																	
				0	1	1	GRAM resolution (Size): 128RGBx160 Display resolution: 128RGBx160 (S7~S390 and G2~G161)																																	
				1	0	0	GRAM resolution: 96RGBx68 Display resolution: 96RGBx68 (S55~S342, G1~G68)																																	
				1	0	1	GRAM resolution: 96RGBx64 Display resolution: 96RGBx64 (S55~S342, G1~G64)																																	
1	1	0	Setting disable																																					
1	1	1	Setting disable																																					
NRESET	I	1	MPU or reset circuit	Reset pin. Setting this pin-low initializes the LSI. Must be reset after power is supplied.																																				
SS_PANEL	I	1	VSSD/ IOVCC	Input pin to select the source driver scan direction on panel module. Must be connected to VSSD or IOVCC.																																				
				<table border="1"> <thead> <tr> <th rowspan="2">SS_PANEL</th> <th colspan="4">Module source output direction</th> </tr> <tr> <th>RSO[2:0] =3'b100, 3'b101</th> <th>RSO[2:0] =3'b010</th> <th>RSO[2:0] =3'b000 (type2), 3'b001, 3'b011</th> <th>RSO[2:0] =3'b000 (type1)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>S55 -> S342</td> <td>S7 -> S366</td> <td>S7 -> S390</td> <td>S1 -> S396</td> </tr> <tr> <td>1</td> <td>S342 -> S55</td> <td>S366 -> S7</td> <td>S390 -> S7</td> <td>S396 -> S1</td> </tr> </tbody> </table>	SS_PANEL	Module source output direction				RSO[2:0] =3'b100, 3'b101	RSO[2:0] =3'b010	RSO[2:0] =3'b000 (type2), 3'b001, 3'b011	RSO[2:0] =3'b000 (type1)	0	S55 -> S342	S7 -> S366	S7 -> S390	S1 -> S396	1	S342 -> S55	S366 -> S7	S390 -> S7	S396 -> S1																	
				SS_PANEL		Module source output direction																																		
RSO[2:0] =3'b100, 3'b101	RSO[2:0] =3'b010	RSO[2:0] =3'b000 (type2), 3'b001, 3'b011	RSO[2:0] =3'b000 (type1)																																					
0	S55 -> S342	S7 -> S366	S7 -> S390	S1 -> S396																																				
1	S342 -> S55	S366 -> S7	S390 -> S7	S396 -> S1																																				
GS_PANEL	I	1	VSSD/ IOVCC	Input pin to select the Gate driver scan direction on panel module. Must be connected to VSSD or IOVCC.																																				
REV_PANEL	I	1	VSSD/ IOVCC	Input pin to select the display reversion . Must be connected to VSSD or IOVCC.																																				
				<table border="1"> <thead> <tr> <th>REV_PANEL</th> <th>Mapping data</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>"0" to maximum pixel voltage for normal white panel</td> </tr> <tr> <td>1</td> <td>"0" to minimum pixel voltage for normal black panel</td> </tr> </tbody> </table>	REV_PANEL	Mapping data	0	"0" to maximum pixel voltage for normal white panel	1	"0" to minimum pixel voltage for normal black panel																														
				REV_PANEL	Mapping data																																			
0	"0" to maximum pixel voltage for normal white panel																																							
1	"0" to minimum pixel voltage for normal black panel																																							

Input Part					
Signals	I/O	Pin Number	Connected with	Description	
BGR_PANEL	I	1	VSSD/ IOVCC	Input pin to select the color mapping . Must be connected to VSSD or IOVCC.	
				BGR_PANEL	Color mapping
				0	S1 · S2 · S3 filter order = R → G → B
		1		S1 · S2 · S3 filter order = B → G → R	
TEST2~1	I	2	VSSD	Test pins. Let it open or connected to VSSD. (Internal pull low)	
OSC	I	1	Open or Connect to VSSD	Oscillator input for test purpose. If not used, please let it open.	

Output Part				
Signals	I/O	Pin Number	Connected with	Description
S1~396	O	396	LCD	Output voltages applied to the liquid crystal. SS=0, ram address "0000" is output from S1. SS=1, ram address "0000" is output from S396. S1,S2,S3 = 'R', 'G', 'B' (SS=0, BGR=0).
G1~162	O	162	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM	O	3	TFT common electrode	The power supply of common voltage in TFT driving. Connect this pin to the common electrode in TFT panel.
VSPROUT	O	3	Open	Positive gamma reference voltage.
VSNROUT	O	3	Open	Negative gamma reference voltage.
VSP	O	5	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and VSP.
VSN	O	3	Stabilizing capacitor	An output from the step-up circuit3. Connect to a stabilizing capacitor between VSSA and VSN.
VGH	O	3	Open	A positive power output from the step-up circuit 2 for the gate line drive circuit.
VGL	O	3	Open	A positive power output from the step-up circuit 2 for the gate line drive circuit.
TE	O	1	MPU or open	A frame start pulse output (amplitude: IOVCC-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it
VTESTOUT NVTESTOUT	O	2	Open	A test pin. Disconnect it.
VDDD	O	3	Open	Output for internal logic voltage. Let it open.
VBGP	O	3	Open	Reference voltage for power circuit. Let it open.
TS7~0	O	8	Open	Test pins. Let these pins open.

Input/Output Part				
Signals	I/O	Pin Number	Connected with	Description
DB0_SDA DB1~17	I/O	18	MPU	When Operates in system interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 For serial interface, this pin (SDA) is for serial data pin when operate on serial data transfer interface mode of Command-parameter Interface mode. Data would be latched on the rising edge of the SCL signal. Let unused data pins open or pulled Gnd or pulled IOVCC.
DUMMY_C1 DUMMY_C2	I/O	8,18	Open	Dummy pads. Disconnect them.
DUMMY1 ~ 25	-	25	Open	Dummy pads. Disconnect them.
DUMMYR1~R2	-	2	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.
LC_SEL1~0	-	2	-	Dummy pin, let it open or pull up/down.

Power Part				
Signals	I/O	Pin Number	Connected with	Description
IOVCC	P	17	Power supply	Power supply for interface pin. IOVCC = 1.65 ~3.3 V.
VSSD	P	17	Power supply	Ground for the logic side. VSSD = 0V
VSSA	P	9	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VCI	P	6	Power supply	A power supply for the analog circuit. VCI = 2.5 ~ 3.3V

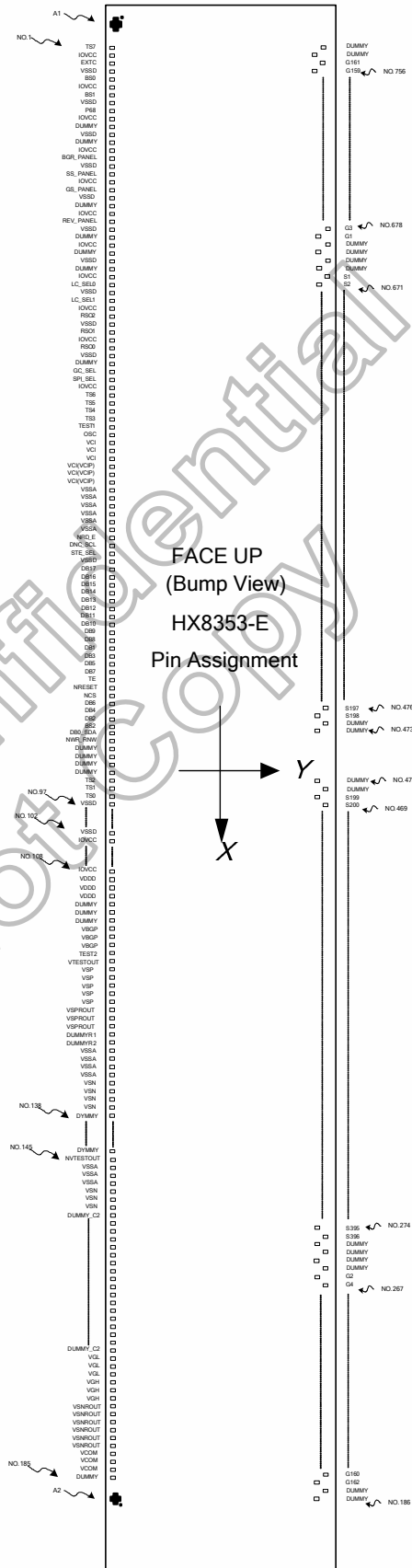
4.2 Pin assignment

Chip size : 10100um x 655um
 (Include Seal-ring and Scribe line)

Chip thickness : 250um(typ.)/350um
 Pad coordinate : PAD center
 Coordinate Origin : Chip Center
 Au Bump Size
 Bump height tolerance +/- 3um
 Bump size tolerance :

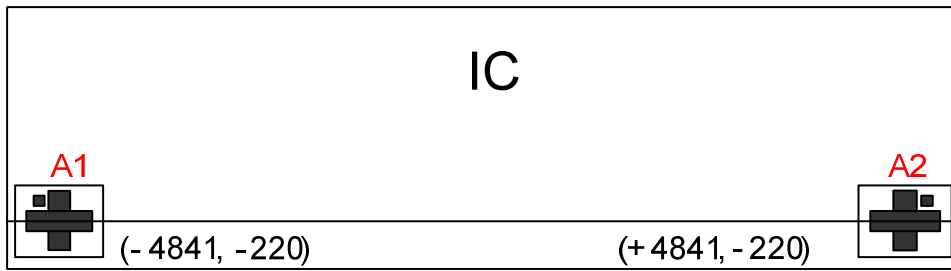
Output bump width : 16 +/- 2um
 Output bump length : 98 +/- 3um
 Input bump width : 35/40 +/- 3um
 Input bump length : 90 +/- 3um

Numbers in the figure corresponds to pad coordinate numbers
 Alignment Mark
 Arrangement : Two places
 A1 : Coordinate(X,Y)=(-4841,-220)
 A2 : Coordinate(X,Y)=(4841,-220)

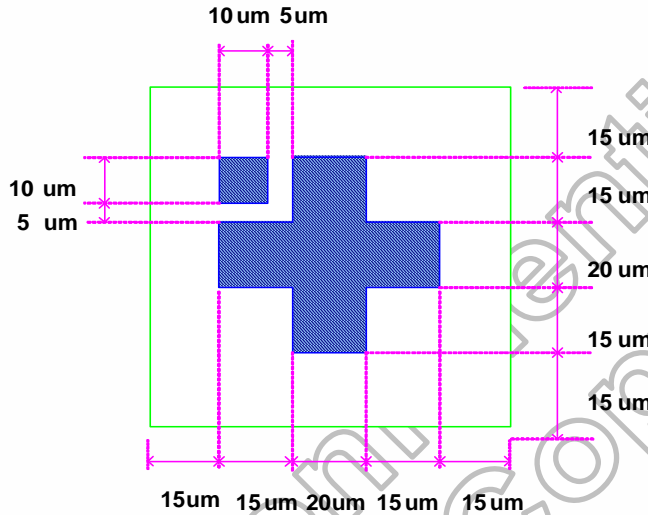


No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y		
561	S112	-1604	110	621	S52	-2564	110	681	G9	-3524	110	741	G129	-4484	110		
562	S111	-1620	227	622	S51	-2580	227	682	G11	-3540	227	742	G131	-4500	227		
563	S110	-1636	110	623	S50	-2596	110	683	G13	-3556	110	743	G133	-4516	110		
564	S109	-1652	227	624	S49	-2612	227	684	G15	-3572	227	744	G135	-4532	227		
565	S108	-1668	110	625	S48	-2628	110	685	G17	-3588	110	745	G137	-4548	110		
566	S107	-1684	227	626	S47	-2644	227	686	G19	-3604	227	746	G139	-4564	227		
567	S106	-1700	110	627	S46	-2660	110	687	G21	-3620	110	747	G141	-4580	110		
568	S105	-1716	227	628	S45	-2676	227	688	G23	-3636	227	748	G143	-4596	227		
569	S104	-1732	110	629	S44	-2692	110	689	G25	-3652	110	749	G145	-4612	110		
570	S103	-1748	227	630	S43	-2708	227	690	G27	-3668	227	750	G147	-4628	227		
571	S102	-1764	110	631	S42	-2724	110	691	G29	-3684	110	751	G149	-4644	110		
572	S101	-1780	227	632	S41	-2740	227	692	G31	-3700	227	752	G151	-4660	227		
573	S100	-1796	110	633	S40	-2756	110	693	G33	-3716	110	753	G153	-4676	110		
574	S99	-1812	227	634	S39	-2772	227	694	G35	-3732	227	754	G155	-4692	227		
575	S98	-1828	110	635	S38	-2788	110	695	G37	-3748	110	755	G157	-4708	110		
576	S97	-1844	227	636	S37	-2804	227	696	G39	-3764	227	756	G159	-4724	227		
577	S96	-1860	110	637	S36	-2820	110	697	G41	-3780	110	757	G161	-4740	110		
578	S95	-1876	227	638	S35	-2836	227	698	G43	-3796	227	758	DUMMY	-4756	227		
579	S94	-1892	110	639	S34	-2852	110	699	G45	-3812	110	759	DUMMY	-4772	110		
580	S93	-1908	227	640	S33	-2868	227	700	G47	-3828	227						
581	S92	-1924	110	641	S32	-2884	110	701	G49	-3844	110						
582	S91	-1940	227	642	S31	-2900	227	702	G51	-3860	227						
583	S90	-1956	110	643	S30	-2916	110	703	G53	-3876	110						
584	S89	-1972	227	644	S29	-2932	227	704	G55	-3892	227						
585	S88	-1988	110	645	S28	-2948	110	705	G57	-3908	110						
586	S87	-2004	227	646	S27	-2964	227	706	G59	-3924	227						
587	S86	-2020	110	647	S26	-2980	110	707	G61	-3940	110						
588	S85	-2036	227	648	S25	-2996	227	708	G63	-3956	227						
589	S84	-2052	110	649	S24	-3012	110	709	G65	-3972	110						
590	S83	-2068	227	650	S23	-3028	227	710	G67	-3988	227						
591	S82	-2084	110	651	S22	-3044	110	711	G69	-4004	110						
592	S81	-2100	227	652	S21	-3060	227	712	G71	-4020	227						
593	S80	-2116	110	653	S20	-3076	110	713	G73	-4036	110						
594	S79	-2132	227	654	S19	-3092	227	714	G75	-4052	227						
595	S78	-2148	110	655	S18	-3108	110	715	G77	-4068	110						
596	S77	-2164	227	656	S17	-3124	227	716	G79	-4084	227						
597	S76	-2180	110	657	S16	-3140	110	717	G81	-4100	110						
598	S75	-2196	227	658	S15	-3156	227	718	G83	-4116	227						
599	S74	-2212	110	659	S14	-3172	110	719	G85	-4132	110						
600	S73	-2228	227	660	S13	-3188	227	720	G87	-4148	227						
601	S72	-2244	110	661	S12	-3204	110	721	G89	-4164	110						
602	S71	-2260	227	662	S11	-3220	227	722	G91	-4180	227						
603	S70	-2276	110	663	S10	-3236	110	723	G93	-4196	110						
604	S69	-2292	227	664	S9	-3252	227	724	G95	-4212	227						
605	S68	-2308	110	665	S8	-3268	110	725	G97	-4228	110						
606	S67	-2324	227	666	S7	-3284	227	726	G99	-4244	227						
607	S66	-2340	110	667	S6	-3300	110	727	G101	-4260	110						
608	S65	-2356	227	668	S5	-3316	227	728	G103	-4276	227						
609	S64	-2372	110	669	S4	-3332	110	729	G105	-4292	110						
610	S63	-2388	227	670	S3	-3348	227	730	G107	-4308	227						
611	S62	-2404	110	671	S2	-3364	110	731	G109	-4324	110						
612	S61	-2420	227	672	S1	-3380	227	732	G111	-4340	227						
613	S60	-2436	110	673	DUMMY	-3396	110	733	G113	-4356	110						
614	S59	-2452	227	674	DUMMY	-3412	227	734	G115	-4372	227						
615	S58	-2468	110	675	DUMMY	-3428	110	735	G117	-4388	110						
616	S57	-2484	227	676	DUMMY	-3444	227	736	G119	-4404	227						
617	S56	-2500	110	677	G1	-3460	110	737	G121	-4420	110						
618	S55	-2516	227	678	G3	-3476	227	738	G123	-4436	227						
619	S54	-2532	110	679	G5	-3492	110	739	G125	-4452	110						
620	S53	-2548	227	680	G7	-3508	227	740	G127	-4468	227						
													Alignment mark			X	Y
													A1	-4841	-220		
													A2	4841	-220		

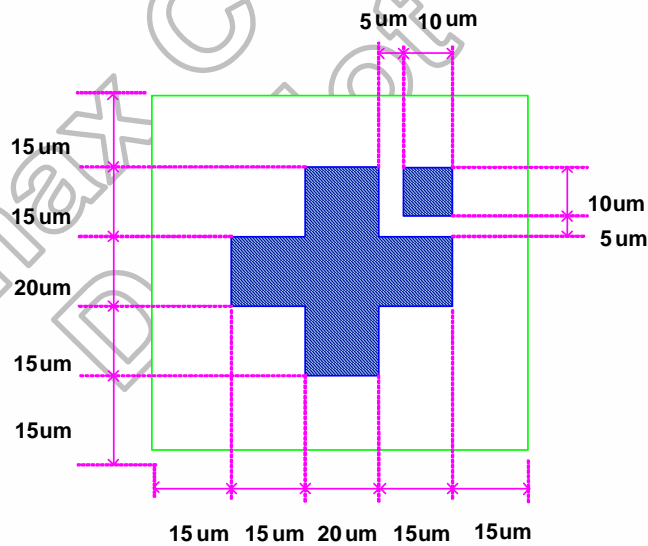
4.4 Alignment mark



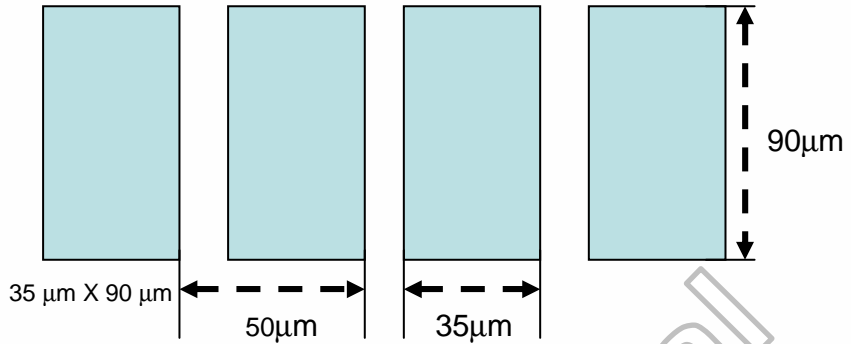
A_MARK (A1)



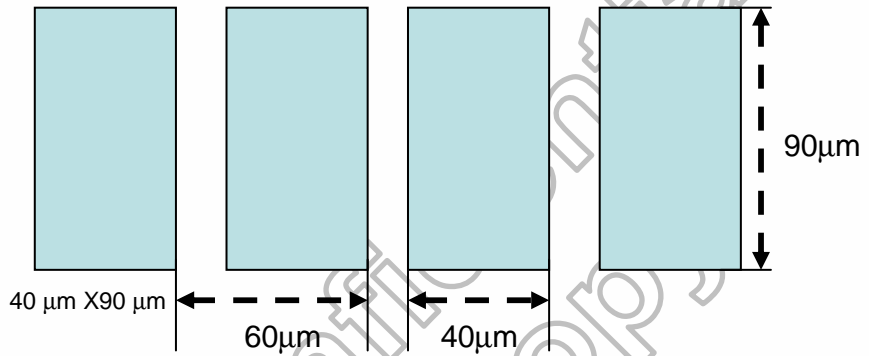
A_MARK (A2)



4.5 Bump size

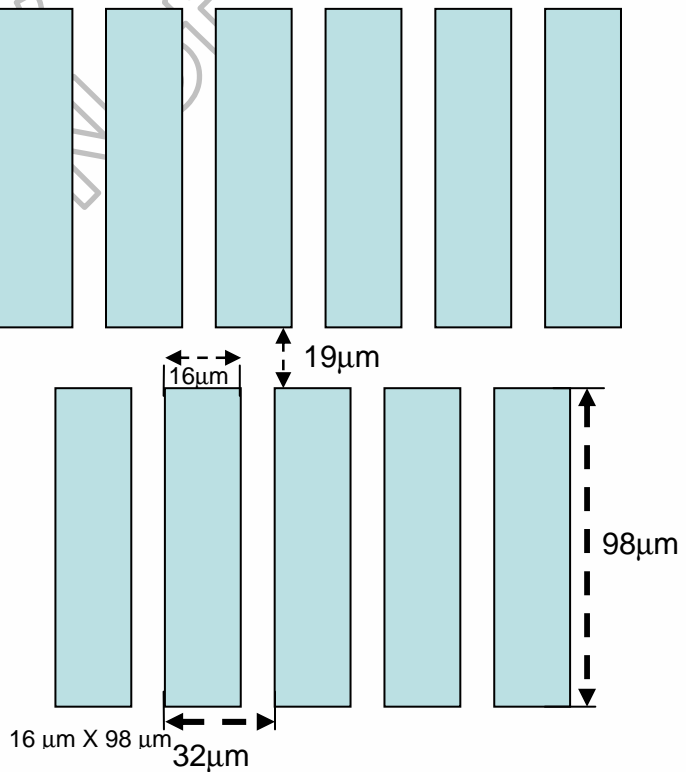


Input/Output PAD



Note: 35μmX90μm : Pad no. 1~62
 Pad no. 90~185
 40μmX90μm: Pad no. 63~89

Output PAD



Note: 16μmX98μm : Pad no.186~759

5. Interface

5.1 System interface

The HX8353-E supports parallel 80-system and 68-system 18-/16-/9-/8-bits bus interface mode and 3-/4- wires serial interface mode. When NCS = "L", the parallel and serial bus system interface of the HX8353-E become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS2-0. For selecting the format of input bus, please refer to Table 5.1 and Table 5.2.

The HX8353-E includes command code and the following parameter and GRAM data. The command code can be written through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

SPI_SEL	P68	BS2	BS1	BS0	Interface
x	0	1	0	0	80-system 8-bit Parallel
x	0	1	0	1	80-system 16-bit Parallel
x	0	1	1	0	80-system 9-bit Parallel
x	0	1	1	1	80-system 18-bit Parallel
x	1	1	0	0	68-system 8-bit Parallel
x	1	1	0	1	68-system 16-bit Parallel
x	1	1	1	0	68-system 9-bit Parallel
x	1	1	1	1	68-system 18-bit Parallel
0	x	0	x	x	3 wire serial Interface only
1	x	0	x	x	4 wire serial Interface only

Table 5.1 Interface selection

Interface	NRD_E	NWR_RNW	DNC_SCL	DB17 – DB0	
				Command/Parameter	GRAM
80-system 8-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB7-DB0
80-system 9-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB8-DB0
80-system 16-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB15-DB0
80-system 18-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB17-DB0
3 wire serial Interface	-	-	SCL	DB0 as SDA	
68-system 8-bit Parallel	E	RW	DNC	DB7-DB0	DB7-DB0
68-system 9-bit Parallel	E	RW	DNC	DB7-DB0	DB8-DB0
68-system 16-bit Parallel	E	RW	DNC	DB7-DB0	DB15-DB0
68-system 18-bit Parallel	E	RW	DNC	DB7-DB0	DB17-DB0
4 wire serial Interface	-	DNC	SCL	DB0 as SDA	

Table 5.2 Interface mode selection

5.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface as listed in Table 5.3 and Table 5.4.

Operations	NWR_RNW	NRD_E	DNC_SCL
Writes command code	0	1	0
Reads internal status	1	0	0
Writes parameter into command or data into GRAM	0	1	1
Reads parameter from command or data from GRAM	1	0	1

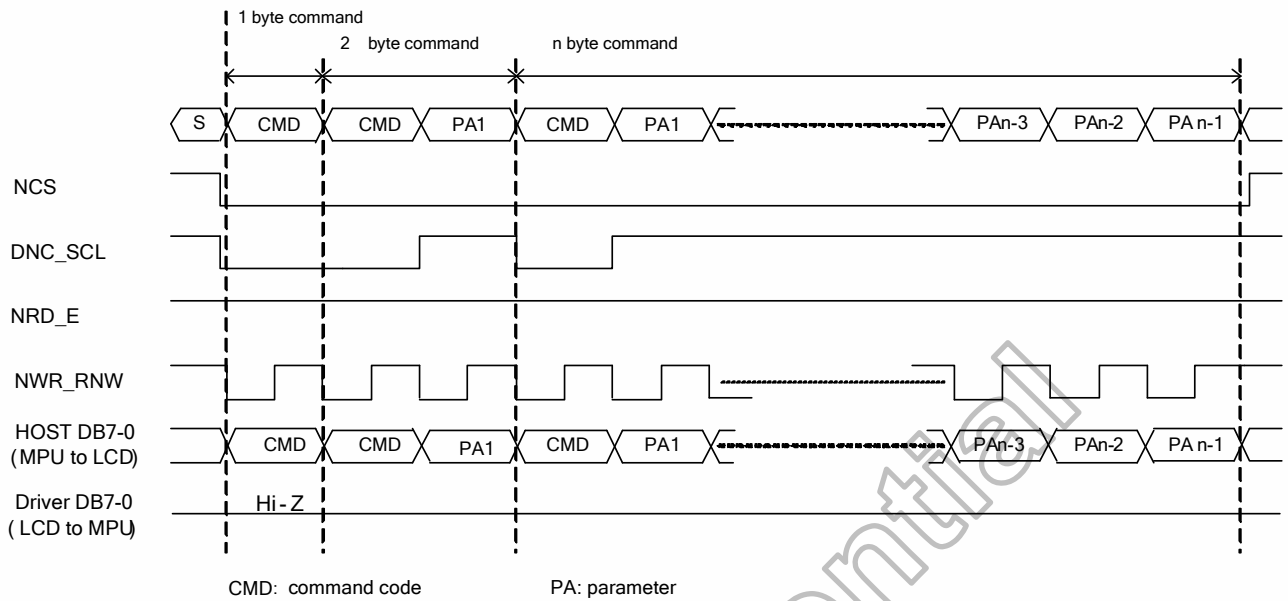
Table 5.3 Data pin function for I80 series CPU

Operations	NWR_RNW	NRD_E	DNC_SCL
Writes command code	0	1	0
Reads internal status	1	1	0
Writes parameter into command or data into GRAM	0	1	1
Reads parameter from command or data from GRAM	1	1	1

Table 5.4 Data pin function for M68 series CPU

Himax Confidential
Do Not Copy

Write to register



Read from register

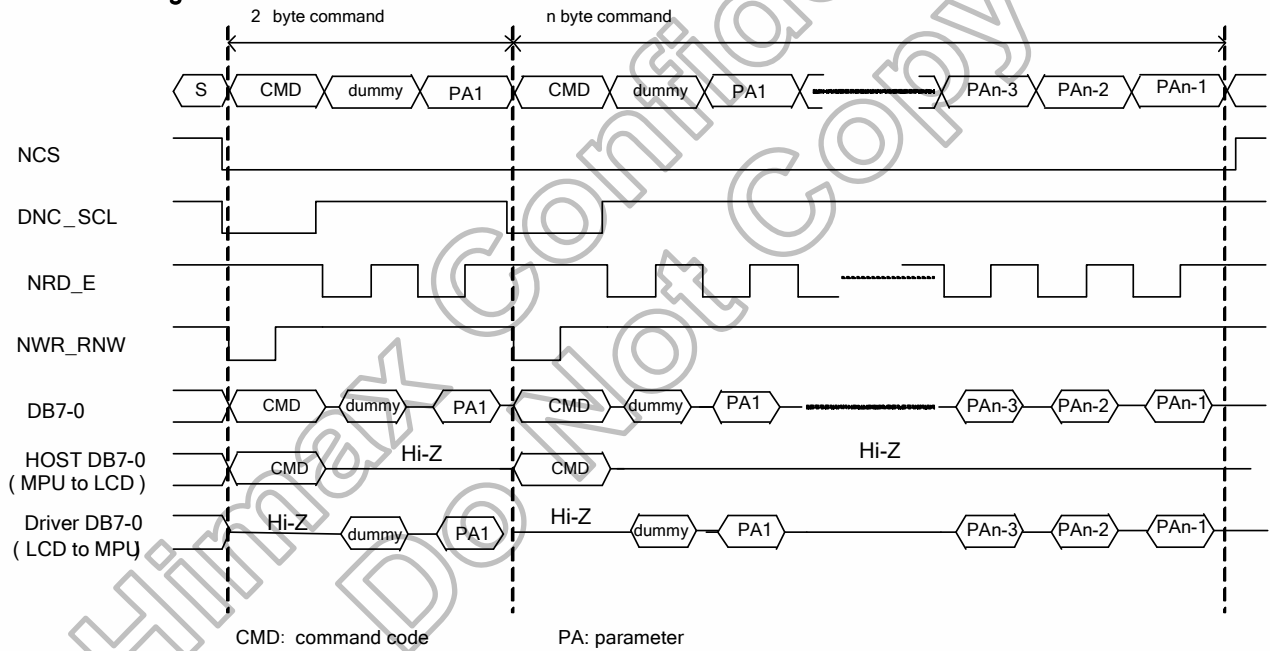
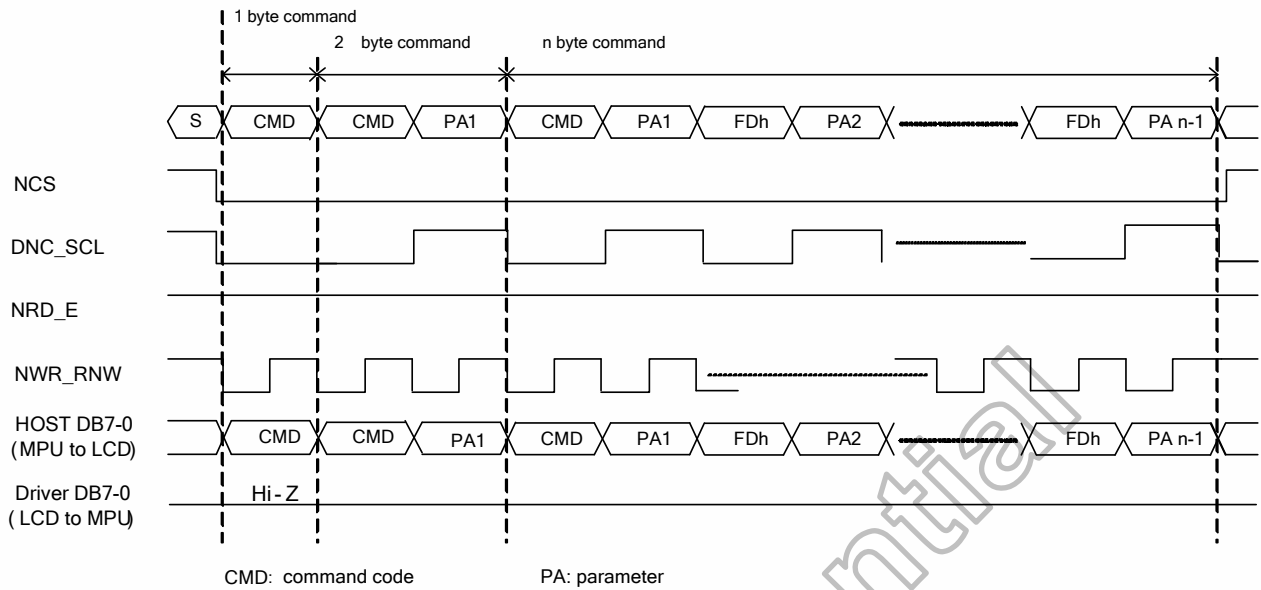


Figure 5.1 Register read/write timing in parallel bus system interface (for I80 series MPU)-1

Write to register



Read from register

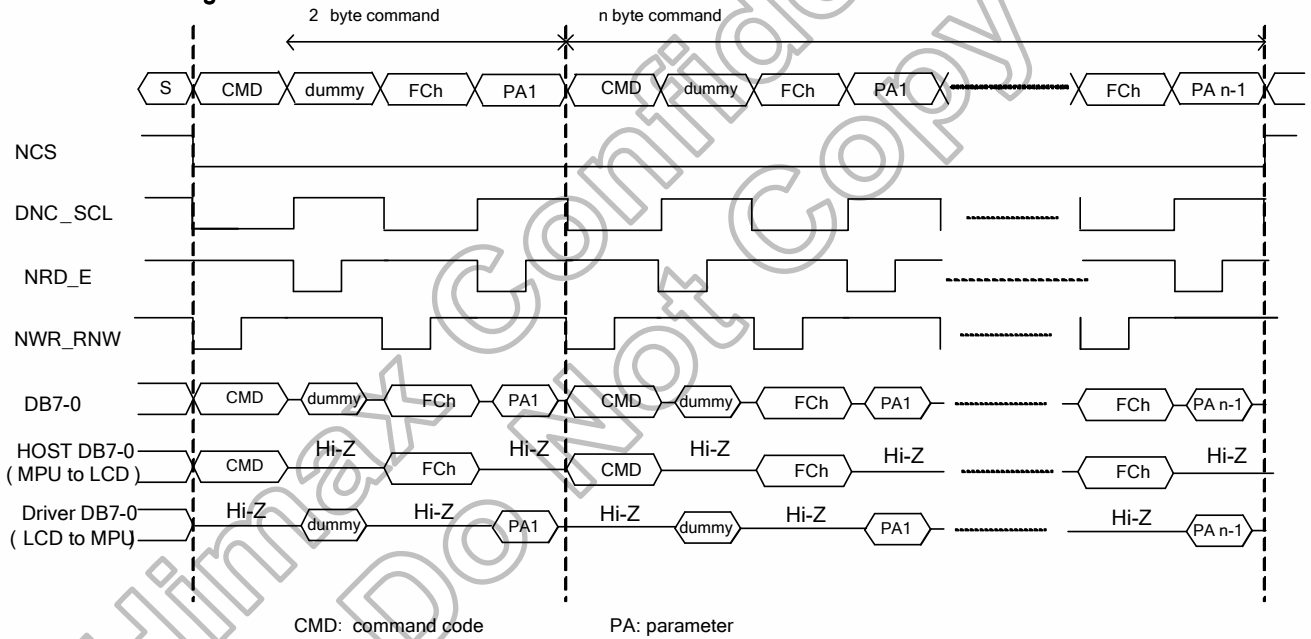
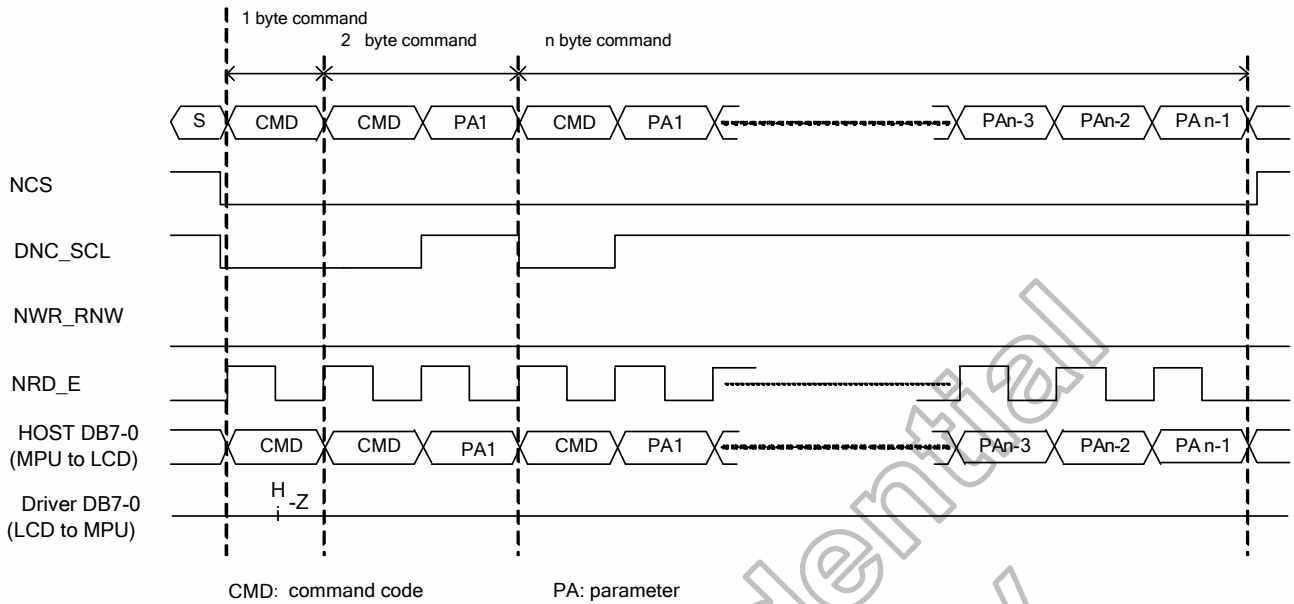


Figure 5.2 Register read/write timing in parallel bus system interface (for I80 series MPU)-2

Write to register



Read from register

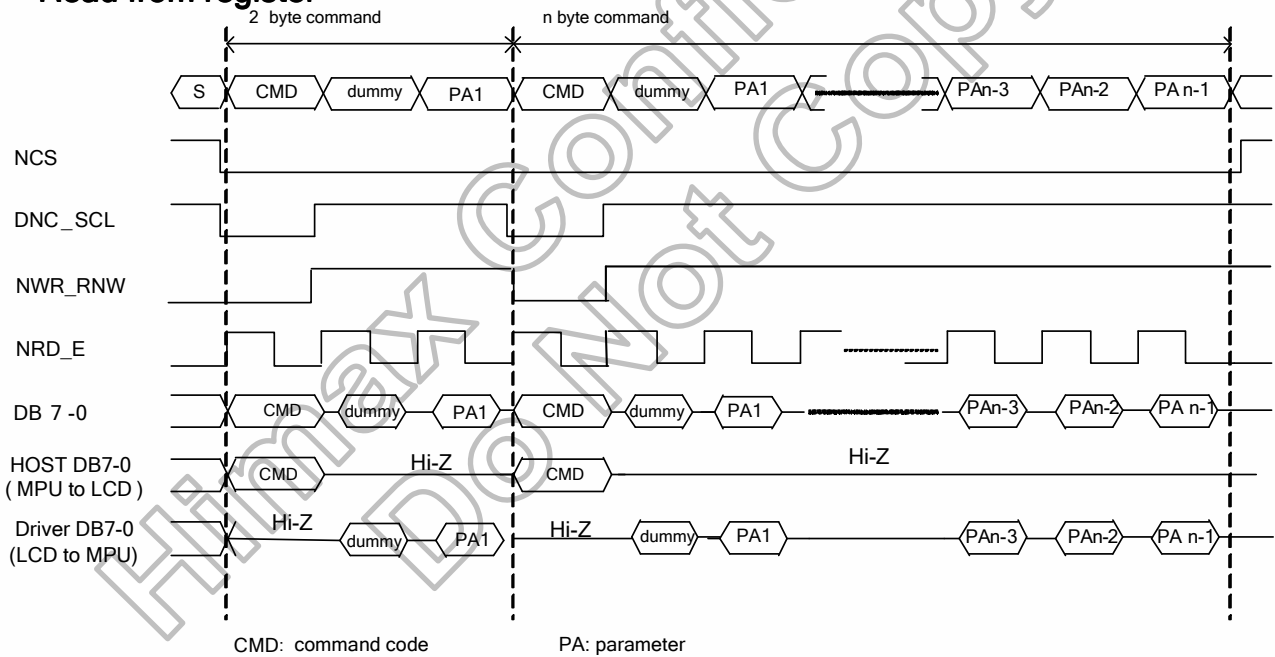
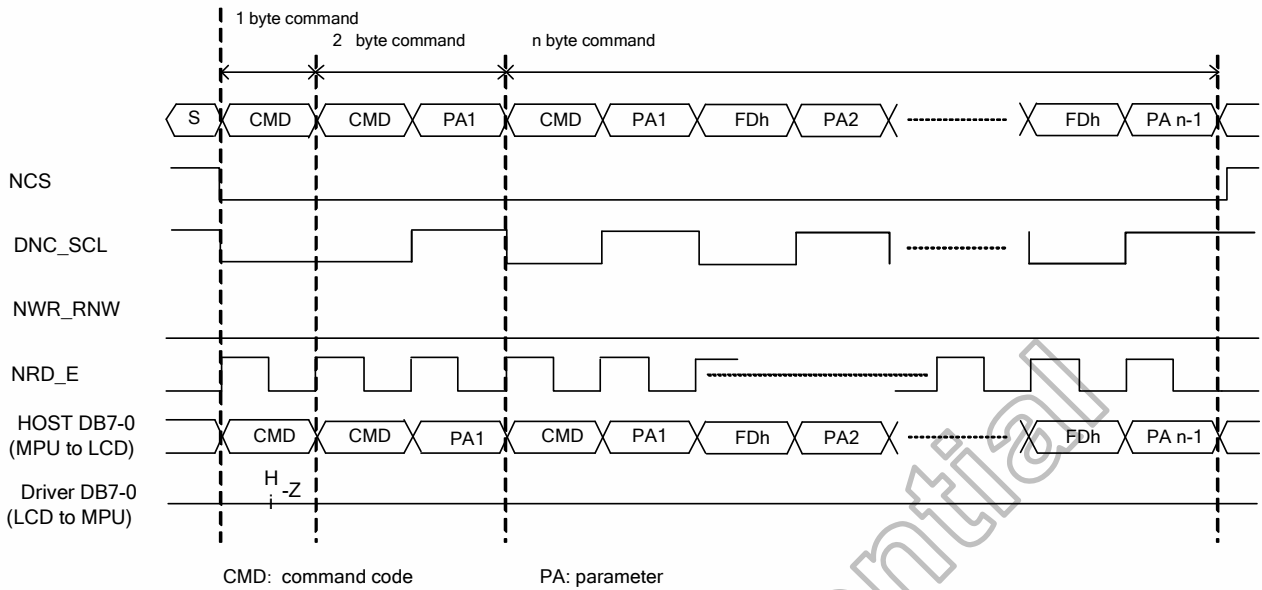


Figure 5.3 Register read/write timing in parallel bus system interface (for M68 series MPU)-1

Write to register



Read from register

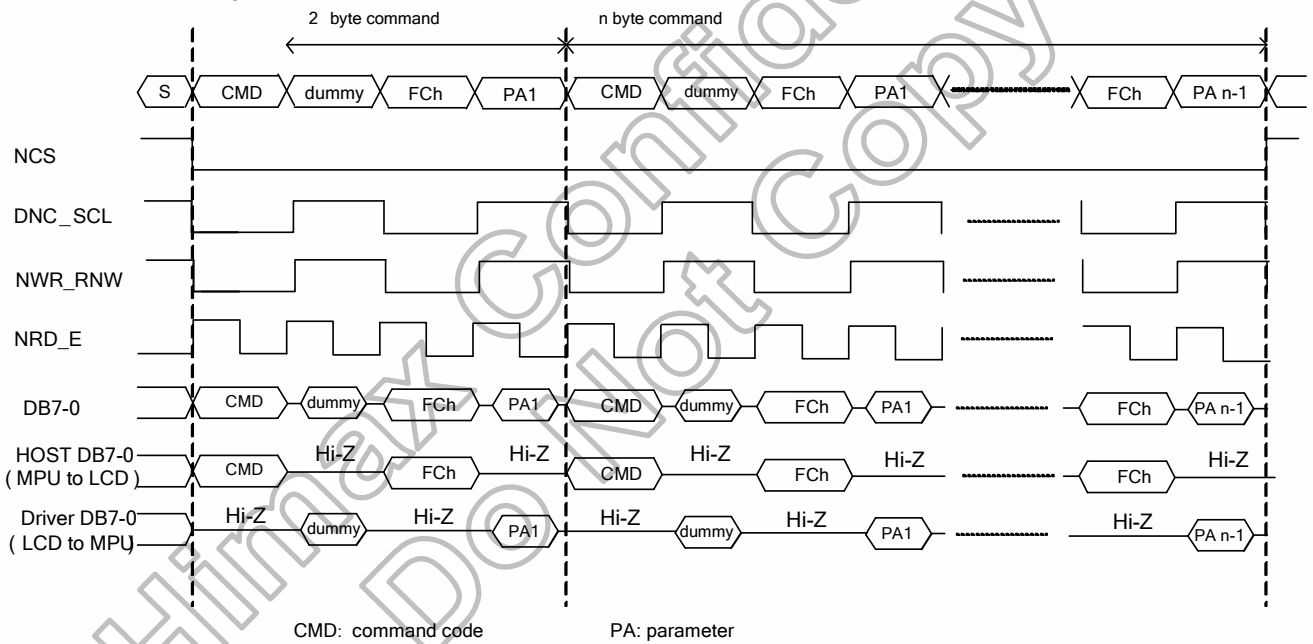
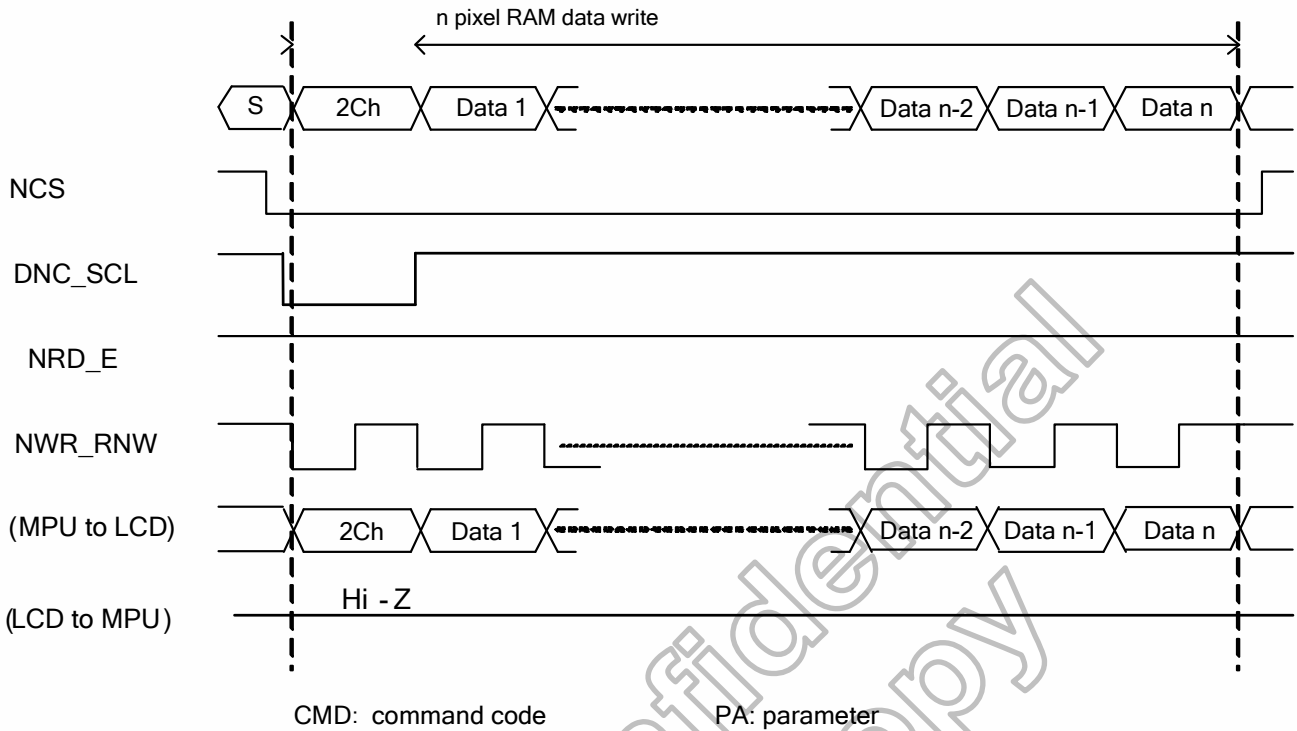


Figure 5.4 Register read/write timing in parallel bus system interface (for M68 series MPU)-2

Write to GRAM



Read from GRAM

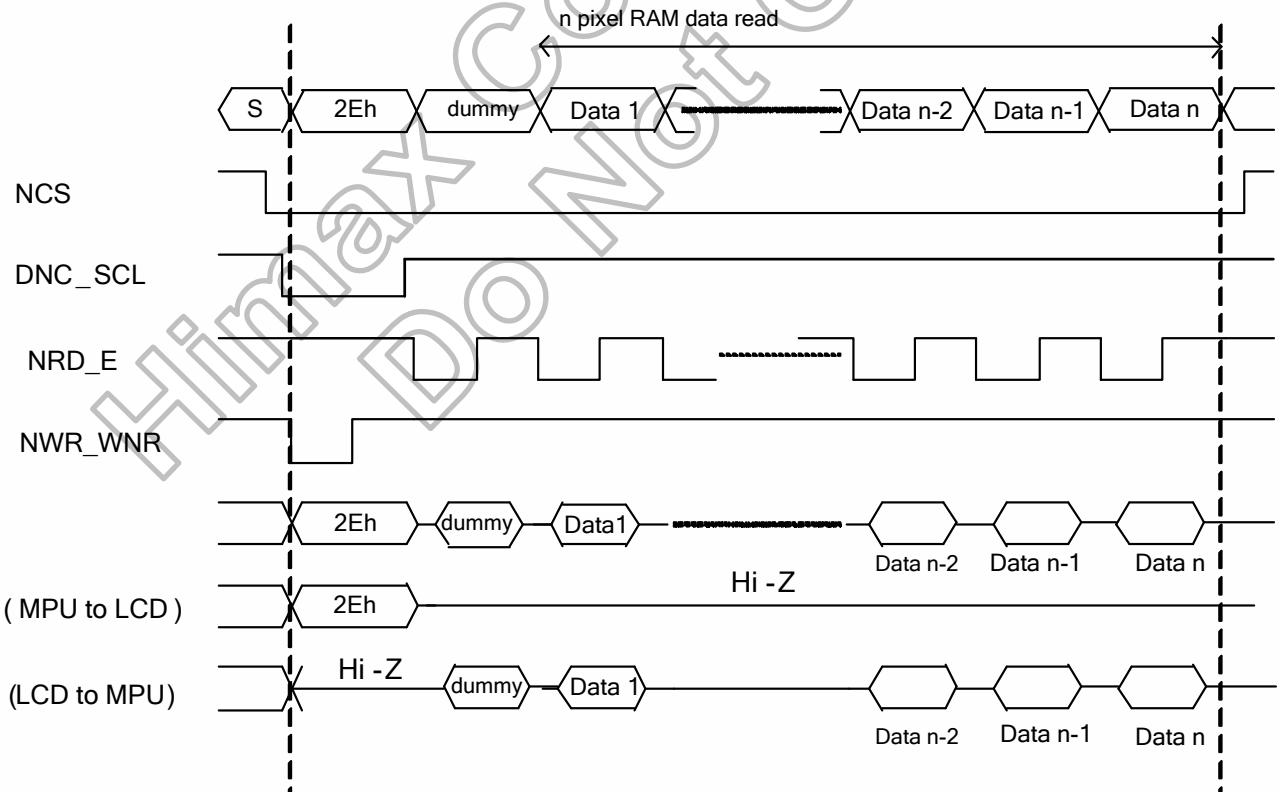
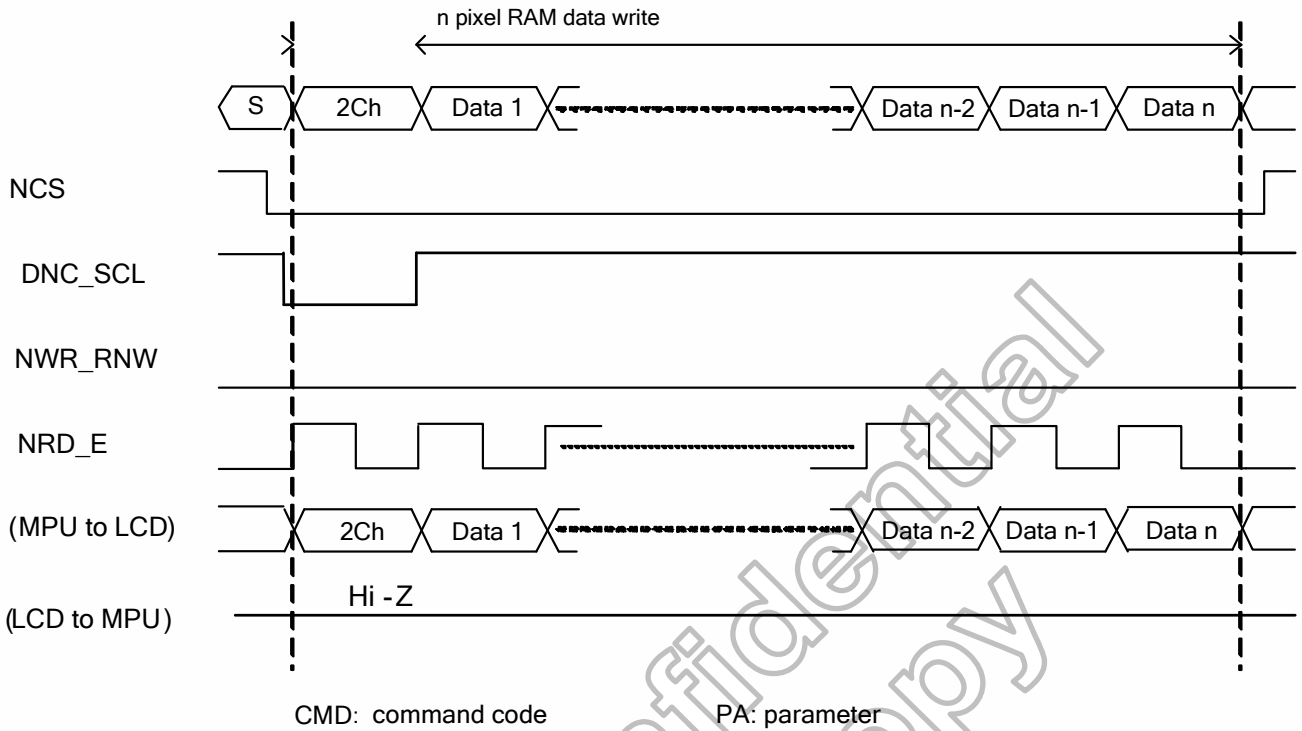


Figure 5.5 GRAM read/write timing in parallel bus system interface (for I80 series MPU)

Write to GRAM



Read from GRAM

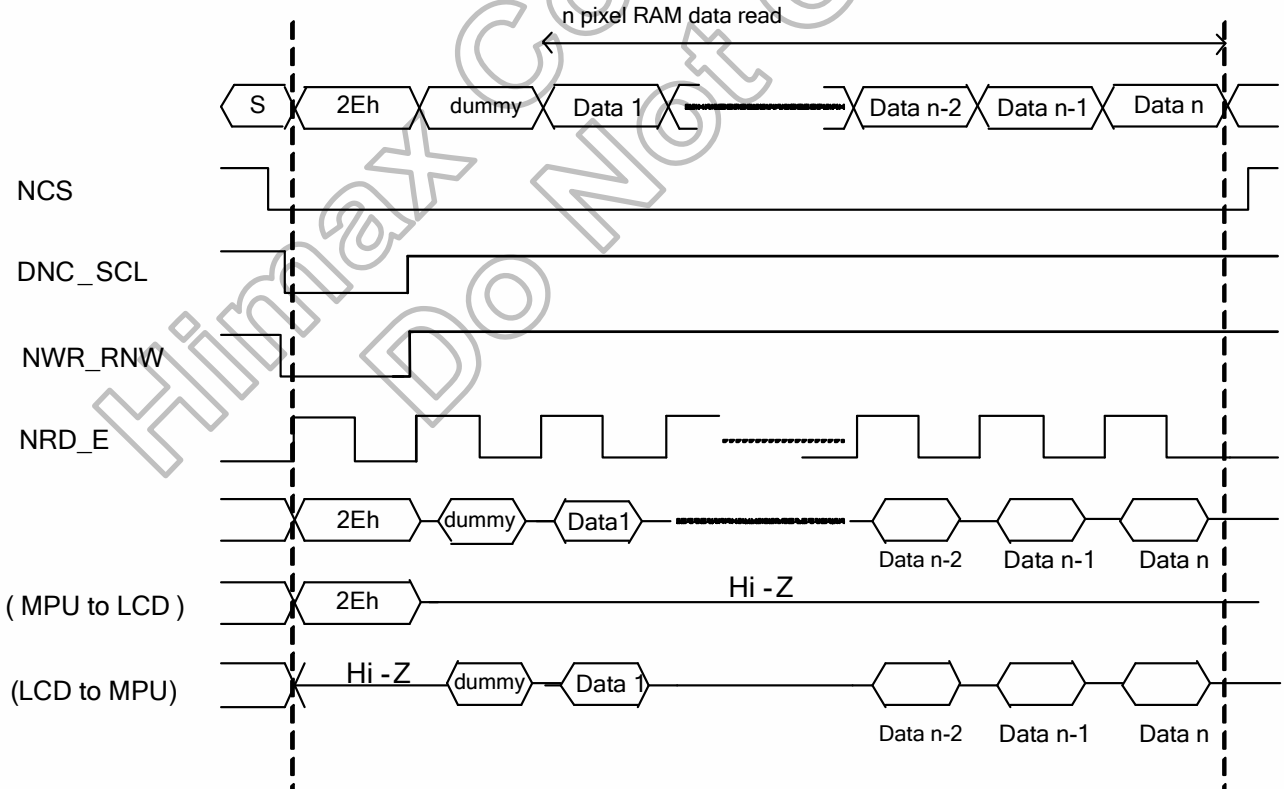


Figure 5.6 GRAM read/write timing in parallel bus system interface (for M68 series MPU)

5.1.2 MCU data color coding

MCU Data Color Coding for RAM data Write

- Parallel 8-Bit Bus Interface (BS2,BS1,BS0="100")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
3AH	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixel/ 3-bytes)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.5 8-bit parallel interface GRAM write table

- Parallel 16-Bit Bus Interface (BS2,BS1,BS0="101")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
3AH	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.6 16-bit parallel interface GRAM write table

- Parallel 9-Bit Bus Interface (BS2,BS1,BS0="110")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
3AH	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.7 9-bit parallel interface GRAM write table

- Parallel 18-Bit Bus Interface (BS2,BS1,BS0="111")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
3AH	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.8 18-bit parallel interface GRAM write table

8-bit bus interface

The I80-system 8-bit parallel bus interface can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0100”. And the M68-system 8-bit parallel bus interface can be used by setting “P68, BS2, BS1, and BS0” pins to “1100”. Figure 5.7 is the example of interface with I80/M68 microcomputer system interface and Figure 5.8 ~Figure 5.10 is bit format per pixel color order.

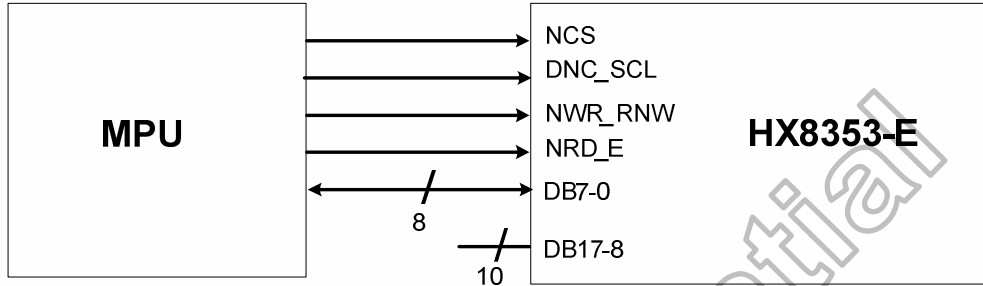


Figure 5.7 Example of 80- / 68- system 8-bit bus interface

262k Color Data	DNC_SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R15	R14	R13	R12	R11	R10	x	x	-
2nd write	1	G15	G14	G13	G12	G11	G10	x	x	-
3rd write	1	B15	B14	B13	B12	B11	B10	x	x	1st pixel (R1/G1/B1)
4th write	1	R25	R24	R23	R22	R21	R20	x	x	-
5th write	1	G25	G24	G23	G22	G21	G20	x	x	-
6th write	1	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

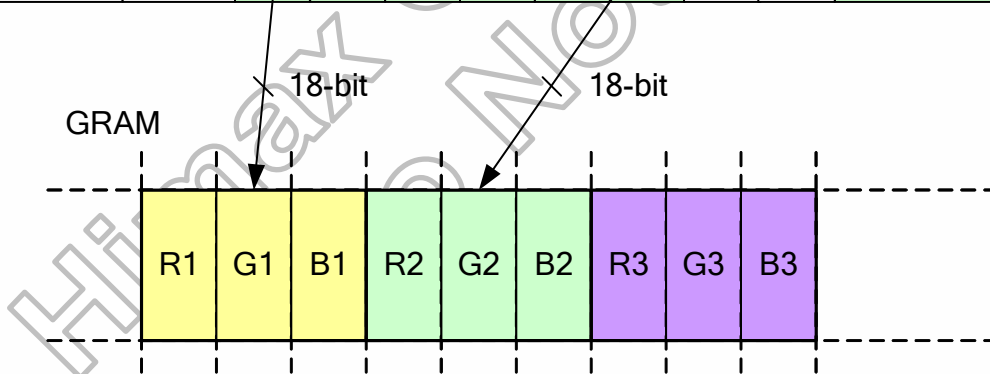
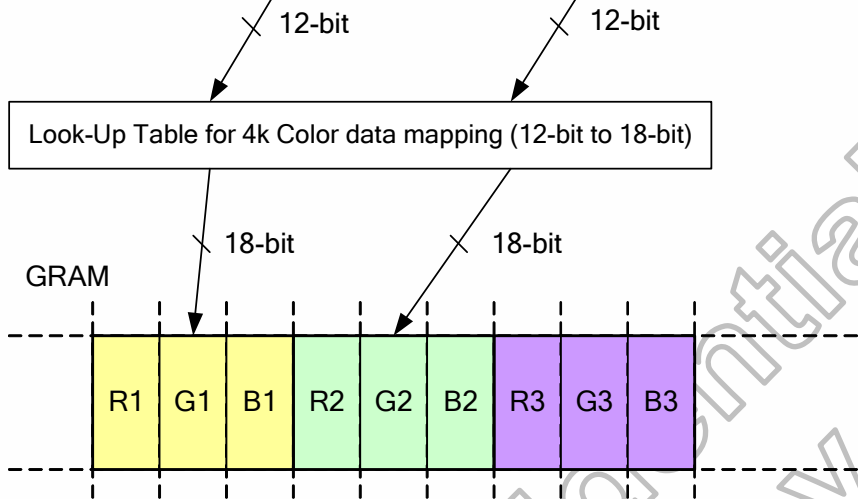


Figure 5.8 Write data for RGB 6-6-6-bit input

4k Color Data	DNC_SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R13	R12	R11	R10	G13	G12	G11	G10	-
2nd write	1	B13	B12	B11	B10	R23	R22	R21	R20	1st pixel (R1/G1/B1)
3rd write	1	G23	G22	G21	G20	B23	B22	B21	B20	2nd pixel (R2/G2/B2)



4k Color Data	DNC_SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R13	R12	R11	R10	G13	G12	G11	G10	-
2nd write	1	B13	B12	B11	B10	R23	R22	R21	R20	1st pixel (R1/G1/B1)
MEMWR	0	The other command								-
MEMWR	0	GRAM Write command code								-
1st write	1	R23	R22	R21	R20	G23	G22	G21	G20	-
2nd write	1	B23	B22	B21	B20	R33	R32	R31	R30	2nd pixel (R2/G2/B2)
3rd write	1	G33	G32	G31	G30	B33	B32	B31	B30	3rd pixel (R3/G3/B3)

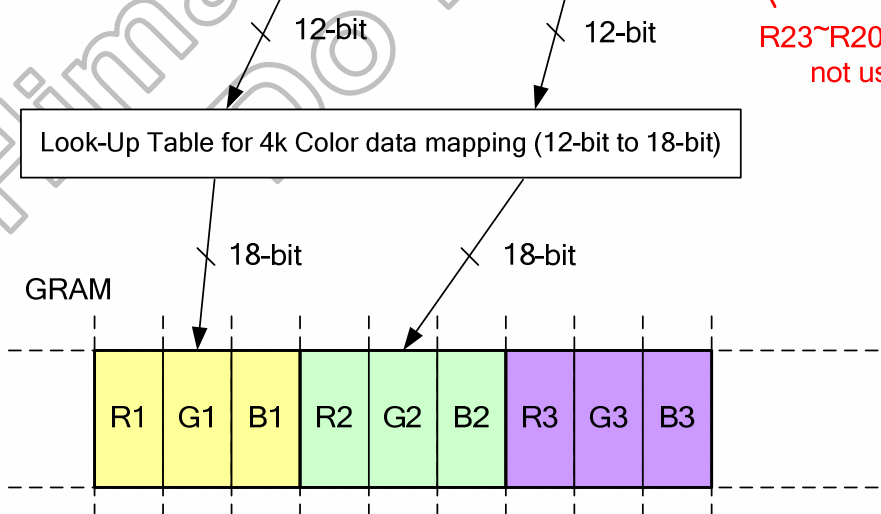


Figure 5.9 Write data for RGB 4-4-4-bit input

65k Color Data	DNC_SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

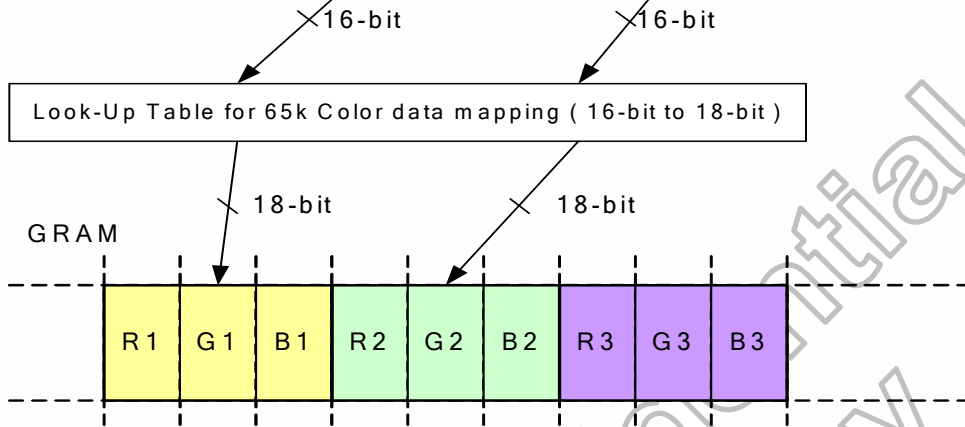


Figure 5.10 Write data for RGB 5-6-5-bit input

Himax Confidential
Do Not Copy

16-bit parallel bus system interface

The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0101”. And the M68-system 16-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1” pins to “1101”. The Figure 5.11 is the example of interface with I80/M68 microcomputer system interface. There are three types of data format to write display data at 18-bit bus Interface. See Figure 5.12 ~ Figure 5.14.

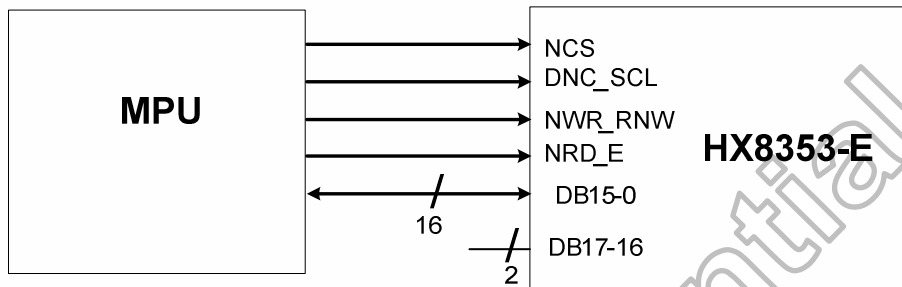


Figure 5.11 Example of I80- / M68- system 16-bit parallel bus interface

	DNC_SCL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	x	x	x	x	x	x	x	x	GRAM Write command code (2Ch)								-
1 st write	1	R15	R14	R13	R12	R11	R10	x	x	G15	G14	G13	G12	G11	G10	x	x	-
2 nd write	1	B15	B14	B13	B12	B11	B10	x	x	R25	R24	R23	R22	R21	R20	x	x	1st pixel (R1/G1/B1)
3 rd write	1	G25	G24	G23	G22	G21	G20	x	x	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

X: Don't care

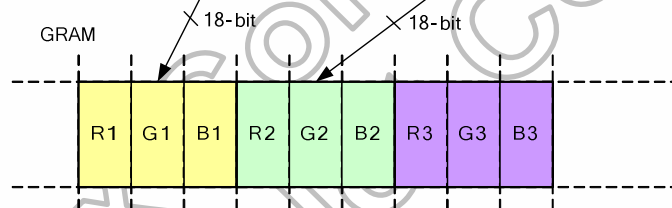


Figure 5.12 GRAM write data for RGB 6-6-6-(262k colors) bit input

4k Color Data	DNC_S CL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code																-
1st write	1	x	x	x	x	R13	R12	R11	R10	G13	G12	G11	G10	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	R23	R22	R21	R20	G23	G22	G21	G20	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

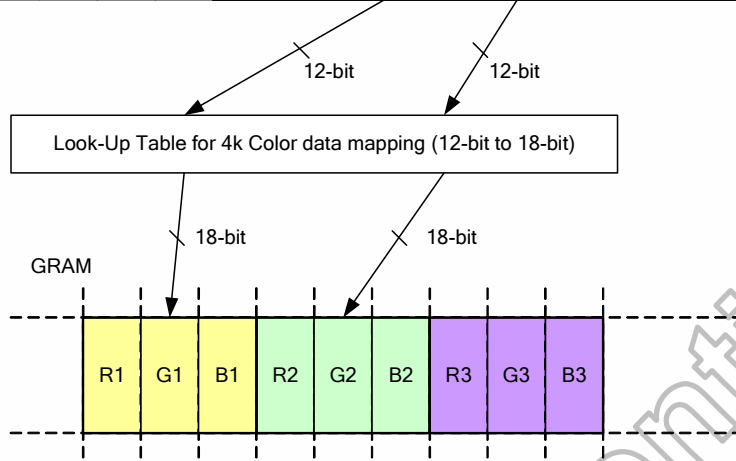


Figure 5.13 Write data for RGB 4-4-4 (4k colors) bit input on 16-bit parallel interface

65k Color Data	DNC_S CL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	x	x	x	x	x	x	x	x	GRAM Write command code								-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

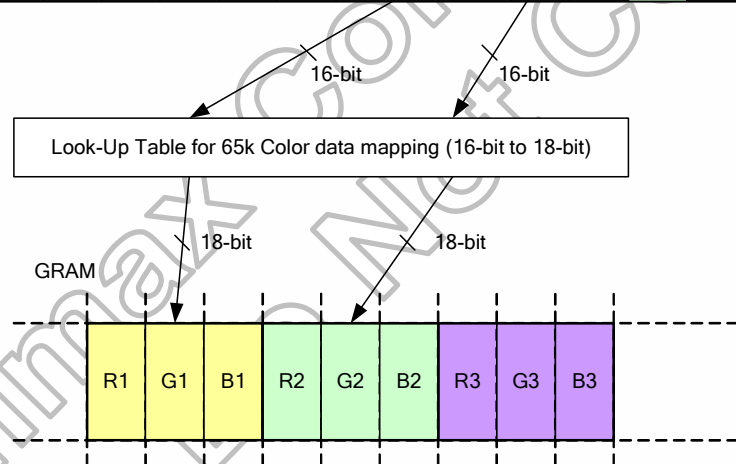


Figure 5.14 Write data for RGB 5-6-5 (65k colors) bit input on 16-bit parallel interface

18-bit parallel bus system interface

The I80-system 18-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0111”. And the M68-system 18-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1111”. The Figure5.15 is the example of interface with I80/M68 microcomputer system interface.

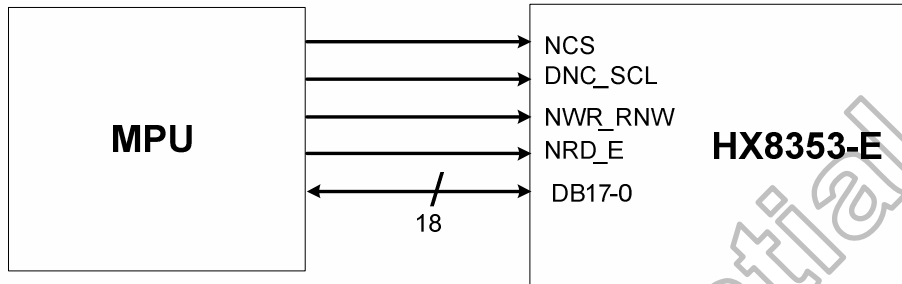


Figure 5.15 Example of I80- / M68- system 18-bit parallel bus interface

There is one type of data format to write display data at 18-bit bus Interface. See Figure 5.16.

262k Color Data	DNC_SCL	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

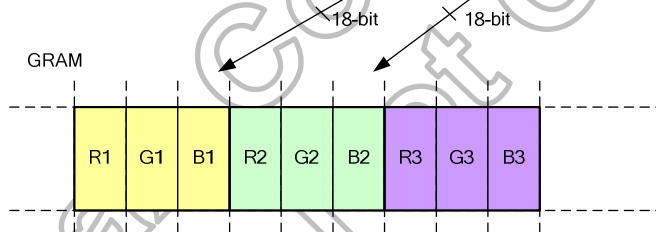


Figure 5.16 Write data for RGB 6-6-6(262k colors) bit input in 18-bit parallel interface

9-bit bus interface

The I80-system 9-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0110”. And the M68-system 9-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1110”. The Figure5.17 is the example of interface with I80/M68 microcomputer system interface.

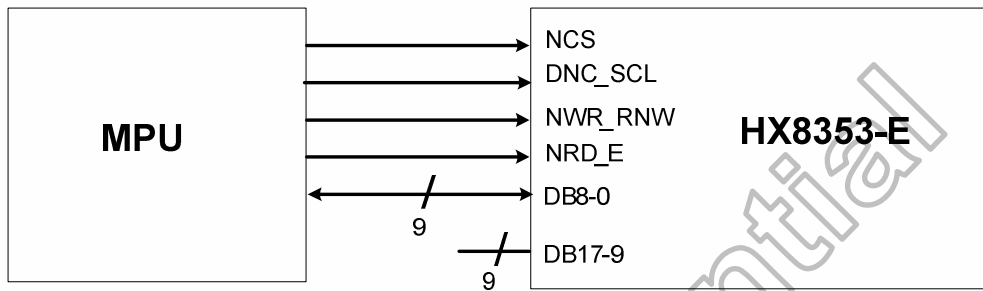


Figure 5.17 Example of 80- / 68- system 9-bit bus interface

There is one type of data format to write display data at 9-bit bus Interface. See Figure 5.18.

262k Color Data	DNC_S CL	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code									-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

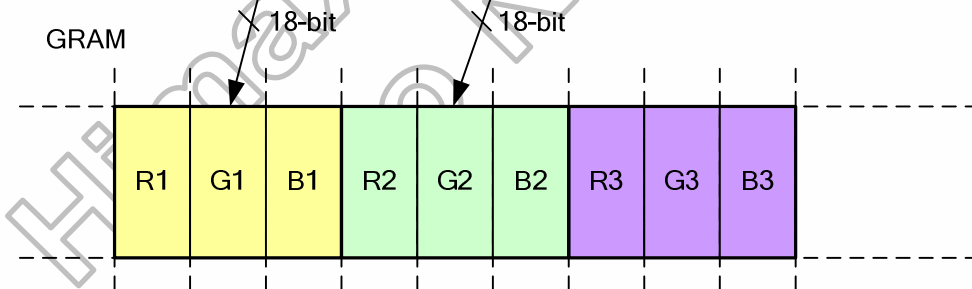


Figure 5.18 Write data for RGB 6-6-6-bit (262k colors) input in 9-bit parallel interface

MCU Data Color Coding for RAM data Read

- Parallel 8-Bit Bus Interface (BS2,BS1,BS0="100")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x		

Table 5.9 8-bit parallel interface GRAM read table

- Parallel 16-Bit Bus Interface (BS2,BS1,BS0="101")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x		

Table 5.10 16-bit parallel interface GRAM read table

- Parallel 9-Bit Bus Interface (BS2,BS1,BS0="110")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register	
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH	
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read	
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.11 9-bit parallel interface GRAM read table

- Parallel 18-Bit Bus Interface (BS2,BS1,BS0="111")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.12 18-bit parallel interface GRAM read table

5.1.3 Serial Interface

The HX8353-E supports serial data transfer interface. The interface selection by setting BS2=0 for serial interface mode. The 3-wires serial bus and 4-wires serial bus is select by SPI_SEL pin. When SPI_SEL pin is low (VSSD), it is selected by 3-wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC_SCL). When SPI_SEL pin is high (IOVCC), it is selected by 4-wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC_SCL) and the command or data transfer signal (NWR_RNW).

Serial data write mode

The 3-wires serial data packet contains a control bit DNC and a transmission byte, and in 4-wires serial case data packet contains just transmission byte and control bit DNC is transferred by NWR_RNW pin. If NWR_RNW is low, the transmission byte is command byte. If NWR_RNW is high, the transmission byte is stored to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, DNC_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

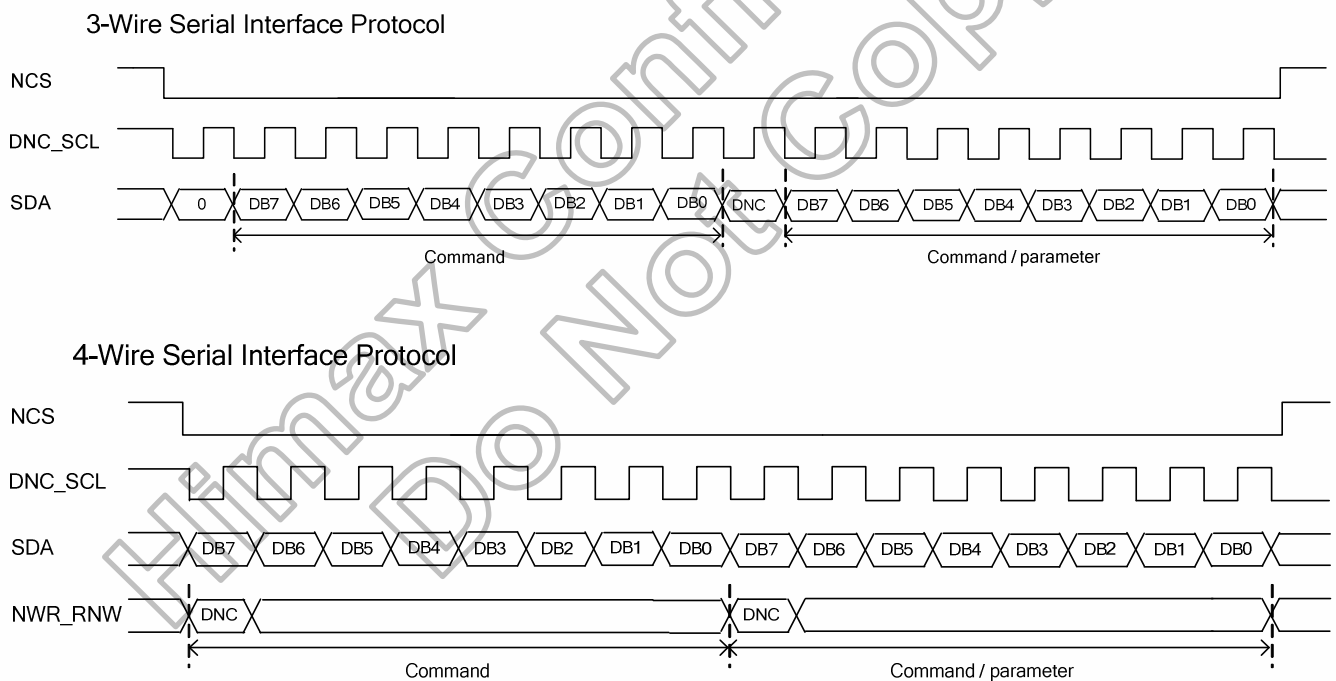


Figure 5.19 Serial interface protocol 3-/4- wire, write mode

Serial data read mode

The microcontroller first has to send a command and then the following byte is transmitted in the opposite direction. The read mode has three type command data transmitted (8- / 24- / 32-bit) is according command code.

3-Wire Serial Interface Protocol

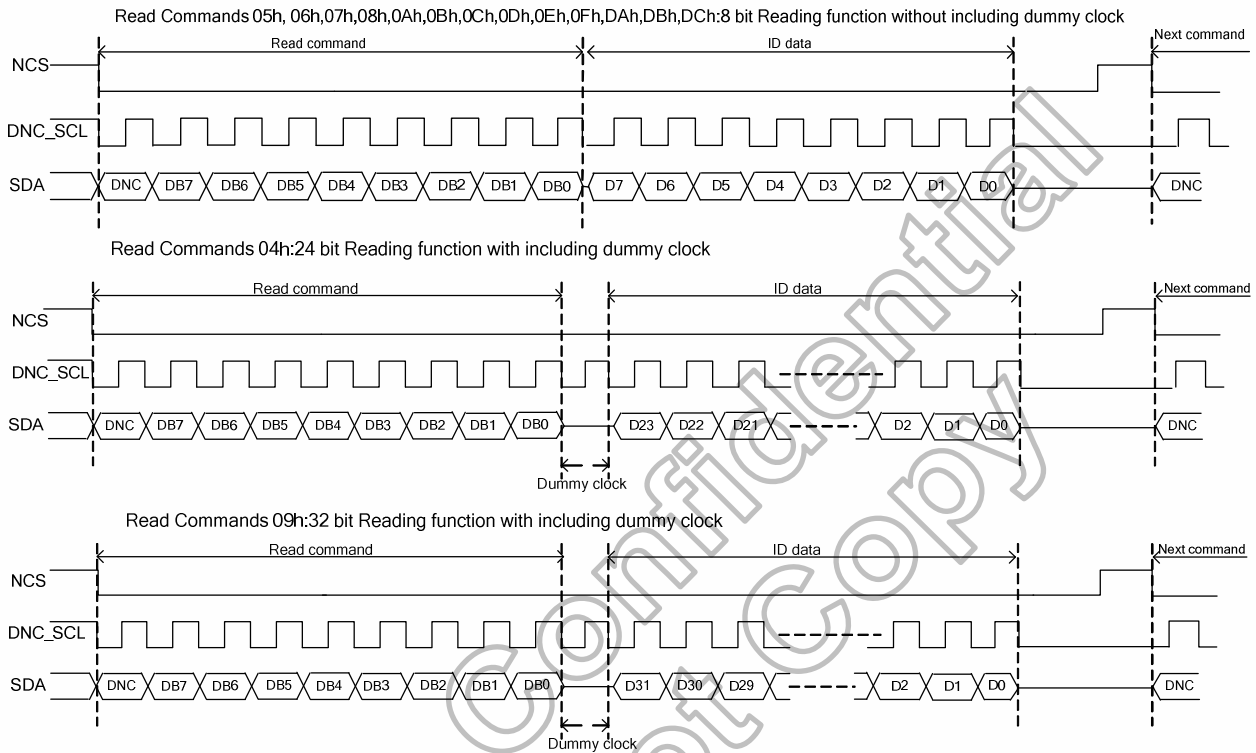


Figure 5.20 3-wire serial interface protocol, read mode

4-Wire Serial Interface Protocol

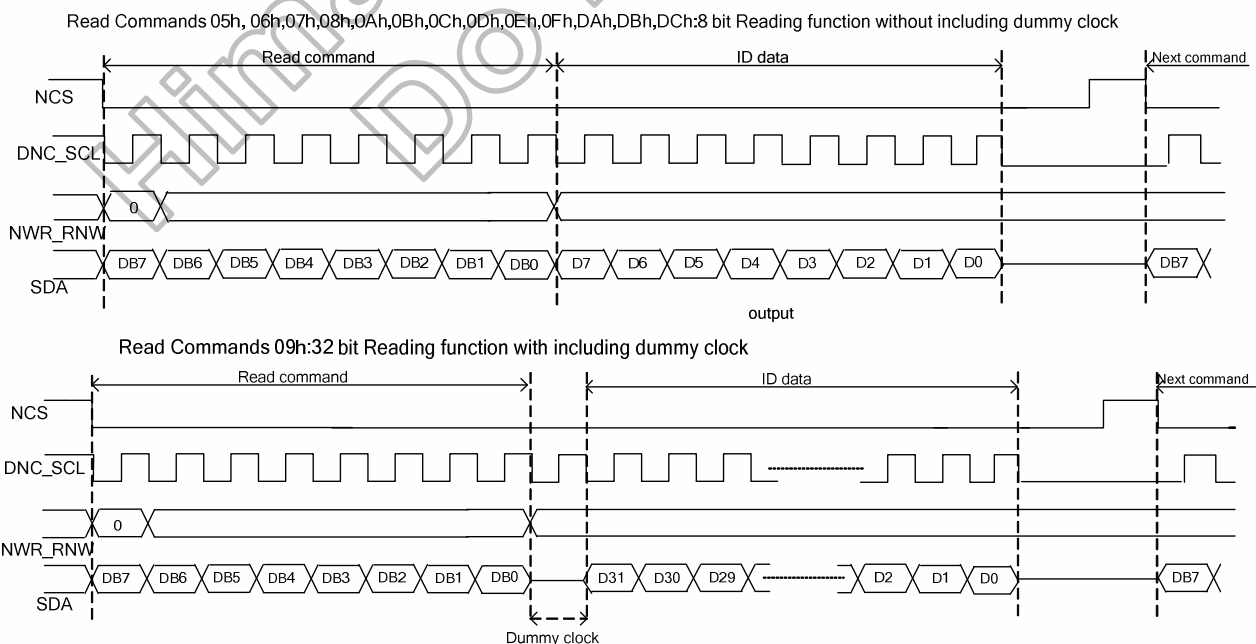


Figure 5.21 4-wire serial interface protocol, read mode

The data format that write display data to SRAM at Serial data bus Interface is shown as Figure5. 22 ~ Figure5. 27.

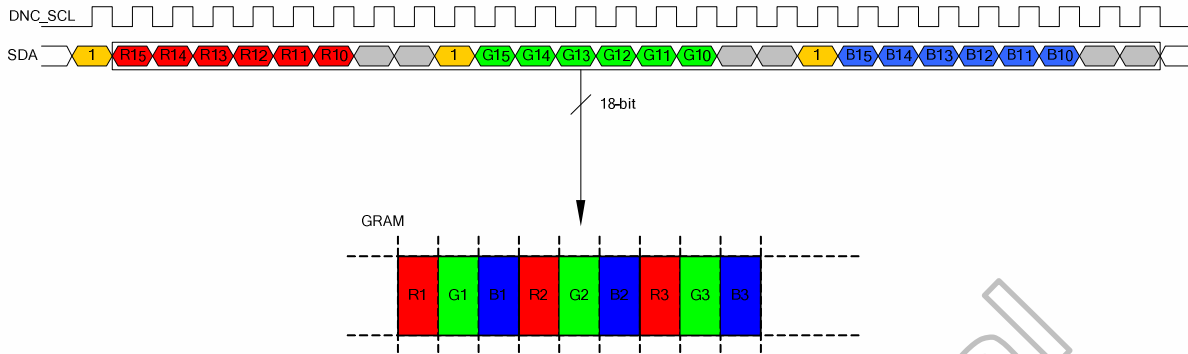


Figure 5.22 3-wire serial write data for RGB (6-6-6) bit input

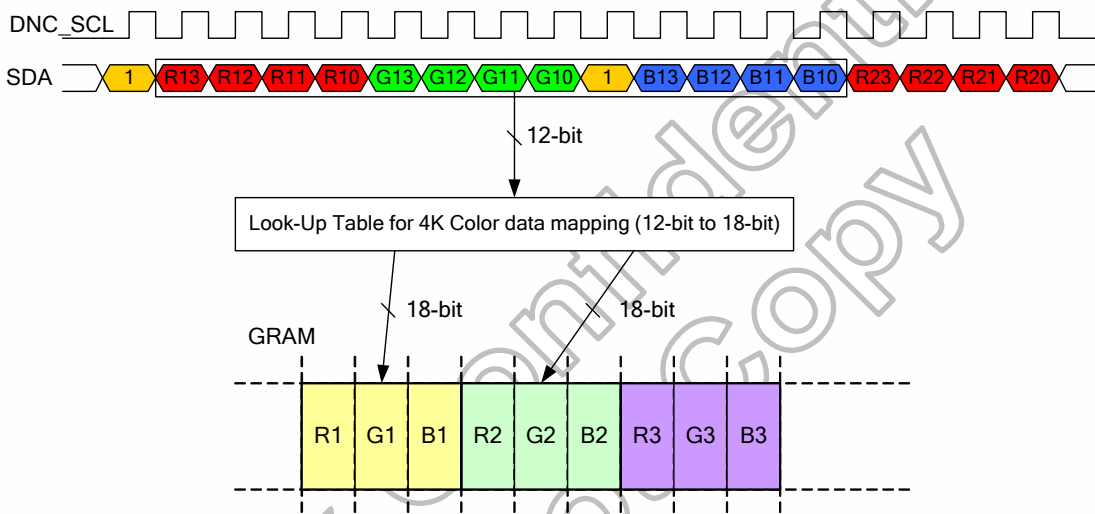


Figure 5.23 3-wire serial write data for RGB 4-4-4-bit input

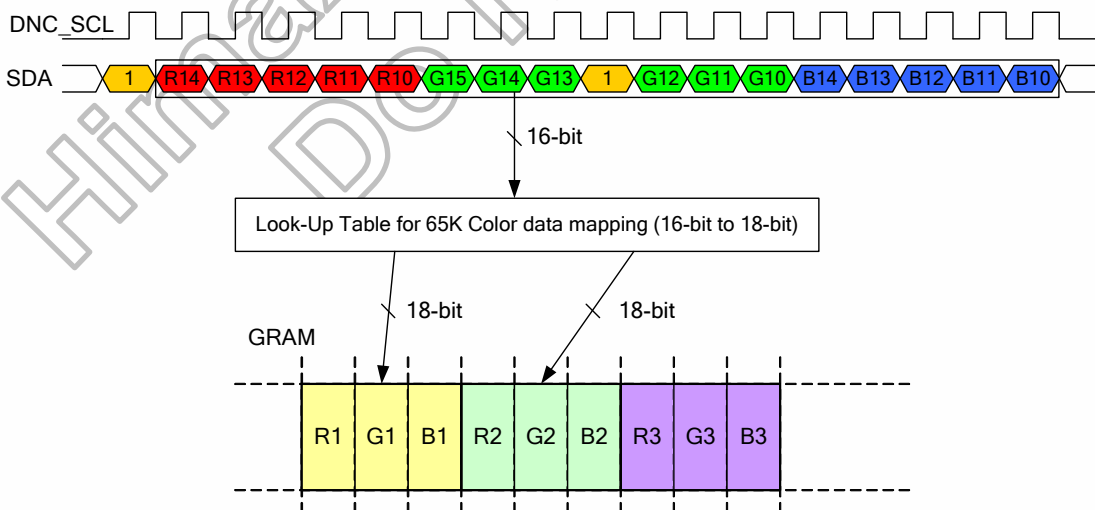


Figure 5.24 3-wire serial write data for RGB 5-6-5-bit input

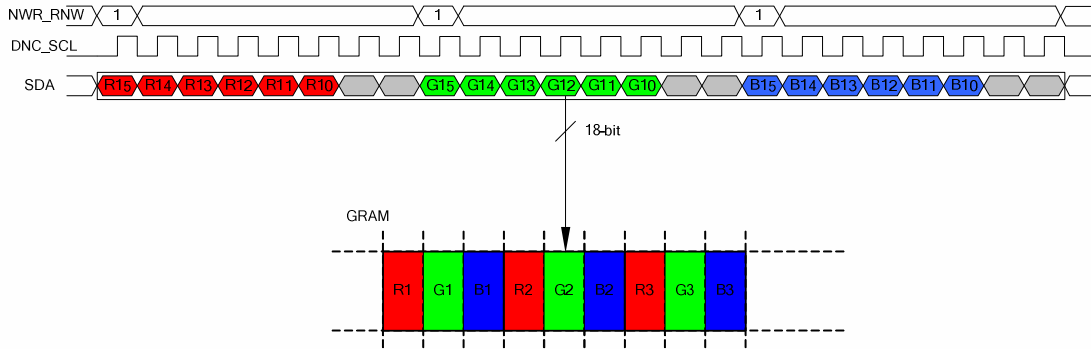


Figure 5.25 4-wire serial write data for RGB (6-6-6) bit input

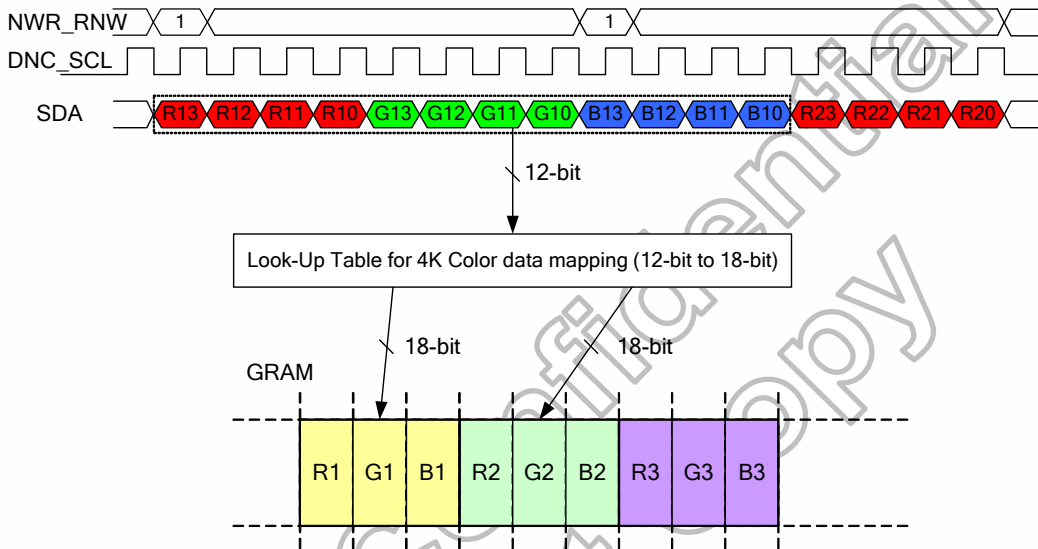


Figure 5.26 4-wire serial write data for RGB 4-4-4-bit input

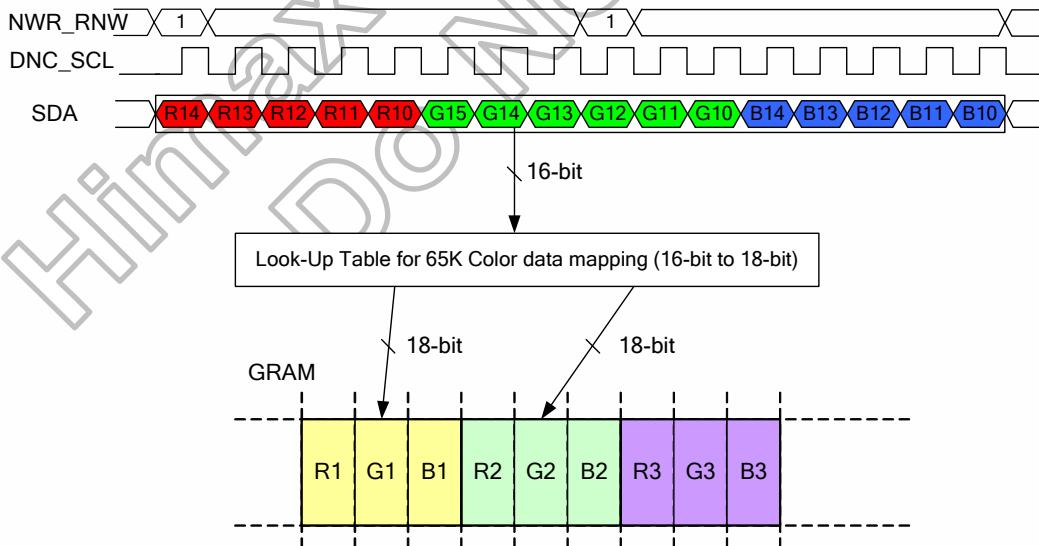


Figure 5.27 4-wire serial write data for RGB 5-6-5-bit input

5.1.4 Display module data transfer recovery

If there is a break on data transmission when transmitting a command before a whole byte has been completed, then the display module will reset the interface so that it will be ready to receive the same byte re-transmitted when the chip select line (NCS) is next activated. See the following figure.

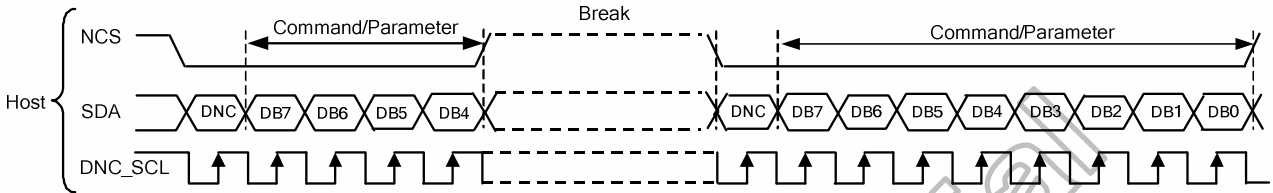
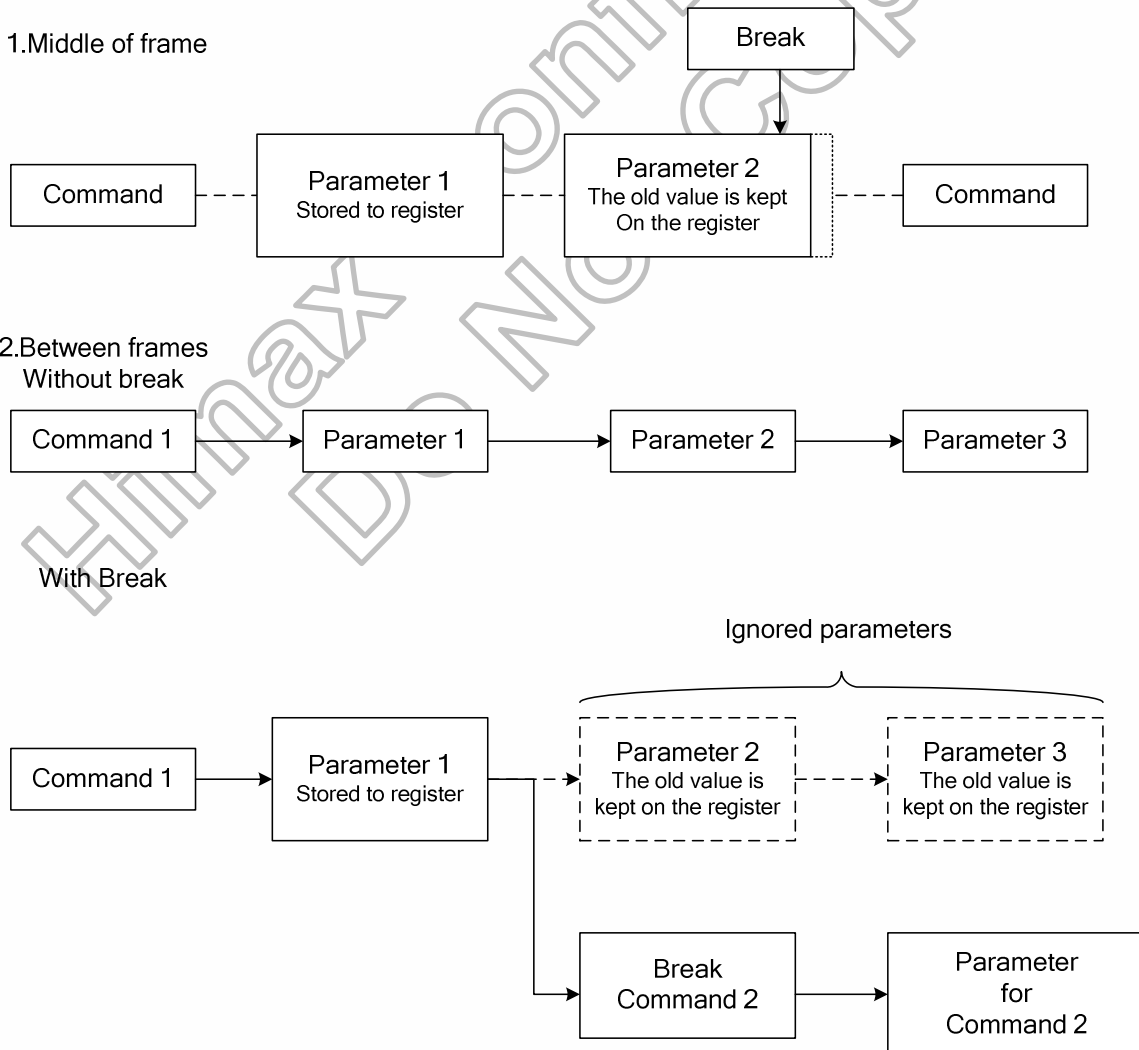


Figure 5.28 Display module data transfer recovery

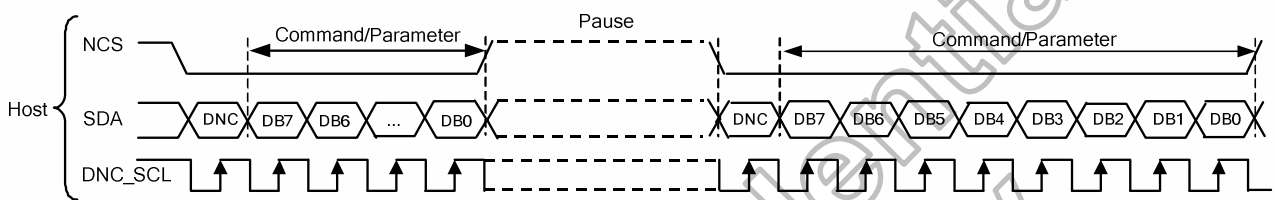
If 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:



5.1.5 Display module data transfer pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

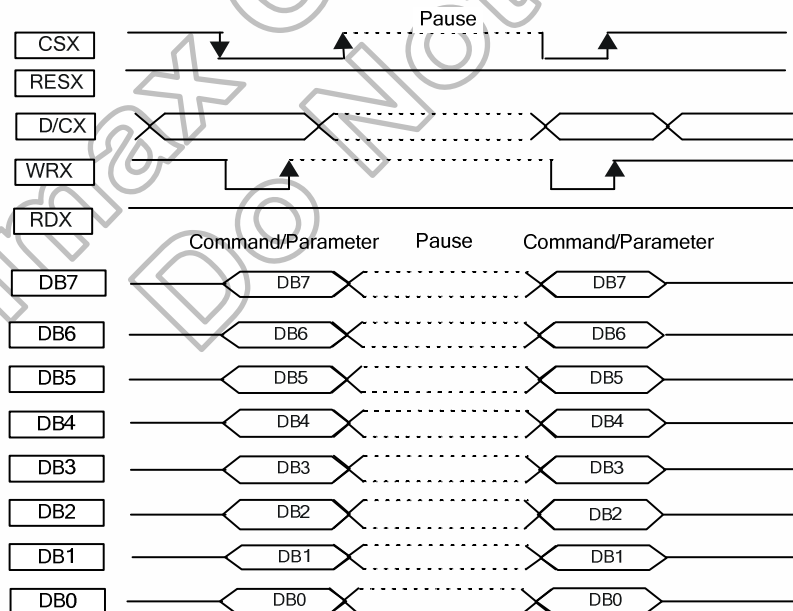
Serial interface pause



This applies to the following 4 conditions:

- a. Command-Pause-Command
- b. Command-Pause-Parameter
- c. Parameter-Pause-Command
- d. Parameter-Pause-Parameter

Parallel interface pause



This applies to the following 4 conditions:

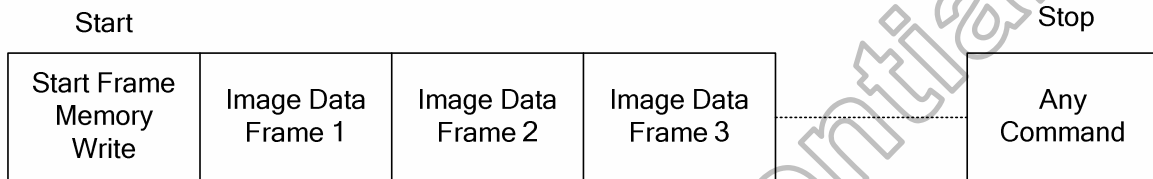
- a. Command-Pause-Command
- b. Command-Pause-Parameter
- c. Parameter-Pause-Command
- d. Parameter-Pause-Parameter

5.1.6 Display module data transfer modes

The Module has three colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

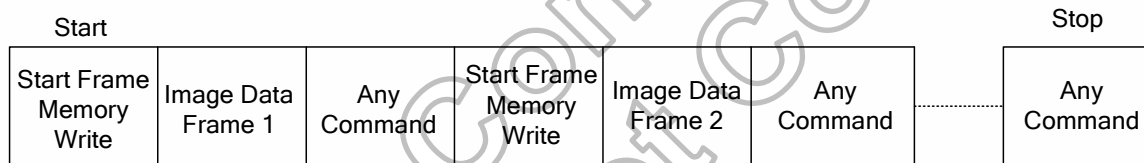
Method 1:

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



Method 2:

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



- Note:** (1) These apply to all Data Transfer Colour modes on both Serial and Parallel interfaces.
 (2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 Color depth conversion

R input (4bit) 12 bit/pixel -mode 4,096 colors	R input (5 bit) 16 bit/pixel -mode 65,536 colors	R output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	00000	R005 R004 R003 R002 R001 R000	1
0001	00001	R015 R014 R013 R012 R011 R010	2
0010	00010	R025 R024 R023 R022 R021 R020	3
0011	00011	R035 R034 R033 R032 R031 R030	4
0100	00100	R045 R044 R043 R042 R041 R040	5
0101	00101	R055 R054 R053 R052 R051 R050	6
0110	00110	R065 R064 R063 R062 R061 R060	7
0111	00111	R075 R074 R073 R072 R071 R070	8
1000	01000	R085 R084 R083 R082 R081 R080	9
1001	01001	R095 R094 R093 R092 R091 R090	10
1010	01010	R105 R104 R103 R102 R101 R100	11
1011	01011	R115 R114 R113 R112 R111 R110	12
1100	01100	R125 R124 R123 R122 R121 R120	13
1101	01101	R135 R134 R133 R132 R131 R130	14
1110	01110	R145 R144 R143 R142 R141 R140	15
1111	01111	R155 R154 R153 R152 R151 R150	16
No Input	10000	R165 R164 R163 R162 R161 R160	17
No Input	10001	R175 R174 R173 R172 R171 R170	18
No Input	10010	R185 R184 R183 R182 R181 R180	19
No Input	10011	R195 R194 R193 R192 R191 R190	20
No Input	10100	R205 R204 R203 R202 R201 R200	21
No Input	10101	R215 R214 R213 R212 R211 R210	22
No Input	10110	R225 R224 R223 R222 R221 R220	23
No Input	10111	R235 R234 R233 R232 R231 R230	24
No Input	11000	R245 R244 R243 R242 R241 R240	25
No Input	11001	R255 R254 R253 R252 R251 R250	26
No Input	11010	R265 R264 R263 R262 R261 R260	27
No Input	11011	R275 R274 R273 R272 R271 R270	28
No Input	11100	R285 R284 R283 R282 R281 R280	29
No Input	11101	R295 R294 R293 R292 R291 R290	30
No Input	11110	R305 R304 R303 R302 R301 R300	31
No Input	11111	R315 R314 R313 R312 R311 R310	32

G input (4bit) 12 bit/pixel -mode 4,096 colors	G input (6 bit) 16 bit/pixel -mode 65,536 colors	G output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	000000	G005 G004 G003 G002 G001 G000	33
0001	000001	G015 G014 G013 G012 G011 G010	34
0010	000010	G025 G024 G023 G022 G021 G020	35
0011	000011	G035 G034 G033 G032 G031 G030	36
0100	000100	G045 G044 G043 G042 G041 G040	37
0101	000101	G055 G054 G053 G052 G051 G050	38
0110	000110	G065 G064 G063 G062 G061 G060	39
0111	000111	G075 G074 G073 G072 G071 G070	40
1000	001000	G085 G084 G083 G082 G081 G080	41
1001	001001	G095 G094 G093 G092 G091 G090	42
1010	001010	G105 G104 G103 G102 G101 G100	43
1011	001011	G115 G114 G113 G112 G111 G110	44
1100	001100	G125 G124 G123 G122 G121 G120	45
1101	001101	G135 G134 G133 G132 G131 G130	46
1110	001110	G145 G144 G143 G142 G141 G140	47
1111	001111	G155 G154 G153 G152 G151 G150	48
No Input	010000	G165 G164 G163 G162 G161 G160	49
No Input	010001	G175 G174 G173 G172 G171 G170	50
No Input	010010	G185 G184 G183 G182 G181 G180	51
No Input	010011	G195 G194 G193 G192 G191 G190	52
No Input	010100	G205 G204 G203 G202 G201 G200	53
No Input	010101	G215 G214 G213 G212 G211 G210	54
No Input	010110	G225 G224 G223 G222 G221 G220	55
No Input	010111	G235 G234 G233 G232 G231 G230	56
No Input	011000	G245 G244 G243 G242 G241 G240	57
No Input	011001	G255 G254 G253 G252 G251 G250	58
No Input	011010	G265 G264 G263 G262 G261 G260	59
No Input	011011	G275 G274 G273 G272 G271 G270	60
No Input	011100	G285 G284 G283 G282 G281 G280	61
No Input	011101	G295 G294 G293 G292 G291 G290	62
No Input	011110	G305 G304 G303 G302 G301 G300	63
No Input	011111	G315 G314 G313 G312 G311 G310	64

G input (4bit) 12 bit/pixel -mode 4,096 colors	G input (6 bit) 16 bit/pixel -mode 65,536 colors	G output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
No Input	100000	G325 G324 G323 G322 G321 G320	65
No Input	100001	G335 G334 G333 G332 G331 G330	66
No Input	100010	G345 G344 G343 G342 G341 G340	67
No Input	100011	G355 G354 G353 G352 G351 G350	68
No Input	100100	G365 G364 G363 G362 G361 G360	69
No Input	100101	G375 G374 G373 G372 G371 G370	70
No Input	100110	G385 G384 G383 G382 G381 G380	71
No Input	100111	G395 G394 G393 G392 G391 G390	72
No Input	101000	G405 G404 G403 G402 G401 G400	73
No Input	101001	G415 G414 G413 G412 G411 G410	74
No Input	101010	G425 G424 G423 G422 G421 G420	75
No Input	101011	G435 G434 G433 G432 G431 G430	76
No Input	101100	G445 G444 G443 G442 G441 G440	77
No Input	101101	G455 G454 G453 G452 G451 G450	78
No Input	101110	G465 G464 G463 G462 G461 G460	79
No Input	101111	G475 G474 G473 G472 G471 G470	80
No Input	110000	G485 G484 G483 G482 G481 G480	81
No Input	110001	G495 G494 G493 G492 G491 G490	82
No Input	110010	G505 G504 G503 G502 G501 G500	83
No Input	110011	G515 G514 G513 G512 G511 G510	84
No Input	110100	G525 G524 G523 G522 G521 G520	85
No Input	110101	G535 G534 G533 G532 G531 G530	86
No Input	110110	G545 G544 G543 G542 G541 G540	87
No Input	110111	G555 G554 G553 G552 G551 G550	88
No Input	111000	G565 G564 G563 G562 G561 G560	89
No Input	111001	G575 G574 G573 G572 G571 G570	90
No Input	111010	G585 G584 G583 G582 G581 G580	91
No Input	111011	G595 G594 G593 G592 G591 G590	92
No Input	111100	G605 G604 G603 G602 G601 G600	93
No Input	111101	G615 G614 G613 G612 G611 G610	94
No Input	111110	G625 G624 G623 G622 G621 G620	95
No Input	111111	G635 G634 G633 G632 G631 G630	96

B input (4bit) 12 bit/pixel -mode 4,096 colors	B input (5 bit) 16 bit/pixel -mode 65,536 colors	B output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	00000	B005 B004 B003 B002 B001 B000	97
0001	00001	B015 B014 B013 B012 B011 B010	98
0010	00010	B025 B024 B023 B022 B021 B020	99
0011	00011	B035 B034 B033 B032 B031 B030	100
0100	00100	B045 B044 B043 B042 B041 B040	101
0101	00101	B055 B054 B053 B052 B051 B050	102
0110	00110	B065 B064 B063 B062 B061 B060	103
0111	00111	B075 B074 B073 B072 B071 B070	104
1000	01000	B085 B084 B083 B082 B081 B080	105
1001	01001	B095 B094 B093 B092 B091 B090	106
1010	01010	B105 B104 B103 B102 B101 B100	107
1011	01011	B115 B114 B113 B112 B111 B110	108
1100	01100	B125 B124 B123 B122 B121 B120	109
1101	01101	B135 B134 B133 B132 B131 B130	110
1110	01110	B145 B144 B143 B142 B141 B140	111
1111	01111	B155 B154 B153 B152 B151 B150	112
No Input	10000	B165 B164 B163 B162 B161 B160	113
No Input	10001	B175 B174 B173 B172 B171 B170	114
No Input	10010	B185 B184 B183 B182 B181 B180	115
No Input	10011	B195 B194 B193 B192 B191 B190	116
No Input	10100	B205 B204 B203 B202 B201 B200	117
No Input	10101	B215 B214 B213 B212 B211 B210	118
No Input	10110	B225 B224 B223 B222 B221 B220	119
No Input	10111	B235 B234 B233 B232 B231 B230	120
No Input	11000	B245 B244 B243 B242 B241 B240	121
No Input	11001	B255 B254 B253 B252 B251 B250	122
No Input	11010	B265 B264 B263 B262 B261 B260	123
No Input	11011	B275 B274 B273 B272 B271 B270	124
No Input	11100	B285 B284 B283 B282 B281 B280	125
No Input	11101	B295 B294 B293 B292 B291 B290	126
No Input	11110	B305 B304 B303 B302 B301 B300	127
No Input	11111	B315 B314 B313 B312 B311 B310	128

6. Display Data GRAM

The display data RAM stores display dots and consists of 384,912 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

6.1 Display data GRAM mapping

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

0000H	0001H	0002H	0003H	-----	0080H	0081H	0082H	0083H
0100H	0101H	0102H	0103H	-----	0180H	0181H	0182H	0183H
0200H	0201H	0202H	0203H	-----	0280H	0281H	0282H	0283H
0300H	0301H	0302H	0303H	-----	0380H	0381H	0382H	0383H
0400H	0401H	0402H	0403H	-----	0480H	0481H	0482H	0483H
0500H	0501H	0502H	0503H	-----	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	-----	⋮	⋮	⋮	⋮
9C00H	9C01H	9C02H	9C03H	-----	9C80H	9C81H	9C82H	9C83H
9D00H	9D01H	9D02H	9D03H	-----	9D80H	9D81H	9D82H	9D83H
9E00H	9E01H	9E02H	9E03H	-----	9E80H	9E81H	9E82H	9E83H
9F00H	9F01H	9F02H	9F03H	-----	9F80H	9F81H	9F82H	9F83H
A000H	A001H	A002H	A003H	-----	A080H	A081H	A082H	A083H
A100H	A101H	A102H	A103H	-----	A180H	A181H	A182H	A183H

Table 6.1 GRAM address for display panel position

6.2 Address counter (AC) of GRAM

The HX8353-E contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MADTCL's MV(B5), MX(B6) and MY(B7)** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the **CASET** (start: **SC**, end: **EC**) and the **PASET** (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

6.2.1 System interface to GRAM write direction

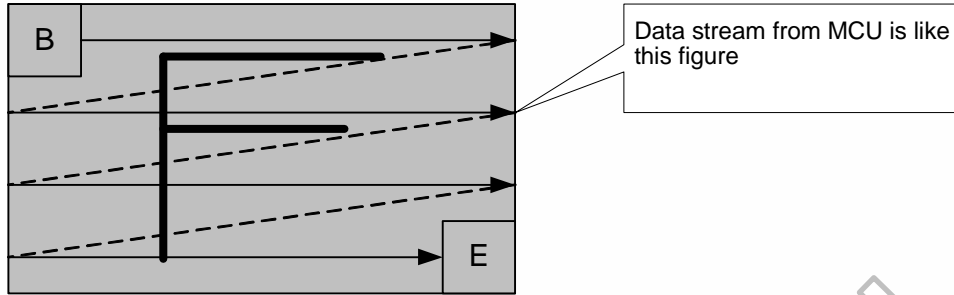


Figure 6.1 Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MADCTL's MV(B5), MX(B6) and MY(B7) bits setting**

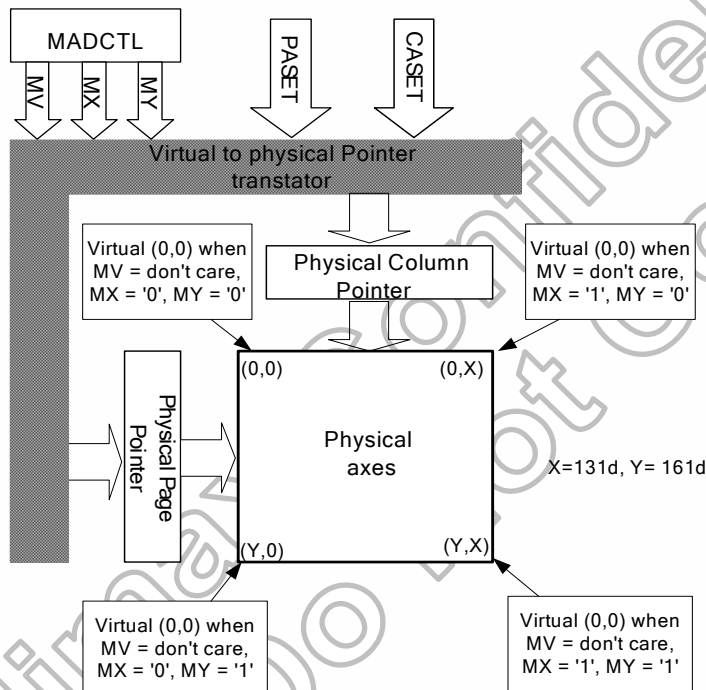


Figure 6.2 Image data writing control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6.2 CASET and PASET control for physical column/page pointers

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

Table 6.3 Rules for updating GRAM order

Himax Confidential
Do Not Copy

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display Data Direction	MADCTR parameter			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6.4 Address direction settings

Example for rotation with MY, MX and MV

This example is using following values: start page=0, end page=40, start column=0 and end column=20=> commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.

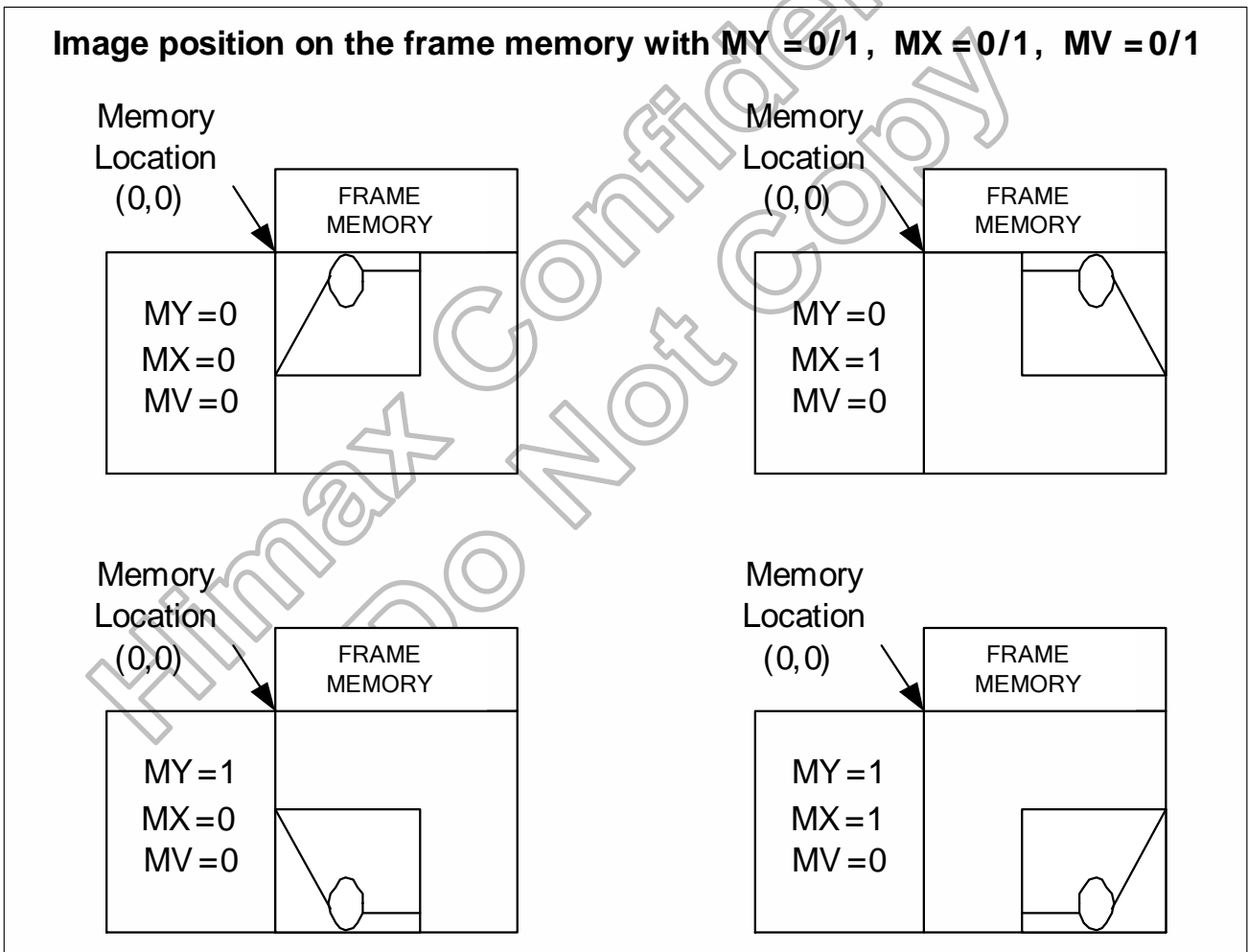
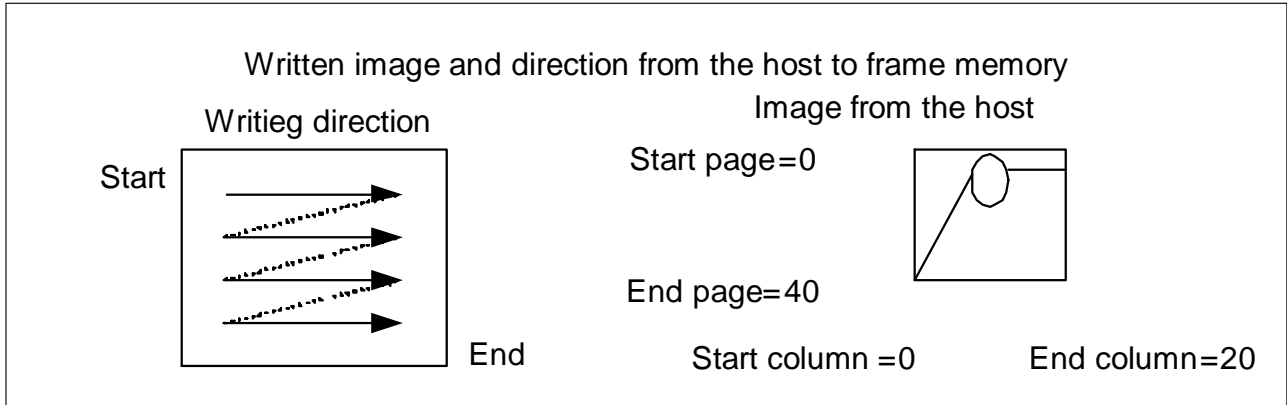


Figure 6.3 Example for rotation with MY, MX and MV – 1

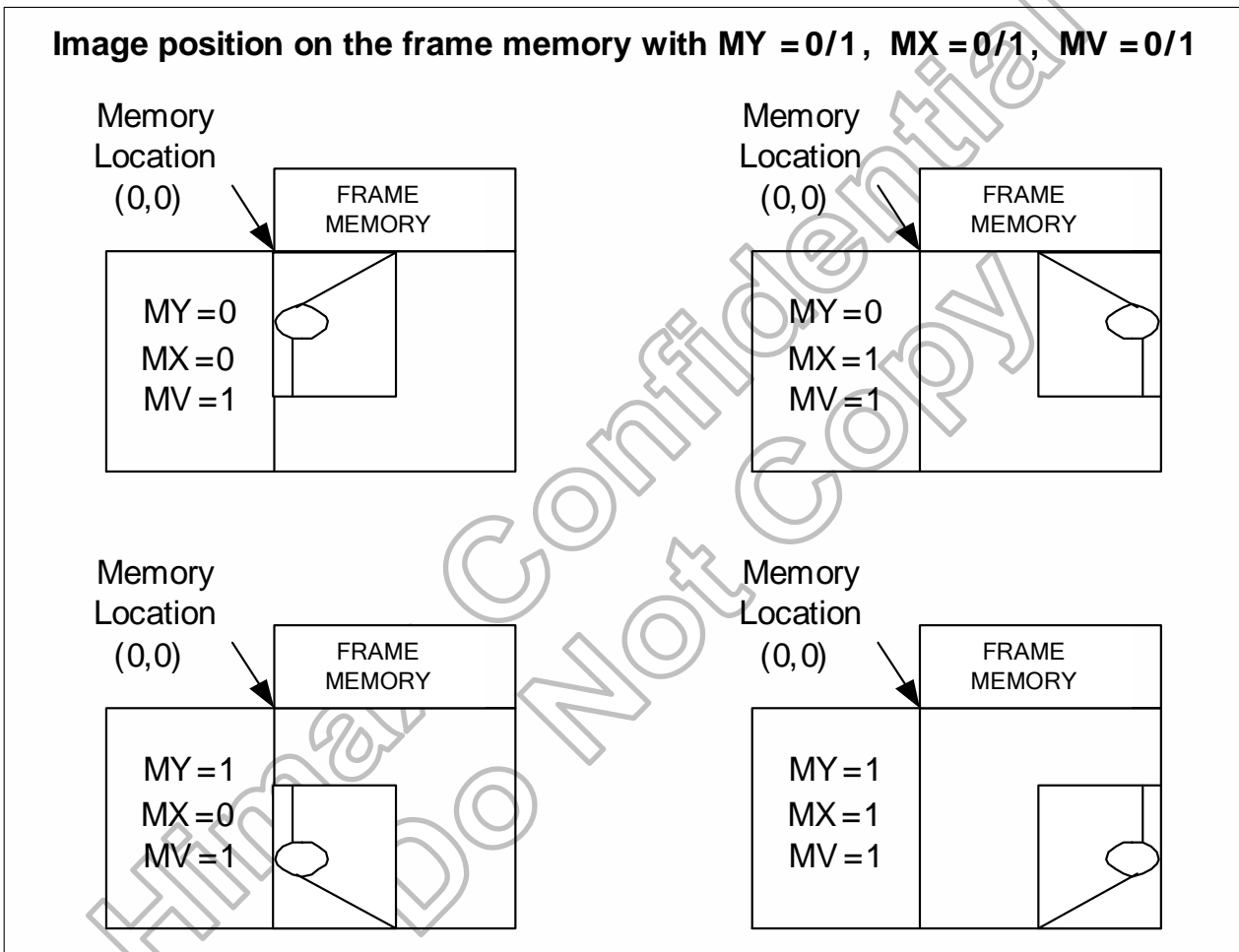
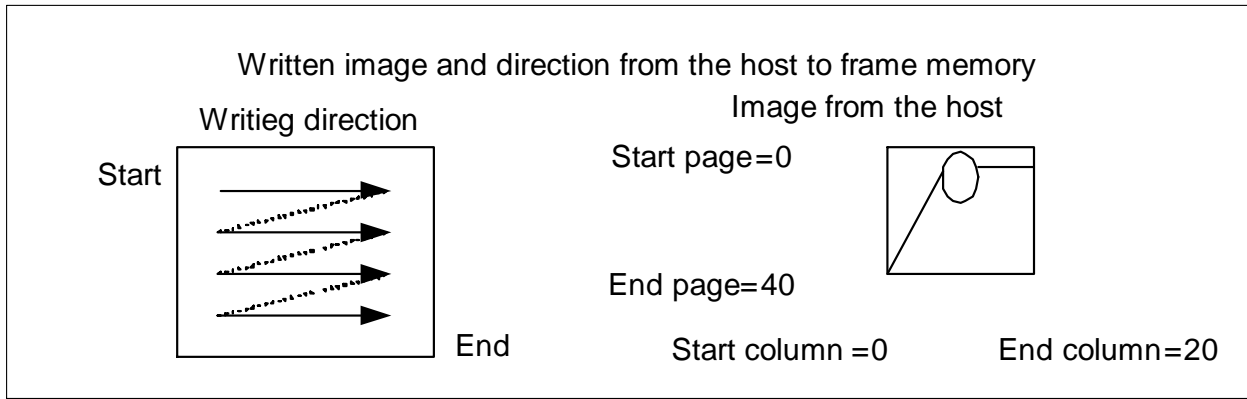
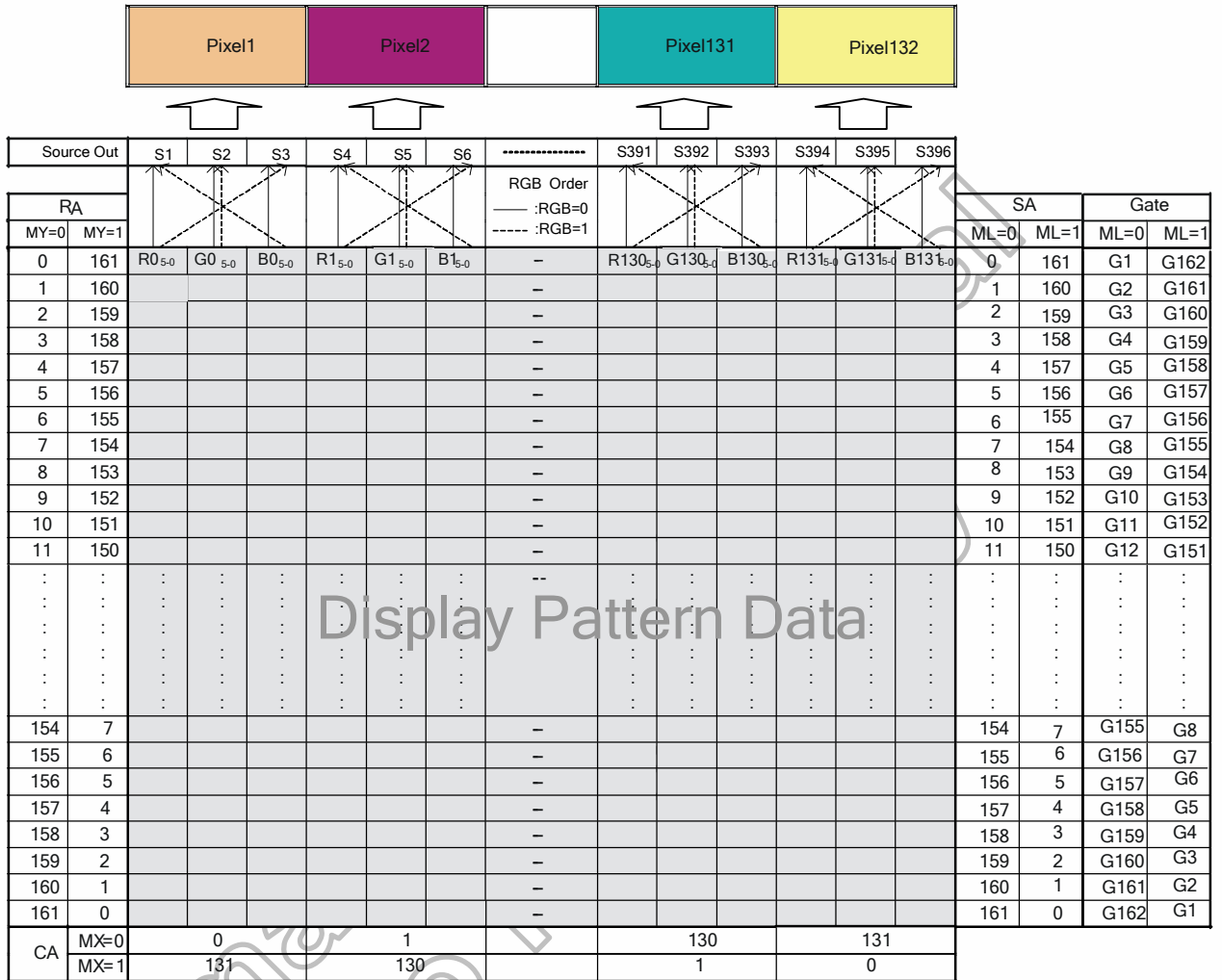


Figure 6.4 Example for rotation with MY, MX and MV – 2

6.3 Source, gate and memory map

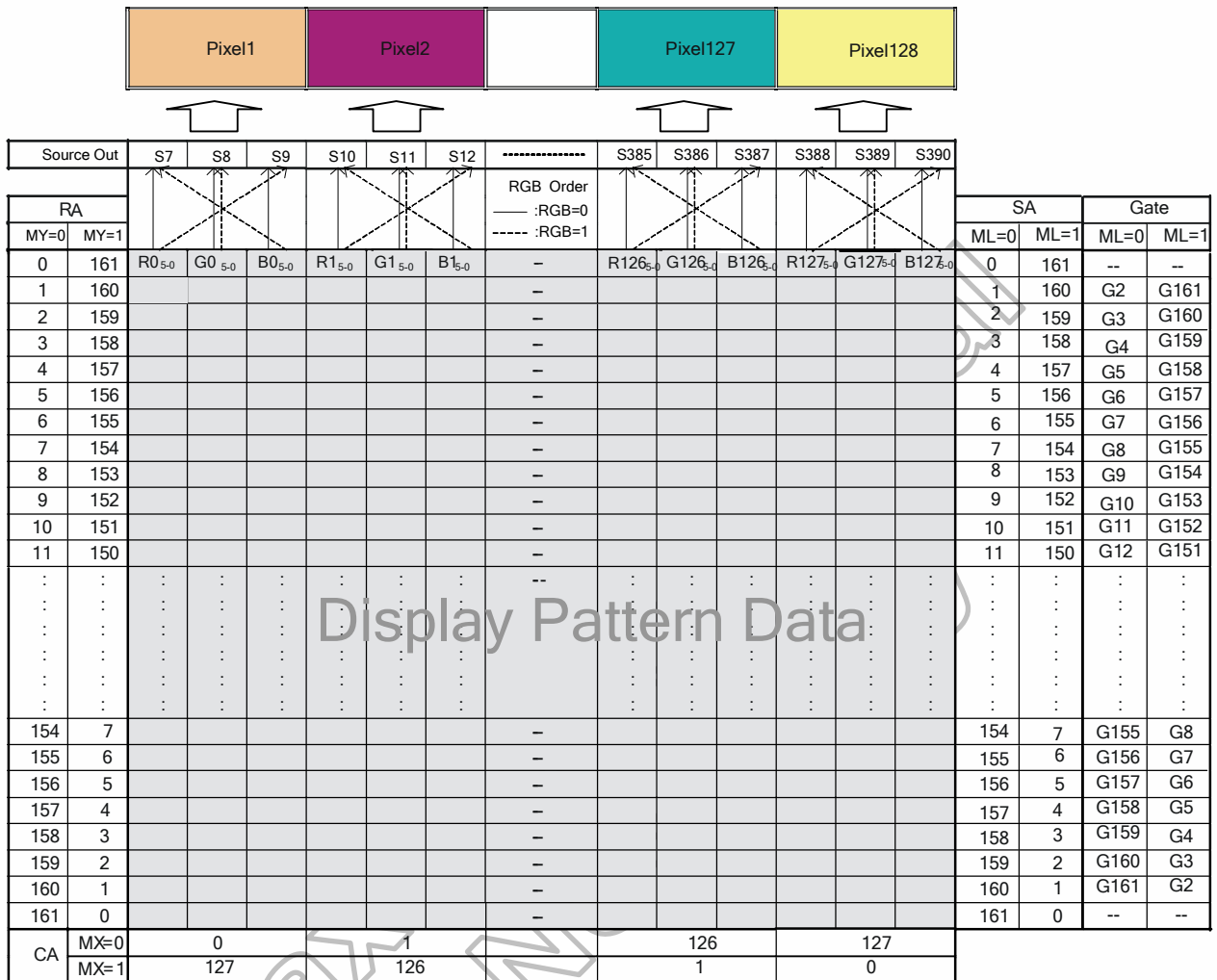
6.3.1 When using 132 x 162 GRAM resolution, display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.5 Memory map, 132 x 162 GRAM resolution, display resolution 132RGB x 162

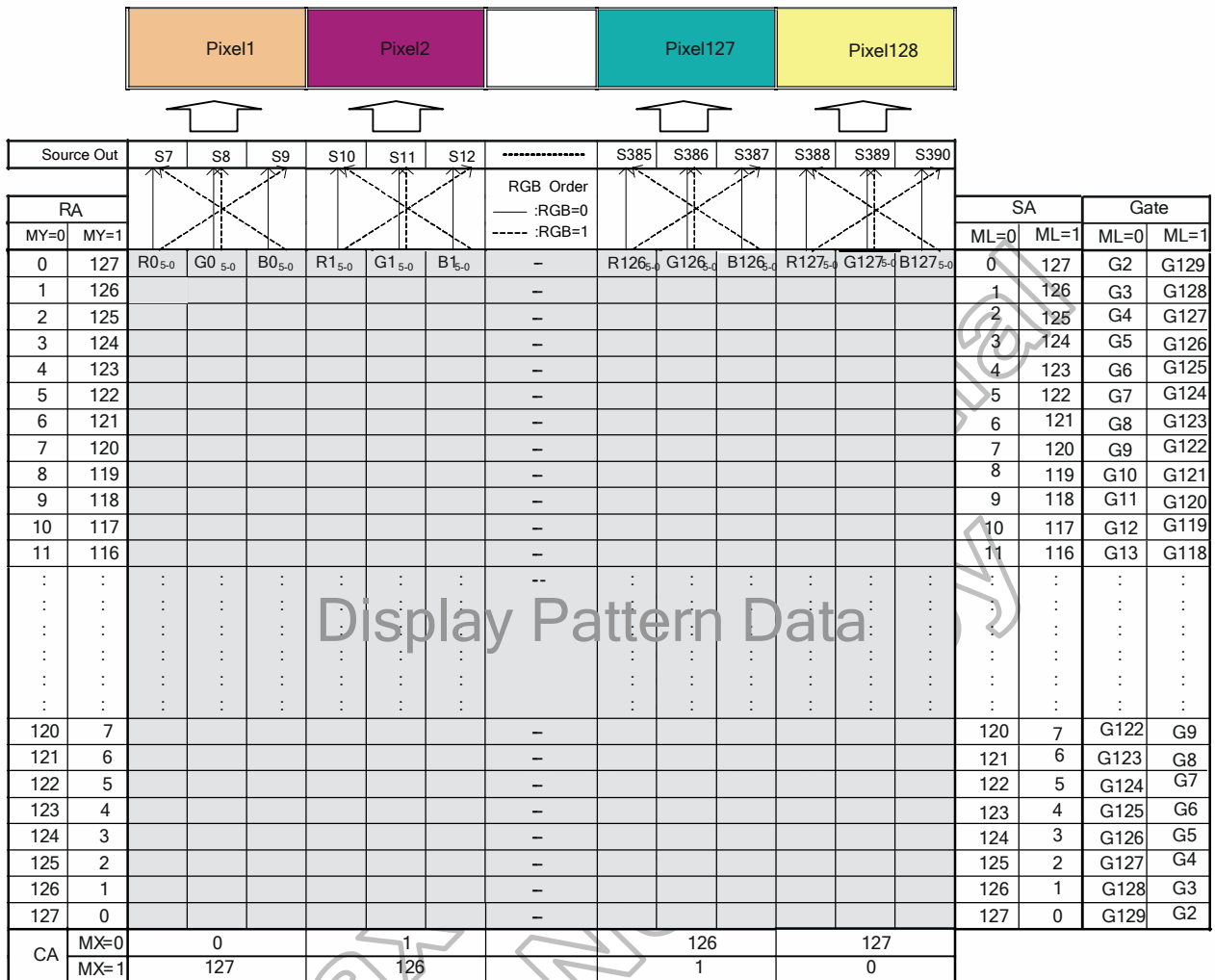
6.3.2 When using 132 x 162 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b000 & STE_SEL=1)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.6 Memory map, 132 x 162 GRAM resolution, display resolution 128RGB x 160

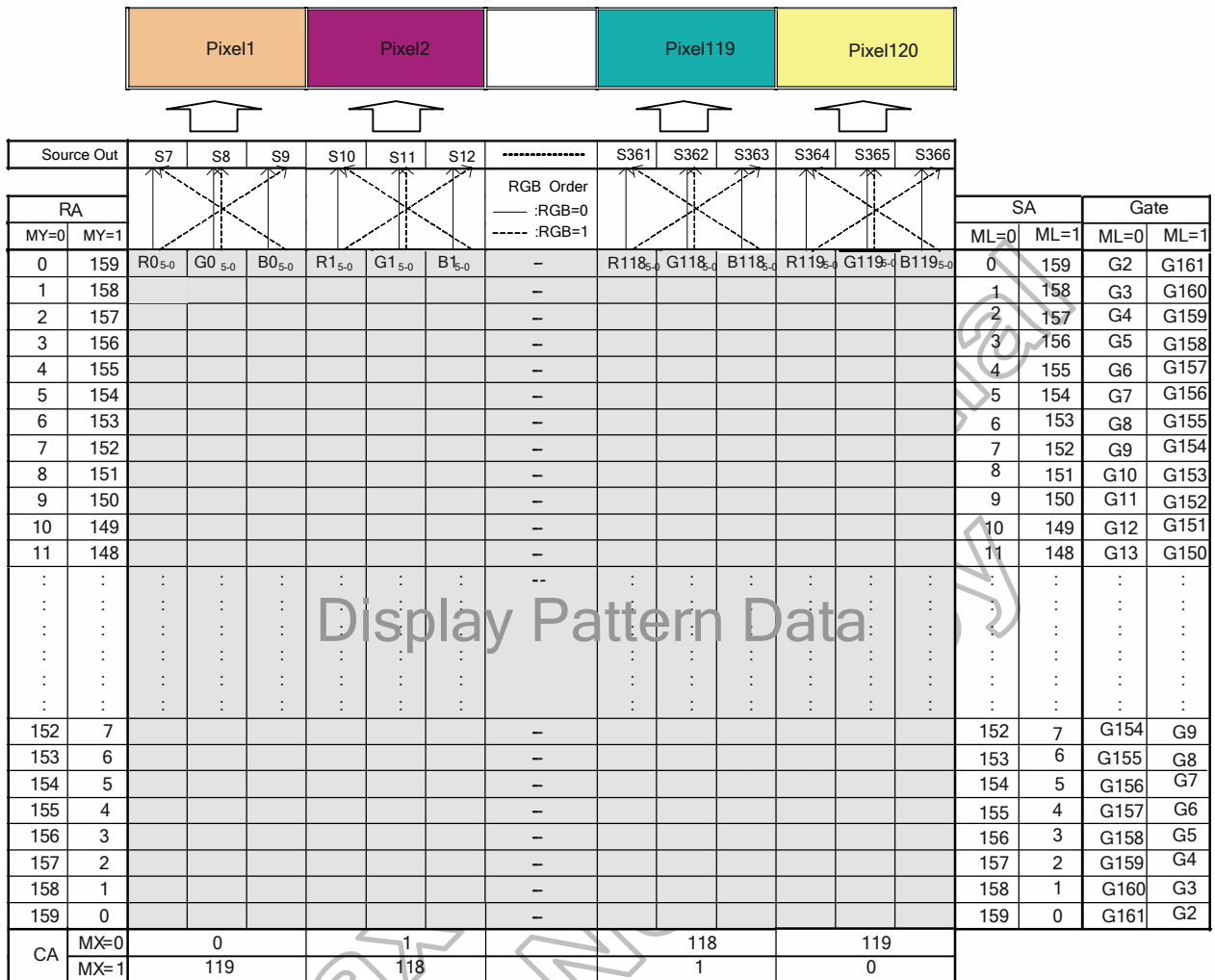
6.3.3 When using 128 x 128 GRAM resolution, display resolution 128RGB x 128 (RSO[2:0]=3'b001)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.7 Memory map, 128 x 128 GRAM resolution, display resolution 128RGB x 128

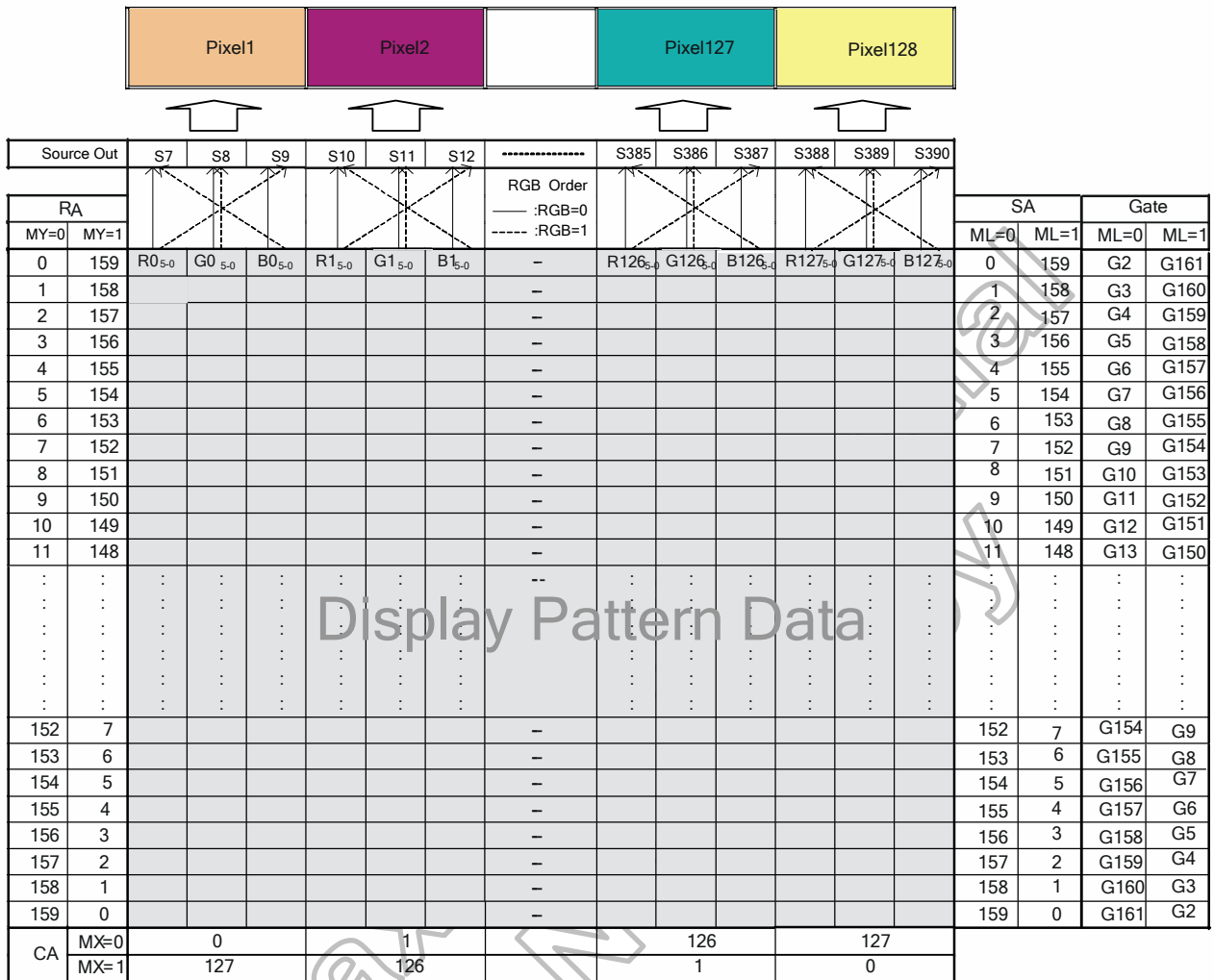
6.3.4 When using 120 x 160 GRAM resolution, display resolution 120RGB x 160 (RSO[2:0]=3'b010)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.8 Memory map, 120 x 160 GRAM resolution, display resolution 120RGB x 160

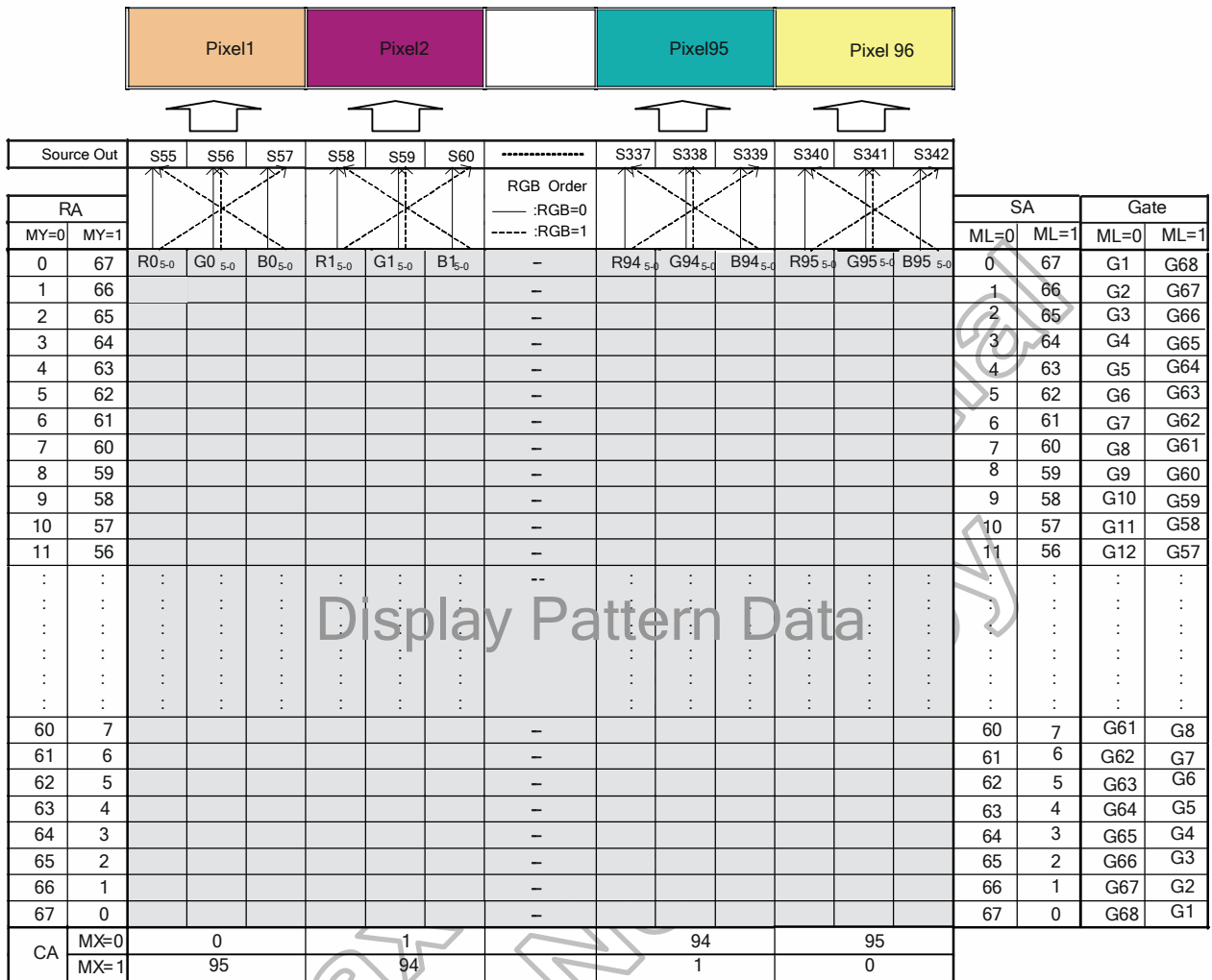
6.3.5 When using 128 x 160 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b011)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.9 Memory map, 128 x 160 GRAM resolution, display resolution 128RGB x 160

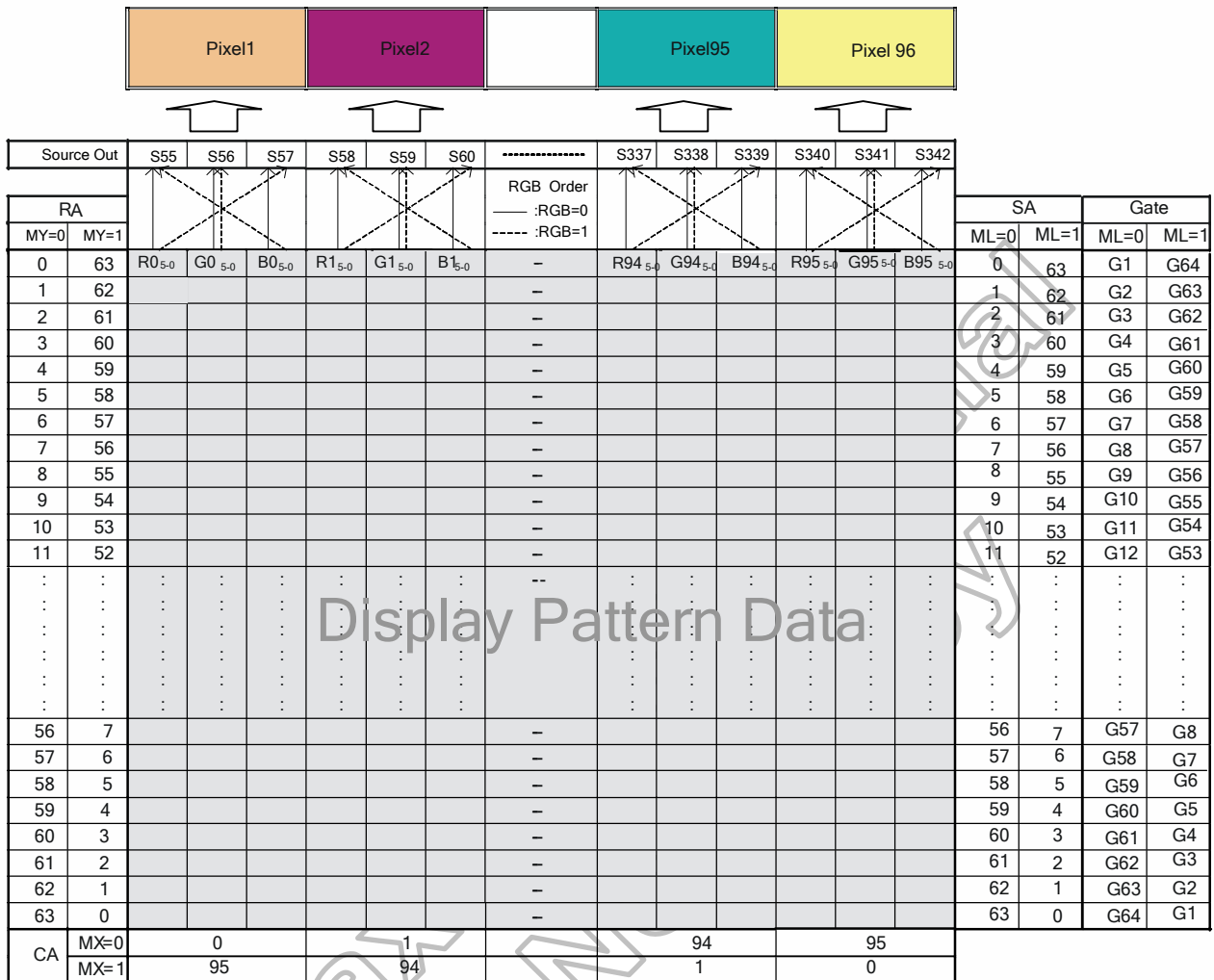
6.3.6 When using 96 x 68 GRAM resolution, display resolution 96RGB x 68 (RSO[2:0]=3'b100)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.10 Memory map, 96 x 68 GRAM resolution, display resolution 96RGB x 68

6.3.7 When using 96 x 64 GRAM resolution, display resolution 96RGB x 64 (RSO[2:0]=3'b101)



Note: RA = Row Address,
 CA = Column Address,
 SA = Scan Address,
 MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
 MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
 ML = Scan direction parameter, DB4 parameter of MADCTL command
 RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.11 Memory map, 96 x 64 GRAM resolution, display resolution 96RGB x 64

6.3.8 Normal display on or partial display on

The HX8353-E has an internal GRAM that store 48,114 bytes pattern data, where one pixel is expressed by 18 bits.

6.3.8.1 132X162 GRAM resolution (size) (display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	-----	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A180H	A181H	A182H	A183H

LCD panel S/G pins	S1	S2	S3	-----	S394	S395	S396
	G1	0000H			-----		
G2	0100H			-----			0183H
G3	0200H			-----			0283H
G4	0300H			-----			0383H
G5	0400H			-----			0483H
G6	0500H			-----			0583H
⋮	⋮			-----			⋮
G157	9C00H			-----			9C83H
G158	9D00H			-----			9D83H
G159	9E00H			-----			9E83H
G160	9F00H			-----			9F83H
G161	A000H			-----			A083H
G162	A100H			-----			A183H

Table 6.5 132X162 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Fh, ML=0.

GRAM	00h	01h	02h	03h	-----	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0580H	0581H	0582H	0583H

9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A180H	A181H	A182H	A183H

LCD panel S/G pins	S1	S2	S3	-----	S394	S395	S396
	Non-displa y area 2	G1	0000H	-----	-----	0083H	
	G2	0100H	-----	-----	0183H		
	G3	0200H	-----	-----	0283H		
	G4	0300H	-----	-----	0383H		
	G5	0400H	-----	-----	0483H		
	G6	0500H	-----	-----	0583H		
Display area 158 lines			-----	-----			
	G157	9C00H	-----	-----	9C83H		
	G158	9D00H	-----	-----	9D83H		
	G159	9E00H	-----	-----	9E83H		
	G160	9F00H	-----	-----	9F83H		
Non-display area 2 lines	G161	A000H	-----	-----	A083H		
	G162	A100H	-----	-----	A183H		

Table 6.6 Partial area of 132X162 GRAM resolution

6.3.8.2 132X162 GRAM resolution (size) (display resolution 128RGB x 160 (RSO[2:0]=3'b000 & STE_SEL=1))

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	-----	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A180H	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	-----	S388	S389	S390
	G2		0102H		-----		0181H
G3		0202H		-----		0281H	
G4		0302H		-----		0381H	
G5		0402H		-----		0481H	
G6		0502H		-----		0581H	
G7		0602H		-----		0681H	
⋮		⋮		-----		⋮	
G158		9D02H		-----		9D81H	
G159		9E02H		-----		9E81H	
G160		9F02H		-----		9F81H	
G161		A002H		-----		A081H	

Table 6.7 132X162 GRAM resolution and 128X160 display resolution

(b) Partial display on

PSL[15:0]=03h, PEL[15:0]=9Eh, ML=0.

GRAM	00h	01h	02h	03h	-----	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0580H	0581H	0582H	0583H

9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	-----	S388	S389	S390
		Non-display area 2 lines	G2	0102H	-----	0181H	G3	0202H
Display area 156 lines	G4	0302H	-----	0381H	G5	0402H	-----	0481H
	G6	0502H	-----	0581H	G7	0602H	-----	0681H
			-----				-----	
	G158	9D02H	-----	9D81H	G159	9E02H	-----	9E81H
	G160	9F02H	-----	9F81H	G161	A002H	-----	A081H
Non-display area 2 lines			-----				-----	

Table 6.8 Partial area of 132X162 GRAM resolution and 128X160 display resolution

6.3.8.3 128X128 GRAM resolution (size) (display resolution 128RGB x 128 → RSO[2:0]=3'b001)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 7Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	-----	7Fh	-----	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	007FH	-----	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	017FH	-----	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	027FH	-----	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	037FH	-----	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	047FH	-----	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	057FH	-----	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
7Eh	7E00H	7E01H	7E02H	7E03H	-----	7E7FH	-----	7E81H	7E82H	7E83H
7Fh	7F00H	7F01H	7F02H	7F03H	-----	7E7FH	-----	7F81H	7F82H	7F83H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C7FH	-----	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D7FH	-----	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E7FH	-----	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F7FH	-----	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A07FH	-----	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A17FH	-----	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	-----	S388	S389	S390
	G2	0000H			-----		
G3	0100H			-----			017FH
G4	0200H			-----			027FH
G5	0300H			-----			037FH
G6	0400H			-----			047FH
G7	0500H			-----			057FH
⋮	⋮			-----			⋮
G126	7C00H			-----			7C7FH
G127	7D00H			-----			7D7FH
G128	7E00H			-----			7E7FH
G129	7F00H			-----			7F7FH

Table 6.9 128X128 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=7Dh, ML=0.

GRAM	00h	01h	02h	03h	-----	7Fh	-----	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	007FH	-----	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	017FH	-----	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	027FH	-----	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	037FH	-----	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	047FH	-----	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	057FH	-----	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
7Eh	7E00H	7E01H	7E02H	7E03H	-----	7E7FH	-----	7E81H	7E82H	7E83H
7Fh	7F00H	7F01H	7F02H	7F03H	-----	7E7FH	-----	7F81H	7F82H	7F83H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C7FH	-----	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D7FH	-----	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E7FH	-----	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F7FH	-----	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A07FH	-----	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A17FH	-----	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	-----	S387	S389	S390
		Non-display area 2 lines	G2	0000H	-----	-----	-----	007FH
	G3	0100H	-----	-----	-----	017FH		
	G4	0200H	-----	-----	-----	027FH		
	G5	0300H	-----	-----	-----	037FH		
	G6	0400H	-----	-----	-----	047FH		
Display area 124 lines	G7	0500H	-----	-----	-----	057FH		
	⋮	⋮	-----	-----	-----	⋮		
	G126	7C00H	-----	-----	-----	7C7FH		
	G127	7D00H	-----	-----	-----	7D7FH		
Non-display area 2 lines	G128	7E00H	-----	-----	-----	7E7FH		
	G129	7F00H	-----	-----	-----	7F7FH		

Table 6.10 Partial area of 128X128 GRAM resolution

6.3.8.4 120X160 GRAM resolution (size) (display resolution 120RGB x 160 → RSO[2:0]=3'b010)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	-----	77h	-----	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0077H	-----	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0177H	-----	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0277H	-----	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0377H	-----	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0477H	-----	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0577H	-----	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C77H	-----	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D77H	-----	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E77H	-----	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F77H	-----	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A077H	-----	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A177H	-----	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	-----	S364	S365	S366
	G2	0000H	-----	-----	-----	0077H	-----
G3	0100H	-----	-----	-----	0177H	-----	-----
G4	0200H	-----	-----	-----	0277H	-----	-----
G5	0300H	-----	-----	-----	0377H	-----	-----
G6	0400H	-----	-----	-----	0477H	-----	-----
G7	0500H	-----	-----	-----	0577H	-----	-----
⋮	⋮	-----	-----	-----	⋮	-----	-----
G158	9C00H	-----	-----	-----	9C77H	-----	-----
G159	9D00H	-----	-----	-----	9D77H	-----	-----
G160	9E00H	-----	-----	-----	9E77H	-----	-----
G161	9F00H	-----	-----	-----	9F77H	-----	-----

Table 6.11 120X160 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

GRAM	00h	01h	02h	03h	-----	77h	-----	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	0077H	-----	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	0177H	-----	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	0277H	-----	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	0377H	-----	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	0477H	-----	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	0577H	-----	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	-----	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C77H	-----	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D77H	-----	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E77H	-----	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F77H	-----	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A077H	-----	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A177H	-----	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	-----	S364	S365	S366
		Non-display area 2 lines	G2	0000H	-----	0077H		
	G3	0100H	-----	0177H				
Display area 156 lines	G4	0200H	-----	0277H				
	G5	0300H	-----	0377H				
	G6	0400H	-----	0477H				
	G7	0500H	-----	0577H				
	⋮	⋮	⋮	-----	⋮	⋮	⋮	
Non-display area 2 lines	G158	9C00H	-----	9C77H				
	G159	9D00H	-----	9D77H				
	G160	9E00H	-----	9E77H				
	G161	9F00H	-----	9F77H				

Table 6.12 Partial area of 120X160 GRAM resolution

6.3.8.5 128X160 GRAM resolution (size) (display resolution 128RGB x 160 (RSO[2:0]=3'b011))

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	-----	7Fh	80h	81h	82h	83h
	DB---DB 17---0	DB---DB 17---0	DB---DB 17---0	DB---DB 17---0	-----	DB---DB 17---0	DB---DB 17---0	DB---DB 17---0	DB---DB 17---0	DB---DB 17---0
00h	0000H	0001H	0002H	0003H	-----	007FH	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	017FH	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	027FH	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	037FH	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	047FH	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	057FH	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C7FH	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D7FH	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E7FH	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F7FH	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A07FH	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A17FH	A180H	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	-----	S388	S389	S390
	G2	0000H	-----	-----	-----	007FH	
G3	0100H	-----	-----	-----	017FH		
G4	0200H	-----	-----	-----	027FH		
G5	0300H	-----	-----	-----	037FH		
G6	0400H	-----	-----	-----	047FH		
G7	0500H	-----	-----	-----	057FH		
⋮	⋮	-----	-----	-----	⋮		
G158	9C00H	-----	-----	-----	9C7FH		
G159	9D00H	-----	-----	-----	9D7FH		
G160	9E00H	-----	-----	-----	9E7FH		
G161	9F00H	-----	-----	-----	9F7FH		

Table 6.13 128X160 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

GRAM	00h	01h	02h	03h	-----	7Fh	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	-----	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	-----	007FH	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	-----	017FH	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	-----	027FH	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	-----	037FH	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	-----	047FH	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	-----	057FH	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	-----	⋮	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	-----	9C7FH	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	-----	9D7FH	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	-----	9E7FH	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	-----	9F7FH	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	-----	A07FH	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	-----	A17FH	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	-----	S388	S389	S390

Non-display area 2 lines	G2	0000H	-----	007FH				
	G3	0100H	-----	017FH				
Display area 156 lines	G4	0200H	-----	027FH				
	G5	0300H	-----	037FH				
	G6	0400H	-----	047FH				
	G7	0500H	-----	057FH				
	⋮	⋮	-----	⋮				
Non-display area 2 lines	G158	9C00H	-----	9C7FH				
	G159	9D00H	-----	9D7FH				
	G160	9E00H	-----	9E7FH				
	G161	9F00H	-----	9F7FH				

Table 6.14 Partial area of 128X160 GRAM resolution

6.3.8.6 96x68 Resolution (RSO[2:0]=3'b100)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	---	5Dh	5Eh	5Fh	---	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
42h	4200H	4201H	4202H	4203H	---	425DH	425EH	425FH	---	4280H	4281H	4282H	4283H
43h	4300H	4301H	4302H	4303H	---	435DH	435EH	435FH	---	4380H	4381H	4382H	4383H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

LCD panel S/G pins	S55	S56	S57	S340	S341	S342
	G1	0000H	-----	-----	005FH	-----
G2	0100H	-----	-----	015FH	-----	-----
G3	0200H	-----	-----	025FH	-----	-----
G4	0300H	-----	-----	035FH	-----	-----
G5	0400H	-----	-----	045FH	-----	-----
G6	0500H	-----	-----	055FH	-----	-----
⋮	⋮	⋮	⋮	⋮	⋮	⋮
G67	4200H	-----	-----	425FH	-----	-----
G68	4300H	-----	-----	435FH	-----	-----

Table 6.15 96X68 GRAM resolution

(b) Partial display on

PSL[15:0]=02, PEL[15:0]=41, ML=0.

GRAM	00h	01h	02h	03h	...	5Dh	5Eh	5Fh	...	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	...	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	...	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	...	005DH	005EH	005FH	...	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	...	015DH	015EH	015FH	...	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	...	025DH	025EH	025FH	...	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	...	035DH	035EH	035FH	...	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	...	045DH	045EH	045FH	...	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	...	055DH	055EH	055FH	...	0580H	0581H	0582H	0583H
...
41h	4100H	4101H	4102H	4103H	...	415DH	415EH	415FH	...	4180H	4181H	4182H	4183H
42h	4200H	4201H	4202H	4203H	...	425DH	425EH	425FH	...	4280H	4281H	4282H	4283H
43h	4300H	4301H	4302H	4303H	...	435DH	435EH	435FH	...	4380H	4381H	4382H	4383H
...
9Ch	9C00H	9C01H	9C02H	9C03H	...	9C5DH	9C5EH	9C5FH	...	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	...	9D5DH	9D5EH	9D5FH	...	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	...	9E5DH	9E5EH	9E5FH	...	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	...	9F5DH	9F5EH	9F5FH	...	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	...	A05DH	A05EH	A05FH	...	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	...	A15DH	A15EH	A15FH	...	A180H	A181H	A182H	A183H

LCD panel S/G pins	S55	S56	S57	S340	S341	S342
	G1	0000H	-----	-----	005FH	-----
G2	0100H	-----	-----	015FH	-----	-----
G3	0200H	-----	-----	025FH	-----	-----
G4	0300H	-----	-----	035FH	-----	-----
G5	0400H	-----	-----	045FH	-----	-----
G6	0500H	-----	-----	055FH	-----	-----
...
G66	4100H	-----	-----	415FH	-----	-----
G67	4200H	-----	-----	425FH	-----	-----
G68	4300H	-----	-----	435FH	-----	-----

Table 6.16 Partial area of 96X68 GRAM resolution

6.3.8.7 96x64 resolution (RSO[2:0]=3'b101)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h	01h	02h	03h	---	5Dh	5Eh	5Fh	---	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
3Fh	3F00H	3F01H	3F02H	3F03H	---	3F5DH	3F5EH	3F5FH	---	3F80H	3F81H	3F82H	3F83H
40h	4000H	4001H	4002H	4003H	---	405DH	405EH	405FH	---	4080H	4081H	4082H	4083H
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

LCD panel S/G pins	S55	S56	S57	S340	S341	S342
	G1	0000H	-----	-----	005FH	-----
G2	0100H	-----	-----	015FH	-----	-----
G3	0200H	-----	-----	025FH	-----	-----
G4	0300H	-----	-----	035FH	-----	-----
G5	0400H	-----	-----	045FH	-----	-----
G6	0500H	-----	-----	055FH	-----	-----
⋮	⋮	⋮	⋮	⋮	⋮	⋮
G63	3E00H	-----	-----	3E5FH	-----	-----
G64	3F00H	-----	-----	3F5FH	-----	-----

Table 6.17 96X64 GRAM resolution

(b) Partial display on

PSL[15:0]=02, PEL[15:0]=3D, ML=0.

GRAM	00h	01h	02h	03h	---	5Dh	5Eh	5Fh	---	80h	81h	82h	83h
	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	---	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0	DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
...	---	---
3Fh	3F00H	3F01H	3F02H	3F03H	---	3F5DH	3F5EH	3F5FH	---	3F80H	3F81H	3F82H	3F83H
40h	4000H	4001H	4002H	4003H	---	405DH	405EH	405FH	---	4080H	4081H	4082H	4083H
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
...	---	---
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S55	S56	S57	S340	S341	S342
		Non-display area 2 lines	G1	0000H	-----	005FH	
	G2	0100H	-----	015FH			
	G3	0200H	-----	025FH			
	G4	0300H	-----	035FH			
	G5	0400H	-----	045FH			
Display area 60 lines	G6	0500H	-----	055FH			
			
	G63	3E00H	-----	3E5FH			
Non-display area 2 lines	G64	3F00H	-----	3F5FH			

Table 6.18 Partial area of 96X64 GRAM resolution

6.4 Vertical scrolling display

The vertical scrolling display is specified by SCRLAR instruction (R33h) and VSCSAD instruction (R37h). The Vertical scrolling is only enable when using 132 x 162 GRAM resolution, display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0) and display resolution 128RGB x 160 (RSO[2:0]=3'b011)

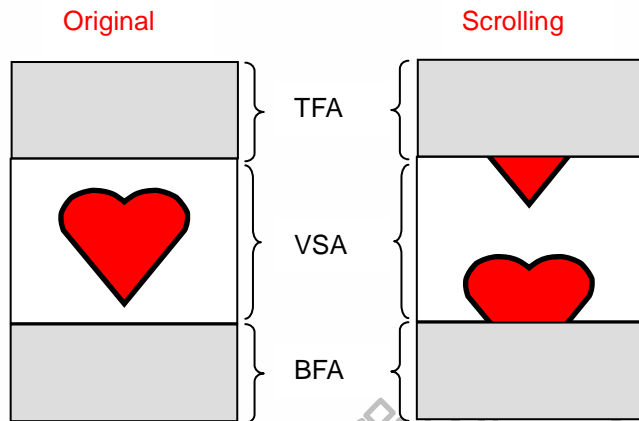


Figure 6.12 Vertical scrolling display

Himax Confidential
Do Not Copy

When RSO[2:0]=3'b000(132RGB x 162) and Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=162 (other setting is prohibited). In this case, scrolling is applied as shown below.

Example 1: RSO=3'b000(132RGB x 162), TFA =3, VSA=157, BFA=2, VSP=4, MADCTR(ML)=0: Scrolling

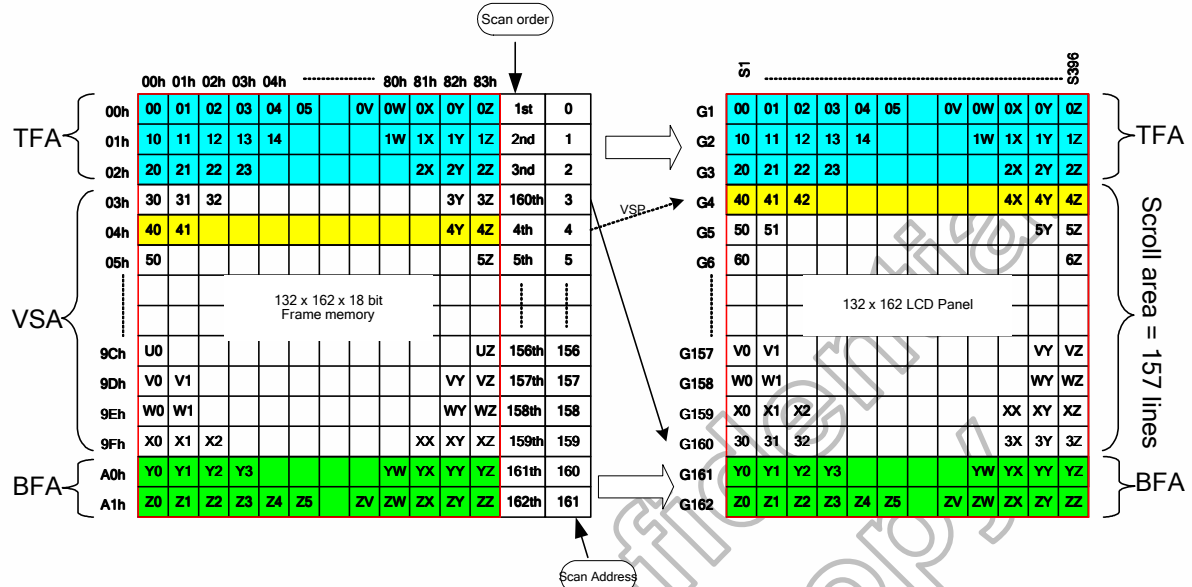


Figure 6.13 Example1 of scrolling

Example 2: RSO=3'b000(132RGB x 162), TFA =3, VSA=157, BFA=2, VSP=4, MADCTR (ML)=1: Scrolling (TFA and BFA are exchanged)

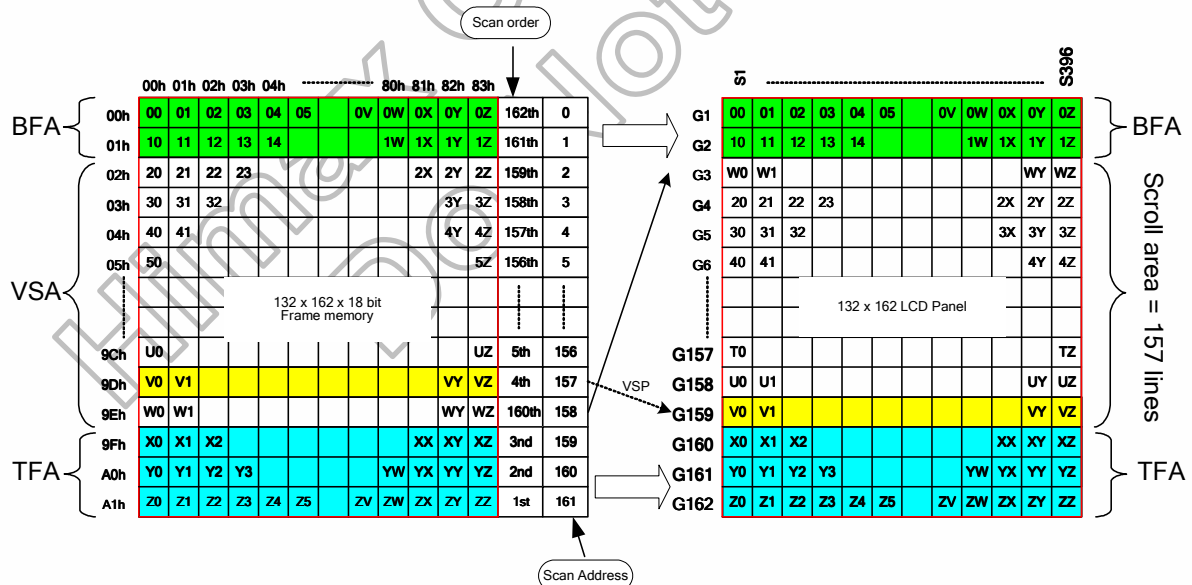


Figure 6.14 Example2 of scrolling

7. Functional Description

7.1 Internal Oscillator

The HX8353-E can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is $\pm 5\%$, it can be adjusted by the **RADJ [3:0]** bits for initial 6MHz internal clock generation. With other dividers setting, the 6MHz internal clock can be used to generate clock for other part of the chip using.

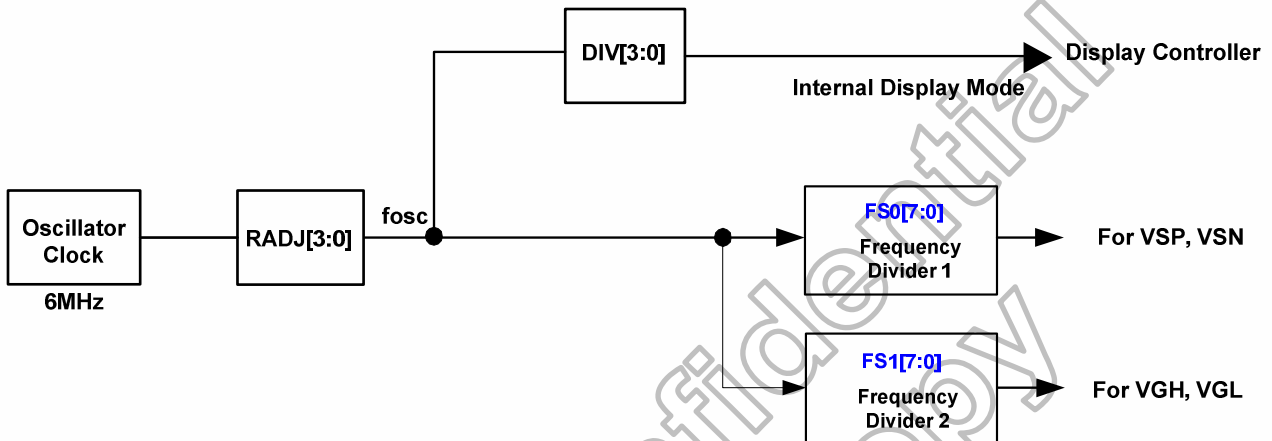


Figure 7.1 HX8353-E internal clock circuit

7.2 Gamma characteristic correction function

The HX8353-E incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

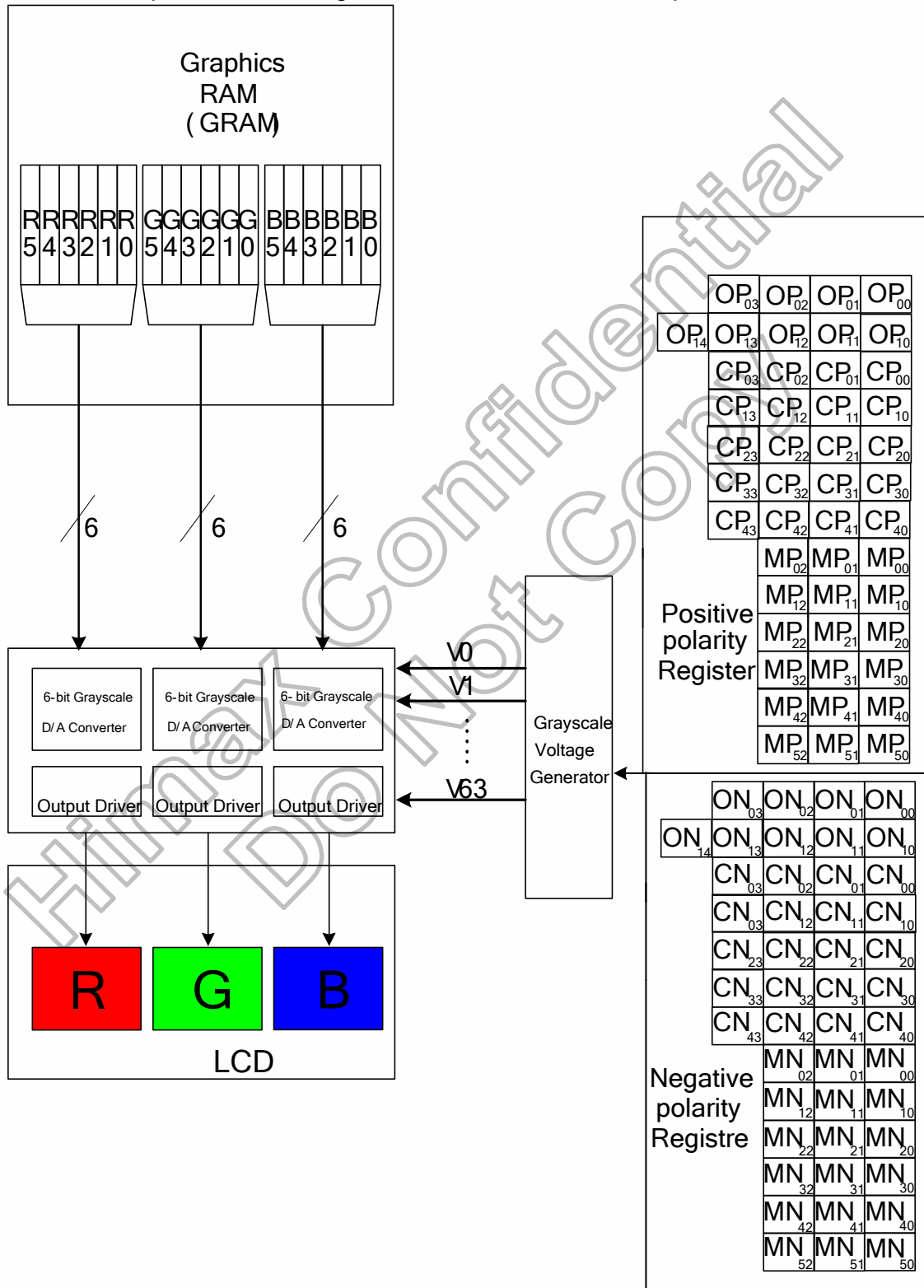
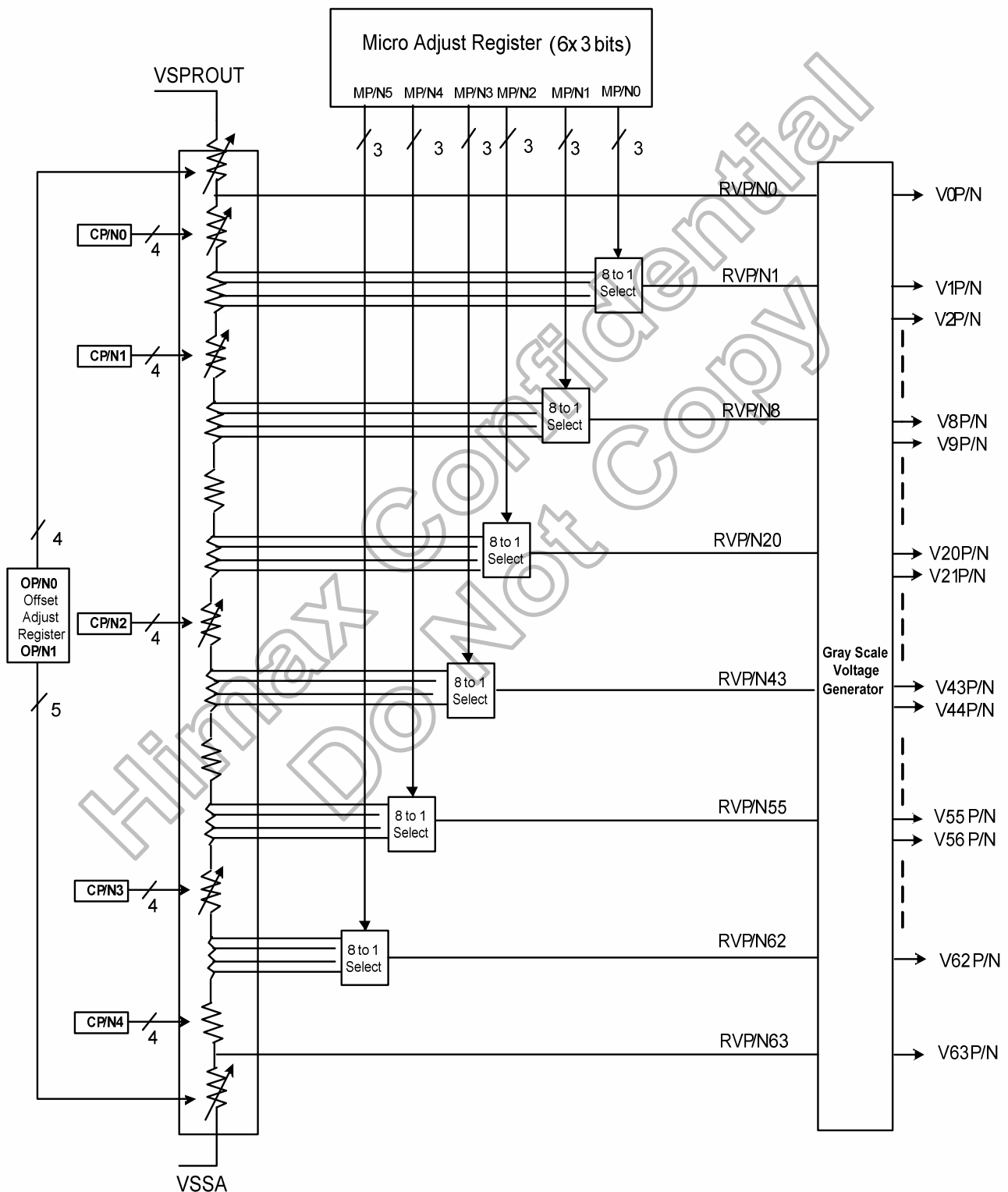


Figure 7.2 Grayscale control

7.2.1 Structure of grayscale voltage generator

Eight reference gamma voltages $V_{gP/N}(0, 1, 8, 20, 43, 55, 62, 63)$ for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages (V_0-V_{63}) can be generated from grayscale amplifier for LCD panel.



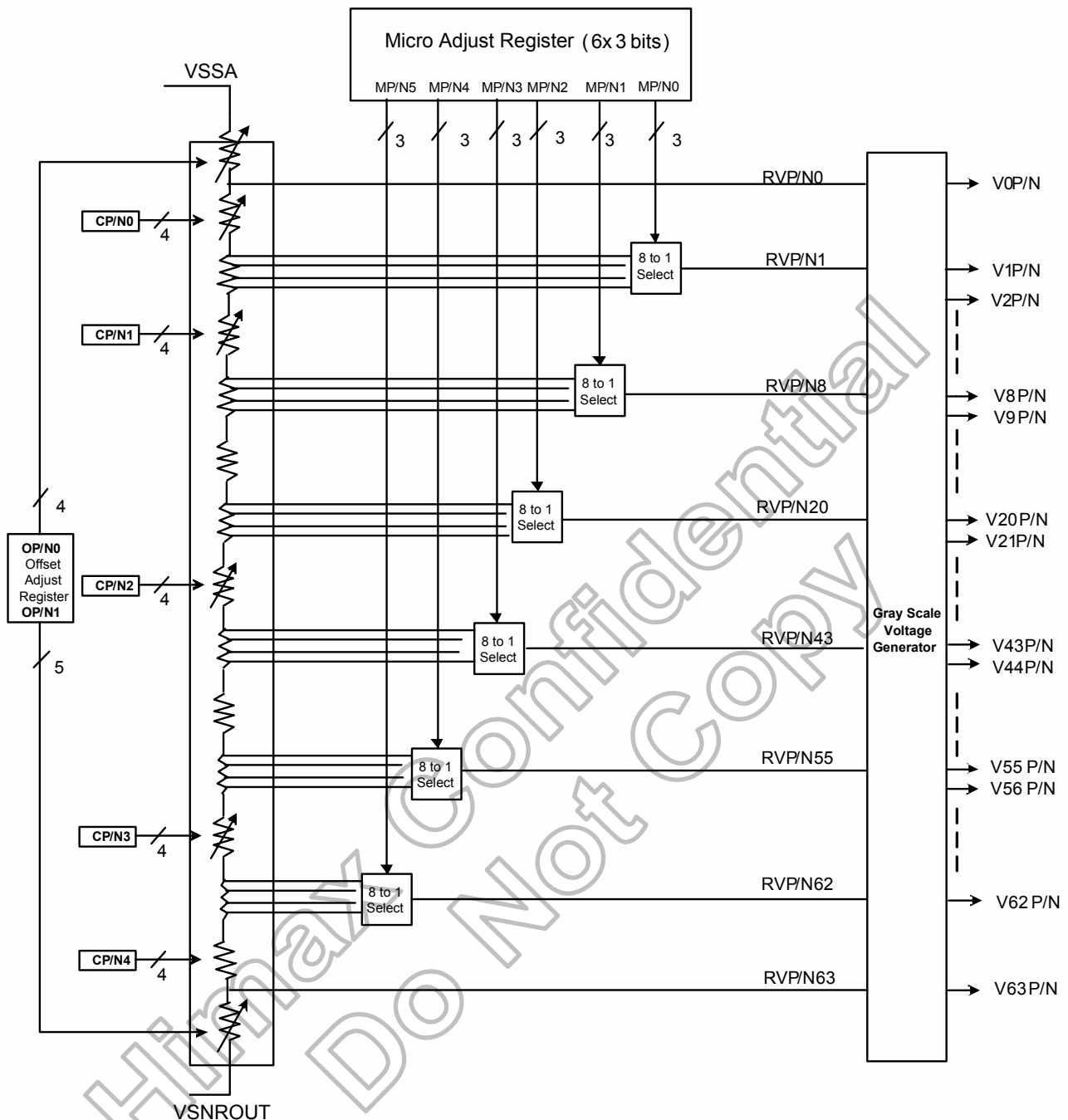


Figure 7.3 Structure of grayscale voltage Positive and Negative Generator

7.2.2 Gamma-characteristics adjustment register

This HX8353-E has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

7.2.2.1 Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

7.2.2.2 Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by controlling these variable resistors in center of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

7.2.2.3 Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (RVP/N 0, 1, 8, 20, 44, 56, 63, 64). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Description
Center Adjustment	CP/N0 3-0	Variable resistor (VRTP/N) for center adjustment
	CP/N1 3-0	Variable resistor (VRCP/N0)for center adjustment
	CP/N2 3-0	Variable resistor (VRMP/N) for center adjustment
	CP/N3 3-0	Variable resistor (VRCP/N1)for center adjustment
	CP/N4 3-0	Variable resistor (VRBP/N)for center adjustment
Macro Adjustment	MP/N0 2-0	8-to-1 selector (reference voltage level of grayscale 1)
	MP/N1 2-0	8-to-1 selector (reference voltage level of grayscale 8)
	MP/N2 2-0	8-to-1 selector (reference voltage level of grayscale 20)
	MP/N3 2-0	8-to-1 selector (reference voltage level of grayscale 43)
	MP/N4 2-0	8-to-1 selector (reference voltage level of grayscale 55)
Offset Adjustment	OP/N0 3-0	Variable resistor (VRP/N0)for offset adjustment
	OP/N1 4-0	Variable resistor (VRP/N1)for offset adjustment

Table 7.1 Gamma-adjustment registers

7.2.3 Gamma resistor stream and 8 to 1 selector

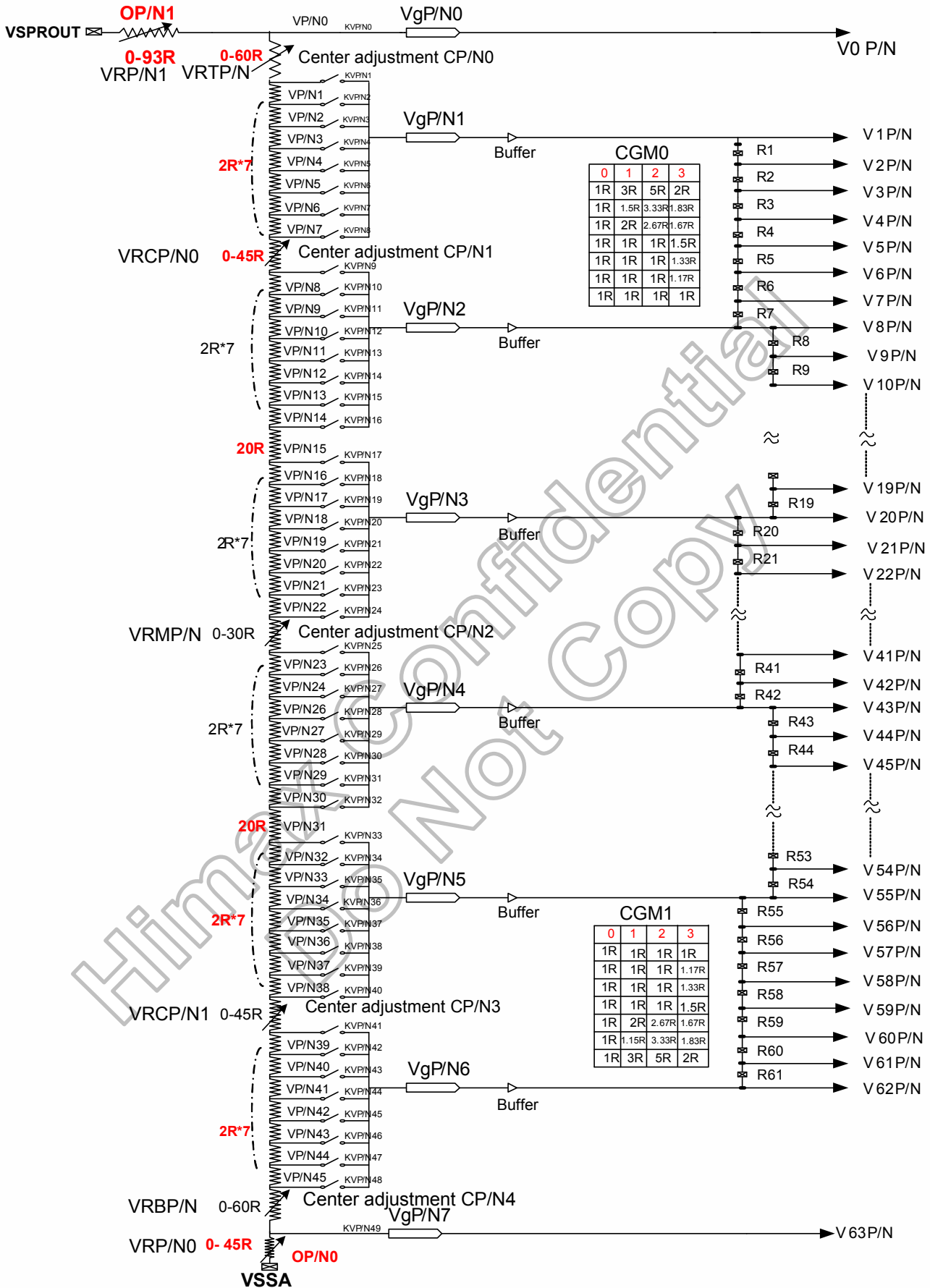
The block consists of two gamma resistor streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63).

HX8353-E

132RGB x 162 dots, 262K Color, TFT Mobile Single Chip Driver



DATA SHEET V01



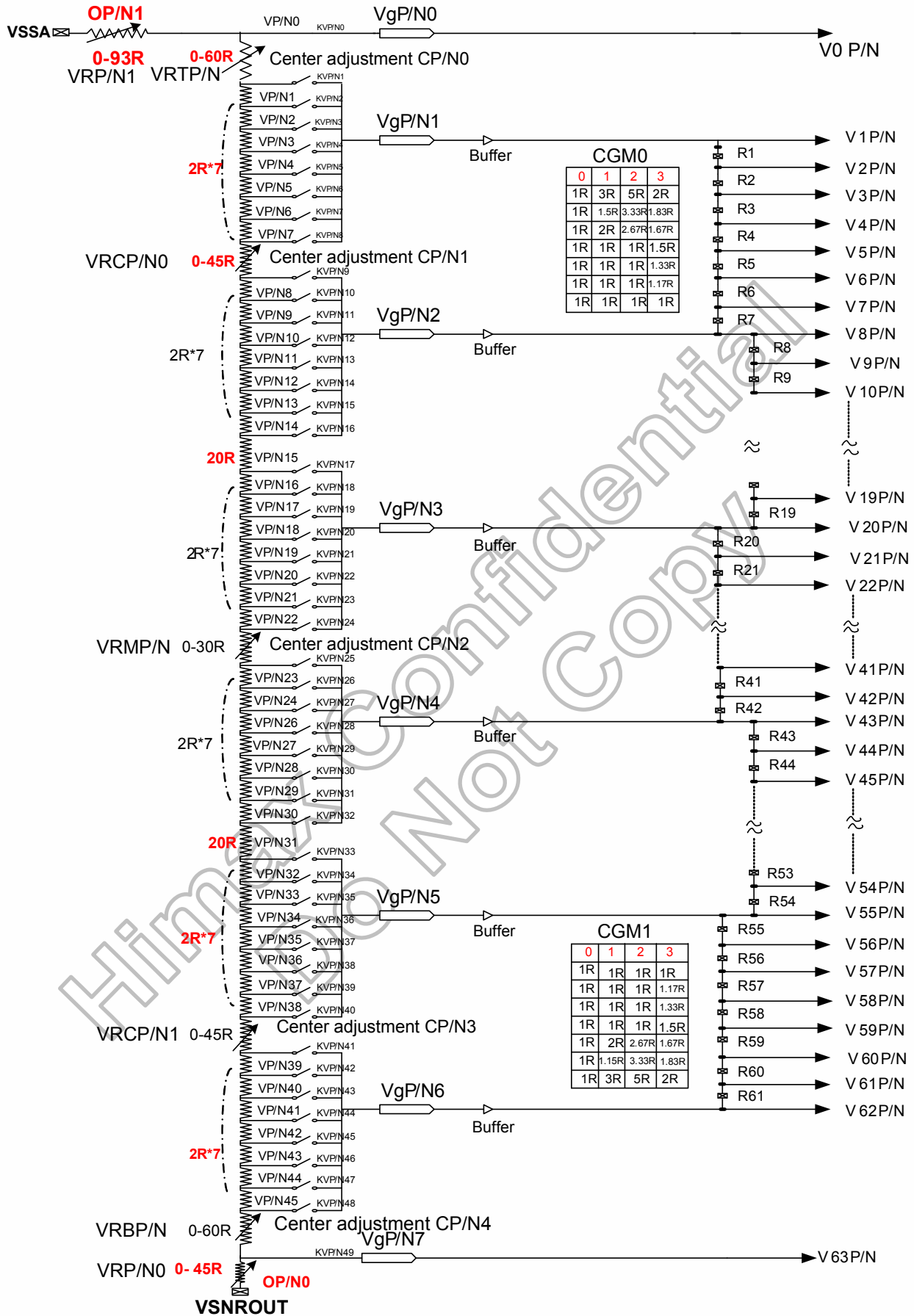


Figure 7.4 Gamma resistor stream and Positive & Negative gamma reference voltage

7.2.4 Variable resistor

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

Value in Register OP/N0 3-0	Resistance VRP/N0	Value in Register OP/N1 4-0	Resistance VRP/N1
0000	0R	00000	0R
0001	3R	00001	3R
0010	6R	00010	6R
•		•	
•		•	
1101	39R	11101	87R
1110	42R	11110	90R
1111	45R	11111	93R

Table 7.2 Offset adjustment

Value in Register CP/N0 3-0	Resistance VRTP/N	Value in Register CP/N4 3-0	Resistance VRBP/N	Value in Register CP/N2 3-0	Resistance VRMP/N0
0000	0R	0000	0R	0000	0R
0001	4R	0001	4R	0001	2R
0010	8R	0010	8R	0010	4R
•		•	•	•	•
•		•	•	•	•
1100		1100	48R	1100	24R
1101	52R	1101	52R	1101	26R
1110	56R	1110	56R	1110	28R
1111	60R	1111	60R	1111	30R

Value in Register CP/N3 3-0	Resistance VRCP/N1	Value in Register CP/N1 3-0	Resistance VRCP/N0
0000	0R	0000	0R
0001	3R	0001	3R
0010	6R	0010	6R
•	•	•	•
•	•	•	•
1100	36R	1100	36R
1101	39R	1101	39R
1110	42R	1110	42R
1111	45R	1111	45R

Table 7.3 Center adjustment

8 to 1 selector

The 8 to 1 selector has eight input voltages generated by gamma resistor stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 2	Vg(P/N) 3	Vg(P/N) 4	Vg(P/N) 5	Vg(P/N) 6
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 7.4 Output voltage of 8 to 1 selector

The grayscale levels are determined by the following formulas.

Reference Voltage	Formula	
VgP/N0	-	$VSPROUT - VD * VRP / N1 / \text{sumRP} / N$
VgP1/VgN7	MP/N0 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N) / \text{sumRP} / N$
	MP/N0 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + 2R) / \text{sumRP} / N$
	MP/N0 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + 4R) / \text{sumRP} / N$
	MP/N0 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + 6R) / \text{sumRP} / N$
	MP/N0 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + 8R) / \text{sumRP} / N$
	MP/N0 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + 10R) / \text{sumRP} / N$
	MP/N0 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + 12R) / \text{sumRP} / N$
	MP/N0 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + 14R) / \text{sumRP} / N$
VgP2/VgN2	MP/N1 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N + 14R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + 16R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + 18R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + 20R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + 22R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + 24R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + 26R + VRCP/N0) / \text{sumRP} / N$
	MP/N1 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + 28R + VRCP/N0) / \text{sumRP} / N$
VgP3/VgN3	MP/N2 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N + 48R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + 50R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + 52R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + 54R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + 56R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + 58R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + 60R + VRCP/N0) / \text{sumRP} / N$
	MP/N2 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + 62R + VRCP/N0) / \text{sumRP} / N$
VgP4/VgN4	MP/N3 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 62R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 64R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 66R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 68R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 70R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 72R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 74R + VRCP/N0) / \text{sumRP} / N$
	MP/N3 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 76R + VRCP/N0) / \text{sumRP} / N$
VgP5/VgN5	MP/N4 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 96R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 98R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 100R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 102R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 104R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 106R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 108R + VRCP/N0) / \text{sumRP} / N$
	MP/N4 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 110R + VRCP/N0) / \text{sumRP} / N$
VgP6/VgN6	MP/N5 2-0=000	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 110R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=001	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 112R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=010	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 114R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=011	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 116R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=100	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 118R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=101	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 120R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=110	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 122R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
	MP/N5 2-0=111	$VSPROUT - VD((VRP/N1 + VRTP/N + VRMP/N + 124R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$
VgP7/VgN7	-	$VSPROUT - VD((VRP/N1 + VRBP/N + VRTP/N + VRMP/N + 104R + VRCP/N0 + VRCP/N1) / \text{sumRP} / N$

SumRP=124R+VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
 SumRN=124R+ VRN0+ VRN1+ VRTN+ VRCN0+VRMN+VRCN1+VRBN
 VD=(VSPROUT-VSSA)

Table 7.5 Voltage calculation formula

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0P/V63N	VgP/N0	V32P/V31N	$VgP/N4+(VgP/N3-VgP/N4)*(11/23)$
V1P/V62N	VgP/N1	V33P/V30N	$VgP/N4+(VgP/N3-VgP/N4)*(10/23)$
V2P/V61N	$VgP/N2+(VgP/N1-VgP/N2)*CT1$	V34P/V29N	$VgP/N4+(VgP/N3-VgP/N4)*(9/23)$
V3P/V60N	$VgP/N2+(VgP/N1-VgP/N2)*CT2$	V35P/V28N	$VgP/N4+(VgP/N3-VgP/N4)*(8/23)$
V4P/V59N	$VgP/N2+(VgP/N1-VgP/N2)*CT3$	V36P/V27N	$VgP/N4+(VgP/N3-VgP/N4)*(7/23)$
V5P/V58N	$VgP/N2+(VgP/N1-VgP/N2)*CT4$	V37P/V26N	$VgP/N4+(VgP/N3-VgP/N4)*(6/23)$
V6P/V57N	$VgP/N2+(VgP/N1-VgP/N2)*CT5$	V38P/V25N	$VgP/N4+(VgP/N3-VgP/N4)*(5/23)$
V7P/V56N	$VgP/N2+(VgP/N1-VgP/N2)*CT6$	V39P/V24N	$VgP/N4+(VgP/N3-VgP/N4)*(4/23)$
V8P/V55N	VgP/N2	V40P/V23N	$VgP/N4+(VgP/N3-VgP/N4)*(3/23)$
V9P/V54N	$VgP/N3+(VgP/N2-VgP/N3)*(22/24)$	V41P/V22N	$VgP/N4+(VgP/N3-VgP/N4)*(2/23)$
V10P/V53N	$VgP/N3+(VgP/N2-VgP/N3)*(20/24)$	V42P/V21N	$VgP/N4+(VgP/N3-VgP/N4)*(1/23)$
V11P/V52N	$VgP/N3+(VgP/N2-VgP/N3)*(18/24)$	V43P/V20N	VgP/N4
V12P/V51N	$VgP/N3+(VgP/N2-VgP/N3)*(16/24)$	V44P/V19N	$VgP/N5+(VgP/N4-VgP/N5)*(22/24)$
V13P/V50N	$VgP/N3+(VgP/N2-VgP/N3)*(14/24)$	V45P/V18N	$VgP/N5+(VgP/N4-VgP/N5)*(20/24)$
V14P/V49N	$VgP/N3+(VgP/N2-VgP/N3)*(12/24)$	V46P/V17N	$VgP/N5+(VgP/N4-VgP/N5)*(18/24)$
V15P/V48N	$VgP/N3+(VgP/N2-VgP/N3)*(10/24)$	V47P/V16N	$VgP/N5+(VgP/N4-VgP/N5)*(16/24)$
V16P/V47N	$VgP/N3+(VgP/N2-VgP/N3)*(8/24)$	V48P/V15N	$VgP/N5+(VgP/N4-VgP/N5)*(14/24)$
V17P/V46N	$VgP/N3+(VgP/N2-VgP/N3)*(6/24)$	V49P/V14N	$VgP/N5+(VgP/N4-VgP/N5)*(12/24)$
V18P/V45N	$VgP/N3+(VgP/N2-VgP/N3)*(4/24)$	V50P/V13N	$VgP/N5+(VgP/N4-VgP/N5)*(10/24)$
V19P/V44N	$VgP/N3+(VgP/N2-VgP/N3)*(2/24)$	V51P/V12N	$VgP/N5+(VgP/N4-VgP/N5)*(8/24)$
V20P/V43N	VgP/N3	V52P/V11N	$VgP/N5+(VgP/N4-VgP/N5)*(6/24)$
V21P/V42N	$VgP/N4+(VgP/N3-VgP/N4)*(22/23)$	V53P/V10N	$VgP/N5+(VgP/N4-VgP/N5)*(4/24)$
V22P/V41N	$VgP/N4+(VgP/N3-VgP/N4)*(21/23)$	V54P/V9N	$VgP/N5+(VgP/N4-VgP/N5)*(2/24)$
V23P/V40N	$VgP/N4+(VgP/N3-VgP/N4)*(20/23)$	V55P/V8N	VgP/N5
V24P/V39N	$VgP/N4+(VgP/N3-VgP/N4)*(19/23)$	V56P/V7N	$VgP/N6+(VgP/N5-VgP/N6)*CB1$
V25P/V38N	$VgP/N4+(VgP/N3-VgP/N4)*(18/23)$	V57P/V6N	$VgP/N6+(VgP/N5-VgP/N6)*CB2$
V26P/V37N	$VgP/N4+(VgP/N3-VgP/N4)*(17/23)$	V58P/V5N	$VgP/N6+(VgP/N5-VgP/N6)*CB3$
V27P/V36N	$VgP/N4+(VgP/N3-VgP/N4)*(16/23)$	V59P/V4N	$VgP/N6+(VgP/N5-VgP/N6)*CB4$
V28P/V35N	$VgP/N4+(VgP/N3-VgP/N4)*(15/23)$	V60P/V3N	$VgP/N6+(VgP/N5-VgP/N6)*CB5$
V29P/V34N	$VgP/N4+(VgP/N3-VgP/N4)*(14/23)$	V61P/V2N	$VgP/N6+(VgP/N5-VgP/N6)*CB6$
V30P/V33N	$VgP/N4+(VgP/N3-VgP/N4)*(13/23)$	V62P/V1N	VgP/N6
V31P/V32N	$VgP/N4+(VgP/N3-VgP/N4)*(12/23)$	V63P/V0N	VgP/N7

Table 7.6 Voltage calculation formula of grayscale voltage

CGM0[1:0]	“00”	“01”	“10”	“11”
CT1	6/7	7.5/10.5	10/15	8.5/10.5
CT2	5/7	6/10.5	6.67/15	6.67/10.5
CT3	4/7	4/10.5	4/15	5.0/10.5
CT4	3/7	3/10.5	3/15	3.5/10.5
CT5	2/7	2/10.5	2/15	2.17/10.5
CT6	1/7	1/10.5	1/15	1/10.5

CGM1[1:0]	“00”	“01”	“10”	“11”
CB1	6/7	9.5/10.5	14/15	9.5/10.5
CB2	5/7	8.5/10.5	13/15	8.33/10.5
CB3	4/7	7.5/10.5	12/15	7.0/10.5
CB4	3/7	6.5/10.5	11/15	5.5/10.5
CB5	2/7	4.5/10.5	8.33/15	3.83/10.5
CB6	1/7	3.0/10.5	5/15	2.0/10.5

Note: Negative gamma don't have CGM0/CGM1 setting, the ratio V2~V7 and V56~V61 is automatically mapping from positive side.

Table 7.7 Voltage calculation formula of grayscale voltage V2~V7 and V56~V61

Relationship between GRAM Data and Output Level (“Normally White Panel”, GRAM data=0)

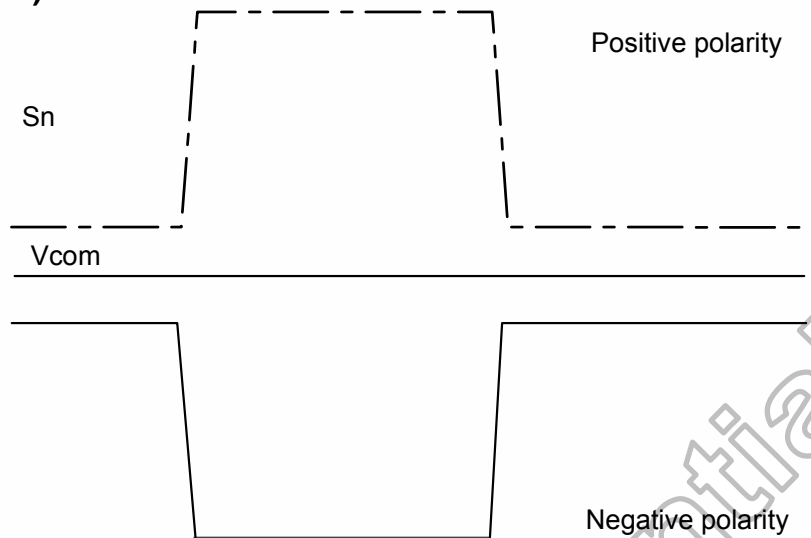


Figure 7.5 Relationship between source output and VCOM

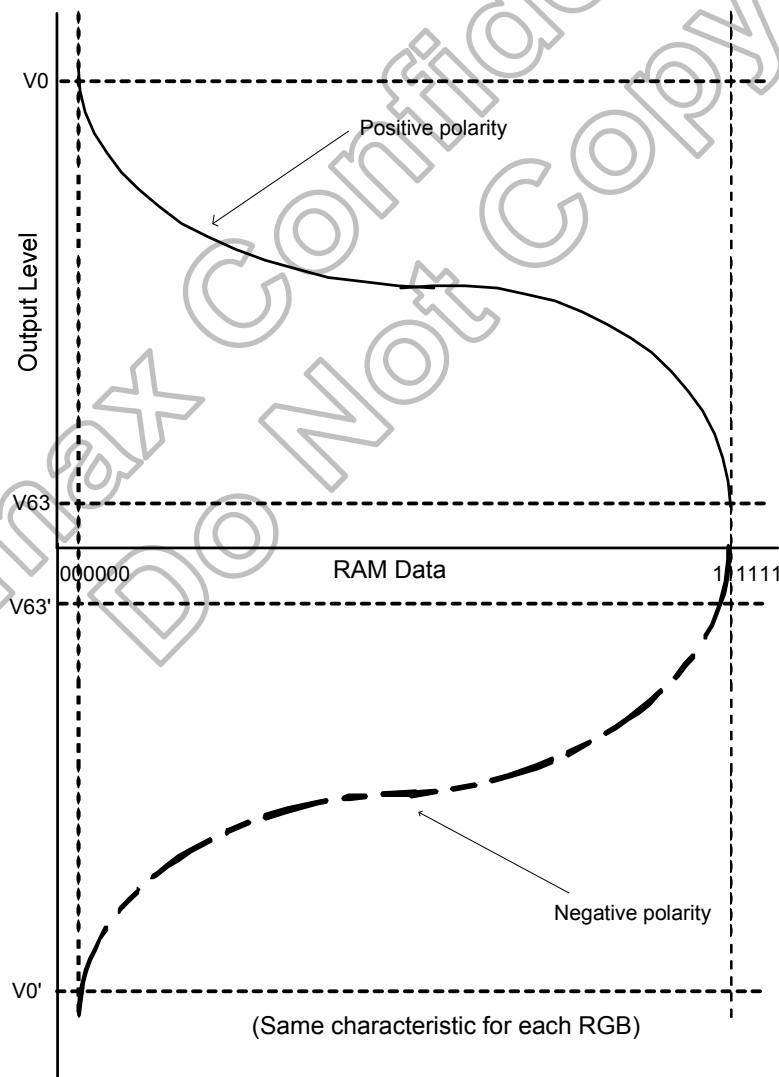


Figure 7.6 Relationship between GRAM data and output level (normal white panel REV_Panel="0")

Four-characteristic gamma curve selection

There are four kind of Gamma Curve is selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

GC_SEL="L":

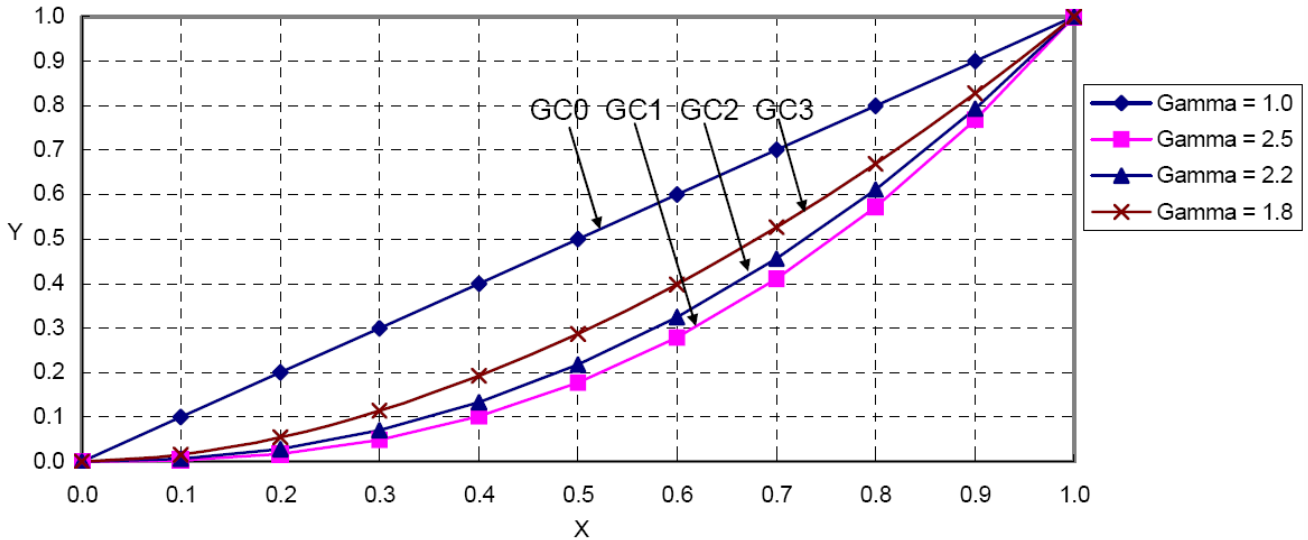


Figure 7.7 Gamma curve according to GC0 to GC3 bit (GC_SEL="L")

GC_SEL="H":

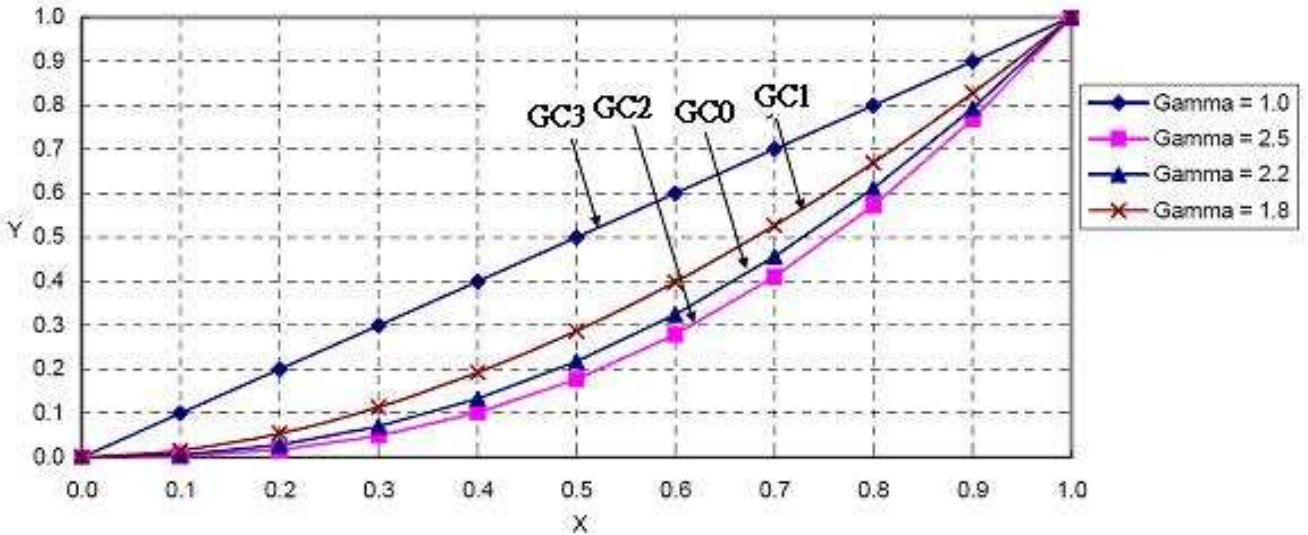


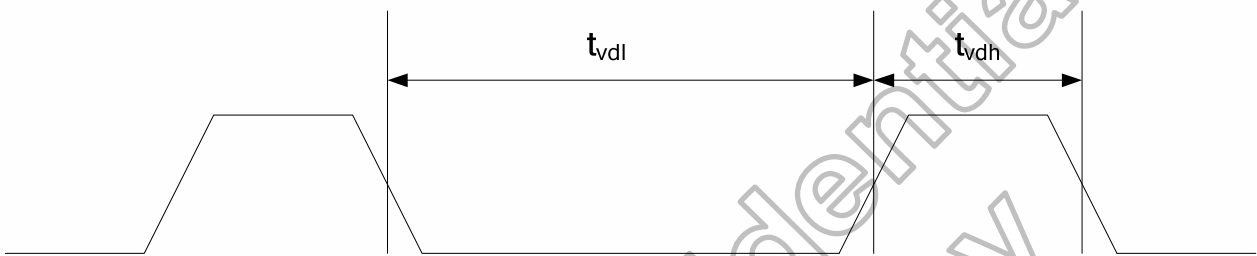
Figure 7.8 Gamma curve according to GC0 to GC3 bit (GC_SEL="H")

7.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.3.1 Tearing effect line modes

Mode 1: The Tearing Effect Output signal consists of V-Blanking Information only:

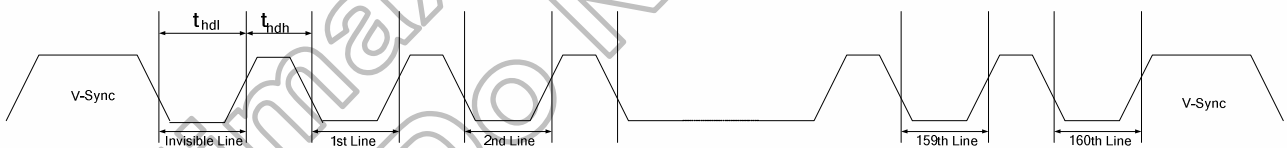


t_{vdh} = The LCD display is not updated from the Frame Memory
 t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

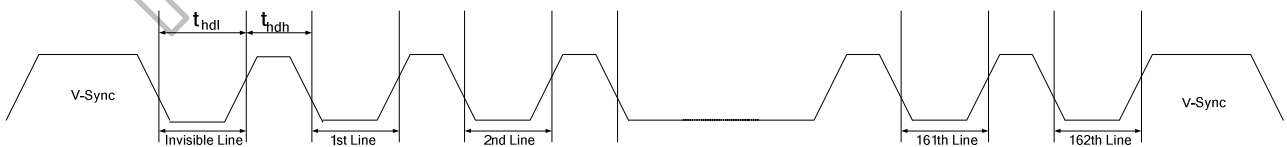
Figure 7.9 TE mode 1 output

Mode 2: The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field on different resolution.

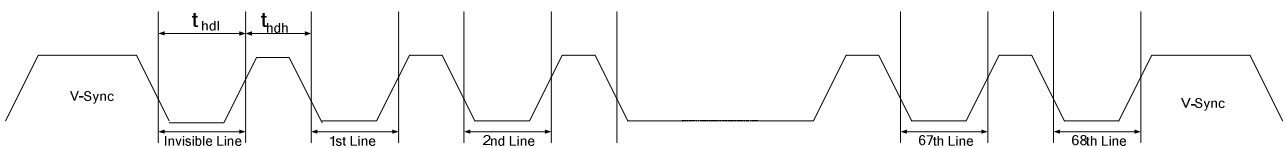
128RGBx160: N=160



132RGBx162: N=162



96x68: N=68



96x64: N=64

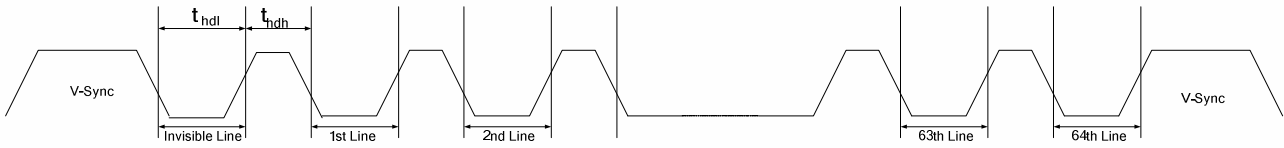
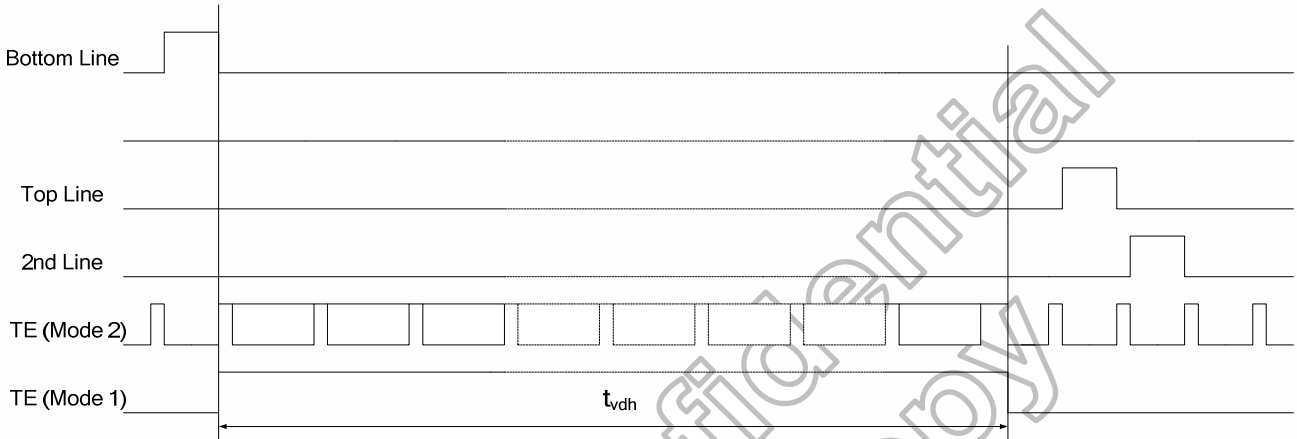


Figure 7.10 TE mode 2 output

t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above.)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

Figure 7.11 TE output waveform

7.3.2 Tearing effect line timing

The Tearing Effect signal is described below.

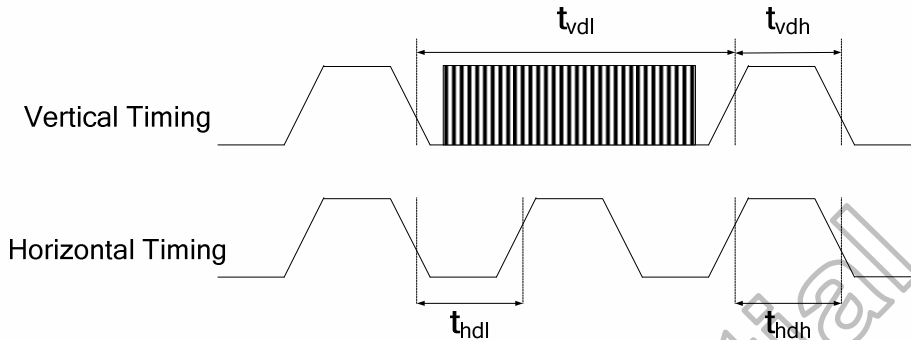


Figure 7.12 Waveform of tearing effect signal

Idle Mode Off (Frame Rate=60Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t _{vdl}	Vertical Timing Low Duration	TBD	-	ms	-
t _{vdh}	Vertical Timing High Duration	1000	-	μs	-
t _{hdl}	Horizontal Timing Low Duration	TBD	-	μs	-
t _{hdh}	Horizontal Timing High Duration	TBD	500	μs	-

Table 7.8 AC characteristics of tearing effect signal

The signal's rise and fall times (t_f, t_r) are stipulated to be equal to or less than 15ns.

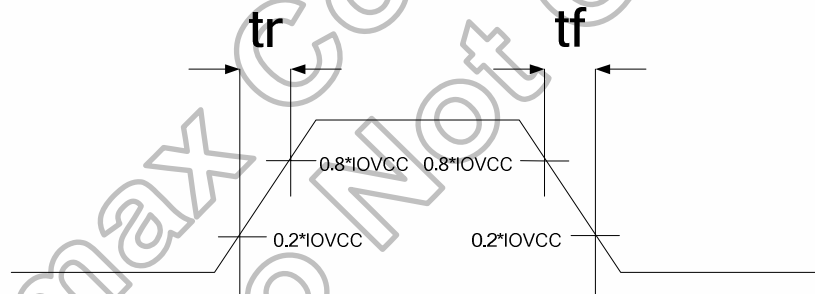


Figure 7.13 Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

7.3.3 Example 1: MPU write is faster than panel read

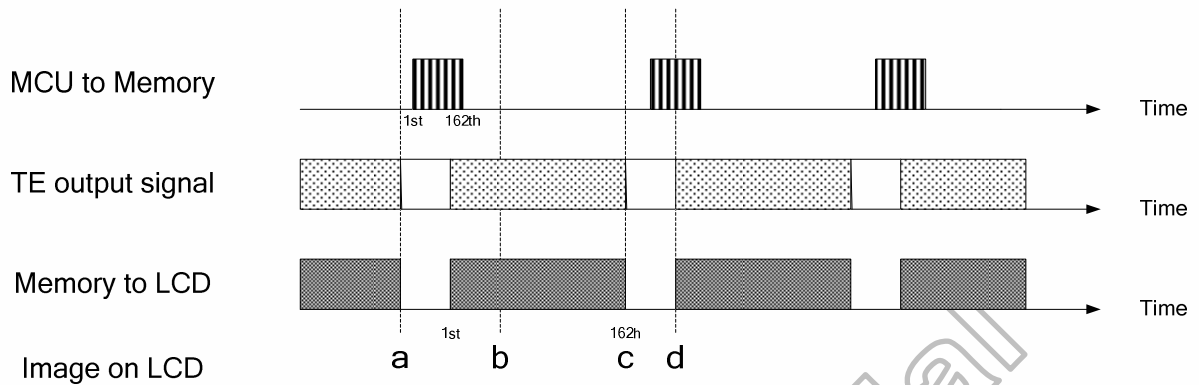


Figure 7.14 Timing of MPU write is faster than panel read

Data write to frame memory is now synchronized to the panel scan. It should be written during the vertical sync pulse of the tearing effect output line. This ensures that data is always written ahead of the panel scan and each panel frame refresh has a complete new image:

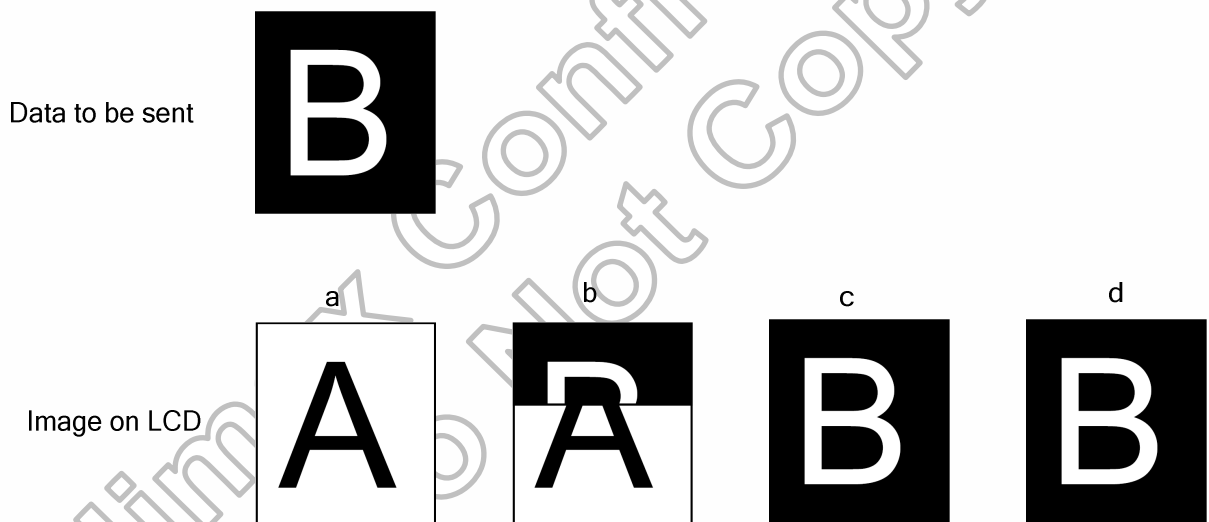


Figure 7.15 Display of MPU write is faster than panel read

7.3.4 Example 2: MPU write is slower than panel read

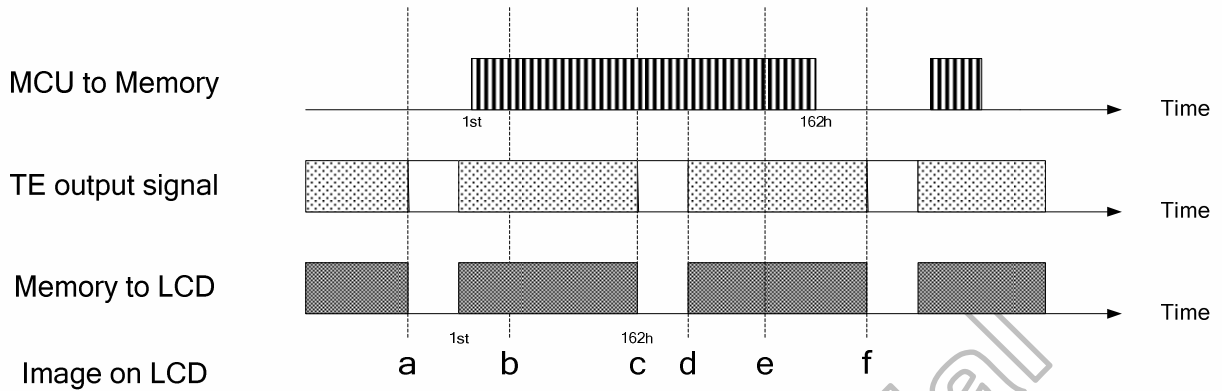


Figure 7.16 Timing of MPU write is slower than panel read

The MPU to frame memory write begins just after panel read has commenced i.e. after one horizontal sync pulse of the tearing effect output line. This allows time for the image to download behind the panel read pointer and finishing download during the subsequent frame before the read pointer “catches” the MPU to frame memory write position.

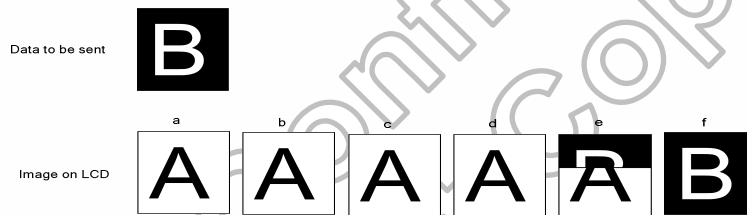


Figure 7.17 Display of MPU write is slower than panel read

7.4 Scan Mode Setting

HX8353-E can set internal register GS_PANEL bit to determine the pin assignment of gate. The GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8353-E.

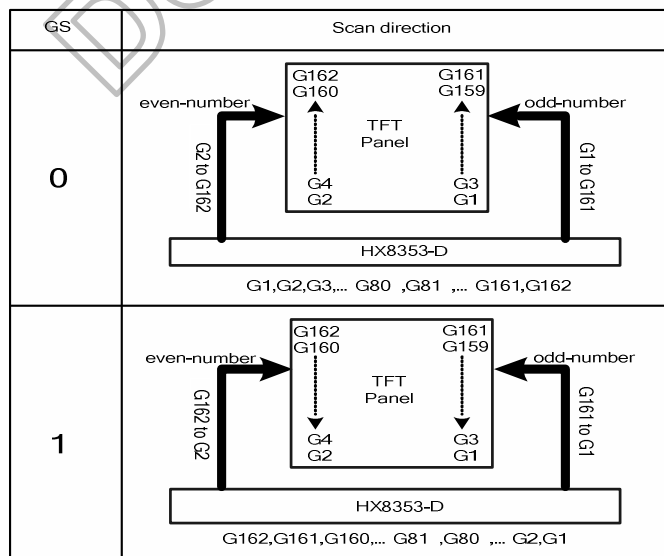


Figure 7.18 Gate Scan Mode

7.5 LCD power generation circuit

7.5.1 Power supply circuit

The power circuit of HX8353-E is used to generate supply voltages for LCD panel driving.

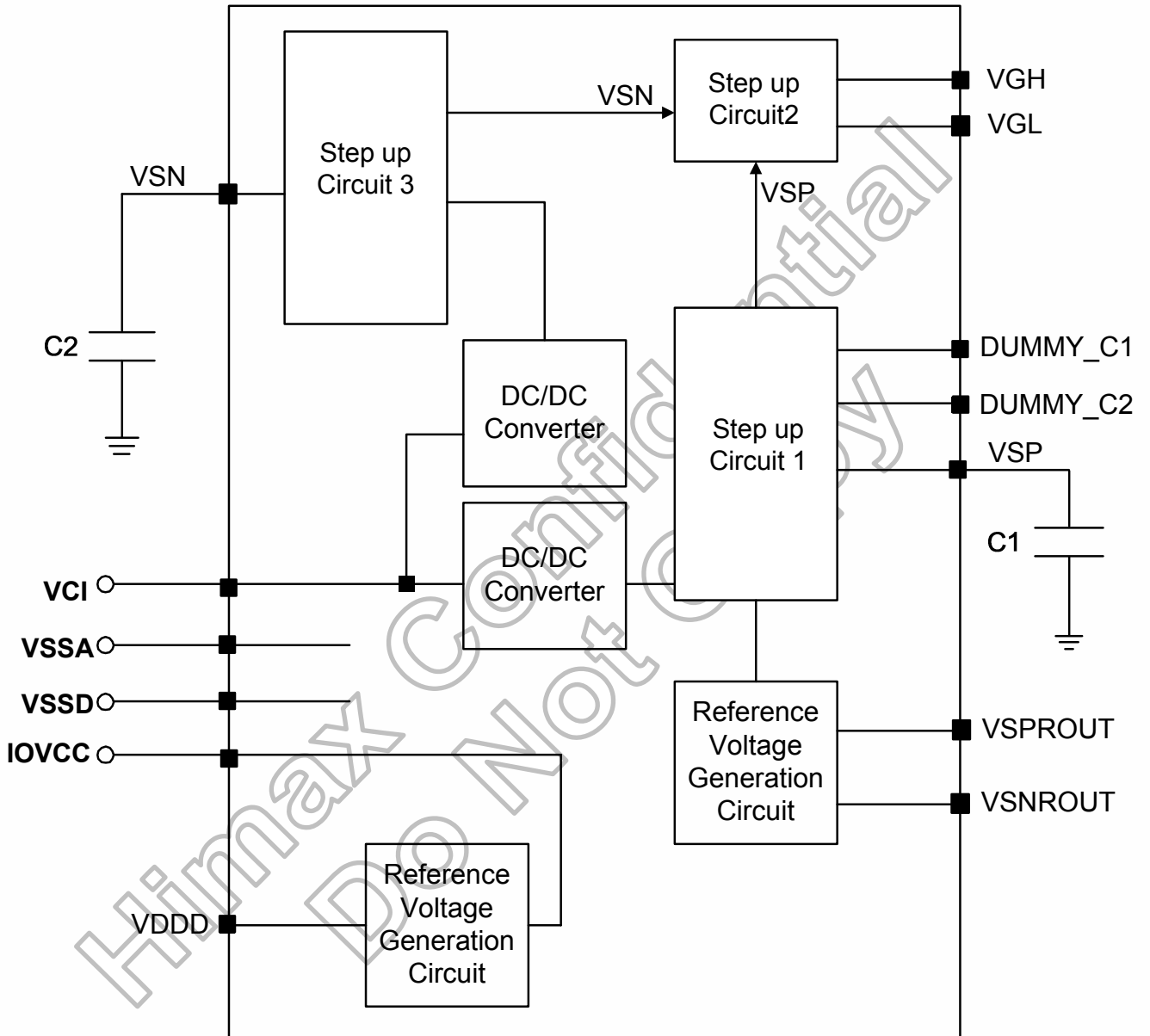


Figure 7.19 Block diagram of HX8353-E power circuit

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity
C1 (VSP)	10V	1 μ F (B characteristics)
C2 (VSN)	10V	1 μ F (B characteristics)

Table 7.9 The adaptability of Capacitor

7.5.2 LCD power generation scheme

The boost voltage generated is shown as below.

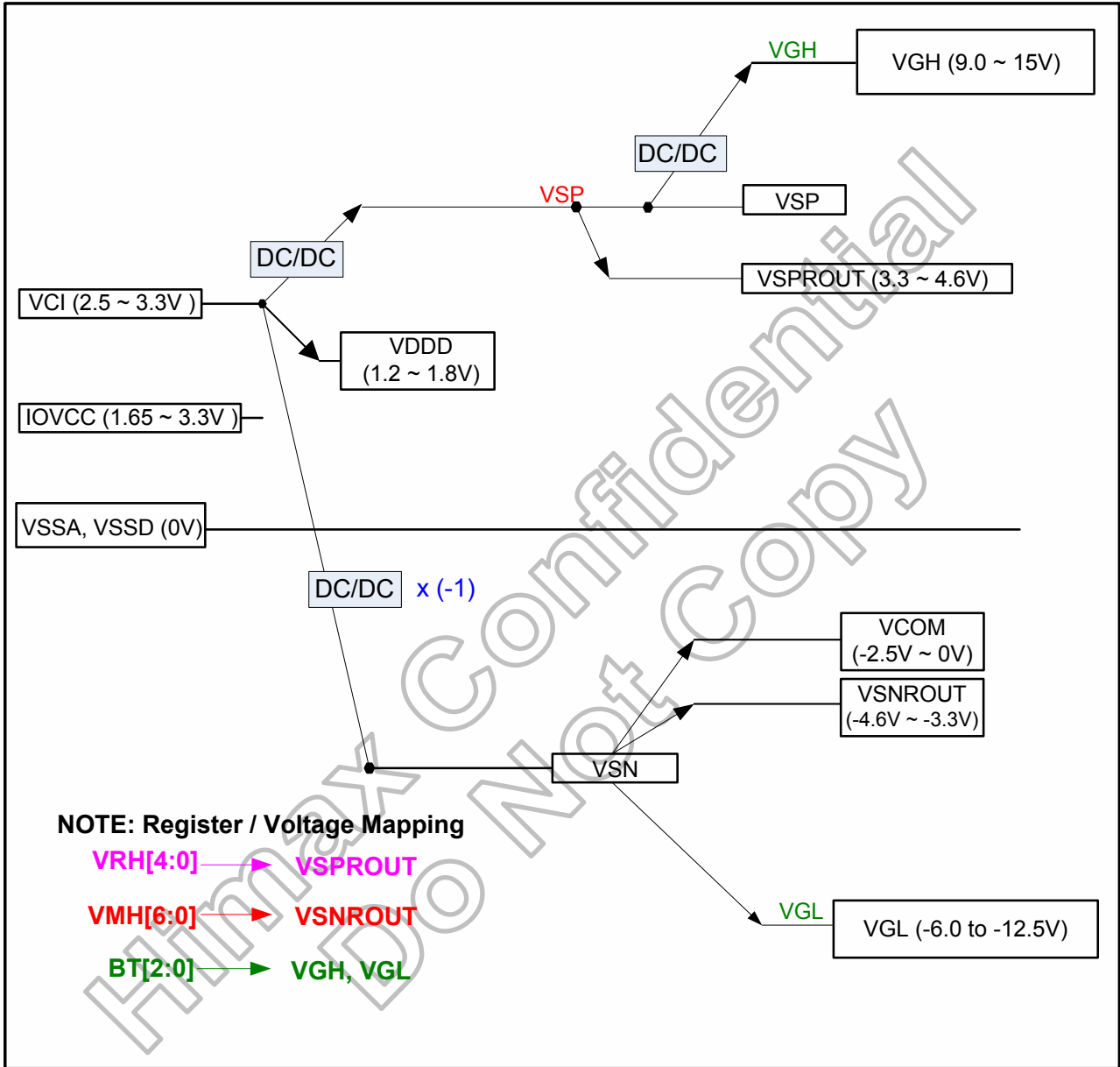


Figure 7.20 LCD power generation scheme

7.6 Power function

7.6.1 Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order.
IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

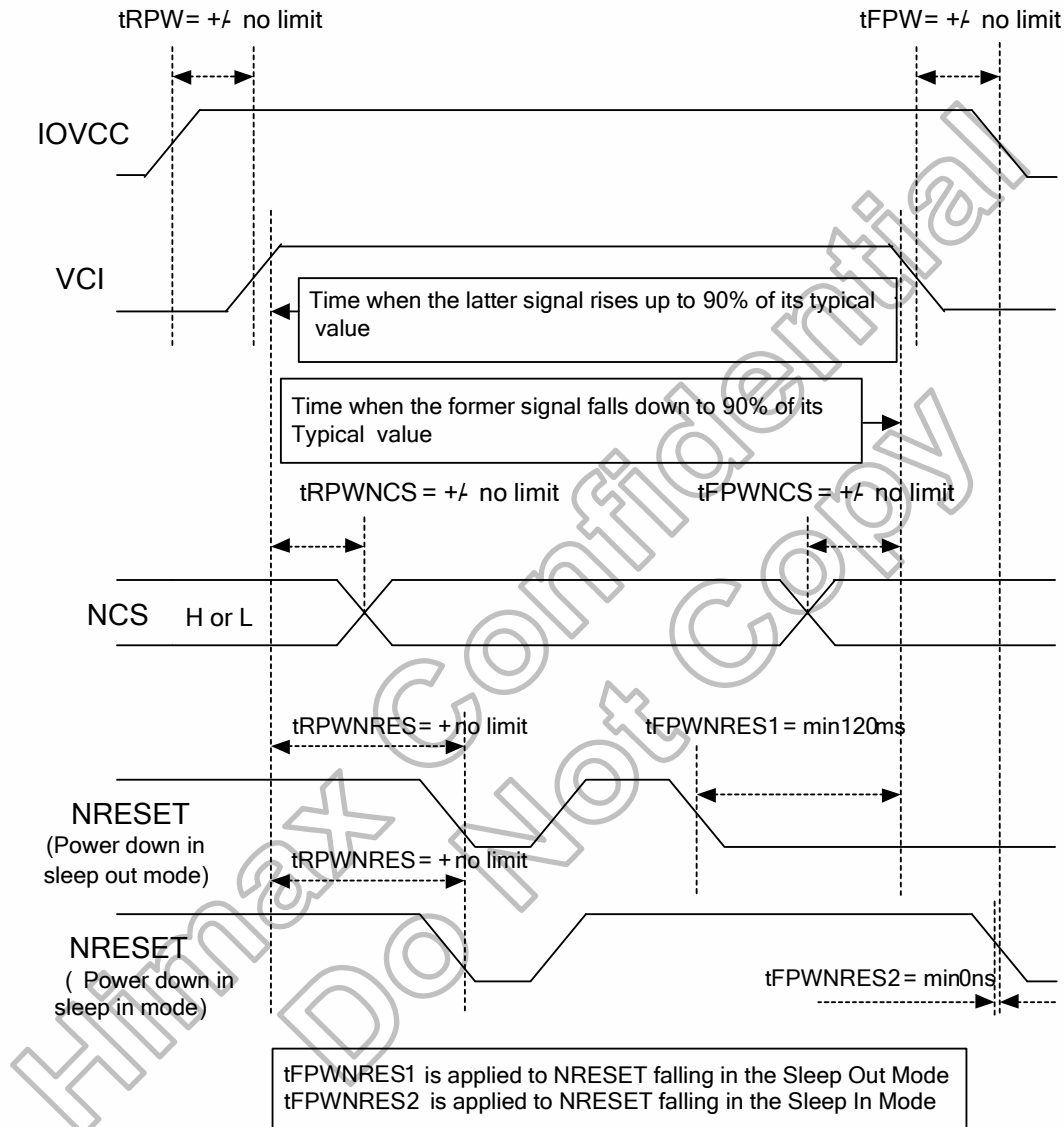
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

- Note:** (1) There will be no damage to the display module if the power sequences are not met.
(2) There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
(3) There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
(4) If NRESET line is not held stable by host during Power on Sequence as defined in Sections 7.5.1.1 and 7.5.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence to ensure correct operation. Otherwise correct function is not guaranteed.

If NRESET line is not held stable by host during Power on Sequence as defined in Sections 7.5.1.1 and 7.5.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence is complete to ensure correct operation, otherwise correct functionality is not guaranteed. The power on/off sequence is illustrated as below.

7.6.1.1 Case 1 – NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCI have been applied, otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

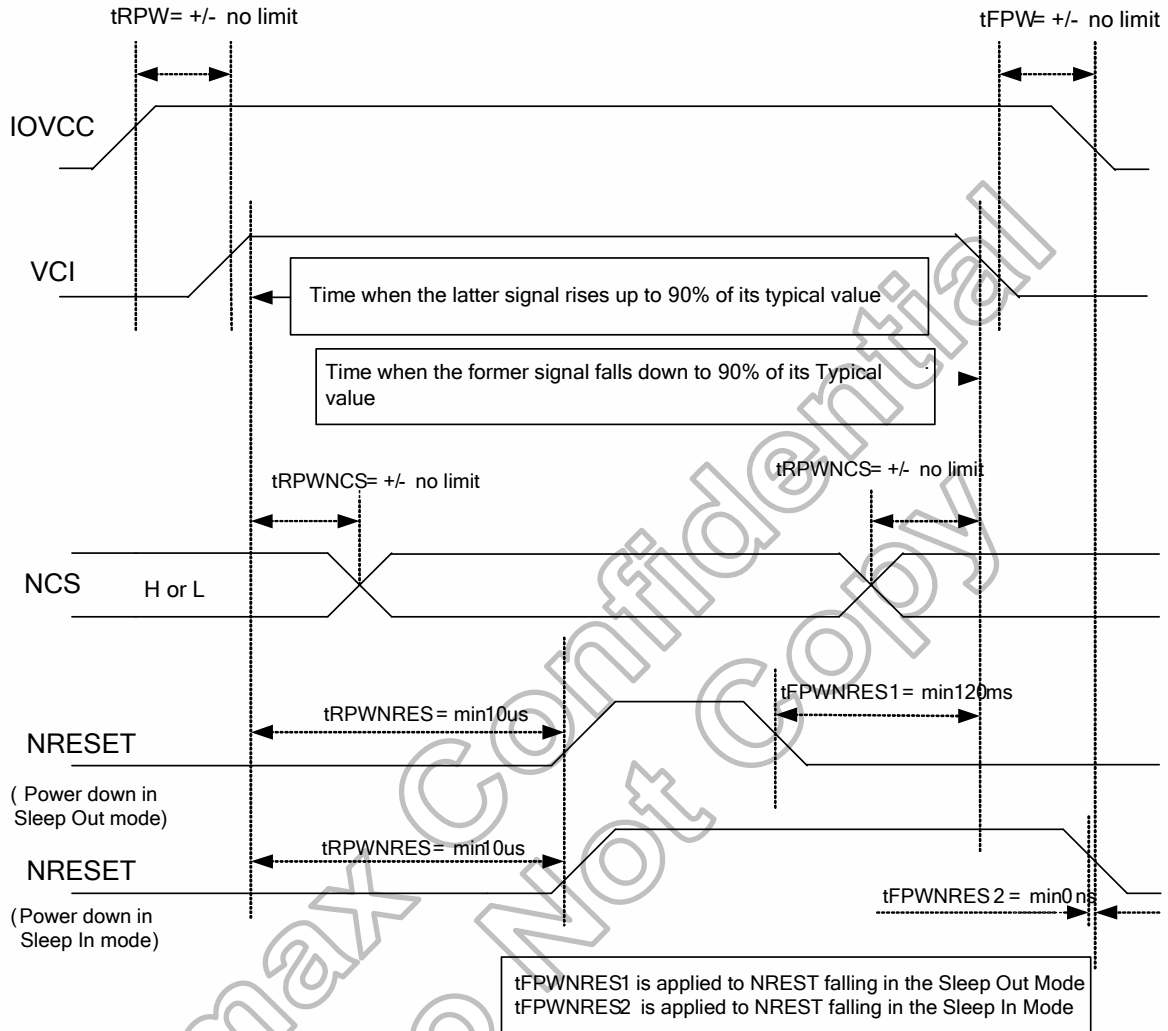


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 7.21 Case 1 – NRESET line is held high or unstable by host at power on

7.6.1.2 Case 2 – NRESET line is held low by host at power on

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after VCI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 7.22 NRESET Line is Held Low by Host at Power On

7.6.2 Power levels definition

7.6.2.1 General definition for power levels on system interface

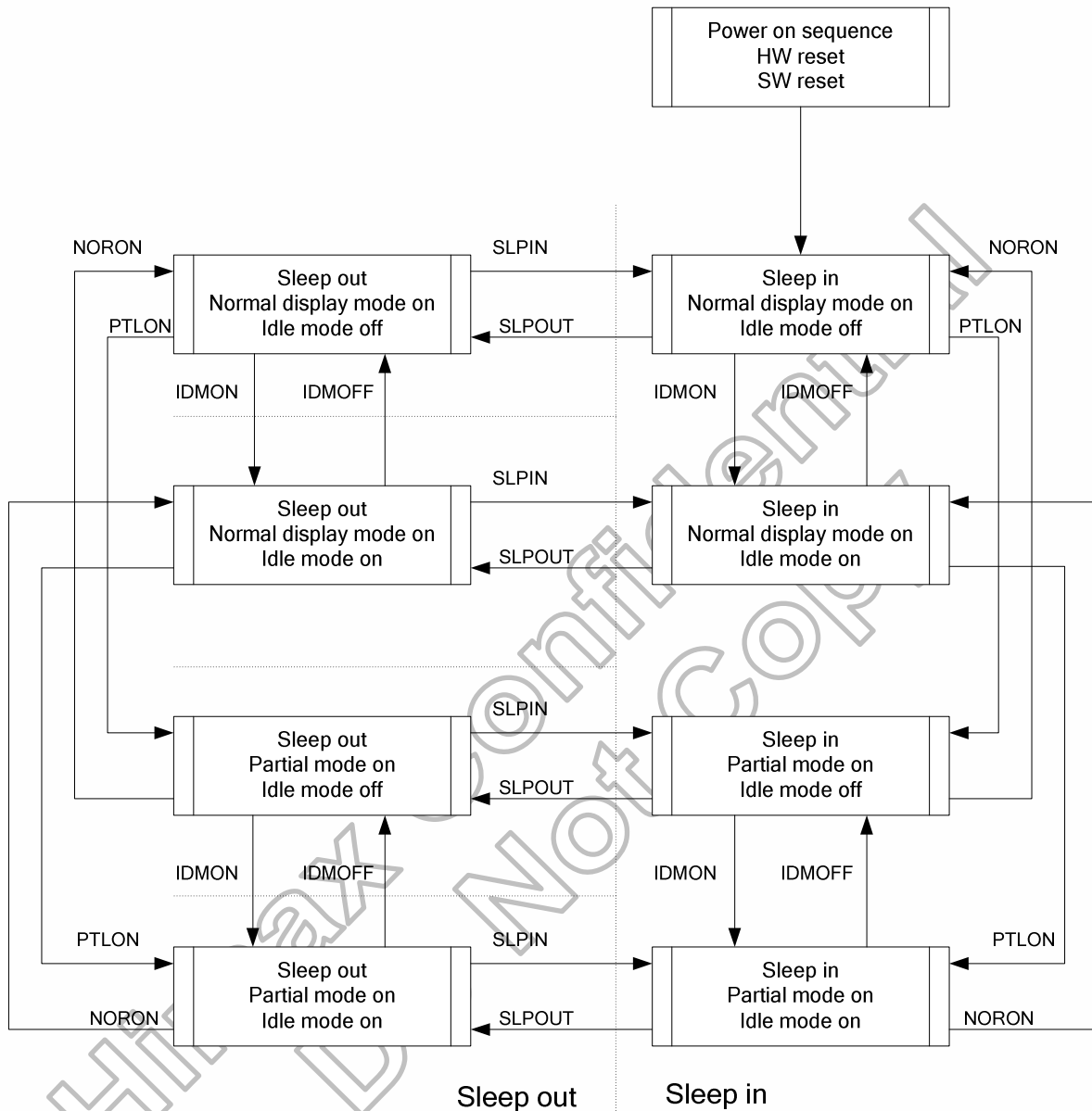


Figure 7.23 Power flow chart for different power modes

7.6.3 Deep standby mode set up flow

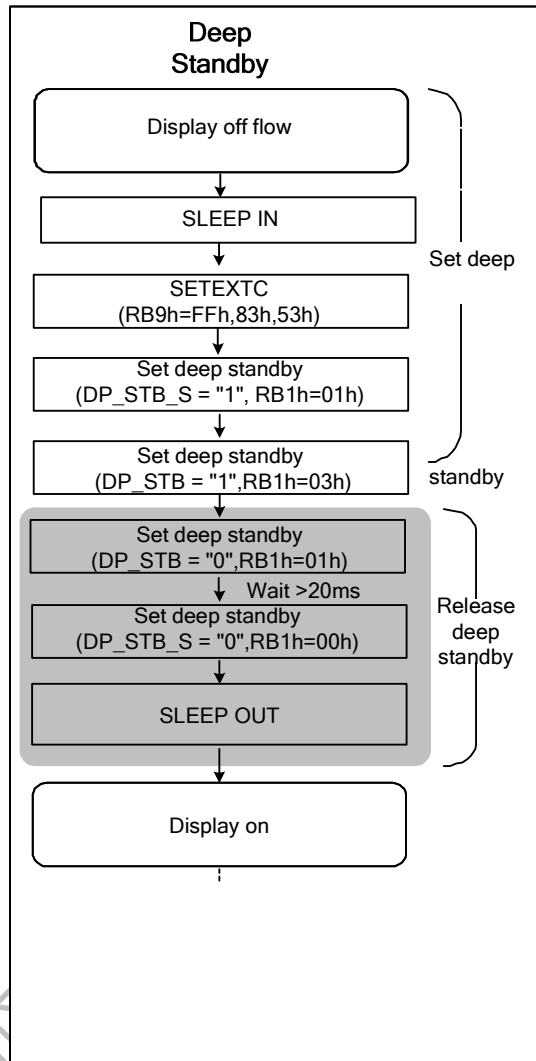


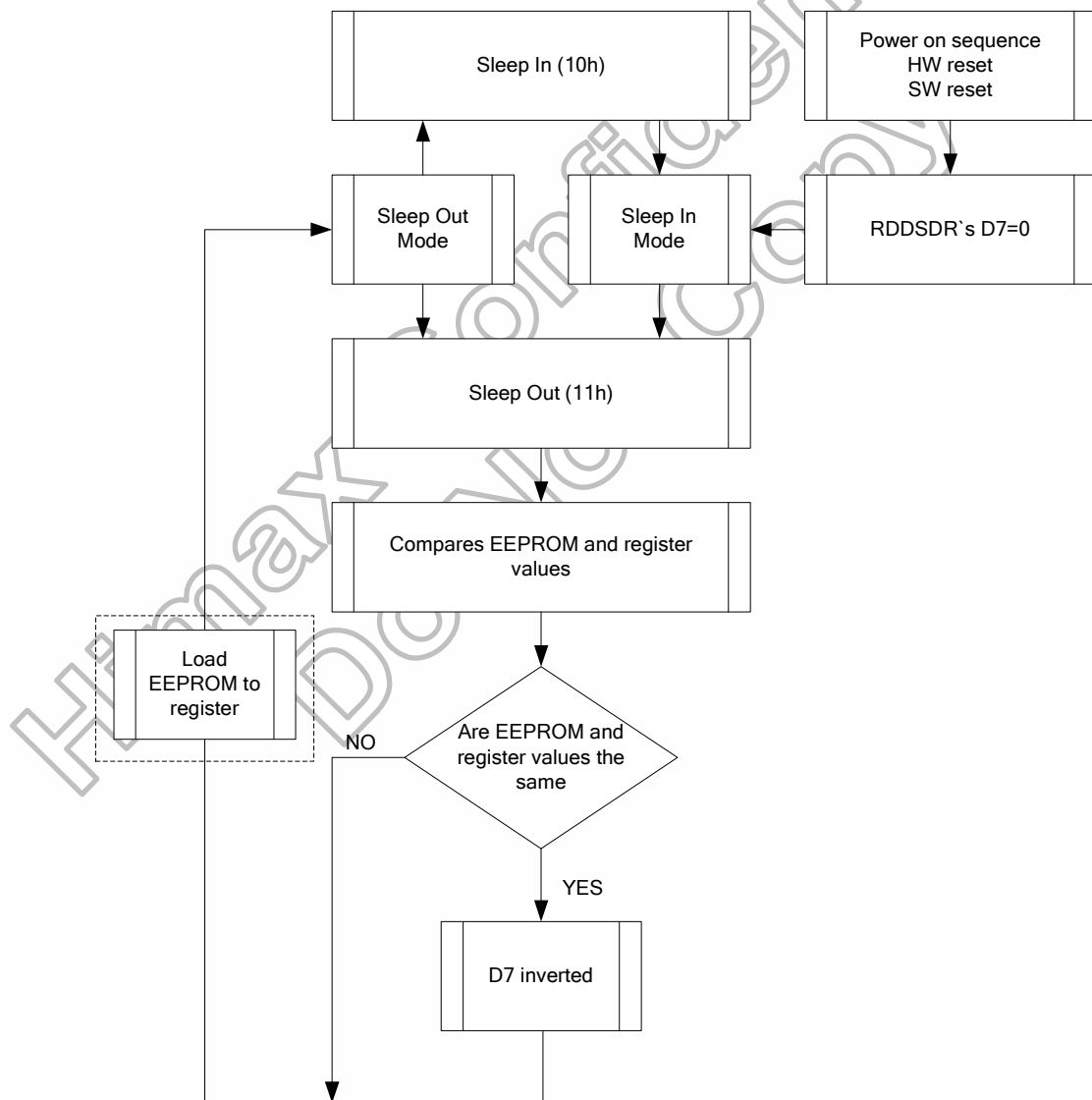
Figure 7.24 Deep standby mode setting flow

7.7 Sleep out – command and self-diagnostic functions of display module

7.7.1 Register loading detection

Sleep Out-command (See section 8.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in section 8.2.10 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The bit used for this command is D7). If those both values are not the same, this bit (D7) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



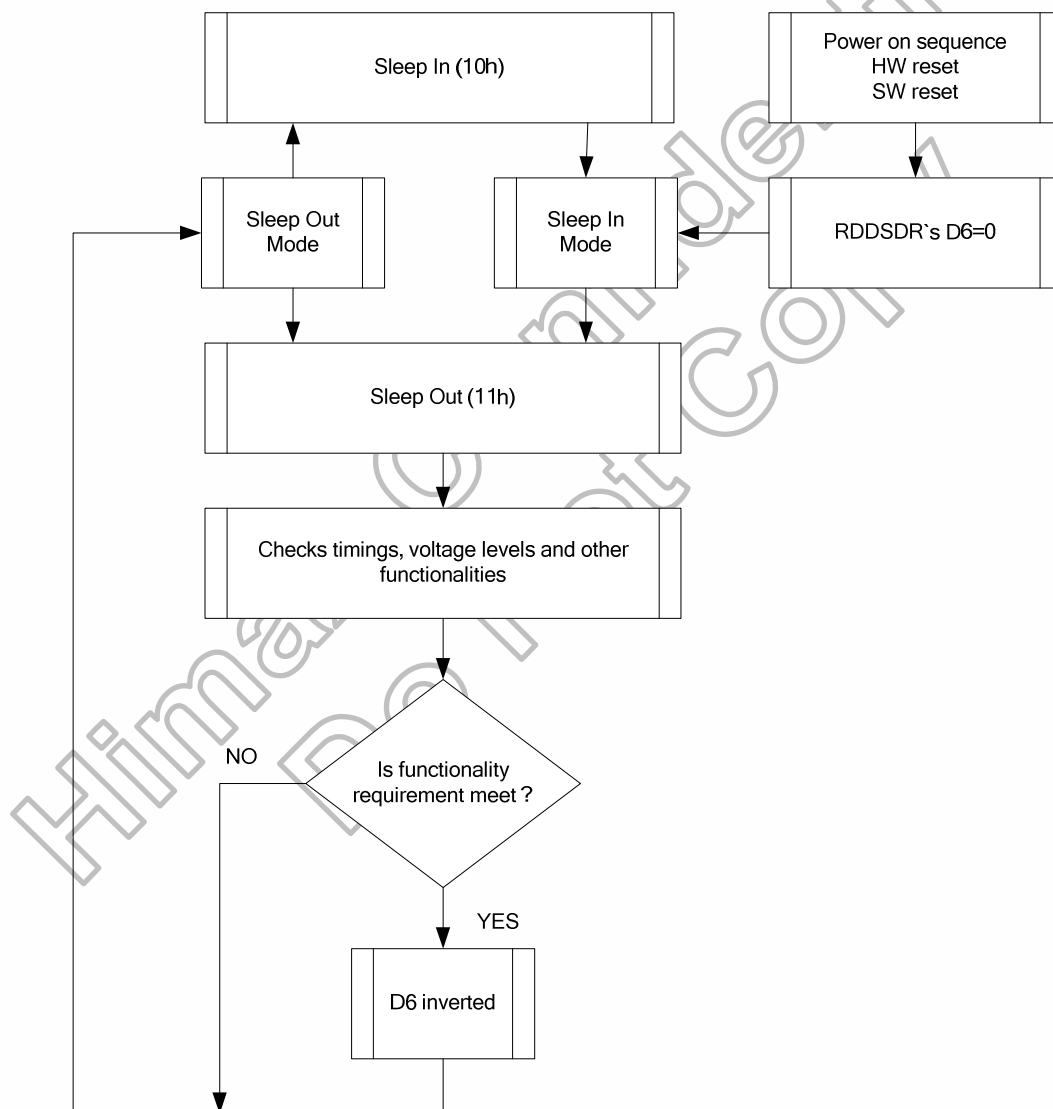
Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

Figure 7.25 RDDSDR register loading detection flow

7.7.2 Functionality detection

Sleep Out-command (See section 8.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in section 8.2.10 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 7.26 Functionality detection flow

7.8 Input / output pin state

7.8.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
VTESTOUT NVTESTOUT	Low	Low	Low

Table 7.10 Characteristics of output pins

7.8.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
NRESET	Input valid	Input valid	Input valid	Input valid	Input valid
NCS	Input valid	Input valid	Input valid	Input valid	Input valid
SPI_SEL	Input valid	Input valid	Input valid	Input valid	Input valid
GC_SEL	Input valid	Input valid	Input valid	Input valid	Input valid
LC_SEL0, LC_SEL1	Input valid	Input valid	Input valid	Input valid	Input valid
DNC_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
NWR_RNW	Input valid	Input valid	Input valid	Input valid	Input valid
NRD_E	Input valid	Input valid	Input valid	Input valid	Input valid
DB17 to DB0	Input valid	Input valid	Input valid	Input valid	Input valid
OSC,P68,BS1,BS2,BS0	Input valid	Input valid	Input valid	Input valid	Input valid
EXTC	Input valid	Input valid	Input valid	Input valid	Input valid
TEST1	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2	Input valid	Input valid	Input valid	Input valid	Input valid
RSO0	Input valid	Input valid	Input valid	Input valid	Input valid
RSO1	Input valid	Input valid	Input valid	Input valid	Input valid
RSO2	Input valid	Input valid	Input valid	Input valid	Input valid

Table 7.11 Characteristics of input pins

8. Command Set

8.1 Command set list

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function	
00	NOP	0	↑	1	0	0	0	0	0	0	0	0	No operation	
01	SWRESET	0	↑	1	0	0	0	0	0	0	0	1	Software reset	
04	RDDIDIF	0	↑	1	0	0	0	0	0	1	0	0	Read display identification information	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	ID1[7:0]									ID1 read
		1	1	↑	ID2[7:0]									ID2 read
		1	1	↑	ID3[7:0]									ID3 read
09	RDDST	0	↑	1	0	0	0	0	1	0	0	1	Read display status	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D31	D30	D29	D28	D27	D26	D25	0		
		1	1	↑	0	D22	D21	D20	D19	D18	D17	D16		
		1	1	↑	D15	0	D13	0	0	D10	D9	D8		
0A	RDDPM	0	↑	1	0	0	0	0	1	0	1	0	Read display power mode	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D7	D6	D5	D4	D3	D2	0	0		
0B	RDDMADCTL	0	↑	1	0	0	0	0	1	0	1	1	Read display MADCTL	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D7	D6	D5	D4	D3	D2	0	0		
0C	RDDCOLM OD	0	↑	1	0	0	0	0	1	1	0	0	Read display pixel format	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	0	0	0	0	0	D2	D1	D0		
0D	RDDIM	0	↑	1	0	0	0	0	1	1	0	1	Read display image mode	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D7	0	D5	0	0	D2	D1	D0		
0E	RDDSM	0	↑	1	0	0	0	0	1	1	1	0	Read display signal mode	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D7	D6	0	0	0	0	0	0		
0F	RDDSDR	0	↑	1	0	0	0	0	1	1	1	1	Read display self-diagnostic result	
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read	
		1	1	↑	D7	D6	D5	D4	0	0	0	0		
10	SLPIN	0	↑	1	0	0	0	1	0	0	0	0	Sleep in and charge-pump off	
11	SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	Sleep out and charge-pump on	
12	PTLON	0	↑	1	0	0	0	1	0	0	1	0	Partial mode on	
13	NORON	0	↑	1	0	0	0	1	0	0	1	1	Normal display mode on	
20	INVOFF	0	↑	1	0	0	1	0	0	0	0	0	Display inversion off	
21	INVON	0	↑	1	0	0	1	0	0	0	0	1	Display inversion on	

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function	
26	GAMSET	0	↑	1	0	0	1	0	0	1	1	0	Gamma set	
		1	↑	1	GC[7:0]									
28	DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	Display off	
29	DISPON	0	↑	1	0	0	1	0	1	0	0	1	Display on	
2A	CASET	0	↑	1	0	0	1	0	1	0	1	0	Column setting	
		1	↑	1	SC[15:8]									Column address start
		1	↑	1	SC[7:0]									Column address start
		1	↑	1	EC[15:8]									Column address end
		1	↑	1	EC[7:0]									Column address end
2B	PASET	0	↑	1	0	0	1	0	1	0	1	1	Row address set	
		1	↑	1	SP[15:8]									Row address start
		1	↑	1	SP[7:0]									Row address start
		1	↑	1	EP[15:8]									Row address end
		1	↑	1	EP[7:0]									Row address end
2C	RAMWR	0	↑	1	0	0	1	0	1	1	0	0	Memory write	
		1	↑	1	D[17:0]									Write GRAM data
2D	RGBSET	0	↑	1	0	0	1	0	1	1	0	1	LUT parameter	
		1	↑	1	-	-	R005	R004	R003	R002	R001	R000	R000	Red tone
					:	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	Rnn0	Red tone
		1	↑	1	:	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	R315	R314	R313	R312	R311	R310	R310	Red tone
		1	↑	1	-	-	G005	G004	G003	G002	G001	G000	G000	Green tone
		1	↑	1	:	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	Gnn0	Green tone
		1	↑	1	:	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	G635	G634	G633	G632	G631	G630	G630	Green tone
		1	↑	1	-	-	B005	B004	B003	B002	B001	B000	B000	Blue tone
		1	↑	1	:	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	Bnn0	Blue tone
		2E	RAMRD	0	↑	1	0	0	1	0	1	1	1	0
1	↑			1	-	-	-	-	-	-	-	-	Dummy read	
1	↑			1	D[15:0]									Read GRAM data
30	PLTAR	0	↑	1	0	0	1	1	0	0	0	0	Partial start end address set	
		1	↑	1	SR[15:8]									Start row
		1	↑	1	SR[7:0]									Start row
		1	↑	1	ER[15:8]									End row
		1	↑	1	ER[7:0]									End row
33	VSCRDEF	0	↑	1	0	0	1	1	0	0	1	1	Vertical Scrolling Definition	
		1	↑	1	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
		1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
		1	↑	1	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
		1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
		1	↑	1	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
34	TEOFF	0	↑	1	0	0	1	1	0	1	0	0	Tear effect Off	
		1	↑	1	0	0	1	1	0	1	0	1	Tear effect mode	
35	TEON	1	↑	1	-	-	-	-	-	-	-	TEMODE		

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
36	MADCTL	0	↑	1	0	0	1	1	0	1	1	0	Memory access control
		1	↑	1	MY	MX	MV	ML	BGR	SS	0	0	
37	VSCRSADD	0	↑	1	0	0	1	1	0	1	1	1	Vertical scrolling start address
		1	↑	1	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	
		1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	
38	IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	Idle mode off
39	IDMON	0	↑	1	0	0	1	1	1	0	0	1	Idle mode on
3A	COLMOD	0	↑	1	0	0	1	1	1	0	1	0	Interface pixel format
		1	↑	1	0	0	0	0	0	D2	D1	D0	
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	module's manufacturer[7:0]								
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	1	LCD module/driver version [6:0]							
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	LCD module/driver ID[7:0]								

Table 8.1 System interface command set

Extended command set

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function	
B0	SETOSC	0	↑	1	-	1	0	1	1	0	0	0	0	Set internal oscillator	
		1	↑	1	-	I_RADJ[3:0](0011)				N_RADJ[3:0](0100)					
B1	SETPWCTR	1	↑	1	-	-	-	-	-	-	-	-	OSC_EN(0)	Set power control	
		0	↑	1	-	1	0	1	1	0	0	0	1		
		1	↑	1	-	-	-	-	-	-	-	-	DP_S TB(0)		DP_S TB_S(0)
		1	↑	1	-	-	-	-	-	-	-	BT[2:0](000)			
		1	↑	1	-	-	-	-	-	-	VRH[5:0](01_1010)				
		1	↑	1	-	-	-	-	-	-	NVRH[5:0](01_1010)				
		1	↑	1	-	-	-	-	-	-	AP[2:0](011)				
B2	SETDISPLAY	1	↑	1	-	FS0[7:0](0000_0001)			FS1[7:0](0001_0001)				Set display control		
		0	↑	1	-	1	0	1	1	0	0	1		0	
		1	↑	1	-	-	-	-	-	-	ISC[3:0](0001)				
		1	↑	1	-	PT[1:0](10)		-	-	-	-	PTG(1)		REF(1)	
B4	SETCYC	1	↑	1	-	-	-	GON(1)	DTE(0)	D[1:0](00)		-	-	Set display cycle	
		0	↑	1	-	1	0	1	1	0	1	0	0		
		1	↑	1	-	-	-	I_NW[1:0](01)		-	-	N_NW[1:0](01)			
		1	↑	1	-	-	-	-	-	-	N_RTN[3:0](1000)				
		1	↑	1	-	-	-	-	-	-	N_DIV[1:0](00)				
		1	↑	1	-	N_DUM[7:0](0000_1100)									
		1	↑	1	-	I_DUM[7:0](0000_1100)									
		1	↑	1	-	GDON[7:0](0000_1101)									
B5	SETBGP	1	↑	1	-	GDON[7:0](0101_0011)									
		0	↑	1	-	1	0	1	1	0	1	0	1	Set BGP voltage	
						NVREF[3:0](0111)			VREF[3:0](0111)						
				FBOF F(0)	VNV DHS_SEL[2:0](011)		-	VVDHS_SEL[2:0](011)							
B6	SETVCOM	0	↑	1	-	1	0	1	1	0	1	1	0	Set VCOM voltage	
		1	↑	1	-	VCOM[6:0](100_1011)									
		1	↑	1	-	-	-	-	-	-	VCM_TIMES[2:0](000)				
B9	SETEXTC	0	↑	1	-	1	0	1	1	1	0	0	1	Enter extension command	
		1	↑	1	-	EXTC1[7:0](0000_0000)									
		1	↑	1	-	EXTC2[7:0](0000_0000)									
BB	SETOTP	1	↑	1	-	EXTC3[7:0](0000_0000)									
		0	↑	1	-	1	0	1	1	1	0	1	1	Set OTP	
		1	↑	1	-	OTP_KEY[7:0](0000_0000)									
		1	↑	1	-	OTP_MASK[7:0](0000_0000)									
1	↑	1	-	OTP_INDEX[7:0](0000_0000)											
C0	SETSTBA	1	↑	1	-	LOAD_DISABLE(0)	VPP_ENABLE(0)	OTP_POR(0)	OTP_PWE(0)	OTP_PTM[1:0](00)		VPP_SEL(0)	OTP_PROG(0)	Set Source option	
		1	↑	1	-	OTPDOUT[7:0](1111_1111)									
		0	↑	1	-	1	1	0	0	0	0	0	0		
		1	↑	1	-	N_OPON[7:0](8'h20)									
		1	↑	1	-	I_OPON[7:0](8'h10)									
		1	↑	1	-	STBA[15:8](8'h0C)									
				STBA[7:0](8'hC7)											
				GENON[7:0](8'h10)											

		1	↑	1	-	-	-	-	-	-	-	-	OTPS 1B (1)				
C3	SETID	0	↑	1	-	1	1	0	0	0	0	1	1	Set ID			
		1	↑	1	-	ID1[7:0] (0000_0000)											
		1	↑	1	-	ID2[7:0] (0000_0000)											
		1	↑	1	-	ID3[7:0] (0000_0000)											
CC	SETPANEL	1	↑	1	-	-	-	-	-	-	-	-	ID_TIMES[2:0] (000)	Set Panel characteristics			
		0	↑	1	-	1	1	0	0	1	1	0	0				
D0	GETHID	1	↑	1	-	-	-	-	-	-	-	-	-	Read Himax internal ID			
		0	1	↑	-	1	1	0	1	0	0	0	0				
		ID_VERSION[7:0] (1000_0101)															
(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function			
E0	SETGAMMA	0	↑	1	-	1	1	1	0	0	0	0	0	Set Gamma			
		1	↑	1	-	-	MP1[2:0] (000)			-	MP0[2:0] (000)						
		1	↑	1	-	-	MP3[2:0] (110)			-	MP2[2:0] (000)						
		1	↑	1	-	-	MP5[2:0] (011)			-	MP4[2:0] (000)						
		1	↑	1	-	-	-	-	-	CP0[3:0] (0110)			CP1[3:0] (1100)				
		1	↑	1	-	-	CP2[3:0] (1000)			-	CP3[3:0] (0010)				CP4[3:0] (0100)		
		1	↑	1	-	-	-	-	-	OP0[3:0] (1111)			OP1[4:0] (0_0110)				
		1	↑	1	-	-	-	-	-	CGM1[1:0] (11)		CGM0[1:0] (10)					
		1	↑	1	-	-	MN1[2:0] (111)			-	MN0[2:0] (100)						
		1	↑	1	-	-	MN3[2:0] (111)			-	MN2[2:0] (001)						
		1	↑	1	-	-	MN5[2:0] (111)			-	MN4[2:0] (111)						
		1	↑	1	-	-	-	-	-	CN0[3:0] (0100)			CN1[3:0] (0010)				
		1	↑	1	-	-	CN2[3:0] (1000)			-	CN3[3:0] (1100)				CN4[3:0] (0110)		
		1	↑	1	-	-	-	-	-	ON0[3:0] (0011)			ON1[4:0] (1_1110)				
		1	↑	1	-	-	-	-	-	ON1[4:0] (1_1110)							
		FE	SET_SPI_RD EN	0	↑	1	-	1	1	1	1	1	1		1	0	SPI READ EN
				1	↑	1	-	A7	A6	A5	A4	A3	A2		A1	A0	Set SPI Read address
FF	GET_SPI_RD EN	0	↑	1	-	1	1	1	1	1	1	1	1	SPI READ EN			
		1	1	↑	-	Get FE A[7:0] parameter									Get FE A[7:0] parameter		
		1	1	↑	-	Get FE A[7:0] parameter											
		1	1	↑	-	Get FE A[7:0] parameter											
		1	1	↑	-	Get FE A[7:0] parameter											
1	1	↑	-	Get FE A[7:0] parameter													

Table 8.2 System Interface In-House Command Set

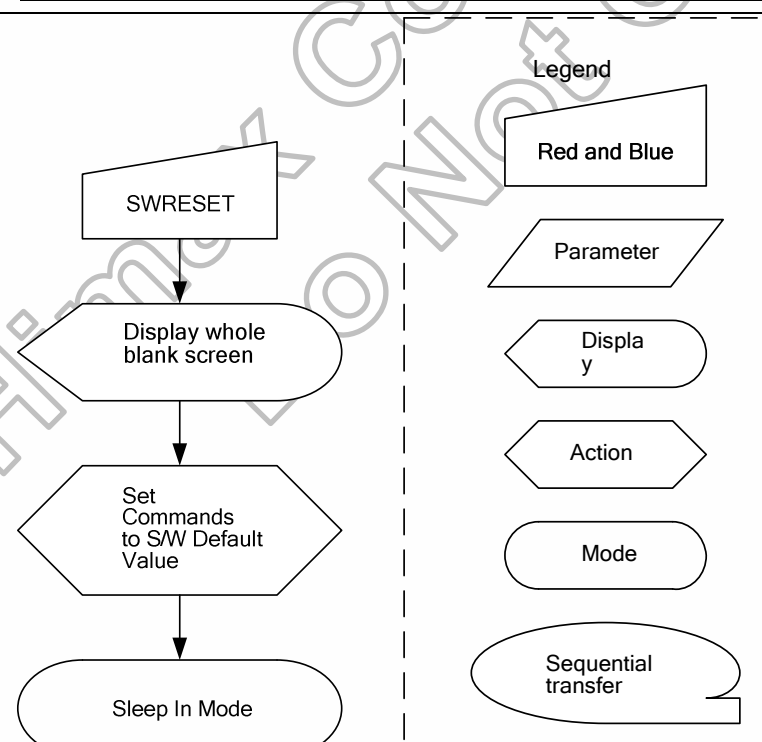
8.2 Command description

8.2.1 NOP

00 H	NOP (No Operation)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR (Memory Write) or RAMRD (Memory Read) command.												
Restriction													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						N/A						
	S/W Reset						N/A						
	H/W Reset						N/A						
Flow Chart	-												

Himax Confidential
Do Not Copy

8.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. Note: The GRAM contents are unaffected by this command.</p>												
Restriction	<p>It will be necessary to wait 5m sec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.</p>												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						N/A						
	S/W Reset						N/A						
	H/W Reset						N/A						
Flow Chart	 <pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> Sleep[Sleep In Mode] </pre>												

8.2.3 Read display identification information (04h)

04 H	RDDIDIF (Read Display Identification Information)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3 rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4 th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	This read byte returns 24-bit display identification information. The 1st Parameter is dummy read. The 2 nd ~ 4th Parameter identifies the LCD module's manufacturer. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:												
	ID Byte Value ID2[7:0]			Version			Changes						
	80h			-			-						
	81h			-			-						
	82h			-			-						
	83h			-			-						
	84h			-			-						
85h			-			-							
The 4th parameter identifies the LCD module/driver.													
Restriction	-												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						See Description						
	S/W Reset						See Description						
	H/W Reset						See Description						
Flow Chart	Serial I/F Mode				Parallel I/F Mode				<div style="border: 1px dashed black; padding: 5px;"> Legend <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px;"></div> Command <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px; transform: rotate(-15deg);"></div> Parameter <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px; border-radius: 10px;"></div> Display <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px; border-radius: 10px;"></div> Action <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px; border-radius: 10px;"></div> Mode <div style="border: 1px solid black; width: 40px; height: 20px; margin-bottom: 5px; border-radius: 10px;"></div> Sequential transfer </div>				
	<div style="text-align: center;"> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto;"></div> RDDID (04h) </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Dummy Clock </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID1[7:0] </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID2[7:0] </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID3[7:0] </div>				<div style="text-align: center;"> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto;"></div> RDDID (04h) </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Dummy Read </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID1[7:0] </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID2[7:0] </div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; width: 60px; height: 30px; margin: 0 auto 10px auto; transform: rotate(-15deg);"> Send ID3[7:0] </div>								

8.2.4 Read display status (09h)

09 H	RDDST (Read Display Status)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	1	09
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	D31	D30	D29	D28	D27	D26	D25	0	-
3 rd parameter	1	1	↑	-	0	D22	D21	D20	D19	D18	D17	D16	-
4 th parameter	1	1	↑	-	D15	0	D13	0	0	D10	D9	D8	-
5 th parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	0	-

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D31	Booster Voltage Status	-
D30	Page Address Order (MY)	-
D29	Column Address Order (MX)	-
D28	Page/Column Order (MV)	-
D27	Line Address Order (ML)	-
D26	RGB/BGR Order	-
D25	Display Data Latch Order	-
D24	Switching between Segment outputs and RAM	Set to '0'
D23	Switching between Common outputs and RAM	Set to '0'
D22	Interface Color Pixel Format Definition	-
D21		-
D20		-
D19	Idle Mode On/Off	-
D18	Partial Mode On/Off	-
D17	Sleep In/Out	-
D16	Display Normal Mode On/Off	-
D15	Vertical Scrolling Status	-
D14	Horizontal Scrolling Status	Set to '0'
D13	Inversion Status	-
D12	All Pixels On	Set to '0'
D11	All Pixels Off	Set to '0'
D10	Display On/Off	-
D9	Tearing Effect Line On/Off	-
D8	Gamma Curve Selection	-
D7		-
D6		-
D5	Tearing Effect Output Line Mode	-
D4	Horizontal Sync. (HS, RGB I/F)	Set to '0'
D3	Vertical Sync. (VS, RGB I/F)	Set to '0'
D2	Pixel Clock (DOTCLK, RGB I/F)	Set to '0'
D1	Data Enable (DE, RGB I/F)	Set to '0'
D0	Parity Error	Set to '0'

Bit Values are explained overleaf.

Bit D31 – Booster Voltage Status
 '0' = Booster Off or has a fault.
 '1' = Booster On and working OK.

Bit D30 – Page Address Order
 '0' = Top to Bottom (When MADCTL B7(MY) = '0').
 '1' = Bottom to Top (When MADCTL B7(MY) = '1').

Bit D29 – Column Address Order
 '0' = Left to Right (When MADCTL B6(MX) = '0').
 '1' = Right to Left (When MADCTL B6(MX) = '1').

Bit D28 – Page / Column Order
 '0' = Normal Mode (When MADCTL B5(MV) = '0').

'1' = Reverse Mode (When MADCTL B5(MV) = '1').
 Bit D27 – Line Address Order
 '0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
 '1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').
 Bit D26 – RGB/BGR Order
 '0' = RGB (When MADCTL B3 = '0').
 '1' = BGR (When MADCTL B3 = '1').
 Bit D25 – Display Data Latch Order
 '0' = LCD Refresh Left to Right (When MADCTL B2 = '0').
 '1' = LCD Refresh Right to Left (When MADCTL B2 = '1').
 Note : For bits D27, D26 and D25 also refer to 8.3.29 Memory Access Control (R36h)
 Bit D24 – Switching Between Segment Outputs and RAM
 This bit is not applicable for this project, so it is set to '0'.
 Bit D23 – Switching Between Common Outputs and RAM
 This bit is not applicable for this project, so it is set to '0'.
 Bits D22, D21, D20 –Interface Color Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 bit/pixel	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Bit D19 – Idle Mode On/Off
 '0' = Idle Mode Off.
 '1' = Idle Mode On.
 Bit D18 – Partial Mode On/Off
 '0' = Partial Mode Off.
 '1' = Partial Mode On.
 Bit D17 – Sleep In/Out
 '0' = Sleep In Mode.
 '1' = Sleep Out Mode.
 Bit D16 – Display Normal Mode On/Off
 '0' = Display Normal Mode Off.
 '1' = Display Normal Mode On.
 Bit D15 – Vertical Scrolling On/Off
 '0' = Vertical Scrolling is Off.
 '1' = Vertical Scrolling is On.
 Bit D14 – Horizontal Scrolling Status
 This bit is not applicable for this project, so it is set to '0'.
 Bit D13 – Inversion On/Off
 '0' = Inversion is Off.
 '1' = Inversion is On.
 Bit D12 – All Pixels On
 This bit is not applicable for this project, so it is set to '0'.
 Bit D11 – All Pixels Off
 This bit is not applicable for this project, so it is set to '0'.
 Bit D10 – Display On/Off
 '0' = Display is Off.
 '1' = Display is On.
 Bit D9 – Tearing Effect Line On/Off
 '0' =Tearing Effect Line Off.
 '1' = Tearing Effect On.

Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Bit D5 – Tearing Effect Line Output Mode.

'0' = Mode 1, V-Blanking only.

'1' = Mode 2, both H-Blanking and V-Blanking.

Bit D4 – Horizontal Sync. (HS) RGB I/F On/Off, Note

This bit is not applicable for this project, so it is set to '0'.

Bit D3 – Vertical Sync. (VS) RGB I/F On/Off, Note

This bit is not applicable for this project, so it is set to '0'.

Bit D2 – Pixel Clock (DOTCLK) RGB I/F On/Off, Note

This bit is not applicable for this project, so it is set to '0'.

Bit D1 – Data Enable (DE) RGB I/F On/Off, Note

This bit is not applicable for this project, so it is set to '0'.

Bit D0 – Parity Error

This bit is not applicable for this project, so it is set to '0'.

Restriction

-

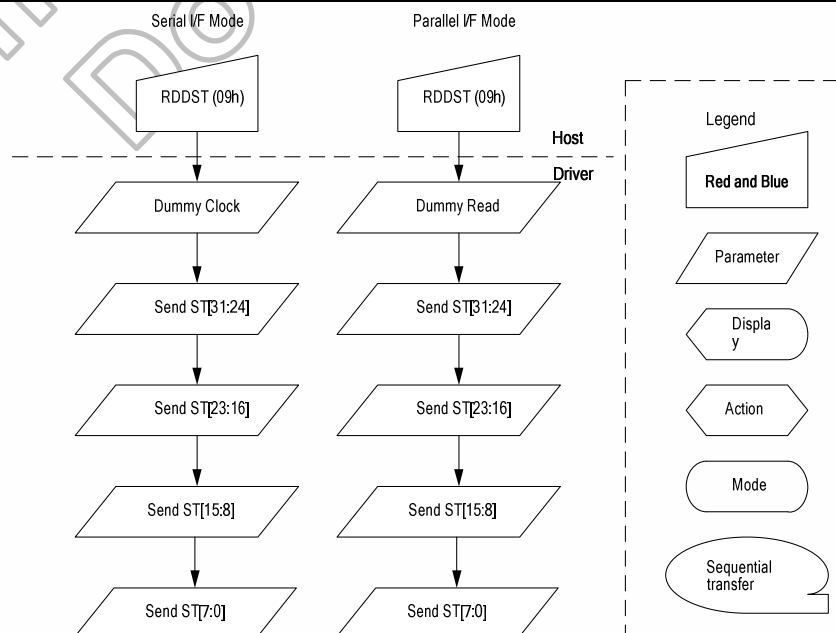
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

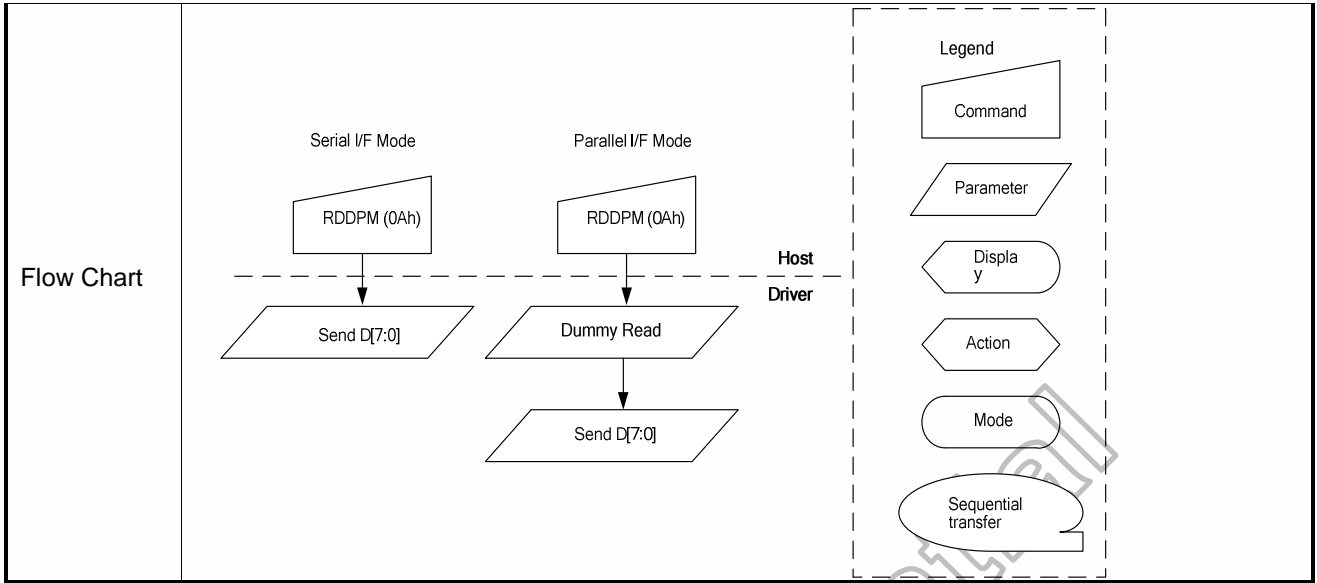
Status	Default Value
Power On Sequence	See Description
S/W Reset	See Description
H/W Reset	See Description

Flow Chart



8.2.5 Read display power mode (0Ah)

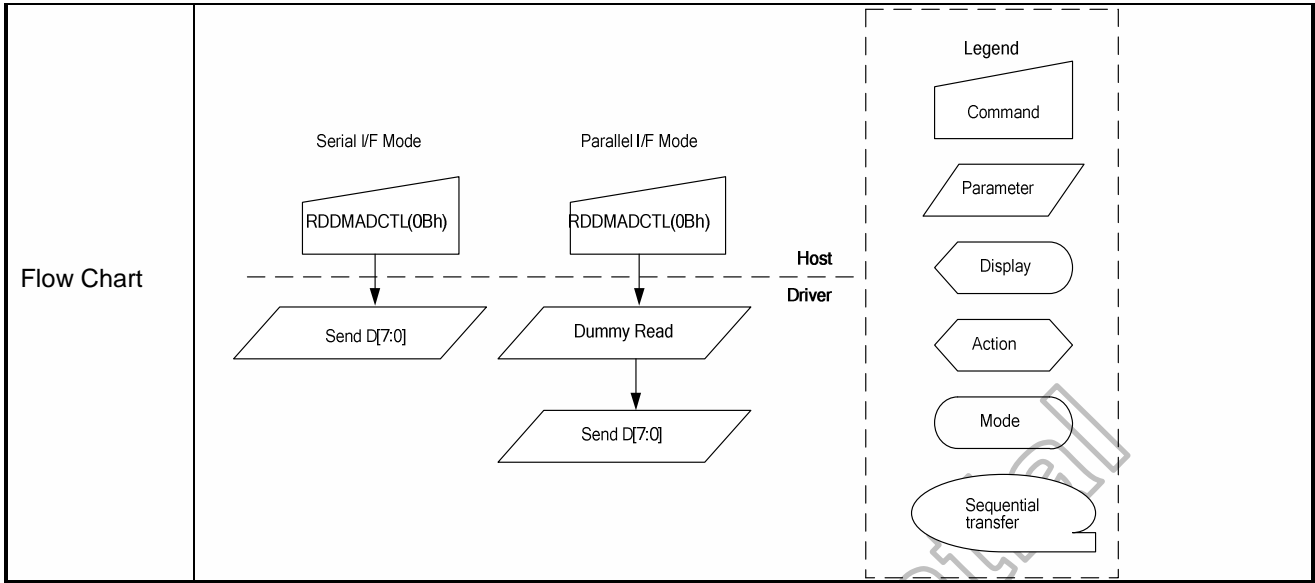
0A H	RDDPM (Read Display Power Mode)																																							
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A																											
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																											
2 nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx																											
Description	This command indicates the current status of the display as described in the table below:																																							
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Booster Voltage Status</td> <td>-</td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td>-</td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td>-</td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td>-</td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td>-</td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td>-</td> </tr> <tr> <td>D1</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> </tbody> </table>													Bit	Description	Comment	D7	Booster Voltage Status	-	D6	Idle Mode On/Off	-	D5	Partial Mode On/Off	-	D4	Sleep In/Out	-	D3	Display Normal Mode On/Off	-	D2	Display On/Off	-	D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
	Bit	Description	Comment																																					
	D7	Booster Voltage Status	-																																					
	D6	Idle Mode On/Off	-																																					
	D5	Partial Mode On/Off	-																																					
	D4	Sleep In/Out	-																																					
	D3	Display Normal Mode On/Off	-																																					
	D2	Display On/Off	-																																					
	D1	Not Defined	Set to '0'																																					
D0	Not Defined	Set to '0'																																						
Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets display supplier's optical requirements).																																								
Bit D6 – Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On.																																								
Bit D5 – Partial Display Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On.																																								
Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.																																								
Bit D3 – Normal Display Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On.																																								
Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On.																																								
Bit D1 – Not Defined This bit is not applicable for this project, so it is set to '0'.																																								
Bit D0 – Not Defined This bit is not applicable for this project, so it is set to '0'.																																								
Restrictions	-																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																
	Status	Availability																																						
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
	Normal Mode On, Idle Mode On, Sleep Out	Yes																																						
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
	Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In or Booster Off	Yes																																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>08h</td> </tr> <tr> <td>S/W Reset</td> <td>08h</td> </tr> <tr> <td>H/W Reset</td> <td>08h</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	08h	S/W Reset	08h	H/W Reset	08h																				
	Status	Default Value																																						
	Power On Sequence	08h																																						
	S/W Reset	08h																																						
H/W Reset	08h																																							



Himax Confidential
Do Not Copy

8.2.6 Read display MADCTL (0Bh)

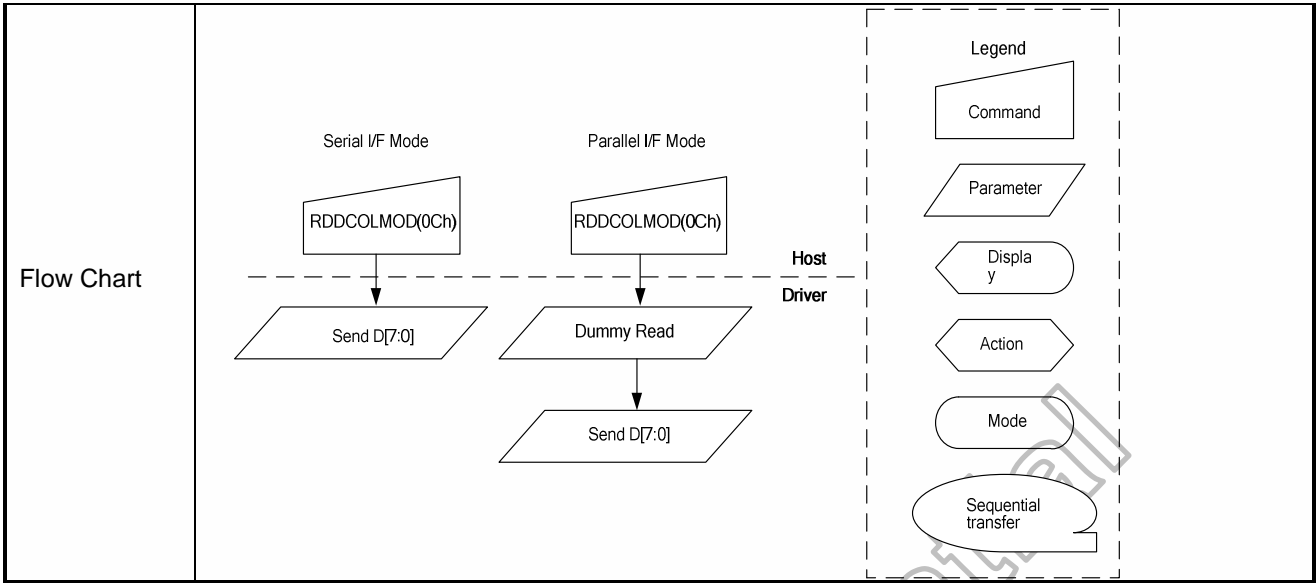
0B H	RDDMADCTL (Read Display MADCTL)												HEX																											
Command	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B																											
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																											
2 nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx																											
Description	This command indicates the current status of the display as described in the table below:																																							
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Page Address Order</td> <td>-</td> </tr> <tr> <td>D6</td> <td>Column Address Order</td> <td>-</td> </tr> <tr> <td>D5</td> <td>Page/Column Order</td> <td>-</td> </tr> <tr> <td>D4</td> <td>Line Address Order</td> <td>-</td> </tr> <tr> <td>D3</td> <td>RGB/BGR Order</td> <td>-</td> </tr> <tr> <td>D2</td> <td>Display Data Latch Order</td> <td>-</td> </tr> <tr> <td>D1</td> <td>Switching between Segment outputs and RAM</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Switching between Common outputs and RAM</td> <td>Set to '0'</td> </tr> </tbody> </table>													Bit	Description	Comment	D7	Page Address Order	-	D6	Column Address Order	-	D5	Page/Column Order	-	D4	Line Address Order	-	D3	RGB/BGR Order	-	D2	Display Data Latch Order	-	D1	Switching between Segment outputs and RAM	Set to '0'	D0	Switching between Common outputs and RAM	Set to '0'
	Bit	Description	Comment																																					
	D7	Page Address Order	-																																					
	D6	Column Address Order	-																																					
	D5	Page/Column Order	-																																					
	D4	Line Address Order	-																																					
	D3	RGB/BGR Order	-																																					
	D2	Display Data Latch Order	-																																					
	D1	Switching between Segment outputs and RAM	Set to '0'																																					
D0	Switching between Common outputs and RAM	Set to '0'																																						
Bit D7 – Page Address Order '0' = Top to Bottom (When MADCTL B7(MY) = '0'). '1' = Bottom to Top (When MADCTL B7(MY) = '1').																																								
Bit D6 – Column Address Order '0' = Left to Right (When MADCTL B6(MX) = '0'). '1' = Right to Left (When MADCTL B6(MX) = '1').																																								
Bit D5 –Page / Column Order '0' = Normal Mode (When MADCTL B5(MV) = '0'). '1' = Reverse Mode (When MADCTL B5(MV) = '1').																																								
Bit D4 – Line Address Order '0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').																																								
Bit D3 – RGB/BGR Order '0' = RGB (When MADCTL B3 = '0'). '1' = BGR (When MADCTL B3 = '1'). Note: For bits D4, D3 and D2 also refer to 8.2.29 Memory Access Control (R36h)																																								
Bit D2 – Display Data Latch Order Display Data Latch Data Order '0' = LCD Refresh Left to Right (When MADCTL B2='0'). '1' = LCD Refresh Right to Left (When MADCTL B2='1').																																								
Bit D1 – Switching Between Segment Outputs and RAM This bit is not applicable for this project, so it is set to '0'.																																								
Bit D0 – Switching Between Common Outputs and RAM This bit is not applicable for this project, so it is set to '0'.																																								
Restrictions	-																																							
Register Availability	Status						Availability																																	
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																																	
	Normal Mode On, Idle Mode On, Sleep Out						Yes																																	
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																																	
	Partial Mode On, Idle Mode On, Sleep Out						Yes																																	
	Sleep In or Booster Off						Yes																																	
Default	Status						Default Value																																	
	Power On Sequence						00h																																	
	S/W Reset						No Change																																	
	H/W Reset						00h																																	



Himax Confidential
Do Not Copy

8.2.7 Read display pixel format (0Ch)

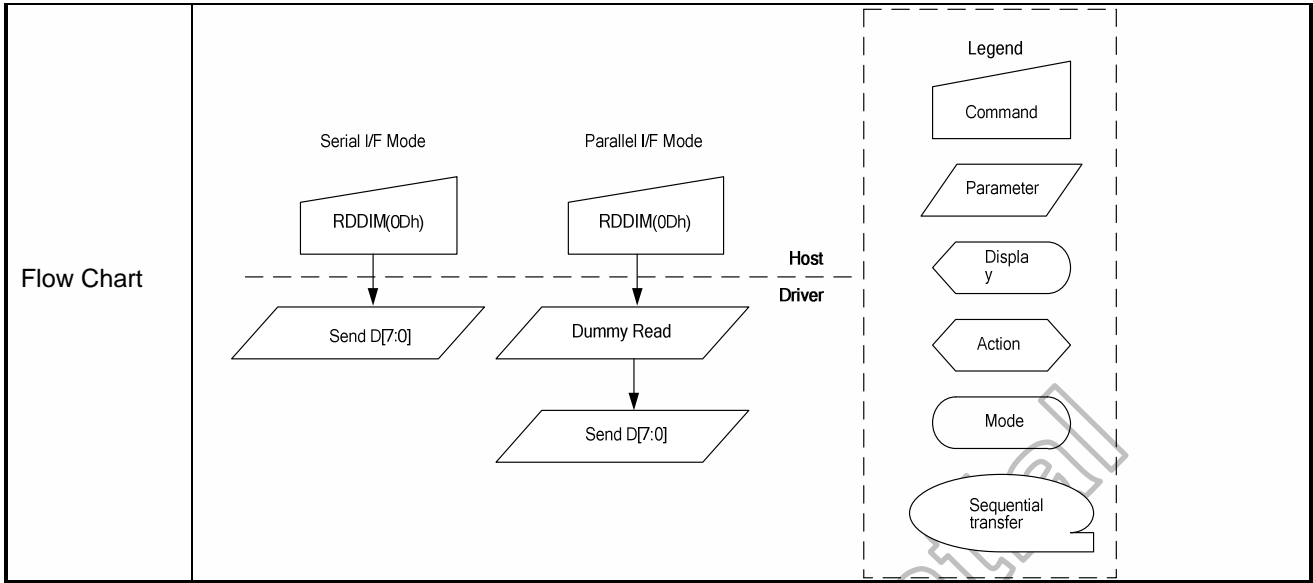
0C H	RDDCOLMOD (Read Display COLMOD)												HEX	
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C	
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-	
2 nd parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	xx	
Description	This command indicates the current status of the display as described in the table below:													
	Bit		Description										Comment	
	D7		RGB Interface Color Format										Set to '0'	
	D6												Set to '0'	
	D5												Set to '0'	
	D4												Set to '0'	
	D3		System Interface Color Format										Set to '0'	
	D2												-	
	D1												-	
	D0												-	
	Bit D7 – RGB Interface Color Format Selection This bit is not applicable for this project, so it is set to '0'. Bits D6, D5, D4 – RGB Interface Color Pixel Format Definition These bits are not applicable for this project, so they are set to '0's'. Bit D3 – System Interface Color Format Selection This bit is not applicable for this project, so it is set to '0'. Bit D2, D1, D0 – Control Interface Color Pixel Format Definition. See section "8.2.33 Interface Pixel Format (R3Ah)".													
	System Interface Color Format						D2	D1	D0					
	Not Defined						0	0	0					
	Not Defined						0	0	1					
	Not Defined						0	1	0					
Not Defined						0	1	1						
Not Defined						1	0	0						
16 bit/pixel						1	0	1						
18 bit/pixel						1	1	0						
Not Defined						1	1	1						
Restrictions														
Register Availability	Status						Availability							
	Normal Mode On, Idle Mode Off, Sleep Out						Yes							
	Normal Mode On, Idle Mode On, Sleep Out						Yes							
	Partial Mode On, Idle Mode Off, Sleep Out						Yes							
	Partial Mode On, Idle Mode On, Sleep Out						Yes							
Sleep In or Booster Off						Yes								
Default	Status						Default Value							
	Power On Sequence						18-bit/pixel							
	S/W Reset						No Change							
	H/W Reset						18-bit/pixel							



Himax Confidential
Do Not Copy

8.2.8 Read display image mode (0Dh)

0D H	RDDIM (Read Display Image Mode)																																																									
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D																																													
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																																													
2 nd parameter	1	1	↑	-	D7	0	D5	0	0	D2	D1	D0	xx																																													
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off ‘0’ = Vertical Scrolling is Off. ‘1’ = Vertical Scrolling is On. Bit D6 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to ‘0’ Bit D5 – Inversion On/Off ‘0’ = Inversion is Off. ‘1’ = Inversion is On. This bit is not applicable for this project, so it is set to ‘0’ Bit D4 – All Pixels On This bit is not applicable for this project, so it is set to ‘0’ Bit D3 – All Pixels Off This bit is not applicable for this project, so it is set to ‘0’ Bits D2, D1, D0 – Gamma Curve Selection																																																									
	<table border="1"> <thead> <tr> <th>Gamma Curve Selected</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (R26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve 2</td> <td>0</td> <td>0</td> <td>1</td> <td>GC1</td> </tr> <tr> <td>Gamma Curve 3</td> <td>0</td> <td>1</td> <td>0</td> <td>GC2</td> </tr> <tr> <td>Gamma Curve 4</td> <td>0</td> <td>1</td> <td>1</td> <td>GC3</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>													Gamma Curve Selected	D2	D1	D0	Gamma Set (R26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
	Gamma Curve Selected	D2	D1	D0	Gamma Set (R26h) Parameter																																																					
	Gamma Curve 1	0	0	0	GC0																																																					
	Gamma Curve 2	0	0	1	GC1																																																					
	Gamma Curve 3	0	1	0	GC2																																																					
	Gamma Curve 4	0	1	1	GC3																																																					
	Not Defined	1	0	0	Not Defined																																																					
	Not Defined	1	0	1	Not Defined																																																					
	Not Defined	1	1	0	Not Defined																																																					
Not Defined	1	1	1	Not Defined																																																						
Restrictions	-																																																									
Register Availability	Status						Availability																																																			
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																																																			
	Normal Mode On, Idle Mode On, Sleep Out						Yes																																																			
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																																																			
	Partial Mode On, Idle Mode On, Sleep Out						Yes																																																			
Sleep In or Booster Off						Yes																																																				
Default	Status						Default Value																																																			
	Power On Sequence						00h																																																			
	S/W Reset						00h																																																			
	H/W Reset						00h																																																			



Himax Confidential
Do Not Copy

8.2.9 Read display signal mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												HEX												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E												
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx												
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off ‘0’ = Tearing Effect Line Off. ‘1’ = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 7.3 for mode definitions. ‘0’ = Mode 1. ‘1’ = Mode 2. Bit D5 – Horizontal Sync. (VSYNC, RGB I/F) On/Off This bit is not applicable for this project, so it is set to ‘0’ Bit D4 – Vertical Sync. (HSYNC, RGB I/F) On/Off This bit is not applicable for this project, so it is set to ‘0’ Bit D3 – Pixel Clock (DCLK, RGB I/F) On/Off This bit is not applicable for this project, so it is set to ‘0’ Bit D2 – Data Enable (ENABLE, RGB I/F) On/Off This bit is not applicable for this project, so it is set to ‘0’ D1 are D0 - are for future use and are set to ‘0’.																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart																									

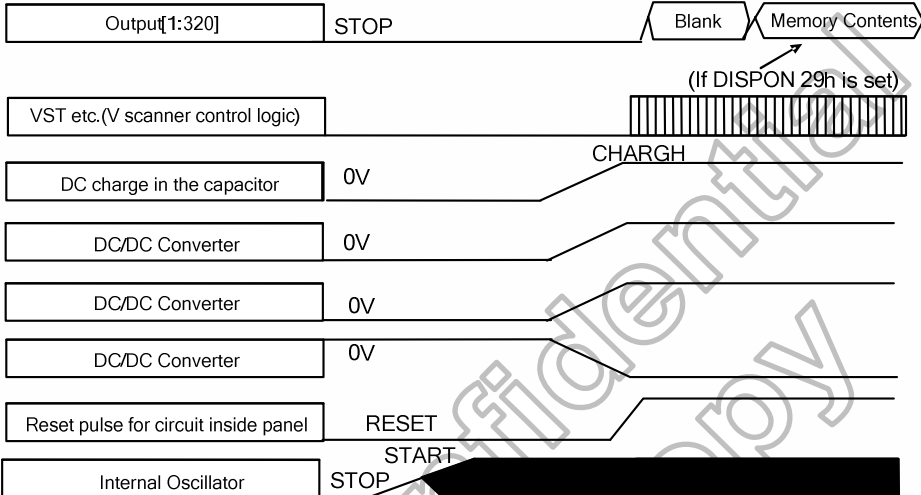
8.2.10 Read display self-diagnostic result (0Fh)

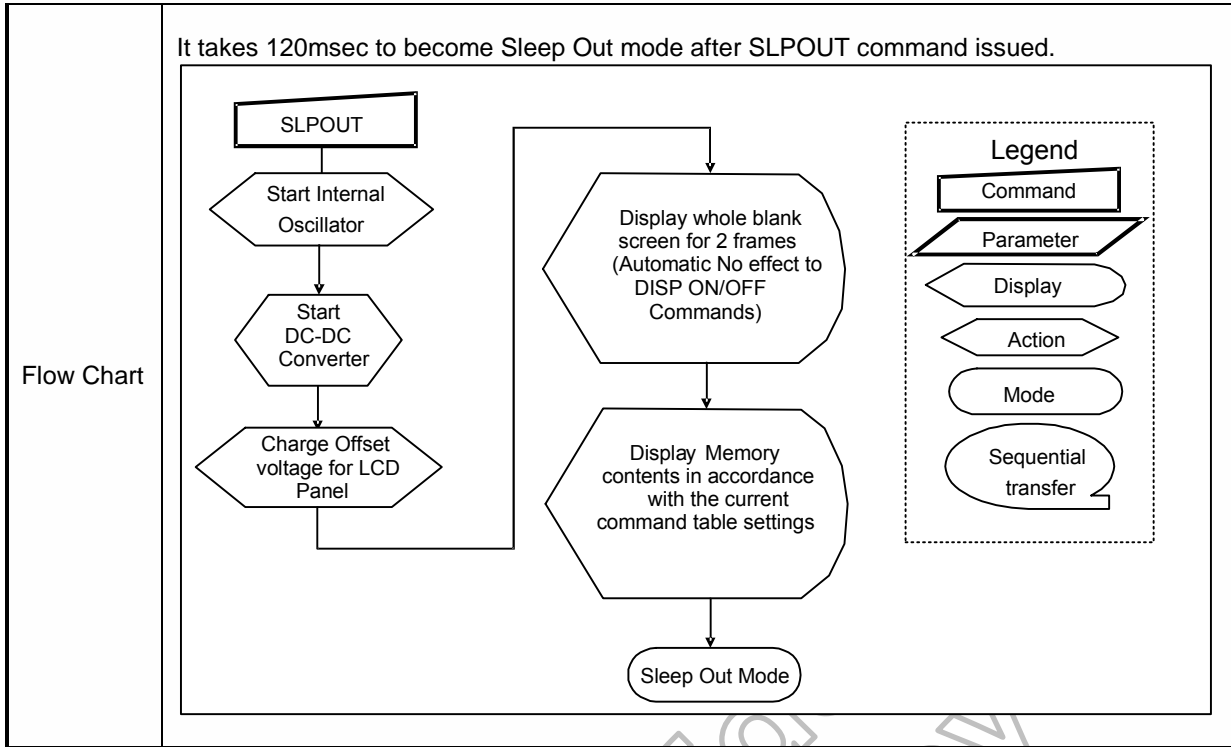
0F H	RDDSDR (Read Display Self-Diagnostic Result)																								
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F												
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd parameter	1	1	↑	-	D7	D6	D5	D4	0	0	0	0	-												
Description	This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below: Bit D7 – Register Loading Detection See section 7.6.1. Bit D6 – Functionality Detection See section 7.6.2. Bit D5 – Chip Attachment Detection Set bit D5 to '0', if this function is not implemented. Bit D4 – Display Glass Break Detection Set bit D4 to '0', if this function is not implemented. Bits D3, D2, D1 and D0 are for future use and are set to '0'.																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart																									

8.2.11 Sleep in (10h)

10 H	SLPIN (Sleep In)																								
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	1	0	0	0	0	10												
Parameter	NO PARAMETER																								
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p>																								
	<p>MCU interface and memory are still working and the memory keeps its contents.</p>																								
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
S/W Reset	Sleep In Mode																								
H/W Reset	Sleep In Mode																								
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>																								

8.2.12 Sleep out (11h)

11 H	SLPOUT (Sleep Out)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> 												
	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display suppliers' factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image. If factory default and register values are same when this load is done and when the display module is already Sleep Out -mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>												
Register Availability	Status		Availability										
	Normal Mode On, Idle Mode Off, Sleep Out		Yes										
	Normal Mode On, Idle Mode On, Sleep Out		Yes										
	Partial Mode On, Idle Mode Off, Sleep Out		Yes										
	Partial Mode On, Idle Mode On, Sleep Out		Yes										
Sleep In or Booster Off		Yes											
Default	Status		Default Value										
	Power On Sequence		Sleep In Mode										
	S/W Reset		Sleep In Mode										
	H/W Reset		Sleep In Mode										



Himax Confidential
Do Not Copy

8.2.13 Partial mode on (12h)

12 H	PTLON (Partial Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. See also section 6.3.8												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Normal Display Mode On						
	S/W Reset						Normal Display Mode On						
	H/W Reset						Normal Display Mode On						
Flow Chart	See Partial Area (30h)												

Himax Confidential
Do Not Copy

8.2.14 Normal display mode on (13h)

13 H	NORON (Normal Display Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. See also section 6.2.1.												
Restriction	This command has no effect when Normal mode is active.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						Normal Display Mode On						
	S/W Reset						Normal Display Mode On						
	H/W Reset						Normal Display Mode On						
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

Himax Confidential
Do Not Copy

8.2.15 Display inversion off (20h)

20 H	INVOFF (Display Inversion Off)																								
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20												
Parameter	NO PARAMETER																								
Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: center; align-items: center;"> <div style="text-align: center;"> <p>memory</p> </div> <div style="margin: 0 20px;"> <p>⇒</p> </div> <div style="text-align: center;"> <p>display</p> </div> </div>																								
Restriction	-																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off				
Status	Default Value																								
Power On Sequence	Display Inversion Off																								
S/W Reset	Display Inversion Off																								
H/W Reset	Display Inversion Off																								
Flow Chart	<div style="border: 1px solid black; padding: 10px;"> <div style="display: flex; justify-content: space-between;"> <div style="width: 60%;"> <pre> graph TD A([Display Inversion On Mode]) --> B[INVOFF] B --> C([Display Inversion OFF Mode]) </pre> </div> <div style="width: 35%; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div> </div>																								

8.2.16 Display inversion on (21h)

21 H	INVON (Display Inversion On)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	<p>This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>memory</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>display</p> </div> </div>												
	Restriction												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						Display Inversion Off						
	S/W Reset						Display Inversion Off						
	H/W Reset						Display Inversion Off						
Flow Chart	<div style="border: 1px solid black; padding: 10px;"> <div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Display Inversion OFF Mode</p> <p>↓</p> <p>INVON</p> <p>↓</p> <p>Display Inversion ON Mode</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; gap: 5px;"> <div style="border: 1px solid black; width: 50px; height: 15px; margin: 0 auto;"></div> <p style="text-align: center;">Command</p> <div style="border: 1px solid black; width: 50px; height: 15px; transform: rotate(-15deg); margin: 0 auto;"></div> <p style="text-align: center;">Parameter</p> <div style="border: 1px solid black; width: 50px; height: 15px; transform: rotate(-30deg); margin: 0 auto;"></div> <p style="text-align: center;">Display</p> <div style="border: 1px solid black; width: 50px; height: 15px; transform: rotate(-15deg); margin: 0 auto;"></div> <p style="text-align: center;">Action</p> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 5px; margin: 0 auto;"></div> <p style="text-align: center;">Mode</p> <div style="border: 1px solid black; width: 50px; height: 15px; border-radius: 10px; margin: 0 auto;"></div> <p style="text-align: center;">Sequential transfer</p> </div> </div> </div> </div>												

8.2.17 Gamma set (26h)

26 H	GAMSET (Gamma Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	1	1	0	26
Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-
Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:												
	GC[7..0]		Parameter		Curve Selected								
	01h		GC0		Gamma Curve 1								
	02h		GC1		Gamma Curve 2								
	04h		GC2		Gamma Curve 3								
08h		GC3		Gamma Curve 4									
Note: All other values are undefined.													
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the Current selected Gamma curve until valid value is received.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						01h						
	S/W Reset						01h						
	H/W Reset						01h						
Flow Chart	<pre> graph TD A[GAMSET] --> B[/GC [7:0]/] B --> C{{New Gamma Curve Loaded}} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: [] Action: <> Mode: [] Sequential transfer: [] 												

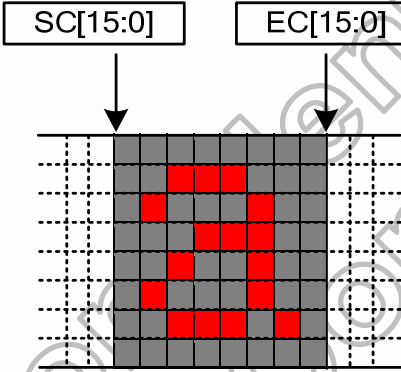
8.2.18 Display off (28h)

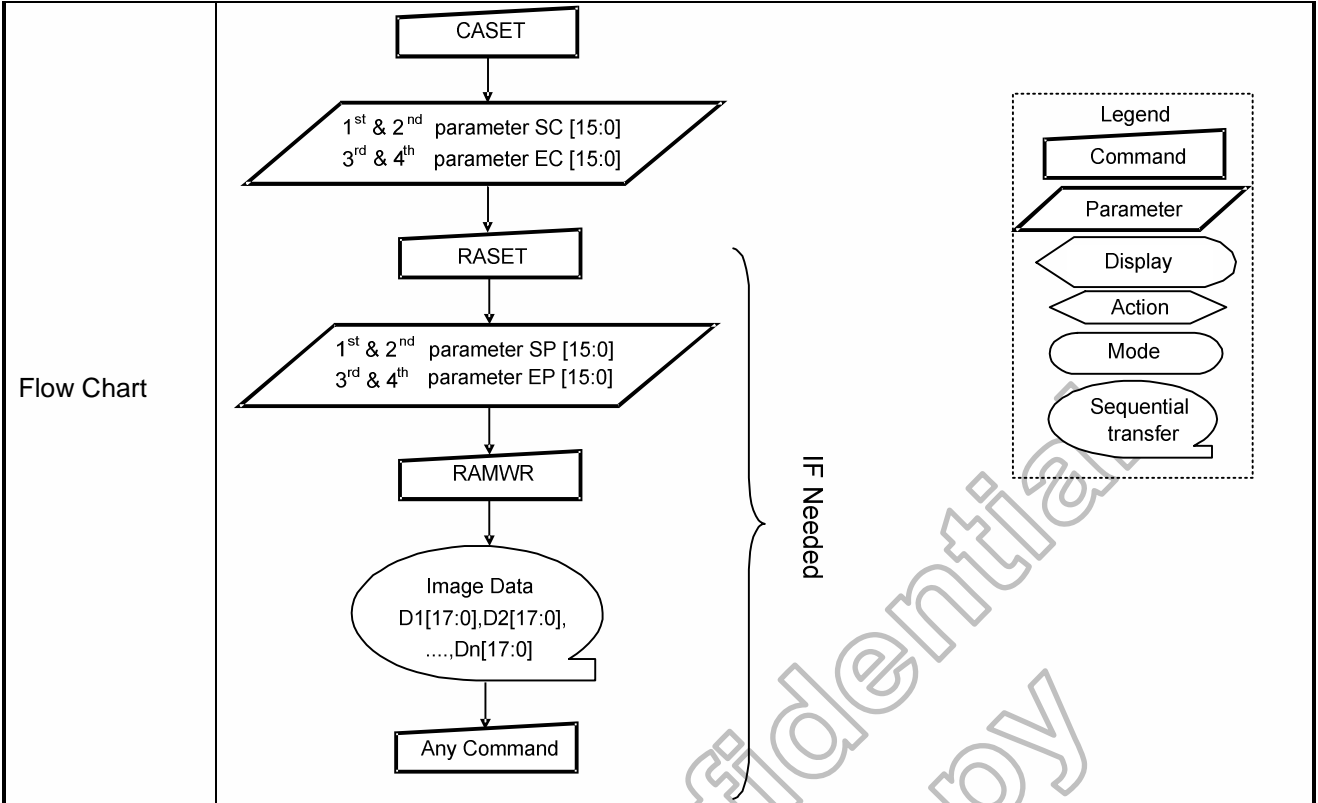
28 H	DISPOFF (Display Off)																								
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28												
Parameter	NO PARAMETER																								
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example)</p> <div style="text-align: center;"> </div>																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
S/W Reset	Display Off																								
H/W Reset	Display Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																								

8.2.19 Display on (29h)

29 H	DISPON (Display On)																								
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	0	1	29												
Parameter	NO PARAMETER																								
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example)</p> <div style="text-align: center;"> </div>																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
S/W Reset	Display Off																								
H/W Reset	Display Off																								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																								

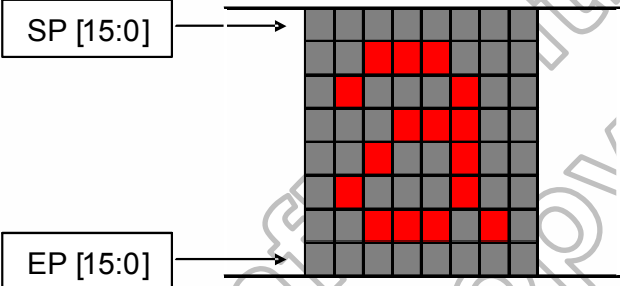
8.2.20 Column address set (2Ah)

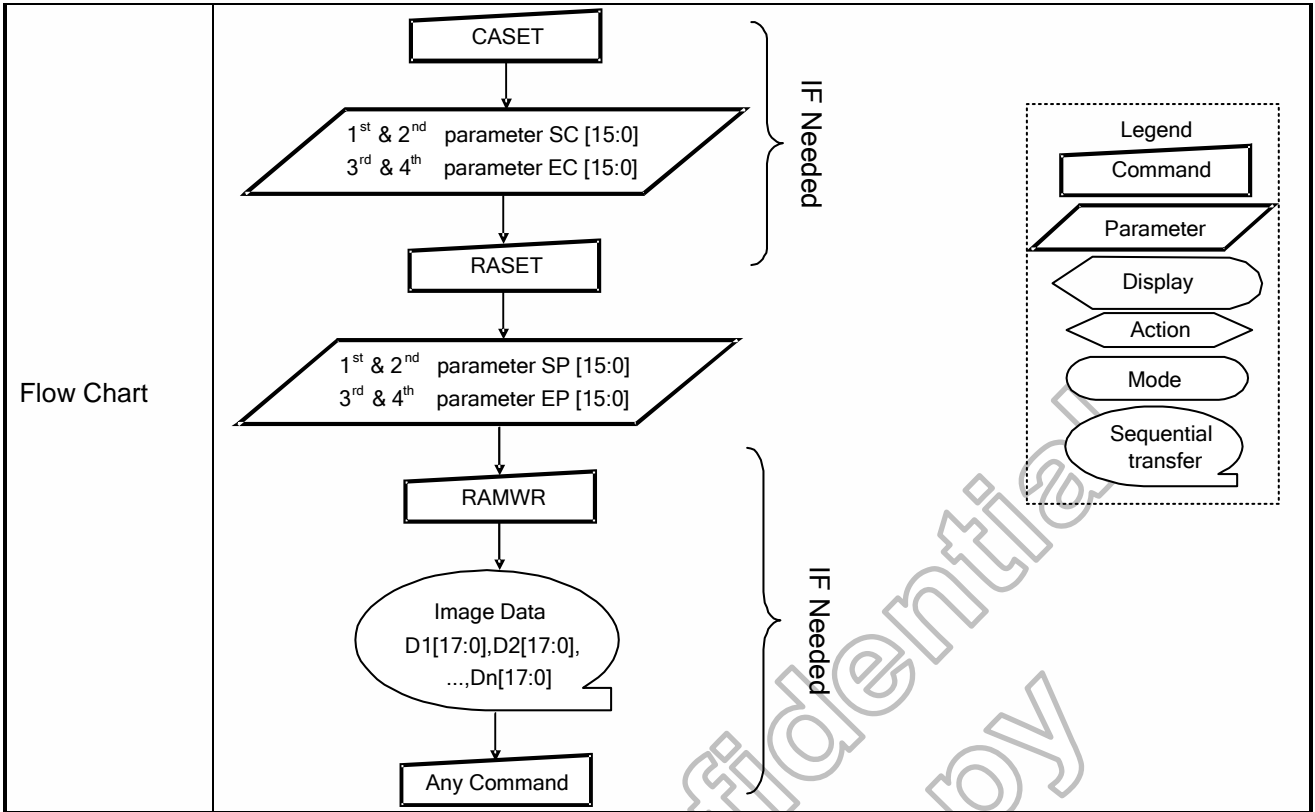
2A H	CASET (Column Address Set)												HEX																			
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0																				
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A																			
1st parameter	1	↑	1	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note																			
2nd parameter	1	↑	1	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0																				
3rd parameter	1	↑	1	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note																			
4th parameter	1	↑	1	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0																				
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p> <p>(Example)</p> 																															
Restriction	<p>SC[15:0] always must be equal to or less than EC[15:0] Note: When SC[15:0] or EC[15:0] is greater than maximum address like below, data out of range will be ignored 0000h ≤ SC[15:0] ≤ EC[15:0] ≤ 0083h, when MADCTL's B5=0 0000h ≤ SC[15:0] ≤ EC[15:0] ≤ 00A1h, when MADCTL's B5=1</p>																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In or Booster Off	Yes																															
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SC[15:0]=0000h</td> <td>EC[15:0]=0083h</td> </tr> <tr> <td rowspan="3">S/W Reset</td> <td colspan="2">When MADCTL's B5=0:</td> </tr> <tr> <td>SC[15:0]=0000h</td> <td>EC[15:0]=0083h</td> </tr> <tr> <td colspan="2">When MADCTL's B5=1:</td> </tr> <tr> <td></td> <td>SC[15:0]=0000h</td> <td>EC[15:0]=00A1h</td> </tr> <tr> <td>H/W Reset</td> <td>SC[15:0]=0000h</td> <td>EC[15:0]=0083h</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SC[15:0]=0000h	EC[15:0]=0083h	S/W Reset	When MADCTL's B5=0:		SC[15:0]=0000h	EC[15:0]=0083h	When MADCTL's B5=1:			SC[15:0]=0000h	EC[15:0]=00A1h	H/W Reset	SC[15:0]=0000h	EC[15:0]=0083h
Status	Default Value																															
Power On Sequence	SC[15:0]=0000h	EC[15:0]=0083h																														
S/W Reset	When MADCTL's B5=0:																															
	SC[15:0]=0000h	EC[15:0]=0083h																														
	When MADCTL's B5=1:																															
	SC[15:0]=0000h	EC[15:0]=00A1h																														
H/W Reset	SC[15:0]=0000h	EC[15:0]=0083h																														



Himax Confidential
Do Not Copy

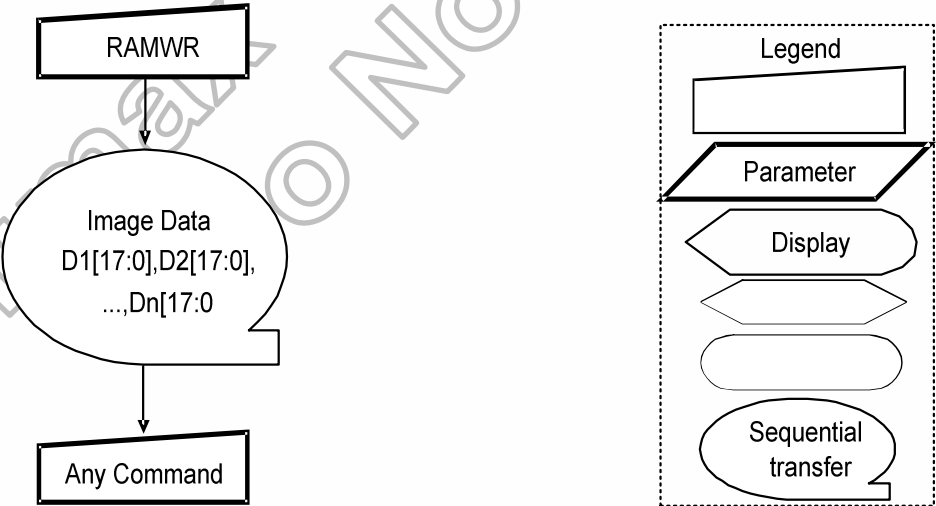
8.2.21 Page address set (2Bh)

2B H	PASET (Page Address Set)																														
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B																		
1st parameter	1	↑	1	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note																		
2nd parameter	1	↑	1	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0																			
3rd parameter	1	↑	1	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note																		
4th parameter	1	↑	1	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0																			
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.</p> <p style="text-align: center;">(Example)</p> <div style="text-align: center;">  </div>																														
Restriction	<p>SP[15:0] always must be equal to or less than EP[15:0] Note: When SP[15:0] or EP[15:0] is greater than maximum row address like below, data of out of range will be ignored 0000h ≤ SP[15:0] ≤ EP[15:0] ≤ 00A1h (When MADCTL's B5=0) 0000h ≤ SP[15:0] ≤ EP[15:0] ≤ 0083h (When MADCTL's B5=1)</p>																														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In or Booster Off	Yes																														
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th colspan="2" style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SP[15:0]=0000h</td> <td>EP[15:0]=00A1h</td> </tr> <tr> <td rowspan="4">S/W Reset</td> <td colspan="2" style="text-align: center;">When MADCTL's B5=0:</td> </tr> <tr> <td>SP[15:0]=0000h</td> <td>EP[15:0]=00A1h</td> </tr> <tr> <td colspan="2" style="text-align: center;">When MADCTL's B5=1:</td> </tr> <tr> <td>SP[15:0]=0000h</td> <td>EP[15:0]=0083h</td> </tr> <tr> <td>H/W Reset</td> <td>SP[15:0]=0000h</td> <td>EP[15:0]=00A1h</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SP[15:0]=0000h	EP[15:0]=00A1h	S/W Reset	When MADCTL's B5=0:		SP[15:0]=0000h	EP[15:0]=00A1h	When MADCTL's B5=1:		SP[15:0]=0000h	EP[15:0]=0083h	H/W Reset	SP[15:0]=0000h	EP[15:0]=00A1h
Status	Default Value																														
Power On Sequence	SP[15:0]=0000h	EP[15:0]=00A1h																													
S/W Reset	When MADCTL's B5=0:																														
	SP[15:0]=0000h	EP[15:0]=00A1h																													
	When MADCTL's B5=1:																														
	SP[15:0]=0000h	EP[15:0]=0083h																													
H/W Reset	SP[15:0]=0000h	EP[15:0]=00A1h																													



Himax Confidential
Do Not Copy

8.2.22 Memory write (2Ch)

2C H	RAMWR (Memory Write)																								
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C												
1st parameter	1	↑	1	D1[15:0]									00..FF												
:	1	↑	1	Dx[15:0]									00..FF												
nth parameter	1	↑	1	Dn[15:0]									00..FF												
Description	<p>This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2) Then D[7:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write.</p>																								
Restriction	In all color modes, there is no restriction on length of parameters.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is not cleared																								
H/W Reset	Contents of memory is not cleared																								
Flow Chart																									

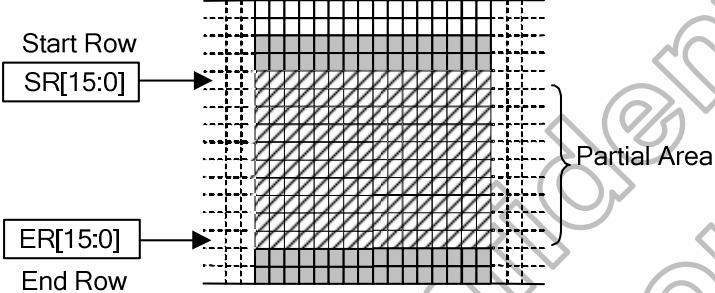
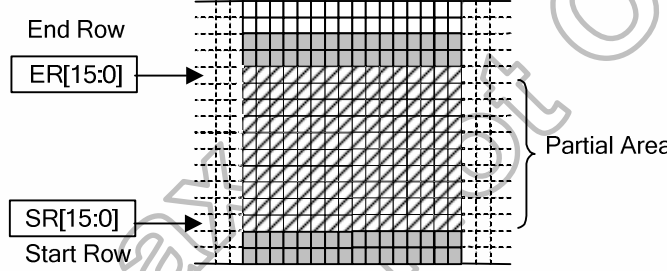
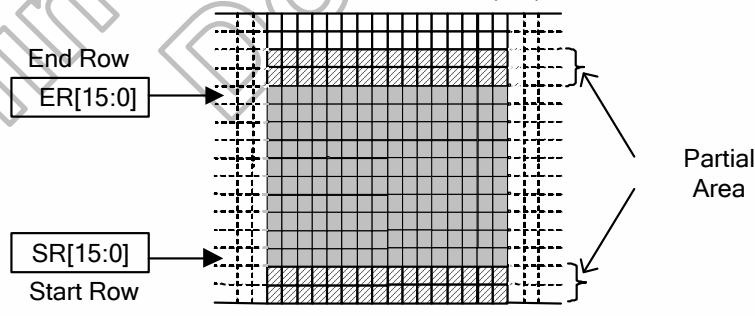
8.2.23 Color set (2Dh)

2D H	RGBSET (Color Set)											
	DNC	NRD	NWR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	HEX
Command	0	1	↑	0	0	1	0	1	1	0	1	2D
1st parameter	1	1	↑	X	X	R005	R004	R003	R002	R001	R000	00..FF
:	1	1	↑	X	X	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	00..FF
32 th parameter	1	1	↑	X	X	R315	R314	R313	R312	R311	R310	00..FF
33rd parameter	1	1	↑	X	X	G005	G004	G003	G002	G001	G000	00..FF
:	1	1	↑	X	X	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	00..FF
96 th parameter	1	1	↑	X	X	G635	G634	G633	G632	G631	G630	00..FF
97 th parameter	1	1	↑	X	X	B005	B004	B003	B002	B001	B000	00..FF
:	1	1	↑	X	X	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	00..FF
128th parameter	1	1	↑	X	X	B315	B314	B313	B312	B311	B310	00..FF
Description	This command is used to define the LUT for 12bit-to-18bit/16bit-to-18bit color depth conversions. (See also section 5.2) 128 bytes must be written to the LUT regardless of the color mode. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.											
Restriction	-											
Register Availability	Status						Availability					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
Sleep In or Booster Off						Yes						
Default	Status						Default Value					
	Power On Sequence						Random values					
	S/W Reset						Contents of the look-up table protected					
	H/W Reset						Random values					
Flow Chart												

8.2.24 Memory read (2Eh)

2E H	RAMRD (Memory Read)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	D1[15:0]								00..FF	
:	1	↑	1	Dx[15:0]								00..FF	
(n+1)th parameter	1	↑	1	Dn[15:0]								00..FF	
Description	<p>This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.</p> <p>The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2)</p> <p>Then D[7:0] is read back from the frame memory and the column register and the page register incremented</p> <p>Frame Read can be stopped by sending any other command.</p>												
Restriction	-												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						Contents of memory is set randomly						
	S/W Reset						Contents of memory is not cleared						
	H/W Reset						Contents of memory is not cleared						
Flow Chart	<pre> graph TD A[RAMRD] --> B[/Dummy/] B --> C([Image Data D1[17:0], D2[17:0] ..., Dn[17:0]]) C --> D[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval with arrow Action: Oval with arrow Mode: Oval Sequential transfer: Oval with tail 												

8.2.25 Partial area (30h)

30 H	PLTAR (Partial Area)												HEX	
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30	
1st parameter	1	↑	1	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000:	
2nd parameter	1	↑	1	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	013F	
3rd parameter	1	↑	1	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000:	
4th parameter	1	↑	1	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	013F	
Description	<p>This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>If End Row > Start Row when MADCTL B4(ML) = 0:</p>  <p>If End Row > Start Row when MADCTL B4(ML) = 1:</p>  <p>If End Row < Start Row when MADCTL's B4(ML) = 0:</p>  <p>If End Row = Start Row then the Partial Area will be one row deep.</p>													
	Restriction	SR[15:0] and ER[15:0] cannot be exceeding than 00A1h.												

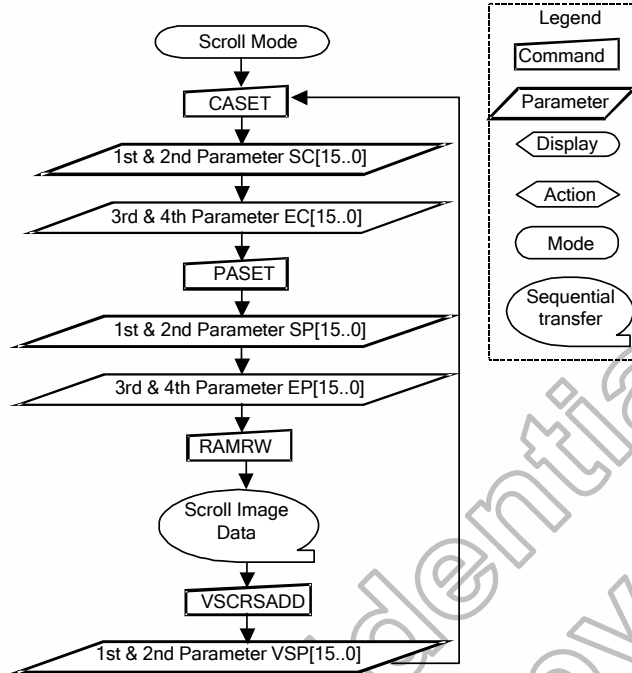
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In or Booster Off		Yes
Default	Status		Default Value
	Power On Sequence	SR[15:0]=0000h	ER[15:0]=00A1h
	S/W Reset	SR[15:0]=0000h	ER[15:0]=00A1h
	H/W Reset	SR[15:0]=0000h	ER[15:0]=00A1h
Flow Chart	1. To Enter Partial Display Mode:		
	<pre> graph TD PLTAR[PLTAR] --> SR[SR[15:0]] SR --> ER[ER[15:0]] ER --> PTLON[PTLON] PTLON --> PM[Partial Mode] </pre>		
Flow Chart	2. To Leave Partial Display Mode		
	<pre> graph TD PM[Partial Mode] --> DISPOFF[DISPOFF] DISPOFF --> NORON[NORON] NORON --> PMOFF[Partial Mode OFF] PMOFF --> RAMRW[RAMRW] RAMRW --> ID[Image Data] ID --> DISPON[DISPON] </pre> <p>(Optional) To prevent Tearing Effect Image displayed</p>		

8.2.26 Vertical scrolling definition (33h)

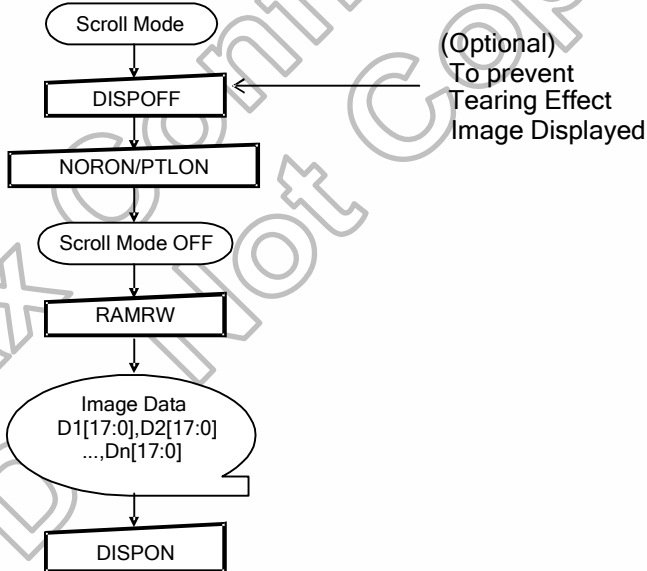
33 H	VSCRDEF (Vertical Scrolling Definition)												HEX
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1st parameter	1	↑	1	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	0000:
2nd parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	00A2
3rd parameter	1	↑	1	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	0000:
4th parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	00A2
5 th parameter	1	↑	1	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	0000:
6 th parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	00A2
Description	<p>This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>												
	<p>When MADCTL B4=1 The 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p>												
Restriction	<p>The condition is (TFA+VSA+BFA)=162, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.</p>												

<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes				
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In or Booster Off	Yes																
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="3">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>TFA[15:0]=0000</td> <td>VSA[15:0]=00A2h</td> <td>BFA[15:0]=0000</td> </tr> <tr> <td>S/W Reset</td> <td>TFA[15:0]=0000</td> <td>VSA[15:0]=00A2h</td> <td>BFA[15:0]=0000</td> </tr> <tr> <td>H/W Reset</td> <td>TFA[15:0]=0000</td> <td>VSA[15:0]=00A2h</td> <td>BFA[15:0]=0000</td> </tr> </tbody> </table>	Status	Default Value			Power On Sequence	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000	S/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000	H/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000
Status	Default Value																
Power On Sequence	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000														
S/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000														
H/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000														
<p>Flow Charts</p>	<p>1. To enter Vertical Scroll Mode:</p> <p>Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.</p>																

2. Continuous Scroll:



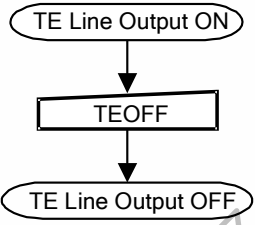
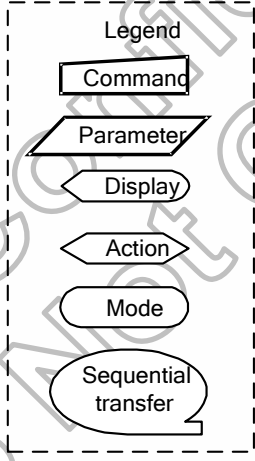
3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

8.2.27 Tearing effect line off (34h)

34 H	TEOFF (Tearing Effect Line OFF)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												

Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.	
Restriction	This command has no effect when Tearing Effect output is already OFF.	
Register Availability	Status	
	Normal Mode On, Idle Mode Off, Sleep Out	
	Normal Mode On, Idle Mode On, Sleep Out	
	Partial Mode On, Idle Mode Off, Sleep Out	
	Partial Mode On, Idle Mode On, Sleep Out	
Sleep In or Booster Off		Availability
		Yes
		Yes
		Yes
		Yes
		Yes
Default	Status	
	Power On Sequence	
	S/W Reset	
	H/W Reset	
		Default Value
		Tearing Effect Off
		Tearing Effect Off
		Tearing Effect Off
Flow Chart	 <pre> graph TD A([TE Line Output ON]) --> B[TEOFF] B --> C([TE Line Output OFF]) </pre>	
		

8.2.28 Tearing effect line on (35h)

35 H	TEON (Tearing Effect Line ON)												HEX
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35
1stparameter	0	↑	1	-	-	-	-	-	-	-	-	TEMODE	-
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When TEMODE=0: The Tearing Effect Output line consists of V-Blanking information only:</p> <p>When TEMODE=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>												
	Restriction	This command has no effect when Tearing Effect output is already ON.											
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						Tearing Effect Off						
	S/W Reset						Tearing Effect Off						
	H/W Reset						Tearing Effect Off						
Flow Chart													
	<p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / Display: < Action: > Mode: () Sequential transfer: () 												

8.2.29 Memory access control (36h)

36 H	MADCTL (Memory Access Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1st parameter	1	↑	1	-	MY	MX	MV	ML	BGR	SS	-	-	-

This command defines read/write scanning direction of frame memory.
 This command makes no change on the other driver status.
 Bit Assignment

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. See Section 6.2.1 "MCU to memory write/read direction"
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
SS	Horizontal ORDER	LCD horizontal refresh direction control

ML="0"

ML="1"

BGR="0"

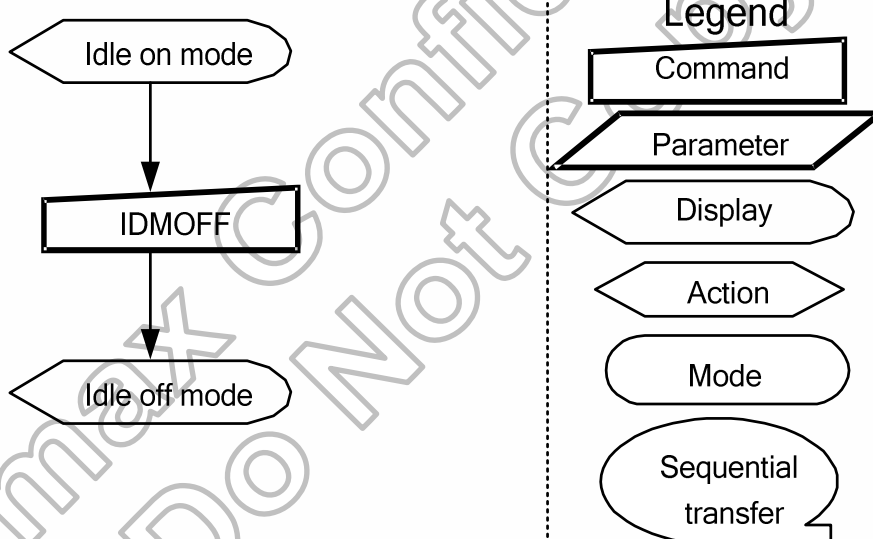
BGR="1"

	<p style="text-align: center;">SS- Horizontal Updating order</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>SS="0"</p> </div> <div style="text-align: center;"> <p>SS="1"</p> </div> </div> <p>Note: Top-Left (0,0) means a physical memory location.</p>												
Restriction	<p>D1 and D0 are set to '00' internally. D2 is implemented if the LCD is updating pixel-by pixel. D2 is set to '0' internally if the LCD is updating line-by-line.</p>												
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In or Booster Off	Yes												
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	No Change												
H/W Reset	00h												
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

8.2.30 Vertical scrolling start address (37h)

37 H	VSCRSADD (Vertical Scrolling Start Address)																								
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37												
1 st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	01.												
2 nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	3F												
	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:</p> <p>When MADCTL B4='0' Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'</p> <p>When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'</p> <p>When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.</p>																								
Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<p>See Vertical Scrolling Definition (33h) description.</p>																								

8.2.31 Idle mode off (38h)

38 H	IDMOFF (Idle Mode Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors.												
Restriction	1. This command has no effect when module is already in idle off mode. 2. RGB I/F enable, this command is working as a NOP (00h) command.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Idle Mode Off						
	S/W Reset						Idle Mode Off						
	H/W Reset						Idle Mode Off						
Flow Chart	 <pre> graph TD A[Idle on mode] --> B[IDMOFF] B --> C[Idle off mode] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Arrowhead Mode: Oval Sequential transfer: Callout box 												

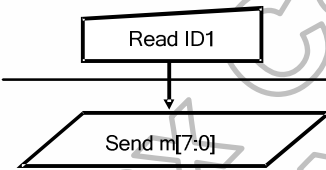
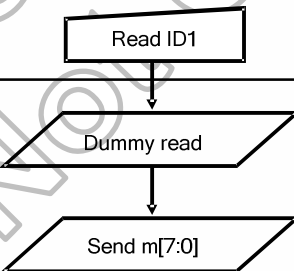
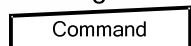
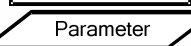

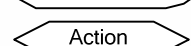
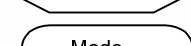
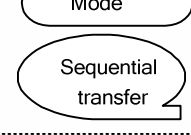
8.2.32 Idle mode on (39h)

39 H	IDMON (Idle Mode On)																																																			
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39																																							
Parameter	NO PARAMETER																																																			
Description	<p>This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p> <p>(Example)</p>																																																			
	<table border="1"> <thead> <tr> <th colspan="4">Memory contents vs. Display Color</th> </tr> <tr> <th></th> <th>R₅ R₄ R₃ R₂ R₁ R₀</th> <th>G₅ G₄ G₃ G₂ G₁ G₀</th> <th>B₅ B₄ B₃ B₂ B₁ B₀</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table>													Memory contents vs. Display Color					R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX
Memory contents vs. Display Color																																																				
	R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₅ B ₄ B ₃ B ₂ B ₁ B ₀																																																	
Black	0XXXXX	0XXXXX	0XXXXX																																																	
Blue	0XXXXX	0XXXXX	1XXXXX																																																	
Red	1XXXXX	0XXXXX	0XXXXX																																																	
Magenta	1XXXXX	0XXXXX	1XXXXX																																																	
Green	0XXXXX	1XXXXX	0XXXXX																																																	
Cyan	0XXXXX	1XXXXX	1XXXXX																																																	
Yellow	1XXXXX	1XXXXX	0XXXXX																																																	
White	1XXXXX	1XXXXX	1XXXXX																																																	
Restriction	This command has no effect when module is already in idle off mode.																																																			
Register Availability	Status						Availability																																													
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																																													
	Normal Mode On, Idle Mode On, Sleep Out						Yes																																													
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																																													
	Partial Mode On, Idle Mode On, Sleep Out						Yes																																													
Sleep In or Booster Off						Yes																																														
Default	Status						Default Value																																													
	Power On Sequence						Idle Mode Off																																													
	S/W Reset						Idle Mode Off																																													
	H/W Reset						Idle Mode Off																																													
Flow Chart																																																				
	<p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Arrow Mode: Oval Sequential transfer: Double-headed arrow 																																																			

8.2.33 Interface pixel format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1 st parameter	1	↑	1	-	-	-	-	-	-	D2	D1	D0	011, 101, 110
Description	This command is used to define the format of RGB picture data, which is to be transfer via the system interface. The formats are shown in the table:												
	Interface Format		D2	D1	D0								
	Not Defined		0	0	0								
	Not Defined		0	0	1								
	Not Defined		0	1	0								
	12 Bit/Pixel		0	1	1								
	Not Defined		1	0	0								
	16 Bit/Pixel		1	0	1								
	18 Bit/Pixel		1	1	0								
Not Defined		1	1	1									
Restriction	-												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						18-bit/pixel						
	S/W Reset						No Change						
	H/W Reset						18-bit/pixel						
Flow Chart	<p>Example:</p> <pre> graph TD A([16Bit/Pixel Mode]) --> B[COLMOD] B --> C[/110/] C --> D([18 Bit/Pixel Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: [] Parameter: [/ /] Display: <> Action: <-> Mode: () Sequential transfer: [] 												

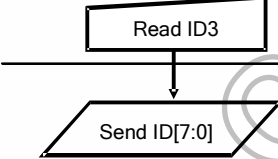
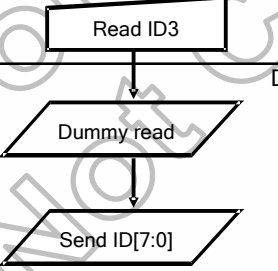
8.2.34 Read ID1 (DAh)

DA H	RDID1 (Read ID1)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	module's manufacturer m[7:0]							-	
Description	This read byte identifies the LCD module's manufacturer.												
Restriction	-												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						xxHEX						
	S/W Reset						xxHEX						
	H/W Reset						xxHEX						
Flow Chart	Serial I/F Mode						Parallel I/F Mode						
													
<div style="border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none">  Command  Parameter  Display  Action  Mode  Sequential transfer </div>													

8.2.35 Read ID2 (DBh)

DB H	RDID2 (Read ID2)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	1	V6	V5	V4	V3	V2	V1	V0	-
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See the following table.												
	ID Byte Value V[7:0]		Version				Changes						
	80h		-				-						
	81h		-				-						
	82h		-				-						
	83h		-				-						
	84h		-				-						
85h		-				-							
Restrictions													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						See Description						
	S/W Reset						See Description						
	H/W Reset						See Description						
Flow Chart	Serial I/F Mode						Parallel I/F Mode						Host Display

8.2.36 Read ID3 (DCh)

DC H	RDID3 (Read ID3)												
	DN C	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	-
Description	This read byte identifies the LCD module/driver.												
Restrictions													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						xxHEX						
	S/W Reset						xxHEX						
	H/W Reset						xxHEX						
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p>  </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p>  </div> </div> <div style="margin-top: 20px; text-align: right;"> <p>Host Display</p> </div> <div style="border: 1px dashed black; padding: 5px; margin-top: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>												

8.2.37 SETOSC: set internal oscillator (B0h)

B0 H	SETOSC(Set Internal Oscillator)													HEX																																																																																																					
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0																																																																																																							
Command	0	↑	1	-	1	0	1	1	0	0	0	0	B0																																																																																																						
1 st parameter	1	↑	1	-	I_RADJ[3:0]				N_RADJ[3:0]				34																																																																																																						
2 nd parameter	1	↑	1	-	-	-	-	-	-	-	-	OSC_EN	00																																																																																																						
Description	<p>These command is used to set internal oscillator related setting OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. N_RADJ[3:0]: Internal oscillator frequency adjusts in Normal / Partial mode. I_RADJ[3:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.</p> <p>For details, please refer to "7.1 Internal Oscillator" section.</p> <table border="1"> <thead> <tr> <th>RADJ3</th> <th>RADJ2</th> <th>RADJ1</th> <th>RADJ0</th> <th>Internal Oscillator Frequency</th> <th>Display Frame rate</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>50% x 6MHz</td><td>30Hz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>67% x 6MHz</td><td>40Hz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>75% x 6MHz</td><td>45Hz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>83% x 6MHz</td><td>50Hz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>100% x 6MHz</td><td>60Hz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>108% x 6MHz</td><td>65Hz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>117% x 6MHz</td><td>70Hz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>125% x 6MHz</td><td>75Hz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>100% x 6MHz</td><td>60Hz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>125% x 6MHz</td><td>75Hz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>141% x 6MHz</td><td>85Hz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>158% x 6MHz</td><td>95Hz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>183% x 6MHz</td><td>110Hz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>191% x 6MHz</td><td>115Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>200% x 6MHz</td><td>120Hz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>217% x 6MHz</td><td>130Hz</td></tr> </tbody> </table>													RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency	Display Frame rate	0	0	0	0	50% x 6MHz	30Hz	0	0	0	1	67% x 6MHz	40Hz	0	0	1	0	75% x 6MHz	45Hz	0	0	1	1	83% x 6MHz	50Hz	0	1	0	0	100% x 6MHz	60Hz	0	1	0	1	108% x 6MHz	65Hz	0	1	1	0	117% x 6MHz	70Hz	0	1	1	1	125% x 6MHz	75Hz	1	0	0	0	100% x 6MHz	60Hz	1	0	0	1	125% x 6MHz	75Hz	1	0	1	0	141% x 6MHz	85Hz	1	0	1	1	158% x 6MHz	95Hz	1	1	0	0	183% x 6MHz	110Hz	1	1	0	1	191% x 6MHz	115Hz	1	1	1	0	200% x 6MHz	120Hz	1	1	1	1	217% x 6MHz	130Hz
	RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency	Display Frame rate																																																																																																													
	0	0	0	0	50% x 6MHz	30Hz																																																																																																													
	0	0	0	1	67% x 6MHz	40Hz																																																																																																													
	0	0	1	0	75% x 6MHz	45Hz																																																																																																													
	0	0	1	1	83% x 6MHz	50Hz																																																																																																													
	0	1	0	0	100% x 6MHz	60Hz																																																																																																													
	0	1	0	1	108% x 6MHz	65Hz																																																																																																													
	0	1	1	0	117% x 6MHz	70Hz																																																																																																													
	0	1	1	1	125% x 6MHz	75Hz																																																																																																													
	1	0	0	0	100% x 6MHz	60Hz																																																																																																													
	1	0	0	1	125% x 6MHz	75Hz																																																																																																													
	1	0	1	0	141% x 6MHz	85Hz																																																																																																													
	1	0	1	1	158% x 6MHz	95Hz																																																																																																													
	1	1	0	0	183% x 6MHz	110Hz																																																																																																													
	1	1	0	1	191% x 6MHz	115Hz																																																																																																													
	1	1	1	0	200% x 6MHz	120Hz																																																																																																													
1	1	1	1	217% x 6MHz	130Hz																																																																																																														
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command																																																																																																																		
Register Availability	Status						Availability																																																																																																												
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																																																																																																												
	Normal Mode On, Idle Mode On, Sleep Out						Yes																																																																																																												
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																																																																																																												
	Partial Mode On, Idle Mode On, Sleep Out						Yes																																																																																																												
Default	Status						Default Value																																																																																																												
	Power On Sequence						OSC_EN=0, N_RADJ[2:0]=4'b0100, I_RADJ[2:0]=4'b0011.																																																																																																												
	S/W Reset						OSC_EN=0, others no change																																																																																																												
	H/W Reset						OSC_EN=0, N_RADJ[2:0]=4'b0100, I_RADJ[2:0]=4'b0011.																																																																																																												
Flow Chart	-																																																																																																																		

8.2.38 SETPOWER: set power (B1h)

B1 H	SETPOWER (Set Power)																																																																																																																																																																																																									
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HE X																																																																																																																																																																																													
Command	0	↑	1	-	1	0	1	1	0	0	0	1	B1																																																																																																																																																																																													
1 st parameter	1	↑	1	-	-	-	-	-	-	-	DP_STB	DP_STB_S	00																																																																																																																																																																																													
2 nd parameter	1	↑	1	-	-	-	-	-	-	BT[2:0]			00																																																																																																																																																																																													
3 rd parameter	1	↑	1	-	-	-	VRH[5:0]						1A																																																																																																																																																																																													
4 th parameter	1	↑	1	-	-	-	NVRH[5:0]						1A																																																																																																																																																																																													
5 th parameter	1	↑	1	-	-	-	-	-	-	AP[2:0]			03																																																																																																																																																																																													
6 th parameter	1	↑	1	-	FS0[7:0]							01																																																																																																																																																																																														
7 th parameter	1	↑	1	-	FS1[7:0]							11																																																																																																																																																																																														
Description	<p>DP_STB, DP_STB_S : These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained.</p> <p>BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.</p> <table border="1"> <thead> <tr> <th>BT2</th> <th>BT1</th> <th>BT0</th> <th>VSP</th> <th>VSN</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>5.0V</td><td>-5.0V</td><td>14.8V</td><td>-12.5V</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>5.0V</td><td>-5.0V</td><td>14.8V</td><td>-10.1V</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>5.0V</td><td>-5.0V</td><td>14.8V</td><td>-7.5V</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>5.0V</td><td>-5.0V</td><td>12.5V</td><td>-12.5V</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>5.0V</td><td>-5.0V</td><td>12.5V</td><td>-10.1V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>5.0V</td><td>-5.0V</td><td>12.5V</td><td>-7.5V</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>5.0V</td><td>-5.0V</td><td>10.0V</td><td>-10.1V</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>5.0V</td><td>-5.0V</td><td>10.0V</td><td>-7.5V</td></tr> </tbody> </table> <p>Note: When VCI = 2.8V, TRI=0, @ IVGH=50uA, IVGL=-50uA</p> <p>VRH[5:0]: Specify the VSPROUT voltage adjusting. VSPROUT voltage is for gamma voltage setting. $VSPROUT = \text{Decimal}(VRH[5:0]) \times 0.05 + 3.3$. The default value is 1Bh(27x0.05+3.3=4.65V)</p> <table border="1"> <thead> <tr> <th>VRH5</th> <th>VRH4</th> <th>VRH3</th> <th>VRH2</th> <th>VRH1</th> <th>VRH0</th> <th>VSPROUT (TRI=0)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>3.30</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>3.35</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>3.40</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3.45</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>3.50</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>3.55</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>3.60</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>3.65</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>4.55</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>4.6</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>STOP</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>STOP</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>STOP</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>STOP</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Internal circuit operations stop. The gamma voltage can be adjusted from external VSPROUT input.</td></tr> </tbody> </table> <p>Note : Please make sure VSPROUT=VSP-0.2V</p>													BT2	BT1	BT0	VSP	VSN	VGH	VGL	0	0	0	5.0V	-5.0V	14.8V	-12.5V	0	0	1	5.0V	-5.0V	14.8V	-10.1V	0	1	0	5.0V	-5.0V	14.8V	-7.5V	0	1	1	5.0V	-5.0V	12.5V	-12.5V	1	0	0	5.0V	-5.0V	12.5V	-10.1V	1	0	1	5.0V	-5.0V	12.5V	-7.5V	1	1	0	5.0V	-5.0V	10.0V	-10.1V	1	1	1	5.0V	-5.0V	10.0V	-7.5V	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VSPROUT (TRI=0)	0	0	0	0	0	0	3.30	0	0	0	0	0	1	3.35	0	0	0	0	1	0	3.40	0	0	0	0	1	1	3.45	0	0	0	1	0	0	3.50	0	0	0	1	0	1	3.55	0	0	0	1	1	0	3.60	0	0	0	1	1	1	3.65	:	:	:	:	:	:	:	0	1	1	0	0	1	4.55	0	1	1	0	1	0	4.6	0	1	1	0	1	1	STOP	0	1	1	1	0	0	STOP	:	:	:	:	:	:	:	1	1	1	1	0	1	STOP	1	1	1	1	1	0	STOP	1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VSPROUT input.
	BT2	BT1	BT0	VSP	VSN	VGH	VGL																																																																																																																																																																																																			
	0	0	0	5.0V	-5.0V	14.8V	-12.5V																																																																																																																																																																																																			
	0	0	1	5.0V	-5.0V	14.8V	-10.1V																																																																																																																																																																																																			
	0	1	0	5.0V	-5.0V	14.8V	-7.5V																																																																																																																																																																																																			
	0	1	1	5.0V	-5.0V	12.5V	-12.5V																																																																																																																																																																																																			
	1	0	0	5.0V	-5.0V	12.5V	-10.1V																																																																																																																																																																																																			
	1	0	1	5.0V	-5.0V	12.5V	-7.5V																																																																																																																																																																																																			
	1	1	0	5.0V	-5.0V	10.0V	-10.1V																																																																																																																																																																																																			
	1	1	1	5.0V	-5.0V	10.0V	-7.5V																																																																																																																																																																																																			
VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VSPROUT (TRI=0)																																																																																																																																																																																																				
0	0	0	0	0	0	3.30																																																																																																																																																																																																				
0	0	0	0	0	1	3.35																																																																																																																																																																																																				
0	0	0	0	1	0	3.40																																																																																																																																																																																																				
0	0	0	0	1	1	3.45																																																																																																																																																																																																				
0	0	0	1	0	0	3.50																																																																																																																																																																																																				
0	0	0	1	0	1	3.55																																																																																																																																																																																																				
0	0	0	1	1	0	3.60																																																																																																																																																																																																				
0	0	0	1	1	1	3.65																																																																																																																																																																																																				
:	:	:	:	:	:	:																																																																																																																																																																																																				
0	1	1	0	0	1	4.55																																																																																																																																																																																																				
0	1	1	0	1	0	4.6																																																																																																																																																																																																				
0	1	1	0	1	1	STOP																																																																																																																																																																																																				
0	1	1	1	0	0	STOP																																																																																																																																																																																																				
:	:	:	:	:	:	:																																																																																																																																																																																																				
1	1	1	1	0	1	STOP																																																																																																																																																																																																				
1	1	1	1	1	0	STOP																																																																																																																																																																																																				
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VSPROUT input.																																																																																																																																																																																																				

NVRH[5:0]: Specify the VSNR voltage adjusting. VSNR voltage is for gamma voltage setting. $VSNR = \text{Decimal}(-3.3 - nVNRH[5:0]) \times 0.05$. The default value is 1Bh $(-3.3 - 27 \times 0.05 = -4.65V)$

NVRH5	NVRH4	NVRH3	NVRH2	NVRH1	NVRH0	VSNROUT (TRI=0)
0	0	0	0	0	0	-3.30
0	0	0	0	0	1	-3.35
0	0	0	0	1	0	-3.40
0	0	0	0	1	1	-3.45
0	0	0	1	0	0	-3.50
0	0	0	1	0	1	-3.55
0	0	0	1	1	0	-3.60
0	0	0	1	1	1	-3.65
:	:	:	:	:	:	:
0	1	1	0	0	1	-4.55
0	1	1	0	1	0	-4.6
0	1	1	0	1	1	STOP
0	1	1	1	0	0	STOP
:	:	:	:	:	:	:
1	1	1	1	0	1	STOP
1	1	1	1	1	0	STOP
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VSNR input.

Note : Please make sure $VSNR = VSN + 0.2V$

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Small

FS0[7:0]: Set the operating frequency for VSP and VSN voltage generation.

FS07	FS06	FS05	FS04	FS03	FS02	FS01	FS00	Operation Frequency for VSP and VSN
0	0	0	0	0	0	0	0	$f_{osc}/1$
0	0	0	0	0	0	0	1	$f_{osc}/1$
0	0	0	0	0	0	1	0	$f_{osc}/2$
0	0	0	0	0	0	1	1	$f_{osc}/3$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$f_{osc}/254$
1	1	1	1	1	1	1	1	$f_{osc}/255$

FS1[7:0]: Set the operating frequency for VGH and VGL voltage generation.

FS17	FS16	FS15	FS14	FS13	FS12	FS11	FS10	Operation Frequency for VGH and VGL
0	0	0	0	0	0	0	0	$f_{osc}/1$
0	0	0	0	0	0	0	1	$f_{osc}/1$
0	0	0	0	0	0	1	0	$f_{osc}/2$
0	0	0	0	0	0	1	1	$f_{osc}/3$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$f_{osc}/254$
1	1	1	1	1	1	1	1	$f_{osc}/255$

Note: Ensure that the operation frequency of $FS1 \geq FS0$.

Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In or Booster Off	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1</td> </tr> <tr> <td>SW Reset</td> <td>VCOMG=0, PON=0, DK=1, STB=1, othes no change</td> </tr> <tr> <td>H/W Reset</td> <td>DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1	SW Reset	VCOMG=0, PON=0, DK=1, STB=1, othes no change	H/W Reset	DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1				
	Status	Default Value												
	Power On Sequence	DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1												
SW Reset	VCOMG=0, PON=0, DK=1, STB=1, othes no change													
H/W Reset	DP_STB=0, DP_STB_S=0, BT[2:0]=100, VRH[5:0]=6'h1B, NVRH[5:0]=6'h1B, AP[2:0]=011, FS0[7:0]=8'h40, FS1[7:0]=8'h08, GASEN=1, VCOMG=0, PON=0, DK=1, XDK=0, TRI=0, STB=1													
Flow Chart	-													

Himax Confidential
Do Not Copy

8.2.39 SETDISPLAY: set display related register (B2h)

B2H	SETDISPLAY(Set Display Control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	0	B2
1 st parameter	1	↑	1	-	-	-	-	-	ISC[3:0]			-	01
2 nd parameter	1	↑	1	-	PT[1:0]		-	-	-	-	PTG	REF	83
3 rd parameter	1	↑	1	-	-	-	GON	DTE	D[1:0]		-	-	20

This command is used to set display related register

D[1:0]: When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level.
 When D[1:0]= '01', the internal display of the HX8353-E is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
0	x	Fixed to VGH
1	0	Fixed to VGL
1	1	Normal Operation (VGH/VGL)

PT[1:0] : Specify the Non-display area source output in partial display mode.

Description

REV_Panel	GRAM Data	Source Output Level						GND	Hi-z
		Display area		Non-display Area					
		Positive	Negative	PT1-0=(0,*)		PT1-0=(1,0)	PT1-0=(1,1)		
1 (Normally Black Panel)	18'h00000 18'h3FFFF	V63P V0P	V0N V63N	V63P	V0N			GND	Hi-z
0 (Normally White Panel)	18'h00000 18'h3FFFF	V0P V63P	V63N V0N	V63P	V0N				

REF: Refresh display in non-display area in Partial mode enable bit.
 REF = '0': Refresh display operation is disabling.
 REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

	<p>ISC[3:0]: Specify the scan cycle of gate driver when REF = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1. The polarity is inverted every scan cycle.</p> <table border="1"> <thead> <tr> <th>ISC3</th> <th>ISC2</th> <th>ISC1</th> <th>ISC0</th> <th>Scan Cycle</th> <th>f_{FLM} = 60Hz</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1 frame</td><td>17ms</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>5 frames</td><td>83ms</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>9 frames</td><td>150ms</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>13 frames</td><td>217ms</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>17 frames</td><td>283ms</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>21 frames</td><td>350ms</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>25 frames</td><td>417ms</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>29 frames</td><td>483ms</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>33 frames</td><td>550ms</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>37 frames</td><td>616ms</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>41 frames</td><td>683ms</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>45 frames</td><td>750ms</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>49 frames</td><td>816ms</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>53 frames</td><td>883ms</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>57 frames</td><td>950ms</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td colspan="2">Setting inhibited</td></tr> </tbody> </table>	ISC3	ISC2	ISC1	ISC0	Scan Cycle	f _{FLM} = 60Hz	0	0	0	0	1 frame	17ms	0	0	0	1	5 frames	83ms	0	0	1	0	9 frames	150ms	0	0	1	1	13 frames	217ms	0	1	0	0	17 frames	283ms	0	1	0	1	21 frames	350ms	0	1	1	0	25 frames	417ms	0	1	1	1	29 frames	483ms	1	0	0	0	33 frames	550ms	1	0	0	1	37 frames	616ms	1	0	1	0	41 frames	683ms	1	0	1	1	45 frames	750ms	1	1	0	0	49 frames	816ms	1	1	0	1	53 frames	883ms	1	1	1	0	57 frames	950ms	1	1	1	1	Setting inhibited	
ISC3	ISC2	ISC1	ISC0	Scan Cycle	f _{FLM} = 60Hz																																																																																																		
0	0	0	0	1 frame	17ms																																																																																																		
0	0	0	1	5 frames	83ms																																																																																																		
0	0	1	0	9 frames	150ms																																																																																																		
0	0	1	1	13 frames	217ms																																																																																																		
0	1	0	0	17 frames	283ms																																																																																																		
0	1	0	1	21 frames	350ms																																																																																																		
0	1	1	0	25 frames	417ms																																																																																																		
0	1	1	1	29 frames	483ms																																																																																																		
1	0	0	0	33 frames	550ms																																																																																																		
1	0	0	1	37 frames	616ms																																																																																																		
1	0	1	0	41 frames	683ms																																																																																																		
1	0	1	1	45 frames	750ms																																																																																																		
1	1	0	0	49 frames	816ms																																																																																																		
1	1	0	1	53 frames	883ms																																																																																																		
1	1	1	0	57 frames	950ms																																																																																																		
1	1	1	1	Setting inhibited																																																																																																			
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command																																																																																																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																																																																																										
Status	Availability																																																																																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																																																																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																																																																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																																																																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																																																																																																						
Sleep In or Booster Off	Yes																																																																																																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.</td> </tr> <tr> <td>S/W Reset</td> <td>D[1:0]=2'b00, GON=1, DTE=0, others no change</td> </tr> <tr> <td>H/W Reset</td> <td>D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.	S/W Reset	D[1:0]=2'b00, GON=1, DTE=0, others no change	H/W Reset	D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.																																																																																														
Status	Default Value																																																																																																						
Power On Sequence	D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.																																																																																																						
S/W Reset	D[1:0]=2'b00, GON=1, DTE=0, others no change																																																																																																						
H/W Reset	D[1:0]=2'b00, GON=1, DTE=0, PT[1:0]=2'b10, REF=1, PTG=1, ISC[3:0]=4'b0001, NL[5:0]=6'h27, SCN[6:0]=7'h00.																																																																																																						
Flow Chart	-																																																																																																						

8.2.40 SETCYC: set display cycle register (B4h)

B4 H	SETCYC (Set display cycle)																																																															
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																			
Command	0	↑	1	-	1	0	1	1	0	1	0	0	B4																																																			
1 st parameter	1	↑	1	-	-	-	I/_NW[1:0]	-	-	-	N_NW[1:0]	-	11																																																			
2 nd parameter	1	↑	1	-	-	-	-	-	-	N_RTN[3:0]			08																																																			
3 rd parameter	1	↑	1	-	-	-	-	-	-	-	N_DIV[3:0]		00																																																			
4 th parameter	1	↑	1	-	-	-	-	-	N_DUM[7:0]			0C																																																				
5 th parameter	1	↑	1	-	-	-	-	I_DUM[7:0]			0C																																																					
6 th parameter	1	↑	1	-	-	-	-	GDON[7:0]			0D																																																					
7 th parameter	1	↑	1	-	-	-	-	GDOF[7:0]			53																																																					
8 th parameter	1	↑	1	-	-	-	-	L_BASE[7:0]			59																																																					
Description	<p>N_NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.</p> <p>I_NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>NW[1:0]</th> <th>LCD driving Inversion Type</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Column inversion</td> </tr> <tr> <td>01</td> <td>1-dot inversion</td> </tr> <tr> <td>10</td> <td>2-dot inversion</td> </tr> <tr> <td>11</td> <td>4-dot inversion</td> </tr> </tbody> </table> <p>N_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation. Clock cycles=1/internal operation clock frequency(fosc)</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>RTN[3:0]</th> <th>Clock number per Line</th> </tr> </thead> <tbody> <tr><td>4'b0000</td><td>89</td></tr> <tr><td>4'b0001</td><td>90</td></tr> <tr><td>4'b0010</td><td>91</td></tr> <tr><td>4'b0011</td><td>92</td></tr> <tr><td>4'b0100</td><td>93</td></tr> <tr><td>4'b0101</td><td>94</td></tr> <tr><td>4'b0110</td><td>95</td></tr> <tr><td>4'b0111</td><td>96</td></tr> <tr><td>4'b1000</td><td>97</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>4'b1110</td><td>103</td></tr> <tr><td>4'b1111</td><td>104</td></tr> </tbody> </table> <p>N_DIV[3:0]: Specify the division ratio of internal clocks IN Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the N_RTN[3:0] bits (1H period clock cycle), N_DIV[3:0], and N_DUM[7:0] bits.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIV1</th> <th>DIV0</th> <th>Internal Display Operation Clock Frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>fosc / 6</td> </tr> <tr> <td>0</td> <td>1</td> <td>fosc / 12</td> </tr> <tr> <td>1</td> <td>0</td> <td>fosc / 24</td> </tr> <tr> <td>1</td> <td>1</td> <td>fosc / 48</td> </tr> </tbody> </table> <p>Note : fosc = R-C oscillation frequency</p>													NW[1:0]	LCD driving Inversion Type	00	Column inversion	01	1-dot inversion	10	2-dot inversion	11	4-dot inversion	RTN[3:0]	Clock number per Line	4'b0000	89	4'b0001	90	4'b0010	91	4'b0011	92	4'b0100	93	4'b0101	94	4'b0110	95	4'b0111	96	4'b1000	97	:	:	4'b1110	103	4'b1111	104	DIV1	DIV0	Internal Display Operation Clock Frequency	0	0	fosc / 6	0	1	fosc / 12	1	0	fosc / 24	1	1	fosc / 48
	NW[1:0]	LCD driving Inversion Type																																																														
	00	Column inversion																																																														
	01	1-dot inversion																																																														
	10	2-dot inversion																																																														
	11	4-dot inversion																																																														
	RTN[3:0]	Clock number per Line																																																														
	4'b0000	89																																																														
	4'b0001	90																																																														
	4'b0010	91																																																														
4'b0011	92																																																															
4'b0100	93																																																															
4'b0101	94																																																															
4'b0110	95																																																															
4'b0111	96																																																															
4'b1000	97																																																															
:	:																																																															
4'b1110	103																																																															
4'b1111	104																																																															
DIV1	DIV0	Internal Display Operation Clock Frequency																																																														
0	0	fosc / 6																																																														
0	1	fosc / 12																																																														
1	0	fosc / 24																																																														
1	1	fosc / 48																																																														

N_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
I_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4
:	:
190d	190
others	Setting Inhibited

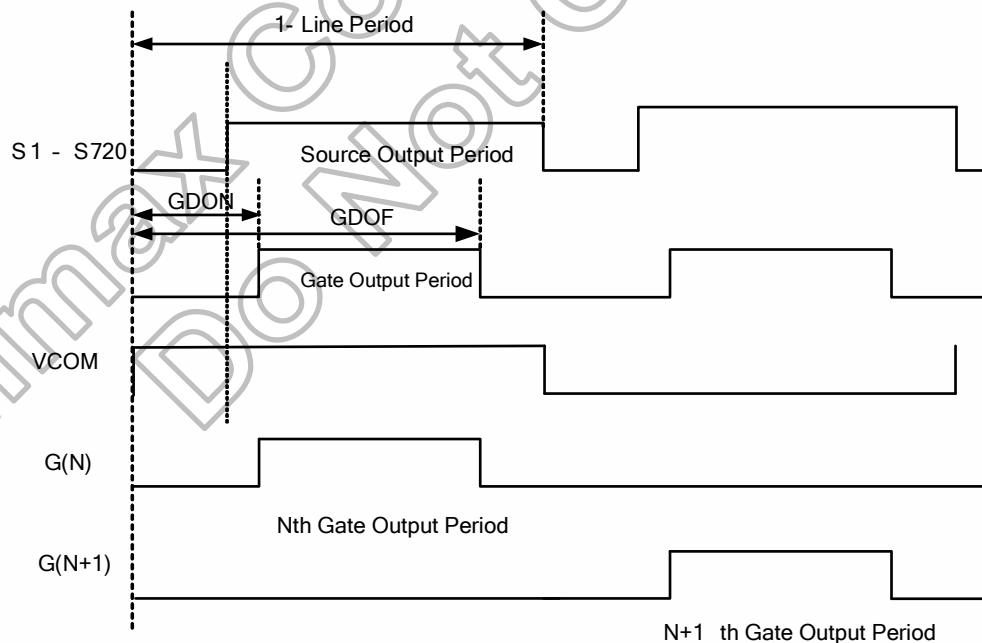
Formula for the Frame Frequency during internal display mode:

$$\text{Frame frequency} = \text{fosc} / (\text{RTN} \times \text{DIV} \times (162 + \text{DUM})) \text{ [Hz]}$$

Fosc : RC oscillation frequency

GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting "00h", "01h", "02h" is inhibited).

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the $\text{GDON}[7:0] + 1 \leq \text{GDOF}[7:0] \leq \text{RTN} - 1$).



L_BASE[7:0]: Basic line clock number. Internal line clock = L_BASE[7:0] + RTN[3:0].

Restrictions If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

	Status	Default Value
	Default	Power On Sequence
	S/W Reset	No change
	HW Reset	I_NW[2:0]=3'b001, N_NW[2:0]=3'b001, I_RTN[3:0]=4'b0000, N_RTN[3:0]=4'b0000, N_DUM[7:0]=8'b00001100, I_DUM[7:0]=8'b00001100, GDON[7:0]=8'b00001101, GDOF[7:0]=8'b01110000,
Flow Chart	-	

Himax Confidential
Do Not Copy

8.2.41 SETBGP: set internal reference voltage register (B5h)

B5 H	SETBGP (Set Reference Voltage)												HEX																																																																											
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0																																																																												
Command	0	↑	1	-	1	0	1	1	0	1	0	1	B5																																																																											
1 st parameter	1	↑	1	-	NVREF[3:0]				VREF[3:0]				77																																																																											
2 nd parameter	1	↑	1	-	FBOFF	VNVDHS_SEL[2:0]			VVDHS_SEL[2:0]				33																																																																											
Description	This command is used to set internal reference Voltage.																																																																																							
	<p>VREF[3:0]: Positive reference voltage setting. NVREF[3:0]: Negative reference voltage setting.</p> <table border="1"> <thead> <tr> <th>VREF[3:0]/NVREF[3:0]</th> <th>VREF voltage</th> <th>NVREF voltage</th> </tr> </thead> <tbody> <tr><td>4'b0000</td><td>4.1V</td><td>-4.1V</td></tr> <tr><td>4'b0001</td><td>4.2V</td><td>-4.2V</td></tr> <tr><td>4'b0010</td><td>4.3V</td><td>-4.3V</td></tr> <tr><td>4'b0011</td><td>4.4V</td><td>-4.4V</td></tr> <tr><td>4'b0100</td><td>4.45V</td><td>-4.45V</td></tr> <tr><td>4'b0101</td><td>4.5V</td><td>-4.5V</td></tr> <tr><td>4'b0110</td><td>4.55V</td><td>-4.55V</td></tr> <tr><td>4'b0111</td><td>4.6V</td><td>-4.6V</td></tr> <tr><td>4'b1000</td><td>4.65V</td><td>-4.65V</td></tr> <tr><td>4'b1001</td><td>4.7V</td><td>-4.7V</td></tr> <tr><td>4'b1010</td><td>4.75V</td><td>-4.75V</td></tr> <tr><td>4'b1011</td><td>4.8V</td><td>-4.8V</td></tr> <tr><td>4'b1100</td><td>4.85V</td><td>-4.85V</td></tr> <tr><td>4'b1101</td><td>4.9V</td><td>-4.9V</td></tr> <tr><td>4'b1110</td><td>4.95V</td><td>-4.95V</td></tr> <tr><td>4'b1111</td><td>5V</td><td>-5V</td></tr> </tbody> </table> <p>Note: Ensure that $VSP - 0.1 \geq VREF$ and $VSN + 0.1 \leq NVREF$.</p> <p>VVDHS_SEL[2:0]: VSP voltage setting VNVDHS_SEL[2:0]: VSN voltage setting</p> <table border="1"> <thead> <tr> <th>VVDHS_SEL [2:0]/VNVDHS [2:0]</th> <th>VSP voltage</th> <th>VSN voltage</th> </tr> </thead> <tbody> <tr><td>4'b000</td><td>4.463V</td><td>-4.39V</td></tr> <tr><td>4'b001</td><td>4.539V</td><td>-4.479V</td></tr> <tr><td>4'b010</td><td>4.617V</td><td>-4.57V</td></tr> <tr><td>4'b011</td><td>4.699V</td><td>-4.659V</td></tr> <tr><td>4'b100</td><td>4.782V</td><td>-4.747V</td></tr> <tr><td>4'b101</td><td>4.867V</td><td>-4.825V</td></tr> <tr><td>4'b110</td><td>4.954V</td><td>-4.866V</td></tr> </tbody> </table>													VREF[3:0]/NVREF[3:0]	VREF voltage	NVREF voltage	4'b0000	4.1V	-4.1V	4'b0001	4.2V	-4.2V	4'b0010	4.3V	-4.3V	4'b0011	4.4V	-4.4V	4'b0100	4.45V	-4.45V	4'b0101	4.5V	-4.5V	4'b0110	4.55V	-4.55V	4'b0111	4.6V	-4.6V	4'b1000	4.65V	-4.65V	4'b1001	4.7V	-4.7V	4'b1010	4.75V	-4.75V	4'b1011	4.8V	-4.8V	4'b1100	4.85V	-4.85V	4'b1101	4.9V	-4.9V	4'b1110	4.95V	-4.95V	4'b1111	5V	-5V	VVDHS_SEL [2:0]/VNVDHS [2:0]	VSP voltage	VSN voltage	4'b000	4.463V	-4.39V	4'b001	4.539V	-4.479V	4'b010	4.617V	-4.57V	4'b011	4.699V	-4.659V	4'b100	4.782V	-4.747V	4'b101	4.867V	-4.825V	4'b110	4.954V	-4.866V
	VREF[3:0]/NVREF[3:0]	VREF voltage	NVREF voltage																																																																																					
	4'b0000	4.1V	-4.1V																																																																																					
	4'b0001	4.2V	-4.2V																																																																																					
	4'b0010	4.3V	-4.3V																																																																																					
	4'b0011	4.4V	-4.4V																																																																																					
	4'b0100	4.45V	-4.45V																																																																																					
	4'b0101	4.5V	-4.5V																																																																																					
	4'b0110	4.55V	-4.55V																																																																																					
	4'b0111	4.6V	-4.6V																																																																																					
	4'b1000	4.65V	-4.65V																																																																																					
	4'b1001	4.7V	-4.7V																																																																																					
	4'b1010	4.75V	-4.75V																																																																																					
	4'b1011	4.8V	-4.8V																																																																																					
	4'b1100	4.85V	-4.85V																																																																																					
	4'b1101	4.9V	-4.9V																																																																																					
	4'b1110	4.95V	-4.95V																																																																																					
	4'b1111	5V	-5V																																																																																					
	VVDHS_SEL [2:0]/VNVDHS [2:0]	VSP voltage	VSN voltage																																																																																					
4'b000	4.463V	-4.39V																																																																																						
4'b001	4.539V	-4.479V																																																																																						
4'b010	4.617V	-4.57V																																																																																						
4'b011	4.699V	-4.659V																																																																																						
4'b100	4.782V	-4.747V																																																																																						
4'b101	4.867V	-4.825V																																																																																						
4'b110	4.954V	-4.866V																																																																																						

	4'b111	5.019V	-4.867V
	FBOFF: Internal used, not open.		
Restrictions	Must enable SETEXTC command		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In or Booster Off		Yes
Default	Status		Default Value
	Power On Sequence		NVREF[3:0]=0111, VREF[3:0]=0111, VNVDHS_SEL[2:0]=011, VVDHS_SEL[2:0]=011, FBOFF=0
	S/W Reset		No change
	H/W Reset		NVREF[3:0]=0111, VREF[3:0]=0111, VNVDHS_SEL[2:0]=011, VVDHS_SEL[2:0]=011, FBOFF=0
Flow Chart	-		

Himax Confidential
Do Not Copy

8.2.42 SETCOM: set VCOM voltage related register (B6h)

B6 H	SETCOM (Set VCOM Voltage)												HEX
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	↑	1	-	1	0	1	1	0	1	1	0	B6
1 st parameter	1	↑	1	-	-	VCOM[6:0]						4B	
2 nd parameter	1	↑	1	-	-	-	-	-	-	VCM_TIMES[2:0]		00	
Description	This command is used to set VCOM Voltage.												
	VCOM[6:0]: DC VCOM voltage setting.												
	VCOM[6:0]							VCOM Voltage					
	0	0	0	0	0	0	0	0	0	0	0	0	-2.500
	0	0	0	0	0	0	0	0	1	0	0	0	-2.480
	0	0	0	0	0	0	0	1	0	0	0	0	-2.460
	0	0	0	0	0	0	0	1	1	0	0	0	-2.440
	0	0	0	0	0	1	0	0	0	0	0	0	-2.420
	:							:					
	:							:					
	1	1	1	1	1	0	1	0	0	0	0	0	-0.060
	1	1	1	1	1	0	1	1	0	0	0	0	-0.040
	1	1	1	1	1	1	0	0	0	0	0	0	-0.020
	1	1	1	1	1	1	0	1	0	0	0	0	VSSA
	1	1	1	1	1	1	1	0	0	0	0	0	VSSA
1	1	1	1	1	1	1	1	0	0	0	0	VSSA	
VCM_OTP_TIMES[2:0]: Read VCOM OTP programmed times.													
VCM_TIMES[2:0]				VCOM OTP programmed times									
3'b000				Not programmed									
3b001				1 time									
3'b010				2 times									
3'b011				3 times									
3'b100				4 times									
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						VCOM[6:0]=8'h4B, VCOM_OTP_TIMES[2:0]=3'b000						
	S/W Reset						No change						
	H/W Reset						OTP value						
Flow Chart	-												

8.2.43 SETEXTC: enable extension command (B9h)

B9 H	SETEXTC (Set Extended Command Set)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	1	0	0	1	B9
1 st parameter	1	↑	1	-	EXTC1[7:0]							00	
2 nd parameter	1	↑	1	-	EXTC2[7:0]							00	
3 rd parameter	1	↑	1	-	EXTC3[7:0]							00	
Description	This command is used to set extended command set access enable.												
	Extend cmd				Command description								
	Enable				After command (B9h), must write 3 parameters (FFh,83h,53h) by order								
	Disable(default)				After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh,83h,53h)								
Restrictions	-												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status				Default Value								
	Power On Sequence				EXTC1[7:0]=8'h00, EXTC2[7:0]=8'h00, EXTC3[7:0]=8'h00								
	S/W Reset				No change								
	H/W Reset				EXTC1[7:0]=8'h00, EXTC2[7:0]=8'h00, EXTC3[7:0]=8'h00								
Flow Chart	-												

8.2.44 SETOTP: set OTP setting (BBh)

BB H	SETOTP (Set OTP related setting)													HEX											
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	↑	1	-	1	0	1	1	1	0	1	1	BB												
1 st parameter	1	↑	1	-	OTP_KEY[7:0]							00													
2 nd parameter	1	↑	1	-	OTP_MASK[7:0]							00													
3 rd parameter	1	↑	1	-	OTP_INDEX[7:0]							00													
4 th parameter	1	↑	1	-	LOA D_DI SABL E	VPP_ EN	OTP_ POR	OTP_ PWE	OTP_PTM[1:0]		VPP_ SEL	OTP_ PRO G	00												
5 th parameter	1	1	↑	-	OTPDOUT[7:0]							FF													
Description	<p>This command is used to set the OTP related setting.</p> <p>OTP_KEY[7:0]: "AAh" OTP register access enable and other registers access disable. "55h" OTP register access disable and other registers access enable.</p> <p>OTP_MASK[7:0]: Bit programming mask. If "1", means don't programming this bit.</p> <p>OTP_INDEX[7:0]: Set index of OTP to be programmed.</p> <p>LOAD_DIS: When written to "1", OTP load disable.</p> <p>VPP_EN: When written to "1", OTP power OP is enable.</p> <p>OTP_POR: for OTP read control. When set to from "0" to "1", OTP data can be read the related OTP index at OTP_DOUT[7:0].</p> <p>OTP_PROG : When this bit set to "1", it will programmed to the setting OTP index from related register value.</p> <p>OTP_PWE : Internal use, not open.</p> <p>OTP_PTM[1:0] : Internal use, not open.</p> <p>VPP_SEL : When set to '1', VPP input voltage is fed to OTP.</p> <p>OTP_DOUT[7:0] : OTP read data.</p>																								
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00</td> </tr> <tr> <td>S/W Reset</td> <td>OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00</td> </tr> <tr> <td>H/W Reset</td> <td>OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00	S/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00	H/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00				
Status	Default Value																								
Power On Sequence	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00																								
S/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00																								
H/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00																								
Flow Chart	-																								

8.2.45 SETSTBA: set Source option related register (C0h)

C0 H	SETSTBA (Set Source Option)												HEX
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	↑	1	-	1	1	0	0	0	0	0	0	C0
1 st parameter	1	↑	1	-	N_OPON[7:0]							20	
2 nd parameter	1	↑	1	-	I_OPON[7:0]							10	
3 rd parameter	1	↑	1	-	STBA[15:8]							0C	
4 th parameter	1	↑	1	-	STBA[7:0]							C7	
5 th parameter	1	↑	1	-	GENON[7:0]							10	
6 th parameter	1	↑	1	-	-	-	-	-	-	-	-	OTPS1B	00

This command is used to set source related setting.

N_OPON[7:0]: Source OP on period control on Normal/Partial mode setting. The period time is defined as SYSCLK number in internal clock display mode.

I_OPON[7:0]: Source OP on period control on Idle/Idle Partial mode setting. The period time is defined as SYSCLK number in internal clock display mode.

Clock cycle=1/internal operation clock frequency(fosc)

N_OPON[7:0] / I_OPON[7:0]	Source OP on Period
8'h00	Setting Inhabited
8'h01	1 clock cycle
8'h02	2 clock cycle
:	:
8'hFF	255 clock cycle

STBA[14:6]: Source Bias current setting. The driving ability= Driving Level1 x Driving Level2.

STBA[4:2] , STBA[1:0]: Gamma Bias current setting. The driving ability= Driving Level1 x Driving Level2.

STBA15, STBA5: Not used.

Description

STBA14	STBA13	STBA12	STBA11	STBA10	Source Driving Level1
0	0	0	1	1	1x
0	0	0	0	0	2x
0	0	0	1	0	3x
0	0	1	0	0	4x
0	0	1	1	0	5x
0	1	1	0	0	6x
0	1	1	1	0	7x
1	1	1	0	0	8x
1	1	1	1	0	9x

STBA9	STBA8	STBA7	STBA6	Source Driving Level2
0	0	1	1	Small
0	0	1	0	Middle Small
0	0	0	0	Middle
0	1	0	0	Middle Large
1	1	0	0	Large

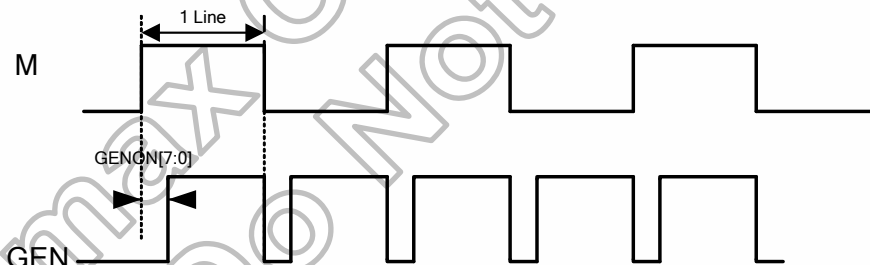
STBA4	STBA3	STBA2	Gamma Driving Level1
0	0	1	1x
0	0	0	2x
0	1	1	3x
0	1	0	4x
1	0	1	5x
1	0	0	6x
1	1	1	7x
1	1	0	8x

STBA1	STBA0	Gamma Driving Level2
0	0	Small
0	1	Middle Small
1	0	Middle
1	1	Large

GENON[7:0]: Gamma OP on period control. The period time is defined as SYSCLK number in internal clock display mode.

Clock cycle=1/internal operation clock frequency(fosc)

GENON[7:0]	Gamma OP on Period
8'h00	0 clock cycle
8'h01	1 clock cycle
8'h02	2 clock cycle
:	:
8'hFF	255 clock cycle



OTPS1B: Internal used, not open.

Restrictions	Must enable SETEXTC command													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In or Booster Off	Yes													

Default	Status	Default Value
	Power On Sequence	N_OPON[7:0]=8'h20, I_OPON[7:0]=8'h10, STBA[15:8]=8'h0C, STBA[7:0]=8'hC7, GENON[7:0]=8'h10
	S/W Reset	No change
	H/W Reset	N_OPON[7:0]=8'h20, I_OPON[7:0]=8'h10, STBA[15:8]=8'h0C, STBA[7:0]=8'hC7, GENON[7:0]=8'h10
Flow Chart	-	

Himax Confidential
Do Not Copy

8.2.46 SETTID: set ID (C3h)

C3 H	SETID (Set ID)												HEX
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	↑	1	-	1	1	0	0	0	0	1	1	C3
1 st parameter	1	↑	1	-	ID1[7:0]							00	
2 nd parameter	1	↑	1	-	ID2[7:0]							00	
3 rd parameter	1	↑	1	-	ID3[7:0]							00	
4 th parameter					-	-	-	-	-	ID_TIMES[2:0]		00	
Description	This command is used to set ID.												
	ID_OTP_TIMES[2:0]: Read ID OTP programmed times.												
	ID_TIMES[2:0]		ID OTP programmed times										
	3'b000		Not programmed										
	3'b001		1 time										
	3'b010		2 times										
3'b011		3 times											
3'b100		4 times											
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						OTP value						
	S/W Reset						No Change						
	H/W Reset						OTP value						
Flow Chart	-												

8.2.47 SETPANEL: set panel characteristic (CCh)

CCH	SETPANEL(Set Panel Characteristic Register)												HEX												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	↑	1	-	1	1	0	0	1	1	0	0	CC												
1 st parameter	1	↑	1	-	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00												
Description	<p>This command is used to set Panel characteristic related register</p> <p>REV_PANEL: The source output data polarity selected. '0': normally white panel. '1': normally black panel.</p> <p>BGR_PANEL: The color filter order direction selected. '0': S1:S2:S3='R':'G':'B' '1': S1:S2:S3='B':'G':'R'</p> <p>GS_PANEL: The gate driver output shift direction selected. '0': G1→G320 '1': G320→G1</p> <p>SS_PANEL: The source driver output shift direction selected. '0': S720→S1 '1': S1→S720</p>																								
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0	S/W Reset	No change	H/W Reset	SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0				
Status	Default Value																								
Power On Sequence	SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0																								
S/W Reset	No change																								
H/W Reset	SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0																								
Flow Chart	-																								

8.2.48 GETHID: Read Himax Internal ID (D0h)

D0H	GETHID (Read Himax Internal ID)													HEX
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	↑	1	-	0	1	0	1	0	0	1	1	D0	
1 st parameter	1	↑	1	-	ID_VERSION[7:0] (0101_0011)							53		
Description	This command is used to Read Himax Internal ID													
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command													
Register Availability	Status						Availability							
	Normal Mode On, Idle Mode Off, Sleep Out						Yes							
	Normal Mode On, Idle Mode On, Sleep Out						Yes							
	Partial Mode On, Idle Mode Off, Sleep Out						Yes							
	Partial Mode On, Idle Mode On, Sleep Out						Yes							
	Sleep In or Booster Off						Yes							
Default	Status						Default Value							
	Power On Sequence						ID_VERSION[7:0]=53h							
	S/W Reset						ID_VERSION[7:0]=53h							
	H/W Reset						ID_VERSION[7:0]=53h							
Flow Chart	-													

Himax Confidential
Do Not Copy

8.2.49 SETGAMMA: set gamma curve (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)																								
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	1	1	1	0	0	0	0	0	E0												
1 st parameter	1	↑	1	-	-	MP1[2:0]		-	MP0[2:0]				00												
2 nd parameter	1	↑	1	-	-	MP3[2:0]		-	MP2[2:0]				60												
3 rd parameter	1	↑	1	-	-	MP5[2:0]		-	MP4[2:0]				30												
4 th parameter	1	↑	1	-	-	-	-	-	CP0[3:0]				06												
5 th parameter	1	↑	1	-	CP2[3:0]			CP1[3:0]					8C												
6 th parameter	1	↑	1	-	-	-	-	-	CP3[3:0]				02												
7 th parameter	1	↑	1	-	-	-	-	-	CP4[3:0]				04												
8 th parameter	1	↑	1	-	-	-	-	-	OP0[3:0]				0F												
9 th parameter	1	↑	1	-	-	-	-	OP1[4:0]				06													
10 th parameter	1	↑	1	-	-	-	-	-	CGM1[1:0]	CGM0[1:0]		0E													
11 th parameter	1	↑	1	-	-	MN1[2:0]		-	MN0[2:0]				74												
12 th parameter	1	↑	1	-	-	MN3[2:0]		-	MN2[2:0]				71												
13 th parameter	1	↑	1	-	-	MN5[2:0]		-	MN4[2:0]				77												
14 th parameter	1	↑	1	-	-	-	-	-	CN0[3:0]				04												
15 th parameter	1	↑	1	-	CN2[3:0]			CN1[3:0]					82												
16 th parameter	1	↑	1	-	-	-	-	-	CN3[3:0]				0C												
17 th parameter	1	↑	1	-	-	-	-	-	CN4[3:0]				06												
18 th parameter	1	↑	1	-	-	-	-	-	ON0[3:0]				03												
19 th parameter	1	↑	1	-	-	-	-	-	ON1[4:0]				1E												
Description	This command is used for Gamma Curve related Setting. For details, please refer to Section 7.2.																								
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>GC0 value</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>GC0 value</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	GC0 value	S/W Reset	No change	H/W Reset	GC0 value				
Status	Default Value																								
Power On Sequence	GC0 value																								
S/W Reset	No change																								
H/W Reset	GC0 value																								
Flow Chart	-																								

8.2.50 SET SPI READ: Set SPI read address (FEh)

FEH	SET SPI READ (Set SPI read address)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	1	1	1	1	0	FE
1 st parameter	1	↑	1	-	A7	A6	A5	A4	A3	A2	A1	A0	-
Description	This command is used to set SPI-4W read address												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						No change						
	S/W Reset						No change						
	H/W Reset						No change						
Flow Chart	-												

Himax Confidential
Do Not Copy

8.2.51 GET SPI READ: Get SPI read address (FFh)

FFH	GET SPI READ (Get SPI read address)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	1	1	1	1	1	FF
1 st parameter	1	↑	1	-									-
2 nd parameter	1	↑	1	-									-
3 rd parameter	1	↑	1	-									-
4 th parameter	1	↑	1	-									-
5 th parameter	1	↑	1	-									-
Description	This command is used to get the SPI-4W read address index's parameters												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						No change						
	S/W Reset						No change						
	H/W Reset						No change						
Flow Chart	-												

9. Layout Recommendation

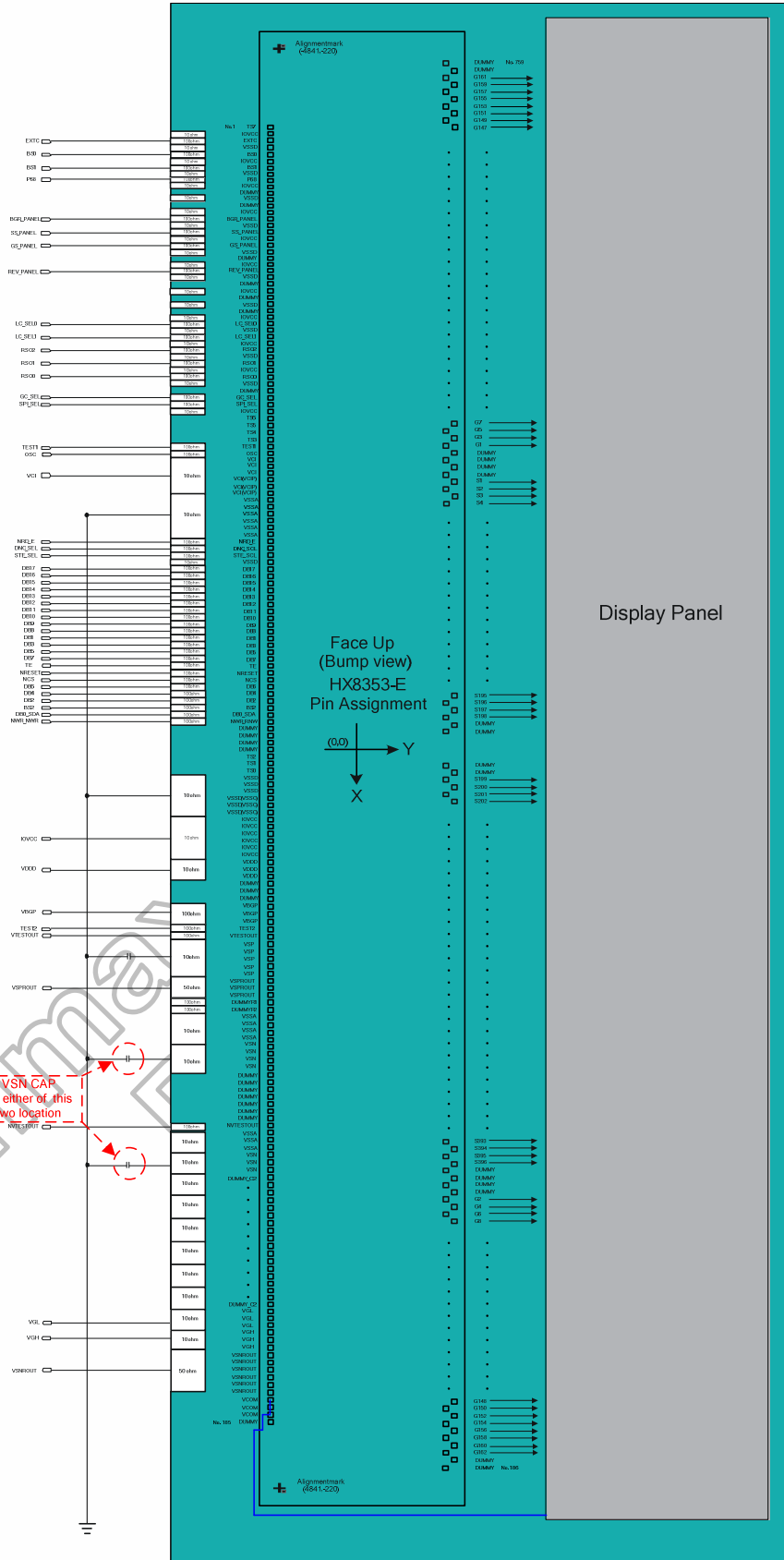


Figure 9.1 Layout recommendation of HX8353-E

Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
IM[3:0], IFSEL	Input	100	Ω
NRD, NWR_SCL, DNC_SCL, NCS, SDA	Input	100	Ω
NRESET	Input	100	Ω
TE, CABP_PWM_OUT, BC_CTRL	Output	100	Ω
DB[17:0],	I/O	100	Ω
DOTCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
VSN	Capacitor connection	10	Ω
VSP	Capacitor connection	10	Ω
VDDD	Output	10	Ω
VSPROUT,VSNROUT	Output	50	Ω
DUMMY_C1, DUMMY_C2	Dummy	10	Ω
TEST[2:1]	Input	100	Ω
TEST[10:3]	Output	100	Ω
VCOM, DUMMY1~24	Dummy	100	Ω
VTEST, NVTEST	Test Pin	100	Ω

Table 9.1 Maximum layout resistance

10. OTP Programming

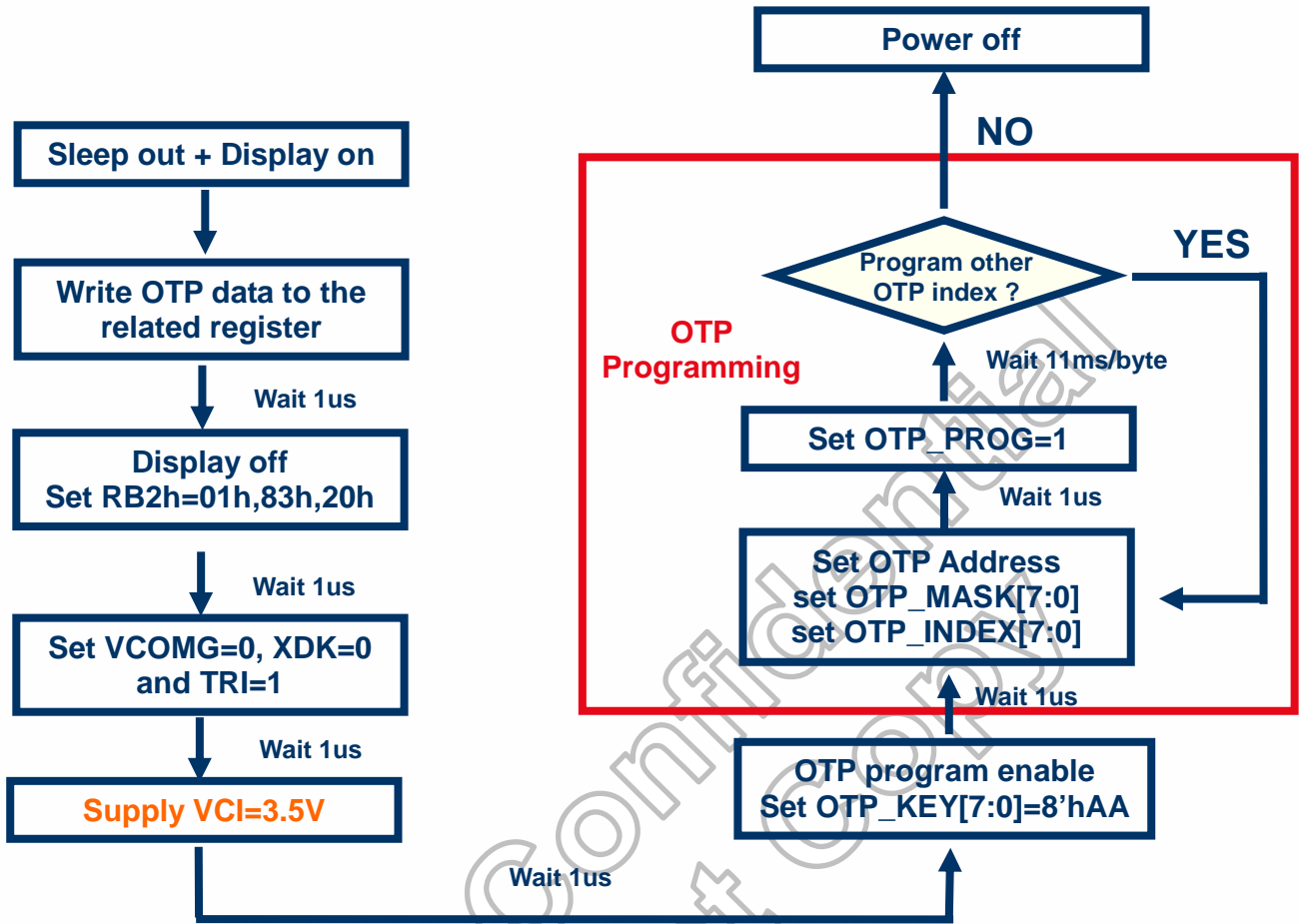
INDEX	D7	D6	D5	D4	D3	D2	D1	D0
0	ID1 [7:0]							
1	ID2 [7:0]							
2	ID3 [7:0]							
3	ID1 [7:0]							
4	ID2 [7:0]							
5	ID3 [7:0]							
6	ID1 [7:0]							
7	ID2 [7:0]							
8	ID3 [7:0]							
9	ID1 [7:0]							
A	ID2 [7:0]							
B	ID3 [7:0]							
18	*	*	*	*	nValid_ID4	nValid_ID3	nValid_ID2	nValid_ID1
19	nValid_VCMC1	VCMC[6:0]						
1A	nValid_VCMC2	VCMC[6:0]						
1B	nValid_VCMC3	VCMC[6:0]						
1C	nValid_VCMC4	VCMC[6:0]						
1D	nValid_PANEL	1'b1	1'b1	1'b1	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
20	nValid_Gamma	MP1[2:0](3'b010)			*	MP0[2:0](3'b000)		
21	*	MP3[2:0](3'b111)			*	MP2[2:0](3'b100)		
22	*	MP5[2:0](3'b000)			*	MP4[2:0](3'b000)		
23	*	*			CP0[3:0](4'b0000)			
24	CP2[3:0](4'b0111)				CP1[3:0](4'b0100)			
25	*	*	*	*	CP3[3:0](4'b0010)			
26	*	*	*	*	CP4[3:0](4'b1001)			
27	*	*	*	*	OP0[3:0](4'b1010)			
28	*			*	OP1[4:0](5'b0_0001)			
29	*	*	*	*	CGM1[1:0](2'b00)		CGM0[1:0](2'b00)	
2A	*	MN1[2:0](3'b111)			*	MN0[2:0](3'b110)		
2B	*	MN3[2:0](3'b010)			*	MN2[2:0](3'b000)		
2C	*	MN5[2:0](3'b111)			*	MN4[2:0](3'b011)		
2D	*	*			CN0[3:0](4'b1000)			
2E	CN2[3:0](4'b0110)				CN1[3:0](4'b0001)			
2F	*	*	*	*	CN3[3:0](4'b0010)			
30	*	*	*	*	CN4[3:0](4'b0000)			
31	*	*	*	*	ON0[3:0](4'b1000)			
32	*	*	*	ON1[4:0](5'b0_0010)				

Table 10.1 OTP address mapping

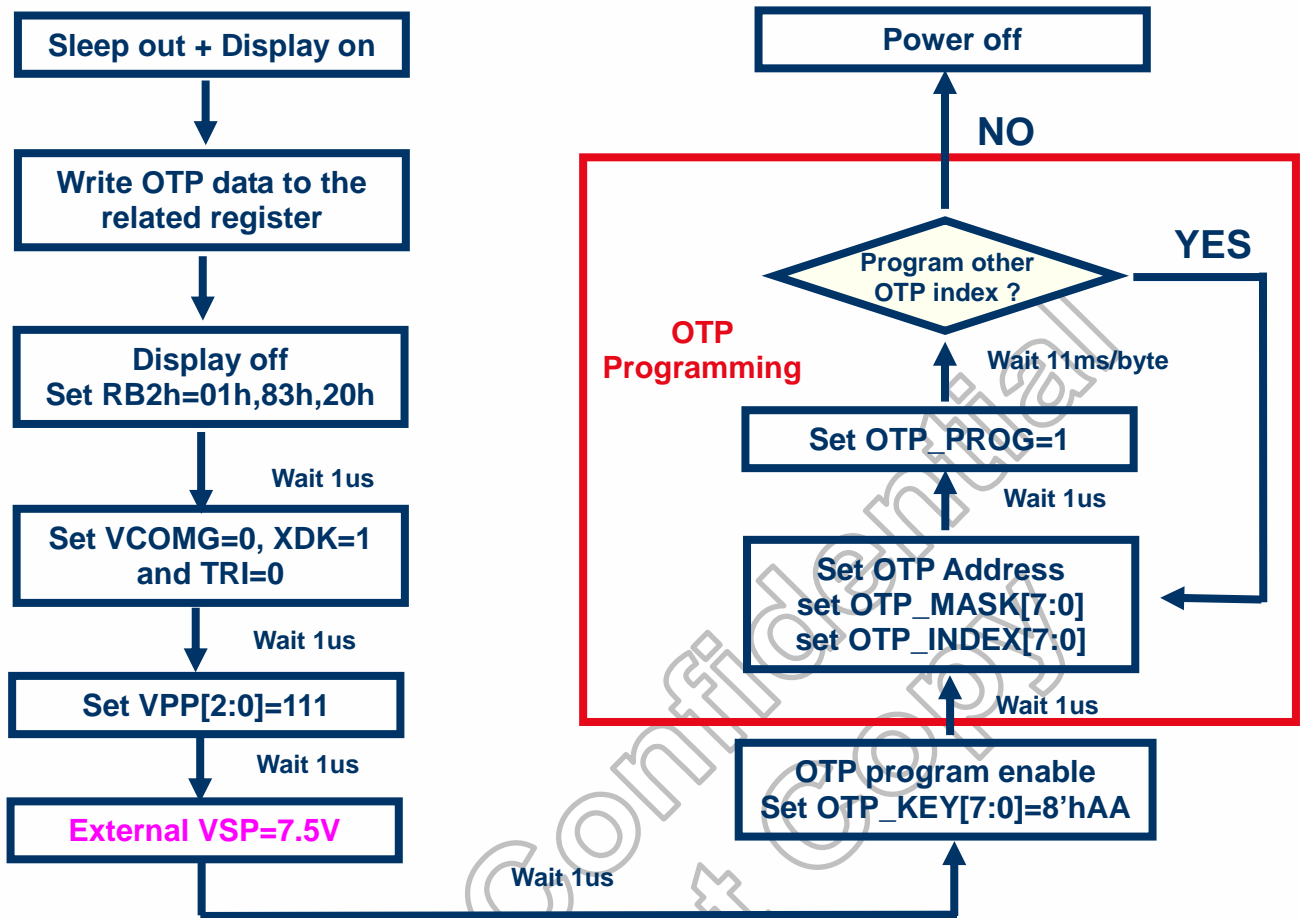
- Note:** (1) The same color means the same VALID bit controlled. When OTP Index programmed, the related VALID bit will be programmed to "0" automatically. If the VALID bit programmed to "0", the OTP value will be reload to related register after HW reset or SLPOUT command.
- (2) If want to program ID1~ID3, it just need to program Index 00h (ID2 and ID3 will be programmed automatically). If ID had be programmed, it also need to program Index 00h when second to eighth times programming (it will be programmed to corresponding Index automatically).
- (3) If want to program VCOM, it just need to program Index 19h. If VCOM had be programmed, it also need to program Index 19h when second to eighth times programming (it will be programmed to corresponding Index automatically).

Himax Confidential
Do Not Copy

10.1 Programming flow (Internal OTP power programming sequence)



10.2 Programming flow (**External** OTP power programming sequence)



11. Electrical Characteristic

11.1 Absolute maximum ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note ^{(1),(2)}
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note ⁽³⁾
Power Supply Voltage 3	VSP ~ VSSA	V	-0.3 to +6.6	Note ⁽⁴⁾
Power Supply Voltage 4	VSSA ~ VSN	V	-0.3 to +4.6	Note ⁽⁵⁾
Power Supply Voltage 5	VSP ~ VSN	V	-0.3 to +9	Note ⁽⁶⁾
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note ⁽⁷⁾
Power Supply Voltage 7	VSSA ~ VGL	V	-16.5 to 0	Note ⁽⁸⁾
Logic Input Voltage	V _{IN}	V	-0.3 to IOVCC+0.5	-
Logic Output Voltage	V _o	V	-0.3 to IOVCC+0.5	-
Operating Temperature	Topr	°C	-30 to +80	Note ^{(9),(10)}
Storage Temperature	Tstg	°C	-55 to +110	Note ^{(9),(10)}

Note: (1) IOVCC, VSSD must be maintained.

(2) To make sure IOVCC ≥ VSSD.

(3) To make sure VCI ≥ VSSA.

(4) To make sure VSP ≥ VSSA.

(5) To make sure VSSA ≥ VSN.

(6) To make sure VSP ≥ VSN.

(7) To make sure VGH ≥ VSSA.

(8) To make sure VSSA ≥ VGL

VGH + |VGL| < 32V

(9) For die and wafer products, specified up to +80°C.

(10) This temperature specifications apply to the TCP package.

Table 11.1 Absolute maximum ratings

11.2 ESD protection level

Mode	Test Condition	Protection Level	Standard
Human Body Model	C=100pF, R=1.5kΩ	±2.0KV	MIL-STD-883F Method 3015.7
Machine Model	C=200pF, R=0.0Ω	±200V	EIA/JEDEC JESD22-A115A

Table 11.2 ESD protection level

11.3 DC characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Source Drive Voltage	VSPROUT	Dual Pump	3.3	4.65	4.8	
Gate Drive High Voltage	VGH	VCI=2.8 Dual Pump (Typ:BT=001)	-	-	-	
		IVGH=80μA	TBD	TBD	TBD	
		IVGH=70μA	TBD	TBD	TBD	
		IVGH=60μA	TBD	TBD	TBD	
		IVGH=50μA	TBD	TBD	TBD	
Gate Drive Low Voltage	VGL	VCI=2.8 Dual Pump (Typ:BT=001)	-	-	-	
		IVGL=-80μA	TBD	TBD	TBD	
		IVGL=-70μA	TBD	TBD	TBD	
		IVGL=-60μA	TBD	TBD	TBD	
		IVGL=-50μA	TBD	TBD	TBD	
IVGL=-40μA	TBD	TBD	TBD			
Drive Supply Voltage	VGH-VGL	-	-	-	30	
Input / Output						
High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3*IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8*IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2*IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
Oscillator frequency	fOSC	Frame rate at 60hz, default Vs and Hs setting TA=25°C	5.7	6	6.3	MHz
Booster (VCI=2.8V)						
VSP boost voltage1	VSP	Dual Pump IVSP=1mA	4.8	5.0	5.2	V
VSN boost voltage	VSN	Dual Pump IVSN=-1mA	-5.2	-5.0	-4.8	
VCOM Generator (VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	-2.5	-	0	V
Source Driver (Typ:TA=25°C VCI=2.8V)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	+/- 10	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPROUT-1.0 ~ VSPROUT-0.1V	-	+/- 30	+/- 50	mV
Output voltage range	VOS	-	0.1	-	VSP-0.1	V
Output offset voltage	Voff	-	-	+/-30	+/-50	mV

11.3.1 Current consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						VCI (mA)	IOVCC (uA)	VCI (mA)	IOVCC (uA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	1-line	Black	X;X;X	TBD	TBD	TBD	TBD
			1-line	1x1 checker board	X;X;X	TBD	TBD	TBD	TBD
			1-line	4x4 checker board	X;X;X	TBD	TBD	TBD	TBD
			1-line	Grayscale Top to Bottom	X;X;X	TBD	TBD	TBD	TBD
			1-line	20B80W	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	60Hz	1-line	20B80W	X;X;X	TBD	TBD	TBD	TBD
		60Hz	1-line	Grey Levels	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	60Hz	1-line	8x8 checker board	X;X;X	TBD	TBD	TBD	TBD
			1-line	Worst pattern	X;X;X	TBD	TBD	TBD	TBD
	- Sleep In Mode	N/A	N/A	N/A	N/A	X;X;X	TBD	TBD	TBD
- Deep Sleep In Mode	N/A	N/A	N/A	N/A	X;X;X	TBD	TBD	TBD	TBD
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	1-line	262k Colors Worst pattern CPU Access @ 15fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
				262k Colors Worst pattern CPU Access @ 25fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
1;1;1	TBD	TBD	TBD	TBD					

Table 11.3 Current consumption

Typical Case:

TA = 25°C
 IOVCC=1.8V
 VCI = 2.8V

Worst Case:

TA = -30 to 80°C
 IOVCC = 1.65V to 1.95V
 VCI = 2.5V to 3.3V
 Includes Process Variance.

11.4 AC characteristics

11.4.1 Parallel interface characteristics (8080-series MPU)

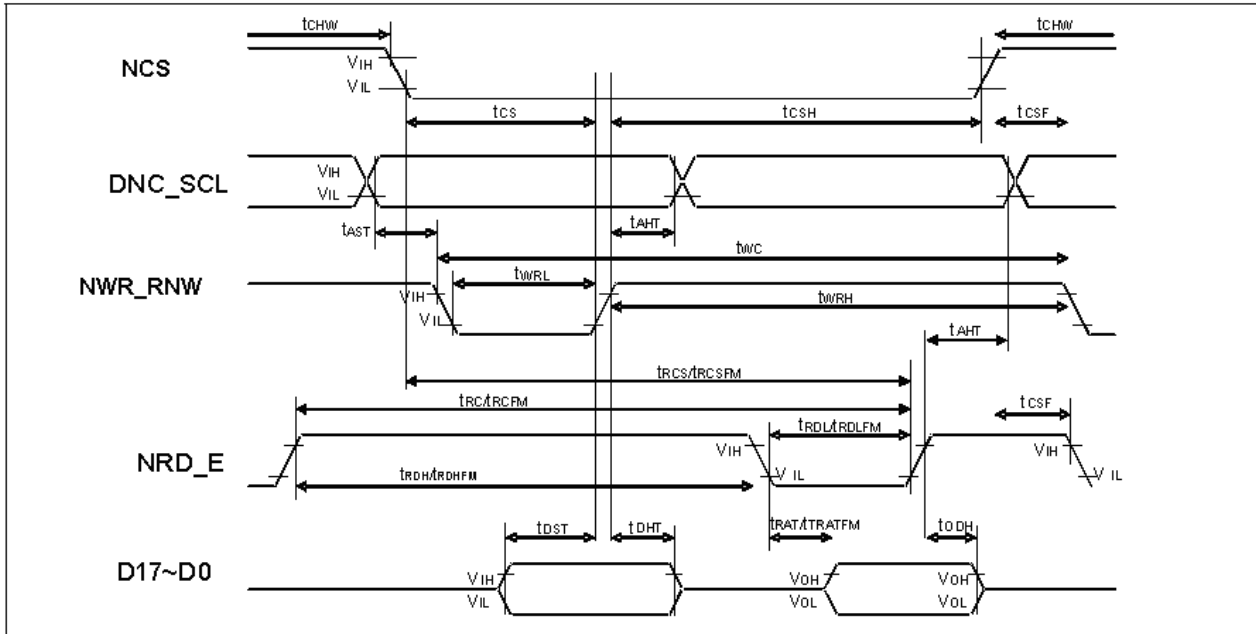


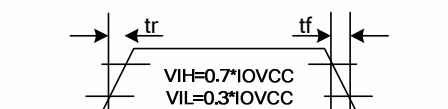
Figure 11.1 Parallel interface characteristics (8080-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, TA = -30 to 70°C)

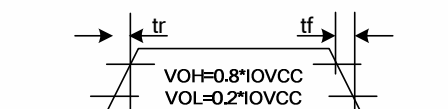
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST	Address setup time	0	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-	ns	-
NCS	tCHW	Chip select "H" pulse width	0	-	-	-
	tCS	Chip select setup time (Write)	15	-	-	-
	tRCS	Chip select setup time (Read ID)	45	-	ns	-
	tRCSFM	Chip select setup time (Read FM)	355	-	-	-
	tCSF	Chip select wait time (Write/Read)	10	-	-	-
NWR_SCL	tCSTH	Chip select hold time	10	-	-	-
	tWC	Write cycle	66	-	-	-
	tWRH	Control pulse "H" duration	15	-	ns	-
NRD_E (ID)	tWRL	Control pulse "L" duration	15	-	-	-
	tRC	Read cycle (ID)	160	-	-	-
	tRDH	Control pulse "H" duration (ID)	90	-	ns	When read ID data
NRD_E (FM)	tRDL	Control pulse "L" duration (ID)	45	-	-	-
	tRCFM	Read cycle (FM)	450	-	-	-
	tRDHFM	Control pulse "H" duration (FM)	90	-	ns	When read from frame memory
D17 to D0	tRDLFM	Control pulse "L" duration (FM)	355	-	-	-
	tDST	Data setup time	10	-	-	-
	tDHT	Data hold time	10	-	-	-
	tRAT	Read access time (ID)	-	40	ns	For maximum CL=30pF
	tRATFM	Read access time (FM)	-	340	-	For minimum CL=8pF
D17 to D0	tODH	Output disable time	20	80	-	-
	tOH	Output high time	-	-	-	-
D17 to D0	tOL	Output low time	-	-	-	-

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



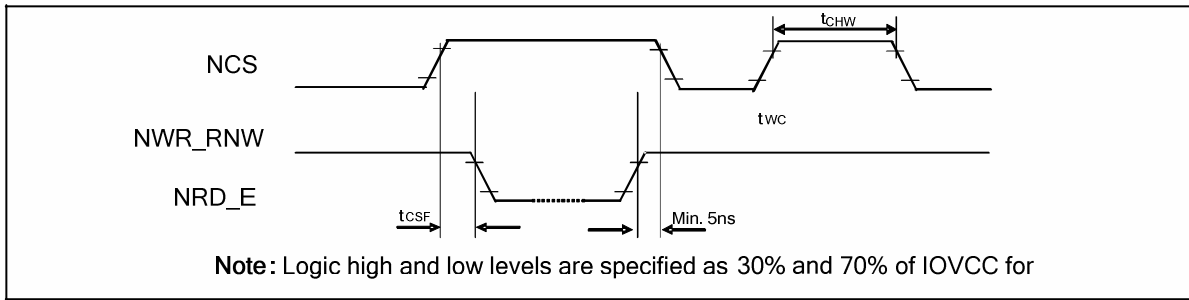


Figure 11.2 Chip select timing

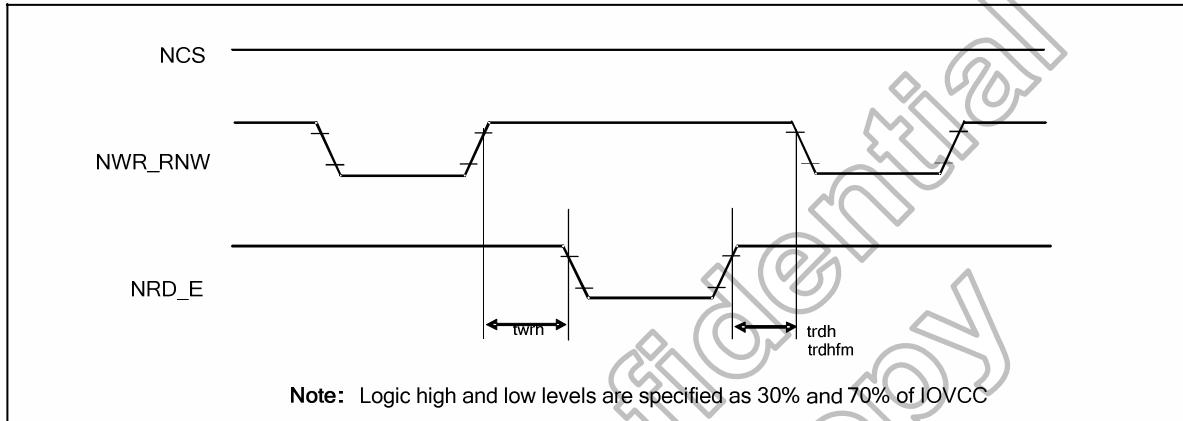


Figure 11.3 Write to read and read to write timing

11.4.2 Serial interface characteristics

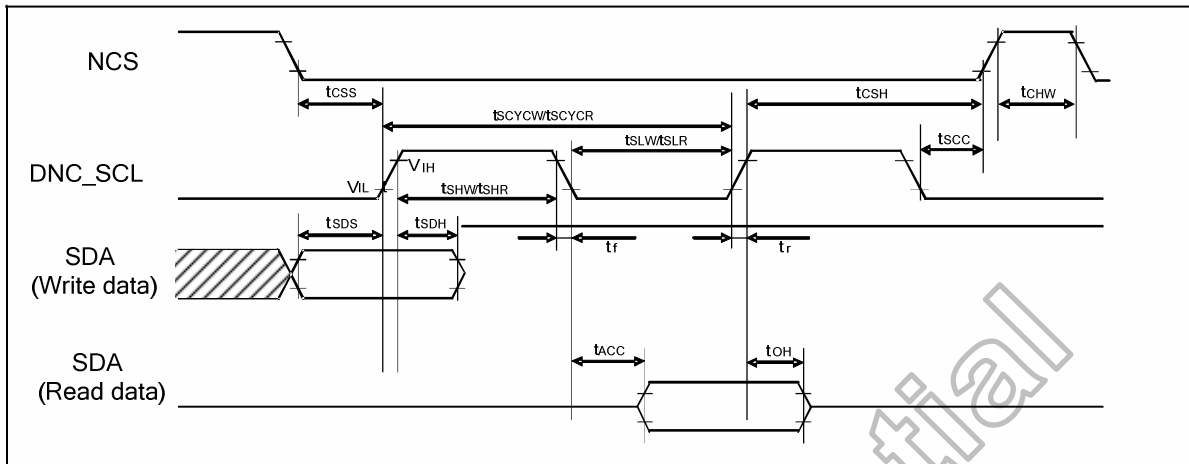


Figure 11.4 Serial interface characteristics

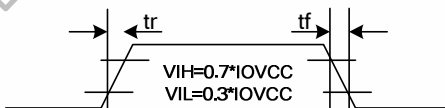
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3 V, TA= -30 to 70° C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	tSCYCW		40		-	
DNC_SCL "H" pulse width (Write)	tSHW	DNC_SCL	16	-	-	ns
DNC_SCL "L" pulse width (Write)	tSLW		16	-	-	
Data setup time (Write)	tSDS	SDA	16	-	-	ns
Data hold time (Write)	tSDH		16	-	-	
Serial clock cycle (Read)	tSCYCR		150		-	
DNC_SCL "H" pulse width (Read)	tSHR	DNC_SCL	60	-	-	ns
DNC_SCL "L" pulse width (Read)	tSLR		60	-	-	
Access Time	tACC	SDI for maximum CL=30pF For minimum CL=8pF	10	-	50	ns
Output disable time	tOH	SDO For maximum CL=30pF For minimum CL=8pF	15	-	50	ns
DNC_SCL to Chip select	tSCC	DNC_SCL, NCS	15	-	-	ns
NCS "H" pulse width	tCHW	NCS	40	-	-	ns
Chip select setup time	tCSS		60	-	-	ns
Chip select hold time	tCSH		65	-	-	ns

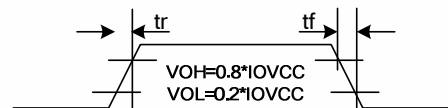
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



11.4.3 Reset input timing

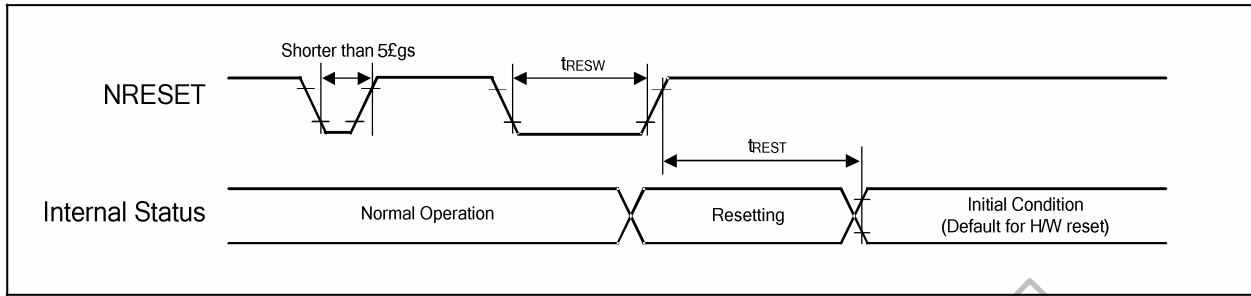


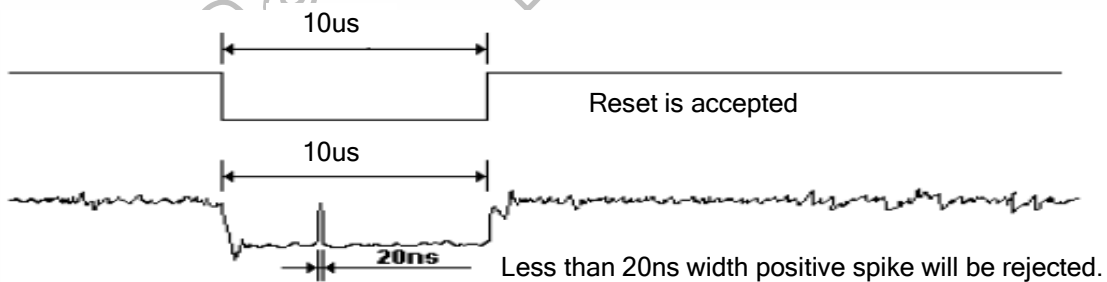
Figure 11.5 Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	μs
tREST	Reset complete time ⁽²⁾	-	5	-	-	When reset applied during Sleep Out mode	ms
		-	120	-	-	When reset applied during Sleep In mode	ms

Note: (1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

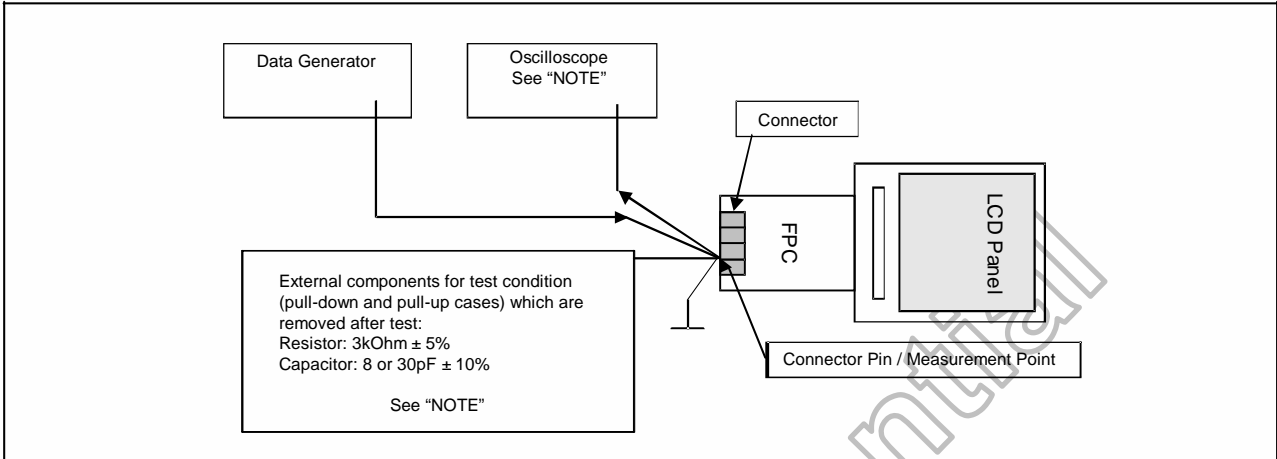
- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for HW reset.
- (3) During Reset Complete Time, ID2 and VCOMQF value in OTP will be latched to internal register during this period. This loading is done every time when there is HW reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



- (5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

11.5 tACC, tOH Measurement Condition

Measurement condition set-up



Note: Capacitances and resistances of the oscilloscope's probe must be included external components in these measurements

Figure 11.6 tACC and tOH measurement condition set-up

Minimum value measurement

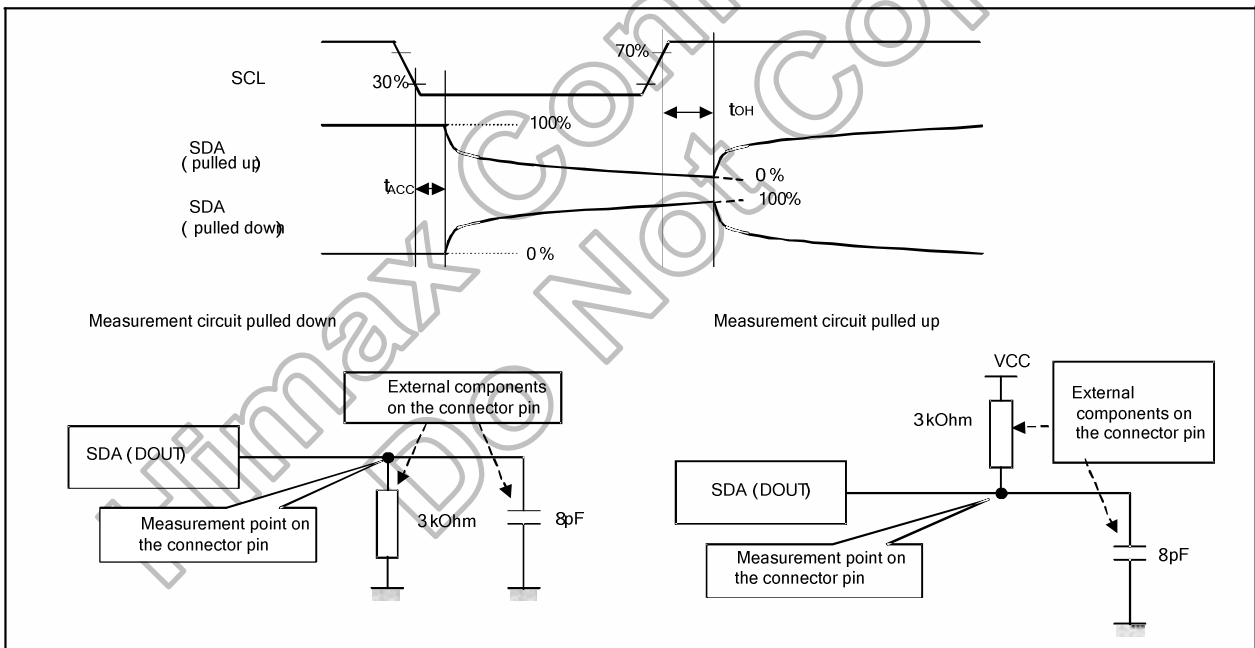


Figure 11.7 tACC and tOH minimum value measurement

Maximum value measurement

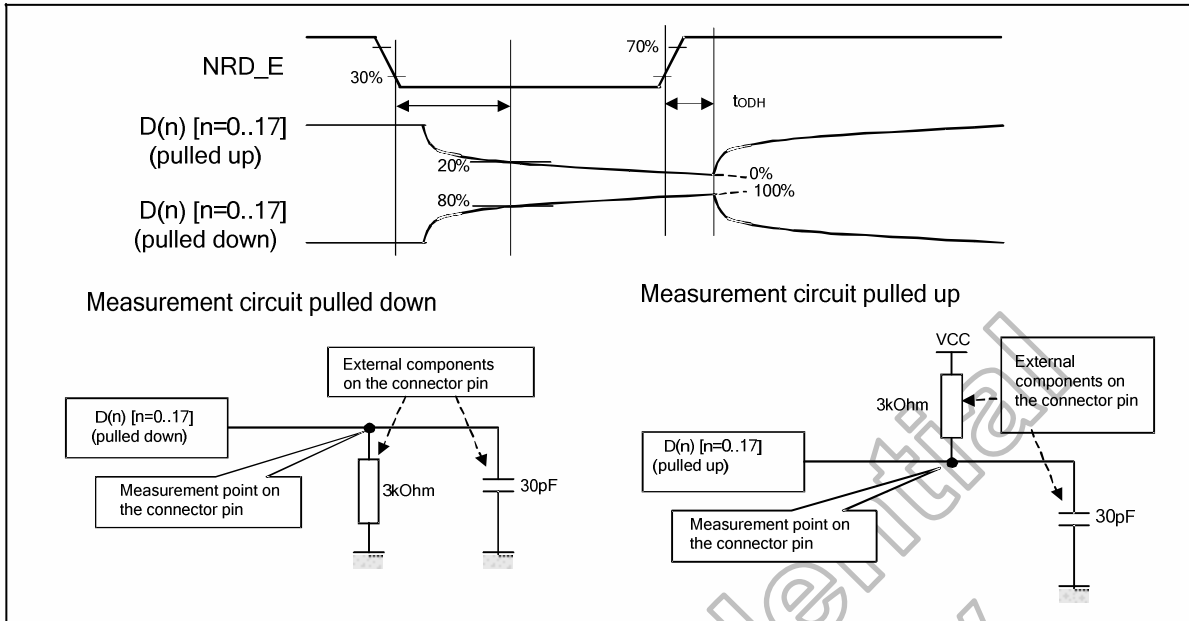
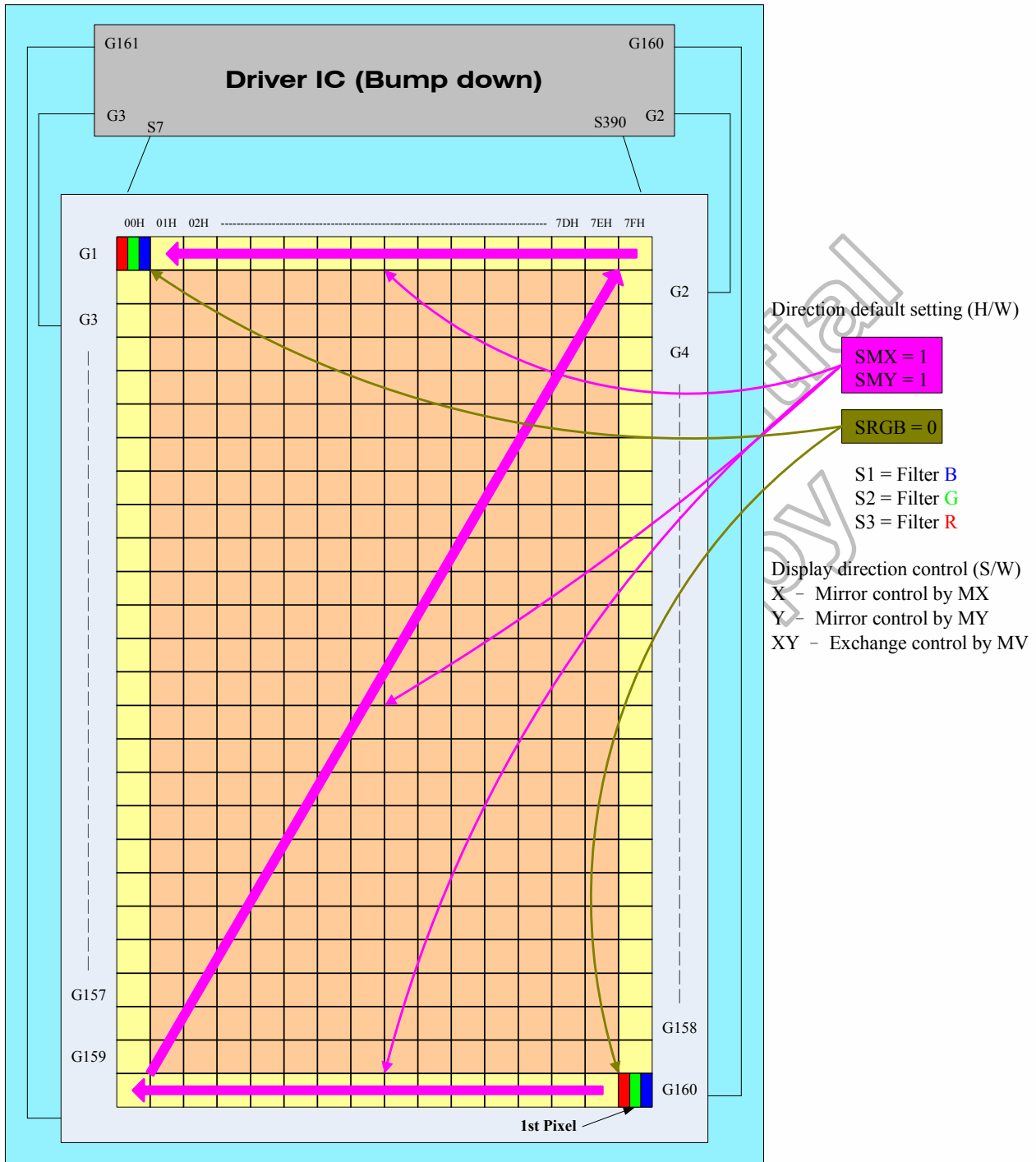


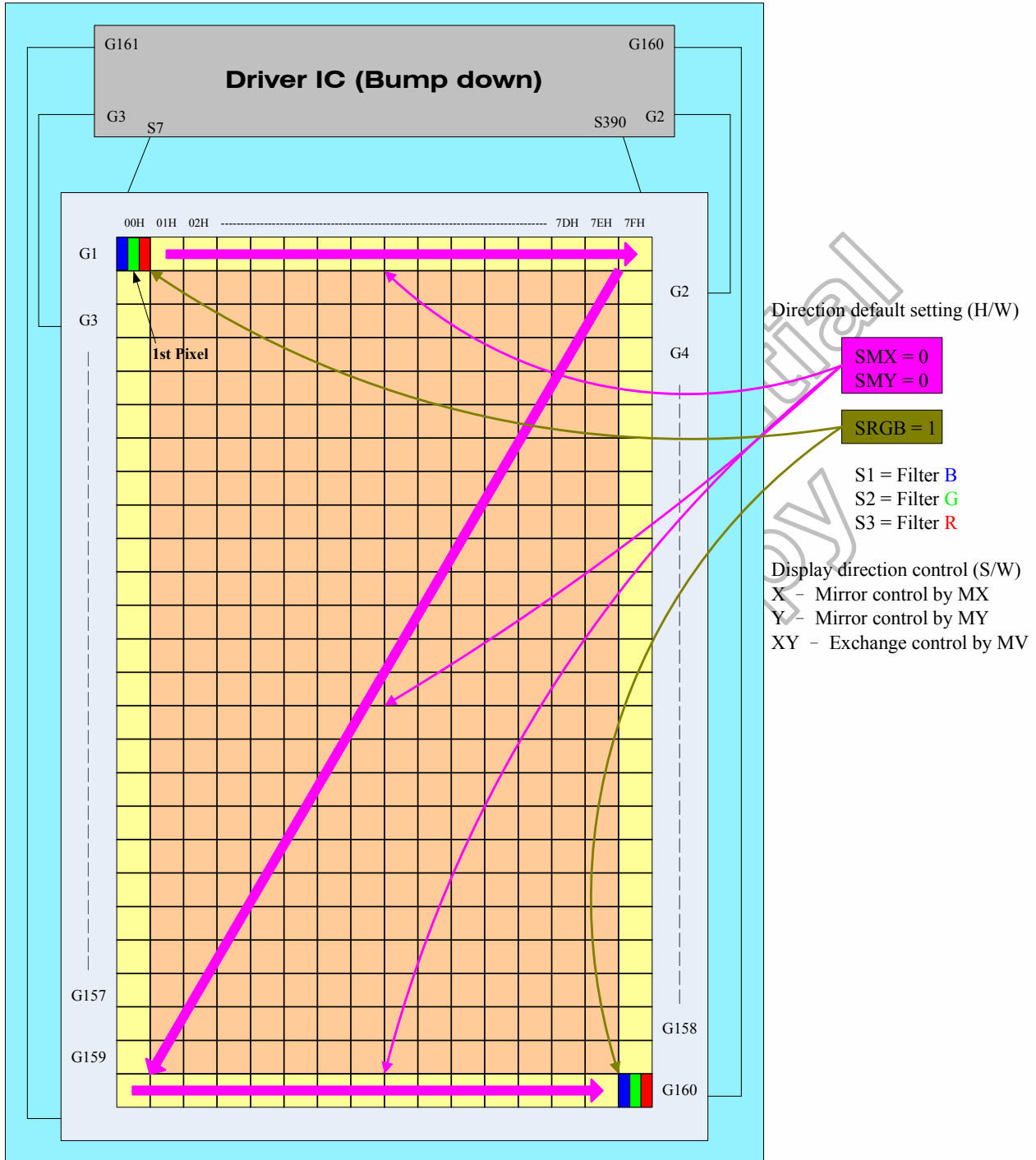
Figure 11.8 tACC and tOH maximum value measurement

Himax Confidential
Do Not Copy

11.6 1st Pixel is at right-bottom of the panel & RGB filter order = RGB



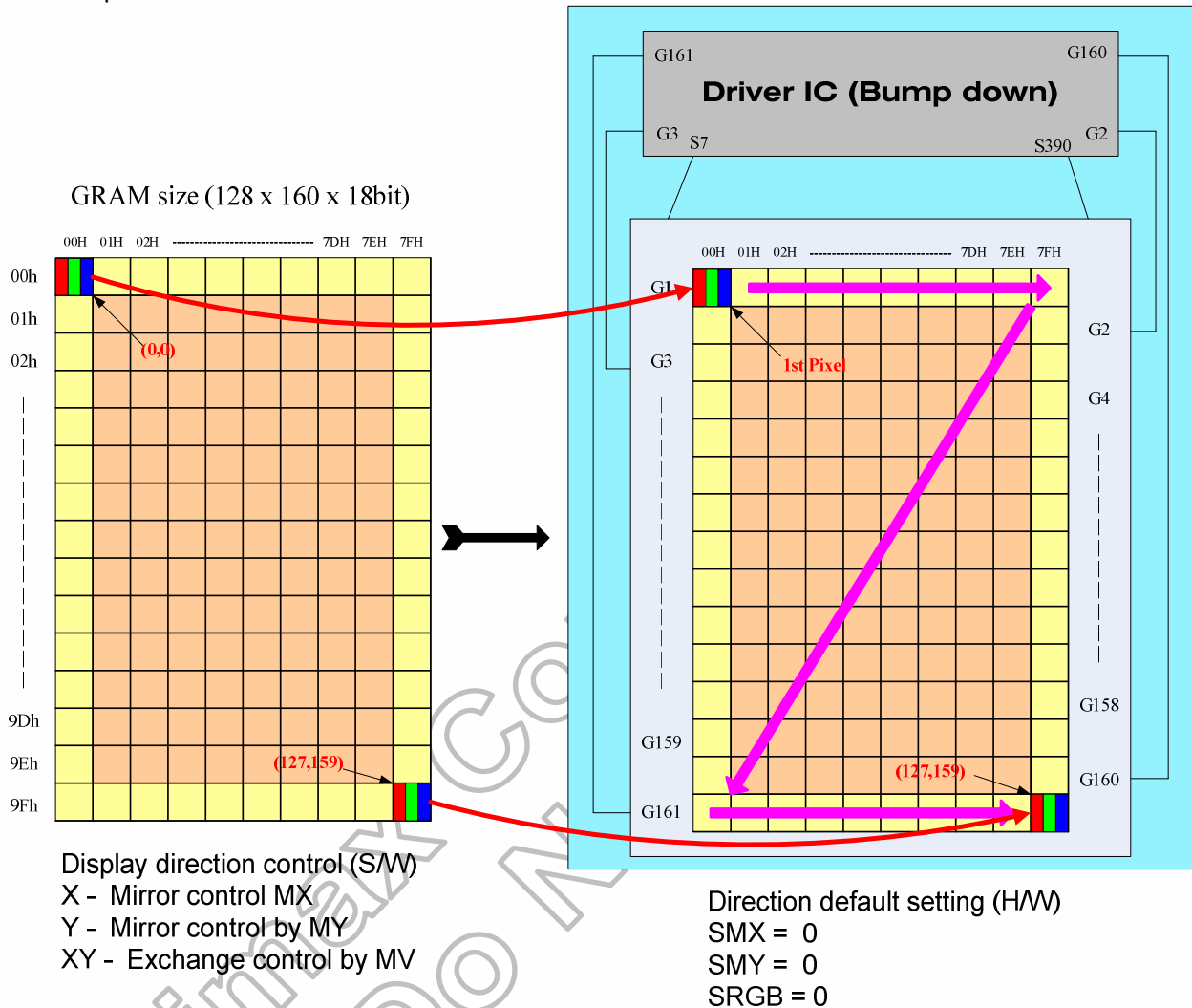
11.7 1st Pixel is at left-top of the panel & RGB filter order = BGR



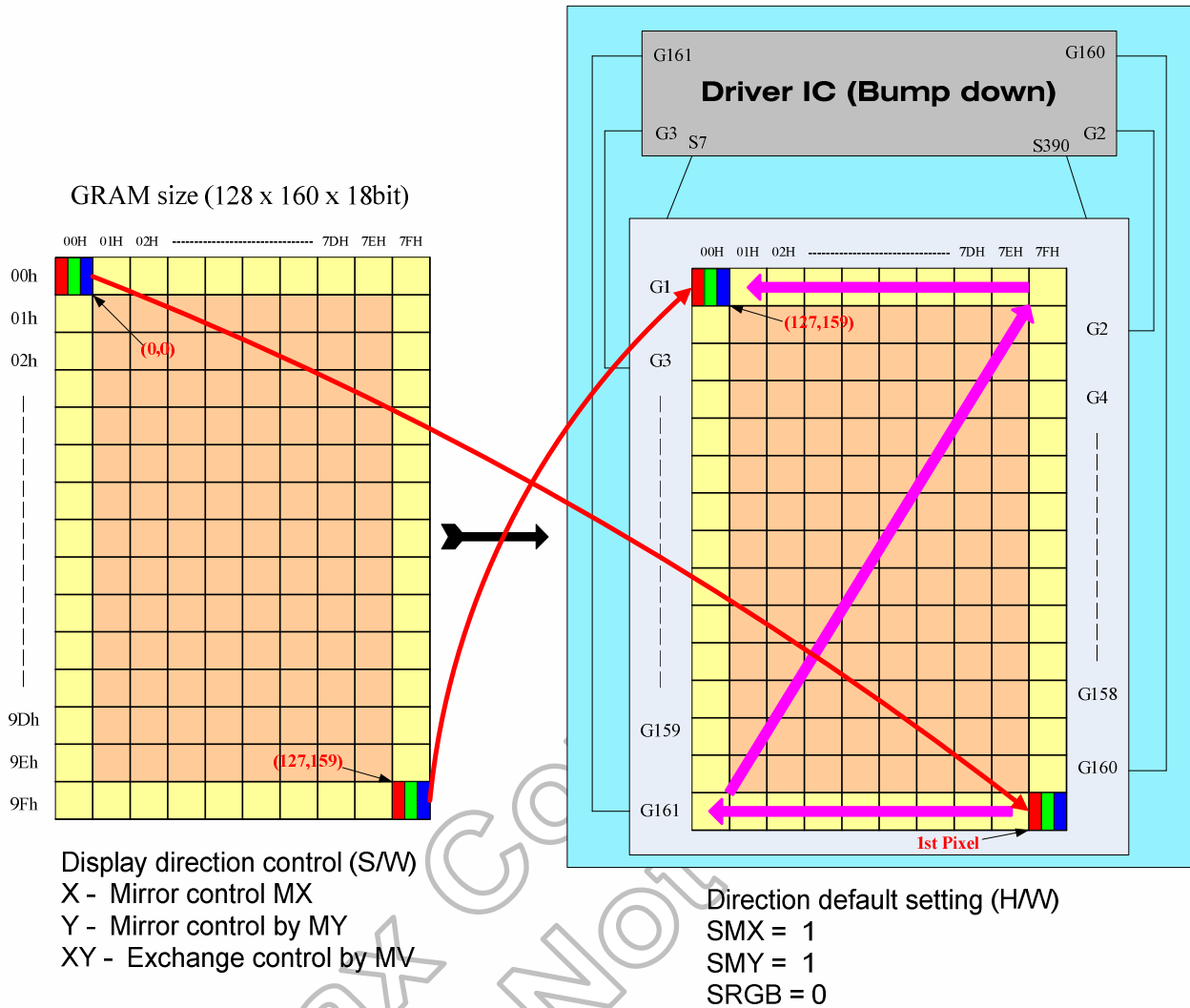
11.8 Application of connection with Different resolution

Case 1 of resolution (128RGB x 160) (RSO[2:0] = 011) RAM size = 128 x 160 x 18-bits (Used)
 Display size = 128RGB x 160

Example for SMX = SMY = 0

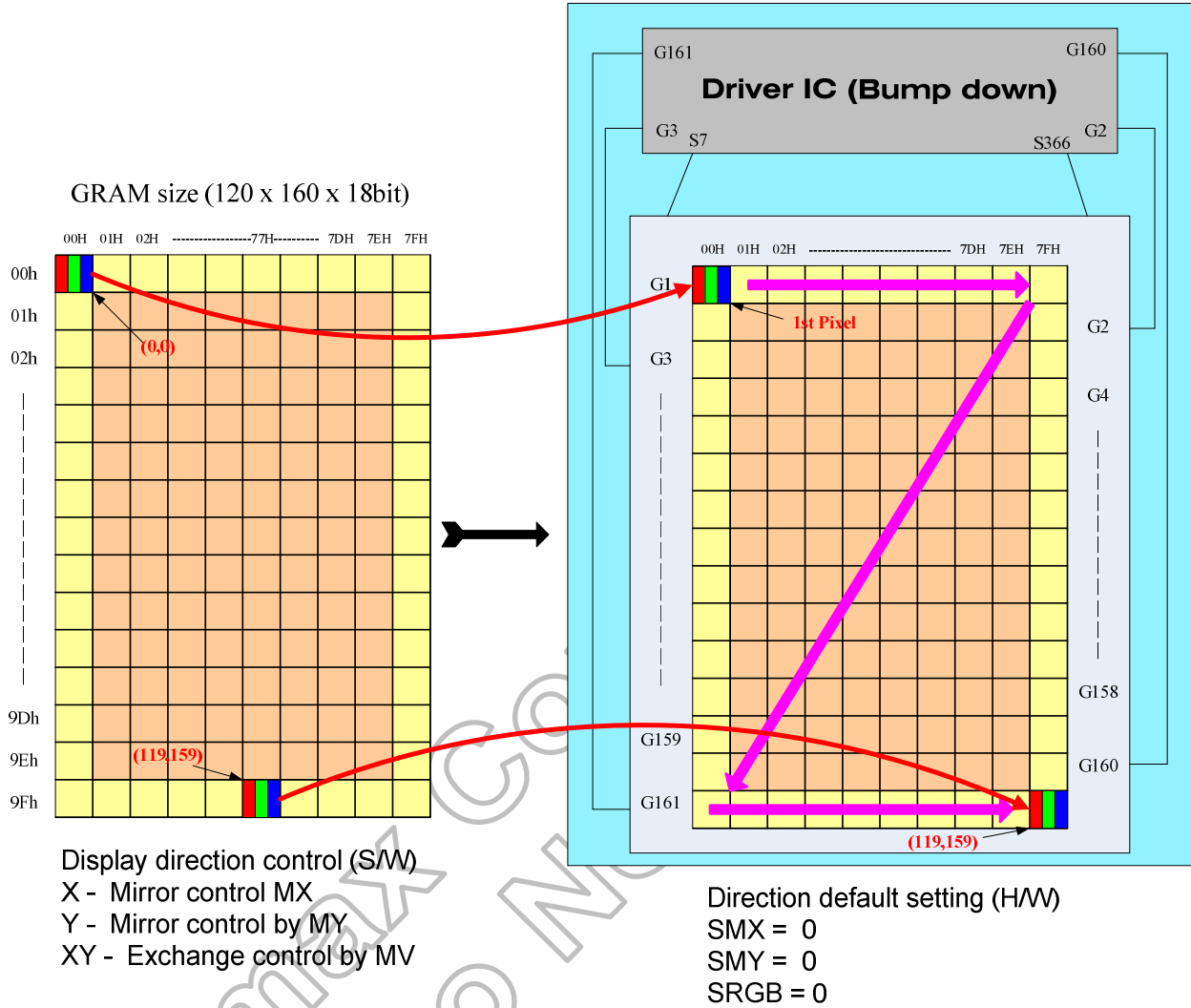


Example for SMX = SMY = 1

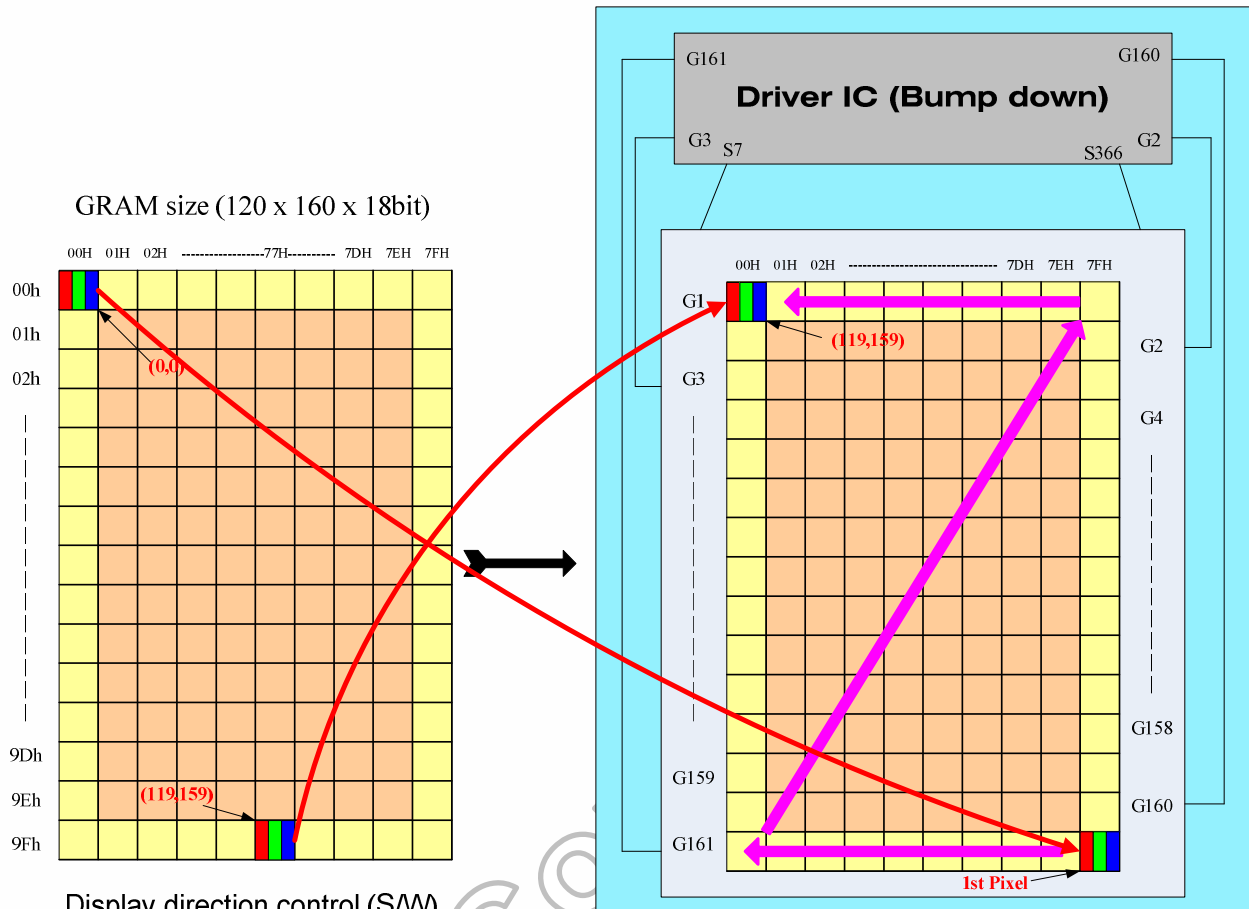


Case 2 of resolution (120RGB x 160) (RSO[2:0] = 010) RAM size = 120 x 160 x 18-bits (Used)
 Display size = 120RGB x 160

Example for SMX = SMY = 0



Example for SMX = SMY = 1



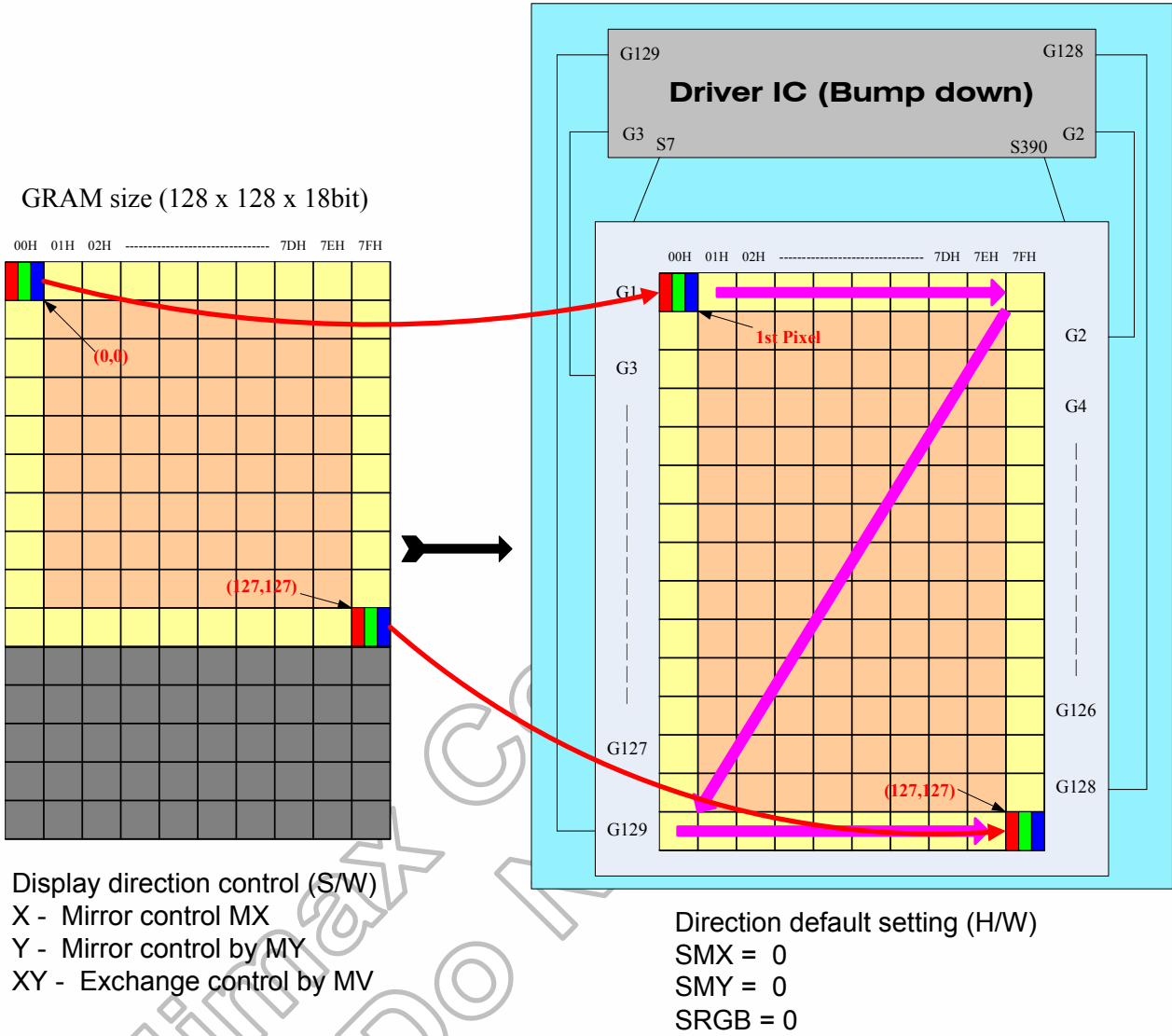
Display direction control (S/W)
 X - Mirror control MX
 Y - Mirror control by MY
 XY - Exchange control by MV

Direction default setting (H/W)
 SMX = 1
 SMY = 1
 SRGB = 0

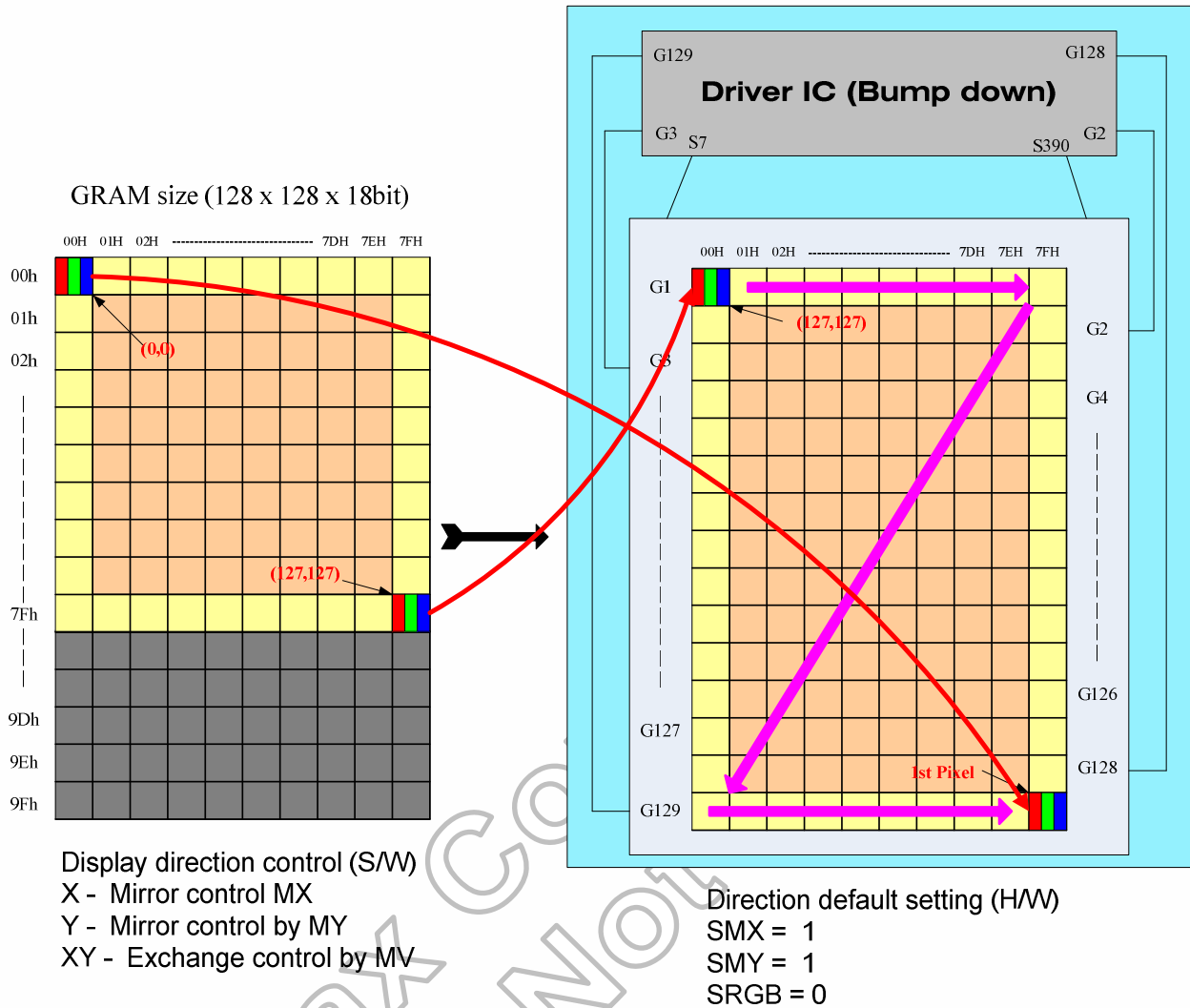
Himax Confidential
 Do Not

Case 3 of resolution (128RGB x 128) (RSO[2:0] = 001) RAM size = 128 x 128 x 18-bits (Used)
 Display size = 128RGB x 128

Example for SMX = SMY = 0

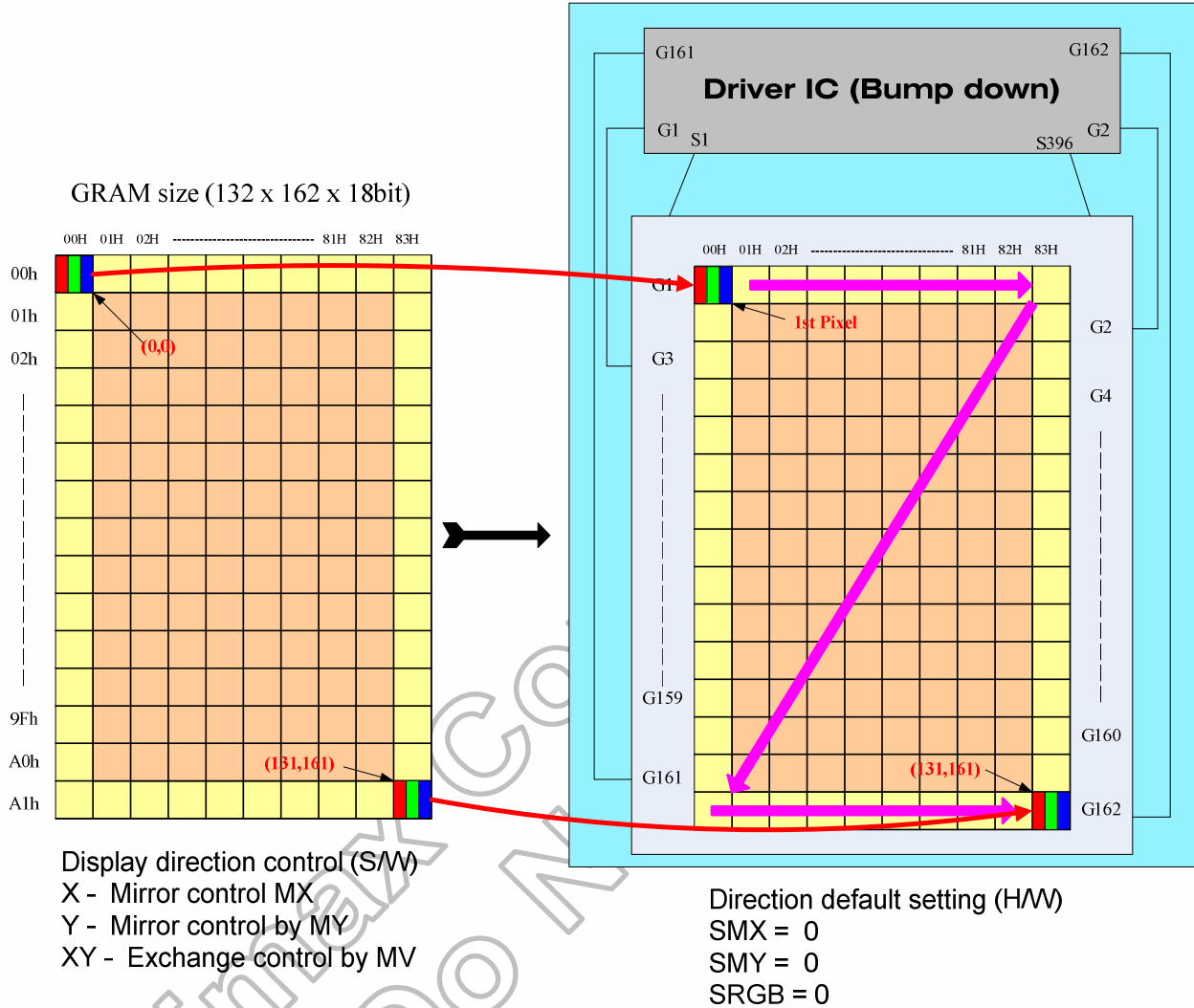


Example for SMX = SMY = 1

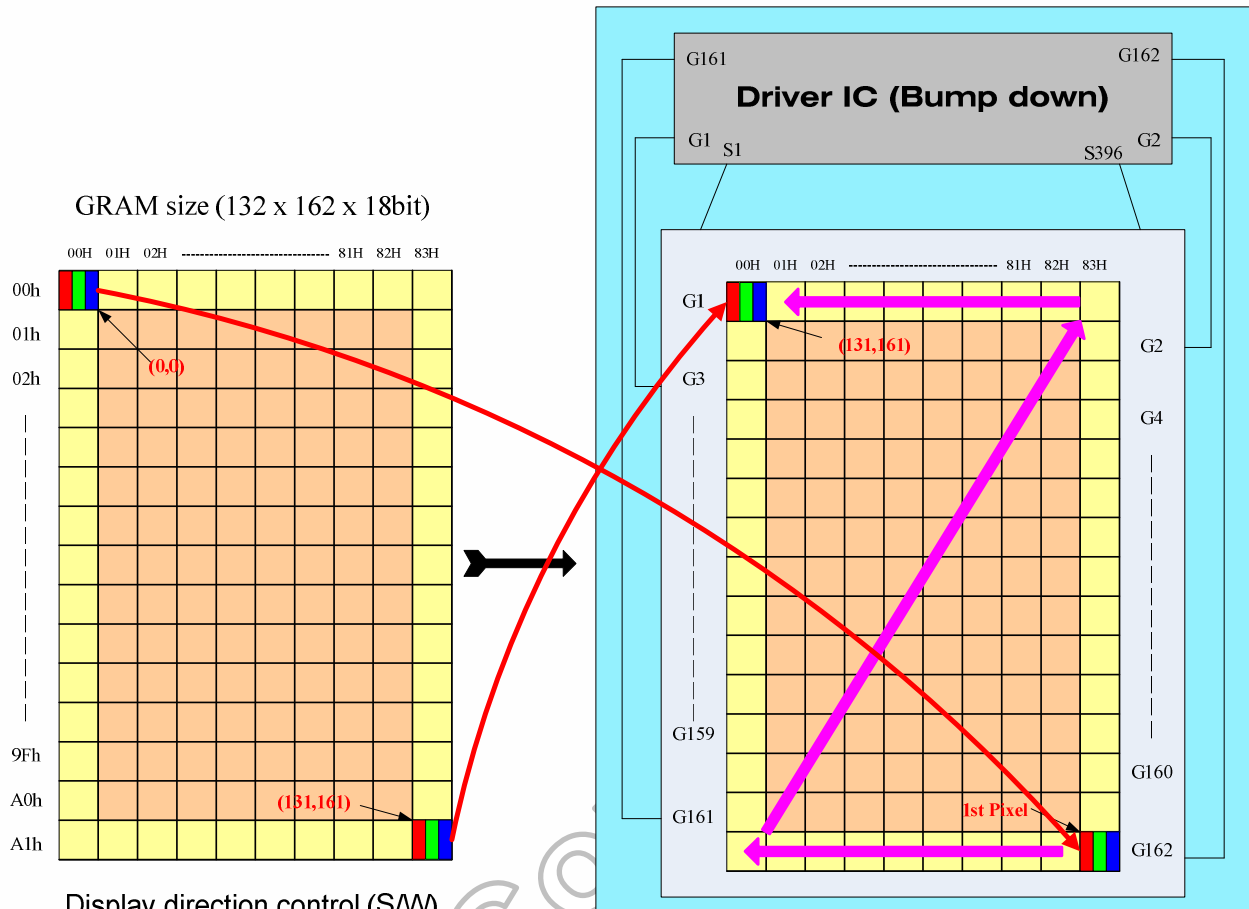


Case 4 of resolution (132RGB x 162) (RSO[2:0] = 000) RAM size = 132 x 162 x 18-bits (Used)
 Display size = 132RGB x 162 ~ Type 1
 (P.S : STE_SEL = 0 → Type 1 ; STE_SEL = 1 → Type 2)

Example for SMX = SMY = 0



Example for SMX = SMY = 1



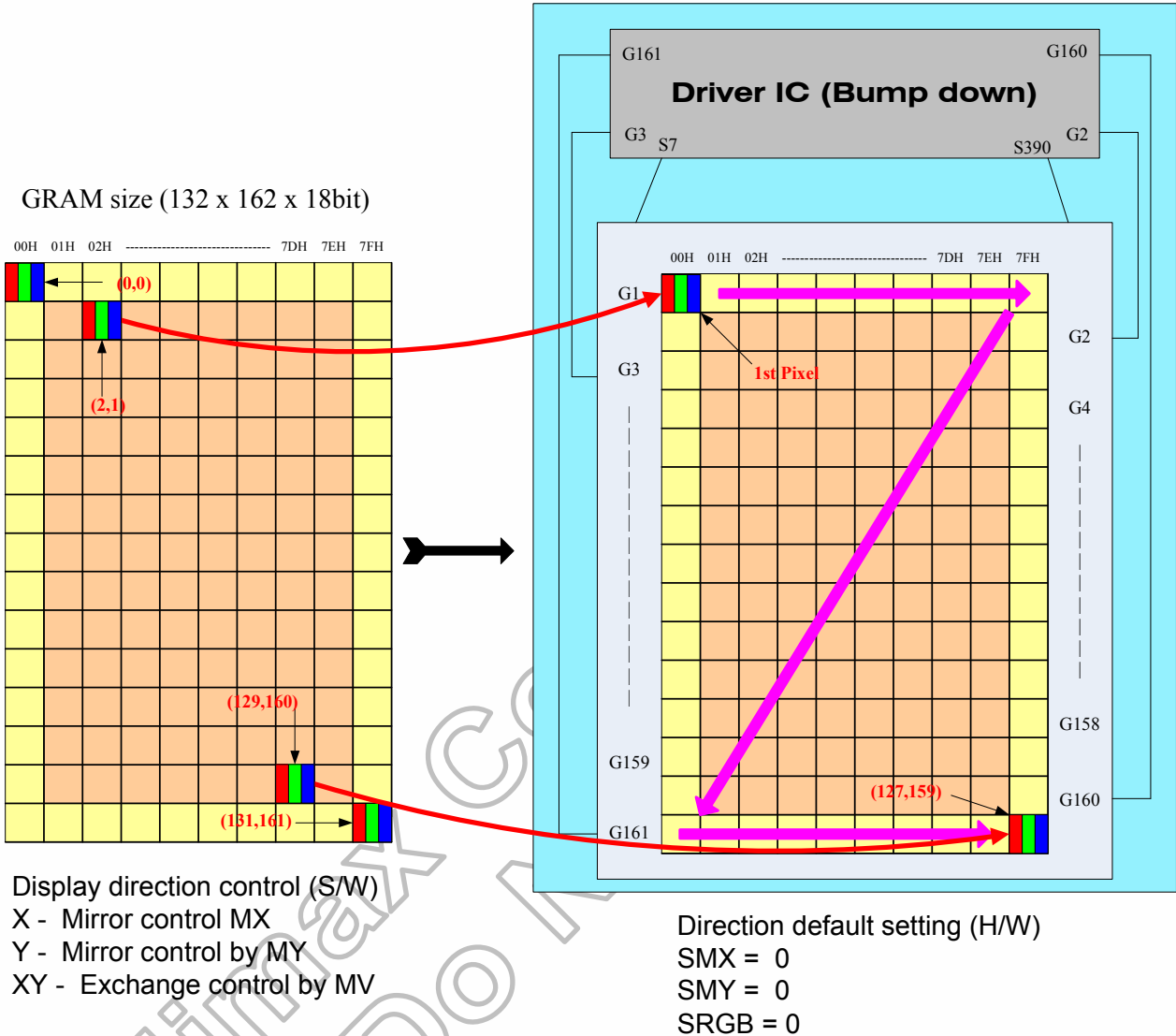
Display direction control (S/W)
 X - Mirror control MX
 Y - Mirror control by MY
 XY - Exchange control by MV

Direction default setting (H/W)
 SMX = 1
 SMY = 1
 SRGB = 0

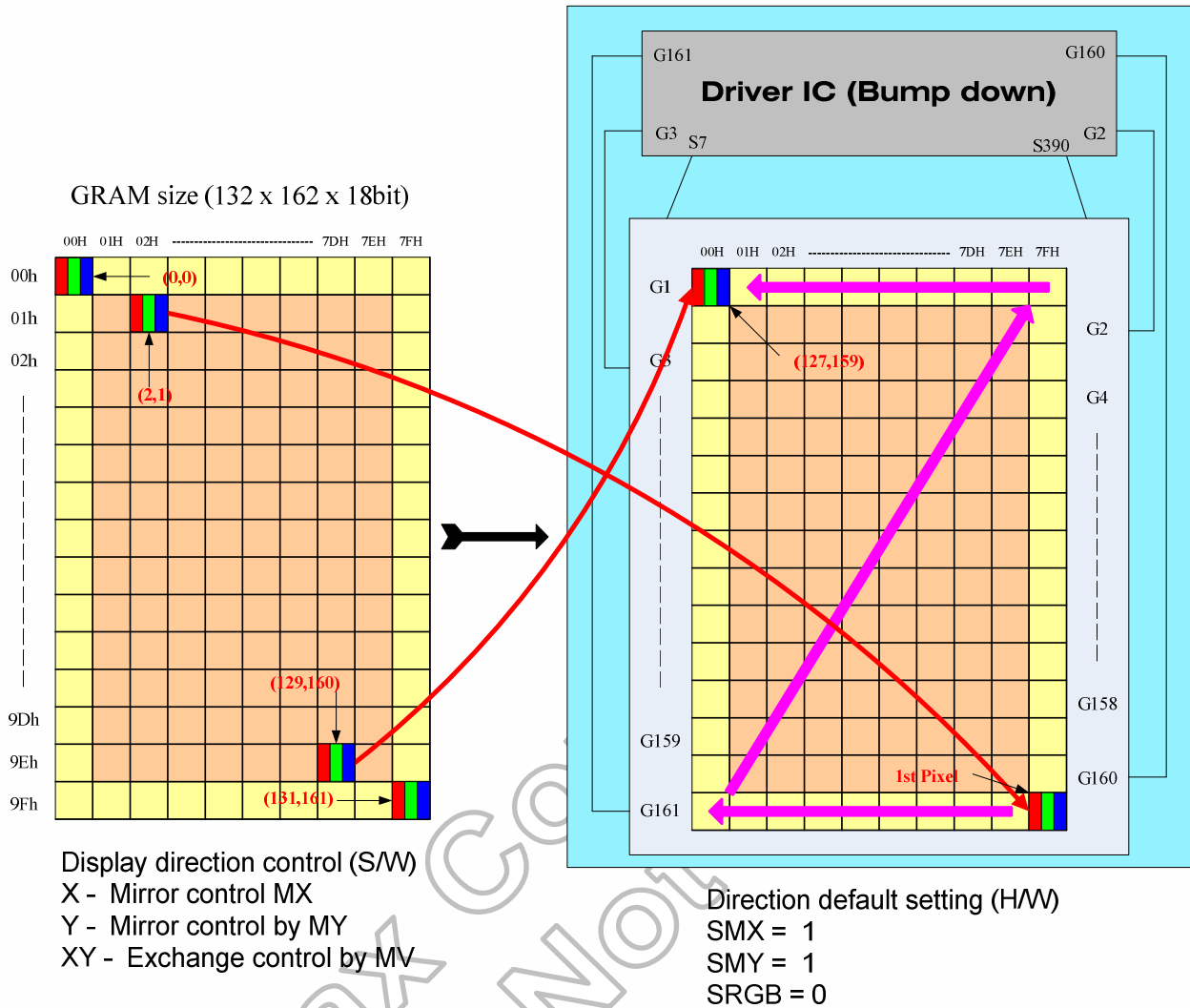
Himax Confidential
 Do Not

Display size = 132RGB x 162 ~ Type 2
 (P.S : STE_SEL = 0 → Type1 ; STE_SEL = 1 → Type 2)

Example for SMX = SMY = 0

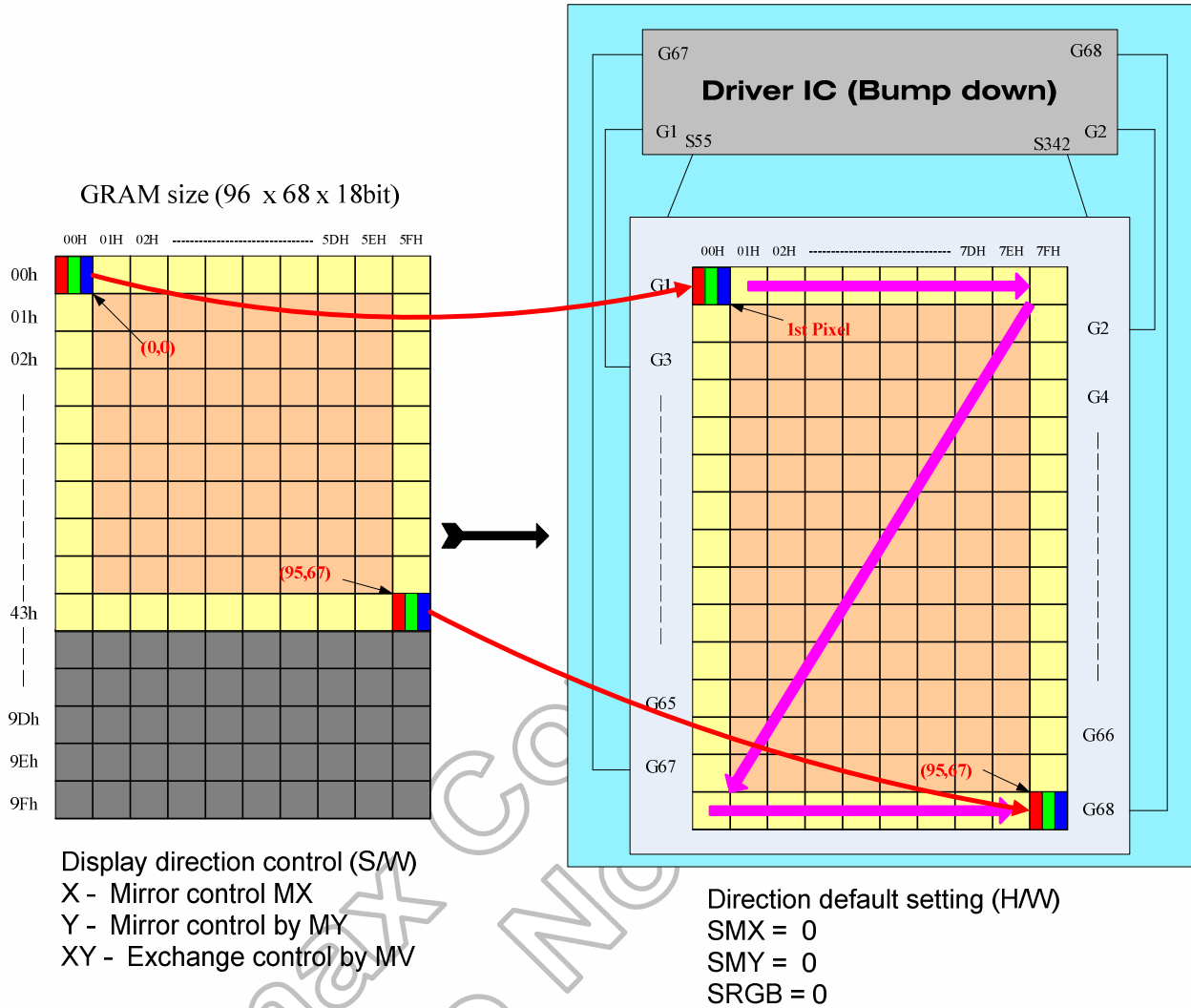


Example for SMX = SMY = 0

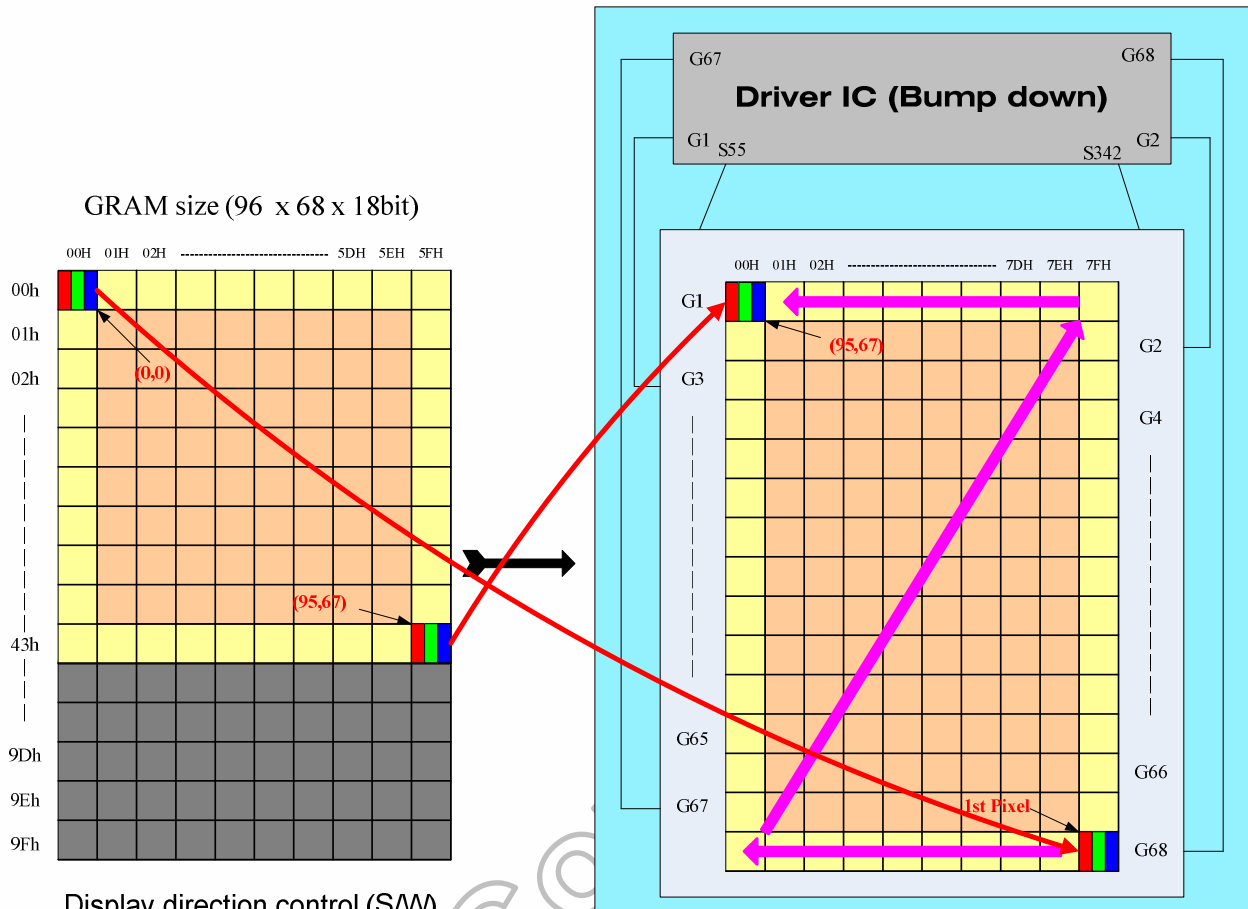


Case 5 of resolution (96RGB x 68) (RSO[2:0] = 100) RAM size = 96 x 68 x 18-bits (Used)
 Display size = 96RGB x 68

Example for SMX = SMY = 0



Example for SMX = SMY = 1



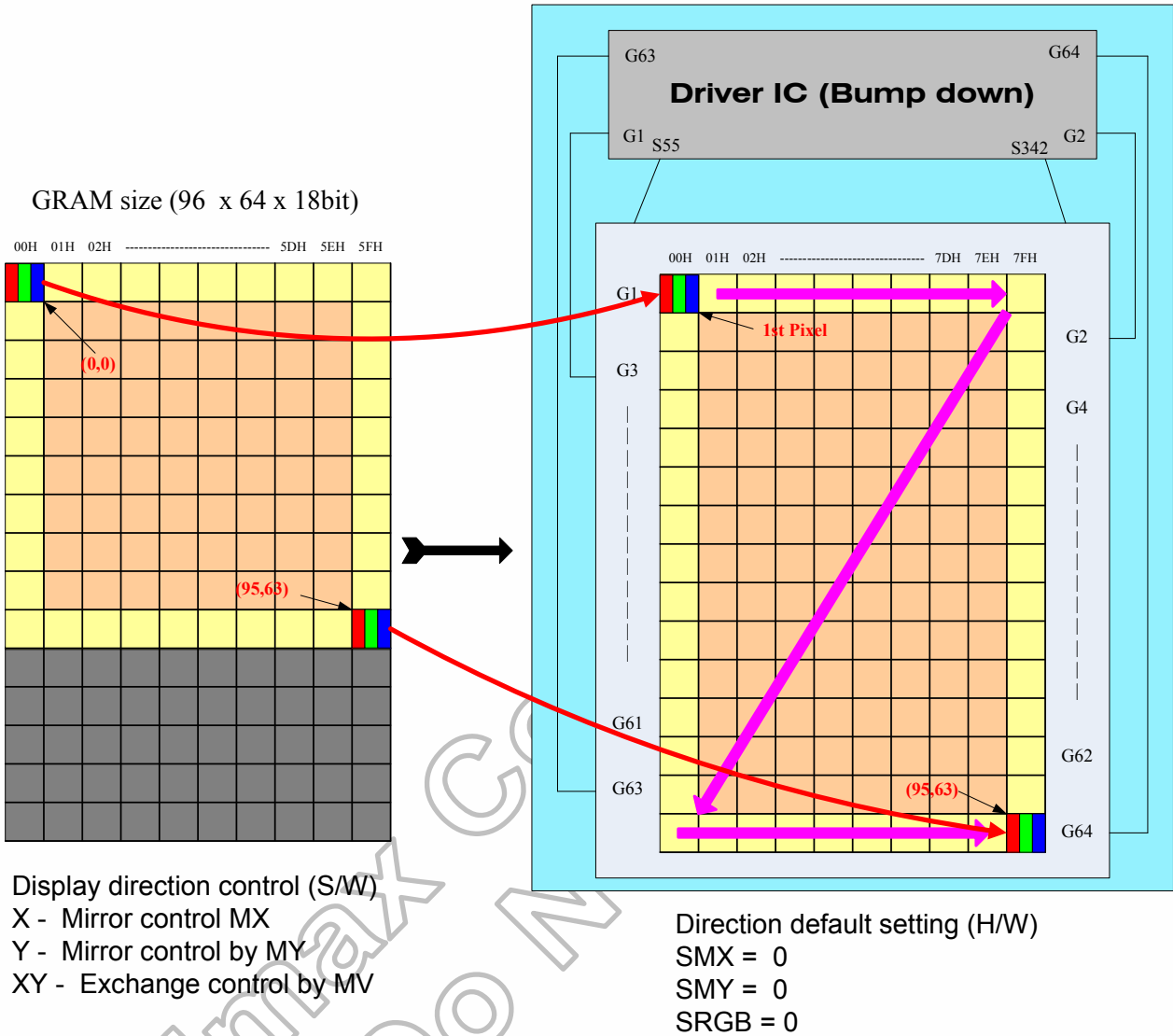
Display direction control (S/W)
 X - Mirror control MX
 Y - Mirror control by MY
 XY - Exchange control by MV

Direction default setting (H/W)
 SMX = 1
 SMY = 1
 SRGB = 0

Himax Confidential
 Do Not

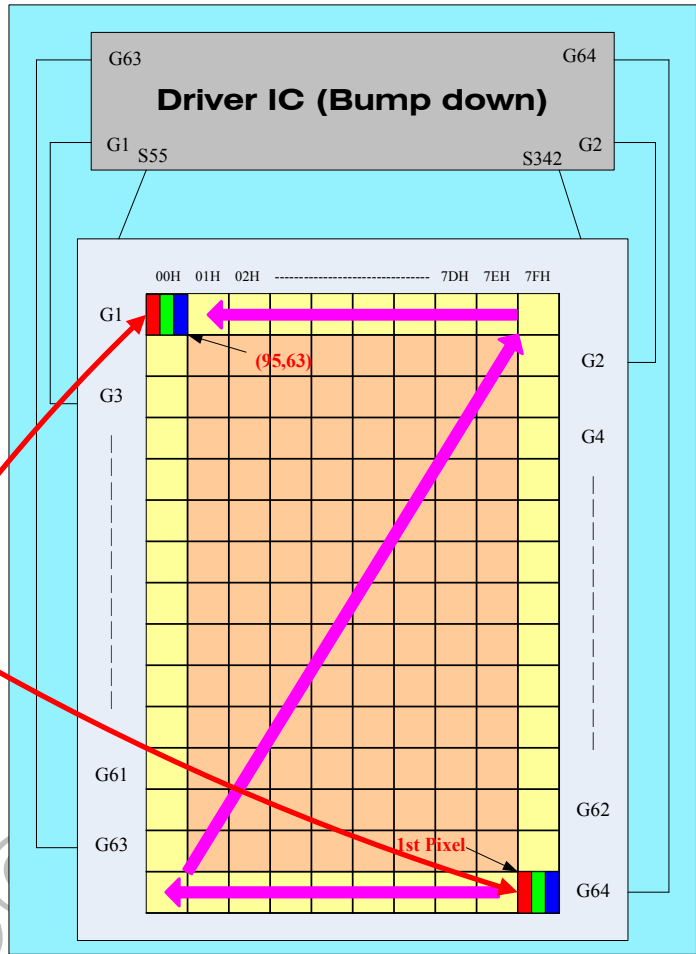
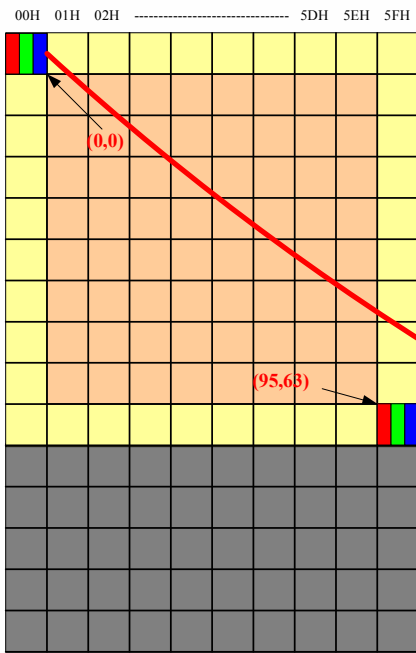
Case 6 of resolution (96RGB x 64) (RSO[2:0] = 101) RAM size = 96 x 64 x 18-bits (Used)
 Display size = 96RGB x 64

Example for SMX = SMY = 0



Example for SMX = SMY = 1

GRAM size (96 x 64 x 18bit)



Display direction control (S/W)
 X - Mirror control MX
 Y - Mirror control by MY
 XY - Exchange control by MV

Direction default setting (H/W)
 SMX = 1
 SMY = 1
 SRGB = 0

12. Ordering Information

Part No.	Package
HX8353-E000 <u>PDxxx</u>	PD : mean COG xxx : mean chip thickness (μm), (default: 250 μm)

13. Revision History

Version	Date	Description of Changes
01	2010-11-23	New setup
	2010/12/31	Modify PAD coordinates
	2011/2/17	Update register and OTP flow
	2011/9/30	1. Page 172 modify Read Himax Internal ID=53h 2. cover page preliminary version 01 delete "preliminary"
01.02	2011/11/15	1. Add reg C0h SETSTBA & B5h SETBGP define 2. Page 13 delete bump height 3. Page 158 modify reg B0h RADJ[3:0] table 4. Page 12 add LC_SEL1~0 pin define
01.03	2012/04/17	Page 181 pad 114 is modified from nvttestout to dummy

Himax Confidential
Do Not Copy