



DATA SHEET

(DOC No. HX8357-B-DS)

HX8357-B

320RGB x 480 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver
Preliminary version 01 January, 2010

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320RGB x 480 dot, 262K color, with internal
GRAM, TFT Mobile Single Chip Driver



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Preliminary Version 01

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1. General Description

This document describes Himax's HX8357-B is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 320RGBx480 dots.

The HX8357-B can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-B also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8357-B is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pages.

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2. Features

2.1 Display

- Resolution:
 - 320(H) x RGB(H) x 480(V)
- Display Color modes
 - Normal Display Mode On
 - 65,536(R(5),G(6),B(5)) colors
 - 262,144(R(6),G(6),B(6)) colors
 - Idle Mode On
 - 8 (R(1),G(1),B(1)) colors.

2.2 Display Module

- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
 - DDVDH = 4.6 to 6.0V (Source output voltage range)
 - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
 - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 320 (H) x 480 (V) x 18 bit

2.3 Display/Control Interface

- Display Interface types supported
 - MIPI-DBI Type-B 8-/9-/16-/18-bit MPU parallel interface.
 - MIPI-DBI Type-C OPTION1/3 Serial data transfer interface.
 - MIPI-DPI 16-/18-data lines parallel video (RGB) interface.
- Color modes
 - 16 bit/pixel: R(5), G(6), B(5)
 - 18 bit/pixel: R(6), G(6), B(6)

2.4 Display Module

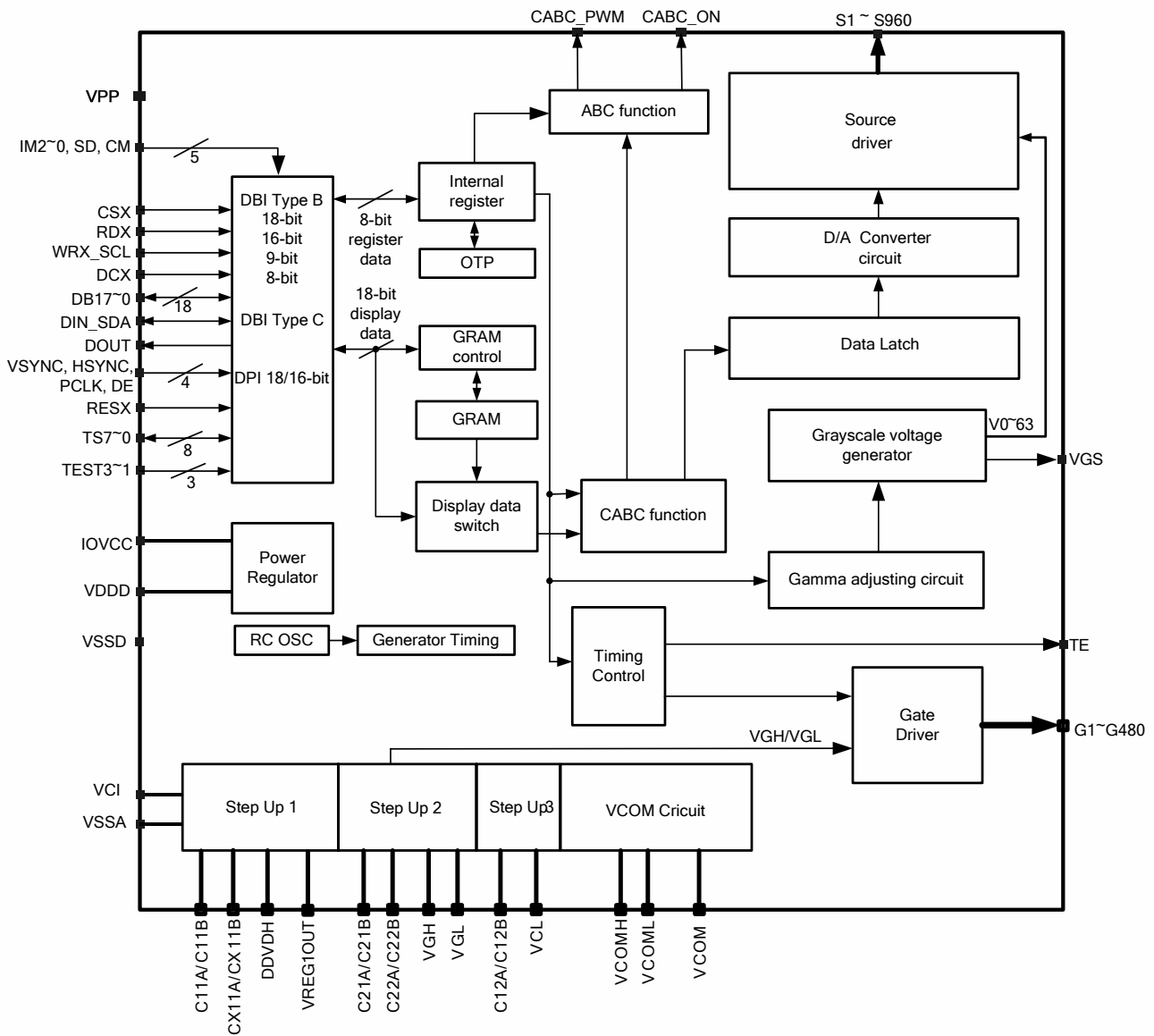
- Logic power supply (IOVCC): 1.65V ~ 3.3V
- Analog power supply (VCI): 2.5V ~ 3.3V
- OTP programming voltage (VPP): 7.5V ± 0.2

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support Line inversion or Frame inversion
- Support Vertical scrolling
- Support Partial display mode
- Support normal black/normal white LCD
- Support wide view angle display
- Support Deep standby mode
- On-chip OTP (One-time-programming) and MTP(Five-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function

3. Device Overview

3.1 Block Diagram



3.2 Pin Description

Input Parts									
Signals	I/O	Pin Number	Connected with	Description					
IM2, IM1, IM0	I	3	VSSD/ IOVCC	Select the MPU interface mode as listed below.					
				IM2	IM1	IM0	Interface mode	DB pins	Color mode
				0	0	0	DBI Type-B 18-bit	DB17-DB0: Data	262K
				0	0	1	DBI Type-B 9-bit	DB17-DB9: Unused, DB8-DB0: Data	262K
				0	1	0	DBI Type-B 16-bit	DB17-DB16: Unused, DB15-DB0: Data	65K / 262K
				0	1	1	DBI Type-B 8-bit	DB17-DB8: Unused, DB7-DB0: Data.	65K / 262K
				1	0	0	Inhibited	-	-
				1	0	1	DBI Type-C Option 1 (9 bits)	DB17-DB0: Data, DIN_SDA, DOUT	8 / 262K
				1	1	0	Inhibited	-	-
				Pixel format (RGB565/RGB666) is selected by Command (0x3Ah)					
CSX	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If not use, please connect to IOVCC.					
RESX	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. If not use, please connect to IOVCC.					
WRX_SCL	I	1	MPU	DBI Type-B: Serves as a write signal and write data at the low level. DBI Type-C: it servers as SCL (Serial Clock). If not use, please connect to IOVCC.					
RDX	I	1	MPU	DBI Type-B: Serves as a read signal and read data at the low level. If not use, please connect to IOVCC.					
DCX	I	1	MPU	Data / Command Selection pin If not use, please connect to IOVCC.					
VSYNC	I	1	MPU	Frame synchronizing signal for DPI I/F mode. If not use, please connect to IOVCC.					
HSYNC	I	1	MPU	Frame synchronizing signal for DPI I/F mode. If not use, please connect to IOVCC.					
PCLK	I	1	MPU	Pixel clock signal for DPI I/F mode. If not use, please connect to VSSD.					
DE	I	1	MPU	A DATA ENABLE signal for DPI I/F mode. If not use, please connect to VSSD.					
SD	I	1	MCU	Control pin of Normal display or shut down display in DPI(RM=1) interface mode.					
				SD	Display mode				
				0	Normal display				
1	Shut down display								
CM	I	1	MCU	Color mode direction H/W select pin in DPI interface mode.					
				CM	Color mode				
				0	Normal display color				
1	8-Color mode								

Output Part				
Signals	I/O	Pin Number	Connected with	Description
S1~S960	O	960	LCD	Output voltages applied to the liquid crystal.
G1~G480	O	480	LCD	Gate driver output pins. These pins output VGH, VGL
VCOM	O	16	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
CABC_ON	O	1	LED driver IC	If use CABC function (setting by BL), the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC. If not used, please open this pin.
CABC_PWM	O	1	LED driver IC	Backlight On/Off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC. If not used, please open this pin.
DOUT	O	1	MPU	Serial data output pin in serial bus system interface. If not used, please open this pin.

Input/Output Part				
Signals	I/O	Pin Number	Connected with	Description
DB17~0	I/O	18	MPU	When Operates in MIPI DBI interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 When Operation in MIPI DPI interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use DB5-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 If not used, please connect to VSSD.
DIN_SDA	I/O	1	MPU	Serial data input pin or input/output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. If not used, please connect to VSSD.

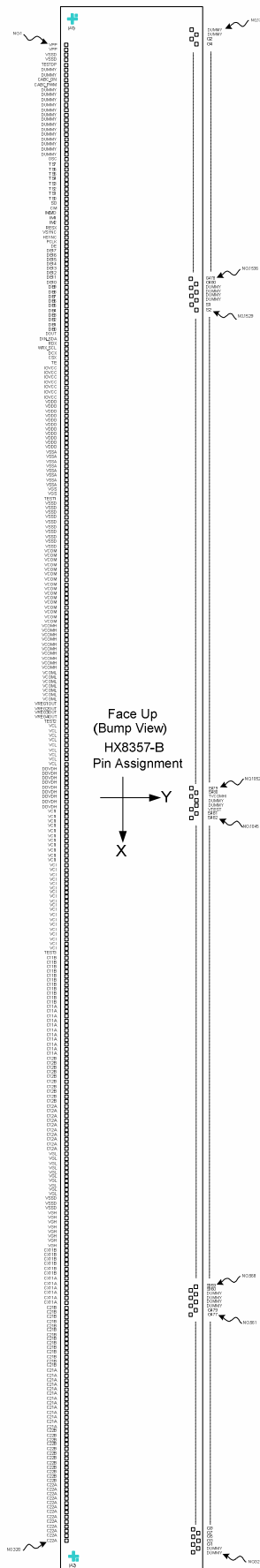
Power Part				
Signals	I/O	Pin Number	Connected with	Description
IOVCC	P	7	Power Supply	IO Pad and Digital power supply, 1.65V~3.3V
VCI	P	19	Power Supply	Analog power supply, 2.5V~3.3V
VPP	P	2	Power Supply	Power supply pin used in OTP program mode and operates at 7.5V ± 0.2. If not in OTP program mode, please let it open.
VSSD	P	15	Ground	Digital ground
VSSA	P	8	Ground	Analog ground
VDDD	O	11	Stabilizing Capacitor	Output from internal logic voltage. Connect to a stabilizing capacitor
VREG1OUT VREG2OUT VREG3OUT VREG4OUT	P	4	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VCI1	O	11	Open	Internal reference voltage output pin, please open this pin.
VCOMH	P	10	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	7	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.

Power Part				
Signals	I/O	Pin Number	Connected with	Description
VCL	P	9	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	9	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH. (See "configuration of the power supply").
VGH	P	8	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSA and VGH. (See "configuration of the power supply").
VGL	P	10	Stabilizing capacitor	An output from the step-up circuit2.or -3 ~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see "configuration of the power supply").
VGS	I	2	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
C11A,C11B CX11A,CX11B	P	34	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	P	20	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	P	52	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.

Test Pin and Others				
Signals	I/O	Pin Number	Connected with	Description
TEST3-1	I	3	GND	Test pin input (Internal pull low)
OSC	I	1	Open	A test pin. Disconnect it.
TESTDP	I	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
TVCOMHI	O	1	Open	A test pin. Disconnect it.
TS7~0	O	8	Open	A test pin. Disconnect it.
DUMMY	-	31	Open	Dummy pin. Disconnect it.

3.3 Pin Assignment

- Chip Size : 23250 x 847 um (Include seal ring and scribe line)
- Chip thickness : 250 um ± 25 um
- Pad Location : PAD Center
- Coordinate Origin : Chip Center
- Au Bump Size :
 - 1. 80 um x 50 um
Input
No. 1 to 320
 - 2. 120 um x 15 um
Staggered LCD output side
No. 321 to 1776
- The chip size includes the core size, seal ring size and scribe line size.
- Au bump pitch : Refer to Pad Coordinate.
- Au bump height : 15 um ± 3 um.
- Numbers in the figure corresponds to pad coordinate numbers.

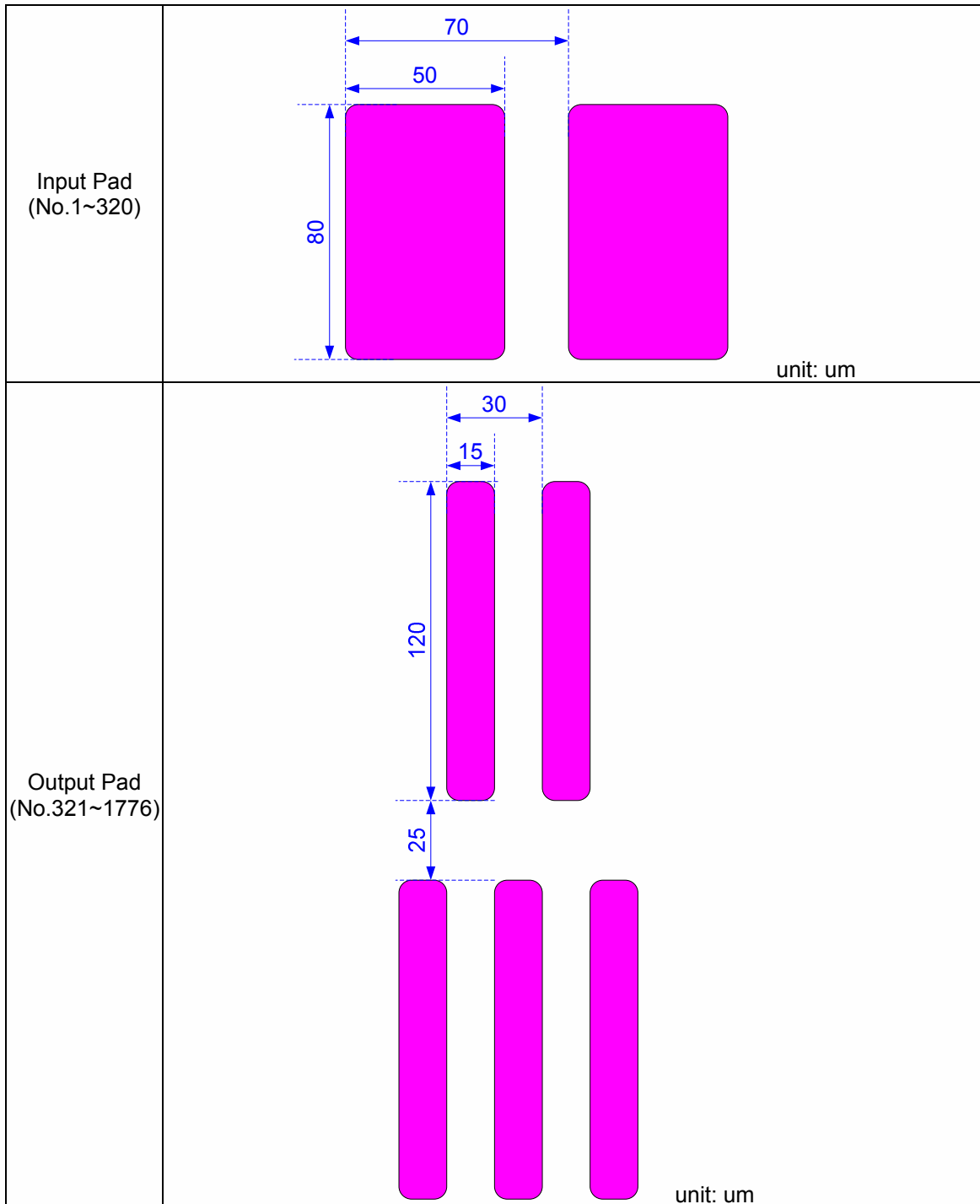


No.	Name	X	Y	Bump size
1681	G188	-9780	269	15 * 120
1682	G186	-9795	124	15 * 120
1683	G184	-9810	269	15 * 120
1684	G182	-9825	124	15 * 120
1685	G180	-9840	269	15 * 120
1686	G178	-9855	124	15 * 120
1687	G176	-9870	269	15 * 120
1688	G174	-9885	124	15 * 120
1689	G172	-9900	269	15 * 120
1690	G170	-9915	124	15 * 120
1691	G168	-9930	269	15 * 120
1692	G166	-9945	124	15 * 120
1693	G164	-9960	269	15 * 120
1694	G162	-9975	124	15 * 120
1695	G160	-9990	269	15 * 120
1696	G158	-10005	124	15 * 120
1697	G156	-10020	269	15 * 120
1698	G154	-10035	124	15 * 120
1699	G152	-10050	269	15 * 120
1700	G150	-10065	124	15 * 120
1701	G148	-10080	269	15 * 120
1702	G146	-10095	124	15 * 120
1703	G144	-10110	269	15 * 120
1704	G142	-10125	124	15 * 120
1705	G140	-10140	269	15 * 120
1706	G138	-10155	124	15 * 120
1707	G136	-10170	269	15 * 120
1708	G134	-10185	124	15 * 120
1709	G132	-10200	269	15 * 120
1710	G130	-10215	124	15 * 120
1711	G128	-10230	269	15 * 120
1712	G126	-10245	124	15 * 120
1713	G124	-10260	269	15 * 120
1714	G122	-10275	124	15 * 120
1715	G120	-10290	269	15 * 120
1716	G118	-10305	124	15 * 120
1717	G116	-10320	269	15 * 120
1718	G114	-10335	124	15 * 120
1719	G112	-10350	269	15 * 120
1720	G110	-10365	124	15 * 120
1721	G108	-10380	269	15 * 120
1722	G106	-10395	124	15 * 120
1723	G104	-10410	269	15 * 120
1724	G102	-10425	124	15 * 120
1725	G100	-10440	269	15 * 120
1726	G98	-10455	124	15 * 120
1727	G96	-10470	269	15 * 120
1728	G94	-10485	124	15 * 120
1729	G92	-10500	269	15 * 120
1730	G90	-10515	124	15 * 120
1731	G88	-10530	269	15 * 120
1732	G86	-10545	124	15 * 120
1733	G84	-10560	269	15 * 120
1734	G82	-10575	124	15 * 120
1735	G80	-10590	269	15 * 120
1736	G78	-10605	124	15 * 120
1737	G76	-10620	269	15 * 120
1738	G74	-10635	124	15 * 120
1739	G72	-10650	269	15 * 120
1740	G70	-10665	124	15 * 120

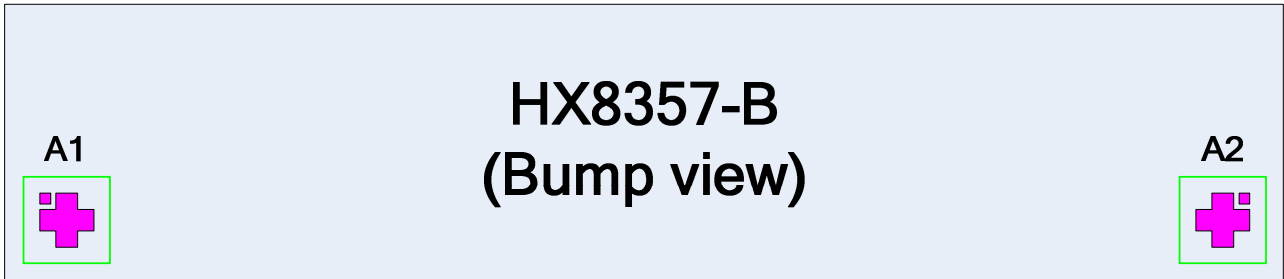
No.	Name	X	Y	Bump size
1741	G68	-10680	269	15 * 120
1742	G66	-10695	124	15 * 120
1743	G64	-10710	269	15 * 120
1744	G62	-10725	124	15 * 120
1745	G60	-10740	269	15 * 120
1746	G58	-10755	124	15 * 120
1747	G56	-10770	269	15 * 120
1748	G54	-10785	124	15 * 120
1749	G52	-10800	269	15 * 120
1750	G50	-10815	124	15 * 120
1751	G48	-10830	269	15 * 120
1752	G46	-10845	124	15 * 120
1753	G44	-10860	269	15 * 120
1754	G42	-10875	124	15 * 120
1755	G40	-10890	269	15 * 120
1756	G38	-10905	124	15 * 120
1757	G36	-10920	269	15 * 120
1758	G34	-10935	124	15 * 120
1759	G32	-10950	269	15 * 120
1760	G30	-10965	124	15 * 120
1761	G28	-10980	269	15 * 120
1762	G26	-10995	124	15 * 120
1763	G24	-11010	269	15 * 120
1764	G22	-11025	124	15 * 120
1765	G20	-11040	269	15 * 120
1766	G18	-11055	124	15 * 120
1767	G16	-11070	269	15 * 120
1768	G14	-11085	124	15 * 120
1769	G12	-11100	269	15 * 120
1770	G10	-11115	124	15 * 120
1771	G8	-11130	269	15 * 120
1772	G6	-11145	124	15 * 120
1773	G4	-11160	269	15 * 120
1774	G2	-11175	124	15 * 120
1775	DUMMY29	-11190	269	15 * 120
1776	DUMMY30	-11205	124	15 * 120

No.	Name	X	Y
A1	Alignment	-11300	-300
A2	Alignment	11300	-300

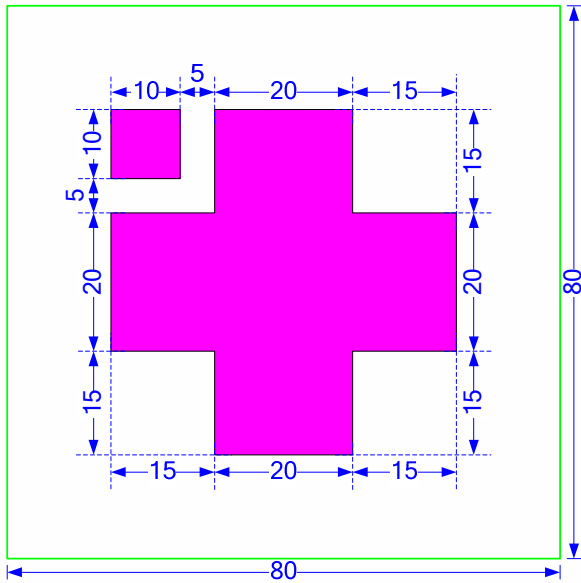
3.5 Bump Arrangement



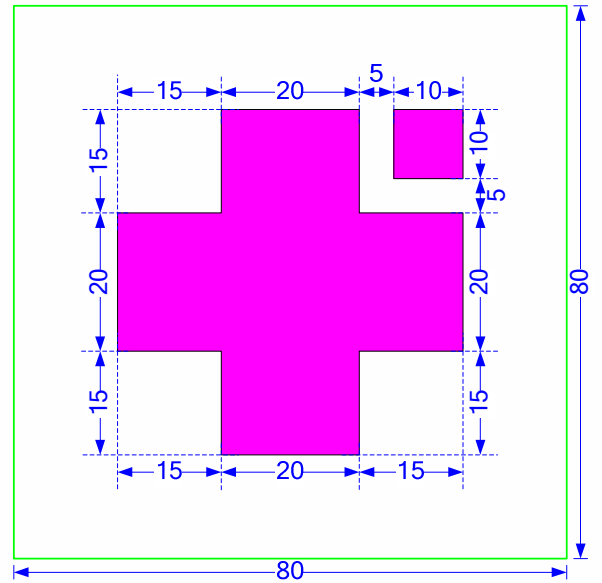
3.6 Alignment Mark



A1 (-11300, -300)



A2 (11300, -300)



unit: um

4. Interface Description

The HX8357-B supports MIPI interfaces: DBI (Display Bus Interface), DPI(Display Pixel Interface). Where DBI supports (18-/16-/9-/8-bit interface) Parallel Interface (Type-B) and Serial interface (Type-C). The interface mode can be selected by IM2-0 pins setting as show in table4.1.

IM2	IM1	IM0	Interface	Color mode
0	0	0	DBI Type-B 18-bit	262K
0	0	1	DBI Type-B 9-bit	262K
0	1	0	DBI Type-B 16-bit	65K / 262K
0	1	1	DBI Type-B 8-bit	65K / 262K
1	0	0	Inhibited	-
1	0	1	DBI Type-C Option 1(9 bits)	8 / 262K
1	1	0	Inhibited	-
1	1	1	DBI Type-C Option 3 (8 bits)	8 / 262K

Table 4.1: Interface Selection

The HX8357-B includes an index register (IR), which is stored the index data of internal control register and GRAM. When DCX =”L”, the command via DBI interface write into register. when DCX =”H”, GRAM data via R2Ch register can be written through data bus. There are two 16-bit bus control registers, which are used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the read data in data bus in first read operation is invalid, and the read data in data bus in second and the following read operation is valid.

Interface	RDX	WRX_SCL	DCX	DB17 –DB0 or other input pin
DBI Type-C Option 1	Unused	SCL	Unused	DB17 – DB0: 18 bit data bus DIN_SDA
DBI Type-C Option 3	Unused	SCL	DCX	DB17 – DB0: 18 bit data bus DIN_SDA
DBI Type-B 8-bit parallel	RDX	WRX	DCX	DB17 – DB8: Unused, DB7 – DB0 : 8 bit data bus
DBI Type-B 9-bit parallel	RDX	WRX	DCX	DB17 – DB9: Unused, DB8 – DB0: 9 bit data bus
DBI Type-B 16-bit parallel	RDX	WRX	DCX	DB17 – DB16: Unused, DB15 – DB0: 16 bit data bus
DBI Type-B 18-bit parallel	RDX	WRX	DCX	DB17 – DB0: 18 bit data bus

Table 4.2: Pin connection according of different interface

4.1 MIPI DBI-B Interface

The selection of DBI Type-B interface is by IM2 pin .When this pin is Low state (VSSD), the interface is use DBI system. And use IM1~IM0 pin to select DBI-B interface mode. The parallel interface timing diagram is described in Figure 4.1 and 4.2.

DBI Type-B Write to register or GRAM

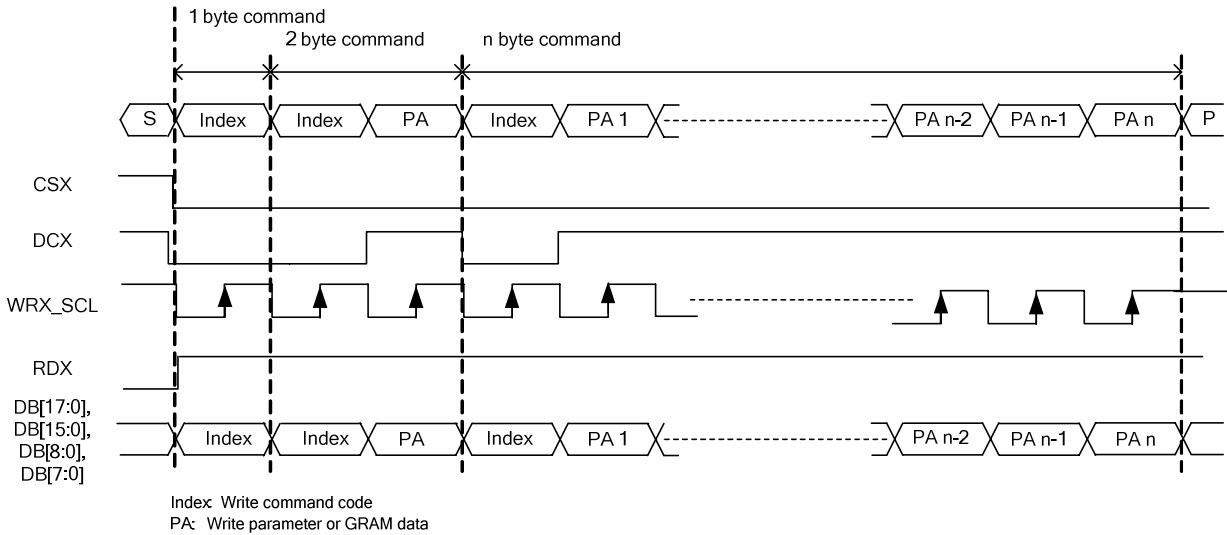


Figure 4.1: DBI-B System interface protocol, write to register or GRAM

DBI Type-B Read from register or GRAM

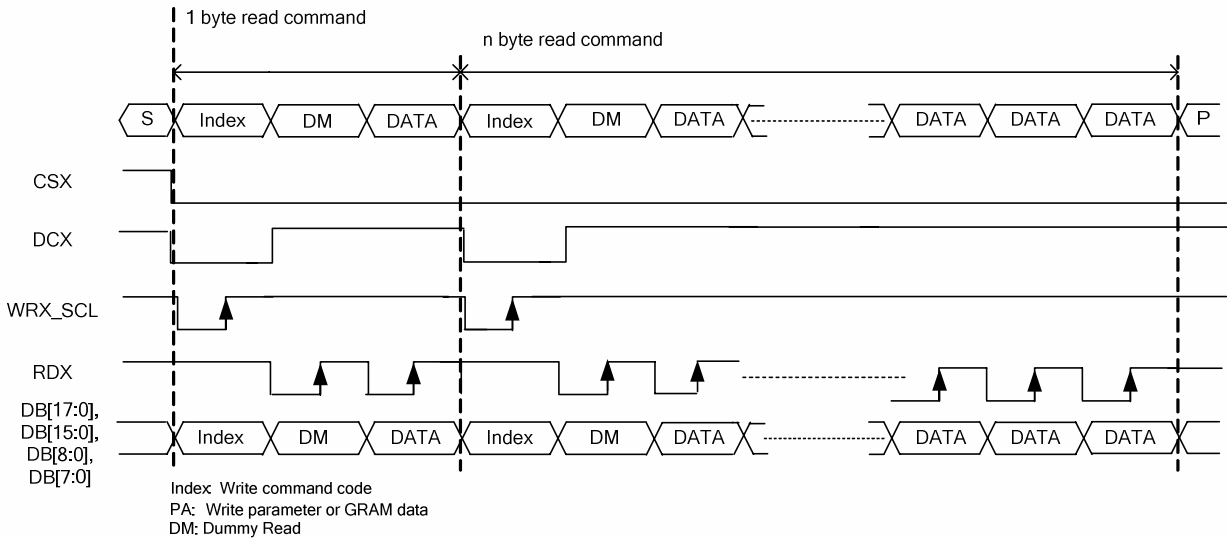


Figure 4.2: DBI-B System interface protocol, read from register or GRAM

4.1.1 DBI Type-B 18-bit Parallel Bus System Interface

The DBI-B system 18-bit bus parallel data transfer can be used by setting “IM2-0” pins to “000”. The Figure 4.3 is the example of interface with 18-bit DBI Type-B microcomputer system interface.

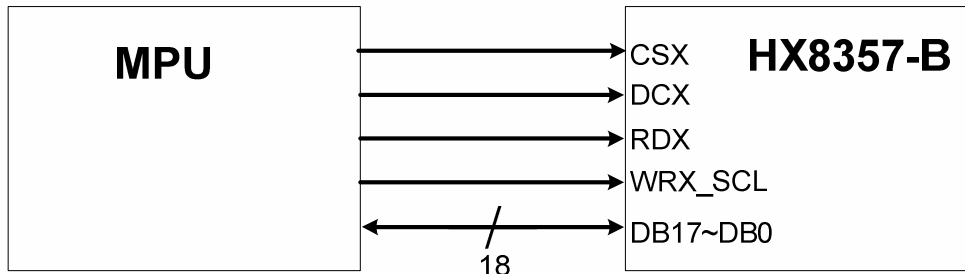


Figure 4.3: Example of DBI Type-B System 18-Bit Parallel Bus Interface

4.1.2 16-bit Parallel Bus System Interface

The DBI-B system 16-bit bus parallel data transfer can be used by setting “IM2-0” pins to “010”. The Figure 4.4 is the example of interface with 16-bit DBI Type-B microcomputer system interface.

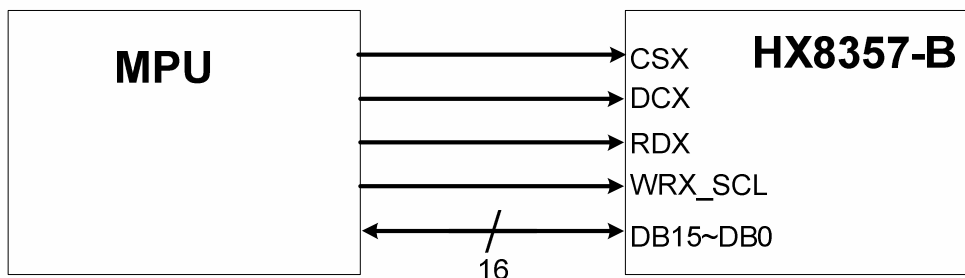


Figure 4.4: Example of DBI-B- System 16-bit bus Interface

4.1.3 9-bit Parallel Bus System Interface

The DBI Type-B system 9-bit bus parallel data transfer can be used by setting “IM2-0” pins to “001”. The Figure 4.5 is the example of interface with 9-bit DBI Type-B microcomputer system interface.

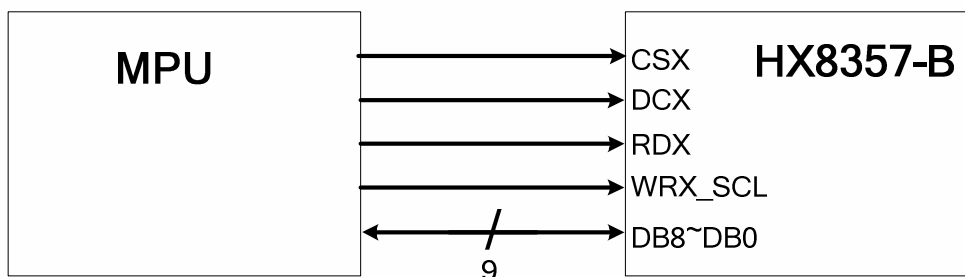


Figure 4.5: Example of DBI Type-B System 9-bit bus Interface

4.1.4 8-bit Parallel Bus System Interface

The DBI Type-B system 8-bit bus parallel data transfer can be used by setting “IM2-0” pins to “011”. The Figure 4.6 is the example of interface with 8-bit DBI Type-B microcomputer system interface.

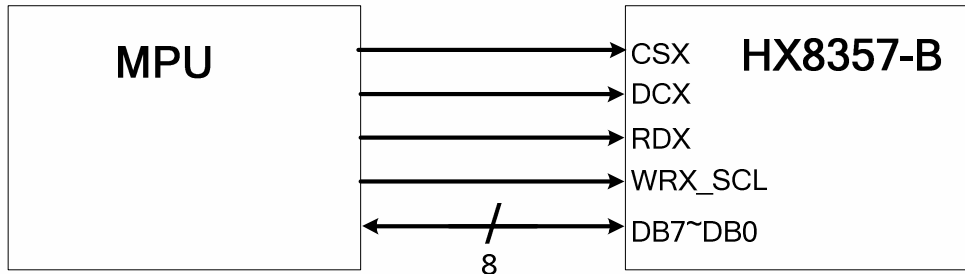


Figure 4.6: Example of DBI Type-B System 8-bit bus Interface

4.1.5 DBI Type-B Interface Data Color Coding

DBI Type-B Interface Data Color Coding for GRAM data **Write**

- DBI Type-B 8-Bits Bus Interface (IM2, IM1, IM0="011")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH
3'h5	X	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3-transfer)
		x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.3: DBI Type-B 8-Bits Interface GRAM Write Table

- DBI Type-B 9-Bits Bus Interface (IM2,IM1,IM0="001")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH	
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.4: DBI Type-B 9-Bits Interface GRAM Write Set Table

- DBI Type-B 16-Bits Bus Interface (IM2,IM1,IM0="010")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH	
3'h5	X	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1-pixels/ 1-transfer)
		x	x	R05	R04	R03	R02	R01	R00	x	x	G05	G04	G03	G02	G01	G00	x	x	
3'h6	0	x	x	B05	B04	B03	B02	B01	B00	x	x	R15	R14	R13	R12	R11	R10	x	x	262K-Color (2-pixels/ 3-transfer)
		x	x	G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	
	1	x	x	x	x	x	x	x	x	x	x	R05	R04	R03	R02	R01	R00	x	x	262K-Color (1-pixels/ 2-transfer)
		x	x	G05	G04	G03	G02	G01	G00	x	x	B05	B04	B03	B02	B01	B00	x	x	
		x	x	G15	G14	G13	G12	G11	G10	x	x	R15	R14	R13	R12	R11	R10	x	x	
				G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	

Table 4.5: DBI Type-B 16-Bits Interface GRAM Write Table

- DBI Type-B 18-Bits Bus Interface (IM2,IM1,IM0="000")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2CH	
3'h6	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1-pixels/ 1-transfer)

Table 4.6: DBI Type-B 18-Bits Interface GRAM Write Set Table

- DBI Type-B 16-Bits Data extend to 18-Bit

Register	GRAM Data																		
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h5	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

Table 4.7: DBI Type-B 16-Bits Data extend to 18-Bit

DBI Type-B Interface Data Color Coding for RAM data Read

- DBI Type-B 8-Bits Bus Interface (IM2, IM1, IM0="011")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH
3'h5	X	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3-transfer)
		x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
		x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 4.8: DBI Type-B 8-Bits Interface GRAM Read Table

- DBI Type-B 9-Bits Bus Interface (IM2, IM1, IM0="001")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH	
3'h6	X	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 4.9: DBI Type-B 9-Bits Interface GRAM Read Set Table

- DBI Type-B 16-Bits Bus Interface (IM2, IM1, IM0="010")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH	
3'h5	X	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1-pixels/ 1-transfer)
		x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	
3'h6	0	x	x	B5	B4	B3	B2	B1	B0	x	x	R15	R14	R13	R12	R11	R10	x	x	262K-Color (2-pixels/ 3-transfer)
		x	x	G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	
	1	x	x	G5	G4	G3	G2	G1	G0	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 2-transfer)
		x	x	x	x	x	x	x	x	x	x	R15	R14	R13	R12	R11	R10	x	x	
		x	x	G15	G14	G13	G12	G11	G10	x	x	B15	B14	B13	B12	B11	B10	x	x	

Table 4.10: DBI Type-B 16-Bits Interface GRAM Read Table

- DBI Type-B 18-Bits Bus Interface (IM2, IM1, IM0="000")

Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command	
Set_pixel_format	DFM	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2EH	
3'h6	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1-pixels/ 1-transfer)

Table 4.11: DBI Type-B 18-Bits Interface GRAM Read Set Table

4.2 Serial Data Transfer Interface (MIPI DBI Type-C)

The HX8357-B supports two type serial data transfer interface, the interface selection by setting IM2-0 pins, The IM2-0 set “101” is select 3 wire option1 serial bus. The IM2-0 is set “111” when select 4 wire option3 serial bus.

The 3 wire serial bus is use: chip select line (CSX), serial input/output data (SDA) and the serial transfer clock line (WRX_SCL).The 4 wire serial bus is use: chip select line (CSX), data/command select (DCX), serial input/output data (DIN_SDA, DOUT) and the serial transfer clock line (WRX_SCL).

4.2.1 Serial data write mode

The 3-Pin serial data packet contains a control bit DCX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal DCX is transferred by DCX pin. If DCX is low, the transmission byte is command byte. If DCX is high, the transmission byte is stored in to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (DIN_SDA) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

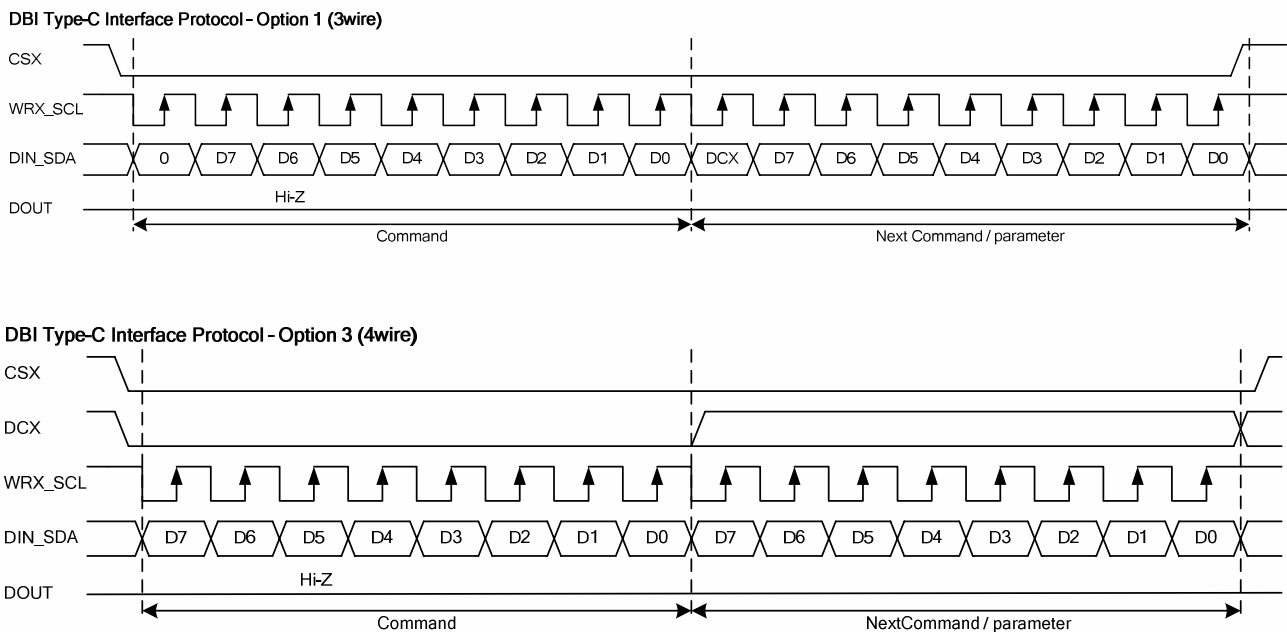


Figure 4.7: DBI Type-C -- Serial Interface protocol 3 wire/4 wire, write mode

4.2.2 Serial data read mode

The micro-controller first has to send a command and then the following byte is transmitted in the opposite direction. The 3-wire serial read data format which just needs 8-bit.

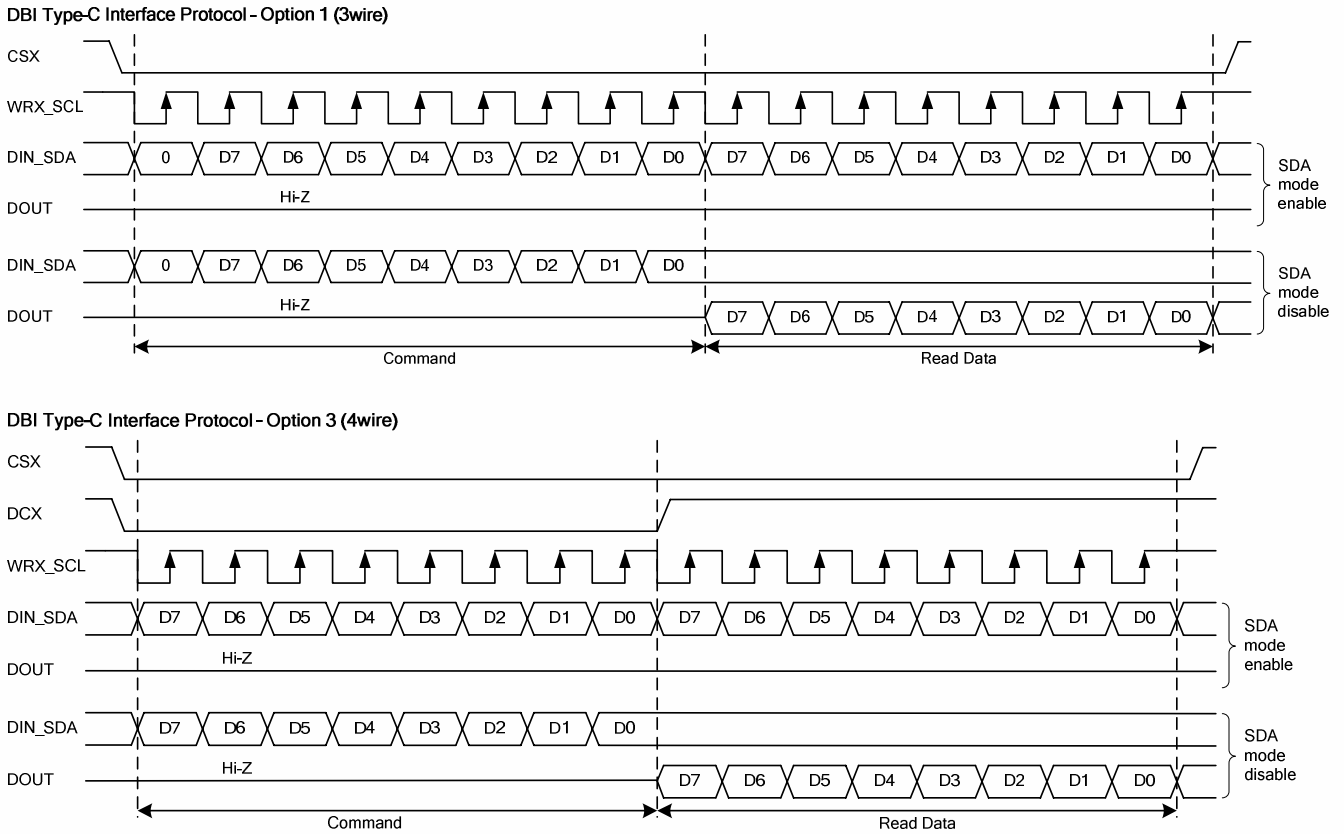


Figure 4.8: Type-C -- Serial Interface protocol 3 wire/4 wire read mode

4.2.3 DBI Type-C Interface Data Color Coding

- DBI Type-C 3/4-wire serial bus Interface (IM2, IM1, IM0="101" or "111")

Register		D7	D6	D5	D4	D3	D2	D1	D0	Command
Set_pixel_format	DFM	0	0	1	0	1	1	0	0	2CH
3'h1	0	X	X	R00	G00	B00	R10	G10	B10	8-Color (1-pixels/ 1-transfer)
	1	X	R00	G00	B00	X	R10	G10	B10	
3'h6	X	R5	R4	R3	R2	R1	R0	X	X	262K-Color (1-pixels/ 3-transfer)
		G5	G4	G3	G2	G1	G0	X	X	
		B5	B4	B3	B2	B1	B0	X	X	

Table 4.12: DBI Type-C Interface GRAM write Table

- DBI TYPE-C 3-Bits Data extend to 18-Bit

Register		GRAM Data																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h1	XX	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0

Table 4.13: DBI Type-C 3-Bits Data extend to 18-Bit

4.2.4 Break and Pause Sequences

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

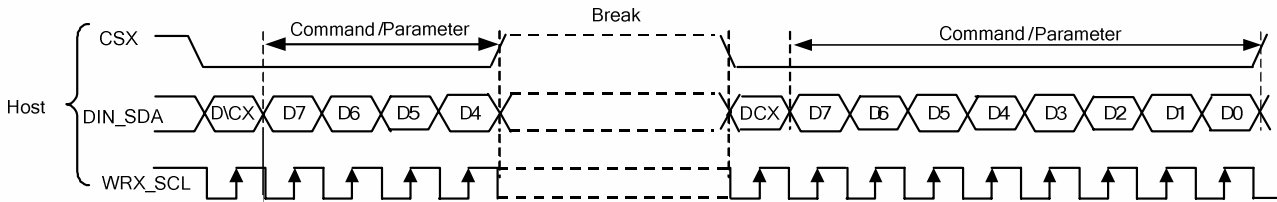


Figure 4.9: Display Module Data Transfer Recovery

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

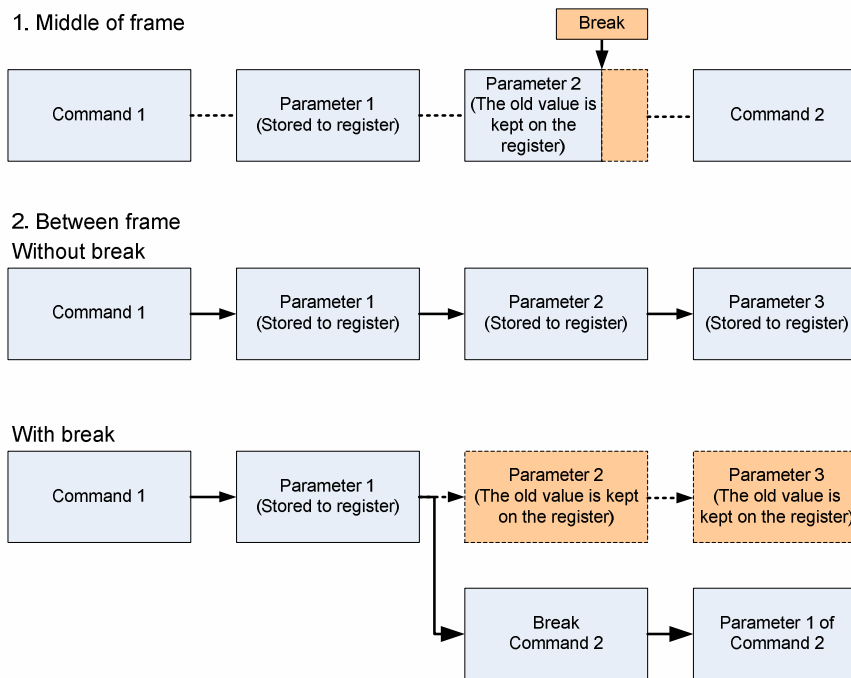


Figure 4.10: Break during parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

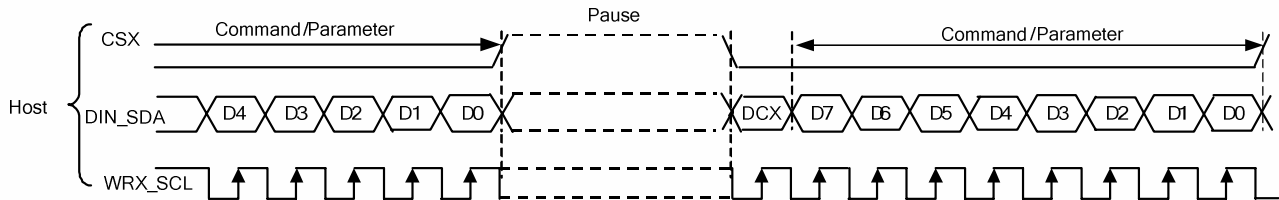


Figure 4.11: Display Module Data Transfer Pause

There are 4 cases where there is possible to see this kind of pause:

- Command – Pause – Command
- Command – Pause – Parameter
- Parameter – Pause – Command
- Parameter – Pause – Parameter

4.3 MIPI DPI interface (Display Pixel Interface)

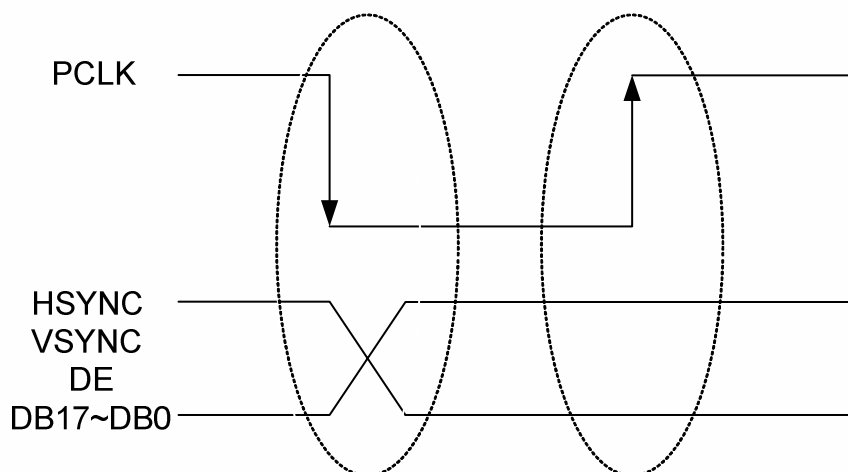
The HX8357-B uses 16 or 18-bit parallel RGB interface which includes: HSYNC, VSYNC, DE, PCLK, DB17~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB17~DB0 –lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display.

This is negative ('-', '0', low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame.

This is negative ('-', '0', low) active and its state is read to the display module by a rising edge of the PCLK-line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display.

This is positive ('+', '1', high) active and its state is read to the display module by a rising edge of the PCLK-line. DB17~DB0 (18 bit: R5-R0, G5-G0 and B5-B0; 16 bit: R4- R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (when DE =1 and there is a rising edge of PCLK). DB17~DB0 – lines can be set to "0" (low) or "1" (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).

Figure 4.12: PCLK cycle

General Timing Diagram

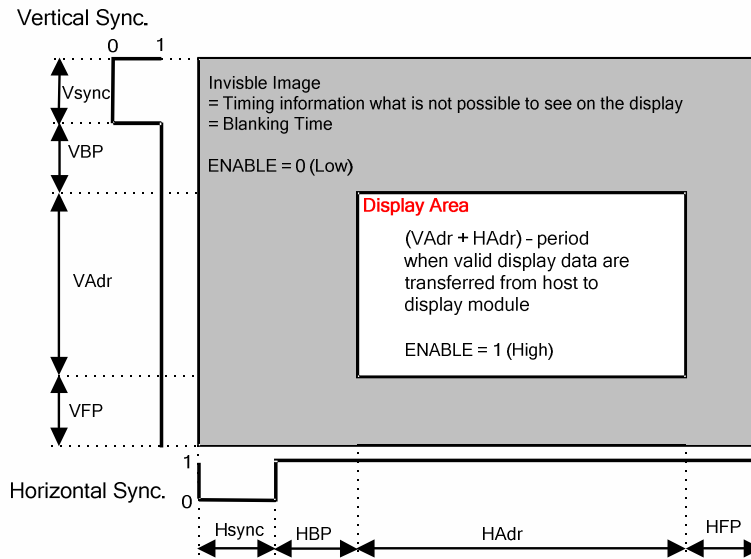


Figure 4.13: General Timing Diagram

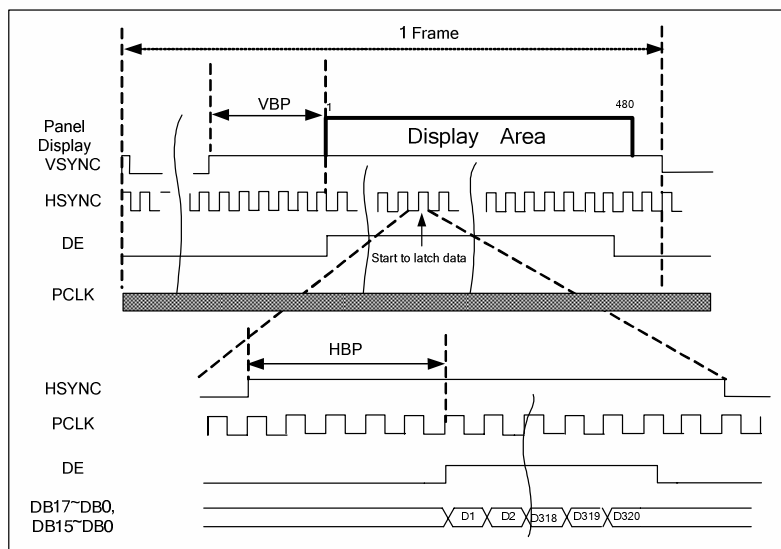


Figure 4.14: DPI (320RGBx480) timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

The MIPI DPI interface includes two types which are 16-/18-bit data format by register 3Ah (set_pixel_format) to select.

4.3.1 16 bit/pixel Color Order on the DPI I/F

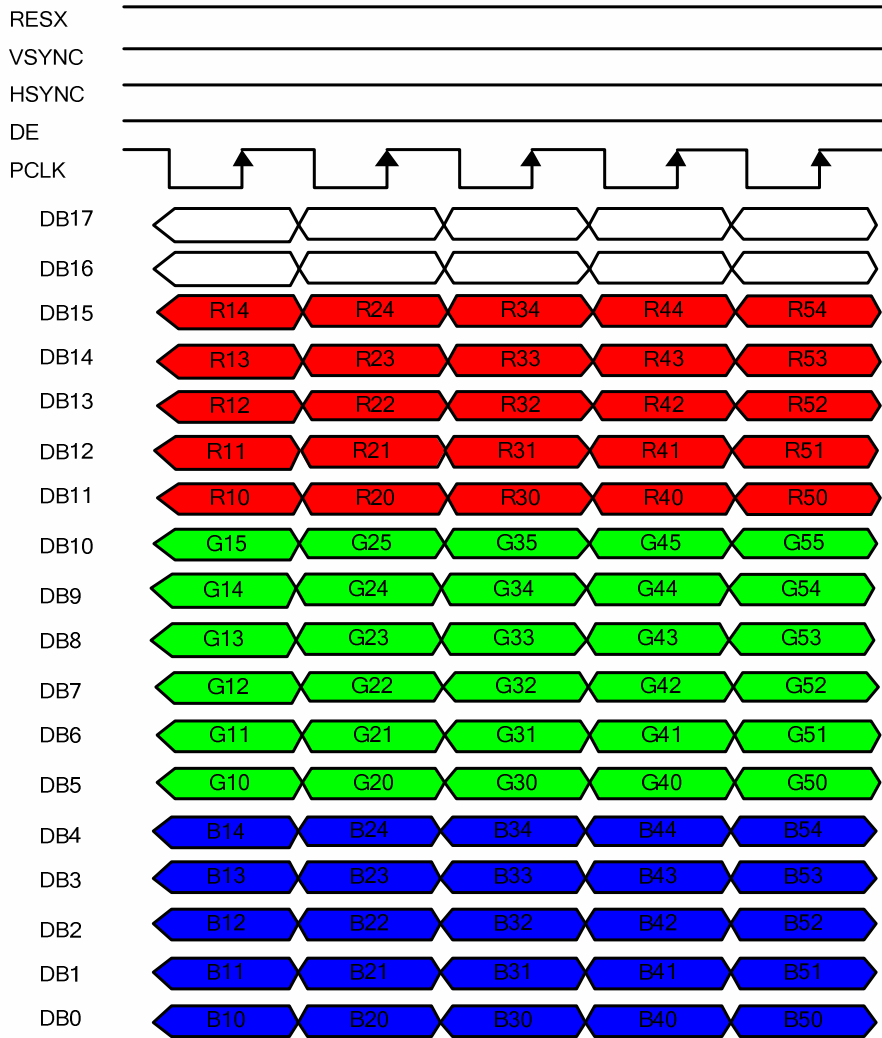


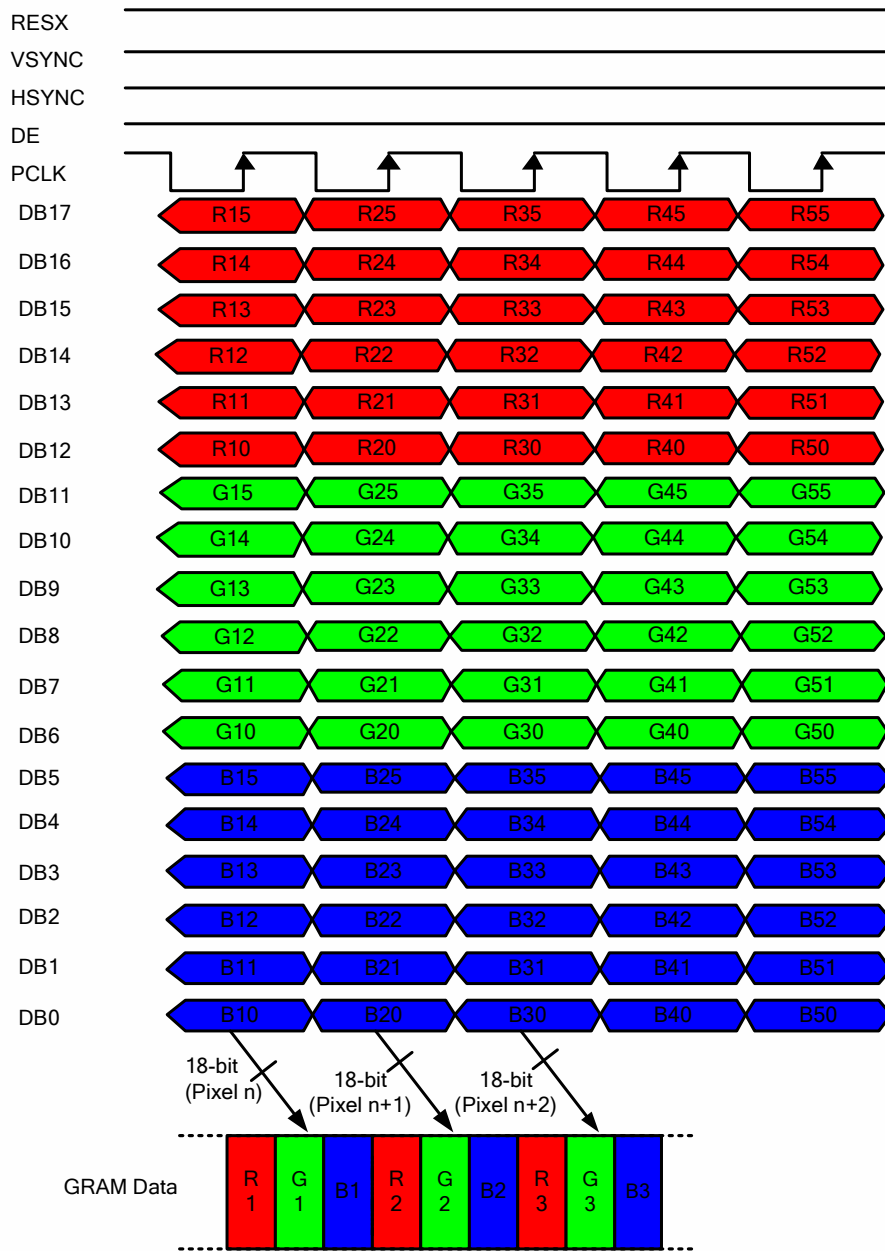
Figure 4.15: 16 bit/pixel 65k Color Order on the DPI I/F

- DPI 16-Bits Data extend to 18-Bit

Register		GRAM Data / Display data																	
Set_pixel format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3'h5	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

Table 4.14: DPI 16-Bits Data extend to 18-Bit

4.3.2 18 bit/pixel Color Order on the DPI I/F



Note: The Data order is as follows, MSB = DB17, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.16: 18 bit/pixel -- 262k Color Order on the DPI I/F

4.3.3 Shutdown and Color Mode Signals

The HX8357-B is support hardware pin control function on DPI interface. If use this function, some OTP data need program for display quality, example Gamma setting, VCOM setting and Power voltage setting.

4.3.3.1 Shutdown for DPI interface hardware control

The Shutdown signal, SD, is used to turn on or turn off the display module. When SD is asserted high, the host processor should stop the video stream data to the display module to reduce interface signal power consumption.

PCLK may also be turned off to further reduce power consumption. The display module may reduce its power consumption by switching off its internal circuits. The control interface shall remain powered on.

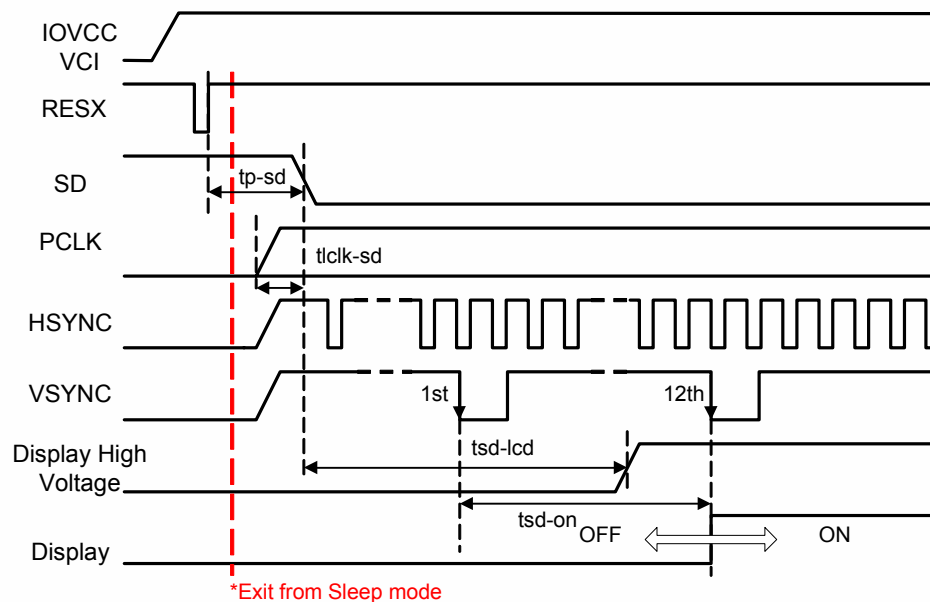


Figure 4.17: Power on and Shutdown Recovery Sequence

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RESX off to falling edge of SD	tp-sd	-	5	-	-	ms
PCLK input to the falling edge of SD	tclk-sd	-	1	-	-	PCLK
Falling edge of SD to display start	tsd-on	-	-	12	-	Vertical period

Table 4.15: AC timing for power-on sequence and recovery sequence from shutdown

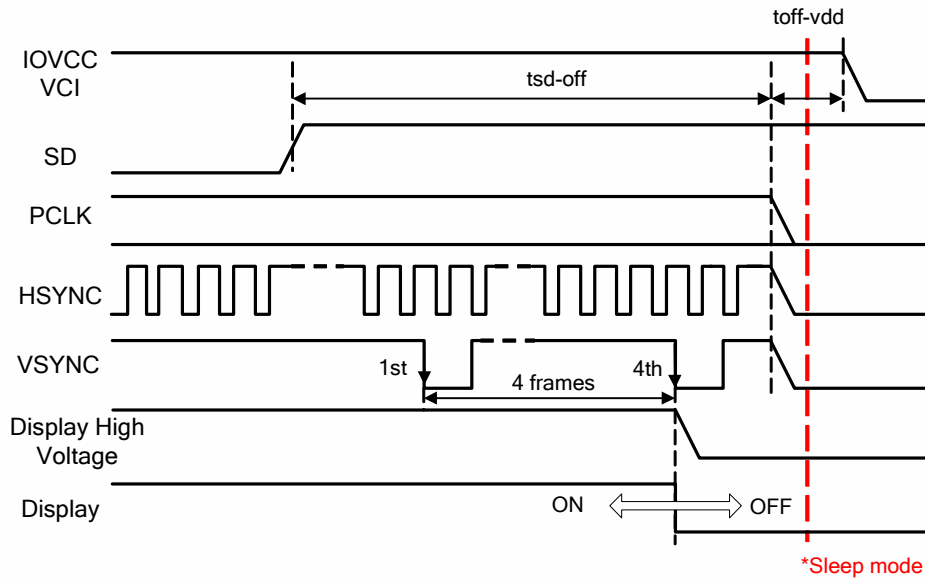


Figure 4.18: Power off and Shutdown Sequence

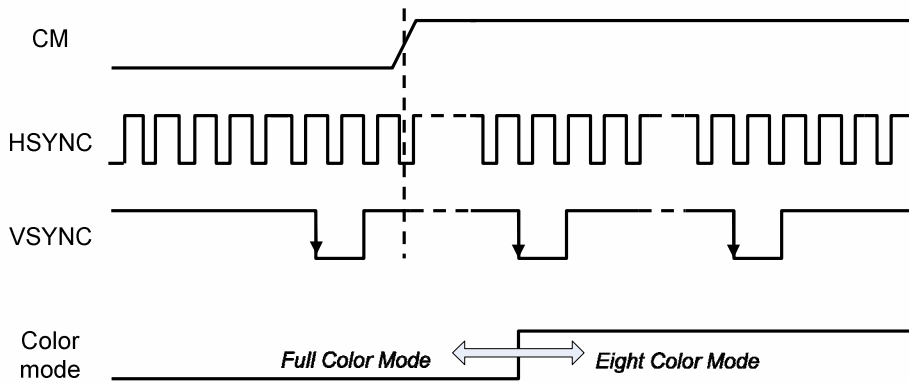
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Rising edge of SD to display off	tsd-off	-	4	-	-	Vertical period
Input-signal-off to IOVCC/VCI off	toff-vdd	-	0	-	-	s

Table 4.16: AC timing for power-off sequence and shutdown sequence

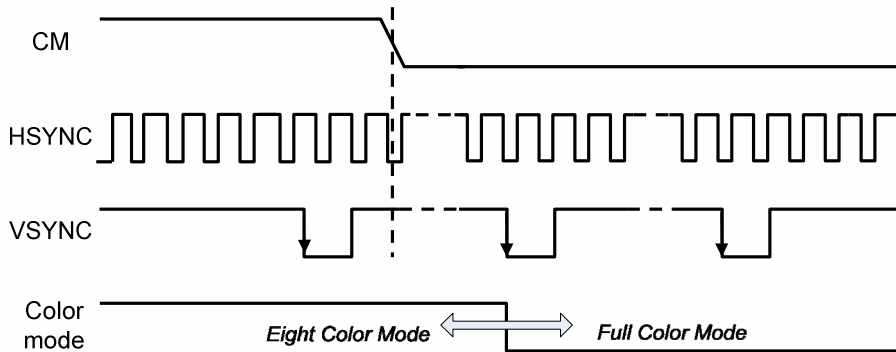
Color mode for DPI interface hardware control

The Color Mode signal, CM, is used to change the displayed number of colors. When CM is asserted high, the display module shall show the image data using eight colors, MSB for each R, G, and B color components. All unnecessary circuits on the display module may be stopped at the same time to reduce display module power consumption.

Transition from full-color mode to 8-color mode shall occur on the VSYNC following a low-to-high transition on CM.

**Figure 4.19: Full-color to 8-color Mode Transition Sequence**

Transition from 8-color mode to full-color mode shall occur on the Vsync following a high-to-low transition on CM.

**Figure 4.20: 8-color to Full-color Mode Transition Sequence**

5. Function Description

5.1 Display Data GRAM

The display data RAM stores display dots and consists of 2,764,800 bits (320x18x480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

5.1.1 Address Counter (AC)

The HX8357-B contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

MX	MY	MV	X Range	Y Range	Panel Resolution
X	X	0	0~319d	0~479d	320RGB x480 dot
		1	0~479d	0~319d	

Table 5.1: Addresses Counter Range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.1.2 MCU to Memory Write/Read Direction

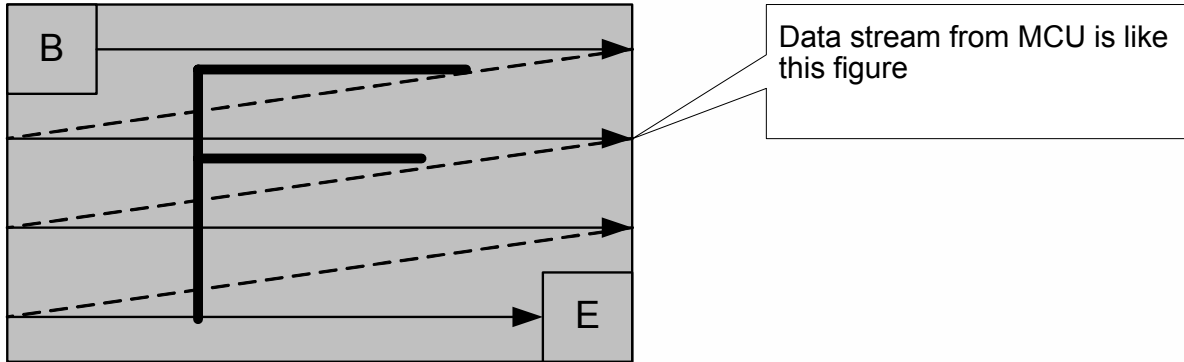


Figure 5.1: MCU to Memory Write/Read Direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

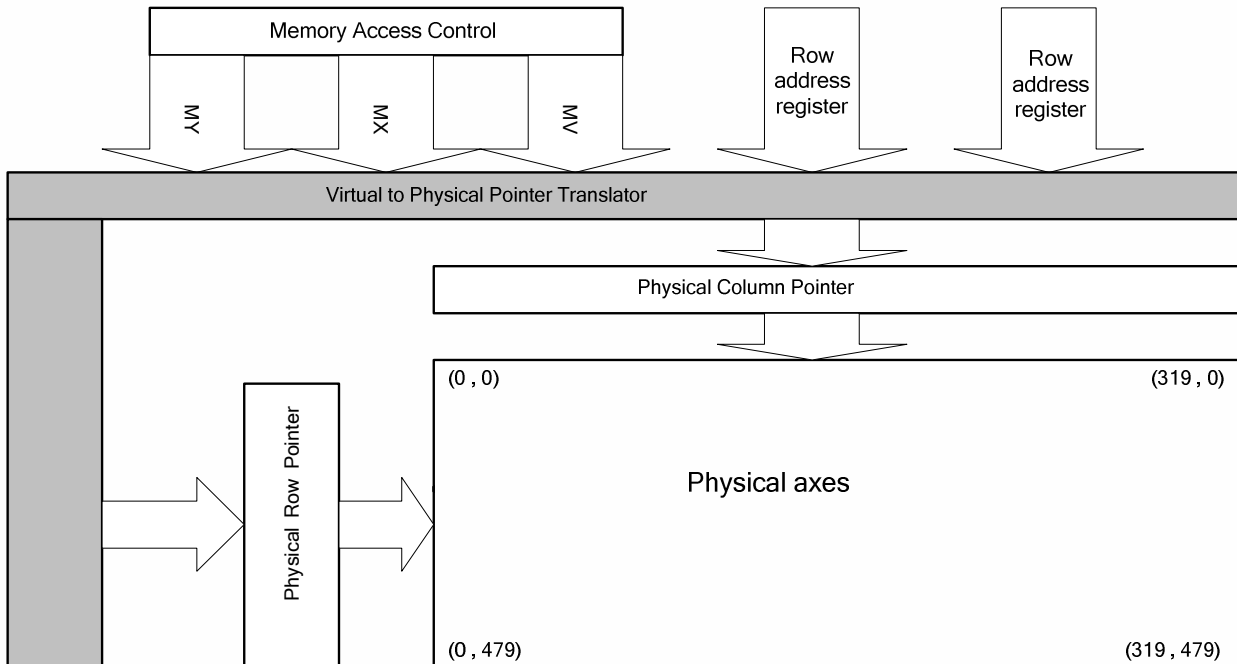


Figure 5.2: MY, MX, MV Setting of GRAM control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Row Pointer) with SC
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Row Pointer)	Direct to (319-Physical Column Pointer)

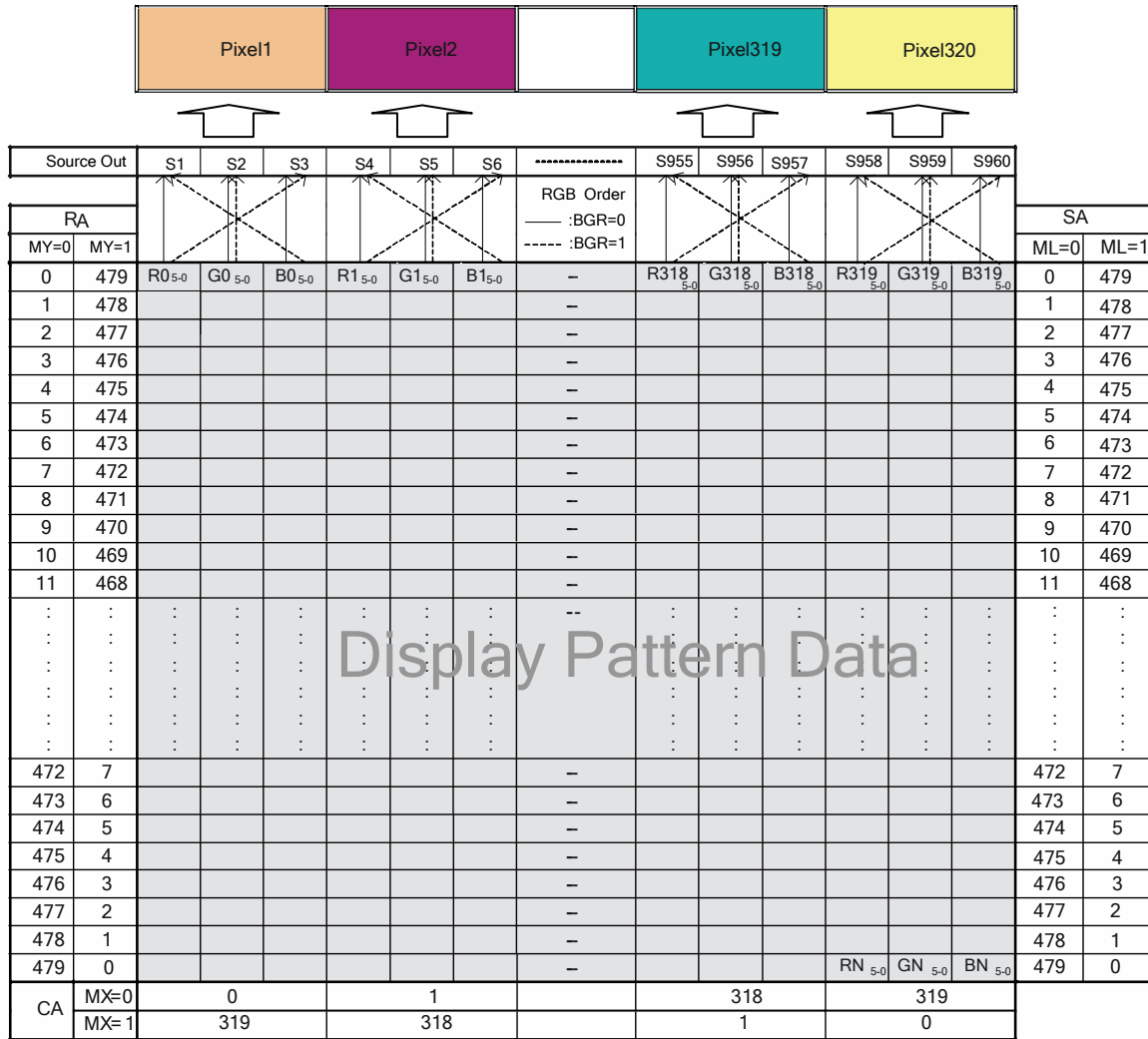
Table 5.2: MY, MX, MV Setting of GRAM address mapping

The following figure depicts the update method set by MV, MX and MY bit.

Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5.3: Address Direction Settings

5.1.3 Source, Gate and Memory Map



Note: RA = Row Address.
 CA = Column Address.
 SA = Scan Address.
 MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control (R36h) command
 MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control (R36h) command
 ML = Scan direction parameter, D4 parameter of Memory Access Control (R36h) command
 BGR = Red, Green and Blue pixel position change, D3 parameter of Memory Access Control (R36h) command

Figure 5.4: Memory Map - 320RGBx480 dot

5.1.4 Fully Display, Partial Display, Vertical Scrolling Display

5.1.4.1 Fully Display

- Example: (1) 320RGBx480 dot display mode.
 (2) NORON (Normal Display Mode On) instruction (R13h).
 (3) SC=0x000h, EC=0x13Fh (R2Ah) and SP=0x000h, EP=0x1DFh (R2Bh), ML=0.

GRAM	00h	01h	-----	13Eh	13Fh
	DB---DB 17 --- 0	DB---DB 17 --- 0	-----	DB---DB 17 --- 0	DB---DB 17 --- 0
00h	000000H	000001H	-----	00013EH	00013FH
001h	001000H	001001H	-----	00113EH	00113FH
002h	002000H	002001H	-----	00213EH	00213FH
003h	003000H	003001H	-----	00313EH	00313FH
004h	004000H	004001H	-----	00413EH	00413FH
005h	005000H	005001H	-----	00513EH	00513FH
⋮	⋮	⋮	-----	⋮	⋮
1DAh	1DA000H	1DA001H	-----	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	-----	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	-----	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	-----	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	-----	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	-----	1DF13EH	1DF13FH

Table 5.3: Memory map of full display

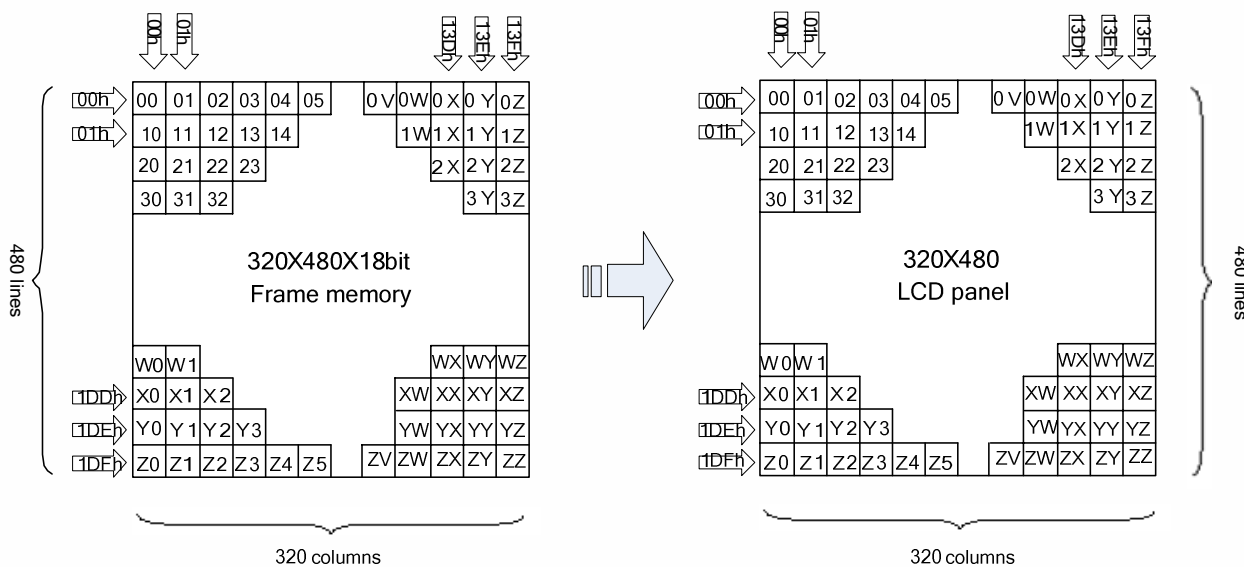


Figure 5.5: Memory map of full display

5.1.4.2 Partial Display

- Example: (1) 320RGBx480 dot display mode.
 (2) PLTON instruction (R12h).
 (3) SR[15:0]=0002h, ER[15:0]=01DBh, ML=0.

GRAM	00h	01h	-----	13Eh	13Fh
	DB---DB 17 --- 0	DB---DB 17 --- 0	-----	DB---DB 17 --- 0	DB---DB 17 --- 0
000h	000000H	000001H	-----	00013EH	00013FH
001h	001000H	001001H	-----	00113EH	00113FH
002h	002000H	002001H	-----	00213EH	00213FH
003h	003000H	003001H	-----	00313EH	00313FH
004h	004000H	004001H	-----	00413EH	00413FH
005h	005000H	005001H	-----	00513EH	00513FH
⋮	⋮	⋮	-----	⋮	⋮
1DAh	1DA000H	1DA001H	-----	1DA13EH	1DA13FH
1DBh	1DB000H	1DB001H	-----	1DB13EH	1DB13FH
1DCh	1DC000H	1DC001H	-----	1DC13EH	1DC13FH
1DDh	1DD000H	1DD001H	-----	1DD13EH	1DD13FH
1DEh	1DE000H	1DE001H	-----	1DE13EH	1DE13FH
1DFh	1DF000H	1DF001H	-----	1DF13EH	1DF13FH

LCD panel S/G pins	Pixel 1	Pixel 2	-----	Pixel319	Pixel320		
	Non-display area	G1	000000H	000001H	-----	00013EH	00013FH
G2		001000H	001001H	-----	00113EH	00113FH	
G3		002000H	002001H	-----	00213EH	00213FH	
G4		003000H	003001H	-----	00313EH	00313FH	
G5		004000H	004001H	-----	00413EH	00413FH	
G6		005000H	005001H	-----	00513EH	00513FH	
Display area -> 234 lines	⋮	⋮	⋮	-----	⋮	⋮	
	G475	1DA000H	1DA001H	-----	1DA13EH	1DA13FH	
	G476	1DB000H	1DB001H	-----	1DB13EH	1DB13FH	
	G477	1DC000H	1DC001H	-----	1DC13EH	1DC13FH	
	G478	1DD000H	1DD001H	-----	1DD13EH	1DD13FH	
	G479	1DE000H	1DE001H	-----	1DE13EH	1DE13FH	
	G480	1DF000H	1DF001H	-----	1DF13EH	1DF13FH	
	Non-display area	⋮	⋮	⋮	-----	⋮	⋮

Table 5.4: Memory map of partial display

5.1.4.3 Vertical Scrolling Display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

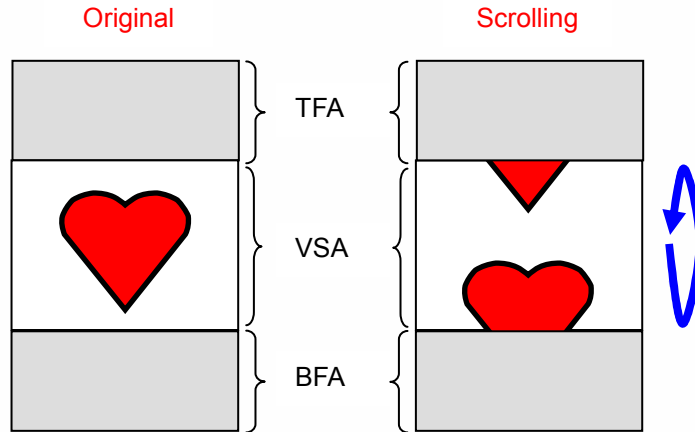


Figure 5.6: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

- Example 1: (1) 320RGBx480 dot display mode.
 (2) TFA=2, VSA=478, BFA=0 when MADCTL B4=0
 (3) VSCRSADD=03h

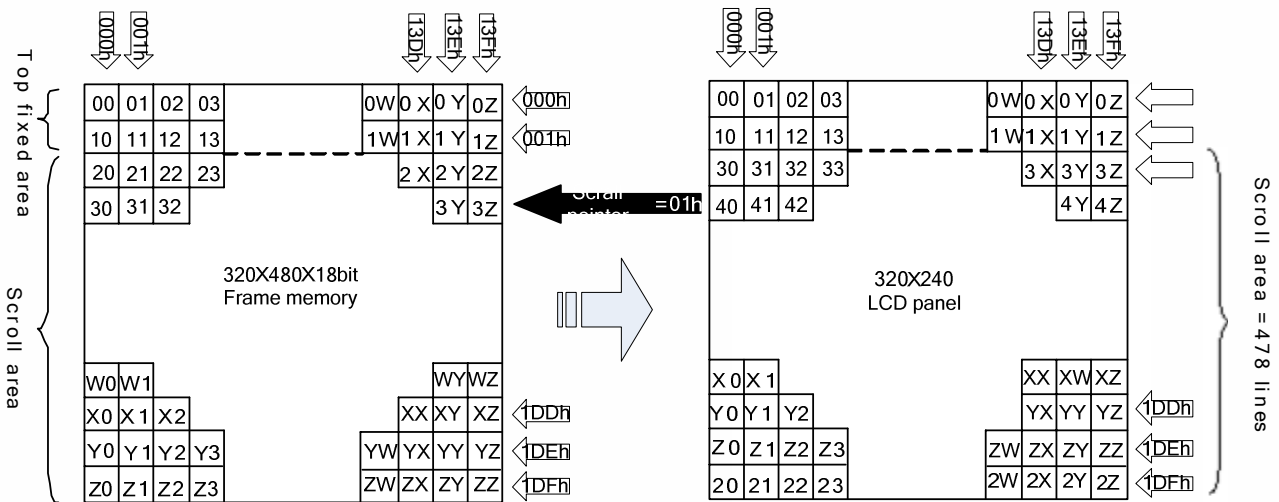


Figure 5.7: Memory map of vertical scrolling example 1

- Example 2: (1) 320RGBx480 dot display mode.
 (2) TFA=2, VSA=476, BFA=2 when MADCTL B4=0
 (3) VSCRSADD=03h

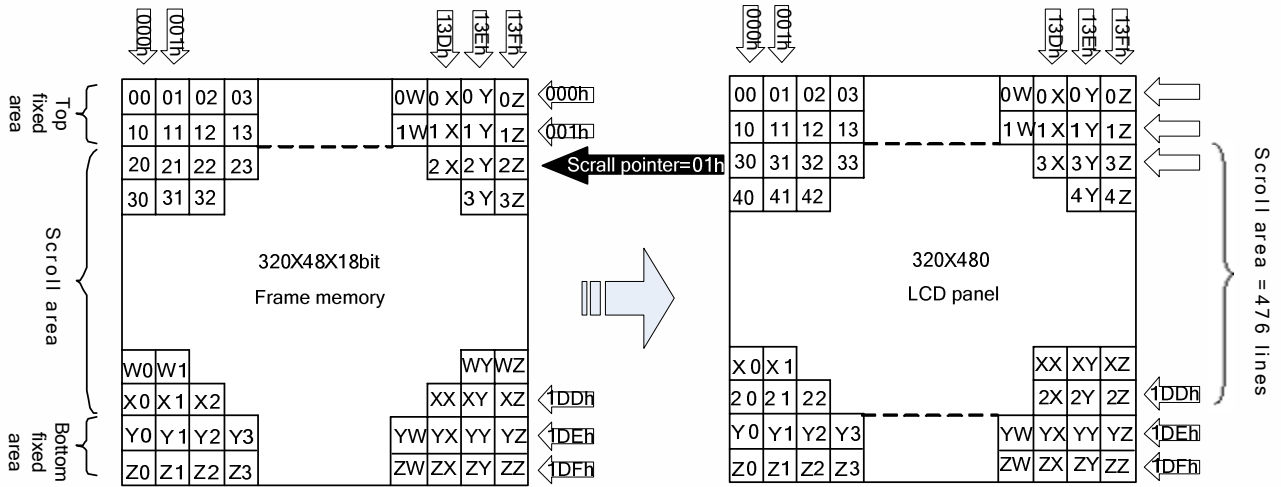


Figure 5.8: Memory map of vertical scrolling example 2

- Example 3: (1) 320RGBx480 dot display mode.
 (2) TFA=2, VSA=476, BFA=2 when MADCTL B4=0
 (3) VSCRSADD=04h

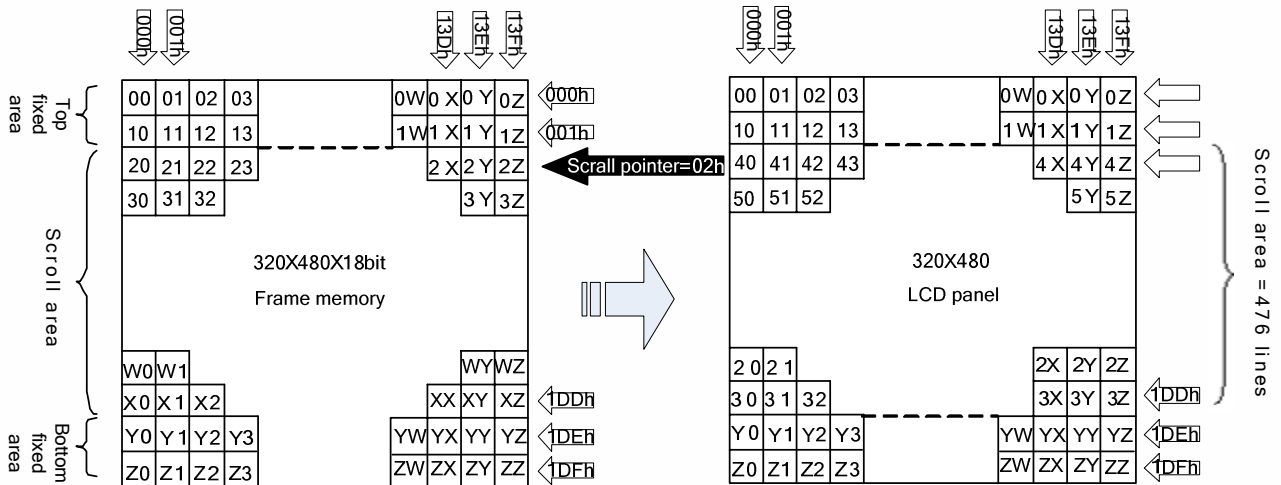


Figure 5.9: Memory map of vertical scrolling example 3

Vertical Scroll Example

There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: $TFA + VSA + BFA \neq$ Panel scan lines

N/A. Do not set $TFA + VSA + BFA \neq$ Panel scan lines. In that case, unexpected picture will be shown.

Case 2: $TFA + VSA + BFA =$ Panel scan lines (Scrolling)

Example 1: (1) 320RGBx480 dot display mode.

(2) When $TFA=0, VSA=480, BFA=0$ and $VSCRSADD=40$. MADCTL parameter $B4="0"$

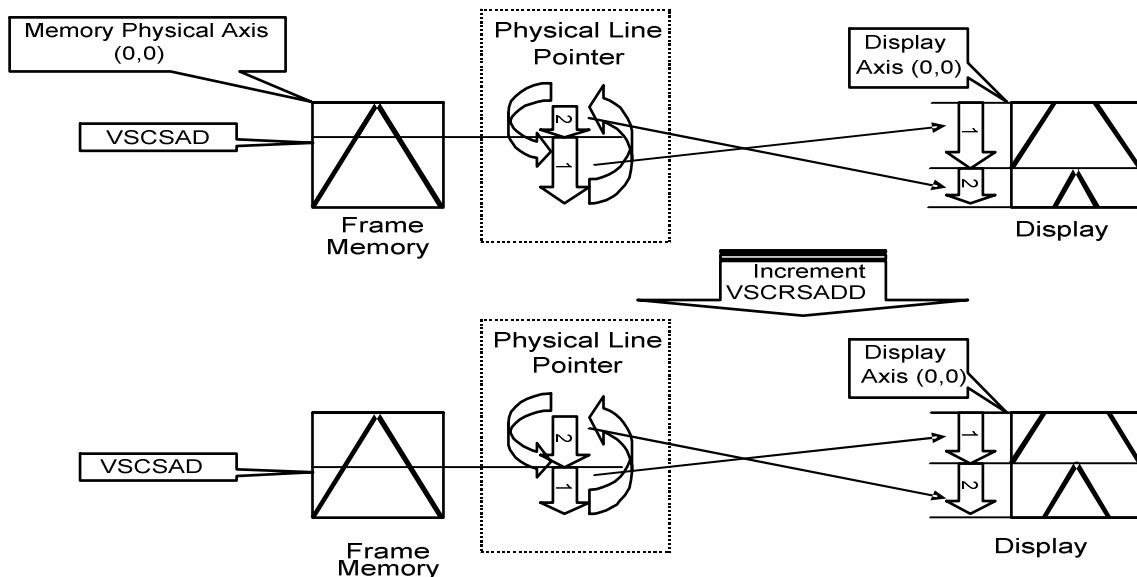


Figure 5.10: Display of Vertical Scroll Example 1

Example 2: (1) 320RGBx480 dot display mode.
 (2) TFA=60, VSA=420, BFA=0 and VSCRSADD =160. MADCTRL parameter B4="1"

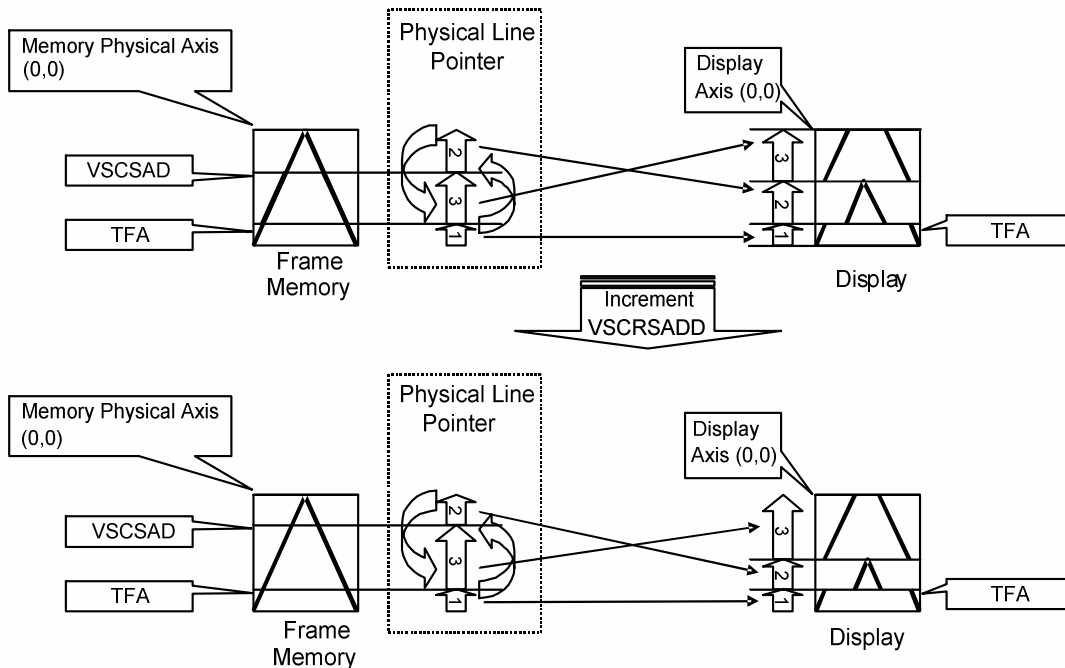


Figure 5.11: Display of Vertical Scroll Example 2

5.2 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

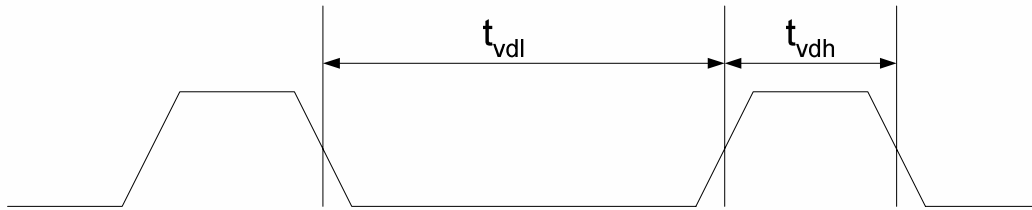


Figure 5.12: Tearing Effect Output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdI= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.

Ex: 1. TSEL[15:0]=0, then TE signal will output after last Line finished.

TSEL[15:0]=2, then TE signal will output at second Line start.

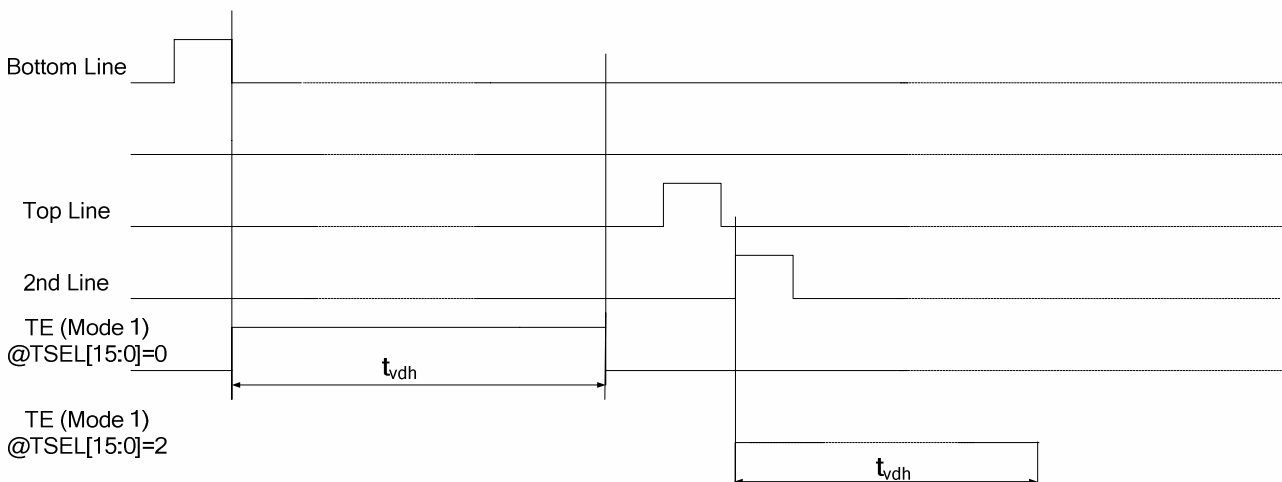


Figure 5.13: TE Delay Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.

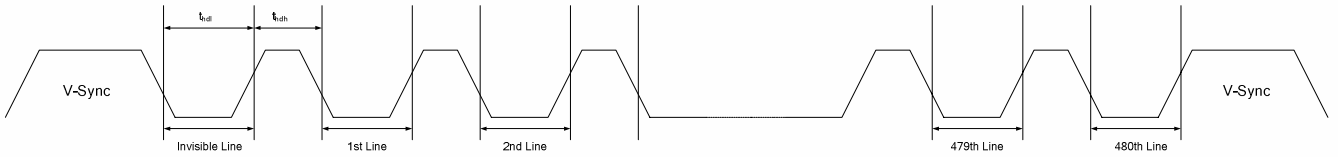


Figure 5.14: Tearing Effect Output signal mode 2

t_{dh}= The LCD display is not updated from the Frame Memory

t_{dl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Under Mode2, the H-sync pulse output amount will be defined by TSEL[15:0] setting.

Ex: TSEL[15:0]=0, then TE signal will output 480 H-sync.

TSEL[15:0]=1, then TE signal will output 480 H-sync.

TSEL[15:0]=2, then TE signal will output 479 H-sync.

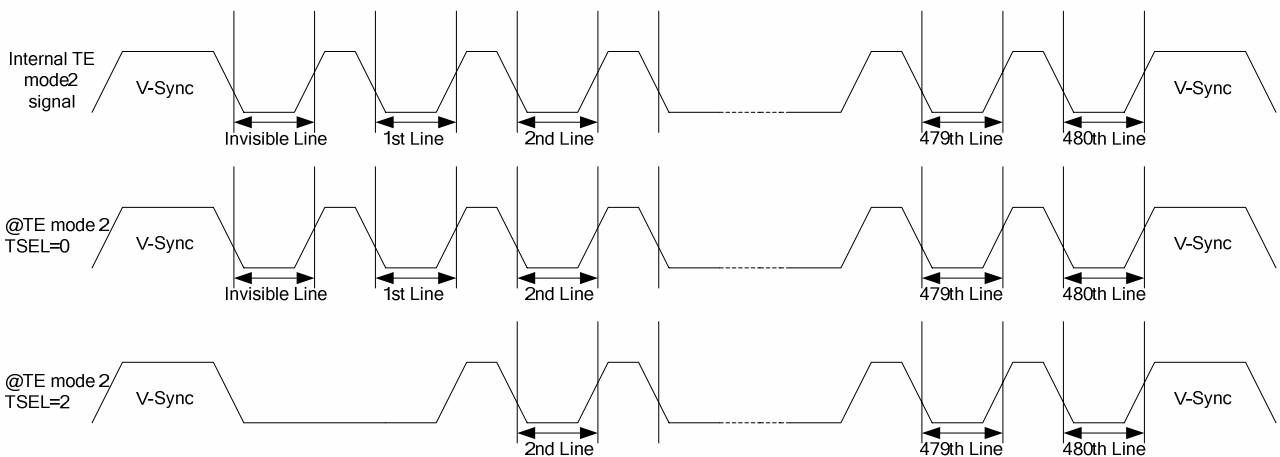
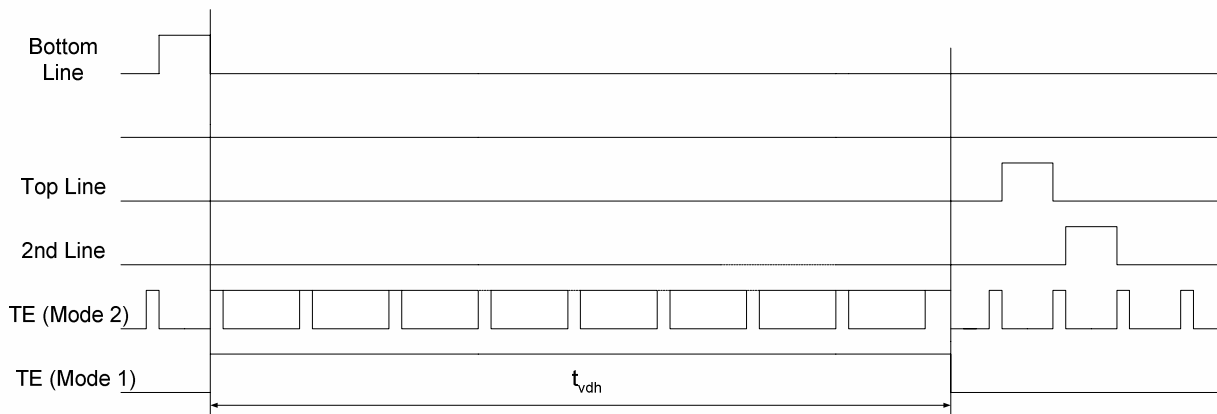


Figure 5.15: TE Output for TELINE setting



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 5.16: Tearing Effect Output signal

5.2.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

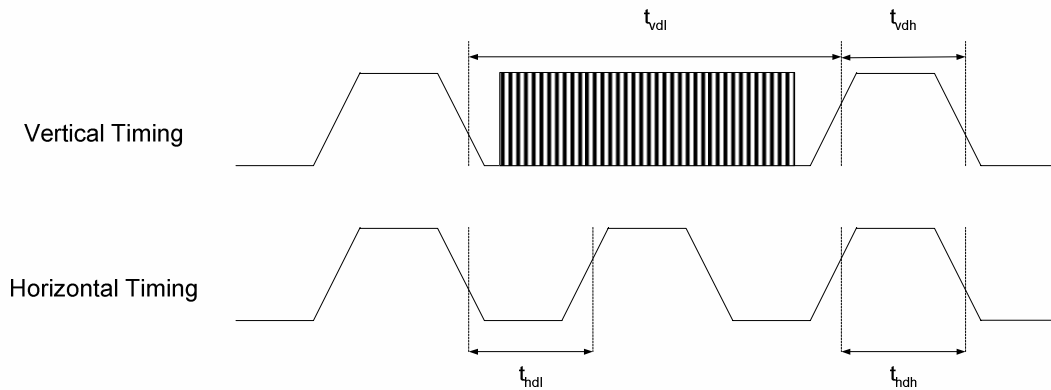


Figure 5.17: Tearing Effect Line Timing

Idle Mode Off (Frame Rate = TBDHz)

Symbol	Parameter	Min.	Max.	Unit	description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: The timings in Table 5.5 apply when MADCTL ML=0 and ML=1

Table 5.5: AC characteristics of Tearing Effect Signal

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

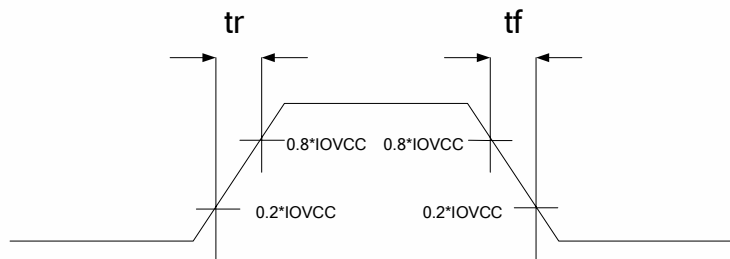


Figure 5.18: Rise and fall times of TE signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

Example 1: MPU's Write is faster than Panel's Read.

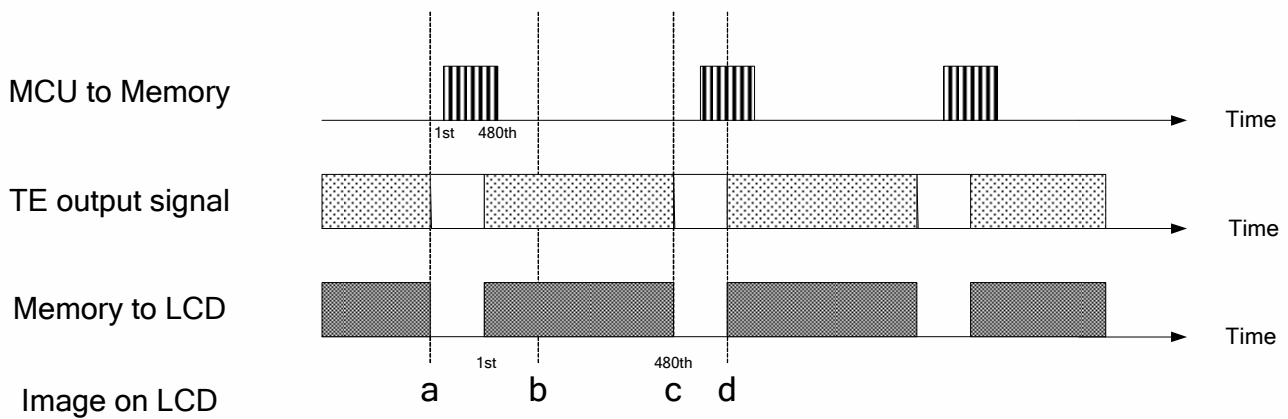


Figure 5.19: Tearing Effect - Example 1-1

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

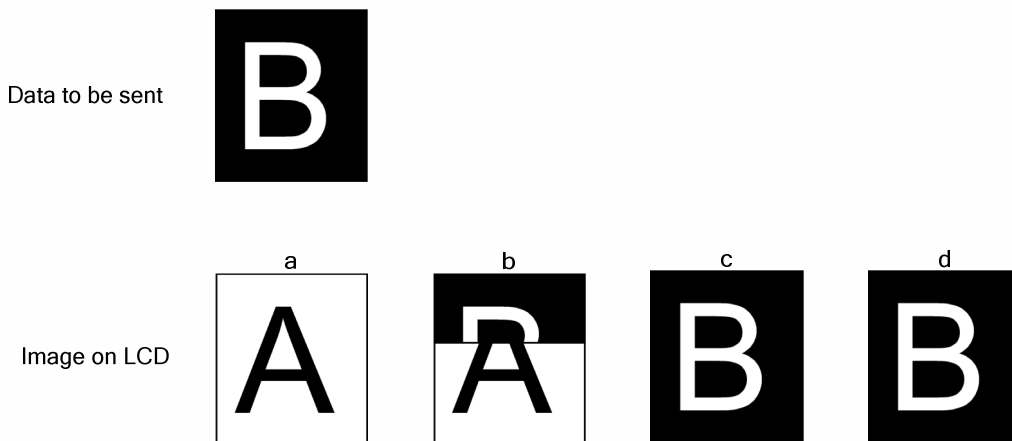


Figure 5.20: Tearing Effect - Example 1-2

Example 2: MPU's Write is slower than Panel's Read.

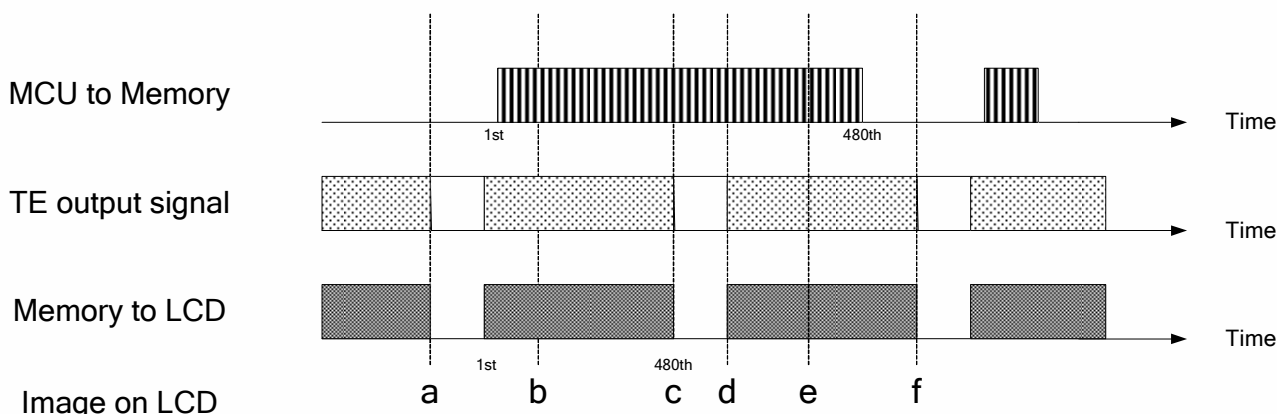


Figure 5.21: Tearing Effect - Example 2-1

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

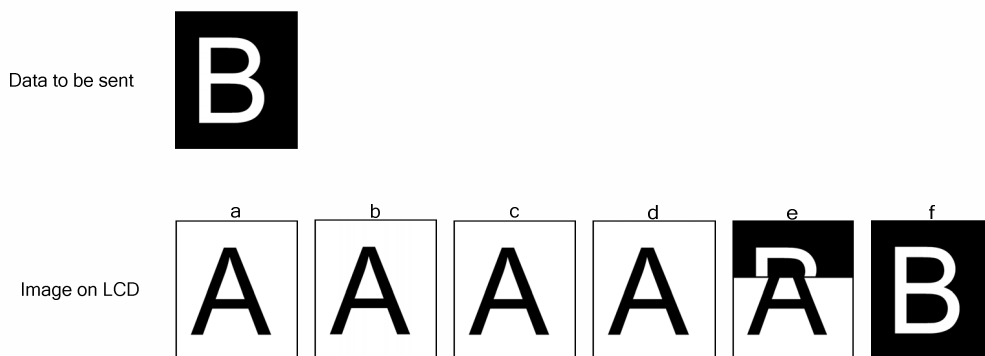


Figure 5.22: Tearing Effect - Example 2-2

5.3 Oscillator

The HX8357-B can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to Set OSC control register (RC5h). The default frequency is 5.2MHz.

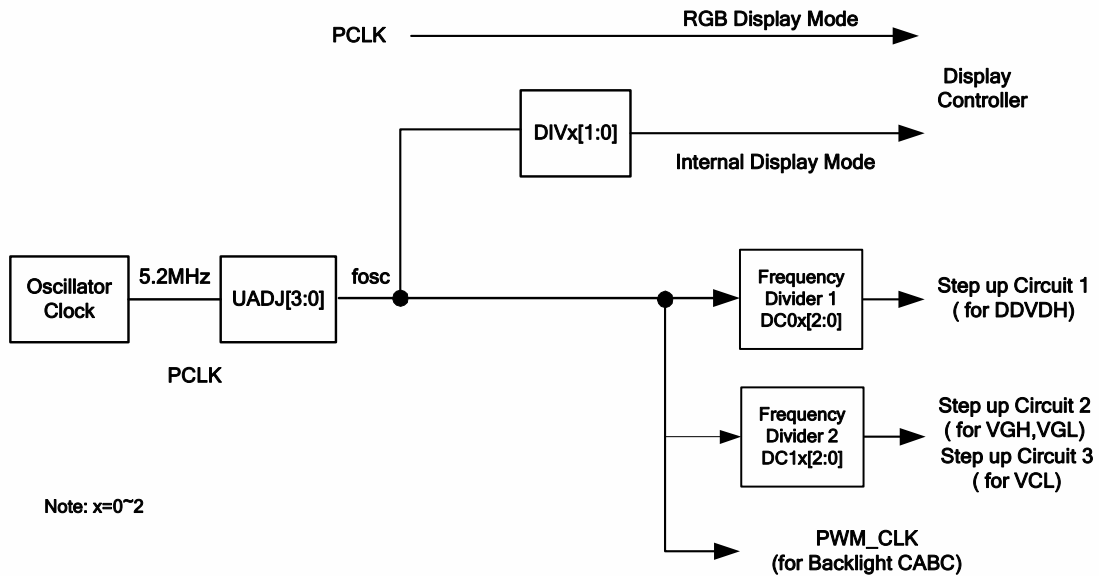


Figure 5.23: Oscillation Circuit

5.4 Source Driver

The HX8357-B contains a 960 channels of source driver (S1~S960) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 960 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.5 Gate Driver

The HX8357-B contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.6 LCD Power Generation Circuit

5.6.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

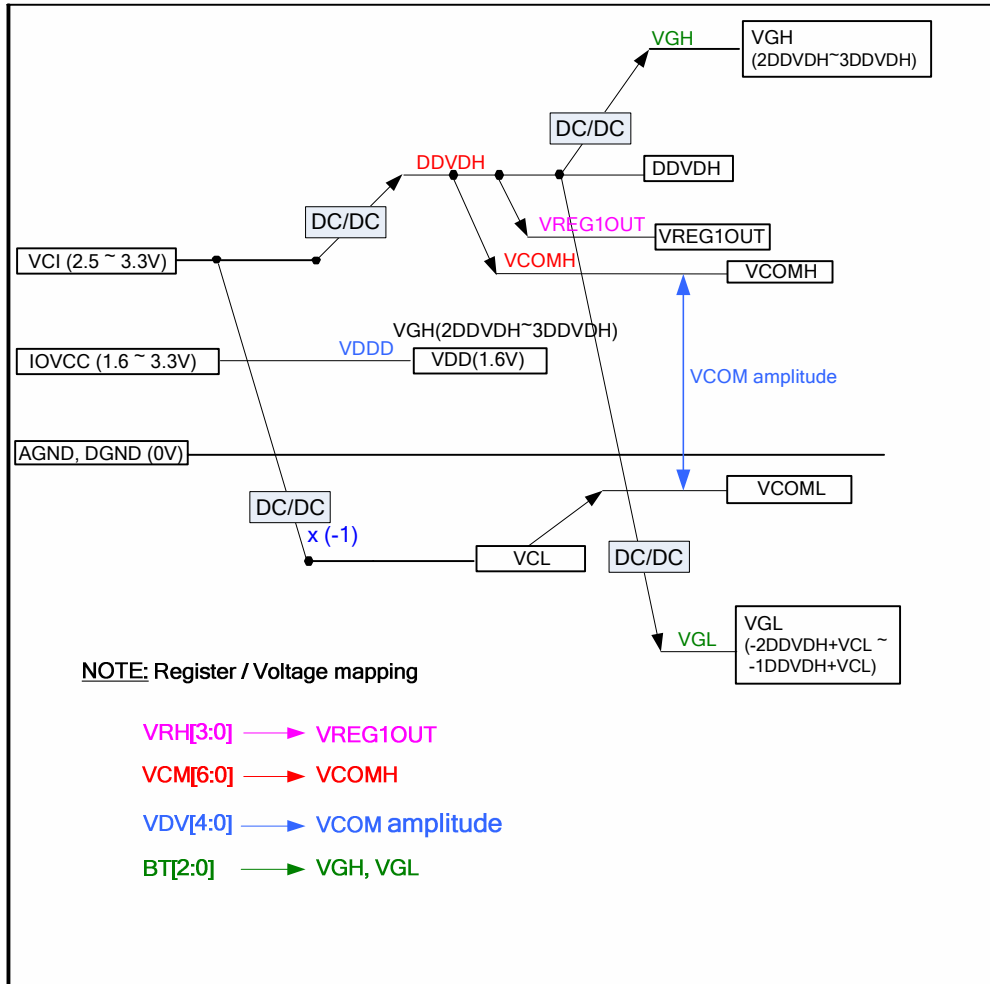


Figure 5.24: LCD Power Generation Scheme

5.6.2 Various Boosting Steps

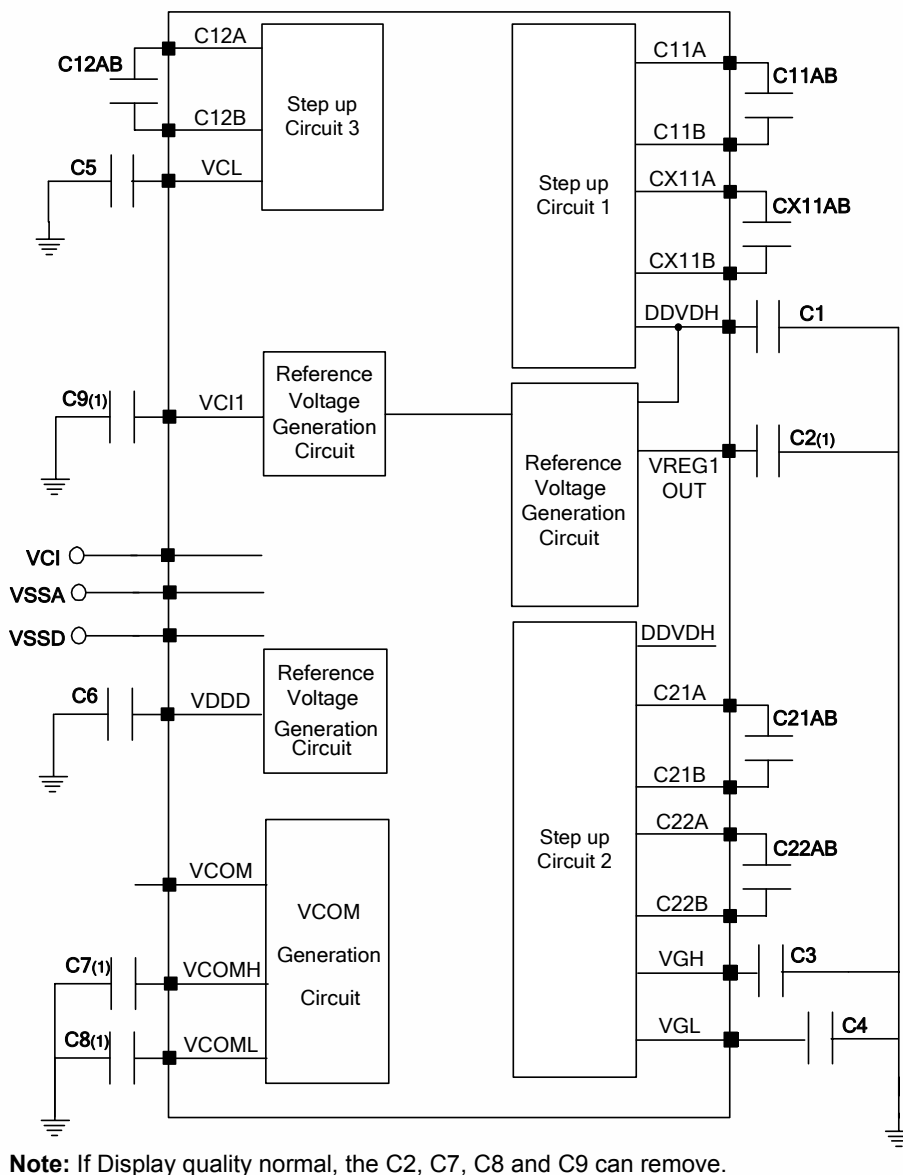


Figure 5.25: Various Boosting Steps

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity	Note
C1 (DDVDH)	10V	1 μ F (B characteristics)	-
C2 (VREG1OUT)	10V	1 μ F (B characteristics)	(1)
C3 (VGH)	25V	1 μ F (B characteristics)	-
C4 (VGL)	16V	1 μ F (B characteristics)	-
C5 (VCL)	6V	1 μ F (B characteristics)	-
C6(VDD)	6V	1 μ F (B characteristics)	-
C7 (VCOMH)	10V	1 μ F (B characteristics)	(1)
C8(VCOML)	6V	1 μ F (B characteristics)	(1)
C9(VCI1)	6V	1 μ F (B characteristics)	(1)
C11AB (C11A/B)	6V	1 μ F (B characteristics)	-
CX11AB (CX11A/B)	6V	1 μ F (B characteristics)	-
C12AB (C12A/B)	6V	1 μ F (B characteristics)	-
C21AB (C21A/B)	10V	1 μ F (B characteristics)	-
C22AB (C22A/B)	10V	1 μ F (B characteristics)	-

Note: If Display quality normal, the C2, C7, C8 and C9 can remove.

Table 5.6: The adoptability of Capacitor

5.7 Gamma Characteristic Correction Function

The HX8357-B incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

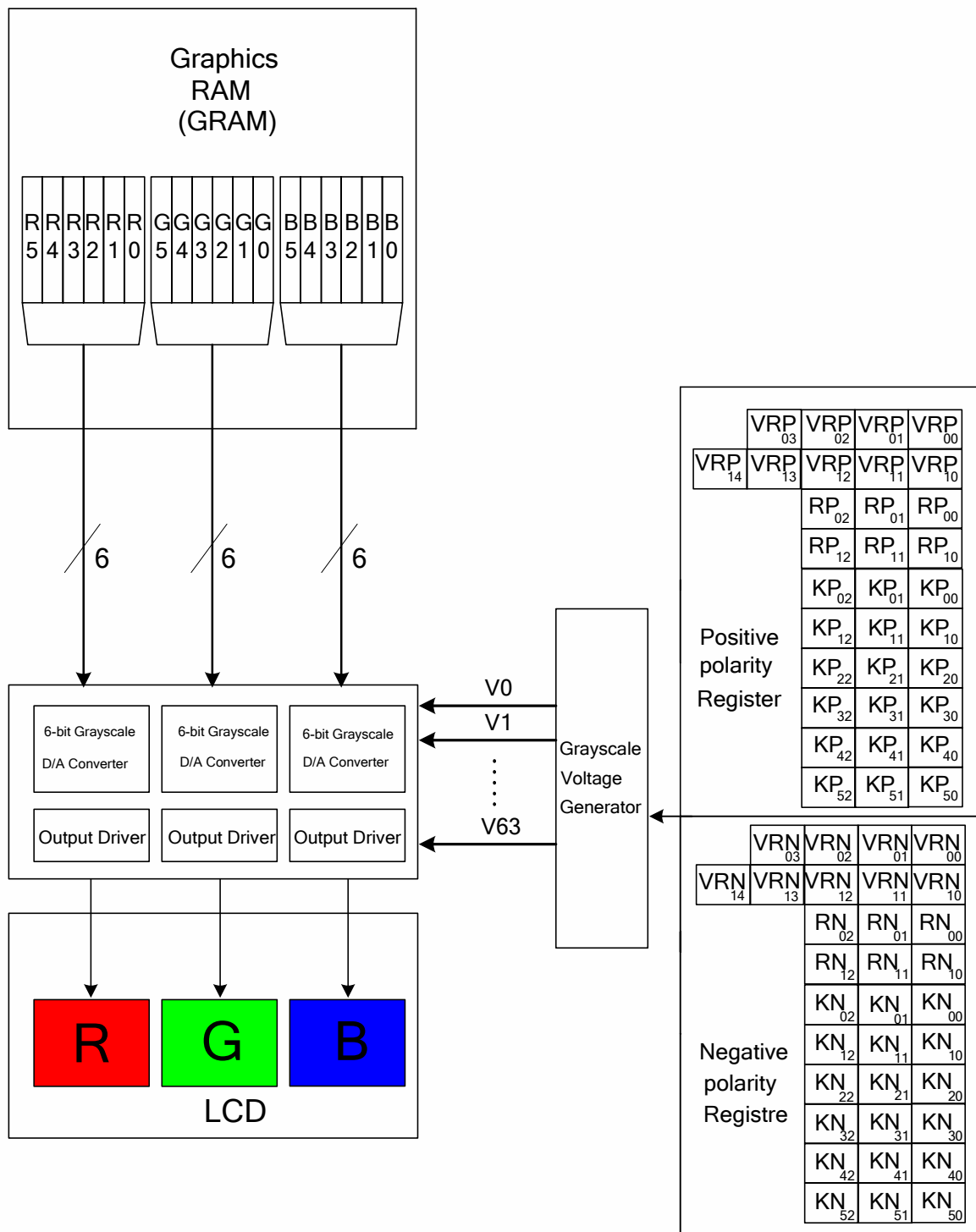


Figure 5.26: Grayscale Control

5.7.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages $VgP/N(0, 1, 8, 20, 43, 55, 62, 63)$ for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages ($V0-V63$) can be generated from grayscale amplifier for LCD panel used.

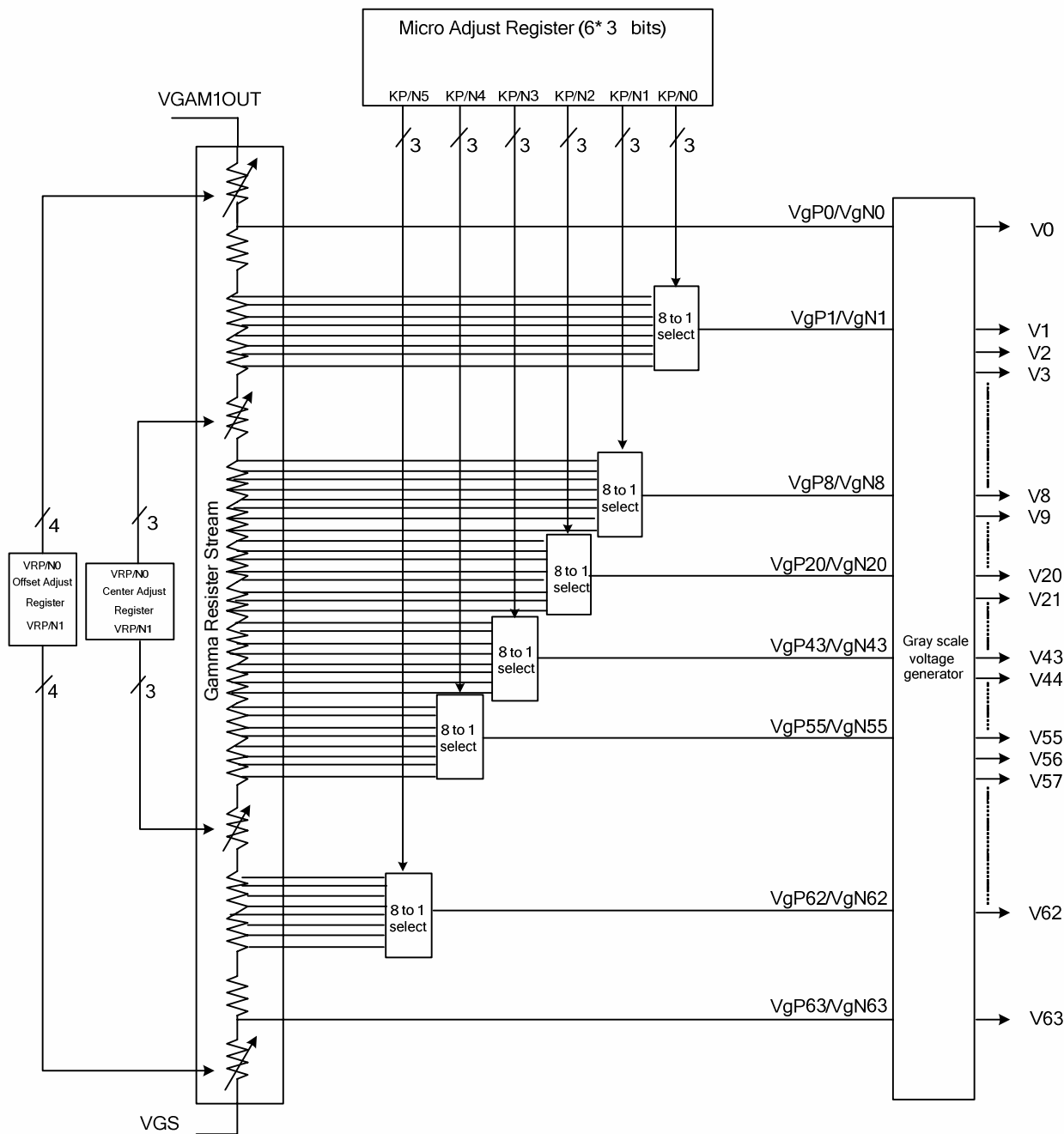


Figure 5.27: Structure of Grayscale Voltage Generator

5.7.2 Gamma-Characteristics Adjustment Register

This HX8357-B has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

A. Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

B. Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

C. Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (KP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	RP0 2-0	RN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	RP1 2-0	RN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	KP0 2-0	KN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	KP1 2-0	KN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	KP2 2-0	KN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	KP3 2-0	KN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	KP4 2-0	KN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	KP5 2-0	KN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	VRP0 3-0	VRN0 3-0	Variable resistor (VROP/N0) for offset adjustment
	VRP1 4-0	VRN1 4-0	Variable resistor (VROP/N1) for offset adjustment

Table 5.7: Gamma-Adjustment Registers

5.7.3 Gamma resistor stream and 8 to 1 Selector

The block consists of two gamma resistor streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (VgP/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

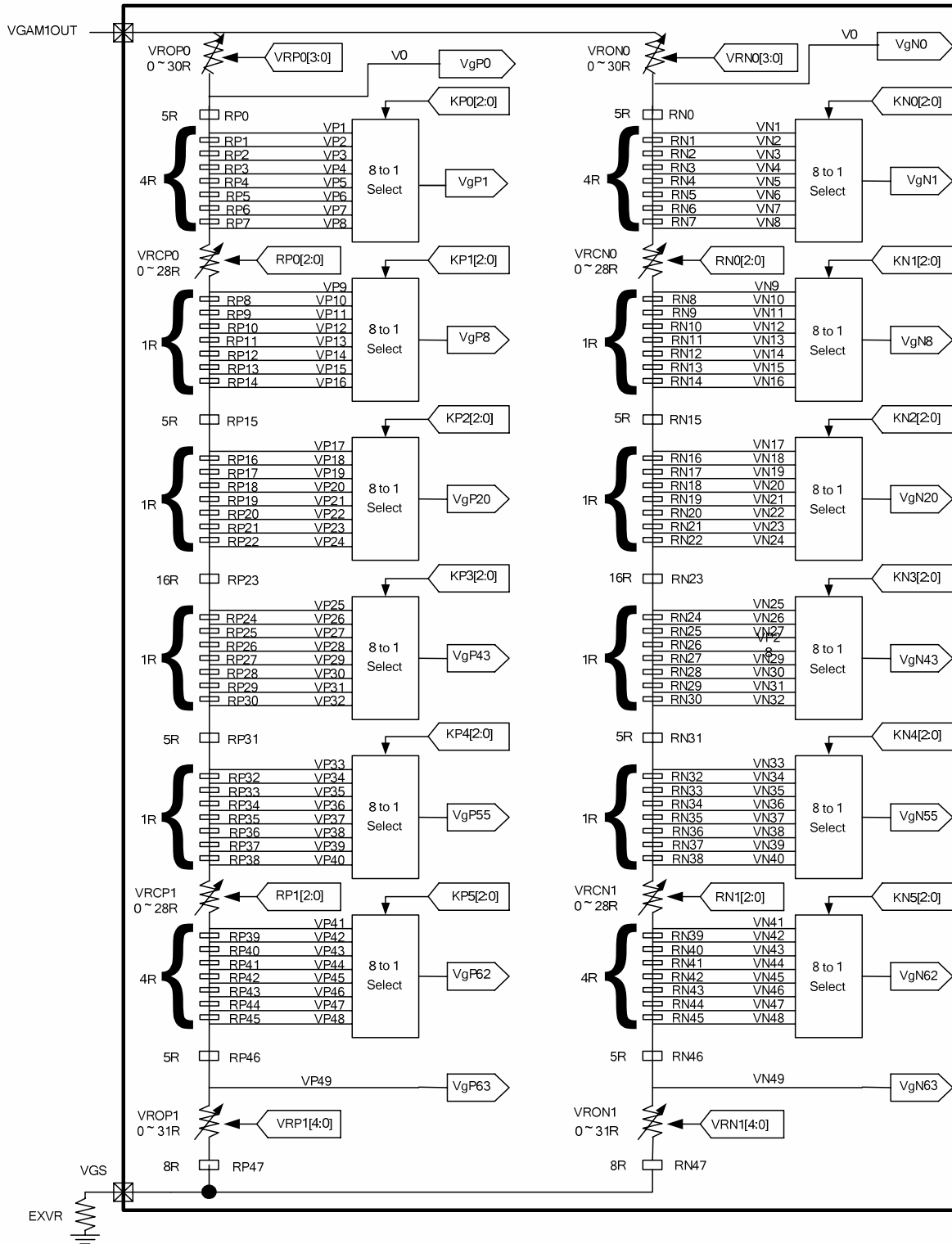


Figure 5.28: Gamma Resistor Stream and Gamma Reference Voltage

A. Variable resistor

There are two types of variable resistors, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5.8: Offset Adjustment 0

Value in Register VR(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5.9: Offset Adjustment 1

Value in Register R(P/N)0/1 2-0	Resistance VRC(P/N)0/1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5.10: Center Adjustment

B. 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resistor stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register K(P/N) 2-0	Voltage level					
	Vg(P/N) 1	Vg(P/N) 8	Vg(P/N) 20	Vg(P/N) 43	V(P/N) 55	V(P/N) 62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5.11: Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	-	VGAM1OUT-VD*VROP0 /sumRP	VP0
VgP1	KP0 2-0=000	VGAM1OUT-VD((VROP0+5R) /sumRP	VP1
	KP0 2-0=001	VGAM1OUT-VD((VROP0+9R) /sumRP	VP2
	KP0 2-0=010	VGAM1OUT-VD((VROP0+13R) /sumRP	VP3
	KP0 2-0=011	VGAM1OUT-VD((VROP0+17R) /sumRP	VP4
	KP0 2-0=100	VGAM1OUT-VD((VROP0+21R) /sumRP	VP5
	KP0 2-0=101	VGAM1OUT-VD((VROP0+25R) /sumRP	VP6
	KP0 2-0=110	VGAM1OUT-VD((VROP0+29R) /sumRP	VP7
	KP0 2-0=111	VGAM1OUT-VD((VROP0+33R) /sumRP	VP8
VgP8	KP1 2-0=000	VGAM1OUT-VD((VROP0+33R+VRCP0) /sumRP	VP9
	KP1 2-0=001	VGAM1OUT-VD((VROP0+34R+VRCP0) /sumRP	VP10
	KP1 2-0=010	VGAM1OUT-VD((VROP0+35R+VRCP0) /sumRP	VP11
	KP1 2-0=011	VGAM1OUT-VD((VROP0+36R+VRCP0) /sumRP	VP12
	KP1 2-0=100	VGAM1OUT-VD((VROP0+37R+VRCP0) /sumRP	VP13
	KP1 2-0=101	VGAM1OUT-VD((VROP0+38R+VRCP0) /sumRP	VP14
	KP1 2-0=110	VGAM1OUT-VD((VROP0+39R+VRCP0) /sumRP	VP15
	KP1 2-0=111	VGAM1OUT-VD((VROP0+40R+VRCP0) /sumRP	VP16
VgP20	KP2 2-0=000	VGAM1OUT-VD((VROP0+45R+VRCP0) /sumRP	VP17
	KP2 2-0=001	VGAM1OUT-VD((VROP0+46R+VRCP0) /sumRP	VP18
	KP2 2-0=010	VGAM1OUT-VD((VROP0+47R+VRCP0) /sumRP	VP19
	KP2 2-0=011	VGAM1OUT-VD((VROP0+48R+VRCP0) /sumRP	VP20
	KP2 2-0=100	VGAM1OUT-VD((VROP0+49R+VRCP0) /sumRP	VP21
	KP2 2-0=101	VGAM1OUT-VD((VROP0+50R+VRCP0) /sumRP	VP22
	KP2 2-0=110	VGAM1OUT-VD((VROP0+51R+VRCP0) /sumRP	VP23
	KP2 2-0=111	VGAM1OUT-VD((VROP0+52R+VRCP0) /sumRP	VP24
VgP43	KP3 2-0=000	VGAM1OUT-VD((VROP0+68R+VRCP0) /sumRP	VP25
	KP3 2-0=001	VGAM1OUT-VD((VROP0+69R+VRCP0) /sumRP	VP26
	KP3 2-0=010	VGAM1OUT-VD((VROP0+70R+VRCP0) /sumRP	VP27
	KP3 2-0=011	VGAM1OUT-VD((VROP0+71R+VRCP0) /sumRP	VP28
	KP3 2-0=100	VGAM1OUT-VD((VROP0+72R+VRCP0) /sumRP	VP29
	KP3 2-0=101	VGAM1OUT-VD((VROP0+73R+VRCP0) /sumRP	VP30
	KP3 2-0=110	VGAM1OUT-VD((VROP0+74R+VRCP0) /sumRP	VP31
	KP3 2-0=111	VGAM1OUT-VD((VROP0+75R+VRCP0) /sumRP	VP32
VgP55	KP4 2-0=000	VGAM1OUT-VD((VROP0+80R+VRCP0) /sumRP	VP33
	KP4 2-0=001	VGAM1OUT-VD((VROP0+81R+VRCP0) /sumRP	VP34
	KP4 2-0=010	VGAM1OUT-VD((VROP0+82R+VRCP0) /sumRP	VP35
	KP4 2-0=011	VGAM1OUT-VD((VROP0+83R+VRCP0) /sumRP	VP36
	KP4 2-0=100	VGAM1OUT-VD((VROP0+84R+VRCP0) /sumRP	VP37
	KP4 2-0=101	VGAM1OUT-VD((VROP0+85R+VRCP0) /sumRP	VP38
	KP4 2-0=110	VGAM1OUT-VD((VROP0+86R+VRCP0) /sumRP	VP39
	KP4 2-0=111	VGAM1OUT-VD((VROP0+87R+VRCP0) /sumRP	VP40
VgP62	KP5 2-0=000	VGAM1OUT-VD((VROP0+87R+VRCP0+VRCP1) /sumRP	VP41
	KP5 2-0=001	VGAM1OUT-VD((VROP0+91R+VRCP0+VRCP1) /sumRP	VP42
	KP5 2-0=010	VGAM1OUT-VD((VROP0+95R+VRCP0+VRCP1) /sumRP	VP43
	KP5 2-0=011	VGAM1OUT-VD((VROP0+99R+VRCP0+VRCP1) /sumRP	VP44
	KP5 2-0=100	VGAM1OUT-VD((VROP0+103R+VRCP0+VRCP1) /sumRP	VP45
	KP5 2-0=101	VGAM1OUT-VD((VROP0+107R+VRCP0+VRCP1) /sumRP	VP46
	KP5 2-0=110	VGAM1OUT-VD((VROP0+111R+VRCP0+VRCP1) /sumRP	VP47
	KP5 2-0=111	VGAM1OUT-VD((VROP0+115R+VRCP0+VRCP1) /sumRP	VP48
VgP63	-	VGAM1OUT-VD((VROP0+120R+VRCP0+VRCP1) /sumRP	VP49

SumRP = 128R +VROP0+ VROP1+ VRCP0+ VRCP1.

SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1.

VD=(VGAM1OUT-VGS).

$[\text{sumRP} \times (\text{sumRN} / (\text{sumRP} + \text{sumRN}))] / [\text{sumRP} \times \text{sumRN} / (\text{sumRP} + \text{sumRN}) + \text{EXVR}]$

Table 5.12: Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula
V0	VgP0
V1	VgP1
V2	$V8+(V1-V8)*(30/48)$
V3	$V8+(V1-V8)*(23/48)$
V4	$V8+(V1-V8)*(16/48)$
V5	$V8+(V1-V8)*(12/48)$
V6	$V8+(V1-V8)*(8/48)$
V7	$V8+(V1-V8)*(4/48)$
V8	VgP8
V9	$V20+(V8-V20)*(22/24)$
V10	$V20+(V8-V20)*(20/24)$
V11	$V20+(V8-V20)*(18/24)$
V12	$V20+(V8-V20)*(16/24)$
V13	$V20+(V8-V20)*(14/24)$
V14	$V20+(V8-V20)*(12/24)$
V15	$V20+(V8-V20)*(10/24)$
V16	$V20+(V8-V20)*(8/24)$
V17	$V20+(V8-V20)*(6/24)$
V18	$V20+(V8-V20)*(4/24)$
V19	$V20+(V8-V20)*(2/24)$
V20	VINP3
V21	$V43+(V20-V43)*(22/23)$
V22	$V43+(V20-V43)*(21/23)$
V23	$V43+(V20-V43)*(20/23)$
V24	$V43+(V20-V43)*(19/23)$
V25	$V43+(V20-V43)*(18/23)$
V26	$V43+(V20-V43)*(17/23)$
V27	$V43+(V20-V43)*(16/23)$
V28	$V43+(V20-V43)*(15/23)$
V29	$V43+(V20-V43)*(14/23)$
V30	$V43+(V20-V43)*(13/23)$
V31	$V43+(V20-V43)*(12/23)$
V32	$V43+(V20-V43)*(11/23)$
V33	$V43+(V20-V43)*(10/23)$
V34	$V43+(V20-V43)*(9/23)$
V35	$V43+(V20-V43)*(8/23)$
V36	$V43+(V20-V43)*(7/23)$
V37	$V43+(V20-V43)*(6/23)$
V38	$V43+(V20-V43)*(5/23)$
V39	$V43+(V20-V43)*(4/23)$
V40	$V43+(V20-V43)*(3/23)$
V41	$V43+(V20-V43)*(2/23)$
V42	$V43+(V20-V43)*(1/23)$
V43	VINP4
V44	$V55+(V43-V55)*(22/24)$
V45	$V55+(V43-V55)*(20/24)$
V46	$V55+(V43-V55)*(18/24)$
V47	$V55+(V43-V55)*(16/24)$
V48	$V55+(V43-V55)*(14/24)$
V49	$V55+(V43-V55)*(12/24)$
V50	$V55+(V43-V55)*(10/24)$
V51	$V55+(V43-V55)*(8/24)$
V52	$V55+(V43-V55)*(6/24)$
V53	$V55+(V43-V55)*(4/24)$
V54	$V55+(V43-V55)*(2/24)$
V55	VINP5
V56	$V62+(V55-V62)*(44/48)$
V57	$V62+(V55-V62)*(40/48)$
V58	$V62+(V55-V62)*(36/48)$
V59	$V62+(V55-V62)*(32/48)$
V60	$V62+(V55-V62)*(25/48)$
V61	$V62+(V55-V62)*(18/48)$
V62	VINP6
V63	VINP7

Table 5.13: Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	$VGAM1OUT-VD \cdot VRON0 / \text{sumRN}$	VN0
VgN1	KN0 2-0=000	$VGAM1OUT-VD((VRON0+5R) / \text{sumRN})$	VN1
	KN0 2-0=001	$VGAM1OUT-VD((VRON0+9R) / \text{sumRN})$	VN2
	KN0 2-0=010	$VGAM1OUT-VD((VRON0+13R) / \text{sumRN})$	VN3
	KN0 2-0=011	$VGAM1OUT-VD((VRON0+17R) / \text{sumRN})$	VN4
	KN0 2-0=100	$VGAM1OUT-VD((VRON0+21R) / \text{sumRN})$	VN5
	KN0 2-0=101	$VGAM1OUT-VD((VRON0+25R) / \text{sumRN})$	VN6
	KN0 2-0=110	$VGAM1OUT-VD((VRON0+29R) / \text{sumRN})$	VN7
VgN8	KN1 2-0=111	$VGAM1OUT-VD((VRON0+33R) / \text{sumRN})$	VN8
	KN1 2-0=000	$VGAM1OUT-VD((VRON0+33R+VRCN0) / \text{sumRN})$	VN9
	KN1 2-0=001	$VGAM1OUT-VD((VRON0+34R+VRCN0) / \text{sumRN})$	VN10
	KN1 2-0=010	$VGAM1OUT-VD((VRON0+35R+VRCN0) / \text{sumRN})$	VN11
	KN1 2-0=011	$VGAM1OUT-VD((VRON0+36R+VRCN0) / \text{sumRN})$	VN12
	KN1 2-0=100	$VGAM1OUT-VD((VRON0+37R+VRCN0) / \text{sumRN})$	VN13
	KN1 2-0=101	$VGAM1OUT-VD((VRON0+38R+VRCN0) / \text{sumRN})$	VN14
VgN20	KN1 2-0=110	$VGAM1OUT-VD((VRON0+39R+VRCN0) / \text{sumRN})$	VN15
	KN1 2-0=111	$VGAM1OUT-VD((VRON0+40R+VRCN0) / \text{sumRN})$	VN16
	KN2 2-0=000	$VGAM1OUT-VD((VRON0+45R+VRCN0) / \text{sumRN})$	VN17
	KN2 2-0=001	$VGAM1OUT-VD((VRON0+46R+VRCN0) / \text{sumRN})$	VN18
	KN2 2-0=010	$VGAM1OUT-VD((VRON0+47R+VRCN0) / \text{sumRN})$	VN19
	KN2 2-0=011	$VGAM1OUT-VD((VRON0+48R+VRCN0) / \text{sumRN})$	VN20
	KN2 2-0=100	$VGAM1OUT-VD((VRON0+49R+VRCN0) / \text{sumRN})$	VN21
VgN43	KN2 2-0=101	$VGAM1OUT-VD((VRON0+50R+VRCN0) / \text{sumRN})$	VN22
	KN2 2-0=110	$VGAM1OUT-VD((VRON0+51R+VRCN0) / \text{sumRN})$	VN23
	KN2 2-0=111	$VGAM1OUT-VD((VRON0+52R+VRCN0) / \text{sumRN})$	VN24
	KN3 2-0=000	$VGAM1OUT-VD((VRON0+68R+VRCN0) / \text{sumRN})$	VN25
	KN3 2-0=001	$VGAM1OUT-VD((VRON0+69R+VRCN0) / \text{sumRN})$	VN26
	KN3 2-0=010	$VGAM1OUT-VD((VRON0+70R+VRCN0) / \text{sumRN})$	VN27
	KN3 2-0=011	$VGAM1OUT-VD((VRON0+71R+VRCN0) / \text{sumRN})$	VNP8
VgN55	KN3 2-0=100	$VGAM1OUT-VD((VRON0+72R+VRCN0) / \text{sumRN})$	VN29
	KN3 2-0=101	$VGAM1OUT-VD((VRON0+73R+VRCN0) / \text{sumRN})$	VN30
	KN3 2-0=110	$VGAM1OUT-VD((VRON0+74R+VRCN0) / \text{sumRN})$	VN31
	KN3 2-0=111	$VGAM1OUT-VD((VRON0+75R+VRCN0) / \text{sumRN})$	VN32
	KN4 2-0=000	$VGAM1OUT-VD((VRON0+80R+VRCN0) / \text{sumRN})$	VN33
	KN4 2-0=001	$VGAM1OUT-VD((VRON0+81R+VRCN0) / \text{sumRN})$	VN34
	KN4 2-0=010	$VGAM1OUT-VD((VRON0+82R+VRCN0) / \text{sumRN})$	VN35
VgN62	KN4 2-0=011	$VGAM1OUT-VD((VRON0+83R+VRCN0) / \text{sumRN})$	VN36
	KN4 2-0=100	$VGAM1OUT-VD((VRON0+84R+VRCN0) / \text{sumRN})$	VN37
	KN4 2-0=101	$VGAM1OUT-VD((VRON0+85R+VRCN0) / \text{sumRN})$	VN38
	KN4 2-0=110	$VGAM1OUT-VD((VRON0+86R+VRCN0) / \text{sumRN})$	VN39
	KN4 2-0=111	$VGAM1OUT-VD((VRON0+87R+VRCN0) / \text{sumRN})$	VN40
	KN5 2-0=000	$VGAM1OUT-VD((VRON0+87R+VRCN0+VRCN1) / \text{sumRN})$	VN41
	KN5 2-0=001	$VGAM1OUT-VD((VRON0+91R+VRCN0+VRCN1) / \text{sumRN})$	VN42
VgN63	KN5 2-0=010	$VGAM1OUT-VD((VRON0+95R+VRCN0+VRCN1) / \text{sumRN})$	VN43
	KN5 2-0=011	$VGAM1OUT-VD((VRON0+99R+VRCN0+VRCN1) / \text{sumRN})$	VN44
	KN5 2-0=100	$VGAM1OUT-VD((VRON0+103R+VRCN0+VRCN1) / \text{sumRN})$	VN45
	KN5 2-0=101	$VGAM1OUT-VD((VRON0+107R+VRCN0+VRCN1) / \text{sumRN})$	VN46
	KN5 2-0=110	$VGAM1OUT-VD((VRON0+111R+VRCN0+VRCN1) / \text{sumRN})$	VN47
	KN5 2-0=111	$VGAM1OUT-VD((VRON0+115R+VRCN0+VRCN1) / \text{sumRN})$	VN48
	VgN63	-	$VGAM1OUT-VD((VRON0+120R+VRCN0+VRCN1) / \text{sumRN})$

SumRP = 128R + VROP0+ VROP1+ VRCN0+ VRCN1;

SumRN = 128R+ VRON0+ VRON1+ VRCN0 + VRCN1

VD = (VGAM1OUT-VGS) [sumRP(sumRN/(sumRP+sumRN))]/[sumRP(sumRN/(sumRP+sumRN))+EXVR)

Table 5.14: Voltage Calculation Formula (Negative Polarity)

Grayscale Voltage	Formula
V0	VgN0
V1	VlgN1
V2	$V8+(V1-V8)*(30/48)$
V3	$V8+(V1-V8)*(23/48)$
V4	$V8+(V1-V8)*(16/48)$
V5	$V8+(V1-V8)*(12/48)$
V6	$V8+(V1-V8)*(8/48)$
V7	$V8+(V1-V8)*(4/48)$
V8	VgN8
V9	$V20+(V8-V20)*(22/24)$
V10	$V20+(V8-V20)*(20/24)$
V11	$V20+(V8-V20)*(18/24)$
V12	$V20+(V8-V20)*(16/24)$
V13	$V20+(V8-V20)*(14/24)$
V14	$V20+(V8-V20)*(12/24)$
V15	$V20+(V8-V20)*(10/24)$
V16	$V20+(V8-V20)*(8/24)$
V17	$V20+(V8-V20)*(6/24)$
V18	$V20+(V8-V20)*(4/24)$
V19	$V20+(V8-V20)*(2/24)$
V20	VgN20
V21	$V43+(V20-V43)*(22/23)$
V22	$V43+(V20-V43)*(21/23)$
V23	$V43+(V20-V43)*(20/23)$
V24	$V43+(V20-V43)*(19/23)$
V25	$V43+(V20-V43)*(18/23)$
V26	$V43+(V20-V43)*(17/23)$
V27	$V43+(V20-V43)*(16/23)$
V28	$V43+(V20-V43)*(15/23)$
V29	$V43+(V20-V43)*(14/23)$
V30	$V43+(V20-V43)*(13/23)$
V31	$V43+(V20-V43)*(12/23)$
V32	$V43+(V20-V43)*(11/23)$
V33	$V43+(V20-V43)*(10/23)$
V34	$V43+(V20-V43)*(9/23)$
V35	$V43+(V20-V43)*(8/23)$
V36	$V43+(V20-V43)*(7/23)$
V37	$V43+(V20-V43)*(6/23)$
V38	$V43+(V20-V43)*(5/23)$
V39	$V43+(V20-V43)*(4/23)$
V40	$V43+(V20-V43)*(3/23)$
V41	$V43+(V20-V43)*(2/23)$
V42	$V43+(V20-V43)*(1/23)$
V43	VgN43
V44	$V55+(V43-V55)*(22/24)$
V45	$V55+(V43-V55)*(20/24)$
V46	$V55+(V43-V55)*(18/24)$
V47	$V55+(V43-V55)*(16/24)$
V48	$V55+(V43-V55)*(14/24)$
V49	$V55+(V43-V55)*(12/24)$
V50	$V55+(V43-V55)*(10/24)$
V51	$V55+(V43-V55)*(8/24)$
V52	$V55+(V43-V55)*(6/24)$
V53	$V55+(V43-V55)*(4/24)$
V54	$V55+(V43-V55)*(2/24)$
V55	VgN55
V56	$V62+(V55-V62)*(44/48)$
V57	$V62+(V55-V62)*(40/48)$
V58	$V62+(V55-V62)*(36/48)$
V59	$V62+(V55-V62)*(32/48)$
V60	$V62+(V55-V62)*(25/48)$
V61	$V62+(V55-V62)*(18/48)$
V62	VgN62
V63	VgN63

Table 5.15: Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Relationship between GRAM Data and Output Level.

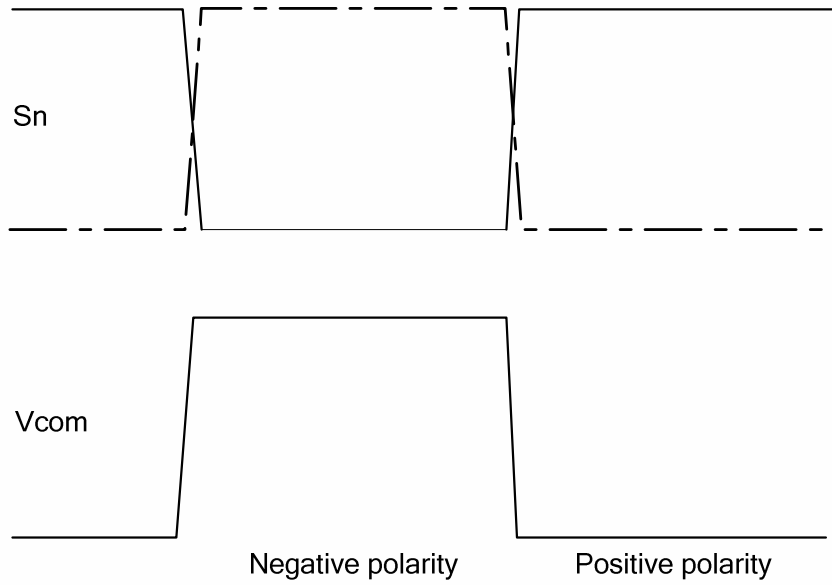
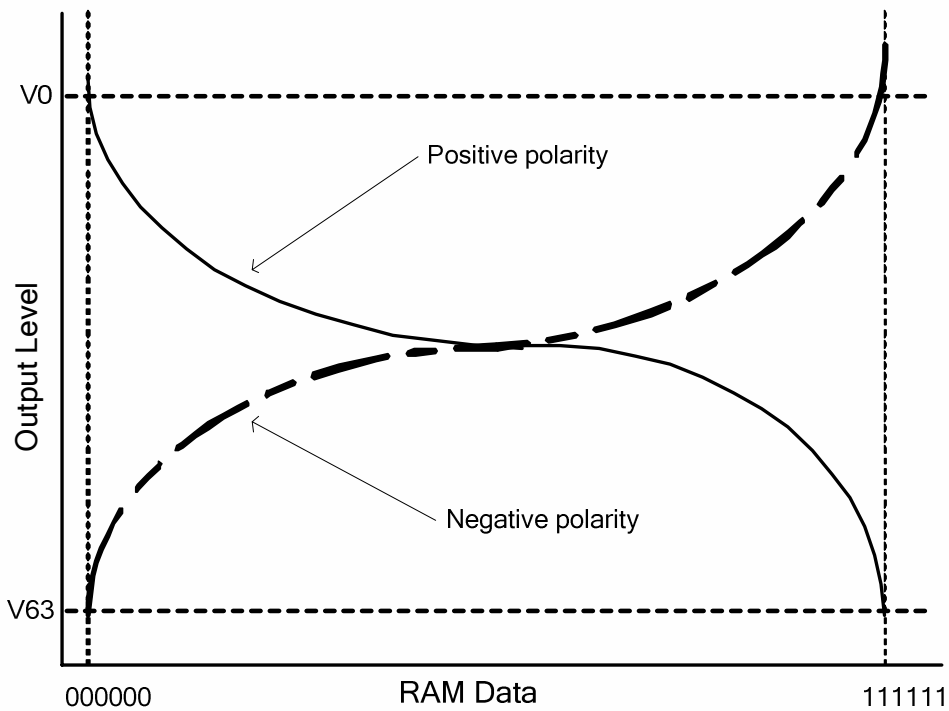


Figure 5.29: Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 5.30: Relationships between GRAM Data and Output Level

5.8 Power Flow Chart for Different Power Modes

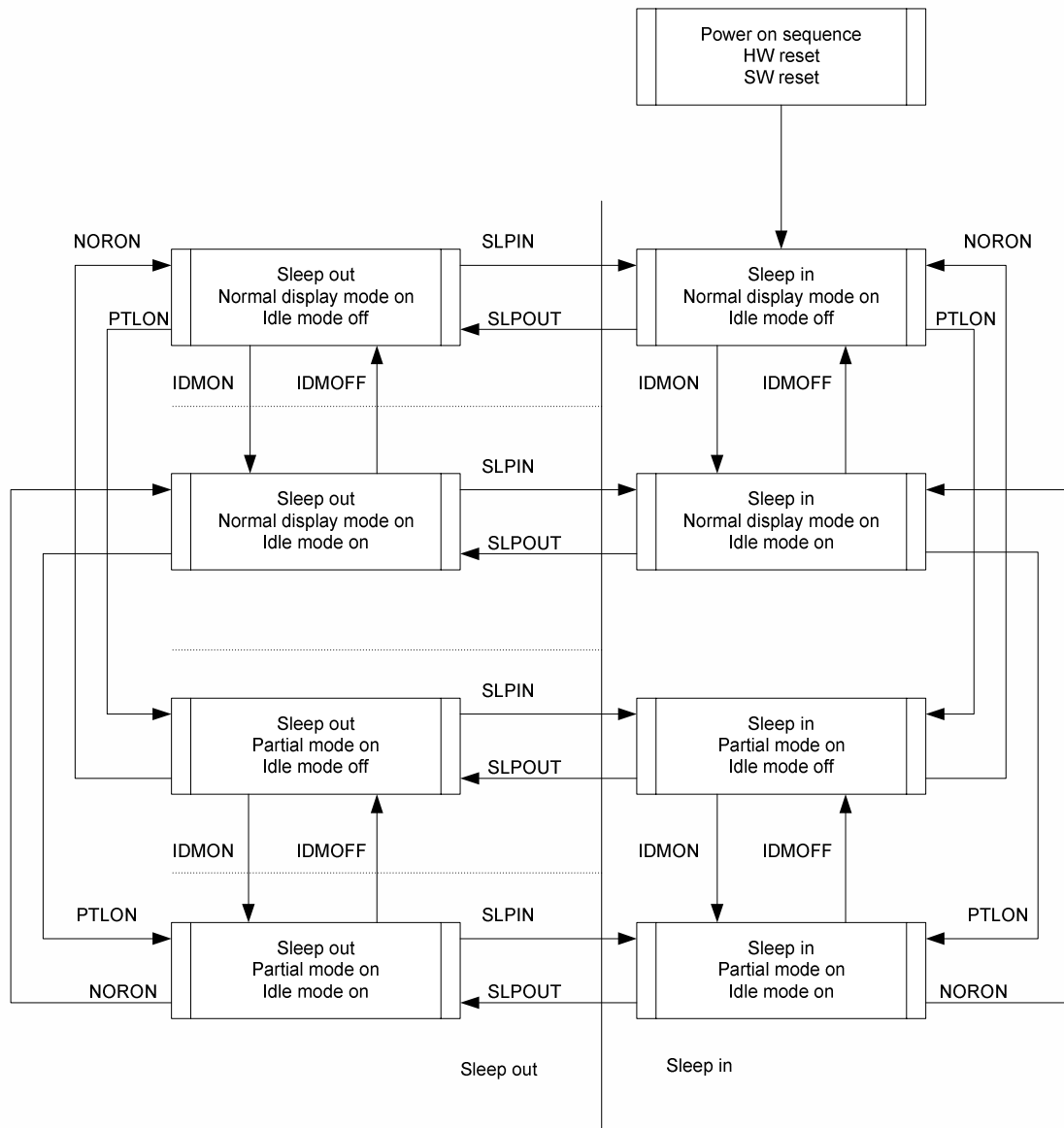


Figure 5.31: Power Flow Chart for Different Power Modes

Mode		Meaning	Other word
Display Mode	Normal Mode	Driving Mode for Fully Display "Partial Mode Off" and "Scroll Mode Off"	Normal Mode On Normal Display Mode On
	Partial Mode	Driving Mode for Partial Display	Partial Mode On
Color Mode	Idle Mode On	8 Color Mode	-
	Idle Mode Off	Full Color Mode	-

Table 5.16: Mode definition

5.9 Input / Output Pin State

5.9.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
CABC_ON, CABC_PWM	Low	Low	Low
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Table 5.17: Characteristics of Output or Bi-directional (I/O) Pins

5.9.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	Section 7.12	Input valid	Input valid	Input valid	Section 7.12
CSX	Input valid	Input valid	Input valid	Input valid	Input valid
DCX	Input valid	Input valid	Input valid	Input valid	Input valid
WRX_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
RDX	Input valid	Input valid	Input valid	Input valid	Input valid
DB17 to DB0 DIN_SDA	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
PCLK	Input valid	Input valid	Input valid	Input valid	Input valid
DE	Input valid	Input valid	Input valid	Input valid	Input valid
IMO2, IM1, IM0, SD, CM	Input valid	Input valid	Input valid	Input valid	Input valid
TEST3-1	Low	Low	Low	Low	Low

Table 5.18: Characteristics of Input Pins

5.9.3 Sleep Out –Command and Self-Diagnostic functions of The Display Module

5.9.4 Register loading Detection

Sleep Out-command (See section 6.2.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.2.9 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

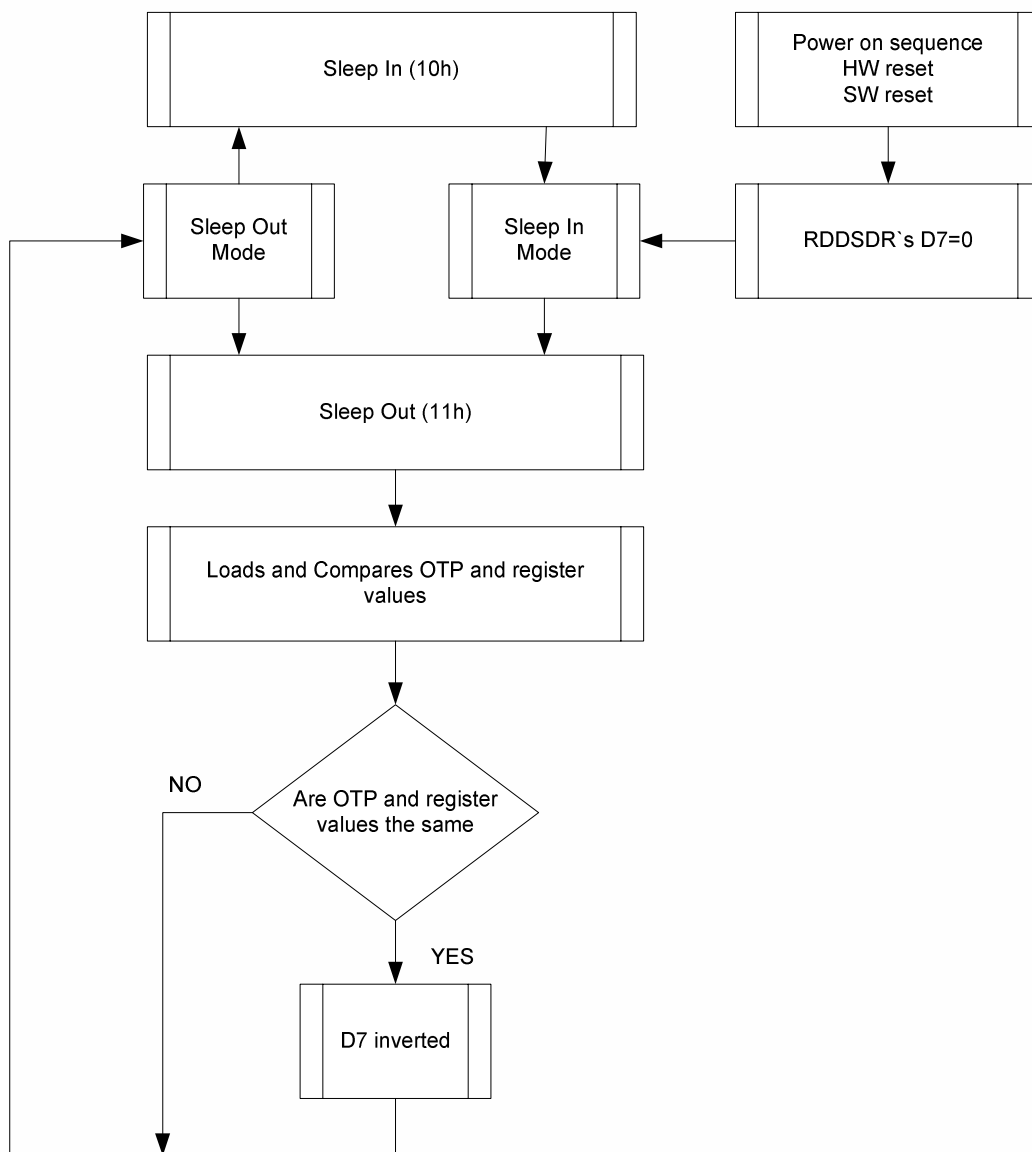


Figure 5.32: Sleep Out Flow Chart – Command and Self-Diagnostic Functions

5.9.5 Functionality Detection

Sleep Out-command (See section 6.2.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 6.2.11 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is following:

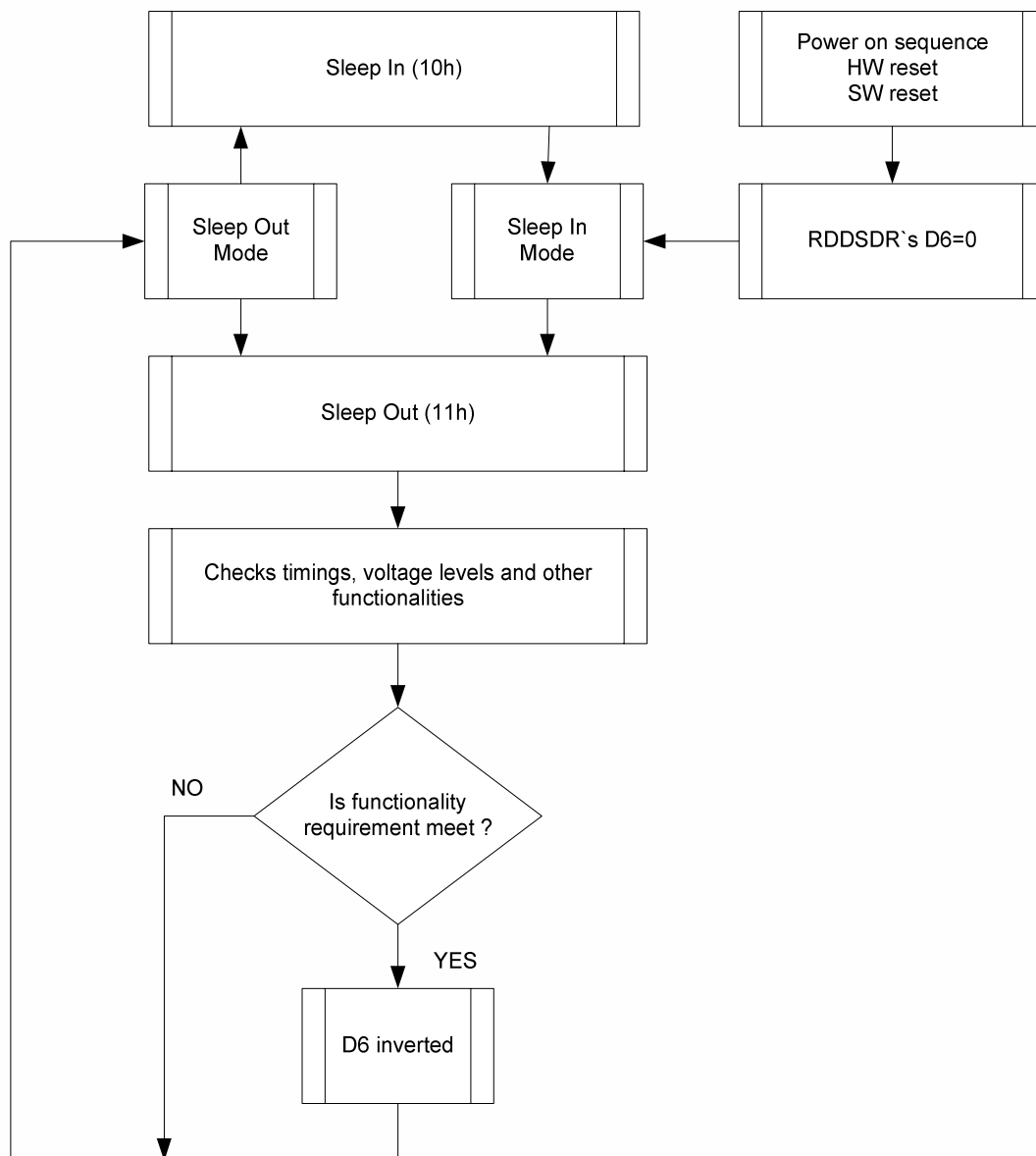


Figure 5.33: Sleep Out Flow Chart Internal Function Detection

5.10 Power On/Off Sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order. During power off, if LCD is in the Sleep Out mode, IOVCC and VCI must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, IOVCC and VCI can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power on Sequence as defined in Sections 7.12.1 and 7.12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power on Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC and VCI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

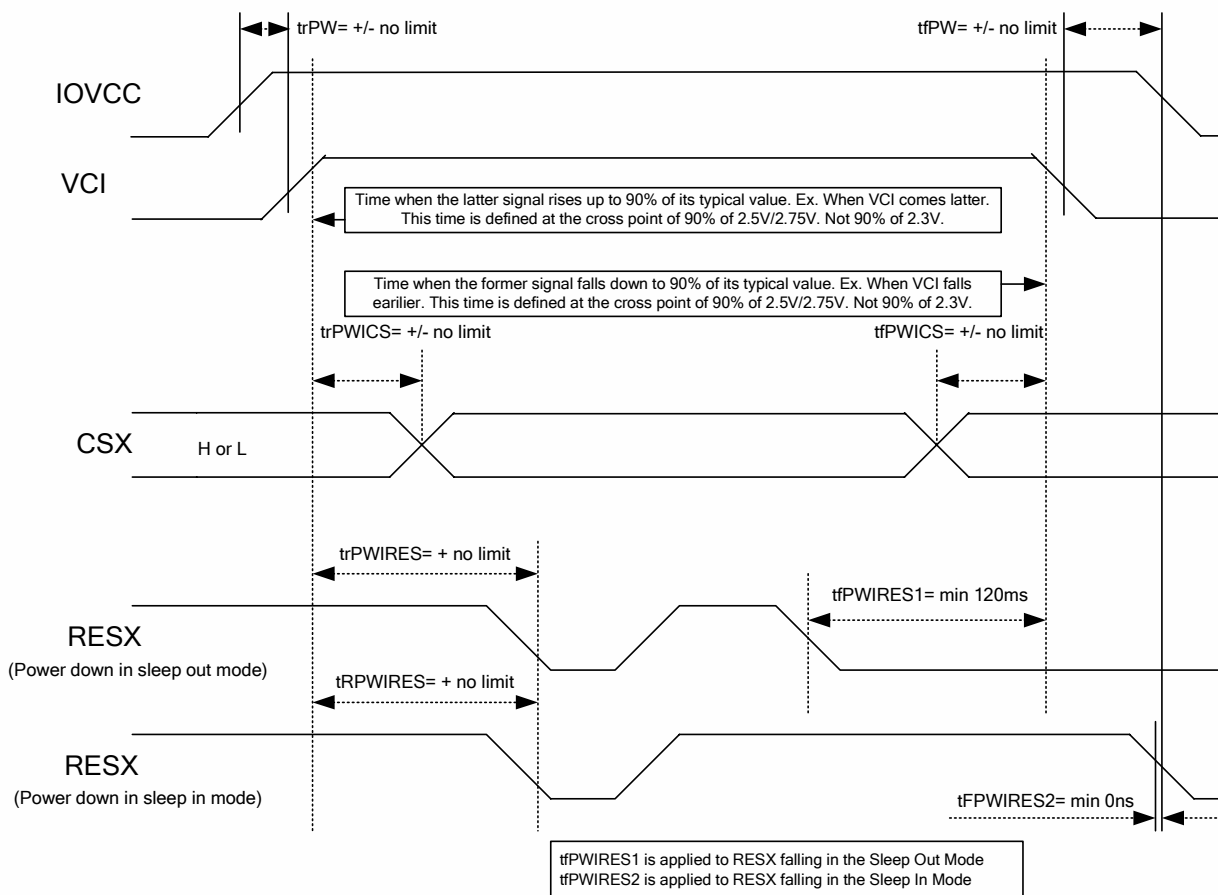


Figure 5.34: Case 1 –RESX line is held High or Unstable by Host at Power On

5.10.2 Case 2 – RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both IOVCC and VCI have been applied.

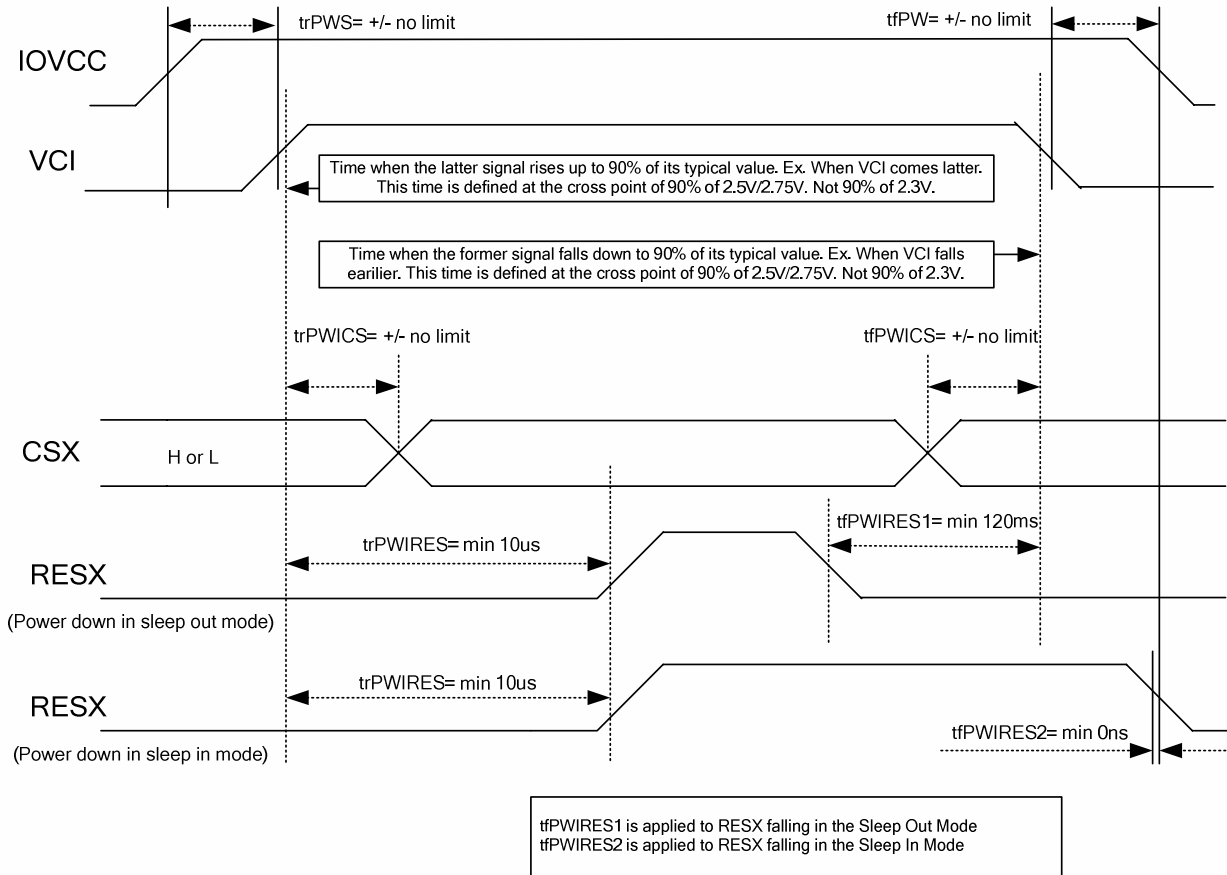


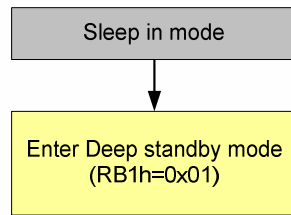
Figure 5.35: Case 2 – RESX line is held Low by Host at Power On

5.11 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power on Sequence" powers it

5.12 Deep standby mode enter/exit flow

A. Enter deep standby mode



* The B1 command is active only in Sleep in mode

Figure 5.36: Enter deep standby mode flow

B. Exit deep standby mode

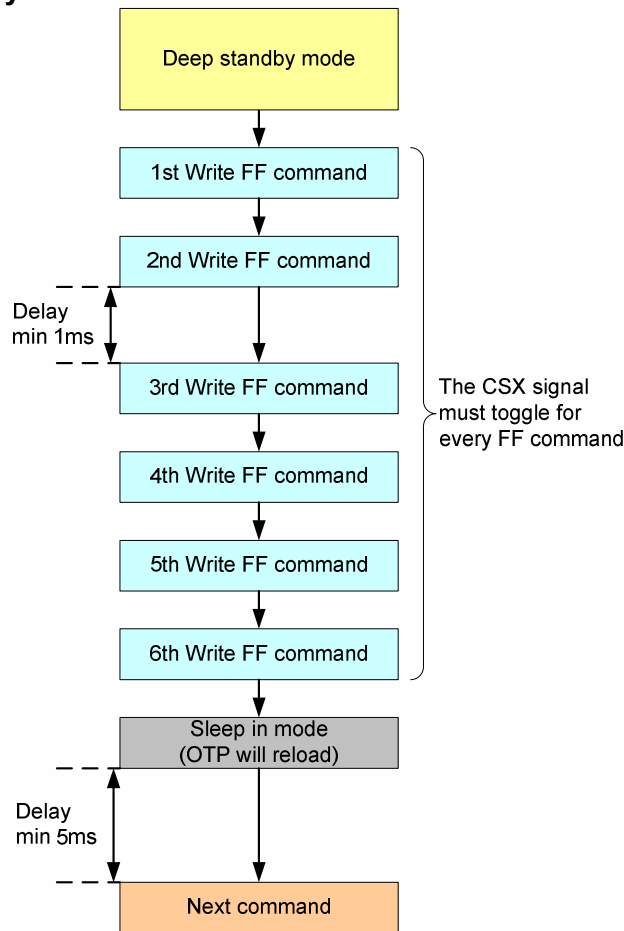


Figure 5.37: Exit Deep standby mode flow

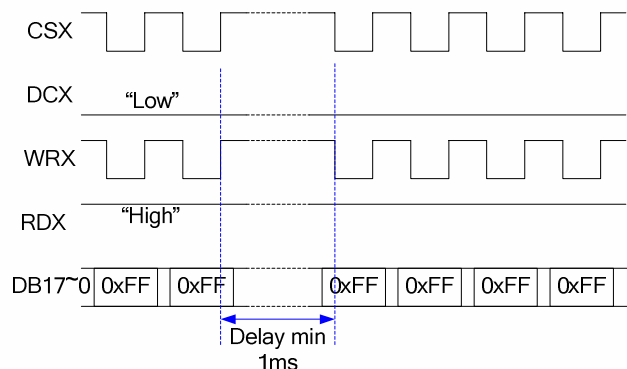


Figure 5.38: Exit Deep standby mode control signals

5.13 Content Adaptive Brightness Control (CABC) Function

The general block diagram of the CABC and the brightness control is illustrated below:

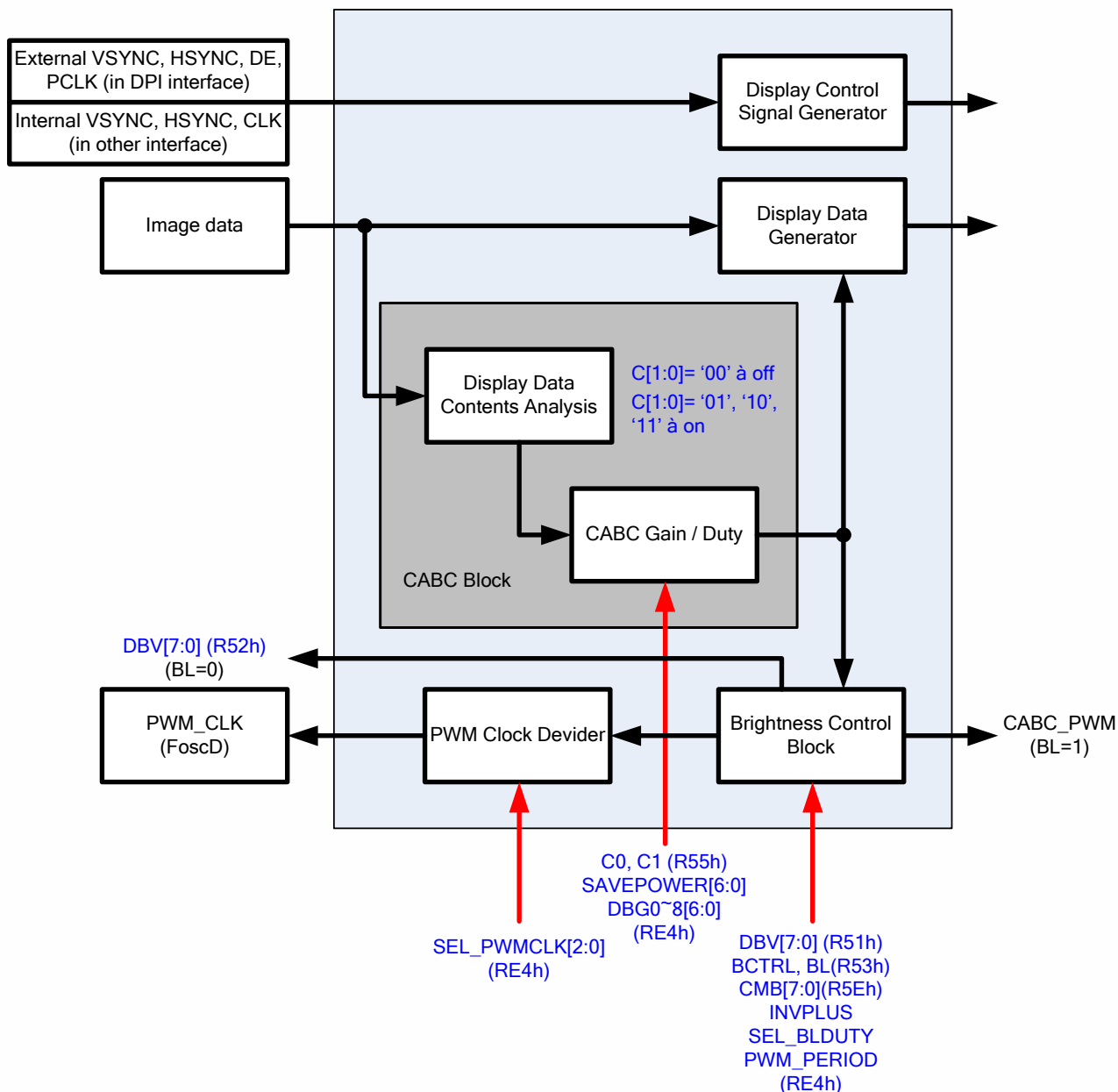


Figure 5.39: Block diagram of the CABC

5.13.1 Module Architectures

HX8357-B can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

• Architecture I

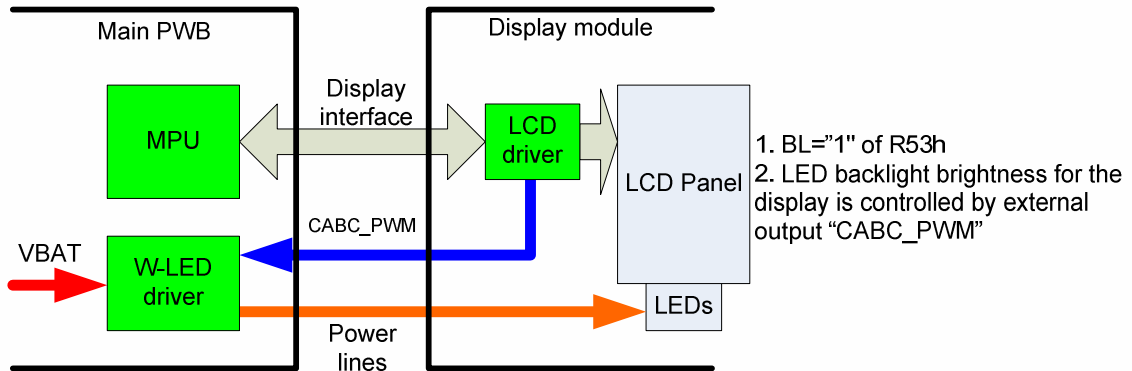


Figure 5.40: Module architecture I

• Architecture II

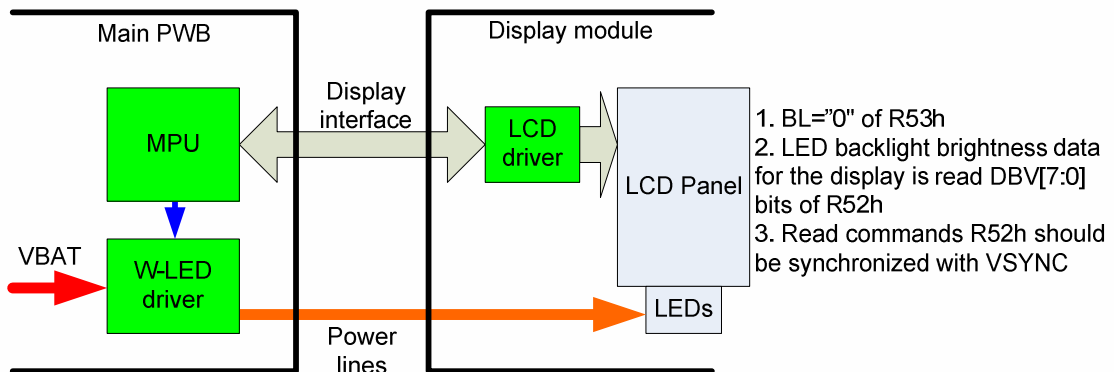


Figure 5.41: Module architecture II

5.13.2 CABC Block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that: Duty (valid level period (LED on) / one complete period) = 1/ gain.

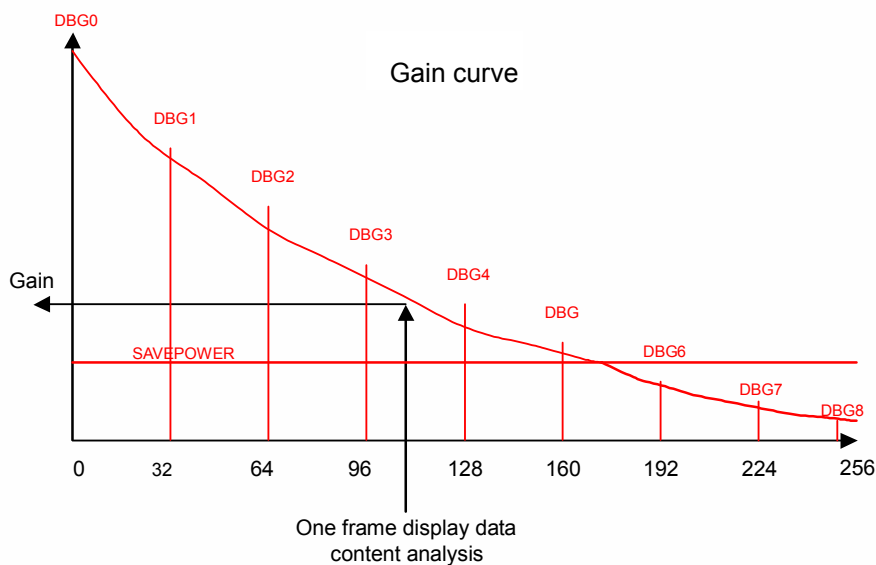


Figure 5.42: CABC Gain / CABC Duty Generation

For power saving of backlight module, there are **SAVEPOWER[6:0]** bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain/duty after one-frame display data contents analysis is smaller (gain)/larger(duty) than **SAVEPOWER[6:0]** bits setting, the CABC block will output CABC gain/duty equal to **SAVEPOWER[6:0]** and ignore the result of display data contents analysis.

5.13.3 Brightness Control Block

There is an external output signal from brightness block, CABC_PWM, to control the LED driver IC in order to control display brightness. The CABC_PWM output active polarity is defined by **INVPULS** bit of RCCh.

The CABC_PWM output period is controlled by **SEL_PWMCLK[2:0]** and **PWM_PERIOD[7:0]** bits of RE4h setting.

For ex: PWM CLK is 5.5MHz (period 180ns), SEL_PWMCLK=110(divide by 64), and PWM_PERIOD=00h.

→ CABC_PWM period = 180ns x 64 x (1x255) = 2.94 ms

There are register bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM duty is calculated as DBV[7:0]/255 x CABC duty(generated after one-frame display data content analysis).

For ex: CABC_PWM period = 2.94 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM duty = (228) / 255 x 74.42% ≅ 66.54%. Correspond to the CABC_PWM period = 2.94 ms, the high-level of CABC_PWM (high effective) = 1.96ms, and the low-level of CABC_PWM = 0.99ms.

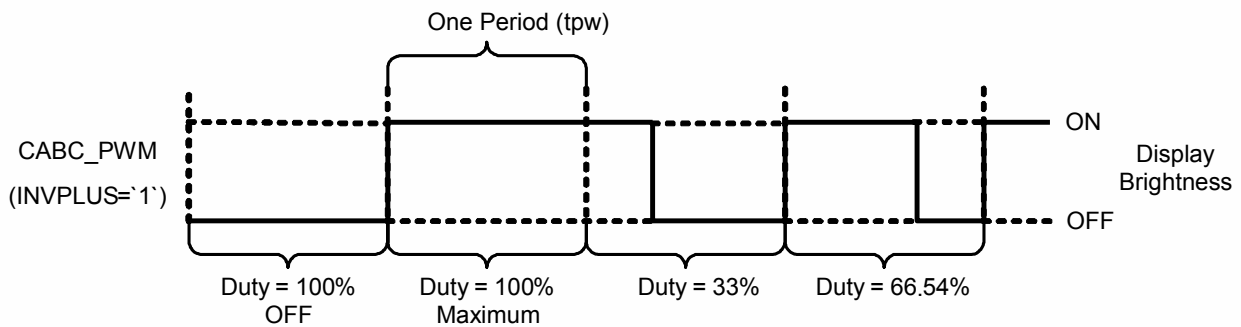


Figure 5.43: CABC_PWM Output Duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Note: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Table 5.19: CABC_PWM timing table

When Architecture II module is used (**BL**=‘0’) with the example below, the CABC_PWM is always output low(**INVPULS**=‘1’) and the CABV[7:0](R52h) will be read a value as 169_{DEC}((169)/255≅ 66.27%).

5.13.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

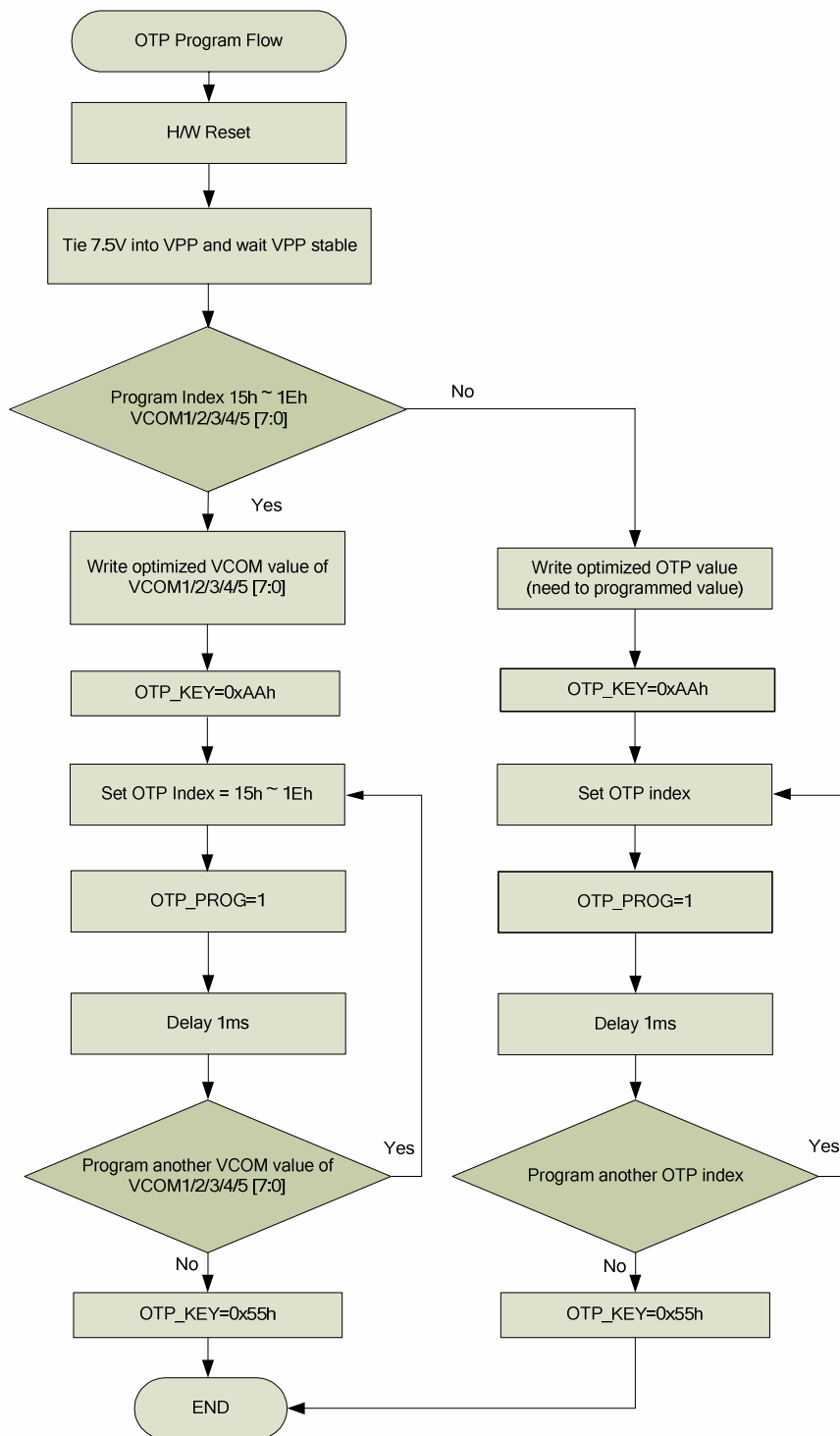
When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. "**CMB[7:0]**, Read CABC minimum brightness (R5Fh) "always read the setting value of "**CMB[7:0]**, Write CABC minimum brightness (R5Eh)"

5.14 OTP Programming

5.14.1 OTP Table

OTP_INDEX (HEX)	Ref. Command	B7	B6	B5	B4	B3	B2	B1	B0	
0		VALID_ID1	VALID_ID2	VALID_ID3	VALID_ID4	VALID_ID5				
1	ID-1(E0)	ID11								
2		ID12								
3		ID13								
4		ID14								
5	ID-2(E0)	ID21								
6		ID22								
7		ID23								
8		ID24								
9	ID-3(E0)	ID31								
A		ID32								
B		ID33								
C		ID34								
D	ID-4(E0)	ID41								
E		ID42								
F		ID43								
10		ID44								
11	ID-5(E0)	ID51								
12		ID52								
13		ID53								
14		ID54								
15	VCOM1(D1)	VALID_VCM1	VCM1[6:0]							
16		-	-	-	VDV1[4:0]					
17	VCOM2(D1)	VALID_VCM2	VCM2[6:0]							
18		-	-	-	VDV2[4:0]					
19	VCOM3(D1)	VALID_VCM3	VCM3[6:0]							
1A		-	-	-	VDV3[4:0]					
1B	VCOM4(D1)	VALID_VCM4	VCM4[6:0]							
1C		-	-	-	VDV4[4:0]					
1D	VCOM5(D1)	VALID_VCM5	VCM5[6:0]							
1E		-	-	-	VDV5[4:0]					
30	SETOSC(C5)	VALID_OSC	-	-	-	-	UADJ[2:0]			
35	SETGAMMA(C8)	VALID_GAMMA	KP1[2:0]			-	KP0[2:0]			
36		-	KP3[2:0]			-	KP2[2:0]			
37		-	KP5[2:0]			-	KP4[2:0]			
38		-	RP1[2:0]			-	RP0[2:0]			
39		-	-	-	-	VRP0[3:0]				
3A		-	-	-	-	VRP1[4:0]				
3B		-	KN1[2:0]			-	KN0[2:0]			
3C		-	KN3[2:0]			-	KN2[2:0]			
3D		-	KN5[2:0]			-	KN4[2:0]			
3E		-	RN1[2:0]			-	RN0[2:0]			
3F		-	-	-	-	VRN0[3:0]				
40		-	-	-	-	VRN1[4:0]				

5.14.2 OTP Programming flow



OTP_KEY[7:0](8h00)	Description	Note
AAh	Enter OTP Program mode	
55h	Leave OTP Program mode	
Other value	Invalid	1. If OTP is in OTP program mode, then keep OTP program mode. 2. If OTP is in non-OTP program mode, then keep non-OTP program mode. 3. OTP_KEY[7:0] can be ignored when user want to do OTP program.

Figure 5.44: OTP Programming Sequence

5.14.3 Programming sequence

Step	Operation																																				
1	Power on and reset the module																																				
2	Connect external power 7.5V to VPP pin																																				
3	Wait 100ms for VPP stable																																				
4	Write optimized value to related register																																				
	<table border="1"> <thead> <tr> <th>Command</th> <th>Register</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>ID1 (E0h)</td> <td>ID1[7:0]</td> <td>LCD module/driver version</td> </tr> <tr> <td>ID2 (E0h)</td> <td>ID2[7:0]</td> <td>LCD module/driver version</td> </tr> <tr> <td>ID3 (E0h)</td> <td>ID3[7:0]</td> <td>LCD module/driver version</td> </tr> <tr> <td>ID4 (E0h)</td> <td>ID4[7:0]</td> <td>LCD module/driver version</td> </tr> <tr> <td>ID5 (E0h)</td> <td>ID5[7:0]</td> <td>LCD module/driver version</td> </tr> <tr> <td>VCOM1 (D1h)</td> <td>VCM1[6:0], VDV1[4:0]</td> <td>VCOMH and VCOM amplitude setting.</td> </tr> <tr> <td>VCOM2 (D1h)</td> <td>VCM2[6:0], VDV2[4:0]</td> <td>VCOMH and VCOM amplitude setting.</td> </tr> <tr> <td>VCOM3 (D1h)</td> <td>VCM3[6:0], VDV3[4:0]</td> <td>VCOMH and VCOM amplitude setting.</td> </tr> <tr> <td>VCOM4 (D1h)</td> <td>VCM4[6:0], VDV4[4:0]</td> <td>VCOMH and VCOM amplitude setting.</td> </tr> <tr> <td>VCOM5 (D1h)</td> <td>VCM5[6:0], VDV5[4:0]</td> <td>VCOMH and VCOM amplitude setting.</td> </tr> <tr> <td>GAMMA(C8h)</td> <td>Gamma value</td> <td>Set gamma parameter</td> </tr> </tbody> </table>	Command	Register	Description	ID1 (E0h)	ID1[7:0]	LCD module/driver version	ID2 (E0h)	ID2[7:0]	LCD module/driver version	ID3 (E0h)	ID3[7:0]	LCD module/driver version	ID4 (E0h)	ID4[7:0]	LCD module/driver version	ID5 (E0h)	ID5[7:0]	LCD module/driver version	VCOM1 (D1h)	VCM1[6:0], VDV1[4:0]	VCOMH and VCOM amplitude setting.	VCOM2 (D1h)	VCM2[6:0], VDV2[4:0]	VCOMH and VCOM amplitude setting.	VCOM3 (D1h)	VCM3[6:0], VDV3[4:0]	VCOMH and VCOM amplitude setting.	VCOM4 (D1h)	VCM4[6:0], VDV4[4:0]	VCOMH and VCOM amplitude setting.	VCOM5 (D1h)	VCM5[6:0], VDV5[4:0]	VCOMH and VCOM amplitude setting.	GAMMA(C8h)	Gamma value	Set gamma parameter
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	VCOM5 (D1h)	VCM5[6:0], VDV5[4:0]	VCOMH and VCOM amplitude setting.																																		
GAMMA(C8h)	Gamma value	Set gamma parameter																																			
5	Set OTP_KEY[7:0] (RE3h)=0xAAh to enter OTP program mode.																																				
6	Specify OTP_index																																				
	<table border="1"> <thead> <tr> <th>OTP_index (Write – For Program)</th> <th>OTP_index (Read – For get OTP value)</th> <th>Parameter</th> </tr> </thead> <tbody> <tr> <td>0x00h</td> <td>0x00h</td> <td>VALID_ID1, VALID_ID2, VALID_ID3, VALID_ID4, VALID_ID5</td> </tr> <tr> <td>0x01h</td> <td>0x01h</td> <td rowspan="4">ID1[7:0]</td> </tr> <tr> <td>0x02h</td> <td>0x02h</td> </tr> <tr> <td>0x03h</td> <td>0x03h</td> </tr> <tr> <td>0x04h</td> <td>0x04h</td> </tr> <tr> <td>0x15h</td> <td>0x15h</td> <td>VALID_VCM1, VCM1[6:0], VDV1[4:0]</td> </tr> <tr> <td>0x16h</td> <td>0x16h</td> <td rowspan="2">VALID_GAMMA, Gamma value</td> </tr> <tr> <td>0x35h ~ 0x40h</td> <td>0x35h ~ 0x40h</td> </tr> </tbody> </table>	OTP_index (Write – For Program)	OTP_index (Read – For get OTP value)	Parameter	0x00h	0x00h	VALID_ID1, VALID_ID2, VALID_ID3, VALID_ID4, VALID_ID5	0x01h	0x01h	ID1[7:0]	0x02h	0x02h	0x03h	0x03h	0x04h	0x04h	0x15h	0x15h	VALID_VCM1, VCM1[6:0], VDV1[4:0]	0x16h	0x16h	VALID_GAMMA, Gamma value	0x35h ~ 0x40h	0x35h ~ 0x40h													
	OTP_index (Write – For Program)	OTP_index (Read – For get OTP value)	Parameter																																		
	0x00h	0x00h	VALID_ID1, VALID_ID2, VALID_ID3, VALID_ID4, VALID_ID5																																		
	0x01h	0x01h	ID1[7:0]																																		
	0x02h	0x02h																																			
	0x03h	0x03h																																			
	0x04h	0x04h																																			
0x15h	0x15h	VALID_VCM1, VCM1[6:0], VDV1[4:0]																																			
0x16h	0x16h	VALID_GAMMA, Gamma value																																			
0x35h ~ 0x40h	0x35h ~ 0x40h																																				
7	Set OTP_Mask=0x00h, programming the entire bit of one parameter.																																				
8	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.																																				
9	Wait 1 ms																																				
10	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (5). Otherwise, set OTP_KEY[7:0]=0x55h to leave OTP program mode and power off the module and remove the external power on PVSS pin.																																				

Note: Set OTP_KEY[7:0] can be ignored when user want to do OTP program.

5.14.4 OTP Read flow

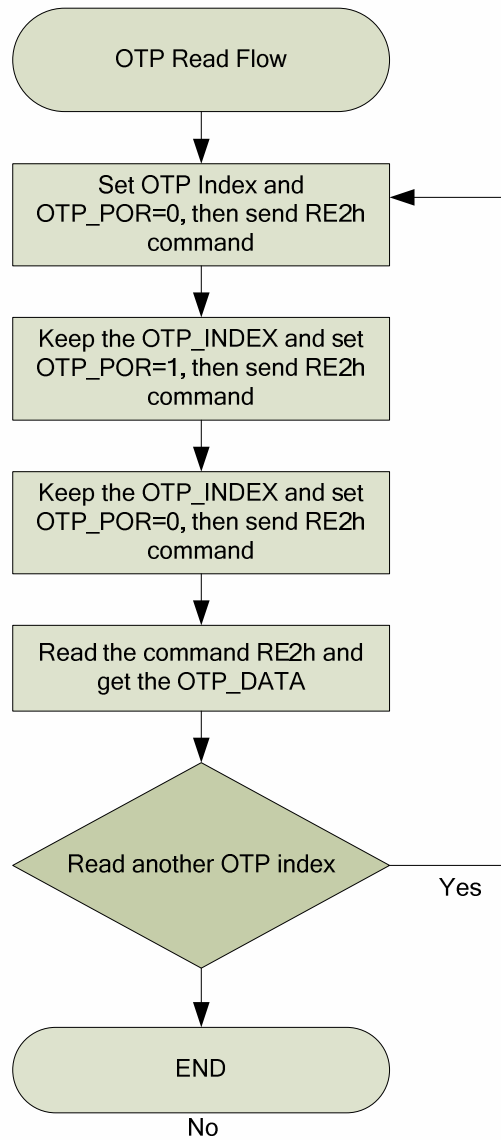
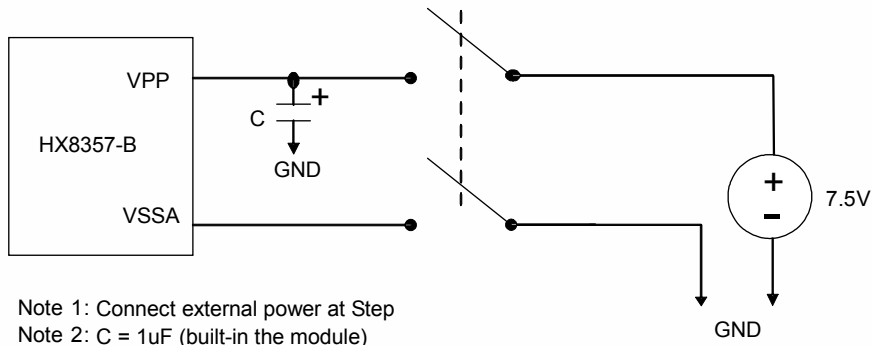


Figure 5.45: OTP Read Sequence

5.14.5 Programming circuitry



Note 1: Connect external power at Step
Note 2: C = 1uF (built-in the module)

6. Command

6.1 Standard Command List

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
00	NOP	0	↑	1	-	0	0	0	0	0	0	0	0	No Operation	Y	Y
01	SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	Software reset	Y	Y
06	RDRED	0	↑	1	-	0	0	0	0	0	1	1	0	Read Red	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	R7	R6	R5	R4	R3	R2	R1	R0	-		
07	RDGREEN	0	↑	1	-	0	0	0	0	0	1	1	1	Read Green	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	G7	G6	G5	G4	G3	G2	G1	G0	-		
08	RDBLUE	0	↑	1	-	0	0	0	0	1	0	0	0	Read Blue	N	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	B7	B6	B5	B4	B3	B2	B1	B0	-		
0A	RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	Read Display Power Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]							-			
0B	RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	Read Display MADCTL	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]							-			
0C	RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	Read Display Pixel Format	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	x	D6	D5	D4	x	D2	D1	D0	-		
0D	RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	Read Display Image Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]							-			
0E	RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	Read Display Signal Mode	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]							-			
0F	RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	Read Display Self-Diagnostic Result	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	D[7:0]							-			
10	SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	Sleep in and charge-pump off	Y	Y
11	SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	Sleep out and charge-pump on	Y	Y
12	PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	Partial Mode On	Y	N
13	NORON	0	↑	1	-	0	0	0	1	0	0	1	1	Normal Display Mode On	Y	N

(Hex)	Operation Code	DCX	WRX	RDX	D17 ~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
20	INVOFF	0	↑	1	-	0	0	1	0	0	0	0	1	Display Inversion off	Y	Y
21	INVON	0	↑	1	-	0	0	1	0	0	0	1	0	Display Inversion on	Y	Y
28	DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	Display off	Y	Y
29	DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	Display on	Y	Y
2A	CASET	0	↑	1	-	0	0	1	0	1	0	1	0	Column Address Set	Y	N
		1	↑	1	-	SC[15:8] (8'b0)								Column address start		
		1	↑	1	-	SC[7:0] (8'b0)								Column address start		
		1	↑	1	-	EC[15:8] (8'b0000_0001)								Column address end		
		1	↑	1	-	EC[7:0] (8'b0011_1111)								Column address end		
2B	PASET	0	↑	1	-	0	0	1	0	1	0	1	1	Row address set	Y	N
		1	↑	1	-	SP[15:8] (8'b0)								Row address start		
		1	↑	1	-	SP[7:0] (8'b0)								Row address start		
		1	↑	1	-	EP[15:8] (8'b0000_0001)								Row address end		
		1	↑	1	-	EP[7:0] (8'b1101_1111)								Row address end		
2C	RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	Memory write	Y	N
		1	↑	1	-	Write data								-		
2E	RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	Memory read	Y	N
		1	↑	1	-	-	-	-	-	-	-	-	-	-		
30	PLTAR	1	1	↑	-	Read data								-	Y	N
		0	↑	1	-	0	0	1	1	0	0	0	0	Partial address set		
		1	↑	1	-	SR[15:8] (8'b0)								Start row		
		1	↑	1	-	SR[7:0] (8'b0)								Start row		
		1	↑	1	-	ER[15:8] (8'b0000_0001)								End row		
1	↑	1	-	ER[7:0] (8'b1101_1111)								End row				
33	VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	Vertical Scrolling Definition)	Y	N
		1	↑	1	-	TFA[15:8] (8'b0)								Top Fixed Area		
		1	↑	1	-	TFA[7:0] (8'b0)								Top Fixed Area		
		1	↑	1	-	VSA[15:8] (8'b0000_0001)								Height of the Vertical Scrolling Area		
		1	↑	1	-	VSA[7:0] (8'b1101_1111)								Height of the Vertical Scrolling Area		
		1	↑	1	-	BFA[15:8] (8'b0)								Bottom Fixed Area		
		1	↑	1	-	BFA[7:0] (8'b0)								Bottom Fixed Area		

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement		
															DM[1:0]		
															00,01,10	11	
34	TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	Tearing Effect line off	Y	N	
35	TEON	0	↑	1	-	0	0	1	1	0	1	0	1	Tearing Effect Line ON	Y	N	
		0	↑	1	-	-	-	-	-	-	-	-	-	TEMODE			-
36	MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	Memory Access Control)	Y	Y	
		1	↑	1	-	MY (0)	MX (0)	MV (0)	ML (0)	BGR (0)	0	SS (0)	GS (0)	-			
37	VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	Vertical Scrolling Start Address	Y	N	
		1	↑	1	-	VSP[15:8] (8'b0)								-			
		1	↑	1	-	VSP[7:0] (8'b0)								-			
38	IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	Idle mode off	Y	N	
39	IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	Idle mode on	Y	N	
3A	COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	Interface Pixel Format	Y	Y	
		1	↑	1	-	0	D[6:4]			0	D[2:0]			-			
3C	RAMWRCON	0	↑	1	-	0	0	1	1	1	1	0	0	Memory write	Y	N	
		1	↑	1	-	Write data								-			
3E	RAMRDCON	0	↑	1	-	0	0	1	1	1	1	1	0	Memory read	Y	N	
		1	↑	1	-	-	-	-	-	-	-	-	-	-			Dummy read
		1	↑	1	-	Read data								-			
44	TESL	0	↑	1	-	0	1	0	0	0	1	0	0	Set tear scan line	Y	N	
		1	↑	1	-	TELINE[15:8] (8'b0)								-			
		1	↑	1	-	TELINE[7:0] (8'b0)								-			
45	GETSL	0	↑	1	-	0	1	0	0	0	1	0	1	Get the current scan line.	Y	N	
		1	↑	1	-	-	-	-	-	-	-	-	-	Dummy read			
		1	↑	1	-	SL[15:8]								-			
		1	↑	1	-	SL[7:0]								-			
A1	Read_DDB_start	0	↑	1	-	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	Y	Y	
		1	↑	1	-	-	-	-	-	-	-	-	-	Dummy read			
		1	↑	1	-	ID1								The five bytes always output			
		1	↑	1	-	ID2											
		1	↑	1	-	ID3											
		1	↑	1	-	ID4											
1	↑	1	-	8'hFF													

CABC command list

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Display mod Implementation Requirement	
															DM[1:0]	
															00,01,10	11
51	WRDISBV	0	↑	1	-	-	-	-	-	-	-	-	-	Write Display Brightness Value	Y	Y
		0	↑	1	-	DBV[7:0] (8'b0)								-		
52	RDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	Read Display Brightness Value	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	DBV[7:0]								-		
53	WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	Write Control Display	Y	Y
		1	↑	1	-	-	-	BCT RL (0)	-	DD (0)	BL (0)	-	-	-	-	
54	RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	Read Control Value Display	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	0	0	BCT RL	0	DD	BL	0	0	-		
55	WRCABC	0	↑	1	-	0	1	0	1	0	1	0	1	-	Y	Y
		1	↑	1	-	-	-	-	-	-	-	-	CABC[1:0] (00)	Write Adaptive Brightness Control		
56	RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	Read Content Adaptive Brightness Control	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	-	-	-	-	-	-	-	CABC[1:0]	-		
5E	WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	Write CABC minimum brightness	Y	Y
		1	↑	1	-	CMB[7:0]								-		
5F	RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	Read CABC minimum brightness	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	CMB[7:0]								-		
68	RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	Y	Y
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read		
		1	1	↑	-	-	-	-	-	-	-	-	-	-		

User Define Command List Table

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
B0	SETEXTC	0	↑	1	-	1	0	1	1	0	0	0	0	Set extended command
		1	↑	1	-	0	0	0	0	0	0	EXTC[1:0]		-
B1	SETDPSTB	0	↑	1	-	1	0	1	1	0	0	0	1	Set Deep standby mode
		1	↑	1	-	0	0	0	0	0	0	0	DP_STB	-
B3	SETGRAM	0	↑	1	-	1	0	1	1	0	0	1	1	Set GRAM access and Interface
		1	↑	1	-	0	0	0	0	0	0	0	0	-
		1	↑	1	-	0	0	0	0	0	TEI[2:0]		-	
		1	↑	1	-	0	0	0	0	DENC[3:0]		-		
B4	SETDISPLAY	0	↑	1	-	1	0	1	1	0	1	0	0	Set Display mode and GRAM write mode
		1	↑	1	-	0	0	0	RM	0	0	DM[1:0]		-
BF	GETDEVICEID	0	↑	1	-	1	0	1	1	1	1	1	1	Read Device ID
		1	1	↑	-	MIPI Alliance code								0x01
		1	1	↑	-	MIPI Alliance code								0x62
		1	1	↑	-	Device ID								0x83
		1	1	↑	-	Device ID								0x57
		1	1	↑	-	Device ID								0xFF
C0	SETPANEL	0	↑	1	-	1	1	0	0	0	0	0	0	Set Panel Driving
		1	↑	1	-	0	0	0	REV	SM	GS	0	0	-
		1	↑	1	-	0	0	NL[5:0]					-	
		1	↑	1	-	0	SCN[6:0]					-		
		1	↑	1	-	0	0	0	NDL	0	PTS[2:0]		-	
		1	↑	1	-	0	0	0	PTG	ISC[3:0]		-		
C1	SETNORTIME	0	↑	1	-	0	0	0	0	1	0	1	1	Set display timing for Normal mode
		1	↑	1	-	0	0	0	BC0	0	DIV0[1:0]		-	
		1	↑	1	-	0	0	0	RTN0[4:0]		-			
		1	↑	1	-	FP0[3:0]		BF0[3:0]			-			
C2	SETPARTIME	0	↑	1	-	1	1	0	0	0	0	1	0	Set display timing for Partial mode
		1	↑	1	-	0	0	0	BC1	0	DIV1[1:0]		-	
		1	↑	1	-	0	0	0	RTN1[4:0]		-			
		1	↑	1	-	FP1[3:0]		BF1[3:0]			-			
C3	SETIDLTIME	0	↑	1	-	1	1	0	0	0	0	1	1	Set display timing for Idle mode
		1	↑	1	-	0	0	0	BC2	0	DIV2[1:0]		-	
		1	↑	1	-	0	0	0	RTN2[4:0]		-			
C5	SETOSC	0	↑	1	-	1	1	0	0	0	1	0	1	Set display frame
		1	↑	1	-	0	0	0	UADJ[3:0]					-
C6	SETRGB	0	↑	1	-	1	1	0	0	0	0	0	0	Set RGB Interface
		1	↑	1	-	SDA_EN	0	0	VPL	HPL	0	EPL	DPL	-

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	
C8	SETGAMMA	0	↑	1	-	1	1	0	0	1	0	0	0	Set Gamma curve	
		1	↑	1	-	0	KP12	KP11	KP10	0	KP02	KP01	KP00	-	
		1	↑	1	-	0	KP32	KP31	KP30	0	KP22	KP21	KP20	-	
		1	↑	1	-	0	KP52	KP51	KP50	0	KP42	KP41	KP40	-	
		1	↑	1	-	0	RP12	RP11	RP10	0	RP02	RP01	RP00	-	
		1	↑	1	-	0	0	0	0	VRP_03	VRP_02	VRP_01	VRP_00	-	
		1	↑	1	-	0	0	0	VRP_14	VRP_13	VRP_12	VRP_11	VRP_10	-	
		1	↑	1	-	0	KN12	KN11	KN10	0	KN02	KN01	KN00	-	
		1	↑	1	-	0	KN32	KN31	KN30	0	KN22	KN21	KN20	-	
		1	↑	1	-	0	KN52	KN51	KN50	0	KN42	KN41	KN40	-	
		1	↑	1	-	0	RN12	RN11	RN10	0	RN02	RN01	RN00	-	
D0	SETPOWER	0	↑	1	-	1	1	0	1	0	0	0	0	Set Power	
		1	↑	1	-	0	AP[2:0]			0	VC[2:0]			-	
		1	↑	1	-	0	PON	0	0	0	BT[2:0]			-	
		1	↑	1	-	0	0	0	0	VRH[3:0]			-		
D1	SETVCOM	0	↑	1	-	1	1	0	1	0	0	0	1	Set VCOM	
		1	↑	1	-	0	VCM[6:0]						-		
D2	SETNORPOW	1	↑	1	-	0	0	0	VDV[4:0]				-		
		0	↑	1	-	1	1	0	1	0	0	1	0	Set Power of Normal mode	
		1	↑	1	-	0	0	0	0	SAP0[2:0]			-		
D3	SETPARPOW	1	↑	1	-	0	DC10[2:0]			DC00[2:0]			-		
		0	↑	1	-	1	1	0	1	0	0	1	1	Set Power of Partial mode	
		1	↑	1	-	0	0	0	0	SAP1[2:0]			-		
D4	SETIDLPOW	1	↑	1	-	0	DC11[2:0]			DC01[2:0]			-		
		0	↑	1	-	1	1	0	1	0	1	0	0	Set Power of Idle mode	
		1	↑	1	-	0	0	0	0	SAP2[2:0]			-		
E0	SETID	1	↑	1	-	0	DC12[2:0]			DC02[2:0]			-		
		0	↑	1	-	1	1	1	0	0	0	0	0	Set ID	
		1	↑	1	-	ID1									-
		1	↑	1	-	ID2									-
		1	↑	1	-	ID3									-
E2	SETOTP	1	↑	1	-	ID4									-
		0	↑	1	-	1	1	1	0	0	0	1	0	Set OTP	
		1	↑	1	-	OTP_MASK[7:0]									-
		1	↑	1	-	OTP_INDEX[7:0]									-
		1	↑	1	-	OTP_L OAD_D ISABL E	OTP_ TEST	OTP_ POR	OTP_ PWE	OTP_PTM[1:0]	VPP_S EL	OTP_ PRO G	-		
E3	SETOTPKEY	1	↑	1	-	OTP_DATA[7:0]									-
		0	↑	1	-	1	1	1	0	0	0	1	1	Set OTP Key	
E4	SETCABC	1	↑	1	-	OTP_KEY[7:0]			-						
		0	↑	1	-	1	1	1	0	0	1	0	0	Set CABC Control	
		1	↑	1	-	0	SEL_PWMCLK[2:0]			SEL_GAIN [1:0]	INVPULS (1)	SEL_BLD UTY (1)	-		
1	↑	1	-	PWM_PERIOD[7:0]						-					
1	↑	1	-	0	DIM_FRAME[6:0]						-				

>> HX8357-B

320RGB x 480 dot, 262K color, TFT Mobile Single Chip Driver



DATA SHEET Preliminary V01

(Hex)	Operation Code	DCX	WRX	RDX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
E9	SETPANEL	0	↑	1	-	1	1	1	0	1	0	0	1	Set Panel related register
		1	↑	1	-	0	0	0	0	SS_PANEL	0	0	BGR_PANEL	-
EE	SETEQ	0	↑	1	-	1	1	1	0	1	1	1	0	Set EQ function
		1	↑	1	-	EQVCI_M1[7:0]							-	
		1	↑	1	-	EQGND_M1[7:0]							-	
		1	↑	1	-	EQVCI_M0[7:0]							-	
		1	↑	1	-	EQGND_M0[7:0]							-	

6.2 Command Description

6.2.1 NOP

00H	NOP (No Operation)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00
Parameter	No Parameter												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.												
Restriction													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Sleep In or Booster Off						Yes						
	Status						Default Value						
	Power On Sequence						N/A						
	S/W Reset						N/A						
Flow Chart	H/W Reset						N/A						

6.2.2 Software Reset (01h)

01 H	SWRESET (Software Reset)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01
Parameter	No Parameter												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command It will be necessary to wait 5msec before sending new command following software reset.												
Restriction	The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						N/A						
	S/W Reset						N/A						
	H/W Reset						N/A						
Flow Chart													

6.2.3 Get_red_channel (06h)

06 H	RDRED (Read Red Colour)												
	DCX	NRD	NWR	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	0	06
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												
Register Availability	Status						Availability						
	Sleep Out						Yes						
	Sleep In						Yes						
Default	Status						Default Value						
	Power On Sequence						00h						
	S/W Reset						00h						
	H/W Reset						00h						
Flow Chart	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p style="text-align: center;">Serial I/F Mode</p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">RDBLUE (06h)</div> <p style="text-align: center;">↓</p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">Send D[7:0]</div> </div> <div style="width: 45%; border-left: 1px dashed black; padding-left: 10px;"> <p style="text-align: center;">Host</p> <hr style="border: 0.5px dashed black;"/> <p style="text-align: center;">Driver</p> </div> </div> <div style="margin-top: 20px;"> <p>Legend</p> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Command</div> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Parameter</div> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Display</div> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Action</div> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Mode</div> <div style="border: 1px solid black; padding: 5px; width: 100px; margin-bottom: 10px;">Sequential transfer</div> </div>												

6.2.4 Get_green_channel (07h)

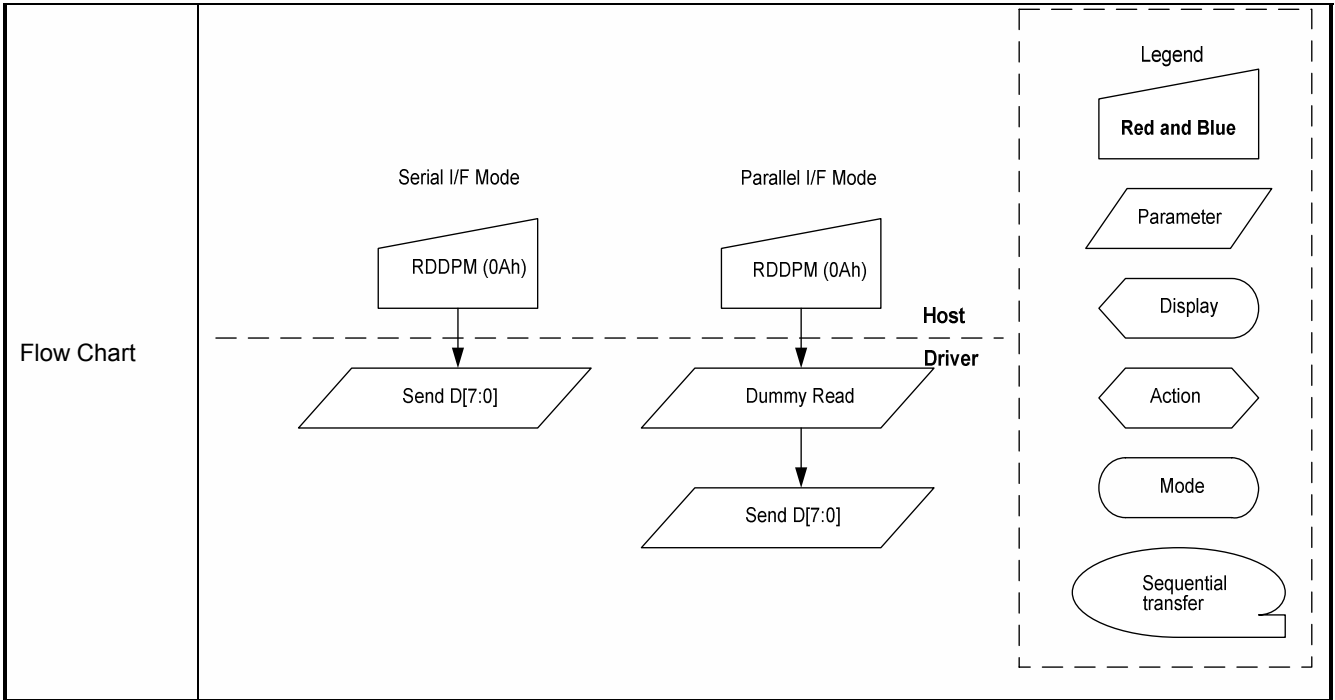
07 H	RDGREEN (Read Green Colour)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	1	01
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used DPI I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												
Register Availability	Status						Availability						
	Sleep Out						Yes						
	Sleep In						Yes						
Default	Status						Default Value						
	Power On Sequence						00h						
	S/W Reset						00h						
	H/W Reset						00h						
Flow Chart	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Serial I/F Mode</p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">RDBLUE (07h)</div> <p style="text-align: center;">↓</p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">Send D[7:0]</div> </div> <div style="width: 45%; border-left: 1px dashed black; padding-left: 10px;"> <p>Legend</p> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Command</div> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Parameter</div> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Display</div> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Action</div> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Mode</div> <div style="border: 1px solid black; padding: 5px; width: 60px; margin: 5px auto;">Sequential transfer</div> </div> </div> <div style="margin-top: 10px; text-align: center;"> Host Driver </div>												

6.2.5 Get_blue_channel (08h)

08 H	RDBLUE (Read Blue Colour)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	0	0	08
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.												
Restriction	The command is active when DM[1:0]="11"												
Register Availability	Status						Availability						
	Sleep Out						Yes						
	Sleep In						Yes						
Default	Status						Default Value						
	Power On Sequence						00h						
	S/W Reset						00h						
	H/W Reset						00h						
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <div style="border: 1px solid black; padding: 5px; width: 100px; margin: 0 auto;">RDBLUE (08h)</div> <p>↓</p> <div style="border: 1px solid black; padding: 5px; width: 150px; margin: 0 auto;">Send D[7:0]</div> </div> <div style="border-left: 1px dashed black; border-right: 1px dashed black; padding: 0 10px;"> <p style="text-align: center;">Host Driver</p> </div> <div style="border: 1px dashed black; padding: 10px; width: 200px;"> <p>Legend</p> <div style="margin-bottom: 5px;">Command</div> <div style="margin-bottom: 5px;">Parameter</div> <div style="margin-bottom: 5px;">Display</div> <div style="margin-bottom: 5px;">Action</div> <div style="margin-bottom: 5px;">Mode</div> <div style="margin-bottom: 5px;">Sequential transfer</div> </div> </div>												

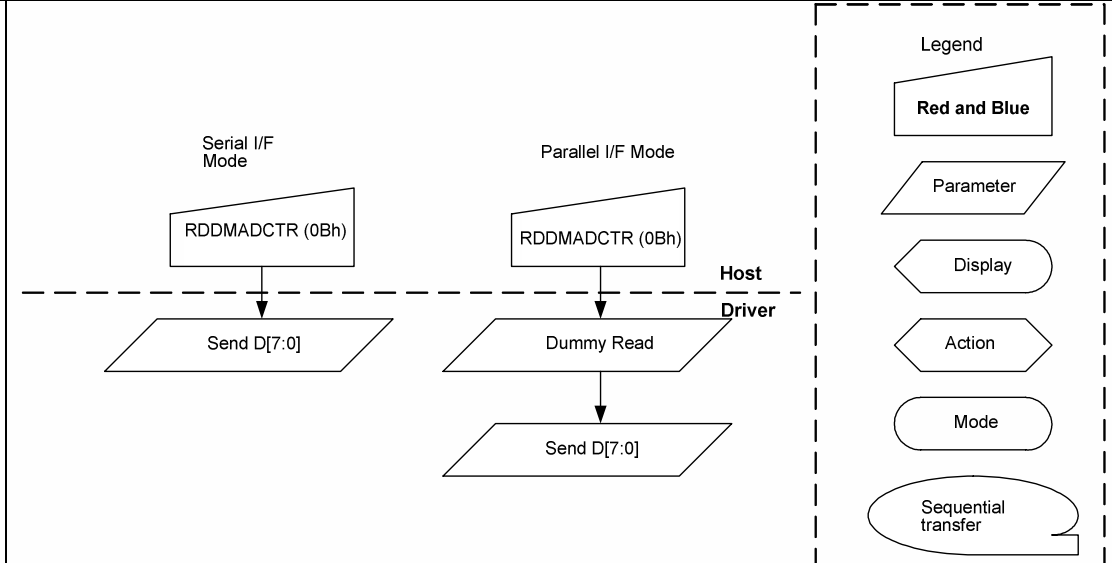
6.2.6 Get_power_mode (0Ah)

0A H	RDDPM (Read Display Power Mode)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	0	0A
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	0	0	xx
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description										Comment	
	D7	Not Defined										Set to '0'	
	D6	Idle Mode On/Off											
	D5	Partial Mode On/Off											
	D4	Sleep In/Out											
	D3	Display Normal Mode On/Off											
	D2	Display On/Off											
	D1	Not Defined										Set to '0'	
	D0	Not Defined										Set to '0'	
Bits D7 for future use and are set to '0'. Bit D6 – Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On. Bit D5 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On. Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode. Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On. Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On.													
Restrictions													
Register Availability	Status											Availability	
	Normal Mode On, Idle Mode Off, Sleep Out											Yes	
	Normal Mode On, Idle Mode On, Sleep Out											Yes	
	Partial Mode On, Idle Mode Off, Sleep Out											Yes	
	Partial Mode On, Idle Mode On, Sleep Out											Yes	
	Sleep In or Booster Off											Yes	
Default	Status											Default Value	
	Power On Sequence											08HEX	
	S/W Reset											08HEX	
	H/W Reset											08HEX	



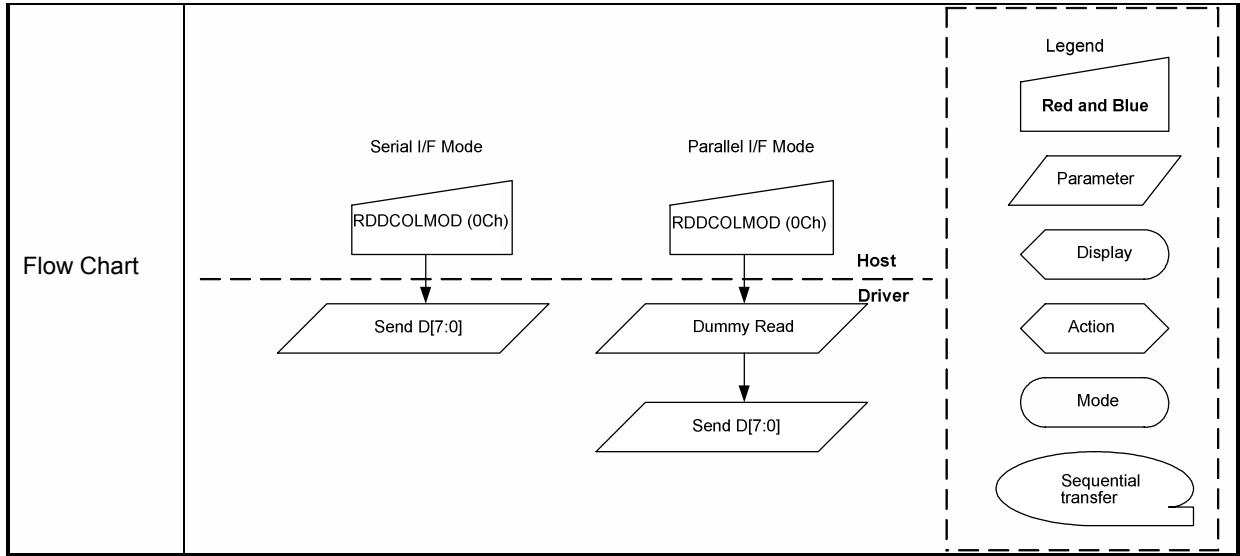
6.2.7 Read Display MADCTL (0Bh)

0B H	RDDMADCTL (Read Display MADCTL)												HEX																										
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0																											
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B																										
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read																										
2 nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	0	D1	D0	xx																										
Description	This command indicates the current status of the display as described in the table below:																																						
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Page Address Order</td> <td></td> </tr> <tr> <td>D6</td> <td>Column Address Order</td> <td></td> </tr> <tr> <td>D5</td> <td>Page/Column Order</td> <td></td> </tr> <tr> <td>D4</td> <td>Line Address Order</td> <td></td> </tr> <tr> <td>D3</td> <td>RGB/BGR Order</td> <td></td> </tr> <tr> <td>D2</td> <td>Reserved</td> <td>Set to '0'</td> </tr> <tr> <td>D1</td> <td>Flip Horizontal</td> <td></td> </tr> <tr> <td>D0</td> <td>Flip Vertical</td> <td></td> </tr> </tbody> </table> <p>Bit D7 – Page Address Order '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').</p> <p>Bit D6 – Column Address Order '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').</p> <p>Bit D5 – Page/Column Order '0' = Normal (When MADCTL B5='0'). '1' = Rotation (When MADCTL B5='1'). Note: For Bits D7 to D5, also refer to Section 5.1.3 MCU to memory write/read direction.</p> <p>Bit D4 – Line Address Order '0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').</p> <p>Bit D3 – RGB/BGR Order '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1'). Note: For Bits D4 and D3 also refer to 9.2.29 Set_address_mode (36h).</p> <p>Bit D2 is for future use and is set to '0'.</p> <p>Bit D1 – Flip Horizontal This bit flips the image shown on the display device left to right. No change is made to the frame memory. '0' = Normal '1' = Flipped</p> <p>Bit D0 – Flip Vertical This bit flips the image shown on the display device top to bottom. No change is made to the frame memory. '0' = Normal</p>													Bit	Description	Comment	D7	Page Address Order		D6	Column Address Order		D5	Page/Column Order		D4	Line Address Order		D3	RGB/BGR Order		D2	Reserved	Set to '0'	D1	Flip Horizontal		D0	Flip Vertical
Bit	Description	Comment																																					
D7	Page Address Order																																						
D6	Column Address Order																																						
D5	Page/Column Order																																						
D4	Line Address Order																																						
D3	RGB/BGR Order																																						
D2	Reserved	Set to '0'																																					
D1	Flip Horizontal																																						
D0	Flip Vertical																																						
Restrictions																																							
Register Availability	Status					Availability																																	
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																	
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																	
	Partial Mode On, Idle Mode Off, Sleep Out					Yes																																	
	Partial Mode On, Idle Mode On, Sleep Out					Yes																																	
	Sleep In or Booster Off					Yes																																	

Default	Status	Default Value
	Power On Sequence	00HEX
	S/W Reset	No Change
Flow Chart	 <p>The flow chart is divided into two sections by a dashed line labeled 'Host' on the left and 'Driver' on the right. Serial I/F Mode: A trapezoidal box labeled 'RDDMADCTR (0Bh)' has an arrow pointing down to a parallelogram box labeled 'Send D[7:0]'. Parallel I/F Mode: A trapezoidal box labeled 'RDDMADCTR (0Bh)' has an arrow pointing down to a parallelogram box labeled 'Dummy Read', which then has an arrow pointing down to another parallelogram box labeled 'Send D[7:0]'. Legend: A dashed box on the right contains several symbols: a trapezoid for 'Red and Blue', a parallelogram for 'Parameter', a rounded rectangle for 'Display', a hexagon for 'Action', an oval for 'Mode', and a speech bubble for 'Sequential transfer'.</p>	

6.2.8 Get_pixel_format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)												HEX
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	-	0	0	0	0	1	1	0	0	0C
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1		-	D6	D5	D4	-	D2	D1	D0	xx
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description										Comment	
	D7	Reserved										Set to '0'	
	D6	DPI Interface Pixel format											
	D5												
	D4												
	D3	Reserved										Set to '0'	
	D2	DBI Interface Pixel format											
	D1												
	D0												
Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition. See section “6.2.33 Set_pixel_format (3Ah)”.													
Interface Colour Format				D6/D2	D5/D1	D4/D0							
Not Defined				0	0	0							
3 bit/pixel				0	0	1							
Not Defined				0	1	0							
Not Defined				0	1	1							
Not Defined				1	0	0							
16 bit/pixel				1	0	1							
18 bit/pixel				1	1	0							
Not Defined				1	1	1							
If a particular interface, either DBI or DPI, is not used then the corresponding bits in the													
Restrictions													
Register Availability	Status					Availability							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes							
	Normal Mode On, Idle Mode On, Sleep Out					Yes							
	Partial Mode On, Idle Mode Off, Sleep Out					Yes							
	Partial Mode On, Idle Mode On, Sleep Out					Yes							
Sleep In or Booster Off					Yes								
Default	Status					Default Value							
	Power On Sequence					66HEX							
	S/W Reset					66HEX							



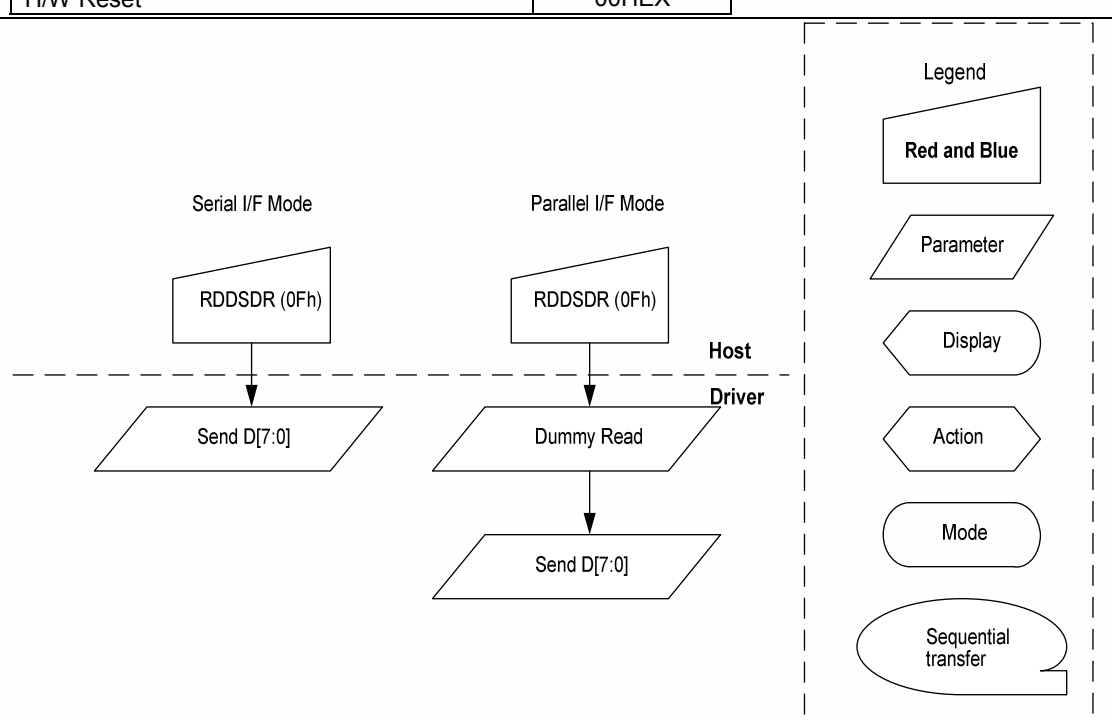
6.2.9 Get_display_mode (0Dh)

0D H	RDDIM (Read Display Image Mode)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	1	0D
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	D7	0	D5	0	0	D2	D1	D0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off ‘0’ = Vertical Scrolling is Off. ‘1’ = Vertical Scrolling is On. Bit D6 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to ‘0’ Bit D5 – Inversion On/Off ‘0’ = Inversion is Off. ‘1’ = Inversion is On. Bit D4 – Reserved Bit D3 – Reserved Bits D2, D1, D0 – Gamma Curve Selection These bit are not applicable for this project, so they are set to ‘000’												
Restrictions													
Register Availability	status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						00HEX						
	S/W Reset						00HEX						
	H/W Reset						00HEX						
Flow Chart													

6.2.10 Get_signal_mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	↑	1	-	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off ‘0’ = Tearing Effect Line Off. ‘1’ = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 7.1 for mode definitions. ‘0’ = Mode 1. ‘1’ = Mode 2. D5 are D0 – are for future use and are set to ‘0’.												
Restrictions													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						00HEX						
	S/W Reset						00HEX						
Flow Chart	<div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Red and Blue Parameter Display Action Mode Sequential transfer </div>												

6.2.11 Get_diagnostic_result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2 nd parameter	1	1	1	-	D7	D6	D5	D4	0	0	0	0	xx
Description	The display module returns the self-diagnostic results following a Sleep Out command. See section 7.10 for a description of the status results. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved Set to '0'.												
Restrictions													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						00HEX						
	S/W Reset						00HEX						
	H/W Reset						00HEX						
Flow Chart	 <p>The flow chart illustrates the sequence of operations for the RDDSDR (0Fh) command. It is divided into two modes: Serial I/F Mode and Parallel I/F Mode. A dashed line separates the Host (top) from the Driver (bottom). In Serial I/F Mode, the Host sends the RDDSDR (0Fh) command, and the Driver responds by sending the data D[7:0]. In Parallel I/F Mode, the Host sends the RDDSDR (0Fh) command, the Driver performs a Dummy Read, and then sends the data D[7:0]. A legend on the right defines the symbols used: a trapezoid for Red and Blue, a parallelogram for Parameter, a rounded rectangle for Display, a hexagon for Action, a rounded rectangle for Mode, and a speech bubble for Sequential transfer.</p>												

6.2.12 Enter_sleep_mode (10h)

10 H	SLPIN (Sleep In)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p>												
	<p>MCU interface and memory are still working and the memory keeps its contents.</p>												
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Sleep in mode						
	S/W Reset						Sleep in mode						
	H/W Reset						Sleep in mode						
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>												
	<p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Diamond Mode: Oval Sequential transfer: Circle with arrow 												

6.2.13 Exit_sleep_omde (11h)

11 H	SLPOUT (Sleep Out)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p>												
	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Sleep In Mode						
	S/W Reset						Sleep In Mode						
	H/W Reset						Sleep In Mode						
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p>												
	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

6.2.14 Enter_partial_mode (12h)

12 H	PTLON (Partial Mode On)													
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	-	0	0	0	1	0	0	1	0	12	
Parameter	No Parameter													
Description	This command turns on partial mode The partial mode window is described by the "Set_partial_area" command (30H). To leave Partial mode, the "Enter_norma_mode" command (13H) should be written.													
Restrictions	This command has no effect when Partial mode is active.													
Register Availability	Status							Availability						
	Normal Mode On, Idle Mode Off, Sleep Out							Yes						
	Normal Mode On, Idle Mode On, Sleep Out							Yes						
	Partial Mode On, Idle Mode Off, Sleep Out							Yes						
	Partial Mode On, Idle Mode On, Sleep Out							Yes						
Default	Status							Default Value						
	Power On Sequence							Normal Mode On						
	S/W Reset							Normal Mode On						
	H/W Reset							Normal Mode On						
Flow Chart	See Partial Area (30h)													

6.2.15 Enter_normal_mode (13h)

13 H	NORON (Normal Display Mode On)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Normal Mode On						
	S/W Reset						Normal Mode On						
	H/W Reset						Normal Mode On						
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

6.2.16 Exit_inversion_mode (20h)

20 H	INVOFF (Display Inversion Off)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												
Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em;">➔</div> <div style="text-align: center;"> <p>Display</p> </div> </div>												
Restriction	This command has no effect when module is already in inversion off mode.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						Display Inversion off						
	S/W Reset						Display Inversion off						
	H/W Reset						Display Inversion off						
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

6.2.17 Enter_inversion_mode (21h)

21 H	INVON (Display Inversion On)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												
Description	<p>This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; justify-content: center; align-items: center;"> <div style="text-align: center;"> <p>memory</p> </div> <div style="margin: 0 20px;">→</div> <div style="text-align: center;"> <p>display</p> </div> </div>												
Restriction	This command has no effect when module is already in inversion on mode.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Display Inversion off						
	S/W Reset						Display Inversion off						
	H/W Reset						Display Inversion off						
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Display Inversion OFF Mode]) --> B[INVON] B --> C([Display Inversion ON Mode]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / Display: [] Action: < Mode: [] Sequential transfer: [] </div> </div>												

6.2.18 Set_display_off (28h)

28H	DISPOFF (Display Off)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.</p> <p style="text-align: center;">Example</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div>												
Restriction	This command has no effect when module is already in display off mode.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Display off						
	S/W Reset						Display off						
	H/W Reset						Display off						
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[Display On Mode] --> B[DISPOFF] B --> C[Display Off Mode] </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none"> Command: [Rectangle] Parameter: [Trapezoid] Display: [Hexagon] Action: [Arrow] Mode: [Oval] Sequential transfer: [Callout box] </div> </div>												

6.2.19 Set_display_on (29h)

29 H	DISPON (Display On)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em;">➔</div> <div style="text-align: center;"> <p>Display</p> </div> </div>												
Restriction	This command has no effect when module is already in display on mode.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In or Booster Off						Yes							
Default	Status						Default Value						
	Power On Sequence						Display off						
	S/W Reset						Display off						
	H/W Reset						Display off						
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([Display Off Mode]) --> B[DISPON] B --> C([Display On Mode]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

6.2.20 Set_column_address (2Ah)

2A H	CASET (Column Address Set)																								
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	1	0	1	0	2A												
1 st parameter	1	1	↑	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00..												
2 nd parameter	1	1	↑	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Note 1												
3 rd parameter	1	1	↑	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	00..												
4 th parameter	1	1	↑	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Note 1												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p> <p>(Example)</p>																								
Restriction	<p>SC[15:0] always must be equal to or less than EC[15:0] Note 1: When SC[15:0] or EC[15:0] is greater than horizontal line (when MADCTL's B5=0) or vertical line (when MADCTL's B5=1), data of out of range will be ignored.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SC[15:0]=0000 The frame memory Column addresses corresponding to the last vertical line.</td> </tr> <tr> <td rowspan="3">S/W Reset</td> <td>When MADCTL's B5=0: SC[15:0]=0000 The frame memory column addresses corresponding to the last vertical line.</td> </tr> <tr> <td>When MADCTL's B5=1: SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.</td> </tr> <tr> <td>SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.</td> </tr> <tr> <td>H/W Reset</td> <td>SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	SC[15:0]=0000 The frame memory Column addresses corresponding to the last vertical line.	S/W Reset	When MADCTL's B5=0: SC[15:0]=0000 The frame memory column addresses corresponding to the last vertical line.	When MADCTL's B5=1: SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.	SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.	H/W Reset	SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.		
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	SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.																								
H/W Reset	SC[15:0]=0000 The frame memory column addresses corresponding to the last horizontal line.																								
Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Arrow pointing left Action: Arrow pointing right Mode: Oval Sequential transfer: Curved arrow <p>If needed</p>																								

6.2.21 Set_page_address (2Bh)

2B H	PASET (Page Address Set)																										
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	-	0	0	1	0	1	0	1	1	2B														
1 st parameter	1	1	↑	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00 ...														
2 nd parameter	1	1	↑	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Note 1														
3 rd parameter	1	1	↑	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	00 ...														
4 th parameter	1	1	↑	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Note 1														
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory. (Example)</p>																										
Restriction	<p>SP[15:0] always must be equal to or less than EP[15:0] Note 1: When SP[15:0] or EP[15:0] is greater than vertical line (When MADCTL's B5=0) or horizontal line (When MADCTL's B5=1), data of out of range will be ignored.</p>																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes				
Status	Availability																										
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Status	Default Value																										
Power On Sequence	SP[15:0]=0000	The frame memory page addresses corresponding to the last horizontal line.																									
S/W Reset	When MADCTL's B5=0: SP[15:0]=0000	When MADCTL's B5=0: The frame memory page addresses corresponding to the last horizontal line.																									
	When MADCTL's B5=1: SP[15:0]=0000	When MADCTL's B5=1: The frame memory page addresses corresponding to the last vertical line.																									
H/W Reset	SP[15:0]=0000	The frame memory page addresses corresponding to the last horizontal line.																									
Flow Chart																											

6.2.22 Write_memory_start (2Ch)

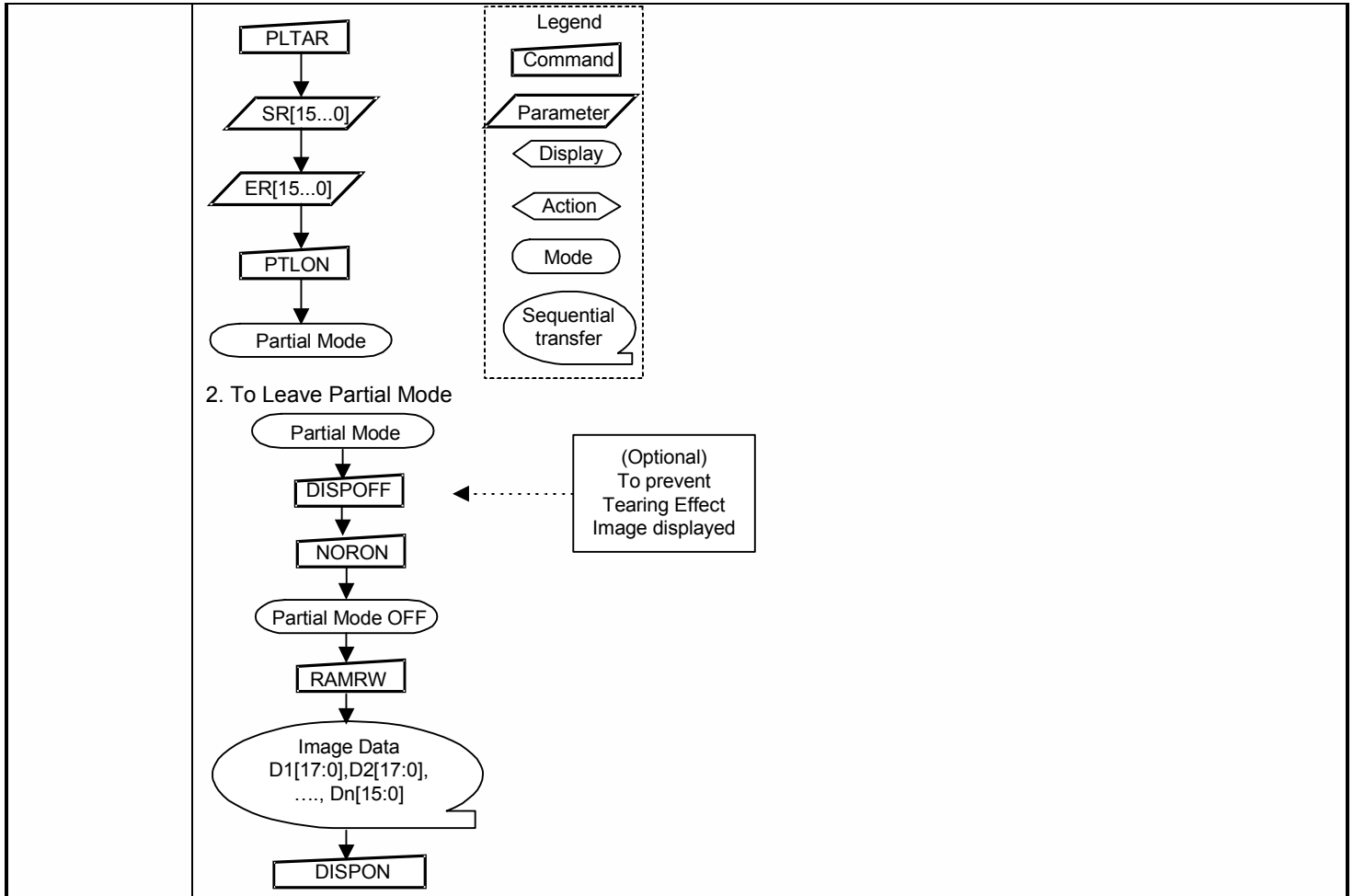
2C H	RAMWR (Memory Write)																						
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	-	0	0	1	0	1	1	0	0	2C										
1 st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF										
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF										
N th parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF										
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column register. Sending any other command can stop frame Write.																						
Restriction	In all colour modes, there is no restriction on length of parameters.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared				
Status	Default Value																						
Power On Sequence	Contents of memory is set randomly																						
S/W Reset	Contents of memory is not cleared																						
Flow Chart	<pre> graph TD RAMWR[RAMWR] --> ImageData([Image Data D1[7:0], D2[7:0], ..., Dn[7:0]]) ImageData --> AnyCommand[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: <> Action: <> Mode: () Sequential transfer: () 																						

6.2.23 Raed_memory_start (2Eh)

2E H	RAMRD (Memory Read)																								
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	1	1	1	0	2E												
1 st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read												
2 nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF												
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF												
(n+1) th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF												
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Frame Read can be stopped by sending any other command.																								
Restriction	In all colour modes, the Frame Read is always 24bit so there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is not cleared																								
H/W Reset	Contents of memory is not cleared																								
Flow Chart	<pre> graph TD A[RAMRD] --> B[/Dummy/] B --> C([Image Data D1[7:0], D2[7:0], ..., Dn[7:0]]) C --> D[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: [] Parameter: / / Display: <> Action: <> Mode: () Sequential transfer: () 																								

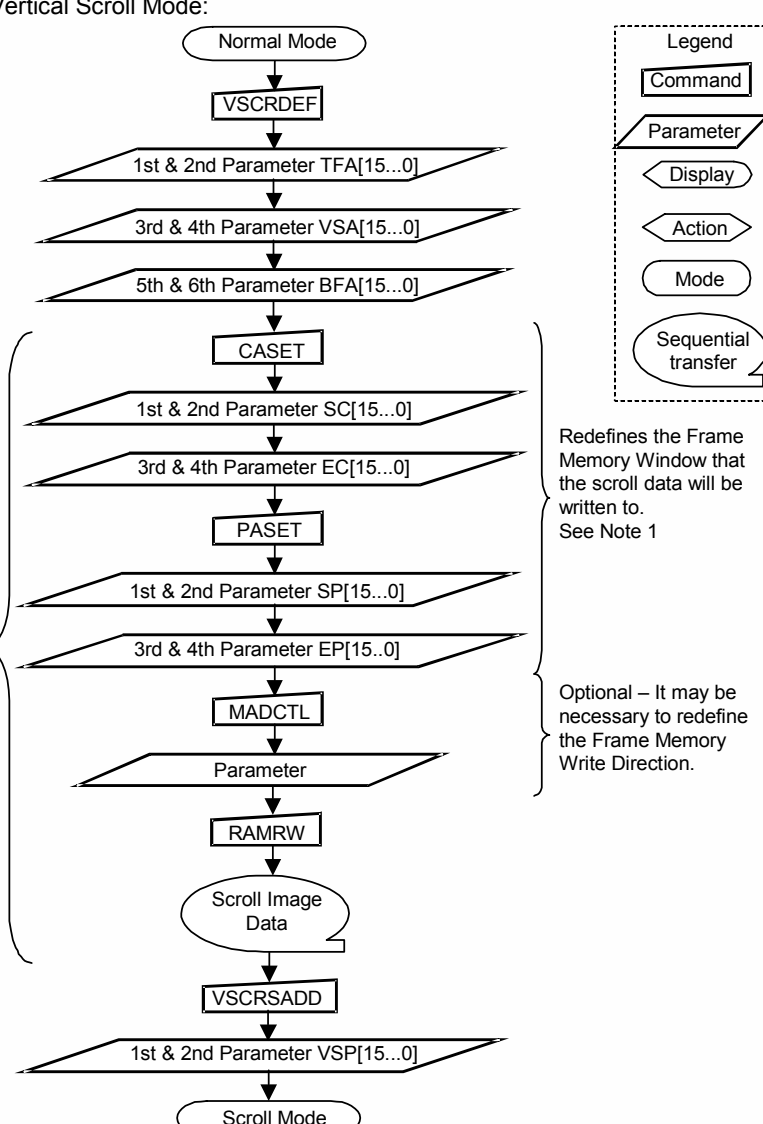
6.2.24 Set_partial_area (30h)

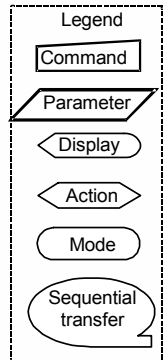
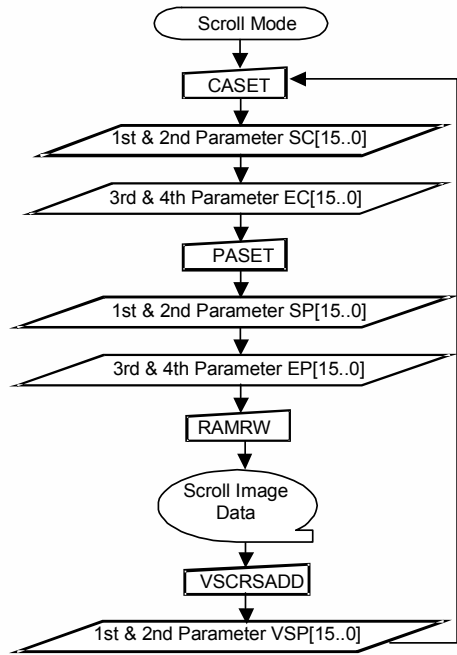
30 H	PLTAR (Partial Area)												HEX	
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	1	↑	-	0	0	1	1	0	0	0	0	30	
1 st Parameter	1	1	↑	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	xx	
2 nd Parameter	1	1	↑	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	xx	
3 rd Parameter	1	1	↑	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	xx	
4 th Parameter	1	1	↑	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	xx	
Description	<p>This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>If End Row > Start Row</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>MADCTL B4=0</p> </div> <div style="text-align: center;"> <p>MADCTL B4=1</p> </div> </div> <p>If End Row < Start Row</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>MADCTL B4=0</p> </div> <div style="text-align: center;"> <p>MADCTL B4=1</p> </div> </div> <p>If End Row = Start Row then the Partial Area will be one row.</p>													
	Restriction	SR[15:0] and ER[15:0] cannot exceed the last vertical line number.												
	Register Availability	Status												Availability
		Normal Mode On, Idle Mode Off, Sleep Out												Yes
		Normal Mode On, Idle Mode On, Sleep Out												Yes
Partial Mode On, Idle Mode Off, Sleep Out													Yes	
Default	Status												Default Value	
	Power On Sequence	SR[15..0]=00											ER[15..0]= Vertical line number	
	S/W Reset	SR[15..0]=00											ER[15..0]= Vertical line number	
	H/W Reset	SR[15..0]=00											ER[15..0]= Vertical line number	
Flow Chart	1. To Enter Partial Mode:-													



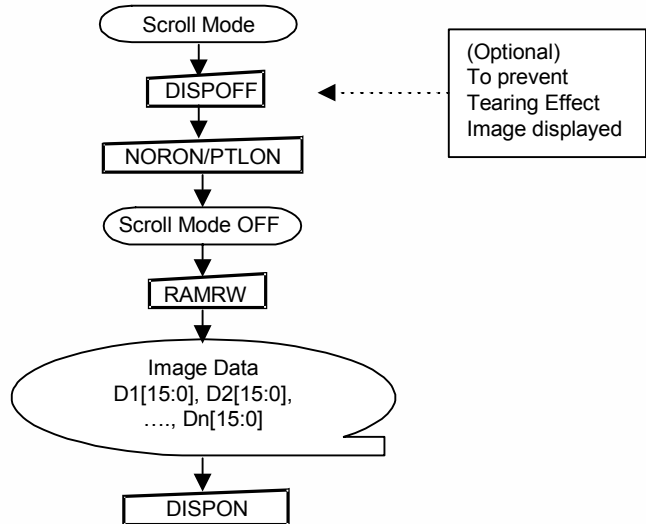
6.2.25 Set_scroll_area (33h)

33 H	VSCRDEF (Vertical Scrolling Definition)												HEX
Command	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	1	1	33
1 st parameter	1	1	↑	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	xx
2 nd parameter	1	1	↑	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	xx
3 rd parameter	1	1	↑	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	xx
4 th parameter	1	1	↑	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	xx
5 th parameter	1	1	↑	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	xx
6 th parameter	1	1	↑	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	xx
Description	<p>When MADCTL B4=0 The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>												
	<p>When MADCTL B4=1 The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>												
Restriction	The condition is (TFA+VSA+BFA)= Vertical line number, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						

	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes
Default	Status	Default Value
	Power On Sequence	TFA[15..0]=0000 VSA[15..0]= The frame memory page address corresponding to the last horizontal line. BFA[15..0]=0000
	SW Reset	TFA[15..0]=0000 VSA[15..0]= The frame memory page address corresponding to the last horizontal line. BFA[15..0]=0000
	H/W Reset	TFA[15..0]=0000 VSA[15..0]= The frame memory page address corresponding to the last horizontal line. BFA[15..0]=0000
Flow Charts	<p>1.To enter Vertical Scroll Mode:</p>  <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> <p style="margin-top: 10px;">Only required for nonrolling scrolling</p> <p style="margin-top: 10px;">Redefines the Frame Memory Window that the scroll data will be written to. See Note 1</p> <p style="margin-top: 10px;">Optional – It may be necessary to redefine the Frame Memory Write Direction.</p> <p style="margin-top: 10px;">Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.</p> <p>2. Continuous Scroll:</p>	



3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

6.2.26 Set_tear_off (34h)

34 H	TEOFF (Tearing Effect Line OFF)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Off						
	S/W Reset						Off						
	H/W Reset						Off						
Flow Chart	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <pre> graph TD A([TE Line Output ON]) --> B[TEOFF] B --> C([TE Line Output OFF]) </pre> </div> <div style="width: 50%;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

6.2.27 Set_tear_on (35h)

35 H	TEON (Tearing Effect Line ON)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care). When M=0: The Tearing Effect Output line consists of V-Blanking information only:</p> <p>When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>												
	Restriction	This command has no effect when Tearing Effect output is already ON.											
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						Off						
	S/W Reset						Off						
	H/W Reset						Off						
Flow Chart													
	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

6.2.28 Set_address_mode (36h)

36 H		MADCTL (Memory Access Control)											
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36
1 st parameter	1	1	↑	-	B7	B6	B5	B4	B3	0	B1	B0	XX

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

BIT	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2		LCD horizontal refresh direction control
B3	Horizontal Flip(SS)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B3	Vertical Flip(GS)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)

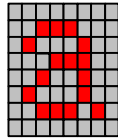
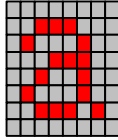
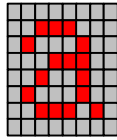
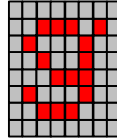
Description

ML – Vertical Updating order

Note: Top-Left (0, 0) means a physical memory location.

RGB-BGR Order

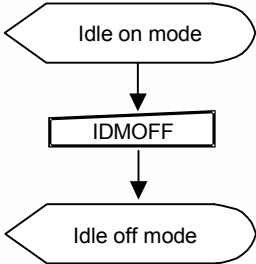
SS Horizontal Flip order

	<p style="text-align: center;">GS Vertical Flip order</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>GS=0</p>  <p>Memory</p>  <p>Display</p> </div> <div style="text-align: center;"> <p>GS=1</p>  <p>Memory</p>  <p>Display</p> </div> </div>	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes
Default	Status	Default Value
	Power On Sequence	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0
	S/W Reset	No Change
	H/W Reset	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0
Flow Chart	<p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; align-items: center;"> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Command</div> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Parameter</div> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Display</div> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Action</div> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Mode</div> <div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">Sequential transfer</div> </div> <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; padding: 5px; margin-right: 10px;">MADCTL</div> <div style="margin-right: 10px;">↓</div> <div style="border: 1px solid black; padding: 5px;">1st parameter B[7:0]</div> </div>	

6.2.29 Set_scroll_start (37h)

37 H	VSCRSADD (Vertical Scrolling Start Address)												HEX
Command	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	37
1 st parameter	1	1	↑	-	VSP	VSP	VSP	VSP	VSP	VSP	VSP	VSP	
2 nd parameter	0	1	↑	-	VSP	VSP	VSP	VSP	VSP	VSP	VSP	VSP	
Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP=3 (Example)</p> <p>When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP=3 (Example)</p>												
	<p>When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.</p>												
Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)), otherwise undesirable image will be displayed on the Panel.</p>												
Register Availability	Status		Availability										
	Normal Mode On, Idle Mode Off, Sleep Out		Yes										
	Normal Mode On, Idle Mode On, Sleep Out		Yes										
	Partial Mode On, Idle Mode Off, Sleep Out		No										
	Partial Mode On, Idle Mode On, Sleep Out		No										
	Sleep In or Booster Off		Yes										
Default	Status		Default Value										
	Power On Sequence		0000h										
	S/W Reset		0000h										
	H/W Reset		0000h										
Flow Chart	See Vertical Scrolling Definition (33h) description.												

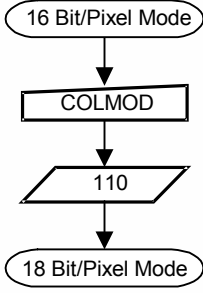
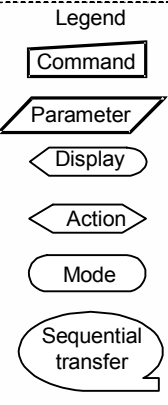
6.2.30 Exit_idle_mode (38h)

38 H	IDMOFF (Idle mode off)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262K colours.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						Idle off mode						
	S/W Reset						Idle off mode						
	H/W Reset						Idle off mode						
Flow Chart	 <pre> graph TD A[Idle on mode] --> B[IDMOFF] B --> C[Idle off mode] </pre>						<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 						

6.2.31 Enter_Idle_mode (39h)

39 H	IDMON (Idle mode on)																																																																																																																																																																																							
	DCX	RDX	WRX	DB15~DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	HEX																																																																																																																																																																											
Command	0	1	↑	-	0	0	1	1	1	0	0	1	39																																																																																																																																																																											
Parameter	No Parameter																																																																																																																																																																																							
Description	<p>This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.</p> <p>(Example)</p> <p>Memory contents vs. Display Colour</p> <table border="1"> <thead> <tr> <th></th> <th>R6</th> <th>R4</th> <th>R3</th> <th>R2</th> <th>R1</th> <th>R0</th> <th>G5</th> <th>G4</th> <th>G3</th> <th>G2</th> <th>G1</th> <th>G0</th> <th>B5</th> <th>B4</th> <th>B3</th> <th>B2</th> <th>B1</th> <th>B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td colspan="6">0XXXXX</td> <td colspan="6">0XXXXX</td> <td colspan="6">0XXXXX</td> </tr> <tr> <td>Blue</td> <td colspan="6">0XXXXX</td> <td colspan="6">0XXXXX</td> <td colspan="6">1XXXXX</td> </tr> <tr> <td>Red</td> <td colspan="6">1XXXXX</td> <td colspan="6">0XXXXX</td> <td colspan="6">0XXXXX</td> </tr> <tr> <td>Magenta</td> <td colspan="6">1XXXXX</td> <td colspan="6">0XXXXX</td> <td colspan="6">1XXXXX</td> </tr> <tr> <td>Green</td> <td colspan="6">0XXXXX</td> <td colspan="6">1XXXXX</td> <td colspan="6">0XXXXX</td> </tr> <tr> <td>Cyan</td> <td colspan="6">0XXXXX</td> <td colspan="6">1XXXXX</td> <td colspan="6">1XXXXX</td> </tr> <tr> <td>Yellow</td> <td colspan="6">1XXXXX</td> <td colspan="6">1XXXXX</td> <td colspan="6">0XXXXX</td> </tr> <tr> <td>White</td> <td colspan="6">1XXXXX</td> <td colspan="6">1XXXXX</td> <td colspan="6">1XXXXX</td> </tr> </tbody> </table> <p>X=don't care</p>														R6	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	Black	0XXXXX						0XXXXX						0XXXXX						Blue	0XXXXX						0XXXXX						1XXXXX						Red	1XXXXX						0XXXXX						0XXXXX						Magenta	1XXXXX						0XXXXX						1XXXXX						Green	0XXXXX						1XXXXX						0XXXXX						Cyan	0XXXXX						1XXXXX						1XXXXX						Yellow	1XXXXX						1XXXXX						0XXXXX						White	1XXXXX						1XXXXX						1XXXXX					
		R6	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0																																																																																																																																																																					
Black	0XXXXX						0XXXXX						0XXXXX																																																																																																																																																																											
Blue	0XXXXX						0XXXXX						1XXXXX																																																																																																																																																																											
Red	1XXXXX						0XXXXX						0XXXXX																																																																																																																																																																											
Magenta	1XXXXX						0XXXXX						1XXXXX																																																																																																																																																																											
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White	1XXXXX						1XXXXX						1XXXXX																																																																																																																																																																											
Restriction	This command has no effect when module is already in idle on mode.																																																																																																																																																																																							
Register Availability	Status						Availability																																																																																																																																																																																	
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																																																																																																																																																																																	
	Normal Mode On, Idle Mode On, Sleep Out						Yes																																																																																																																																																																																	
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																																																																																																																																																																																	
	Partial Mode On, Idle Mode On, Sleep Out						Yes																																																																																																																																																																																	
	Sleep In or Booster Off						Yes																																																																																																																																																																																	
Default	Status						Default Value																																																																																																																																																																																	
	Power On Sequence						Idle off mode																																																																																																																																																																																	
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	H/W Reset						Idle off mode																																																																																																																																																																																	
Flow Chart	<pre> graph TD A([Idle off mode]) --> B[IDMON] B --> C([Idle on mode]) </pre>																																																																																																																																																																																							
	<p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / Display: < Action: > Mode: () Sequential transfer: [] 																																																																																																																																																																																							

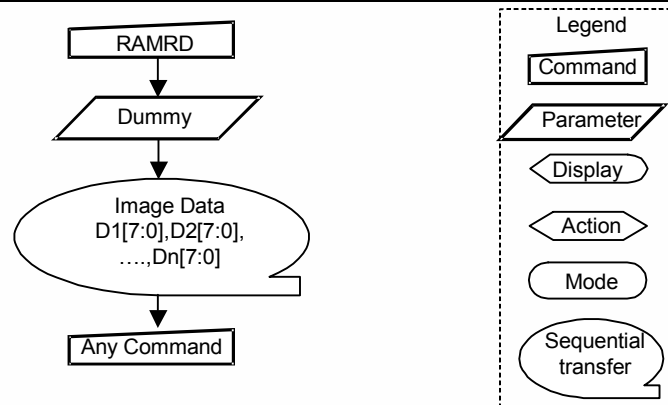
6.2.32 Set_pixel_format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	1	0	3A
1 st parameter	1	1	↑	-	X	D6	D5	D4	X	D2	D1	D0	XX
Description	This command is used to define the format of RGB picture data. D6~D4: DPI Pixel format Definition. D2~D0: DBI Pixel format Definition. The formats are shown in the table:												
	Pixel Format				D6/D2	D5/D1	D4/D0						
	Not Defined				0	0	0						
	3 Bit/Pixel				0	0	1						
	Not Defined				0	1	0						
	Not Defined				0	1	1						
	Not Defined				1	0	0						
	16 Bit/Pixel				1	0	1						
	18 Bit/Pixel				1	1	0						
	Not Defined				1	1	1						
If a particular interface, enter DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module undefined.													
Restriction	There is no visible effect until the Frame Memory is written to.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						18 Bit/Pixel						
	S/W Reset						18 Bit/Pixel						
	H/W Reset						18 Bit/Pixel						
Flow Chart													

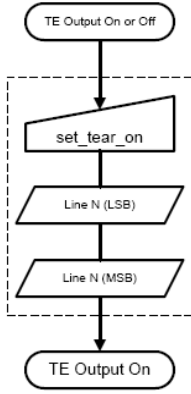
6.2.33 Write_memory_contiune (3Ch)

3C H		Write_memory_contiune											
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	0	0	3C
1 st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
N th parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_contiune or write_memory_start command. Sending any other command can stop frame Write.</p> <p>If set_address_mode B5 = 0: Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_contiune. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p> <p>If set_address_mode B5 = 1: Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_contiune. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p>												
Restriction	In all colour modes, there is no restriction on length of parameters.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status				Default Value								
	Power On Sequence				Contents of memory is set randomly								
	S/W Reset				Contents of memory is not cleared								
Flow Chart	<pre> graph TD RAMWR[RAMWR] --> ImageData[Image Data D1[7:0], D2[7:0], ..., Dn[7:0]] ImageData --> AnyCommand[Any Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: [] Parameter: / Display: <> Action: > Mode: () Sequential transfer: [] 												

6.2.34 Raed_memory_continue (3Eh)

3E H	Raed_memory_continue												HEX												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E												
1 st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read												
2 nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF												
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF												
(n+1) th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF												
Description	<p>This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.</p> <p>If set_address_mode B5 = 0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If set_address_mode B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>																								
Restriction	<p>Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is not cleared																								
H/W Reset	Contents of memory is not cleared																								
Flow Chart																									

6.2.35 Set tear scan lines(44h)

44 H	TEST(Tear Effect Scan Lines)												
	DCX	NWR	NRD	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1 st parameter	1	1	↑	-	TELINE[15:8](8'b0)							00..FF	
2 nd parameter	1	1	↑	-	TELINE[7:0](8'b0)							00..FF	
Description	<p>This command is turns on the display module's Tearing Effect output signal on the TE signal Line. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. See chapter "5.2 Tearing Effect Output Line".</p>												
Restriction	The command has no effect when Tearing Effect output is already ON.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						TELINE[15:8]=0000h						
	S/W Reset						TELINE[15:8]=0000h						
	H/W Reset						TELINE[15:8]=0000h						
Flow Chart	 <pre> graph TD Start([TE Output On or Off]) --> SetTear[set_tear_on] subgraph " " SetTear --> LineNLSB[/Line N (LSB)/] LineNLSB --> LineNMSB[/Line N (MSB)/] end LineNMSB --> End([TE Output On]) </pre>												

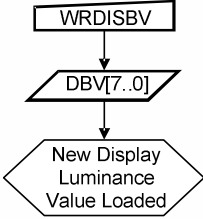
6.2.36 Get scan lines(45h)

45H	GETSL(Mipi new Get Scan Lines)												
	DCX	NWR	NRD	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	↑	1	-	SL[15:8]							00..FF	
3 rd parameter	1	↑	1	-	SL[7:0]							00..FF	
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						Undefined						
	S/W Reset						Undefined						
	H/W Reset						Undefined						
Flow Chart	<p>The flow chart illustrates the process of getting scan lines. It starts with a box labeled 'Get Scan Lines(45h)' in the Host region. An arrow points down to a parallelogram labeled 'Scan Lines MSB' in the Driver region. A second arrow points down to another parallelogram labeled 'Scan Lines LSB' in the Driver region. A dashed horizontal line separates the Host and Driver regions.</p>												

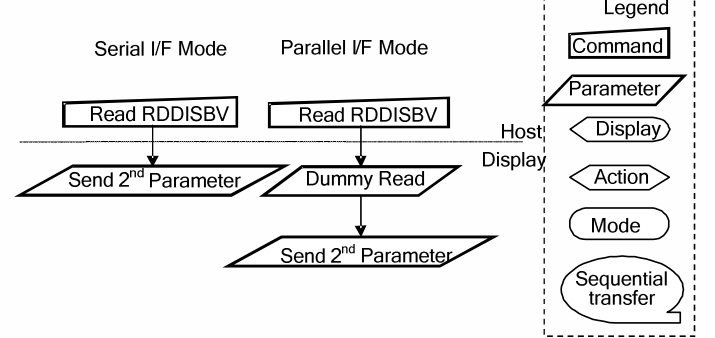
6.2.37 Read_DDB_start (A1h)

A1 H	Read_DDB_start												
	DCX	RDX	WRX	D17~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	Dummy read
2 nd parameter	1	↑	1	-	ID1								
3 rd parameter	1	↑	1	-	ID2								
4 th parameter	1	↑	1	-	ID3								
5 th parameter	1	↑	1	-	ID4								
6 th parameter	1	↑	1	-	1	1	1	1	1	1	1	1	0xFF
Description	The format of returned data is as follows: Parameter 1: Dummy read. Parameter 2: Supplier ID code ID1. Parameter 3: Supplier ID code ID2. Parameter 4: Supplier Elective Data code ID3. Parameter 5: Supplier Elective Data code ID4. Parameter 6: single-byte <i>Escape or Exit Code</i> (0xFF).												
Restrictions													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In or Booster Off						Yes						
Default	Status						Default Value						
	Power On Sequence						OTP Value						
	S/W Reset						OTP Value						
	H/W Reset						OTP Value						
Flow Chart													

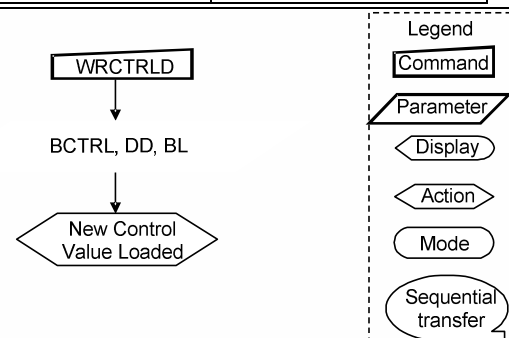
6.2.38 Write Display Brightness (51h)

51 H	WRDISBV (Write Display Brightness)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51
1 st parameter	1	1	↑	-	DBV[7:0]							00 ... FF	
Description	<p>This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "7.17.4 Brightness Control Block".</p>												
Restriction													
Register Availability	Status				Availability								
	Sleep Out				Yes								
	Sleep In				Yes								
Default	Status				Default Value								
	Power On Sequence				00h								
	S/W Reset				00h								
	H/W Reset				00h								
Flow Chart					<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <p>Command: []</p> <p>Parameter: /</p> <p>Display: <</p> <p>Action: ></p> <p>Mode: ()</p> <p>Sequential transfer: ()</p> </div>								

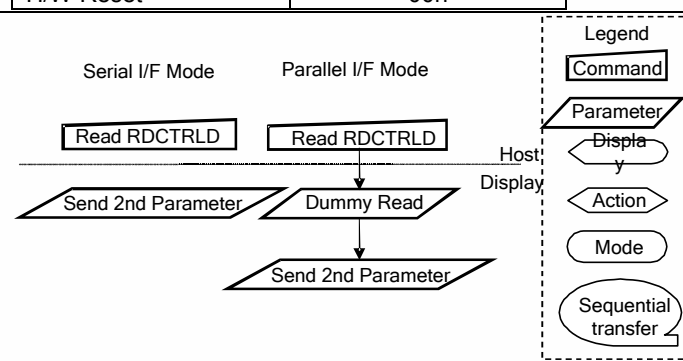
6.2.39 Read Display Brightness Value (52h)

52 H	RDDISBV (Read Display Brightness Value)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2 nd parameter	1	↑	1	-	DBV[7:0]							xx	
Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: "7.17.4 Brightness Control Block", 7.14.1 Display configuration" and "6.2.39 Write Display Brightness (51h)X" DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "6.2.41 Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "6.2.41 Write CTRL Display (53h)" command when bit BCTRL is '1'. When bit BCTRL of "6.2.41 Write CTRL Display (53h)" command is '1' and bit C1/C0 of "6.2.43 Write Content Adaptive Brightness Control (55h)" are '0', DBV[7:0] output is the brightness value specified with "6.2.39 Write Display Brightness (51h)" command. Refers to "2.8.1 Display configuration" for the function matrix.</p>												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart	 <p>The flow chart illustrates the communication sequence for the Read Display Brightness Value (52h) command. It is divided into two modes: Serial I/F Mode and Parallel I/F Mode. In Serial I/F Mode, the Host sends the Read RDDISBV command to the Display, and the Display responds with the 2nd Parameter. In Parallel I/F Mode, the Host sends the Read RDDISBV command to the Display, which then performs a Dummy Read. Subsequently, the Host sends the 2nd Parameter to the Display. A legend defines the symbols used: a rectangle for Command, a parallelogram for Parameter, a diamond for Display, a triangle for Action, an oval for Mode, and a rounded rectangle for Sequential transfer.</p>												

6.2.40 Write CTRL Display (53h)

53 H	WRCTRLD (Write Control Display)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53
1 st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00.. FF
Description	<p>This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don't care.</p>												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart													

6.2.41 Read CTRL Value Display (54h)

54 H	RDCTRLD (Read Control Value Display)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	1	54
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2 nd parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command returns ambient light and brightness control values, see chapter: "6.2.41 Write CTRL Display (53h)X". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit and CABG_ON output is VSSD) 1 = On (CABG_ON output is IOVCC)												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart	 <p>The flow chart illustrates the sequence of operations for the Read RDCTRLD command in both Serial I/F Mode and Parallel I/F Mode. In Serial I/F Mode, the host sends a 'Read RDCTRLD' command, followed by a 'Send 2nd Parameter' action. In Parallel I/F Mode, the host sends a 'Read RDCTRLD' command, which is followed by a 'Dummy Read' action, and then a 'Send 2nd Parameter' action. A legend defines the symbols: a rectangle for 'Command', a parallelogram for 'Parameter', a hexagon for 'Display', a diamond for 'Action', an oval for 'Mode', and a dashed box for 'Sequential transfer'.</p>												

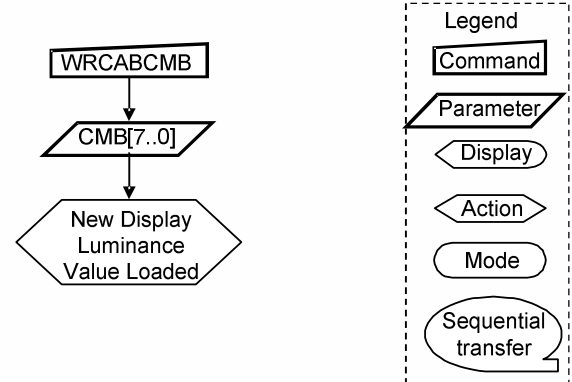
6.2.42 Write Content Adaptive Brightness Control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)																															
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	-	0	1	0	1	0	1	0	1	55																			
1 st parameter	1	1	↑	-	xx	xx	xx	xx	xx	xx	CABC[1:0]		xx																			
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "7.17 Content Adaptive Brightness Control (CABC)".																															
	<table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> <td></td> </tr> </tbody> </table> <p>X = Don't care.</p>													C1	C0	Function	Note	0	0	Off		0	1	User Interface Image		1	0	Still Picture		1	1	Moving Image
C1	C0	Function	Note																													
0	0	Off																														
0	1	User Interface Image																														
1	0	Still Picture																														
1	1	Moving Image																														
Restriction																																
Register Availability	Status		Availability																													
	Sleep Out		Yes																													
	Sleep In		Yes																													
Default	Status		Default Value																													
	Power On Sequence		00h																													
	S/W Reset		00h																													
	H/W Reset		00h																													
Flow Chart	<pre> graph TD WRCABC[Command] --> Param[/Parameter: C[1:0]/] Param --> Mode{New Adaptive Image Mode} </pre>																															

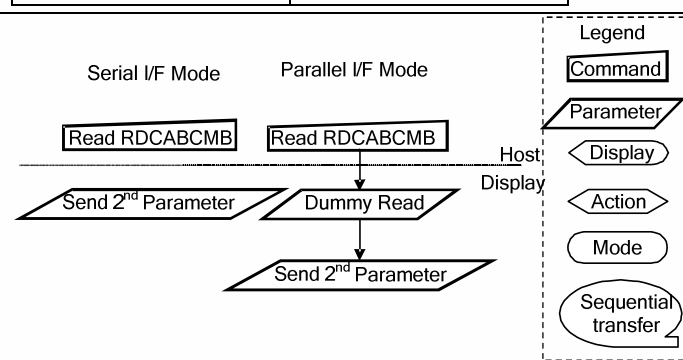
6.2.43 Read Content Adaptive Brightness Control (56h)

56 H	RDCABC (Read Content Adaptive Brightness Control)																																
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56																				
1 st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX																				
2 nd parameter	1	↑	1	-	0	0	0	0	0	0	C1	C0	xx																				
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “7.17 Content Adaptive Brightness Control (CABC)”.</p> <table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> <td></td> </tr> </tbody> </table>													C1	C0	Function	Note	0	0	Off		0	1	User Interface Image		1	0	Still Picture		1	1	Moving Image	
C1	C0	Function	Note																														
0	0	Off																															
0	1	User Interface Image																															
1	0	Still Picture																															
1	1	Moving Image																															
Restriction																																	
Register Availability	Status		Availability																														
	Sleep Out		Yes																														
	Sleep In		Yes																														
Default	Status		Default Value																														
	Power On Sequence		00h																														
	S/W Reset		00h																														
	H/W Reset		00h																														
Flow Chart	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Serial I/F Mode Parallel I/F Mode</p> <pre> graph TD subgraph Serial_I/F_Mode [Serial I/F Mode] RDCABC_S[Read RDCABC] --> S2ndP[Send 2nd Parameter] end subgraph Parallel_I/F_Mode [Parallel I/F Mode] RDCABC_P[Read RDCABC] --> DR[Dummy Read] DR --> S2ndP_P[Send 2nd Parameter] end </pre> </div> <div style="width: 45%; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																																

6.2.44 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E
1 st parameter	1	1	1	-	CMB[7:0]							00.. FF	
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "7.17.4 Minimum brightness setting of CABC function".												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart													

6.2.45 Read CABC minimum brightness (5Fh)

5F H	RDCABCMB (Read CABC minimum brightness)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F
1 st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2 nd parameter	1	↑	1	-	CMB[7:0]							XX	
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "7.17.4 Minimum brightness setting of CABC function". CMB[7:0] is CABC minimum brightness specified with "6.2.45 Write CABC minimum brightness (5Eh)" command.												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart													

6.2.46 Read Automatic Brightness Control Self-Diagnostic Result (68h)

68 H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68
1 st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2 nd parameter	1	↑	1	-	D[7:6]		0	0	0	0	0	0	XX
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: <ul style="list-style-type: none"> • Bit D7 – Register Loading Detection See section “7.15.1 Register loading Detection”. • Bit D6 – Functionality Detection See section “X7.15.2 Functionality Detection “. • Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’. 												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		00h										
	S/W Reset		00h										
	H/W Reset		00h										
Flow Chart	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Serial I/F Mode Parallel I/F Mode</p> <p>Read RDABCSDR Read RDABCSDR</p> <hr/> <p>Send 2nd Parameter Dummy Read</p> <p>Send 2nd Parameter</p> </div> <div style="width: 45%; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <p>Command: []</p> <p>Parameter: /</p> <p>Display: <</p> <p>Action: ></p> <p>Mode: ()</p> <p>Sequential transfer: ↻</p> </div> </div> <p style="margin-left: 100px;">Host: Display:</p>												

6.2.47 Set extended command set (B0h)

B0 H	SETEXTC													
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	-	1	0	1	1	0	0	0	0	B0	
1 st parameter	1	1	↑	-	0	0	0	0	0	0	EXTC[1:0]		XX	
Description	EXTC[1:0]: This register is select command access protect mode.													
	EXTC[1:0]	User Command			Himax command									
		00h ~ AFh			B0h	B1h~DFh	E0h~EFh	F0h~FFh						
	00	Yes			Yes	Yes	Yes	Yes	Yes					
	01	Yes			Yes	Yes	Yes	Yes	No					
	10	Yes			Yes	Yes	Yes	No	No					
11	Yes			Yes	No	No	No	No						
Restriction														
Register Availability	Status		Availability											
	Sleep Out		Yes											
	Sleep In		Yes											
Default	Status		Default Value											
	Power On Sequence		00h											
	S/W Reset		00h											
	H/W Reset		00h											
Flow Chart														

6.2.48 Set Deep Standby mode (B1h)

B1 H	SETDPSTB												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	0	1	B1
1 st parameter	1	1	↑	-	0	0	0	0	0	0	0	DP_STB	XX
Description	DP_STB: Deep standby mode enable bit. See chapter "5.13 Deep standby mode enter/exit flow".												
Restriction													
Register Availability	Status						Availability						
	Sleep Out						No						
	Sleep In						Yes						
Default	Status						Default Value						
	Power On Sequence						00h						
	S/W Reset						No change						
	H/W Reset						00h						
Flow Chart													

6.2.49 Set GRAM access and Interface (B3h)

B3 H	SETGRAM												HEX																																																																																																																																															
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																																																																																																																																																
Command	0	1	↑	-	1	0	1	1	0	0	1	1	B3																																																																																																																																															
1 st parameter	1	1	↑	-	0	0	0	0	0	0	0	0	00h																																																																																																																																															
2 nd parameter	1	1	↑	-	0	0	0	0	0	TEI[2:0]			00h~07h																																																																																																																																															
3 rd parameter	1	1	↑	-	0	0	0	0	DENC[3:0]				00h~07h																																																																																																																																															
4 th parameter	1	1	↑	-	0	0	EPF[1:0]		0	0	0	DFM																																																																																																																																																
Description	<p>TEI[2:0]: TE output cycle setting.</p> <table border="1"> <thead> <tr> <th>TEI[2:0]</th> <th>TE output cycle</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>1 frame</td> </tr> <tr> <td>001</td> <td>2 frame</td> </tr> <tr> <td>011</td> <td>4 frame</td> </tr> <tr> <td>101</td> <td>6 frame</td> </tr> <tr> <td>Others</td> <td>Prohibited</td> </tr> </tbody> </table> <p>DENC[2:0]: Select GRAM write cycle in RGB interface.</p> <table border="1"> <thead> <tr> <th>DENC[2:0]</th> <th>GRAM write cycle</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>1 frame</td> </tr> <tr> <td>001</td> <td>2 frame</td> </tr> <tr> <td>010</td> <td>3 frame</td> </tr> <tr> <td>011</td> <td>4 frame</td> </tr> <tr> <td>100</td> <td>5 frame</td> </tr> <tr> <td>101</td> <td>6 frame</td> </tr> <tr> <td>110</td> <td>7 frame</td> </tr> <tr> <td>111</td> <td>8 frame</td> </tr> </tbody> </table> <p>DFM: It is define image data read/write format to GRAM in DBI Type-B 16bit interface and DBI Type-C Interface. See chapter “4.1.5 DBI TYPE-B Interface Data Color Coding” and “4.2.3 DBI TYPE-C Interface Data Color Coding”.</p> <p>EPF[1:0]: Data format select for 16bbp to 18bbp.</p> <table border="1"> <thead> <tr> <th rowspan="2">EPF[1:0]</th> <th colspan="18">GRAM Data</th> </tr> <tr> <th>DB17</th> <th>DB16</th> <th>DB15</th> <th>DB14</th> <th>DB13</th> <th>DB12</th> <th>DB11</th> <th>DB10</th> <th>DB9</th> <th>DB8</th> <th>DB7</th> <th>DB6</th> <th>DB5</th> <th>DB4</th> <th>DB3</th> <th>DB2</th> <th>DB1</th> <th>DB0</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>R4</td> <td>R3</td> <td>R2</td> <td>R1</td> <td>R0</td> <td>0</td> <td>G5</td> <td>G4</td> <td>G3</td> <td>G2</td> <td>G1</td> <td>G0</td> <td>B4</td> <td>B3</td> <td>B2</td> <td>B1</td> <td>B0</td> <td>0</td> </tr> <tr> <td>2'h1</td> <td>R4</td> <td>R3</td> <td>R2</td> <td>R1</td> <td>R0</td> <td>1</td> <td>G5</td> <td>G4</td> <td>G3</td> <td>G2</td> <td>G1</td> <td>G0</td> <td>B4</td> <td>B3</td> <td>B2</td> <td>B1</td> <td>B0</td> <td>1</td> </tr> <tr> <td>2'h2</td> <td>R4</td> <td>R3</td> <td>R2</td> <td>R1</td> <td>R0</td> <td>R4</td> <td>G5</td> <td>G4</td> <td>G3</td> <td>G2</td> <td>G1</td> <td>G0</td> <td>B4</td> <td>B3</td> <td>B2</td> <td>B1</td> <td>B0</td> <td>B4</td> </tr> <tr> <td>2'h3</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> </tbody> </table>													TEI[2:0]	TE output cycle	000	1 frame	001	2 frame	011	4 frame	101	6 frame	Others	Prohibited	DENC[2:0]	GRAM write cycle	000	1 frame	001	2 frame	010	3 frame	011	4 frame	100	5 frame	101	6 frame	110	7 frame	111	8 frame	EPF[1:0]	GRAM Data																		DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0	2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4	2'h3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
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111	8 frame																																																																																																																																																											
EPF[1:0]	GRAM Data																																																																																																																																																											
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2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0																																																																																																																																										
2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1																																																																																																																																										
2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4																																																																																																																																										
2'h3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x																																																																																																																																										
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	H/W Reset																																																																																																																																																											
Flow Chart																																																																																																																																																												

6.2.50 Set Display mode (B4h)

B4 H	SETDISPLAY												HEX																					
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																						
Command	0	1	↑	-	1	0	1	1	0	1	0	0	B4																					
1 st parameter	1	1	↑	-	0	0	0	RM	0	0	DM[1:0]		XX																					
Description	<p>RM: The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation. RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting</p> <table border="1"> <thead> <tr> <th>RM</th> <th>Interface for RAM Access</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DBI Interface (CPU)</td> </tr> <tr> <td>1</td> <td>DPI Interface (RGB)</td> </tr> </tbody> </table> <p>DM[1:0]: The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, HSYNC or DPI signal.</p> <table border="1"> <thead> <tr> <th>DM 1</th> <th>DM 0</th> <th>Display Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Internal oscillation clock</td> </tr> <tr> <td>0</td> <td>1</td> <td>External VSYNC + HSYNC (Display data from GRAM)</td> </tr> <tr> <td>1</td> <td>0</td> <td>External VSYNC (Display data from GRAM)</td> </tr> <tr> <td>1</td> <td>1</td> <td>External DPI (RGB Through mode)</td> </tr> </tbody> </table> <p>Note: Switching between VSYNC, HSYNC and DPI operation is prohibited.</p>													RM	Interface for RAM Access	0	DBI Interface (CPU)	1	DPI Interface (RGB)	DM 1	DM 0	Display Mode	0	0	Internal oscillation clock	0	1	External VSYNC + HSYNC (Display data from GRAM)	1	0	External VSYNC (Display data from GRAM)	1	1	External DPI (RGB Through mode)
	RM	Interface for RAM Access																																
0	DBI Interface (CPU)																																	
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1	1	External DPI (RGB Through mode)																																
Restriction																																		
Register Availability	Status		Availability																															
	Sleep Out		Yes																															
	Sleep In		Yes																															
Default	Status		Default Value																															
	Power On Sequence																																	
	S/W Reset		No change																															
	H/W Reset																																	
Flow Chart																																		

6.2.51 Get Device ID (BFh)

BF H	GETDEVICEID												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	1	1	1	BF
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	XX
2 nd parameter	1	↑	1	-	0	0	0	0	0	0	0	1	01
3 rd parameter	1	↑	1	-	0	1	1	0	0	0	1	0	62
4 th parameter	1	↑	1	-	1	0	0	0	0	0	1	1	83
5 th parameter	1	↑	1	-	0	1	0	1	0	1	1	1	57
6 th parameter	1	↑	1	-	1	1	1	1	1	1	1	1	FF
Description	The format of returned data is as follows: Parameter 1: Dummy read. Parameter 2: MIPI Alliance code. Parameter 3: MIPI Alliance code. Parameter 4: Device ID code. Parameter 5: Device ID code. Parameter 6: single-byte <i>Escape or Exit Code</i> (0xFF).												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence												
	S/W Reset		No change										
	H/W Reset												
Flow Chart													

6.2.52 Set Panel Driving (C0h)

C0 H	SETPANEL												HEX
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	-	1	1	0	0	0	0	0	0	C0
1 st parameter	1	1	↑	-	0	0	0	REV	SM	GS	0	0	XX
2 nd parameter	1	1	↑	-	0	0	NL[5:0]					XX	
3 rd parameter	1	1	↑	-	0	SCN[6:0]						XX	
4 th parameter	1	1	↑	-	0	0	0	NDL	0	PTS[2:0]		XX	
5 th parameter	1	1	↑	-	0	0	0	PTG	ISC[3:0]			XX	

GS: Select the optimal scan mode for the module.

SM: Sets the gate driver pin arrangement in combination.

Description

SM	GS	Scan direction
0	0	<p>G1,G2,G3,... G157,G158,... G479,G480</p>
0	1	<p>G480,G479,G478,... G158,G157,... G2,G1</p>
1	0	<p>G1,G3... G477,G479, G2,G4,G56. G480</p>
1	1	<p>G480,G478... G4,G2, G479,G477,... G1</p>

REV: Enables the grayscale inversion of the image in display area.

REV	GRAM Data	Display area	
		VCOM = "L"	VCOM = "H"
0	18'h00000	V63P	V0N
	:	:	:
	18'h3FFFF	V0P	V63N
1	18'h00000	V0P	V63N
	:	:	:
	18'h3FFFF	V63P	V0N

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0].

The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Driver line number
0x00 ~ 0x3B	8*(NL[5:0]+1) line
Other setting	Inhibited

SCN[6:0]: Scan line start position.

SCN[6:0]	Start position of Gate			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
0x00 ~ 0x3B	G[1+SCN[6:0]*4]	G[480- SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[480- SCN[6:0]*4]
0x3C ~ 0x77	G[1+SCN[6:0]*4]	G[480- SCN[6:0]*4]	G[2+(SCN[6:0]-0x3C)*8]	G[479- (SCN[6:0]-0x3C)*8]
Other setting	Inhibited	Inhibited	Inhibited	Inhibited

PTS[2:0]: Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

PTS[2:0]	Source output level in non-display area			
	VCOM = "L"		VCOM = "H"	
000	V63P	V0N	V0P	V63N
001	V0P	V63N	V63P	V0N
010	GND	GND	GND	GND
011	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Other	Inhibited	Inhibited	Inhibited	Inhibited

NDL: Sets the source output level in non-display area of refresh scan cycle. Settings are different to normally black panels and normally white panels.

NDL	Source output level in non-display area of refresh scan cycle	
	VCOM = "L"	VCOM = "H"
0	V63P	V0N
1	V0P	V63N

ISC[3:0]: Specify the refresh scan cycle of gate driver when **PTG** select in non-display area. Then refresh scan cycle is set to an odd number from 0~31. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f _{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	183ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	250ms
1	0	0	0	17 frames	283ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	350ms
1	0	1	1	23 frames	383ms
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

>> HX8357-B

320RGB x 480 dot, 262K color, TFT Mobile Single Chip Driver



DATA SHEET Preliminary V01

	PTG: Specify the scan mode of gate driver in non-display area.	
	PTG	Gate Outputs in Non-display Area
	0	Normal Drive
	1	Interval Drive
Restriction		
Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	
	S/W Reset	No change
	H/W Reset	
Flow Chart		

6.2.53 Set display timing for Normal mode (C1h)

C1 H	SETNORTIM																																																																		
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																						
Command	0	1	↑	-	1	1	0	0	0	0	0	1	C1																																																						
1 st parameter	1	1	↑	-	0	0	0	BC0	0	0	DIV0[1:0]		XX																																																						
2 nd parameter	1	1	↑	-	0	0	0	RTN0[4:0]				XX																																																							
3 rd parameter	1	1	↑	-	FP0[3:0]			BP0[3:0]				XX																																																							
Description	<p>BC0: Frame/Line inversion select.</p> <table border="1"> <thead> <tr> <th>BC0</th> <th>Inversion mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Frame</td> </tr> <tr> <td>1</td> <td>Line</td> </tr> </tbody> </table> <p>DIV0[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN1[4:0] bits (1H period clock cycle), FP1[3:0], and BP1[3:0] bits.</p> <table border="1"> <thead> <tr> <th>DIV0[1:0]</th> <th>Division ratio</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1/1</td> </tr> <tr> <td>01</td> <td>1/2</td> </tr> <tr> <td>10</td> <td>1/4</td> </tr> <tr> <td>11</td> <td>1/8</td> </tr> </tbody> </table> <p>RTN0[4:0]: Specify clock number of one line period in Normal mode for internal operation. Clock cycles=1/internal operation clock frequency(fosc)</p> <table border="1"> <thead> <tr> <th>RTN0[4:0]</th> <th>Clock number per Line</th> </tr> </thead> <tbody> <tr> <td>5'b10000</td> <td>168</td> </tr> <tr> <td>5'b10001</td> <td>169</td> </tr> <tr> <td>5'b10010</td> <td>170</td> </tr> <tr> <td>5'b10011</td> <td>171</td> </tr> <tr> <td>5'b10100</td> <td>172</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>5'b11110</td> <td>182</td> </tr> <tr> <td>5'b11111</td> <td>183</td> </tr> <tr> <td>Other</td> <td>Inhibited</td> </tr> </tbody> </table> <p>FP0[3:0]: Set the number of lines for a front porch period (a blank period following the end of display). BP0[3:0]: Set the number of lines for a back porch period (a blank period made before the beginning of display).</p> <table border="1"> <thead> <tr> <th>FP0[3:0] / BP0[3:0]</th> <th>Front / Back porch period</th> </tr> </thead> <tbody> <tr> <td>4'b0000</td> <td>Inhibited</td> </tr> <tr> <td>4'b0001</td> <td>Inhibited</td> </tr> <tr> <td>4'b0010</td> <td>2 lines</td> </tr> <tr> <td>4'b0011</td> <td>3 lines</td> </tr> <tr> <td>4'b0100</td> <td>4 lines</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>4'b1110</td> <td>14 lines</td> </tr> <tr> <td>4'b1111</td> <td>15 lines</td> </tr> </tbody> </table> <p>The condition in setting BP and FP bits are: $BP \geq 2$ lines, $FP \geq 2$ lines, $BP+FP \leq 30$ lines</p> <p>Formula for the Frame Frequency during internal display mode: Frame frequency = $fosc / (RTN \times DIV \times (Scan\ Line + FP + BP))$ [Hz]</p>													BC0	Inversion mode	0	Frame	1	Line	DIV0[1:0]	Division ratio	00	1/1	01	1/2	10	1/4	11	1/8	RTN0[4:0]	Clock number per Line	5'b10000	168	5'b10001	169	5'b10010	170	5'b10011	171	5'b10100	172	:	:	5'b11110	182	5'b11111	183	Other	Inhibited	FP0[3:0] / BP0[3:0]	Front / Back porch period	4'b0000	Inhibited	4'b0001	Inhibited	4'b0010	2 lines	4'b0011	3 lines	4'b0100	4 lines	:	:	4'b1110	14 lines	4'b1111	15 lines
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	S/W Reset		No change																																																																
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Flow Chart																																																																			

6.2.54 Set display timing for Partial mode (C2h)

C2 H	SETPARTIM												HEX																				
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																					
Command	0	1	↑	-	1	1	0	0	0	0	1	0	C2																				
1 st parameter	1	1	↑	-	0	0	0	BC1	0	0	DIV1[1:0]		XX																				
2 nd parameter	1	1	↑	-	0	0	0	RTN1[4:0]				XX																					
3 rd parameter	1	1	↑	-	FP1[3:0]			BP1[3:0]			XX																						
Description	BC1: Frame/Line inversion select. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>BC1</th> <th>Inversion mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Frame</td> </tr> <tr> <td>1</td> <td>Line</td> </tr> </tbody> </table>													BC1	Inversion mode	0	Frame	1	Line														
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	DIV1[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN1[4:0] bits (1H period clock cycle), FP1[3:0], and BP1[3:0] bits. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIV1[1:0]</th> <th>Division ratio</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1/1</td> </tr> <tr> <td>01</td> <td>1/2</td> </tr> <tr> <td>10</td> <td>1/4</td> </tr> <tr> <td>11</td> <td>1/8</td> </tr> </tbody> </table>													DIV1[1:0]	Division ratio	00	1/1	01	1/2	10	1/4	11	1/8										
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	Power On Sequence																																
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6.2.55 Set display timing for Idle mode (C3h)

C3 H	SETIDLTIM												HEX																																																						
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																																																							
Command	0	1	↑	-	1	1	0	0	0	0	1	1	C3																																																						
1 st parameter	1	1	↑	-	0	0	0	BC2	0	0	DIV2[1:0]		XX																																																						
2 nd parameter	1	1	↑	-	0	0	0	RTN2[4:0]				XX																																																							
3 rd parameter	1	1	↑	-	FP2[3:0]			BP2[3:0]				XX																																																							
Description	<p>BC2: Frame/Line inversion select.</p> <table border="1"> <thead> <tr> <th>BC2</th> <th>Inversion mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Frame</td> </tr> <tr> <td>1</td> <td>Line</td> </tr> </tbody> </table> <p>DIV2[1:0]: Specify the division ratio of internal clocks in Normal mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the RTN2[4:0] bits (1H period clock cycle), FP2[3:0], and BP2[3:0] bits.</p> <table border="1"> <thead> <tr> <th>DIV2[1:0]</th> <th>Division ratio</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1/1</td> </tr> <tr> <td>01</td> <td>1/2</td> </tr> <tr> <td>10</td> <td>1/4</td> </tr> <tr> <td>11</td> <td>1/8</td> </tr> </tbody> </table> <p>RTN2[4:0]: Specify clock number of one line period in Normal mode for internal operation. Clock cycles=1/internal operation clock frequency(fosc)</p> <table border="1"> <thead> <tr> <th>RTN2[4:0]</th> <th>Clock number per Line</th> </tr> </thead> <tbody> <tr> <td>5'b10000</td> <td>168</td> </tr> <tr> <td>5'b10001</td> <td>169</td> </tr> <tr> <td>5'b10010</td> <td>170</td> </tr> <tr> <td>5'b10011</td> <td>171</td> </tr> <tr> <td>5'b10100</td> <td>172</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>5'b11110</td> <td>182</td> </tr> <tr> <td>5'b11111</td> <td>183</td> </tr> <tr> <td>Other</td> <td>Inhibited</td> </tr> </tbody> </table> <p>FP2[3:0]: Set the number of lines for a front porch period (a blank period following the end of display). BP2[3:0]: Set the number of lines for a back porch period (a blank period made before the beginning of display).</p> <table border="1"> <thead> <tr> <th>FP2[3:0] / BP2[3:0]</th> <th>Front / Back porch period</th> </tr> </thead> <tbody> <tr> <td>4'b0000</td> <td>Inhibited</td> </tr> <tr> <td>4'b0001</td> <td>Inhibited</td> </tr> <tr> <td>4'b0010</td> <td>2 lines</td> </tr> <tr> <td>4'b0011</td> <td>3 lines</td> </tr> <tr> <td>4'b0100</td> <td>4 lines</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>4'b1110</td> <td>14 lines</td> </tr> <tr> <td>4'b1111</td> <td>15 lines</td> </tr> </tbody> </table> <p>The condition in setting BP and FP bits are: $BP \geq 2$ lines, $FP \geq 2$ lines, $BP+FP \leq 30$ lines</p> <p>Formula for the Frame Frequency during internal display mode: Frame frequency = $fosc / (RTN \times DIV \times (Scan\ Line + FP + BP))$ [Hz]</p>													BC2	Inversion mode	0	Frame	1	Line	DIV2[1:0]	Division ratio	00	1/1	01	1/2	10	1/4	11	1/8	RTN2[4:0]	Clock number per Line	5'b10000	168	5'b10001	169	5'b10010	170	5'b10011	171	5'b10100	172	:	:	5'b11110	182	5'b11111	183	Other	Inhibited	FP2[3:0] / BP2[3:0]	Front / Back porch period	4'b0000	Inhibited	4'b0001	Inhibited	4'b0010	2 lines	4'b0011	3 lines	4'b0100	4 lines	:	:	4'b1110	14 lines	4'b1111	15 lines
	BC2	Inversion mode																																																																	
	0	Frame																																																																	
	1	Line																																																																	
	DIV2[1:0]	Division ratio																																																																	
	00	1/1																																																																	
	01	1/2																																																																	
	10	1/4																																																																	
	11	1/8																																																																	
	RTN2[4:0]	Clock number per Line																																																																	
	5'b10000	168																																																																	
	5'b10001	169																																																																	
	5'b10010	170																																																																	
	5'b10011	171																																																																	
	5'b10100	172																																																																	
:	:																																																																		
5'b11110	182																																																																		
5'b11111	183																																																																		
Other	Inhibited																																																																		
FP2[3:0] / BP2[3:0]	Front / Back porch period																																																																		
4'b0000	Inhibited																																																																		
4'b0001	Inhibited																																																																		
4'b0010	2 lines																																																																		
4'b0011	3 lines																																																																		
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:	:																																																																		
4'b1110	14 lines																																																																		
4'b1111	15 lines																																																																		
Restriction																																																																			
Register Availability	Status		Availability																																																																
	Sleep Out		Yes																																																																
	Sleep In		Yes																																																																
Default	Status		Default Value																																																																
	Power On Sequence																																																																		
	S/W Reset		No change																																																																
	H/W Reset																																																																		
Flow Chart																																																																			

6.2.56 Set display frame (C5h)

C5 H	SETOSC												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	1	0	1	C5
1 st parameter	1	1	↑	-	0	0	0	0	UADJ[3:0]			XX	
Description	UADJ[3:0]: Set the frame rate of full colors normal mode.												
	UADJ[3:0]				Fosc(MHz)								
	0000				1.7981								
	0001				2.2366								
	0010				2.6673								
	0011				3.0995								
	0100				3.5198								
	0101				3.9402								
	0110				4.3609								
	0111				4.7758								
	1000				5.2000								
	1001				5.5791								
	1010				5.9986								
	1011				6.4398								
	1100				6.8374								
	1101				7.2101								
	1110				7.6100								
1111				8.0426									
Restriction													
Register Availability	Status				Availability								
	Sleep Out				Yes								
	Sleep In				Yes								
Default	Status				Default Value								
	Power On Sequence												
	S/W Reset				No change								
	H/W Reset												
Flow Chart													

6.2.57 Set RGB Interface (C6h)

C6 H	SETRGB																																
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	-	1	1	0	0	0	1	1	0	C6																				
1 st parameter	1	1	↑	-	SDA_EN	0	0	VPL	HPL	0	EPL	DPL	XX																				
Description	This command is used to set RGB interface related register																																
	EPL: Specify the polarity of Enable pin in DPI interface mode.																																
	<table border="1"> <thead> <tr> <th>EPL</th> <th>ENABLE pin</th> <th>Display image</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Low</td> <td>Enable</td> <td>Write data to DB17-0</td> </tr> <tr> <td>0</td> <td>High</td> <td>Disable</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Low</td> <td>Disable</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>High</td> <td>Enable</td> <td>Write data to DB17-0</td> </tr> </tbody> </table>													EPL	ENABLE pin	Display image	Operation	0	Low	Enable	Write data to DB17-0	0	High	Disable	Disable	1	Low	Disable	Disable	1	High	Enable	Write data to DB17-0
	EPL	ENABLE pin	Display image	Operation																													
	0	Low	Enable	Write data to DB17-0																													
	0	High	Disable	Disable																													
	1	Low	Disable	Disable																													
	1	High	Enable	Write data to DB17-0																													
	VPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.																																
	HPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.																																
DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.																																	
SDA_EN: DBI Type-C interface pin selection																																	
<table border="1"> <thead> <tr> <th>SDA_EN</th> <th>DIN_SDA</th> <th>DOUT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Data Input</td> <td>Data output</td> </tr> <tr> <td>1</td> <td>Data input/output</td> <td>Not used</td> </tr> </tbody> </table>													SDA_EN	DIN_SDA	DOUT	0	Data Input	Data output	1	Data input/output	Not used												
SDA_EN	DIN_SDA	DOUT																															
0	Data Input	Data output																															
1	Data input/output	Not used																															
Restriction																																	
Register Availability	Status		Availability																														
	Sleep Out		Yes																														
	Sleep In		Yes																														
Default	Status		Default Value																														
	Power On Sequence																																
	S/W Reset		No change																														
	H/W Reset																																
Flow Chart																																	

6.2.58 Set Gamma (C8h)

C8 H	SETGAMMA												HEX
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	
Command	0	1	↑	-	1	1	0	0	1	0	0	0	C8
1 st parameter	1	1	↑	-	0	KP1[2:0]		0	KP0[2:0]		XX		
2 nd parameter	1	1	↑	-	0	KP3[2:0]		0	KP2[2:0]		XX		
3 rd parameter	1	1	↑	-	0	KP5[2:0]		0	KP4[2:0]		XX		
4 th parameter	1	1	↑	-	0	RP1[2:0]		0	RP0[2:0]		XX		
5 th parameter	1	1	↑	-	0	0	0	0	VRP0[3:0]			XX	
6 th parameter	1	1	↑	-	0	0	VRP1[4:0]					XX	
7 th parameter	1	1	↑	-	0	KN1[2:0]		0	KN0[2:0]		XX		
8 th parameter	1	1	↑	-	0	KN3[2:0]		0	KN2[2:0]		XX		
9 th parameter	1	1	↑	-	0	KN5[2:0]		0	KN4[2:0]		XX		
10 th parameter	1	1	↑	-	0	RN1[2:0]		0	RN0[2:0]		XX		
11 th parameter	1	1	↑	-	0	0	0	0	VRN0[3:0]			XX	
12 th parameter	1	1	↑	-	0	0	0	VRN1[4:0]					XX
Description	This command is used for Gamma Curve related Setting. For details, please refer to “5.7 Gamma Characteristic Correction Function”												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence												
	S/W Reset		No change										
	H/W Reset												
Flow Chart													

6.2.59 Set Power (D0h)

D0h	SETPOWER																																																																																																																																																															
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																			
Command	0	1	↑	-	1	1	0	1	0	0	0	0	D0																																																																																																																																																			
1 st parameter	1	1	↑	-	0	AP[2:0]			0	VC[2:0]			XX																																																																																																																																																			
2 nd parameter	1	1	↑	-	0	PON	0	0	0	BT[2:0]																																																																																																																																																						
3 rd parameter	1	1	↑	-	0	0	0	0	VRH[3:0]																																																																																																																																																							
Description	<p>AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.</p> <table border="1"> <thead> <tr> <th>AP2</th> <th>AP1</th> <th>AP0</th> <th>Constant Current of Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Operation of the operational amplifier stops</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Medium</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Medium</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Medium</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Medium High</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Large</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> </tbody> </table> <p>VC[2:0]: Set VCI1 voltage</p> <table border="1"> <thead> <tr> <th rowspan="2">VC[2:0]</th> <th rowspan="2">VCI1</th> <th colspan="2">DDVDH</th> <th rowspan="2">VCL</th> </tr> <tr> <th>DDVDH TRI=0</th> <th>DDVDH TRI=1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>3.24V</td> <td>6.48V</td> <td>6.67V</td> <td>-3.24V</td> </tr> <tr> <td>001</td> <td>3.06V</td> <td>6.12V</td> <td>6.48V</td> <td>-3.06V</td> </tr> <tr> <td>010</td> <td>2.91V</td> <td>5.82V</td> <td>6.12V</td> <td>-2.91V</td> </tr> <tr> <td>011</td> <td>2.77V</td> <td>5.54V</td> <td>5.97V</td> <td>-2.77V</td> </tr> <tr> <td>100</td> <td>2.64V</td> <td>5.28V</td> <td>5.67V</td> <td>-2.64V</td> </tr> <tr> <td>101</td> <td>2.47V</td> <td>4.94V</td> <td>5.40V</td> <td>-2.47V</td> </tr> <tr> <td>110</td> <td>1.92V</td> <td>3.84V</td> <td>5.16V</td> <td>-1.92V</td> </tr> <tr> <td>111</td> <td>VCI</td> <td>VCIx2</td> <td>inhibited</td> <td>-VCI</td> </tr> </tbody> </table> <p>Note: 1. VCI1 ≤ (VCI-0.15)V.</p> <p>BT[3:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.</p> <table border="1"> <thead> <tr> <th>BT2</th> <th>BT1</th> <th>BT0</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td rowspan="3">3xDDVDH</td> <td>-2DDVDH+VCL</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>-2DDVDH</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>-DDVDH+VCL</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td rowspan="3">2DDVDH + VCI1</td> <td>-2DDVDH+VCL</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>-2DDVDH</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>-DDVDH+VCL</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td rowspan="2">2DDVDH</td> <td>-2DDVDH</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>-DDVDH+VCL</td> </tr> </tbody> </table> <p>PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation.</p> <table border="1"> <thead> <tr> <th>PON</th> <th>Operation of step-up circuit 2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </tbody> </table> <p>VRH[3:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting. Note: setting restriction: VREG1OUT ≤ (DDVDH-0.3V)</p> <table border="1"> <thead> <tr> <th>VRH[3:0]</th> <th>VREG1</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Halt</td> </tr> <tr> <td>0001</td> <td>4.000v</td> </tr> <tr> <td>0010</td> <td>4.125v</td> </tr> <tr> <td>0011</td> <td>4.250v</td> </tr> <tr> <td>0100</td> <td>4.375v</td> </tr> <tr> <td>0101</td> <td>4.500v</td> </tr> <tr> <td>0110</td> <td>4.625v</td> </tr> <tr> <td>0111</td> <td>4.750v</td> </tr> </tbody> </table>													AP2	AP1	AP0	Constant Current of Operational Amplifier	0	0	0	Operation of the operational amplifier stops	0	0	1	Medium	0	1	0	Medium	0	1	1	Medium	1	0	0	Medium High	1	0	1	Large	1	1	0	Setting Inhibited	1	1	1	Setting Inhibited	VC[2:0]	VCI1	DDVDH		VCL	DDVDH TRI=0	DDVDH TRI=1	000	3.24V	6.48V	6.67V	-3.24V	001	3.06V	6.12V	6.48V	-3.06V	010	2.91V	5.82V	6.12V	-2.91V	011	2.77V	5.54V	5.97V	-2.77V	100	2.64V	5.28V	5.67V	-2.64V	101	2.47V	4.94V	5.40V	-2.47V	110	1.92V	3.84V	5.16V	-1.92V	111	VCI	VCIx2	inhibited	-VCI	BT2	BT1	BT0	VGH	VGL	0	0	0	3xDDVDH	-2DDVDH+VCL	0	0	1	-2DDVDH	0	1	0	-DDVDH+VCL	0	1	1	2DDVDH + VCI1	-2DDVDH+VCL	1	0	0	-2DDVDH	1	0	1	-DDVDH+VCL	1	1	0	2DDVDH	-2DDVDH	1	1	1	-DDVDH+VCL	PON	Operation of step-up circuit 2	0	OFF	1	ON	VRH[3:0]	VREG1	0000	Halt	0001	4.000v	0010	4.125v	0011	4.250v	0100	4.375v	0101	4.500v	0110	4.625v	0111	4.750v
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0	1	0		-DDVDH+VCL																																																																																																																																																												
0	1	1	2DDVDH + VCI1	-2DDVDH+VCL																																																																																																																																																												
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0111	4.750v																																																																																																																																																															

>> HX8357-B

320RGB x 480 dot, 262K color, TFT Mobile Single Chip Driver



DATA SHEET Preliminary V01

	1000	4.875v	
	1001	5.000v	
	1010	5.125v	
	1011	5.250v	
	1100	5.500v	
	1101	5.750v	
	1110	6.000v	
	1111	6.000v	
Restriction			
Register Availability	Status	Availability	
	Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence		
	S/W Reset	No change	
	H/W Reset		
Flow Chart			

6.2.60 Set VCOM (D1h)

D1H	SETVCOM												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	0	0	1	D1
1 st parameter	1	1	↑	-	0	VCM[6:0]						XX	
2 nd parameter	1	1	↑	-	0	0	0	VDV[4:0]					
Description	VCM(6-0): Set the VCOMH voltage (High level voltage of VCOM) It is possible to amplify from 0.492 to 1 times of VREG1OUT voltage.												
	VCM[6:0]			VCOMH			VCM[6:0]			VCOMH			
	0 0 0 0 0 0			0.492xVREG1OUT			1 0 0 0 0 0			0.748xVREG1OUT			
	0 0 0 0 0 1			0.496xVREG1OUT			1 0 0 0 0 1			0.752xVREG1OUT			
	0 0 0 0 1 0			0.500xVREG1OUT			1 0 0 0 1 0			0.756xVREG1OUT			
	0 0 0 0 1 1			0.504xVREG1OUT			1 0 0 0 1 1			0.760xVREG1OUT			
	0 0 0 1 0 0			0.508xVREG1OUT			1 0 0 1 0 0			0.764xVREG1OUT			
	0 0 0 1 0 1			0.512xVREG1OUT			1 0 0 1 0 1			0.768xVREG1OUT			
	0 0 0 1 1 0			0.516xVREG1OUT			1 0 0 1 1 0			0.772xVREG1OUT			
	0 0 0 1 1 1			0.520xVREG1OUT			1 0 0 1 1 1			0.776xVREG1OUT			
	0 0 1 0 0 0			0.524xVREG1OUT			1 0 0 1 0 0			0.780xVREG1OUT			
	0 0 1 0 0 1			0.528xVREG1OUT			1 0 0 1 0 1			0.784xVREG1OUT			
	0 0 1 0 1 0			0.532xVREG1OUT			1 0 0 1 0 1			0.788xVREG1OUT			
	0 0 1 0 1 1			0.536xVREG1OUT			1 0 0 1 0 1			0.792xVREG1OUT			
	0 0 1 1 0 0			0.540xVREG1OUT			1 0 0 1 1 0			0.796xVREG1OUT			
	0 0 1 1 0 1			0.544xVREG1OUT			1 0 0 1 1 0			0.800xVREG1OUT			
	0 0 1 1 1 0			0.548xVREG1OUT			1 0 0 1 1 0			0.804xVREG1OUT			
	0 0 1 1 1 1			0.552xVREG1OUT			1 0 0 1 1 1			0.808xVREG1OUT			
	0 0 1 0 0 0			0.556xVREG1OUT			1 0 1 0 0 0			0.812xVREG1OUT			
	0 0 1 0 0 1			0.560xVREG1OUT			1 0 1 0 0 1			0.816xVREG1OUT			
	0 0 1 0 1 0			0.564xVREG1OUT			1 0 1 0 1 0			0.820xVREG1OUT			
	0 0 1 0 1 1			0.568xVREG1OUT			1 0 1 0 1 1			0.824xVREG1OUT			
	0 0 1 1 0 0			0.572xVREG1OUT			1 0 1 1 0 0			0.828xVREG1OUT			
	0 0 1 1 0 1			0.576xVREG1OUT			1 0 1 1 0 1			0.832xVREG1OUT			
	0 0 1 1 1 0			0.580xVREG1OUT			1 0 1 1 1 0			0.836xVREG1OUT			
	0 0 1 1 1 1			0.584xVREG1OUT			1 0 1 1 1 1			0.840xVREG1OUT			
	0 0 1 1 0 0			0.588xVREG1OUT			1 0 1 1 0 0			0.844xVREG1OUT			
	0 0 1 1 0 1			0.592xVREG1OUT			1 0 1 1 0 1			0.848xVREG1OUT			
	0 0 1 1 1 0			0.596xVREG1OUT			1 0 1 1 1 0			0.852xVREG1OUT			
	0 0 1 1 1 1			0.600xVREG1OUT			1 0 1 1 1 1			0.856xVREG1OUT			
	0 0 1 1 1 0			0.604xVREG1OUT			1 0 1 1 1 0			0.860xVREG1OUT			
	0 0 1 1 1 1			0.608xVREG1OUT			1 0 1 1 1 1			0.864xVREG1OUT			
	0 0 1 1 1 0			0.612xVREG1OUT			1 0 1 1 1 0			0.868xVREG1OUT			
	0 0 1 1 1 1			0.616xVREG1OUT			1 0 1 1 1 1			0.872xVREG1OUT			
	0 1 0 0 0 0			0.620xVREG1OUT			1 1 0 0 0 0			0.876xVREG1OUT			
	0 1 0 0 0 1			0.624xVREG1OUT			1 1 0 0 0 1			0.880xVREG1OUT			
	0 1 0 0 1 0			0.628xVREG1OUT			1 1 0 0 1 0			0.884xVREG1OUT			
	0 1 0 0 1 1			0.632xVREG1OUT			1 1 0 0 1 1			0.888xVREG1OUT			
	0 1 0 1 0 0			0.636xVREG1OUT			1 1 0 1 0 0			0.892xVREG1OUT			
	0 1 0 1 0 1			0.640xVREG1OUT			1 1 0 1 0 1			0.896xVREG1OUT			
	0 1 0 1 1 0			0.644xVREG1OUT			1 1 0 1 1 0			0.900xVREG1OUT			
	0 1 0 1 1 1			0.648xVREG1OUT			1 1 0 1 1 1			0.904xVREG1OUT			
	0 1 0 1 0 0			0.652xVREG1OUT			1 1 0 1 0 0			0.908xVREG1OUT			
	0 1 0 1 0 1			0.656xVREG1OUT			1 1 0 1 0 1			0.912xVREG1OUT			
	0 1 0 1 1 0			0.660xVREG1OUT			1 1 0 1 1 0			0.916xVREG1OUT			
	0 1 0 1 1 1			0.664xVREG1OUT			1 1 0 1 1 1			0.920xVREG1OUT			
	0 1 0 1 1 0			0.668xVREG1OUT			1 1 0 1 1 0			0.924xVREG1OUT			
	0 1 0 1 1 1			0.672xVREG1OUT			1 1 0 1 1 1			0.928xVREG1OUT			
0 1 0 1 1 0			0.676xVREG1OUT			1 1 0 1 1 0			0.932xVREG1OUT				
0 1 0 1 1 1			0.680xVREG1OUT			1 1 0 1 1 1			0.936xVREG1OUT				
0 1 1 0 0 0			0.684xVREG1OUT			1 1 1 0 0 0			0.940xVREG1OUT				
0 1 1 0 0 1			0.688xVREG1OUT			1 1 1 0 0 1			0.944xVREG1OUT				
0 1 1 0 1 0			0.692xVREG1OUT			1 1 1 0 1 0			0.948xVREG1OUT				
0 1 1 0 1 1			0.696xVREG1OUT			1 1 1 0 1 1			0.952xVREG1OUT				
0 1 1 0 1 0			0.700xVREG1OUT			1 1 1 0 1 0			0.956xVREG1OUT				
0 1 1 0 1 1			0.704xVREG1OUT			1 1 1 0 1 1			0.960xVREG1OUT				

0 1 1 0 1 1 0	0.708xVREG1OUT	1 1 1 0 1 1 0	0.964xVREG1OUT
0 1 1 0 1 1 1	0.712xVREG1OUT	1 1 1 0 1 1 1	0.968xVREG1OUT
0 1 1 1 0 0 0	0.716xVREG1OUT	1 1 1 1 0 0 0	0.972xVREG1OUT
0 1 1 1 0 0 1	0.720xVREG1OUT	1 1 1 1 0 0 1	0.976xVREG1OUT
0 1 1 1 0 1 0	0.724xVREG1OUT	1 1 1 1 0 1 0	0.980xVREG1OUT
0 1 1 1 0 1 1	0.728xVREG1OUT	1 1 1 1 0 1 1	0.984xVREG1OUT
0 1 1 1 1 0 0	0.732xVREG1OUT	1 1 1 1 1 0 0	0.988xVREG1OUT
0 1 1 1 1 0 1	0.736xVREG1OUT	1 1 1 1 1 0 1	0.992xVREG1OUT
0 1 1 1 1 1 0	0.740xVREG1OUT	1 1 1 1 1 1 0	0.996xVREG1OUT
0 1 1 1 1 1 1	0.744xVREG1OUT	1 1 1 1 1 1 1	1.000xVREG1OUT

VDV(4-0): Specify the VCOM amplitude factors for panel common driving (VCOML = VCOMH – VCOM amplitude, VCOML ≥ VCL+0.5V). It is possible to setup from 0.7 to 1.32 times of VREG1OUT. When VCOMG = 0, the VDV(4-0) setup is invalid and VCOML is output VSSA

VDV[4:0]	VMAG
0 0 0 0 0	0.70xVREG1OUT
0 0 0 0 1	0.72xVREG1OUT
0 0 0 1 0	0.74xVREG1OUT
0 0 0 1 1	0.76xVREG1OUT
0 0 1 0 0	0.78xVREG1OUT
0 0 1 0 1	0.80xVREG1OUT
0 0 1 1 0	0.82xVREG1OUT
0 0 1 1 1	0.84xVREG1OUT
0 1 0 0 0	0.86xVREG1OUT
0 1 0 0 1	0.88xVREG1OUT
0 1 0 1 0	0.90xVREG1OUT
0 1 0 1 1	0.92xVREG1OUT
0 1 1 0 0	0.94xVREG1OUT
0 1 1 0 1	0.96xVREG1OUT
0 1 1 1 0	0.98xVREG1OUT
0 1 1 1 1	1.00xVREG1OUT
1 0 0 0 0	1.02xVREG1OUT
1 0 0 0 1	1.04xVREG1OUT
1 0 0 1 0	1.06xVREG1OUT
1 0 0 1 1	1.08xVREG1OUT
1 0 1 0 0	1.10xVREG1OUT
1 0 1 0 1	1.12xVREG1OUT
1 0 1 1 0	1.14xVREG1OUT
1 0 1 1 1	1.16xVREG1OUT
1 1 0 0 0	1.18xVREG1OUT
1 1 0 0 1	1.20xVREG1OUT
1 1 0 1 0	1.22xVREG1OUT
1 1 0 1 1	1.24xVREG1OUT
1 1 1 0 0	1.26xVREG1OUT
1 1 1 0 1	1.28xVREG1OUT
1 1 1 1 0	1.30xVREG1OUT
1 1 1 1 1	1.32xVREG1OUT

Restriction

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	No change
H/W Reset	

Flow Chart

6.2.61 Set Power for Normal mode (D2h)

D2H	SETNORPOW												HEX																																													
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																																														
Command	0	1	↑	-	1	1	0	1	0	0	1	0	D2																																													
1 st parameter	1	1	↑	-	0	0	0	0	0	SAP0[2:0]			XX																																													
2 nd parameter	1	1	↑	-	0	DC10[2:0]		0	DC00[2:0]			XX																																														
Description	<p>SAP0[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.</p> <table border="1"> <thead> <tr> <th colspan="3">SAP0[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Operation Stop</td> <td>Operation Stop</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0.5</td> <td>0.50</td> </tr> </tbody> </table>													SAP0[2:0]			Gamma Driver Amplifier	Source Driver Amplifier	0	0	0	Operation Stop	Operation Stop	0	0	1	1.00	1.00	0	1	0	1.00	0.75	0	1	1	1.00	0.50	1	0	0	0.75	1.00	1	0	1	0.75	0.75	1	1	0	0.75	0.50	1	1	1	0.5	0.50
	SAP0[2:0]			Gamma Driver Amplifier	Source Driver Amplifier																																																					
	0	0	0	Operation Stop	Operation Stop																																																					
	0	0	1	1.00	1.00																																																					
	0	1	0	1.00	0.75																																																					
	0	1	1	1.00	0.50																																																					
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	1	1	0	0.75	0.50																																																					
	1	1	1	0.5	0.50																																																					
	<p>DC00[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal mode.</p> <table border="1"> <thead> <tr> <th colspan="3">DC00[2:0]</th> <th>Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table>													DC00[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency									
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	1	1	0	4 x H Line Frequency																																																						
	1	1	1	8 x H Line Frequency																																																						
	<p>DC10[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal mode.</p> <table border="1"> <thead> <tr> <th colspan="3">DC10[2:0]</th> <th>Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table>													DC10[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency									
	DC10[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3																																																						
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1	1	1	8 x H Line Frequency																																																							
<p>Note: Ensure that the operation frequency of step-up circuit 1 ≥ step-up circuit 2</p>																																																										
Restriction																																																										
Register Availability	Status		Availability																																																							
	Sleep Out		Yes																																																							
	Sleep In		Yes																																																							
Default	Status		Default Value																																																							
	Power On Sequence																																																									
	S/W Reset		No change																																																							
	H/W Reset																																																									
Flow Chart																																																										

6.2.62 Set Power for Partial mode (D3h)

D3H	SETPARPOW												HEX																																													
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0																																														
Command	0	1	↑	-	1	1	0	1	0	0	1	1	D3																																													
1 st parameter	1	1	↑	-	0	0	0	0	0	SAP1[2:0]			XX																																													
2 nd parameter	1	1	↑	-	0	DC11[2:0]			0	DC01[2:0]			XX																																													
Description	<p>SAP1[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.</p> <table border="1"> <thead> <tr> <th colspan="3">SAP1[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Operation Stop</td> <td>Operation Stop</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0.5</td> <td>0.50</td> </tr> </tbody> </table>													SAP1[2:0]			Gamma Driver Amplifier	Source Driver Amplifier	0	0	0	Operation Stop	Operation Stop	0	0	1	1.00	1.00	0	1	0	1.00	0.75	0	1	1	1.00	0.50	1	0	0	0.75	1.00	1	0	1	0.75	0.75	1	1	0	0.75	0.50	1	1	1	0.5	0.50
	SAP1[2:0]			Gamma Driver Amplifier	Source Driver Amplifier																																																					
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	<p>DC01[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Partial mode.</p> <table border="1"> <thead> <tr> <th colspan="3">DC01[2:0]</th> <th>Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table>													DC01[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency									
	DC01[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1																																																						
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1	1	0	4 x H Line Frequency																																																							
1	1	1	8 x H Line Frequency																																																							
<p>DC11[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Partial mode.</p> <table border="1"> <thead> <tr> <th colspan="3">DC11[2:0]</th> <th>Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table>													DC11[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency										
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Restriction																																																										
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	Sleep Out		Yes																																																							
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Default	Status		Default Value																																																							
	Power On Sequence																																																									
	S/W Reset		No change																																																							
	H/W Reset																																																									
Flow Chart																																																										

6.2.63 Set Power for Idle mode (D4h)

D4H	SETIDLPOW																																																																																																																																	
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																					
Command	0	1	↑	-	1	1	0	1	0	1	0	0	D4																																																																																																																					
1 st parameter	1	1	↑	-	0	0	0	0	0	SAP2[2:0]			XX																																																																																																																					
2 nd parameter	1	1	↑	-	0	DC12[2:0]			0	DC02[2:0]			XX																																																																																																																					
Description	<p>SAP2[2:0]: Adjust the amount of fixed current from the fixed current source for the source and gamma driver operational amplifier in the Normal display.</p> <table border="1"> <thead> <tr> <th colspan="3">SAP2[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Operation Stop</td> <td>Operation Stop</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0.5</td> <td>0.50</td> </tr> </tbody> </table> <p>DC02[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle mode. For details, please refer to "5.6 Oscillator" section.</p> <table border="1"> <thead> <tr> <th colspan="3">DC02[2:0]</th> <th>Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table> <p>DC12[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle mode.</p> <table border="1"> <thead> <tr> <th colspan="3">DC12[2:0]</th> <th>Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>¼ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>½ x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1 x H Line Frequency</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibited</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>3 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4 x H Line Frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8 x H Line Frequency</td> </tr> </tbody> </table> <p>Note: Ensure that the operation frequency of step-up circuit 1 ≥ step-up circuit 2</p>													SAP2[2:0]			Gamma Driver Amplifier	Source Driver Amplifier	0	0	0	Operation Stop	Operation Stop	0	0	1	1.00	1.00	0	1	0	1.00	0.75	0	1	1	1.00	0.50	1	0	0	0.75	1.00	1	0	1	0.75	0.75	1	1	0	0.75	0.50	1	1	1	0.5	0.50	DC02[2:0]			Operation Frequency of Step-up Circuit 1 and Extra Step-up Circuit 1	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency	DC12[2:0]			Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3	0	0	0	¼ x H Line Frequency	0	0	1	½ x H Line Frequency	0	1	0	1 x H Line Frequency	0	1	1	Setting Inhibited	1	0	0	2 x H Line Frequency	1	0	1	3 x H Line Frequency	1	1	0	4 x H Line Frequency	1	1	1	8 x H Line Frequency
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Flow Chart																																																																																																																																		

6.2.64 Set ID (E0h)

E0 H	SETID (Set ID)												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	0	0	E0
1 st parameter	1	↑	1	-	ID1[7:0]							--	
2 nd parameter	1	↑	1	-	ID2[7:0]							--	
3 rd parameter	1	↑	1	-	ID3[7:0]							--	
4 th parameter	1	↑	1	-	ID4[7:0]							--	
Description	ID1~4: User can program any value to OTP for module number.												
Restrictions	SETEXTC turn on to enable this command.												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						All 0x00h						
	S/W Reset						No Change						
	H/W Reset						OTP value						
Flow Chart													

6.2.65 Set OTP Related Setting (E2h)

E2 H	SETOTP(Set OTP Related Setting)													HEX
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0		
Command	0	1	↑	-	1	1	1	0	0	0	1	0	E2	
1 st parameter	1	↑	1	-	OTP_MASK[7:0]								-	
2 nd parameter	1	↑	1	-	OTP_INDEX[7:0]								-	
3 rd parameter	1	↑	1	-	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]	VPP_SEL	OTP_PROG	-		
4 th parameter	1	↑	1	-	OTP_DATA[7:0]								-	
Description	This command is used to set OTP Related Setting OTP_MASK[7:0]: Bit programming mask, if 1, means don't programming this bit OTP_INDEX[6:0]: Set location of OTP to be programmed OTP_LOAD_DISABLE: When written to 1, auto load from OTP to internal register when SLPOUT command received is disabled, this is used when OTP is not yet programmed OTP_TEST: Internal use, not open. Please set "0". OTP_POR: OTP read control bit. OTP_PWE: Internal use, not open. Please set "0". OTP_PTM[1:0]: Internal use, not open. Please set "00". VPP_SEL: Internal use, not open. Please set "0". OTP_PROG: When set OTP_PROG=1, internal register begin written to OTP. Please refer to "5.14.2 OTP programming flow". OTP_DATA[7:0]: OTP data of read OTP index.													
Restrictions	SETEXTC turn on to enable this command.													
Register Availability	Status		Availability											
	Normal Mode On, Idle Mode Off, Sleep Out		Yes											
	Normal Mode On, Idle Mode On, Sleep Out		Yes											
	Partial Mode On, Idle Mode Off, Sleep Out		Yes											
	Partial Mode On, Idle Mode On, Sleep Out		Yes											
	Sleep In		Yes											
Default	Status		Default Value											
	Power On Sequence		OTP_MASK[7:0]=8'h00, OTP_INDEX[6:0]=7'h7F, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=2'b00, VPP_SEL=0, OTP_PROG=0											
	S/W Reset		No change											
	H/W Reset		OTP_MASK[7:0]=8'h00, OTP_INDEX[6:0]=7'h7F, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=2'b00, VPP_SEL=0, OTP_PROG=0											
Flow Chart														

6.2.66 SETOTPKEY (E3h)

E3 H	SET OTP_KEY												HEX												
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0													
Command	0	1	↑	-	1	1	1	0	0	0	1	1	E3												
1 st parameter	1	↑	1	-	OTP_KEY[7:0]							-													
Description	<p>OTP_KEY[7:0]: To enter or leave OTP program mode. When enter OTP program mode, other user commands can't be set. Only stop OTP program and set OTP_KEY[7:0]=55h, leave OTP program mode, then the other user commands can be set.</p> <table border="1"> <thead> <tr> <th>OTP_KEY[7:0]</th> <th>Description</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>AAh</td> <td>Enter OTP program mode</td> <td></td> </tr> <tr> <td>55h</td> <td>Leave OTP program mode</td> <td></td> </tr> <tr> <td>Other values</td> <td>Invalid</td> <td>If OTP is in OTP program mode, then keep OTP program mode If OTP is in non-OTP program mode, then keep non-OTP program mode.</td> </tr> </tbody> </table>													OTP_KEY[7:0]	Description	Note	AAh	Enter OTP program mode		55h	Leave OTP program mode		Other values	Invalid	If OTP is in OTP program mode, then keep OTP program mode If OTP is in non-OTP program mode, then keep non-OTP program mode.
	OTP_KEY[7:0]	Description	Note																						
	AAh	Enter OTP program mode																							
	55h	Leave OTP program mode																							
	Other values	Invalid	If OTP is in OTP program mode, then keep OTP program mode If OTP is in non-OTP program mode, then keep non-OTP program mode.																						
OTP_KEY[7:0] can be ignored when user want to do OTP program.																									
Restrictions	SETEXTC turn on to enable this command.																								
Register Availability	Status						Availability																		
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																		
	Normal Mode On, Idle Mode On, Sleep Out						Yes																		
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																		
	Partial Mode On, Idle Mode On, Sleep Out						Yes																		
	Sleep In or Booster Off						Yes																		
Default	Status						Default Value																		
	Power On Sequence						OTP_KEY[7:0]=8'h00																		
	S/W Reset						No change																		
	H/W Reset						OTP_KEY[7:0]=8'h00																		
Flow Chart																									

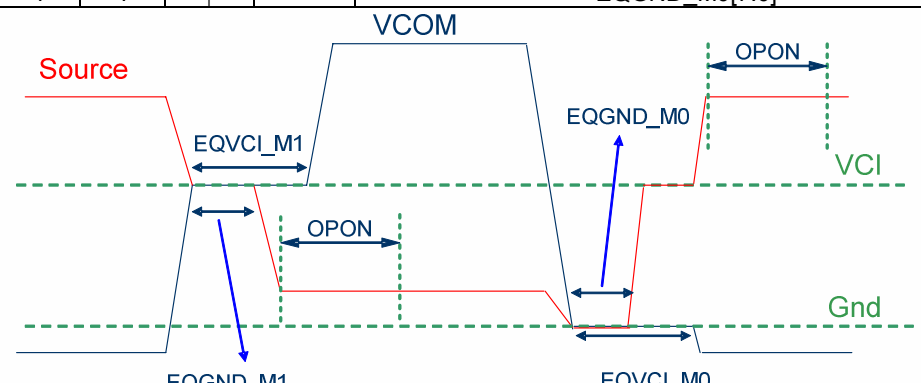
6.2.67 SETCABC(E4h)

E4 H	SETCABC																														
	DCX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	-	1	1	1	0	0	1	0	1	E4																		
1 st Parameter	1	↑	1	-	0	SEL_PWMCLK[2:0]		SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY	-	-																		
2 nd Parameter	1	↑	1	-	PWM_PERIOD[7:0]								-																		
3 rd Parameter	1	↑	1	-	0	DIM_FRAME[6:0]							-																		
Description	SEL_PWMCLK[2:0]: Internal PWM_CLK divider for CABC clock. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SEL_PWMCLK[2:0]</th> <th>Divider</th> </tr> </thead> <tbody> <tr><td>0</td><td>PWM_CLK/1</td></tr> <tr><td>1</td><td>PWM_CLK/2</td></tr> <tr><td>2</td><td>PWM_CLK/4</td></tr> <tr><td>3</td><td>PWM_CLK/8</td></tr> <tr><td>4</td><td>PWM_CLK/16</td></tr> <tr><td>5</td><td>PWM_CLK/32</td></tr> <tr><td>6</td><td>PWM_CLK/64</td></tr> <tr><td>7</td><td>PWM_CLK/128</td></tr> </tbody> </table>													SEL_PWMCLK[2:0]	Divider	0	PWM_CLK/1	1	PWM_CLK/2	2	PWM_CLK/4	3	PWM_CLK/8	4	PWM_CLK/16	5	PWM_CLK/32	6	PWM_CLK/64	7	PWM_CLK/128
	SEL_PWMCLK[2:0]	Divider																													
0	PWM_CLK/1																														
1	PWM_CLK/2																														
2	PWM_CLK/4																														
3	PWM_CLK/8																														
4	PWM_CLK/16																														
5	PWM_CLK/32																														
6	PWM_CLK/64																														
7	PWM_CLK/128																														
Note:1. PWM_CLK is OSC frequency in any interface SEL_GAIN[1:0]: Internal use, not open. Please set to "11". INVPULS: The polarity setting of PWM_OUT. Condition: BL=1, BCTRL=1 and DBV[7:0]=0x00h INVPULS=1, PWM_OUT will pull Low. INVPULS=0, PWM_OUT will pull High. SEL_BLDUTY: Internal use, not open. Please set to "1". PWM_PERIOD[7:0]: The backlight PWM output period setting. Backlight PWM output period = 1 / [(PWM_CLK / clock divider (PWM_DIV)) x (255 x PWM_PERIOD[7:0])]																															
Restriction	SETEXTC turn on to enable this command.																														
Register Availability	Status		Availability																												
	Normal Display On, Sleep Out		Yes																												
	Partial Display On, Sleep Out		Yes																												
	Sleep In or Booster Off		Yes																												
Default	Status		Default Value																												
	Power On Sequence																														
	SW Reset		PWM_PERIOD[7:0]= OTP value, DIM_FRAME[6:0]=OTP value Others=No Change																												
	H/W Reset																														
Flow Chart																															

6.2.68 Set Panel related (E9h)

E9 H	SETPANEL												
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	0	0	1	E9
1 st parameter	1	1	↑	-	0	0	0	0	SS_PANEL	0	0	BGR_PANEL	XX
Description	This command is internal use for display panel setting. SS_PANEL: The source driver output shift direction selected. When SS_PANEL = 0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed. BGR_PANEL: The color filter order direction selected.												
Restriction													
Register Availability	Status		Availability										
	Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence												
	S/W Reset		No change										
	H/W Reset												
Flow Chart													

6.2.69 Set EQ function (EEh)

EEH	SETEQ												HEX								
	DCX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0									
Command	0	1	↑	-	1	1	1	0	1	1	1	0	EE								
1 st parameter	1	1	↑	-	EQVCI_M1[7:0]							XX									
2 nd parameter	1	1	↑	-	EQGND_M1[7:0]							XX									
3 rd parameter	1	1	↑	-	EQVCI_M0[7:0]							XX									
4 th parameter	1	1	↑	-	EQGND_M0[7:0]							XX									
Description																					
Restriction																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																				
Sleep Out	Yes																				
Sleep In	Yes																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td></td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td></td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence		S/W Reset	No change	H/W Reset	
Status	Default Value																				
Power On Sequence																					
S/W Reset	No change																				
H/W Reset																					
Flow Chart																					

7. Layout Recommendation

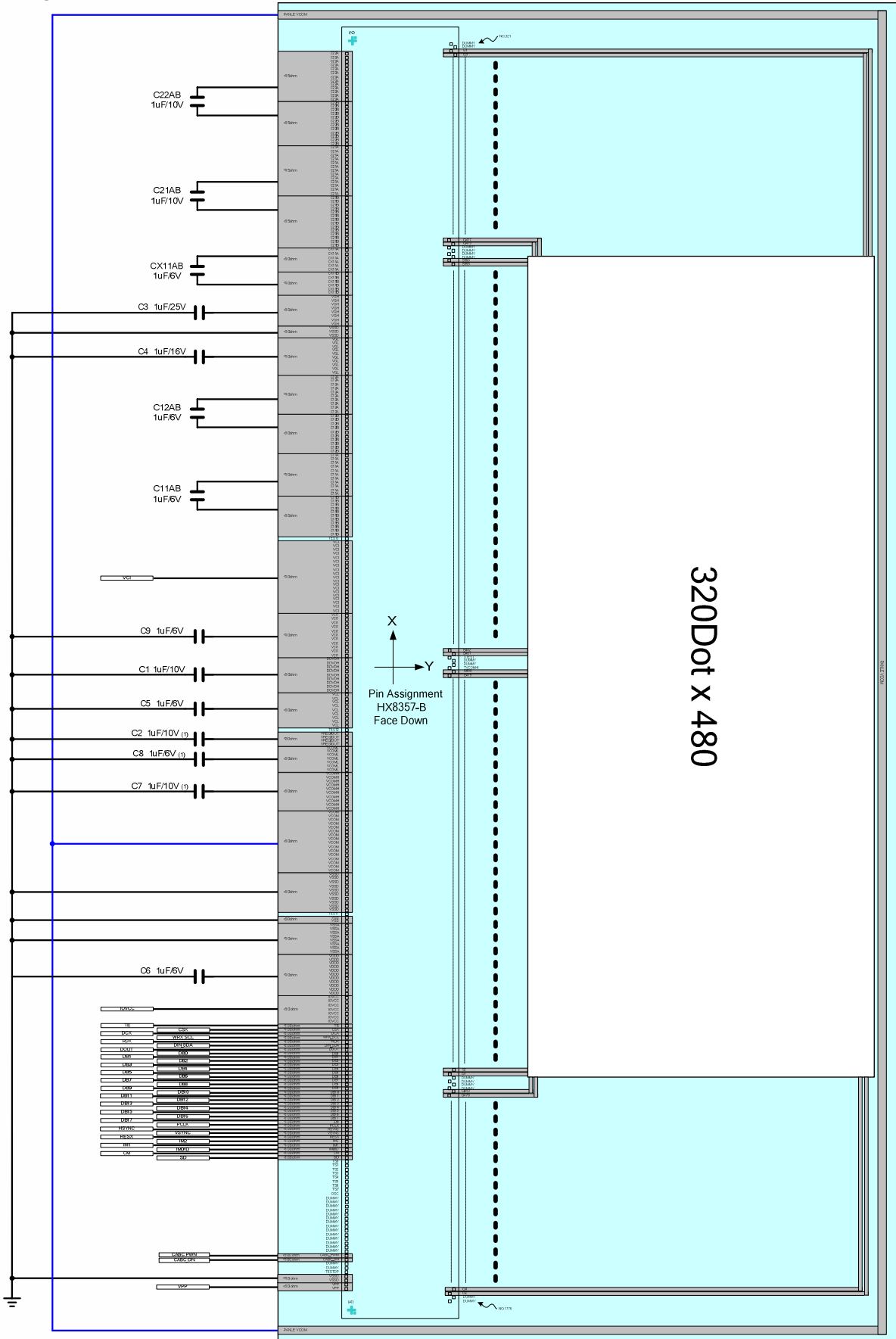


Figure 7.1: Layout Recommendation of HX8357-B

7.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VPP	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
IM[2:0], SD, CM	Input	100	Ω
CSX, DCX, WRX_SCL, RDX, RESX	Input	100	Ω
PCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
VCI1	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1OUT, VREG2OUT, VREG3OUT, VREG4OUT	Capacitor connection	30	Ω
VCOM	Panel connection	10	Ω
VCOMH, VCOML	Capacitor connection	10	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
TE, DOUT, CABC_ON, CABC_PWM	Output	100	Ω
DIN_SDA, DB[17:0]	Input/Output	100	Ω

Table 7.1: Maximum Layout Resistance

7.2 External Components Connection

Capacitor	Recommended voltage	Capacity	Note
C1 (DDVDH-VSSA)	10V	1 μ F (B characteristics)	-
C2 (VREG1OUT-VSSA)	10V	1 μ F (B characteristics)	Note ⁽¹⁾
C3 (VGH-VSSA)	25V	1 μ F (B characteristics)	-
C4 (VGL-VSSA)	16V	1 μ F (B characteristics)	-
C5 (VCL-VSSA)	6V	1 μ F (B characteristics)	-
C6(VDD-VSSA)	6V	1 μ F (B characteristics)	-
C7 (VCOMH-VSSA)	10V	1 μ F (B characteristics)	Note ⁽¹⁾
C8 (VCOML-VSSA)	6V	1 μ F (B characteristics)	Note ⁽¹⁾
C9 (VCI1-VSSA)	6V	1 μ F (B characteristics)	Note ⁽¹⁾
C11AB (C11A/B)	6V	1 μ F (B characteristics)	-
CX11AB (CX11A/B)	6V	1 μ F (B characteristics)	-
C12AB (C12A/B)	6V	1 μ F (B characteristics)	-
C21AB (C21A/B)	10V	1 μ F (B characteristics)	-
C22AB (C22A/B)	10V	1 μ F (B characteristics)	-

Note: (1) If Display quality normal, the C2, C7, C8 and C9 can remove.

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +3.6	Note ^{(1),(2)}
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +3.6	Note ^{(1),(3)}
Power Supply Voltage 3	DDVDH ~ GAND	V	-0.3 to +6.6	Note ⁽⁴⁾
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to -3.6	Note ⁽⁵⁾
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9.6	Note ⁽⁶⁾
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note ⁽⁷⁾
Power Supply Voltage 7	VSSA ~ VGL	V	0 to -16.5	Note ⁽⁸⁾
Input Voltage	V _{IN}	V	-0.3 to IOVCC+0.3	-
Operating Temperature	T _{opr}	°C	-40 to +85	Note ^{(9),(10)}
Storage Temperature	T _{stg}	°C	-55 to +110	Note ^{(9),(10)}

Note: (1) IOVCC, VSSD must be maintained.

(2) To make sure IOVCC ≥ VSSD.

(3) To make sure VCI ≥ VSSA.

(4) To make sure DDVDH ≥ VSSA.

(5) To make sure VSSA ≥ VCL.

(6) To make sure DDVDH ≥ VCL.

(7) To make sure VGH ≥ VSSA.

(8) To make sure VSSA ≥ VGL

VGH + |VGL| < 32V

(9) For die and wafer products, specified up to +85°C.

(10) This temperature specifications apply to the TCP package.

8.2 DC Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V _{IH}	V	IOVCC= 1.65 ~ 3.3V	0.7xIOVCC	-	IOVCC	-
Input low voltage	V _{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVCC	-
Output high voltage(1) (DB17-0 Pins)	V _{OH1}	V	I _{OH} = -0.1 mA	0.8xIOVCC	-	-	-
Output low voltage (DB17-0 Pins)	V _{OL1}	V	IOVCC= 1.65 ~ 2.4V I _{OL} = 0.1mA	-	-	0.2xIOVCC	-
I/O leakage current	I _{Li}	μA	V _{in} = 0 ~ IOVCC	-1	-	1	-
Current consumption during normal operation (IOVCC – VSSD)	I _{OP(IOVCC)}	μA	IOVCC=VCI=2.8V , T _A =25°C , GRAM data = 0000h, Frame rate = 60Hz, REV=0, AP=100, DC0=00, DC01=11, BT=1000, DC=111, VRH=0011, VCM=0100000,VDV=01110, VCOMG=1	-	TBD	-	-
Current consumption during normal operation (VCI – VSSA)	I _{OP(VCI)}	mA		-	TBD	-	-
Current consumption during sleep in mode (IOVCC – VSSD)	I _{SL(IOVCC)}	μA	IOVCC=VCI=2.8V , T _A =25°C	-	TBD	-	-
Current consumption during sleep in mode (VCI – VSSA)	I _{SL(VCI)}	μA		-	TBD	-	-
Current consumption during deep-standby mode (IOVCC – VSSD)	I _{D_STB(IOVCC)}	μA	IOVCC=VCI=2.8V , T _A =25°C	-	1	-	-
Current consumption during deep-standby (VCI – VSSA)	I _{D_STB(VCI)}	μA		-	1	-	-
Output voltage deviation	-	mV	-	-	TBD	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	TBD	-	-

Table 8.1: DC Characteristic

8.3 AC Characteristics

8.3.1 DBI Type-B interface characteristics

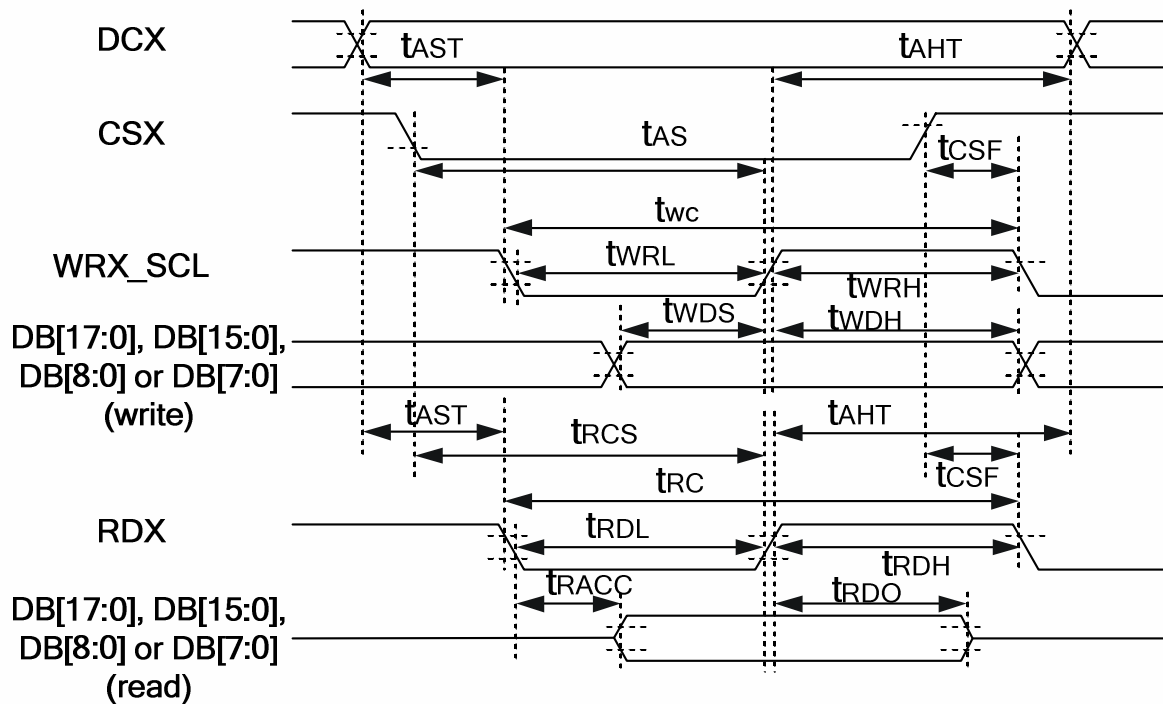


Figure 8.1: DBI Type-B interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tAST	Address setup time	10	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-		
CSX	tCS	Chip select setup time (Write)	20	-	ns	-
	tRCS	Chip select setup time (Read)	20	-		
	tCSF	Chip select wait time (Write/Read)	20	-		
WRX_SCL	tWC	Write cycle	100	-	ns	-
	tWRH	Control pulse "H" duration	30	-		
	tWRL	Control pulse "L" duration	25	-		
RDX	tRC	Read cycle	450	-	ns	-
	tRDH	Control pulse "H" duration	250	-		
	tRDL	Control pulse "L" duration	170	-		
DB[17:0], DB[15:0], DB[8:0], or DB[7:0]	tWDT	Data setup time	15	-	ns	For maximum CL=30pF For minimum CL=8pF
	tWHT	Data hold time	25	-		
	tRACC	Read access time	10	340		
	tROH	Output disable time	10	-		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.2: DBI Type-B Interface Characteristics

8.3.2 DBI Type-C interface characteristics

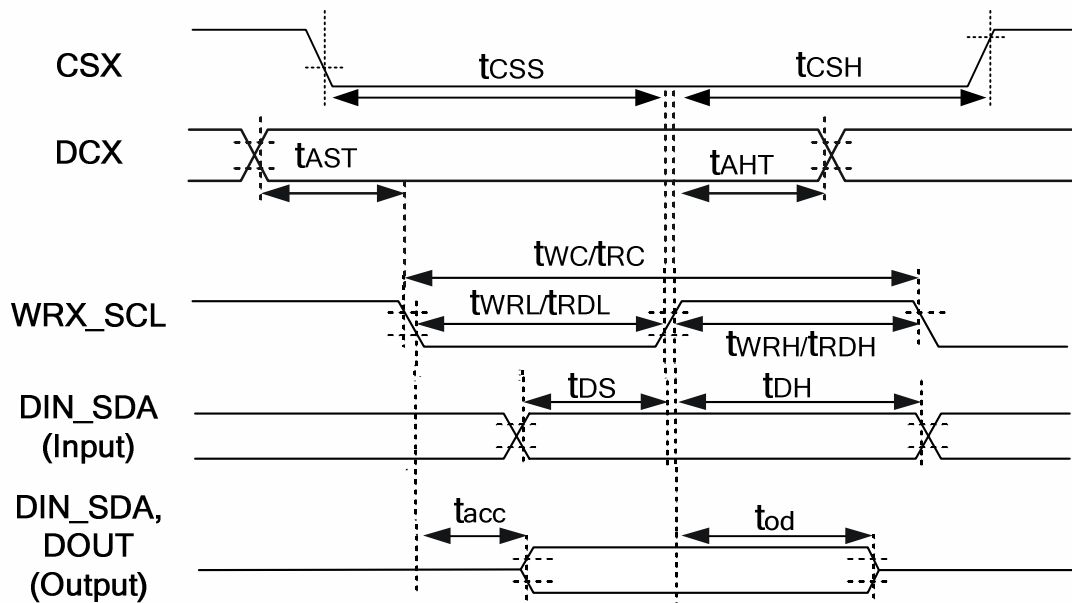


Figure 8.2: DBI Type-C interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	40	-	ns	-
	t_{CSH}	Chip select setup time (Read)	40	-	ns	
DCX	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-	ns	
WRX_SCL (Write)	t_{WC}	Write cycle	100	-	ns	-
	t_{WRH}	Control pulse "H" duration	40	-		
	t_{WRL}	Control pulse "L" duration	40	-		
WRX_SCL (Read)	t_{RC}	Read cycle	300	-	ns	-
	t_{RDH}	Control pulse "H" duration	120	-		
	t_{RDL}	Control pulse "L" duration	120	-		
DIN_SDA (Input)	t_{DS}	Data setup time	30	-	ns	For maximum C _L =30pF For minimum C _L =8pF
	t_{DH}	Data hold time	30	-		
DIN_SDA, DOUT (Output)	t_{RACC}	Read access time	-	100	ns	
	t_{OD}	Output disable time	10	-		

Note: The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.3: DBI Type-C Interface Characteristics

8.3.3 DPI Interface Characteristics

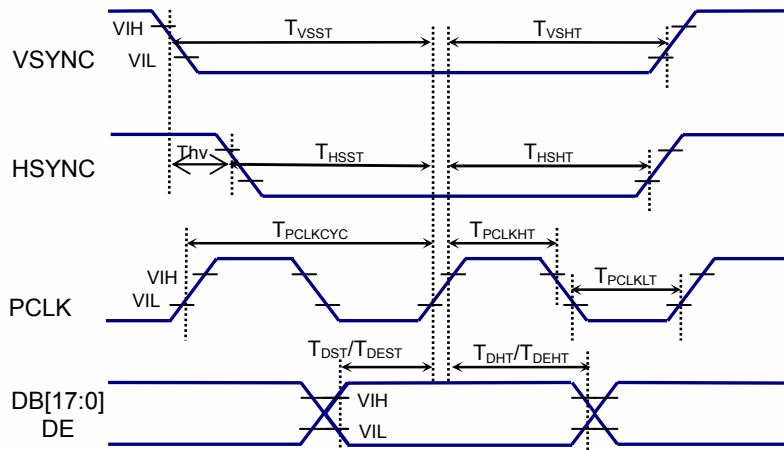


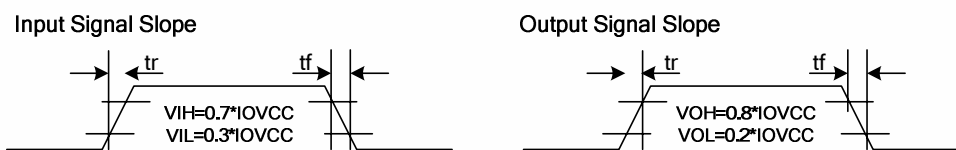
Figure 8.3: DPI Interface Characteristics 1

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

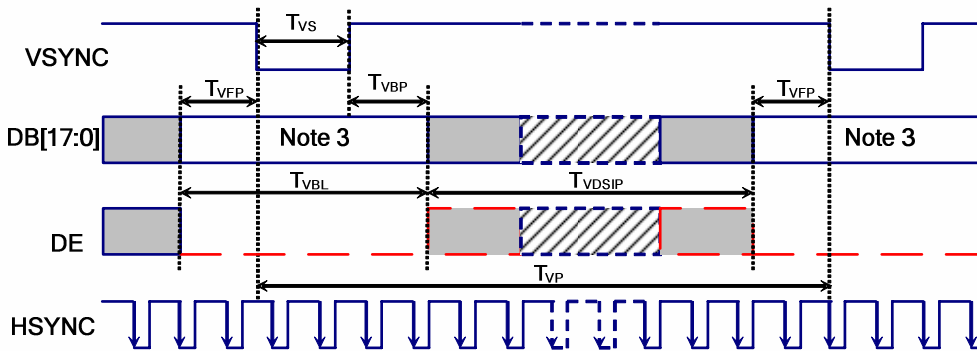
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
PCLK cycle time	T _{DCYC}	-	125	-	-	ns
Pixel low pulse width	T _{CLKLT}	-	15	-	-	ns
Pixel high pulse width	T _{CLKHT}	-	15	-	-	ns
Vertical Sync. set-up time	T _{VSSST}	-	15	-	-	ns
Vertical Sync. hold time	T _{VSSHT}	-	15	-	-	ns
Horizontal Sync. set-up time	T _{HSST}	-	15	-	-	ns
Horizontal Sync. hold time	T _{VSHT}	-	15	-	-	ns
Data Enable set-up time	T _{DEST}	-	15	-	-	ns
Data Enable hold time	T _{DEHT}	-	15	-	-	ns
Data setup time	T _{DST}	-	15	-	-	ns
Data hold time	T _{DHT}	-	15	-	-	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Table 8.4: DPI Interface Characteristics 1



Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

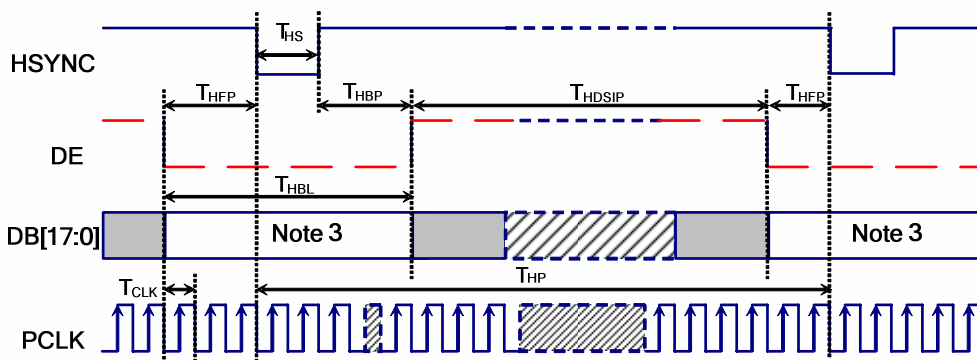


Figure 8.4: DPI Interface Characteristics 2

Item	Symbol	Condition	Specification			Unit
			Min	Typ.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	486	-	-	HS
Vertical low pulse width	T_{VS}	-	2	-	-	HS
Vertical front porch	T_{VFP}	-	2	-	-	HS
Vertical back porch	T_{VBP}	-	2	-	-	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6	-	-	HS
Vertical active area	T_{VDSIP}	-	480			HS
Vertical refresh rate	TVRR	Frame rate	-	60	-	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	326	-	-	PCLK
Horizontal low pulse width	T_{HS}	-	2	-	-	PCLK
Horizontal front porch	T_{HFP}	-	2	-	-	PCLK
Horizontal back porch	T_{HBP}	-	2	-	-	PCLK
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	6	-	-	PCLK
Horizontal active area	T_{HDISP}	-	320			PCLK
Pixel clock cycle	f_{CLKCYC}	-	-	8	-	MHz
TVRR=60Hz						

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70°C (to +85°C no damage)
 (2) Data lines can be set to "High" or "Low" during blanking time – Don't care.
 (3) HP is multiples of PCLK.

Table 8.5: DPI Interface Characteristics 2

8.3.4 Reset Input Timing

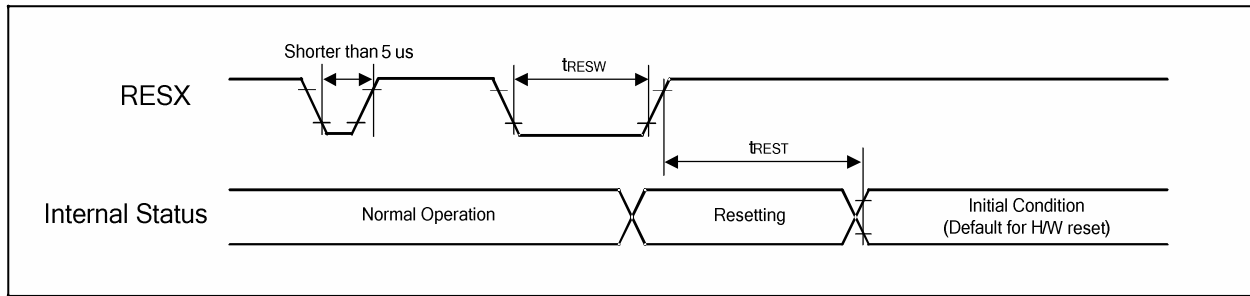


Figure 8.5: Reset Input Timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width ⁽¹⁾	RESX	10	-	-	-	µs
tREST	Reset complete time ⁽¹⁾	-	-	-	5	When reset applied during Sleep In mode	ms
		-	-	-	120	When reset applied during Sleep Out mode	ms

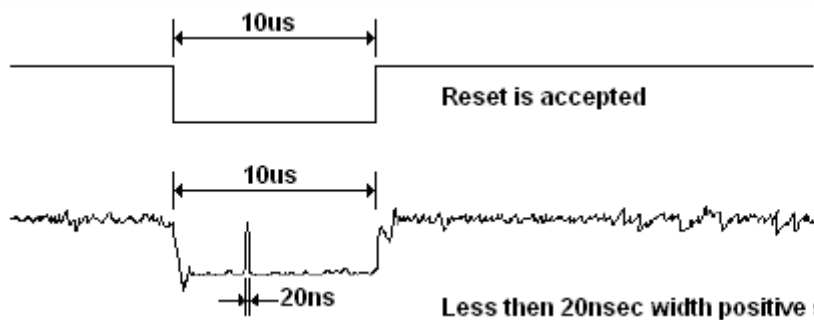
Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table. RESET Pulse.

RESET	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5 µs and 10µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 1ms after a rising edge of RESX.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.6: Reset Input Timing

9. Ordering Information

Part No.	Package
HX8357-B000 <u>PDxxx</u>	PD : mean COG xxx : mean chip thickness (μm), (default: 250 μm)

10. Revision History

Version	Date	Description of Changes
01	2010/01/18	1. New setup
01	-----	1. Modify the frame rate of DPI Interface Characteristics 2 (P186) 2. Modify Operation Frequency of Step-up Circuit 1 and 2(P169, 170, 171)