DATA SHEET

(DOC No. HX8392-A-DS)

HX8392-A

800RGB x 1280 dot, 16.7M color, with internal GRAM, LTPS Mobile Single Chip Driver

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Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This document describes Himax's HX8392-A supports WXGA resolution driving controller. The HX8392-A is designed to provide a single-chip solution that combines a source driver, gate driver control, power supply circuit to drive a LTPS dot matrix LCD with 800RGBx1280 dots at maximum.

The HX8392-A can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8392-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8392-A supports MIPI DSI (Display Serial Interface) interface mode. The interface mode is selected by the external hardware pins BS3~0.

The HX8392-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Single chip solution for a WXGA LTPS type LCD display
- Resolution:
  - 800RGB x 1280
  - 768RGB x 1280
  - 720RGB x 1280
  - 600RGB x 1024
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit 6(R):6(G):6(B))
    - 65k colours (16-bit 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 800 source channel outputs
- Internal level shifter for Gate Driver control
- Supports 1-dot / 2-dot / 4-dot / column inversion
- Gamma correction (4 preset gamma curve)
- On module VCOM control (-2 to 0V common electrode output voltage range)
- On module DC/DC converter
  - VSP=4.7 to 5.7V
  - VSN=-5.7 to -4.7V
  - Positive source output voltage level: VSPR=3.5V to 5V
  - Negative source output voltage level: VSNR=-5V to -3.5V
  - Positive gate driver output voltage level: VGH=+9V to +12V
  - Negative gate driver output voltage level: VGL=-5V to -8V
  - VCOM=-2.0V to 0V, a step=16mV
- Internal memory for image data

2.3 Display / Control interface

- Display interface types supported
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.02
    - Support D-PHY version 1.00

2.4 Input power

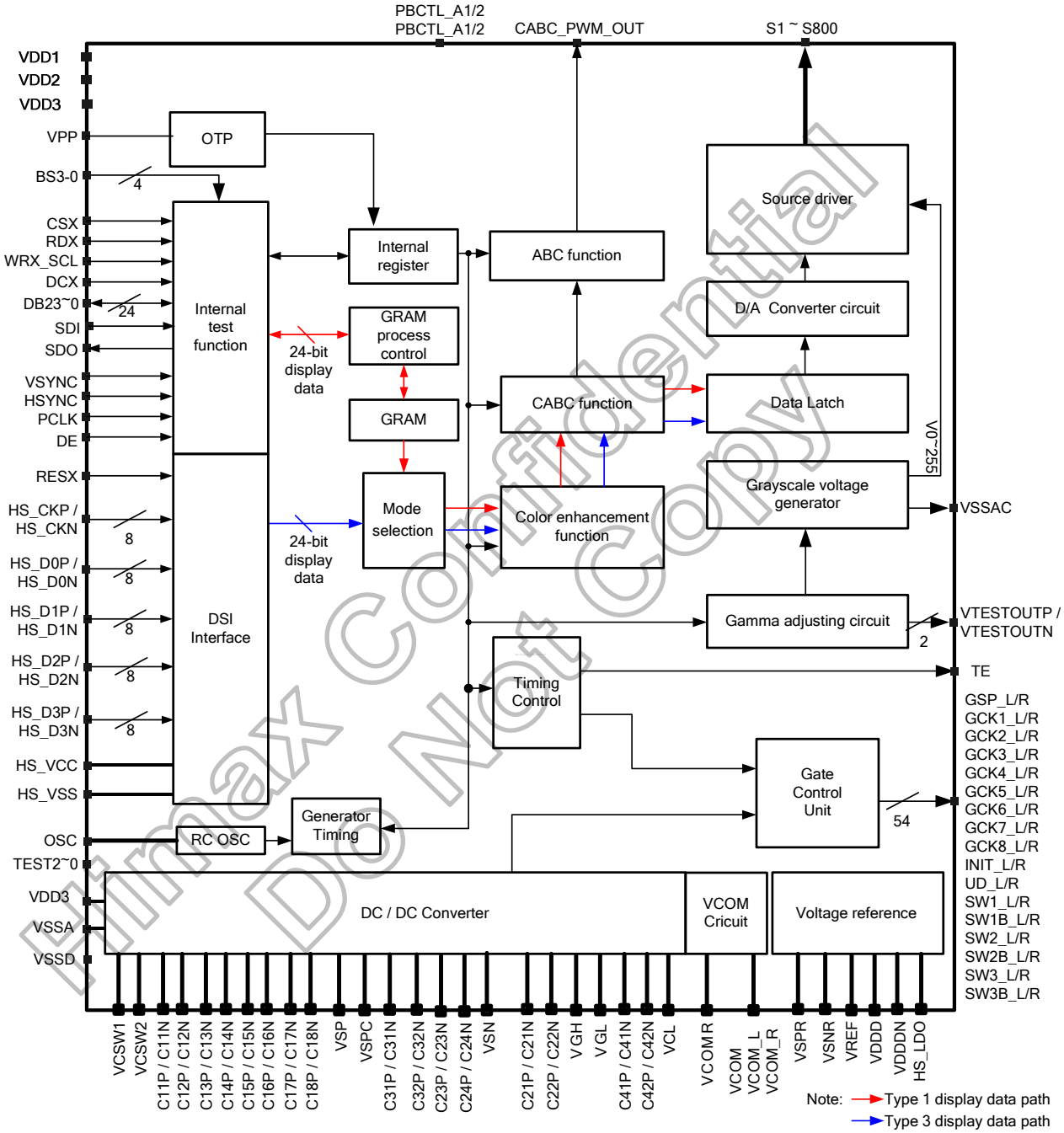
- I/O and interface power supply (VDD1): 1.65V to 3.3V
- Analog power supply (VDD2): 2.5V to 4.8V
- Logic power supply (VDD3): 2.5V to 4.8V
- High speed interface power supply (HS_VCC): 2.5V to 4.8V
- OTP programming voltage (VPP): 7.5V ± 0.2V

2.5 Miscellaneous

- Partial display mode
- Software programmable color depth mode
- Oscillator for display clock generation
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Optimized layout for COG assembly
- Temperature range: -40 to +85 ℃
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM setting ,ID setting
- Support CABC (Content Adaptive Brightness Control) function
- Support Color enhancement

3. Device Overview

3.1 Block diagram



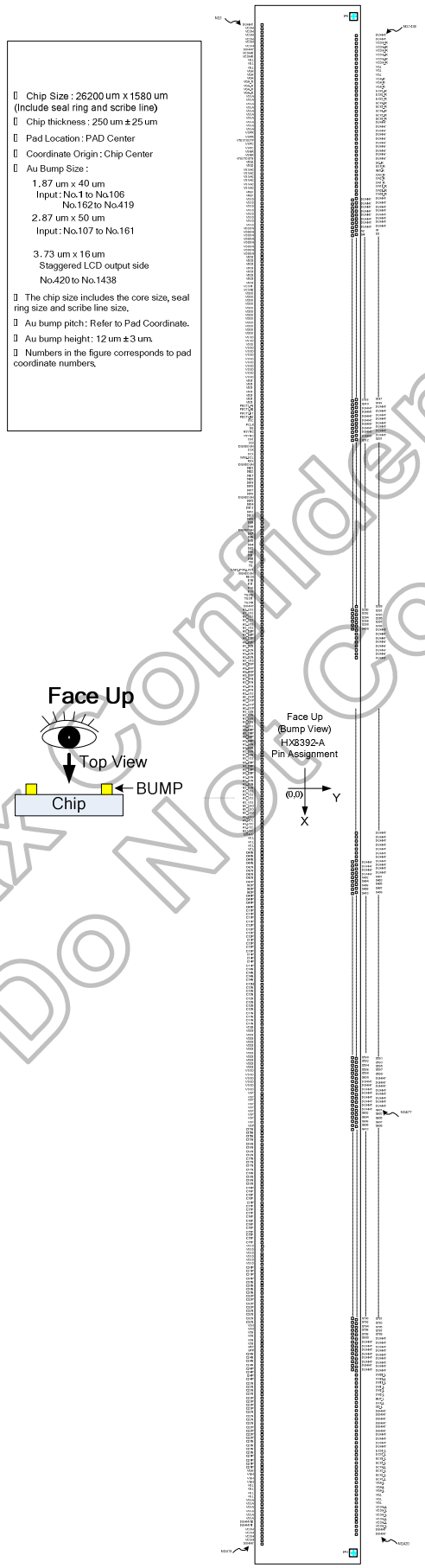
3.2 Pin description

<table>
<tr><th colspan="5">Host interface pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin no.</th><th>Connected with</th><th>Description</th></tr>
<tr><td>BS3 ~ BS0</td><td>I</td><td>4</td><td>VSSD / VDD1</td><td>Select the MPU interface mode as listed below:
<table>
<tr><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>DB pins</th><th>Display mode</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">DSI interface (note 2)</td><td rowspan="2">HS_CP/N, HS_D0P/N, HS_D1P/N, HS_D2P/N, HS_D3P/N</td><td rowspan="2">Type 1/3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="4">Other setting</td><td>Not open, only for internal test</td><td>-</td><td>-</td></tr>
</table>
Note 1: Pixel format (RGB565 / RGB666 / RGB888) is selected by DCS command (0x3Ah)
Must be connected to VSSD or VDD1.
Note 2: Input pin to select clock/data lane polarity in DSI interface only.
<table>
<tr><th>Pin name</th><th>HS_CP</th><th>HS_CN</th><th>HS_DxP</th><th>HS_DxN</th></tr>
<tr><td>BS[3-0]=”0110”</td><td>Positive</td><td>Negative</td><td>Positive</td><td>Negative</td></tr>
<tr><td>BS[3-0]=”0111”</td><td>Negative</td><td>Positive</td><td>Negative</td><td>Positive</td></tr>
</table></td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1).</td></tr>
<tr><td>RDX</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>DCX</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>WRX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>DB23~0</td><td>I/O</td><td>24</td><td>MPU</td><td>Only for internal test.
Let the unused pins open for each mode.</td></tr>
<tr><td>SDO</td><td>O</td><td>1</td><td>MPU</td><td>Only for internal test.
Let it to open .</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Only for internal test.
Please connect it to VSSD or VDD1.</td></tr>
<tr><th colspan="5">Source driver output pins</th></tr>
<tr><td>S1 to S800</td><td>O</td><td>800</td><td>LCD</td><td>Output voltages applied to the liquid crystal.
<table>
<tr><th>RGB resolution</th><th>Source channels</th></tr>
<tr><td>600RGB</td><td>S1 ~ S300, S501~S800</td></tr>
<tr><td>720RGB</td><td>S1 ~ S360, S441~S800</td></tr>
<tr><td>768RGB</td><td>S1 ~ S384, S417~S800</td></tr>
<tr><td>800RGB</td><td>S1 ~ S800</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>1</td><td>MPU</td><td>Serves TE (Tearing Effect) output pin.</td></tr>
<tr><td>TE1</td><td>O</td><td>1</td><td>MPU</td><td>Serves TE (Tearing Effect) pin of each scan line.</td></tr>
<tr><th colspan="5">Gate Driver control singal</th></tr>
<tr><td>GSP_L,
GSP_R</td><td>O</td><td>2</td><td>LCD</td><td>Gate driver start pulse.</td></tr>
<tr><td>GCK1_L,
GCK1_R</td><td>O</td><td>2</td><td>LCD</td><td>Gate driver clock 1
If not use, let it open</td></tr>
<tr><td>GCK2_L,
GCK2_R</td><td>O</td><td>2</td><td>LCD</td><td>Gate driver clock 2
If not use, let it open</td></tr>
<tr><td>GCK3~8_L,
GCK3~8_R</td><td>O</td><td>12</td><td>LCD</td><td>Gate driver clock 3~10
If not use, let it open</td></tr>
<tr><td>INIT_L,
INIT_R</td><td>O</td><td>2</td><td>LCD</td><td>Initialization signal for panel
If not use, let it open</td></tr>
<tr><td>UD_L,
UD_R</td><td>O</td><td>2</td><td>LCD</td><td>Invert control signal panel for Panel
If not use, let it open</td></tr>
</table>

SW1_L, SW1_R, SW1B_L, SW1B_R	O	4	LCD	Source driver output select signal 1 If not use, let it open
SW2_L, SW2_R, SW2B_L, SW2B_R	O	4	LCD	Source driver output select signal 2 If not use, let it open
SW3_L, SW3_R, SW3B_L, SW3B_R	O	4	LCD	Source driver output select signal 3 If not use, let it open
Power supply pins				
VDD1	I	7	Power supply	A power supply for the I/O circuit. VDD1=1.65 to 3.3V
VDD2	I	2	Power supply	A power supply for the analog power. VDD2=2.5V to 4.8V VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.
VDD3	I	20	Power supply	A power supply for the logic power, DC/DC converter VDD3=2.5V to 4.8V.
VSSA	P	16	Power supply	Analoge ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSAC	P	6	Power supply	Analoge ground. Must connect to VSSA on the FPC.
VSSD	P	32	Power supply	Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VPP	I	2	Power supply	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
Power supply pins				
VSP	I	10	Stabilizing capacitor	Input voltage from the set-up circuit (4.7V to 5.5V). it is generated from VDD3.
VSN	I	6	Stabilizing capacitor	Input voltage from the set-up circuit (-4.7V to -5.5V). it is generated from VDD3. Place a schottkey barrier diode between VSN and VGL.
VCL	I	4	Stabilizing capacitor	Input voltage from the set-up circuit (-VDD3). it is generated from VDD3.
VSPC	I	2	VSP	Positive boosting reference voltage input.
VSPR	O	2	Stabilizing capacitor	Positive regulated voltage output (3.5V to VSP - 0.5)
VSNR	O	2	Stabilizing capacitor	Positive regulated voltage output (-3.5V to VSN + 0.5)
VDDD	O	12	Stabilizing capacitor	Internal logic voltage output
VDDDN	O	8	Stabilizing capacitor	Internal logic voltage output (-2.5V fixed)
VREF	O	2	Stabilizing capacitor	Reference voltage from internal band gap circuit. The tolerance of VREF voltage is ± 3 % .(1.8V fixed)
VGH	O	7	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.
VGH_L	O	3	LCD	Output voltage for Panel. **if not used , Please open.**
VGH_R	O	7	LCD	Output voltage for Panel. **if not used , Please open.**
VGL	O	13	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL.
VCOM, VCOM_L, VCOM_R	O	22	Stabilizing capacitor	The power supply of common voltage in DC com driving. The voltage range is set between -2V to 0V. It must be connected a stabilizing capacitor 2.2u to VSSD.
VCOMR	I	2	Input	The input pad of external VCOM voltage.
DC/DC pumping				
C11P, C11N C12P, C12N C13P, C13N C14P, C14N C15P, C15N C16P, C16N C17P, C17N C18P, C18N	I/O	64	Step-up Capacitor	**In internal charge pumping mode:** Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSP voltage. **In external charge pumping mode mode:** Not used, Please open these pin.
C31P, C31N C32P, C32N C23P, C23N C24P, C24N	I/O	32	Step-up Capacitor	**In internal charge pumping mode:** Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSN voltage. **In external charge pumping mode mode:** Not used, Please open these pin.

C21P, C21N C22P, C22N	I/O	16	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH and VGL voltage.
C41P, C41N C42P, C42N	I/O	16	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VCL voltage.
VCSW1, VCSW2	O	2	-	**In internal charge pumping mode:** Not used, Please open these pin. **In external charge pumping mode mode:** VCSW1 and VCSW2 connect to HX5186-A.
CABC & ABC & Ambient light sensor				
CABC_PWM_OUT	O	1	-	Backlight on/fff control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to VDD1.
Programming PWM output				
PBCTL_A1/ PBCTL_A2	O	2	-	Dummy pin. Please open.
PBCTL_B1/ PBCTL_B2	O	2	-	Dummy pin. Please open
High speed interface parts				
HS_D0P, HS_D0N	I/O	8	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSD or open..
HS_CP, HSI_CN	I	8	DSI Host	MIPI-DSI CLOCK differential signal input pins. if not used , Please connected to VSSD or open..
HS_D1P, HS_D1N	I	8	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 1) if not used , Please connected to VSSD or open.
HS_D2P, HS_D2N	I	8	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 2) if not used , Please connected to VSSD or open..
HS_D3P, HS_D3N	I	8	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSD or open..
HS_VCC	P	4	Power Supply	Power supply for the MIPI DSI analog power. HS_VCC=2.5V to 4.8V
HS_VSS	P	14	Ground	MIPI DSI analogy ground. HS_VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
HS_LDO	O	4	Capacitor	DSI I/F: DSI regulator output pin. (1.5V) Connect to a stabilizing capacitor between HS_LDO and HS_VSS If not used, please open these pins.
Test Pins				
OSC	I	1	Open	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.(weak pull low)
TEST0	I	1	Open	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TEST1	I	1	Open	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TEST2	I	1	Open	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
VTESTOUTP	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR1 DUMMYR2	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
DUMMY	-	166	Open	Not used. Let it open.
IOGNDDUM	-	5	Open	Dummy pad. Connect to grand internally.

3.3 Pin assignment



3.4 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-12977.5	-696.5	61	VDDDN	-9377.5	-696.5	121	RDX	-5535	-696.5	181	HS_D1N	-1302.5	-696.5
2	VCOM	-12917.5	-696.5	62	VDDDN	-9317.5	-696.5	122	IOGNDDUM	-5460	-696.5	182	HS_D1N	-1242.5	-696.5
3	VCOM	-12857.5	-696.5	63	VDDDN	-9257.5	-696.5	123	DB23	-5385	-696.5	183	HS_D1N	-1182.5	-696.5
4	VCOM	-12797.5	-696.5	64	VDDDN	-9197.5	-696.5	124	DB22	-5310	-696.5	184	HS_D1N	-1122.5	-696.5
5	VCOM	-12737.5	-696.5	65	VDD3	-9137.5	-696.5	125	DB21	-5235	-696.5	185	HS_VSS	-1062.5	-696.5
6	VCOM	-12677.5	-696.5	66	VDD3	-9077.5	-696.5	126	DB20	-5160	-696.5	186	HS_CKP	-1002.5	-696.5
7	VCOM	-12617.5	-696.5	67	VDD3	-9017.5	-696.5	127	DB19	-5085	-696.5	187	HS_CKP	-942.5	-696.5
8	DUMMY	-12557.5	-696.5	68	VDD3	-8957.5	-696.5	128	DB18	-5010	-696.5	188	HS_CKP	-882.5	-696.5
9	VCOMR	-12497.5	-696.5	69	VDD3	-8897.5	-696.5	129	DB17	-4935	-696.5	189	HS_CKP	-822.5	-696.5
10	VCOMR	-12437.5	-696.5	70	VDD3	-8837.5	-696.5	130	DB16	-4860	-696.5	190	HS_CKN	-762.5	-696.5
11	VGL	-12377.5	-696.5	71	VDD3	-8777.5	-696.5	131	IOGNDDUM	-4785	-696.5	191	HS_CKN	-702.5	-696.5
12	VGL	-12317.5	-696.5	72	VDD3	-8717.5	-696.5	132	DB15	-4710	-696.5	192	HS_CKN	-642.5	-696.5
13	VGL	-12257.5	-696.5	73	VCSW1	-8657.5	-696.5	133	DB14	-4635	-696.5	193	HS_CKN	-582.5	-696.5
14	VGH	-12197.5	-696.5	74	VCSW2	-8597.5	-696.5	134	DB13	-4560	-696.5	194	HS_VSS	-522.5	-696.5
15	VGH	-12137.5	-696.5	75	VDDD	-8537.5	-696.5	135	DB12	-4485	-696.5	195	HS_D0P	-462.5	-696.5
16	VGH	-12077.5	-696.5	76	VDDD	-8477.5	-696.5	136	DB11	-4410	-696.5	196	HS_D0P	-402.5	-696.5
17	VGH_R	-12017.5	-696.5	77	VDDD	-8417.5	-696.5	137	DB10	-4335	-696.5	197	HS_D0P	-342.5	-696.5
18	VGH_R	-11957.5	-696.5	78	VDDD	-8357.5	-696.5	138	DB9	-4260	-696.5	198	HS_D0P	-282.5	-696.5
19	VGH_R	-11897.5	-696.5	79	VDDD	-8297.5	-696.5	139	DB8	-4185	-696.5	199	HS_D0N	-222.5	-696.5
20	VGH_R	-11837.5	-696.5	80	VDDD	-8237.5	-696.5	140	IOGNDDUM	-4110	-696.5	200	HS_D0N	-162.5	-696.5
21	VSSA	-11777.5	-696.5	81	VDDD	-8177.5	-696.5	141	DB7	-4035	-696.5	201	HS_D0N	-102.5	-696.5
22	VSSA	-11717.5	-696.5	82	VDDD	-8117.5	-696.5	142	DB6	-3960	-696.5	202	HS_D0N	-42.5	-696.5
23	VSSA	-11657.5	-696.5	83	VDDD	-8057.5	-696.5	143	DB5	-3885	-696.5	203	HS_VSS	17.5	-696.5
24	VSSA	-11597.5	-696.5	84	VDDD	-7997.5	-696.5	144	DB4	-3810	-696.5	204	HS_D3P	77.5	-696.5
25	VSSA	-11537.5	-696.5	85	VDDD	-7937.5	-696.5	145	DB3	-3735	-696.5	205	HS_D3P	137.5	-696.5
26	VSSA	-11477.5	-696.5	86	VDDD	-7877.5	-696.5	146	DB2	-3660	-696.5	206	HS_D3P	197.5	-696.5
27	VSSA	-11417.5	-696.5	87	VSSD	-7817.5	-696.5	147	DB1	-3585	-696.5	207	HS_D3P	257.5	-696.5
28	VSSA	-11357.5	-696.5	88	VSSD	-7757.5	-696.5	148	DB0	-3510	-696.5	208	HS_D3N	317.5	-696.5
29	VSSA	-11297.5	-696.5	89	VSSD	-7697.5	-696.5	149	TE1	-3435	-696.5	209	HS_D3N	377.5	-696.5
30	VSSA	-11237.5	-696.5	90	VSSD	-7637.5	-696.5	150	TE	-3360	-696.5	210	HS_D3N	437.5	-696.5
31	VSPR	-11177.5	-696.5	91	VSSD	-7577.5	-696.5	151	CABC_PWM_OUT	-3285	-696.5	211	HS_D3N	497.5	-696.5
32	VSPR	-11117.5	-696.5	92	VSSD	-7517.5	-696.5	152	IOGNDDUM	-3210	-696.5	212	HS_VSS	557.5	-696.5
33	VTESTOUTP	-11057.5	-696.5	93	VSSD	-7457.5	-696.5	153	RESX	-3135	-696.5	213	HS_VSS	617.5	-696.5
34	VSPC	-10997.5	-696.5	94	VSSD	-7397.5	-696.5	154	BS0	-3060	-696.5	214	HS_VSS	677.5	-696.5
35	VSPC	-10937.5	-696.5	95	VSSD	-7337.5	-696.5	155	BS1	-2985	-696.5	215	HS_VSS	737.5	-696.5
36	VSNR	-10877.5	-696.5	96	VSSD	-7277.5	-696.5	156	BS2	-2910	-696.5	216	HS_LDO	797.5	-696.5
37	VSNR	-10817.5	-696.5	97	VSSD	-7217.5	-696.5	157	BS3	-2835	-696.5	217	HS_LDO	857.5	-696.5
38	VTESTOUTN	-10757.5	-696.5	98	VSSD	-7157.5	-696.5	158	TEST2	-2760	-696.5	218	HS_LDO	917.5	-696.5
39	VDD2	-10697.5	-696.5	99	VDD1	-7097.5	-696.5	159	TEST1	-2685	-696.5	219	HS_LDO	977.5	-696.5
40	VDD2	-10637.5	-696.5	100	VDD1	-7037.5	-696.5	160	TEST0	-2610	-696.5	220	HS_VCC	1037.5	-696.5
41	VSSAC	-10577.5	-696.5	101	VDD1	-6977.5	-696.5	161	DUMMY	-2535	-696.5	221	HS_VCC	1097.5	-696.5
42	VSSAC	-10517.5	-696.5	102	VDD1	-6917.5	-696.5	162	HS_VSS	-2442.5	-696.5	222	HS_VCC	1157.5	-696.5
43	VSSAC	-10457.5	-696.5	103	VDD1	-6857.5	-696.5	163	HS_VSS	-2382.5	-696.5	223	HS_VCC	1217.5	-696.5
44	VSSAC	-10397.5	-696.5	104	VDD1	-6797.5	-696.5	164	HS_VSS	-2322.5	-696.5	224	DUMMY	1277.5	-696.5
45	VSSAC	-10337.5	-696.5	105	VDD1	-6737.5	-696.5	165	HS_VSS	-2262.5	-696.5	225	VCL	1337.5	-696.5
46	VSSAC	-10277.5	-696.5	106	PVCTL_A1	-6660	-696.5	166	HS_VSS	-2202.5	-696.5	226	VCL	1397.5	-696.5
47	VREF	-10217.5	-696.5	107	PVCTL_A2	-6585	-696.5	167	HS_VSS	-2142.5	-696.5	227	VCL	1457.5	-696.5
48	VREF	-10157.5	-696.5	108	PVCTL_B1	-6510	-696.5	168	HS_D2P	-2082.5	-696.5	228	VCL	1517.5	-696.5
49	VSSD	-10097.5	-696.5	109	PVCTL_B2	-6435	-696.5	169	HS_D2P	-2022.5	-696.5	229	C41N	1577.5	-696.5
50	VSSD	-10037.5	-696.5	110	OSC	-6360	-696.5	170	HS_D2P	-1962.5	-696.5	230	C41N	1637.5	-696.5
51	VSSD	-9977.5	-696.5	111	PCLK	-6285	-696.5	171	HS_D2P	-1902.5	-696.5	231	C41N	1697.5	-696.5
52	VSSD	-9917.5	-696.5	112	DE	-6210	-696.5	172	HS_D2N	-1842.5	-696.5	232	C41N	1757.5	-696.5
53	VSSD	-9857.5	-696.5	113	HSYNC	-6135	-696.5	173	HS_D2N	-1782.5	-696.5	233	C42N	1817.5	-696.5
54	VSSD	-9797.5	-696.5	114	VSYNC	-6060	-696.5	174	HS_D2N	-1722.5	-696.5	234	C42N	1877.5	-696.5
55	VSSD	-9737.5	-696.5	115	SDO	-5985	-696.5	175	HS_D2N	-1662.5	-696.5	235	C42N	1937.5	-696.5
56	VSSD	-9677.5	-696.5	116	SDI	-5910	-696.5	176	HS_VSS	-1602.5	-696.5	236	C42N	1997.5	-696.5
57	VDDDN	-9617.5	-696.5	117	IOGNDDUM	-5835	-696.5	177	HS_D1P	-1542.5	-696.5	237	C42P	2057.5	-696.5
58	VDDDN	-9557.5	-696.5	118	CSX	-5760	-696.5	178	HS_D1P	-1482.5	-696.5	238	C42P	2117.5	-696.5
59	VDDDN	-9497.5	-696.5	119	DCX	-5685	-696.5	179	HS_D1P	-1422.5	-696.5	239	C42P	2177.5	-696.5
60	VDDDN	-9437.5	-696.5	120	WRX_SCL	-5610	-696.5	180	HS_D1P	-1362.5	-696.5	240	C42P	2237.5	-696.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
241	C41P	2297.5	-696.5	301	VSP	5897.5	-696.5	361	VSN	9497.5	-696.5	421	DUMMY	12711	703.5
242	C41P	2357.5	-696.5	302	VSP	5957.5	-696.5	362	VSN	9557.5	-696.5	422	VCOM	12641	703.5
243	C41P	2417.5	-696.5	303	VSP	6017.5	-696.5	363	VSN	9617.5	-696.5	423	VCOM	12571	703.5
244	C41P	2477.5	-696.5	304	VSP	6077.5	-696.5	364	VSN	9677.5	-696.5	424	VCOM	12501	703.5
245	C11P	2537.5	-696.5	305	C15N	6137.5	-696.5	365	VPP	9737.5	-696.5	425	VCOM	12431	703.5
246	C11P	2597.5	-696.5	306	C15N	6197.5	-696.5	366	VPP	9797.5	-696.5	426	VCOM	12361	703.5
247	C11P	2657.5	-696.5	307	C15N	6257.5	-696.5	367	C24N	9857.5	-696.5	427	VCOM	12291	703.5
248	C11P	2717.5	-696.5	308	C15N	6317.5	-696.5	368	C24N	9917.5	-696.5	428	VGL	12221	703.5
249	C12P	2777.5	-696.5	309	C16N	6377.5	-696.5	369	C24N	9977.5	-696.5	429	VGL	12151	703.5
250	C12P	2837.5	-696.5	310	C16N	6437.5	-696.5	370	C24N	10037.5	-696.5	430	VGL	12081	703.5
251	C12P	2897.5	-696.5	311	C16N	6497.5	-696.5	371	C24P	10097.5	-696.5	431	VGH_L	12011	703.5
252	C12P	2957.5	-696.5	312	C16N	6557.5	-696.5	372	C24P	10157.5	-696.5	432	VGH_L	11941	703.5
253	C13P	3017.5	-696.5	313	C17N	6617.5	-696.5	373	C24P	10217.5	-696.5	433	VGH_L	11871	703.5
254	C13P	3077.5	-696.5	314	C17N	6677.5	-696.5	374	C24P	10277.5	-696.5	434	GCK1_L	11801	703.5
255	C13P	3137.5	-696.5	315	C17N	6737.5	-696.5	375	C23N	10337.5	-696.5	435	GCK2_L	11731	703.5
256	C13P	3197.5	-696.5	316	C17N	6797.5	-696.5	376	C23N	10397.5	-696.5	436	GCK3_L	11661	703.5
257	C14P	3257.5	-696.5	317	C18N	6857.5	-696.5	377	C23N	10457.5	-696.5	437	GCK4_L	11591	703.5
258	C14P	3317.5	-696.5	318	C18N	6917.5	-696.5	378	C23N	10517.5	-696.5	438	GCK5_L	11521	703.5
259	C14P	3377.5	-696.5	319	C18N	6977.5	-696.5	379	C23P	10577.5	-696.5	439	GCK6_L	11451	703.5
260	C14P	3437.5	-696.5	320	C18N	7037.5	-696.5	380	C23P	10637.5	-696.5	440	GCK7_L	11381	703.5
261	C14N	3497.5	-696.5	321	C18P	7097.5	-696.5	381	C23P	10697.5	-696.5	441	GCK8_L	11311	703.5
262	C14N	3557.5	-696.5	322	C18P	7157.5	-696.5	382	C23P	10757.5	-696.5	442	DUMMY	11241	703.5
263	C14N	3617.5	-696.5	323	C18P	7217.5	-696.5	383	C22N	10817.5	-696.5	443	DUMMY	11171	703.5
264	C14N	3677.5	-696.5	324	C18P	7277.5	-696.5	384	C22N	10877.5	-696.5	444	DUMMY	11101	703.5
265	C13N	3737.5	-696.5	325	C17P	7337.5	-696.5	385	C22N	10937.5	-696.5	445	DUMMY	11031	703.5
266	C13N	3797.5	-696.5	326	C17P	7397.5	-696.5	386	C22N	10997.5	-696.5	446	DUMMY	10961	703.5
267	C13N	3857.5	-696.5	327	C17P	7457.5	-696.5	387	C22P	11057.5	-696.5	447	DUMMY	10891	703.5
268	C13N	3917.5	-696.5	328	C17P	7517.5	-696.5	388	C22P	11117.5	-696.5	448	DUMMY	10821	703.5
269	C12N	3977.5	-696.5	329	C16P	7577.5	-696.5	389	C22P	11177.5	-696.5	449	DUMMY	10751	703.5
270	C12N	4037.5	-696.5	330	C16P	7637.5	-696.5	390	C22P	11237.5	-696.5	450	DUMMY	10681	703.5
271	C12N	4097.5	-696.5	331	C16P	7697.5	-696.5	391	C21N	11297.5	-696.5	451	DUMMY	10611	703.5
272	C12N	4157.5	-696.5	332	C16P	7757.5	-696.5	392	C21N	11357.5	-696.5	452	UD_L	10541	703.5
273	C11N	4217.5	-696.5	333	C15P	7817.5	-696.5	393	C21N	11417.5	-696.5	453	GSP_L	10471	703.5
274	C11N	4277.5	-696.5	334	C15P	7877.5	-696.5	394	C21N	11477.5	-696.5	454	INIT_L	10401	703.5
275	C11N	4337.5	-696.5	335	C15P	7937.5	-696.5	395	C21P	11537.5	-696.5	455	SW3_L	10331	703.5
276	C11N	4397.5	-696.5	336	C15P	7997.5	-696.5	396	C21P	11597.5	-696.5	456	SW2_L	10261	703.5
277	VDD3	4457.5	-696.5	337	VSSD	8057.5	-696.5	397	C21P	11657.5	-696.5	457	SW1_L	10191	703.5
278	VDD3	4517.5	-696.5	338	VSSD	8117.5	-696.5	398	C21P	11717.5	-696.5	458	SW1B_L	10121	703.5
279	VDD3	4577.5	-696.5	339	VSSD	8177.5	-696.5	399	VGH	11777.5	-696.5	459	SW2B_L	10051	703.5
280	VDD3	4637.5	-696.5	340	VSSD	8237.5	-696.5	400	VGH	11837.5	-696.5	460	SW3B_L	9981	703.5
281	VDD3	4697.5	-696.5	341	VSSD	8297.5	-696.5	401	VGH	11897.5	-696.5	461	DUMMY	9911	703.5
282	VDD3	4757.5	-696.5	342	VSSD	8357.5	-696.5	402	VGH	11957.5	-696.5	462	DUMMY	9893	613.5
283	VDD3	4817.5	-696.5	343	C31P	8417.5	-696.5	403	VGL	12017.5	-696.5	463	DUMMY	9875	703.5
284	VDD3	4877.5	-696.5	344	C31P	8477.5	-696.5	404	VGL	12077.5	-696.5	464	DUMMY	9857	613.5
285	VDD3	4937.5	-696.5	345	C31P	8537.5	-696.5	405	VGL	12137.5	-696.5	465	DUMMY	9839	703.5
286	VDD3	4997.5	-696.5	346	C31P	8597.5	-696.5	406	VGL	12197.5	-696.5	466	DUMMY	9821	613.5
287	VDD3	5057.5	-696.5	347	C31N	8657.5	-696.5	407	VSSA	12257.5	-696.5	467	DUMMY	9803	703.5
288	VDD3	5117.5	-696.5	348	C31N	8717.5	-696.5	408	VSSA	12317.5	-696.5	468	DUMMY	9785	613.5
289	VSSD	5177.5	-696.5	349	C31N	8777.5	-696.5	409	VSSA	12377.5	-696.5	469	DUMMY	9767	703.5
290	VSSD	5237.5	-696.5	350	C31N	8837.5	-696.5	410	VSSA	12437.5	-696.5	470	DUMMY	9749	613.5
291	VSSD	5297.5	-696.5	351	C32P	8897.5	-696.5	411	VSSA	12497.5	-696.5	471	DUMMY	9731	703.5
292	VSSD	5357.5	-696.5	352	C32P	8957.5	-696.5	412	VSSA	12557.5	-696.5	472	DUMMY	9713	613.5
293	VSSD	5417.5	-696.5	353	C32P	9017.5	-696.5	413	DUMMYR2	12617.5	-696.5	473	DUMMY	9695	703.5
294	VSSD	5477.5	-696.5	354	C32P	9077.5	-696.5	414	DUMMYR1	12677.5	-696.5	474	DUMMY	9677	613.5
295	VSP	5537.5	-696.5	355	C32N	9137.5	-696.5	415	VCOM	12737.5	-696.5	475	DUMMY	9659	703.5
296	VSP	5597.5	-696.5	356	C32N	9197.5	-696.5	416	VCOM	12797.5	-696.5	476	DUMMY	9641	613.5
297	VSP	5657.5	-696.5	357	C32N	9257.5	-696.5	417	VCOM	12857.5	-696.5	477	DUMMY	9623	703.5
298	VSP	5717.5	-696.5	358	C32N	9317.5	-696.5	418	VCOM	12917.5	-696.5	478	S800	9605	613.5
299	VSP	5777.5	-696.5	359	VSN	9377.5	-696.5	419	DUMMY	12977.5	-696.5	479	S799	9587	703.5
300	VSP	5837.5	-696.5	360	VSN	9437.5	-696.5	420	DUMMY	12781	703.5	480	S798	9569	613.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
481	S797	9551	703.5	541	S737	8471	703.5	601	S677	7391	703.5	661	S617	6311	703.5
482	S796	9533	613.5	542	S736	8453	613.5	602	S676	7373	613.5	662	S616	6293	613.5
483	S795	9515	703.5	543	S735	8435	703.5	603	S675	7355	703.5	663	S615	6275	703.5
484	S794	9497	613.5	544	S734	8417	613.5	604	S674	7337	613.5	664	S614	6257	613.5
485	S793	9479	703.5	545	S733	8399	703.5	605	S673	7319	703.5	665	S613	6239	703.5
486	S792	9461	613.5	546	S732	8381	613.5	606	S672	7301	613.5	666	S612	6221	613.5
487	S791	9443	703.5	547	S731	8363	703.5	607	S671	7283	703.5	667	S611	6203	703.5
488	S790	9425	613.5	548	S730	8345	613.5	608	S670	7265	613.5	668	S610	6185	613.5
489	S789	9407	703.5	549	S729	8327	703.5	609	S669	7247	703.5	669	S609	6167	703.5
490	S788	9389	613.5	550	S728	8309	613.5	610	S668	7229	613.5	670	S608	6149	613.5
491	S787	9371	703.5	551	S727	8291	703.5	611	S667	7211	703.5	671	S607	6131	703.5
492	S786	9353	613.5	552	S726	8273	613.5	612	S666	7193	613.5	672	S606	6113	613.5
493	S785	9335	703.5	553	S725	8255	703.5	613	S665	7175	703.5	673	S605	6095	703.5
494	S784	9317	613.5	554	S724	8237	613.5	614	S664	7157	613.5	674	S604	6077	613.5
495	S783	9299	703.5	555	S723	8219	703.5	615	S663	7139	703.5	675	S603	6059	703.5
496	S782	9281	613.5	556	S722	8201	613.5	616	S662	7121	613.5	676	S602	6041	613.5
497	S781	9263	703.5	557	S721	8183	703.5	617	S661	7103	703.5	677	S601	6023	703.5
498	S780	9245	613.5	558	S720	8165	613.5	618	S660	7085	613.5	678	DUMMY	6005	613.5
499	S779	9227	703.5	559	S719	8147	703.5	619	S659	7067	703.5	679	DUMMY	5987	703.5
500	S778	9209	613.5	560	S718	8129	613.5	620	S658	7049	613.5	680	DUMMY	5969	613.5
501	S777	9191	703.5	561	S717	8111	703.5	621	S657	7031	703.5	681	DUMMY	5951	703.5
502	S776	9173	613.5	562	S716	8093	613.5	622	S656	7013	613.5	682	DUMMY	5933	613.5
503	S775	9155	703.5	563	S715	8075	703.5	623	S655	6995	703.5	683	DUMMY	5915	703.5
504	S774	9137	613.5	564	S714	8057	613.5	624	S654	6977	613.5	684	DUMMY	5897	613.5
505	S773	9119	703.5	565	S713	8039	703.5	625	S653	6959	703.5	685	DUMMY	5879	703.5
506	S772	9101	613.5	566	S712	8021	613.5	626	S652	6941	613.5	686	DUMMY	5861	613.5
507	S771	9083	703.5	567	S711	8003	703.5	627	S651	6923	703.5	687	DUMMY	5843	703.5
508	S770	9065	613.5	568	S710	7985	613.5	628	S650	6905	613.5	688	DUMMY	5825	613.5
509	S769	9047	703.5	569	S709	7967	703.5	629	S649	6887	703.5	689	DUMMY	5807	703.5
510	S768	9029	613.5	570	S708	7949	613.5	630	S648	6869	613.5	690	DUMMY	5789	613.5
511	S767	9011	703.5	571	S707	7931	703.5	631	S647	6851	703.5	691	DUMMY	5771	703.5
512	S766	8993	613.5	572	S706	7913	613.5	632	S646	6833	613.5	692	DUMMY	5753	613.5
513	S765	8975	703.5	573	S705	7895	703.5	633	S645	6815	703.5	693	DUMMY	5735	703.5
514	S764	8957	613.5	574	S704	7877	613.5	634	S644	6797	613.5	694	S600	5717	613.5
515	S763	8939	703.5	575	S703	7859	703.5	635	S643	6779	703.5	695	S599	5699	703.5
516	S762	8921	613.5	576	S702	7841	613.5	636	S642	6761	613.5	696	S598	5681	613.5
517	S761	8903	703.5	577	S701	7823	703.5	637	S641	6743	703.5	697	S597	5663	703.5
518	S760	8885	613.5	578	S700	7805	613.5	638	S640	6725	613.5	698	S596	5645	613.5
519	S759	8867	703.5	579	S699	7787	703.5	639	S639	6707	703.5	699	S595	5627	703.5
520	S758	8849	613.5	580	S698	7769	613.5	640	S638	6689	613.5	700	S594	5609	613.5
521	S757	8831	703.5	581	S697	7751	703.5	641	S637	6671	703.5	701	S593	5591	703.5
522	S756	8813	613.5	582	S696	7733	613.5	642	S636	6653	613.5	702	S592	5573	613.5
523	S755	8795	703.5	583	S695	7715	703.5	643	S635	6635	703.5	703	S591	5555	703.5
524	S754	8777	613.5	584	S694	7697	613.5	644	S634	6617	613.5	704	S590	5537	613.5
525	S753	8759	703.5	585	S693	7679	703.5	645	S633	6599	703.5	705	S589	5519	703.5
526	S752	8741	613.5	586	S692	7661	613.5	646	S632	6581	613.5	706	S588	5501	613.5
527	S751	8723	703.5	587	S691	7643	703.5	647	S631	6563	703.5	707	S587	5483	703.5
528	S750	8705	613.5	588	S690	7625	613.5	648	S630	6545	613.5	708	S586	5465	613.5
529	S749	8687	703.5	589	S689	7607	703.5	649	S629	6527	703.5	709	S585	5447	703.5
530	S748	8669	613.5	590	S688	7589	613.5	650	S628	6509	613.5	710	S584	5429	613.5
531	S747	8651	703.5	591	S687	7571	703.5	651	S627	6491	703.5	711	S583	5411	703.5
532	S746	8633	613.5	592	S686	7553	613.5	652	S626	6473	613.5	712	S582	5393	613.5
533	S745	8615	703.5	593	S685	7535	703.5	653	S625	6455	703.5	713	S581	5375	703.5
534	S744	8597	613.5	594	S684	7517	613.5	654	S624	6437	613.5	714	S580	5357	613.5
535	S743	8579	703.5	595	S683	7499	703.5	655	S623	6419	703.5	715	S579	5339	703.5
536	S742	8561	613.5	596	S682	7481	613.5	656	S622	6401	613.5	716	S578	5321	613.5
537	S741	8543	703.5	597	S681	7463	703.5	657	S621	6383	703.5	717	S577	5303	703.5
538	S740	8525	613.5	598	S680	7445	613.5	658	S620	6365	613.5	718	S576	5285	613.5
539	S739	8507	703.5	599	S679	7427	703.5	659	S619	6347	703.5	719	S575	5267	703.5
540	S738	8489	613.5	600	S678	7409	613.5	660	S618	6329	613.5	720	S574	5249	613.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
721	S573	5231	703.5	781	S513	4151	703.5	841	S453	3071	703.5	901	DUMMY	1991	703.5
722	S572	5213	613.5	782	S512	4133	613.5	842	S452	3053	613.5	902	DUMMY	1925	703.5
723	S571	5195	703.5	783	S511	4115	703.5	843	S451	3035	703.5	903	DUMMY	1855	703.5
724	S570	5177	613.5	784	S510	4097	613.5	844	S450	3017	613.5	904	DUMMY	1785	703.5
725	S569	5159	703.5	785	S509	4079	703.5	845	S449	2999	703.5	905	DUMMY	1715	703.5
726	S568	5141	613.5	786	S508	4061	613.5	846	S448	2981	613.5	906	DUMMY	1645	703.5
727	S567	5123	703.5	787	S507	4043	703.5	847	S447	2963	703.5	907	DUMMY	1575	703.5
728	S566	5105	613.5	788	S506	4025	613.5	848	S446	2945	613.5	908	DUMMY	1505	703.5
729	S565	5087	703.5	789	S505	4007	703.5	849	S445	2927	703.5	909	DUMMY	1435	703.5
730	S564	5069	613.5	790	S504	3989	613.5	850	S444	2909	613.5	910	DUMMY	1365	703.5
731	S563	5051	703.5	791	S503	3971	703.5	851	S443	2891	703.5	911	DUMMY	1295	703.5
732	S562	5033	613.5	792	S502	3953	613.5	852	S442	2873	613.5	912	DUMMY	1225	703.5
733	S561	5015	703.5	793	S501	3935	703.5	853	S441	2855	703.5	913	DUMMY	1155	703.5
734	S560	4997	613.5	794	S500	3917	613.5	854	S440	2837	613.5	914	DUMMY	1085	703.5
735	S559	4979	703.5	795	S499	3899	703.5	855	S439	2819	703.5	915	DUMMY	1015	703.5
736	S558	4961	613.5	796	S498	3881	613.5	856	S438	2801	613.5	916	DUMMY	945	703.5
737	S557	4943	703.5	797	S497	3863	703.5	857	S437	2783	703.5	917	DUMMY	875	703.5
738	S556	4925	613.5	798	S496	3845	613.5	858	S436	2765	613.5	918	DUMMY	805	703.5
739	S555	4907	703.5	799	S495	3827	703.5	859	S435	2747	703.5	919	DUMMY	735	703.5
740	S554	4889	613.5	800	S494	3809	613.5	860	S434	2729	613.5	920	DUMMY	665	703.5
741	S553	4871	703.5	801	S493	3791	703.5	861	S433	2711	703.5	921	DUMMY	595	703.5
742	S552	4853	613.5	802	S492	3773	613.5	862	S432	2693	613.5	922	DUMMY	525	703.5
743	S551	4835	703.5	803	S491	3755	703.5	863	S431	2675	703.5	923	DUMMY	455	703.5
744	S550	4817	613.5	804	S490	3737	613.5	864	S430	2657	613.5	924	DUMMY	385	703.5
745	S549	4799	703.5	805	S489	3719	703.5	865	S429	2639	703.5	925	DUMMY	315	703.5
746	S548	4781	613.5	806	S488	3701	613.5	866	S428	2621	613.5	926	DUMMY	245	703.5
747	S547	4763	703.5	807	S487	3683	703.5	867	S427	2603	703.5	927	DUMMY	175	703.5
748	S546	4745	613.5	808	S486	3665	613.5	868	S426	2585	613.5	928	DUMMY	105	703.5
749	S545	4727	703.5	809	S485	3647	703.5	869	S425	2567	703.5	929	DUMMY	35	703.5
750	S544	4709	613.5	810	S484	3629	613.5	870	S424	2549	613.5	930	DUMMY	-35	703.5
751	S543	4691	703.5	811	S483	3611	703.5	871	S423	2531	703.5	931	DUMMY	-105	703.5
752	S542	4673	613.5	812	S482	3593	613.5	872	S422	2513	613.5	932	DUMMY	-175	703.5
753	S541	4655	703.5	813	S481	3575	703.5	873	S421	2495	703.5	933	DUMMY	-245	703.5
754	S540	4637	613.5	814	S480	3557	613.5	874	S420	2477	613.5	934	DUMMY	-315	703.5
755	S539	4619	703.5	815	S479	3539	703.5	875	S419	2459	703.5	935	DUMMY	-385	703.5
756	S538	4601	613.5	816	S478	3521	613.5	876	S418	2441	613.5	936	DUMMY	-455	703.5
757	S537	4583	703.5	817	S477	3503	703.5	877	S417	2423	703.5	937	DUMMY	-525	703.5
758	S536	4565	613.5	818	S476	3485	613.5	878	S416	2405	613.5	938	DUMMY	-595	703.5
759	S535	4547	703.5	819	S475	3467	703.5	879	S415	2387	703.5	939	DUMMY	-665	703.5
760	S534	4529	613.5	820	S474	3449	613.5	880	S414	2369	613.5	940	DUMMY	-735	703.5
761	S533	4511	703.5	821	S473	3431	703.5	881	S413	2351	703.5	941	DUMMY	-805	703.5
762	S532	4493	613.5	822	S472	3413	613.5	882	S412	2333	613.5	942	DUMMY	-875	703.5
763	S531	4475	703.5	823	S471	3395	703.5	883	S411	2315	703.5	943	DUMMY	-945	703.5
764	S530	4457	613.5	824	S470	3377	613.5	884	S410	2297	613.5	944	DUMMY	-1015	703.5
765	S529	4439	703.5	825	S469	3359	703.5	885	S409	2279	703.5	945	DUMMY	-1085	703.5
766	S528	4421	613.5	826	S468	3341	613.5	886	S408	2261	613.5	946	DUMMY	-1155	703.5
767	S527	4403	703.5	827	S467	3323	703.5	887	S407	2243	703.5	947	DUMMY	-1225	703.5
768	S526	4385	613.5	828	S466	3305	613.5	888	S406	2225	613.5	948	DUMMY	-1295	703.5
769	S525	4367	703.5	829	S465	3287	703.5	889	S405	2207	703.5	949	DUMMY	-1365	703.5
770	S524	4349	613.5	830	S464	3269	613.5	890	S404	2189	613.5	950	DUMMY	-1435	703.5
771	S523	4331	703.5	831	S463	3251	703.5	891	S403	2171	703.5	951	DUMMY	-1505	703.5
772	S522	4313	613.5	832	S462	3233	613.5	892	S402	2153	613.5	952	DUMMY	-1575	703.5
773	S521	4295	703.5	833	S461	3215	703.5	893	S401	2135	703.5	953	DUMMY	-1645	703.5
774	S520	4277	613.5	834	S460	3197	613.5	894	DUMMY	2117	613.5	954	DUMMY	-1715	703.5
775	S519	4259	703.5	835	S459	3179	703.5	895	DUMMY	2099	703.5	955	DUMMY	-1785	703.5
776	S518	4241	613.5	836	S458	3161	613.5	896	DUMMY	2081	613.5	956	DUMMY	-1855	703.5
777	S517	4223	703.5	837	S457	3143	703.5	897	DUMMY	2063	703.5	957	DUMMY	-1925	703.5
778	S516	4205	613.5	838	S456	3125	613.5	898	DUMMY	2045	613.5	958	DUMMY	-1991	613.5
779	S515	4187	703.5	839	S455	3107	703.5	899	DUMMY	2027	703.5	959	DUMMY	-2009	703.5
780	S514	4169	613.5	840	S454	3089	613.5	900	DUMMY	2009	613.5	960	DUMMY	-2027	613.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
961	DUMMY	-2045	703.5	1021	S345	-3125	703.5	1081	S285	-4205	703.5	1141	S225	-5285	703.5
962	DUMMY	-2063	613.5	1022	S344	-3143	613.5	1082	S284	-4223	613.5	1142	S224	-5303	613.5
963	DUMMY	-2081	703.5	1023	S343	-3161	703.5	1083	S283	-4241	703.5	1143	S223	-5321	703.5
964	DUMMY	-2099	613.5	1024	S342	-3179	613.5	1084	S282	-4259	613.5	1144	S222	-5339	613.5
965	DUMMY	-2117	703.5	1025	S341	-3197	703.5	1085	S281	-4277	703.5	1145	S221	-5357	703.5
966	S400	-2135	613.5	1026	S340	-3215	613.5	1086	S280	-4295	613.5	1146	S220	-5375	613.5
967	S399	-2153	703.5	1027	S339	-3233	703.5	1087	S279	-4313	703.5	1147	S219	-5393	703.5
968	S398	-2171	613.5	1028	S338	-3251	613.5	1088	S278	-4331	613.5	1148	S218	-5411	613.5
969	S397	-2189	703.5	1029	S337	-3269	703.5	1089	S277	-4349	703.5	1149	S217	-5429	703.5
970	S396	-2207	613.5	1030	S336	-3287	613.5	1090	S276	-4367	613.5	1150	S216	-5447	613.5
971	S395	-2225	703.5	1031	S335	-3305	703.5	1091	S275	-4385	703.5	1151	S215	-5465	703.5
972	S394	-2243	613.5	1032	S334	-3323	613.5	1092	S274	-4403	613.5	1152	S214	-5483	613.5
973	S393	-2261	703.5	1033	S333	-3341	703.5	1093	S273	-4421	703.5	1153	S213	-5501	703.5
974	S392	-2279	613.5	1034	S332	-3359	613.5	1094	S272	-4439	613.5	1154	S212	-5519	613.5
975	S391	-2297	703.5	1035	S331	-3377	703.5	1095	S271	-4457	703.5	1155	S211	-5537	703.5
976	S390	-2315	613.5	1036	S330	-3395	613.5	1096	S270	-4475	613.5	1156	S210	-5555	613.5
977	S389	-2333	703.5	1037	S329	-3413	703.5	1097	S269	-4493	703.5	1157	S209	-5573	703.5
978	S388	-2351	613.5	1038	S328	-3431	613.5	1098	S268	-4511	613.5	1158	S208	-5591	613.5
979	S387	-2369	703.5	1039	S327	-3449	703.5	1099	S267	-4529	703.5	1159	S207	-5609	703.5
980	S386	-2387	613.5	1040	S326	-3467	613.5	1100	S266	-4547	613.5	1160	S206	-5627	613.5
981	S385	-2405	703.5	1041	S325	-3485	703.5	1101	S265	-4565	703.5	1161	S205	-5645	703.5
982	S384	-2423	613.5	1042	S324	-3503	613.5	1102	S264	-4583	613.5	1162	S204	-5663	613.5
983	S383	-2441	703.5	1043	S323	-3521	703.5	1103	S263	-4601	703.5	1163	S203	-5681	703.5
984	S382	-2459	613.5	1044	S322	-3539	613.5	1104	S262	-4619	613.5	1164	S202	-5699	613.5
985	S381	-2477	703.5	1045	S321	-3557	703.5	1105	S261	-4637	703.5	1165	S201	-5717	703.5
986	S380	-2495	613.5	1046	S320	-3575	613.5	1106	S260	-4655	613.5	1166	DUMMY	-5735	613.5
987	S379	-2513	703.5	1047	S319	-3593	703.5	1107	S259	-4673	703.5	1167	DUMMY	-5753	703.5
988	S378	-2531	613.5	1048	S318	-3611	613.5	1108	S258	-4691	613.5	1168	DUMMY	-5771	613.5
989	S377	-2549	703.5	1049	S317	-3629	703.5	1109	S257	-4709	703.5	1169	DUMMY	-5789	703.5
990	S376	-2567	613.5	1050	S316	-3647	613.5	1110	S256	-4727	613.5	1170	DUMMY	-5807	613.5
991	S375	-2585	703.5	1051	S315	-3665	703.5	1111	S255	-4745	703.5	1171	DUMMY	-5825	703.5
992	S374	-2603	613.5	1052	S314	-3683	613.5	1112	S254	-4763	613.5	1172	DUMMY	-5843	613.5
993	S373	-2621	703.5	1053	S313	-3701	703.5	1113	S253	-4781	703.5	1173	DUMMY	-5861	703.5
994	S372	-2639	613.5	1054	S312	-3719	613.5	1114	S252	-4799	613.5	1174	DUMMY	-5879	613.5
995	S371	-2657	703.5	1055	S311	-3737	703.5	1115	S251	-4817	703.5	1175	DUMMY	-5897	703.5
996	S370	-2675	613.5	1056	S310	-3755	613.5	1116	S250	-4835	613.5	1176	DUMMY	-5915	613.5
997	S369	-2693	703.5	1057	S309	-3773	703.5	1117	S249	-4853	703.5	1177	DUMMY	-5933	703.5
998	S368	-2711	613.5	1058	S308	-3791	613.5	1118	S248	-4871	613.5	1178	DUMMY	-5951	613.5
999	S367	-2729	703.5	1059	S307	-3809	703.5	1119	S247	-4889	703.5	1179	DUMMY	-5969	703.5
1000	S366	-2747	613.5	1060	S306	-3827	613.5	1120	S246	-4907	613.5	1180	DUMMY	-5987	613.5
1001	S365	-2765	703.5	1061	S305	-3845	703.5	1121	S245	-4925	703.5	1181	DUMMY	-6005	703.5
1002	S364	-2783	613.5	1062	S304	-3863	613.5	1122	S244	-4943	613.5	1182	S200	-6023	613.5
1003	S363	-2801	703.5	1063	S303	-3881	703.5	1123	S243	-4961	703.5	1183	S199	-6041	703.5
1004	S362	-2819	613.5	1064	S302	-3899	613.5	1124	S242	-4979	613.5	1184	S198	-6059	613.5
1005	S361	-2837	703.5	1065	S301	-3917	703.5	1125	S241	-4997	703.5	1185	S197	-6077	703.5
1006	S360	-2855	613.5	1066	S300	-3935	613.5	1126	S240	-5015	613.5	1186	S196	-6095	613.5
1007	S359	-2873	703.5	1067	S299	-3953	703.5	1127	S239	-5033	703.5	1187	S195	-6113	703.5
1008	S358	-2891	613.5	1068	S298	-3971	613.5	1128	S238	-5051	613.5	1188	S194	-6131	613.5
1009	S357	-2909	703.5	1069	S297	-3989	703.5	1129	S237	-5069	703.5	1189	S193	-6149	703.5
1010	S356	-2927	613.5	1070	S296	-4007	613.5	1130	S236	-5087	613.5	1190	S192	-6167	613.5
1011	S355	-2945	703.5	1071	S295	-4025	703.5	1131	S235	-5105	703.5	1191	S191	-6185	703.5
1012	S354	-2963	613.5	1072	S294	-4043	613.5	1132	S234	-5123	613.5	1192	S190	-6203	613.5
1013	S353	-2981	703.5	1073	S293	-4061	703.5	1133	S233	-5141	703.5	1193	S189	-6221	703.5
1014	S352	-2999	613.5	1074	S292	-4079	613.5	1134	S232	-5159	613.5	1194	S188	-6239	613.5
1015	S351	-3017	703.5	1075	S291	-4097	703.5	1135	S231	-5177	703.5	1195	S187	-6257	703.5
1016	S350	-3035	613.5	1076	S290	-4115	613.5	1136	S230	-5195	613.5	1196	S186	-6275	613.5
1017	S349	-3053	703.5	1077	S289	-4133	703.5	1137	S229	-5213	703.5	1197	S185	-6293	703.5
1018	S348	-3071	613.5	1078	S288	-4151	613.5	1138	S228	-5231	613.5	1198	S184	-6311	613.5
1019	S347	-3089	703.5	1079	S287	-4169	703.5	1139	S227	-5249	703.5	1199	S183	-6329	703.5
1020	S346	-3107	613.5	1080	S286	-4187	613.5	1140	S226	-5267	613.5	1200	S182	-6347	613.5

No.	Name	X	Y
1201	S181	-6365	703.5
1202	S180	-6383	613.5
1203	S179	-6401	703.5
1204	S178	-6419	613.5
1205	S177	-6437	703.5
1206	S176	-6455	613.5
1207	S175	-6473	703.5
1208	S174	-6491	613.5
1209	S173	-6509	703.5
1210	S172	-6527	613.5
1211	S171	-6545	703.5
1212	S170	-6563	613.5
1213	S169	-6581	703.5
1214	S168	-6599	613.5
1215	S167	-6617	703.5
1216	S166	-6635	613.5
1217	S165	-6653	703.5
1218	S164	-6671	613.5
1219	S163	-6689	703.5
1220	S162	-6707	613.5
1221	S161	-6725	703.5
1222	S160	-6743	613.5
1223	S159	-6761	703.5
1224	S158	-6779	613.5
1225	S157	-6797	703.5
1226	S156	-6815	613.5
1227	S155	-6833	703.5
1228	S154	-6851	613.5
1229	S153	-6869	703.5
1230	S152	-6887	613.5
1231	S151	-6905	703.5
1232	S150	-6923	613.5
1233	S149	-6941	703.5
1234	S148	-6959	613.5
1235	S147	-6977	703.5
1236	S146	-6995	613.5
1237	S145	-7013	703.5
1238	S144	-7031	613.5
1239	S143	-7049	703.5
1240	S142	-7067	613.5
1241	S141	-7085	703.5
1242	S140	-7103	613.5
1243	S139	-7121	703.5
1244	S138	-7139	613.5
1245	S137	-7157	703.5
1246	S136	-7175	613.5
1247	S135	-7193	703.5
1248	S134	-7211	613.5
1249	S133	-7229	703.5
1250	S132	-7247	613.5
1251	S131	-7265	703.5
1252	S130	-7283	613.5
1253	S129	-7301	703.5
1254	S128	-7319	613.5
1255	S127	-7337	703.5
1256	S126	-7355	613.5
1257	S125	-7373	703.5
1258	S124	-7391	613.5
1259	S123	-7409	703.5
1260	S122	-7427	613.5

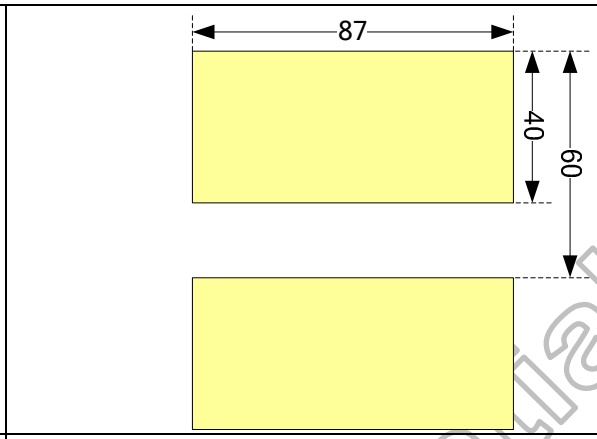
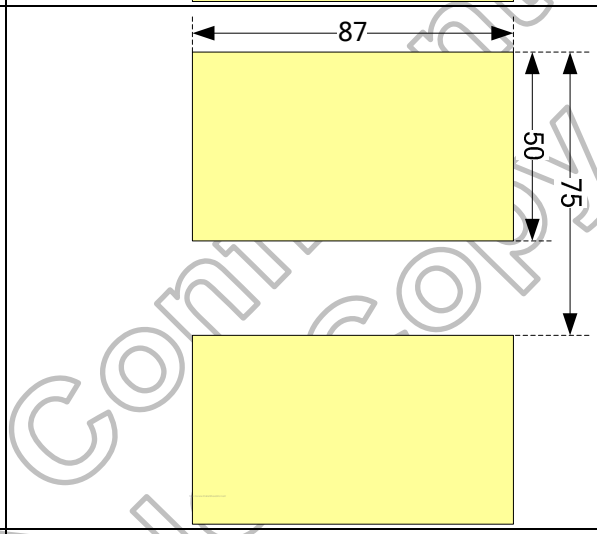
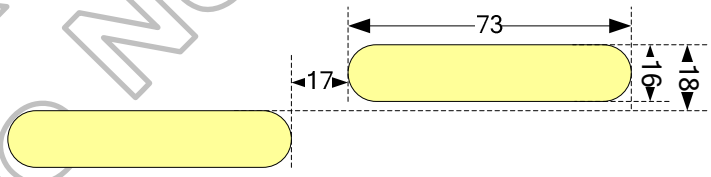
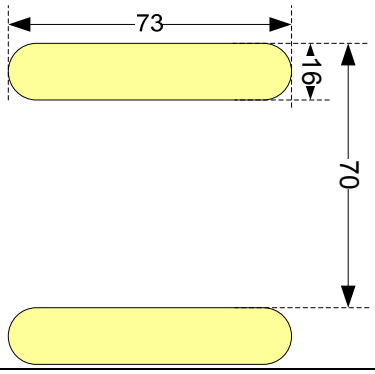
No.	Name	X	Y
1261	S121	-7445	703.5
1262	S120	-7463	613.5
1263	S119	-7481	703.5
1264	S118	-7499	613.5
1265	S117	-7517	703.5
1266	S116	-7535	613.5
1267	S115	-7553	703.5
1268	S114	-7571	613.5
1269	S113	-7589	703.5
1270	S112	-7607	613.5
1271	S111	-7625	703.5
1272	S110	-7643	613.5
1273	S109	-7661	703.5
1274	S108	-7679	613.5
1275	S107	-7697	703.5
1276	S106	-7715	613.5
1277	S105	-7733	703.5
1278	S104	-7751	613.5
1279	S103	-7769	703.5
1280	S102	-7787	613.5
1281	S101	-7805	703.5
1282	S100	-7823	613.5
1283	S99	-7841	703.5
1284	S98	-7859	613.5
1285	S97	-7877	703.5
1286	S96	-7895	613.5
1287	S95	-7913	703.5
1288	S94	-7931	613.5
1289	S93	-7949	703.5
1290	S92	-7967	613.5
1291	S91	-7985	703.5
1292	S90	-8003	613.5
1293	S89	-8021	703.5
1294	S88	-8039	613.5
1295	S87	-8057	703.5
1296	S86	-8075	613.5
1297	S85	-8093	703.5
1298	S84	-8111	613.5
1299	S83	-8129	703.5
1300	S82	-8147	613.5
1301	S81	-8165	703.5
1302	S80	-8183	613.5
1303	S79	-8201	703.5
1304	S78	-8219	613.5
1305	S77	-8237	703.5
1306	S76	-8255	613.5
1307	S75	-8273	703.5
1308	S74	-8291	613.5
1309	S73	-8309	703.5
1310	S72	-8327	613.5
1311	S71	-8345	703.5
1312	S70	-8363	613.5
1313	S69	-8381	703.5
1314	S68	-8399	613.5
1315	S67	-8417	703.5
1316	S66	-8435	613.5
1317	S65	-8453	703.5
1318	S64	-8471	613.5
1319	S63	-8489	703.5
1320	S62	-8507	613.5

No.	Name	X	Y
1321	S61	-8525	703.5
1322	S60	-8543	613.5
1323	S59	-8561	703.5
1324	S58	-8579	613.5
1325	S57	-8597	703.5
1326	S56	-8615	613.5
1327	S55	-8633	703.5
1328	S54	-8651	613.5
1329	S53	-8669	703.5
1330	S52	-8687	613.5
1331	S51	-8705	703.5
1332	S50	-8723	613.5
1333	S49	-8741	703.5
1334	S48	-8759	613.5
1335	S47	-8777	703.5
1336	S46	-8795	613.5
1337	S45	-8813	703.5
1338	S44	-8831	613.5
1339	S43	-8849	703.5
1340	S42	-8867	613.5
1341	S41	-8885	703.5
1342	S40	-8903	613.5
1343	S39	-8921	703.5
1344	S38	-8939	613.5
1345	S37	-8957	703.5
1346	S36	-8975	613.5
1347	S35	-8993	703.5
1348	S34	-9011	613.5
1349	S33	-9029	703.5
1350	S32	-9047	613.5
1351	S31	-9065	703.5
1352	S30	-9083	613.5
1353	S29	-9101	703.5
1354	S28	-9119	613.5
1355	S27	-9137	703.5
1356	S26	-9155	613.5
1357	S25	-9173	703.5
1358	S24	-9191	613.5
1359	S23	-9209	703.5
1360	S22	-9227	613.5
1361	S21	-9245	703.5
1362	S20	-9263	613.5
1363	S19	-9281	703.5
1364	S18	-9299	613.5
1365	S17	-9317	703.5
1366	S16	-9335	613.5
1367	S15	-9353	703.5
1368	S14	-9371	613.5
1369	S13	-9389	703.5
1370	S12	-9407	613.5
1371	S11	-9425	703.5
1372	S10	-9443	613.5
1373	S9	-9461	703.5
1374	S8	-9479	613.5
1375	S7	-9497	703.5
1376	S6	-9515	613.5
1377	S5	-9533	703.5
1378	S4	-9551	613.5
1379	S3	-9569	703.5
1380	S2	-9587	613.5

No.	Name	X	Y
1381	S1	-9605	703.5
1382	DUMMY	-9623	613.5
1383	DUMMY	-9641	703.5
1384	DUMMY	-9659	613.5
1385	DUMMY	-9677	703.5
1386	DUMMY	-9695	613.5
1387	DUMMY	-9713	703.5
1388	DUMMY	-9731	613.5
1389	DUMMY	-9749	703.5
1390	DUMMY	-9767	613.5
1391	DUMMY	-9785	703.5
1392	DUMMY	-9803	613.5
1393	DUMMY	-9821	703.5
1394	DUMMY	-9839	613.5
1395	DUMMY	-9857	703.5
1396	DUMMY	-9875	613.5
1397	DUMMY	-9893	703.5
1398	SW3B_R	-9963	703.5
1399	SW2B_R	-10033	703.5
1400	SW1B_R	-10103	703.5
1401	SW1_R	-10173	703.5
1402	SW2_R	-10243	703.5
1403	SW3_R	-10313	703.5
1404	INIT_R	-10383	703.5
1405	GSP_R	-10453	703.5
1406	UD_R	-10523	703.5
1407	DUMMY	-10593	703.5
1408	DUMMY	-10663	703.5
1409	DUMMY	-10733	703.5
1410	DUMMY	-10803	703.5
1411	DUMMY	-10873	703.5
1412	DUMMY	-10943	703.5
1413	DUMMY	-11013	703.5
1414	DUMMY	-11083	703.5
1415	DUMMY	-11153	703.5
1416	DUMMY	-11223	703.5
1417	GCK8_R	-11293	703.5
1418	GCK7_R	-11363	703.5
1419	GCK6_R	-11433	703.5
1420	GCK5_R	-11503	703.5
1421	GCK4_R	-11573	703.5
1422	GCK3_R	-11643	703.5
1423	GCK2_R	-11713	703.5
1424	GCK1_R	-11783	703.5
1425	VGH_R	-11853	703.5
1426	VGH_R	-11923	703.5
1427	VGH_R	-11993	703.5
1428	VGL	-12063	703.5
1429	VGL	-12133	703.5
1430	VGL	-12203	703.5
1431	VCOM	-12273	703.5
1432	VCOM	-12343	703.5
1433	VCOM	-12413	703.5
1434	VCOM	-12483	703.5
1435	VCOM	-12553	703.5
1436	VCOM	-12623	703.5
1437	DUMMY	-12693	703.5
1438	DUMMY	-12763	703.5

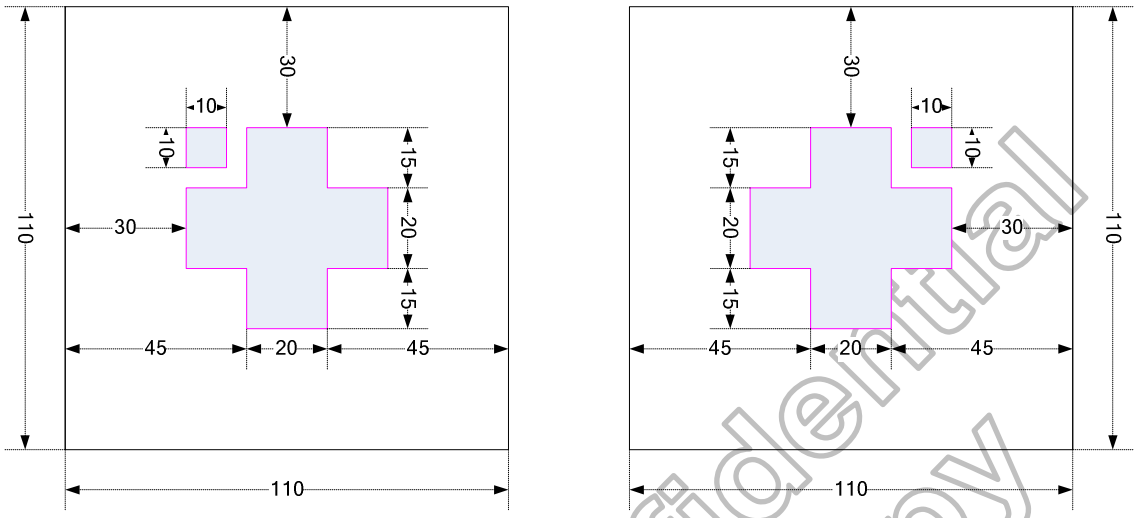
Alignment Mark	X	Y
A+	-12999	679
A-	12999	679

3.4.1 Bump arrangement

Input PAD (No.1 ~ 106, No.162 ~419)	
Input PAD (No.107 ~161)	
Output PAD (No.462 ~ 901, No.958 ~ 1397)	
Output PAD (No.420 ~461, No.902 ~957, No.1398 ~ 1438)	

Unit: um

3.4.2 Alignment Mark



4. Interface

4.1 Interface select

The HX8392-A supports DSI (Display Serial Interface).

The interface mode can be selected by BS3-0 pins setting as show in Table 4.1.

BS3	BS2	BS1	BS0	Interface	Display data	Display mode
0	1	1	0	DSI I/F	DSI I/F / GRAM	Type 1/3
0	1	1	1			
Other setting				Not open, only for internal test	-	-

Table 4.1: Interface selection

Interface	RDX	WRX_SCL	DCX	D23–D0 or other input pin
DSI (Display Serial Interface)	Unused	Unused	Unused	HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, DS_D1N, HS_D2P, DS_D2N, HS_D3P, DS_D3N

Table 4.2: Pin connection based on different interface

4.2 DSI system interface

The selection of interface is by BS(3-0) =”0110 “ or “0111”, the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.1 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

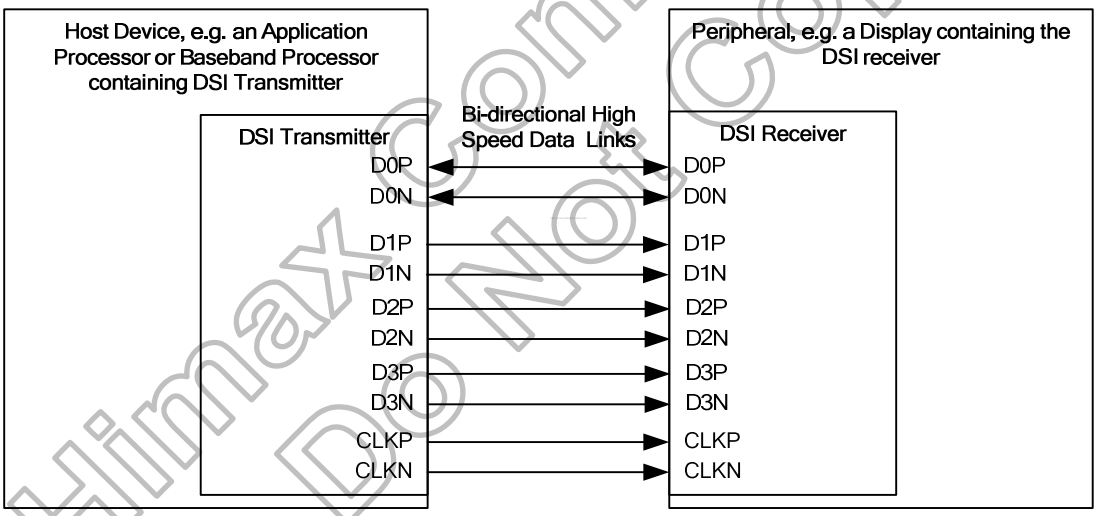


Figure 4.1: DSI transmitter and receiver interface

Please refer to “**DRAFT MIPI Alliance Standard for DSI**” for DSI detailed specifications. The data lane number select by internal register(RBAh).

4.2.1 DSI layer definitions

According Figure 4.2 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four layers, PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

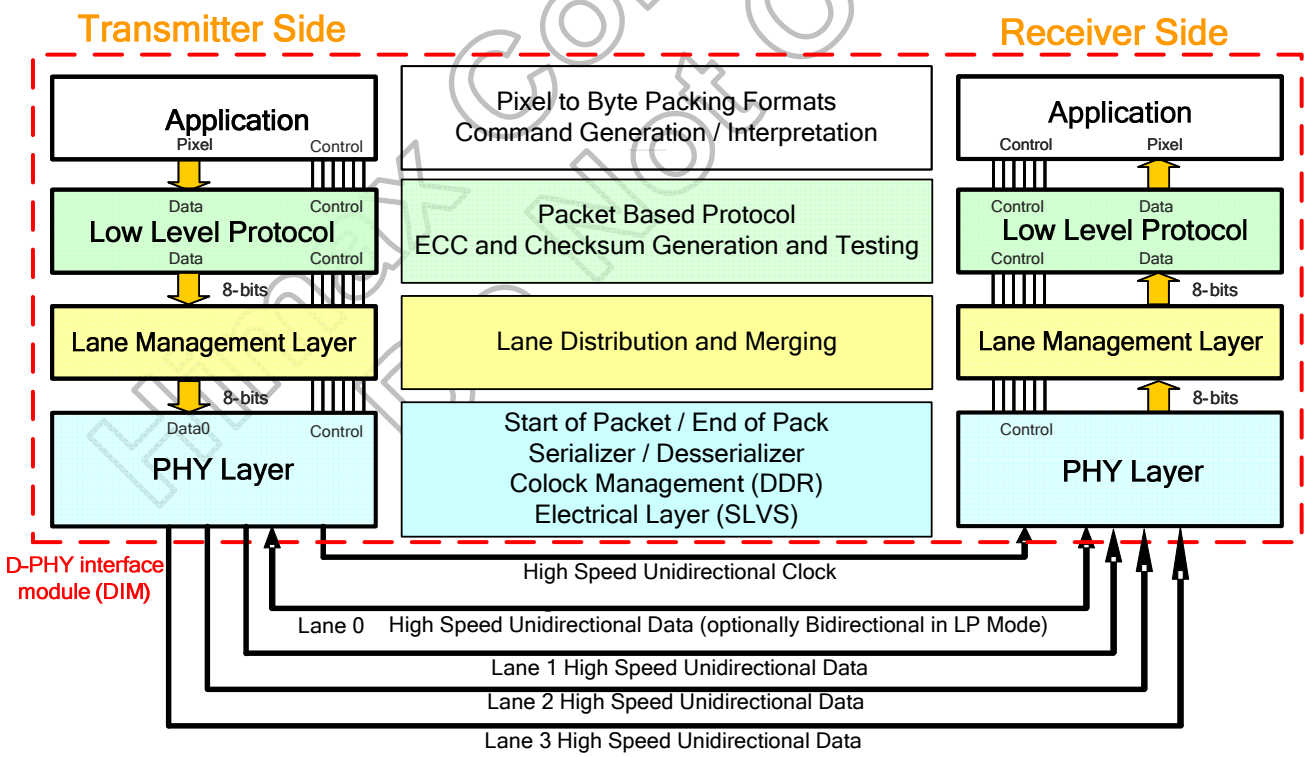
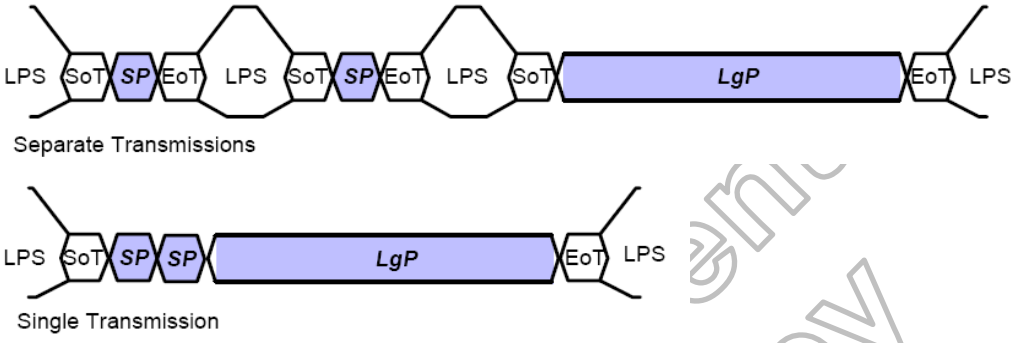


Figure 4.2: DSI transmitter and receiver interface

4.2.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.3 illustrates multiple HS Transmission packets.

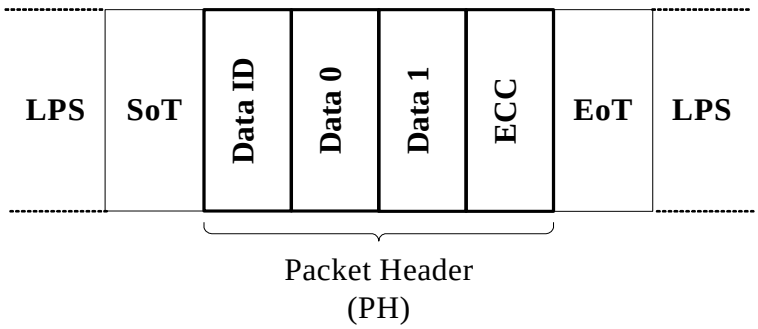


LPS：Low power state
SoT：Start of Transmission
SP：Short Packet
LgP：Long Packet
EoT：End of Transmission

Figure 4.3: Multiple Packets Transmission

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data and an 8-bit ECC. Figure 4.4 shows the structure of the Short packet.

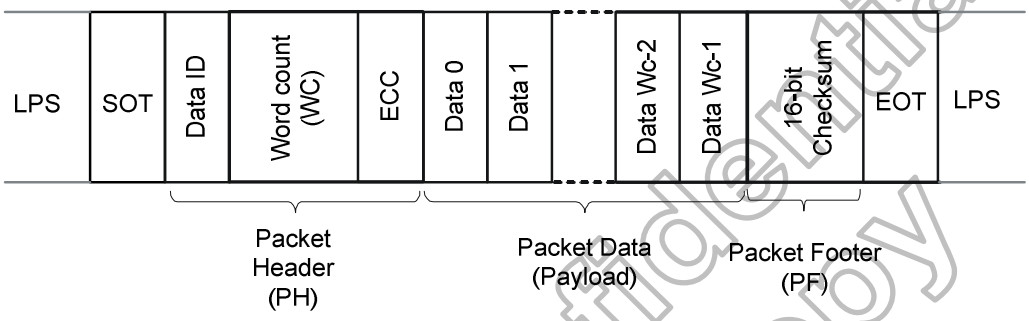


DI(Data ID)：Contain Virtual Channel Identifier and Data Type.
ECC(Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

Figure 4.4: Structure of the Short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,5**35** bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.5 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = 4 bytes PH + (2^{16}-1)bytes Payload + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：The receiver use WC to determine the packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：Mean 16-bit Checksum.

Figure 4.5: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.6 the shows format of Data ID.

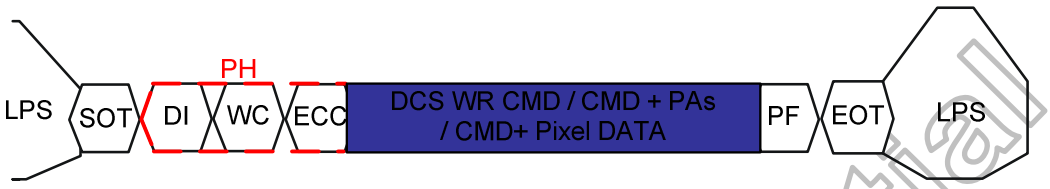
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type.

Figure 4.6: The format of data ID.

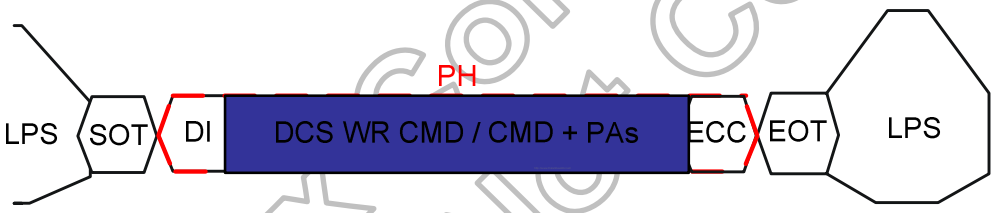
Due to Data Type (DT) mean format of transmission type, Figure 4.7 show Short- / Long-packet transmission command sequence.

Long packet write Command / Parameters / Pixel Datas



DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet write Command / Parameters



DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.7: show Short- / Long-packet transmission command sequence

4.2.3 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.3 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet(EoTp)	Short
05h	000101	DCS WRITE, no parameter	Short
15h	010101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.3: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	V Sync start, Start of VSA pulse.	4 bytes (DI+00h+00h+ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	
Note: V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.		

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes (DI+00h+00h +ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
06h	DCS Read command, the returned data shall be Long packet format.	4 bytes (DI+Data0+Data1+ECC)
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types = 00 0101(05h), 01 0101 (15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

NOTE: (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC

Ex. 05h, 29h, 00, 1Ch — Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC

Ex. 15h, 36h, 08h, 11h — MADCTL(36h)-BGR bit=1

(2) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

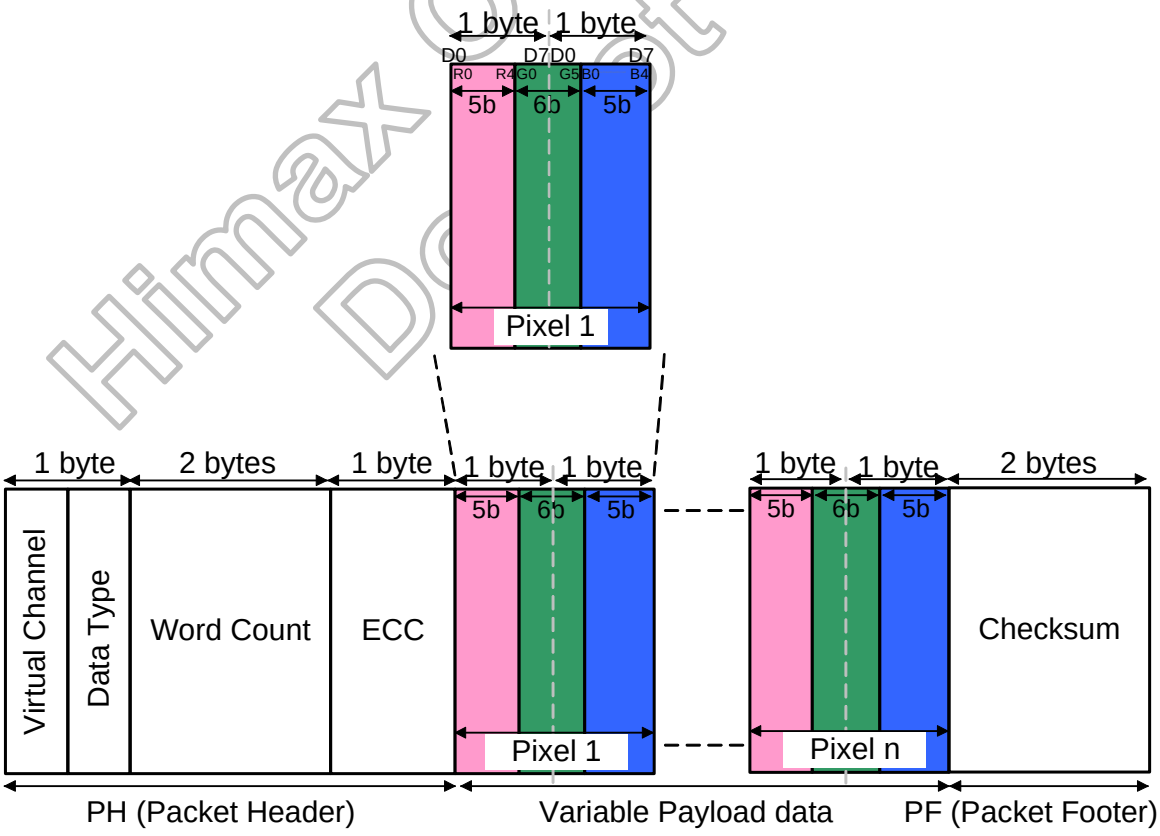
- ◆ If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(4) **One byte <= Length of payload DATA <= 2^{16}-1**

Maximum Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + Maximum Return Packet Size + ECC)
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

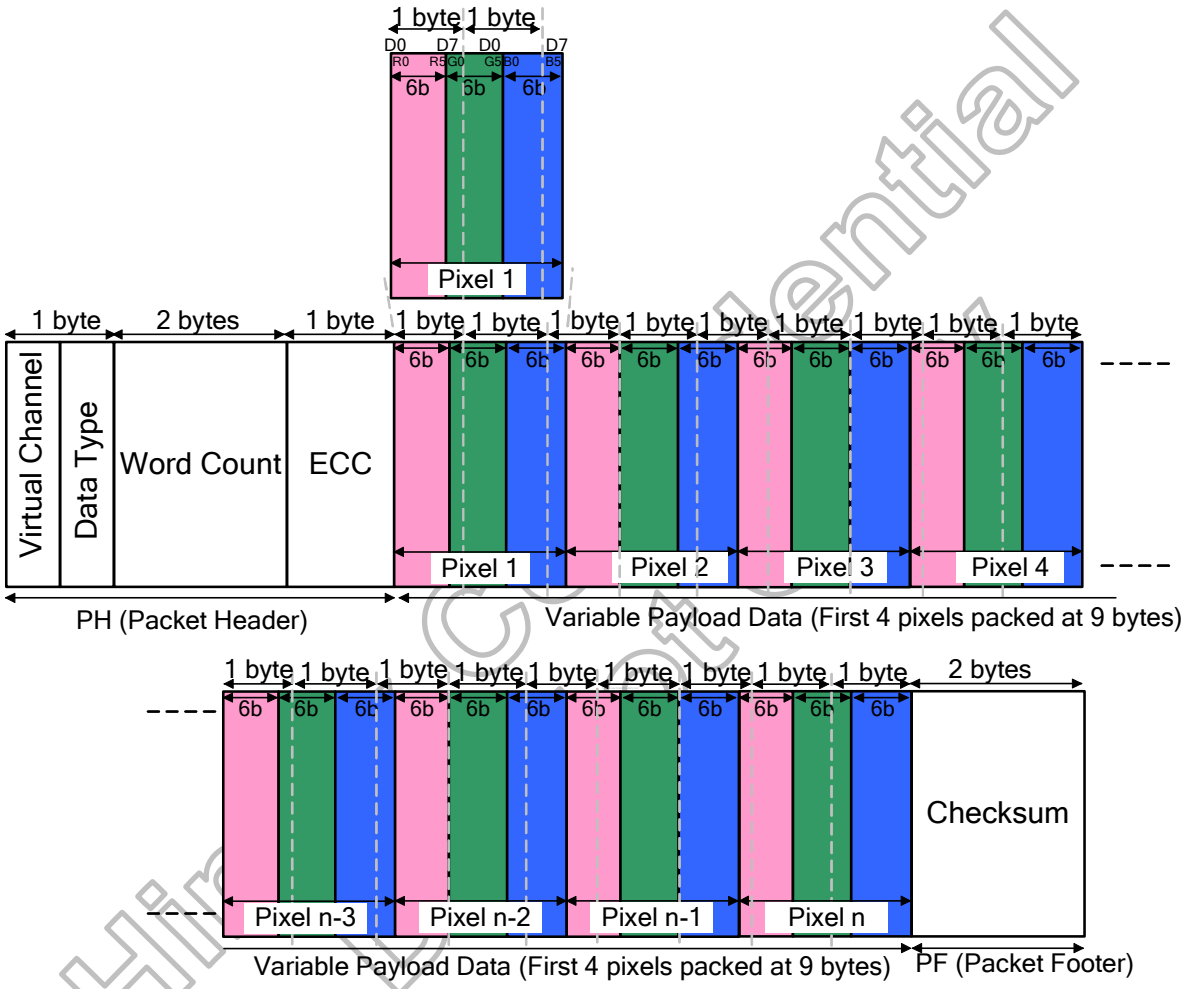
Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	
Note: (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



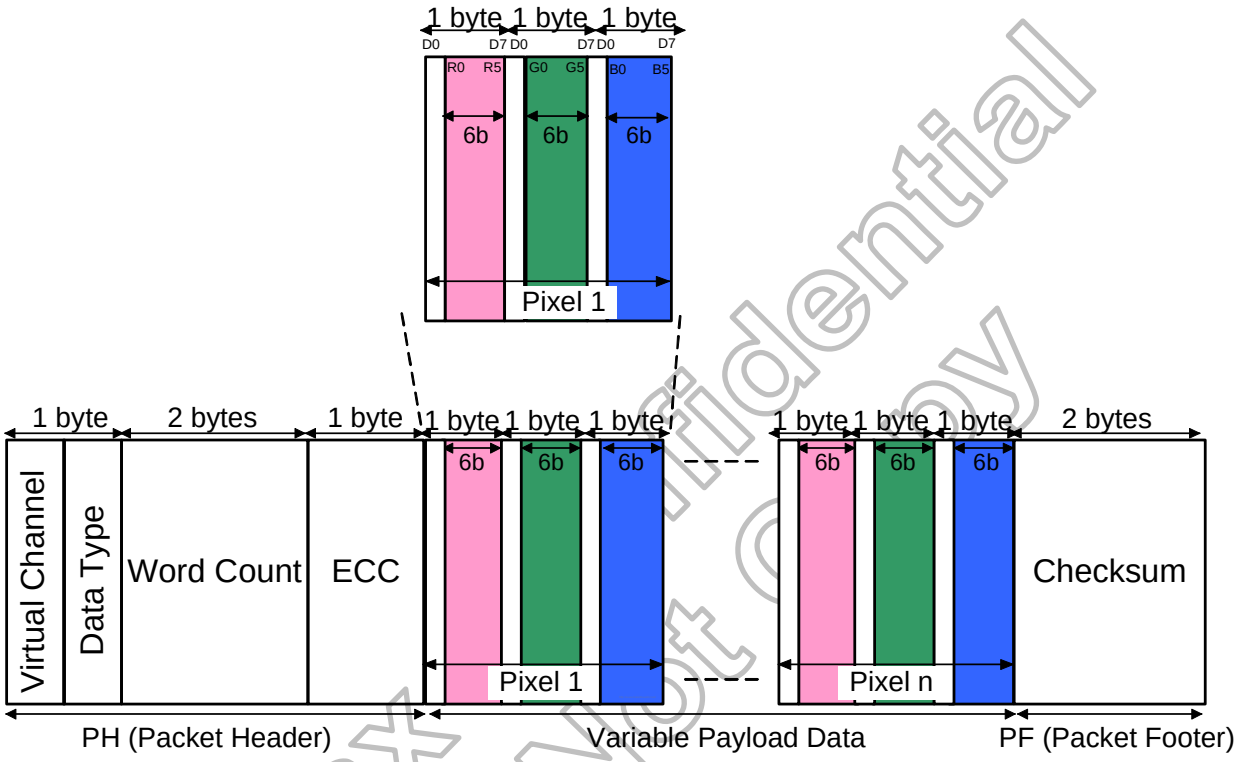
Note: Within a color component, the "LSB is sent first, the MSB last ".

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



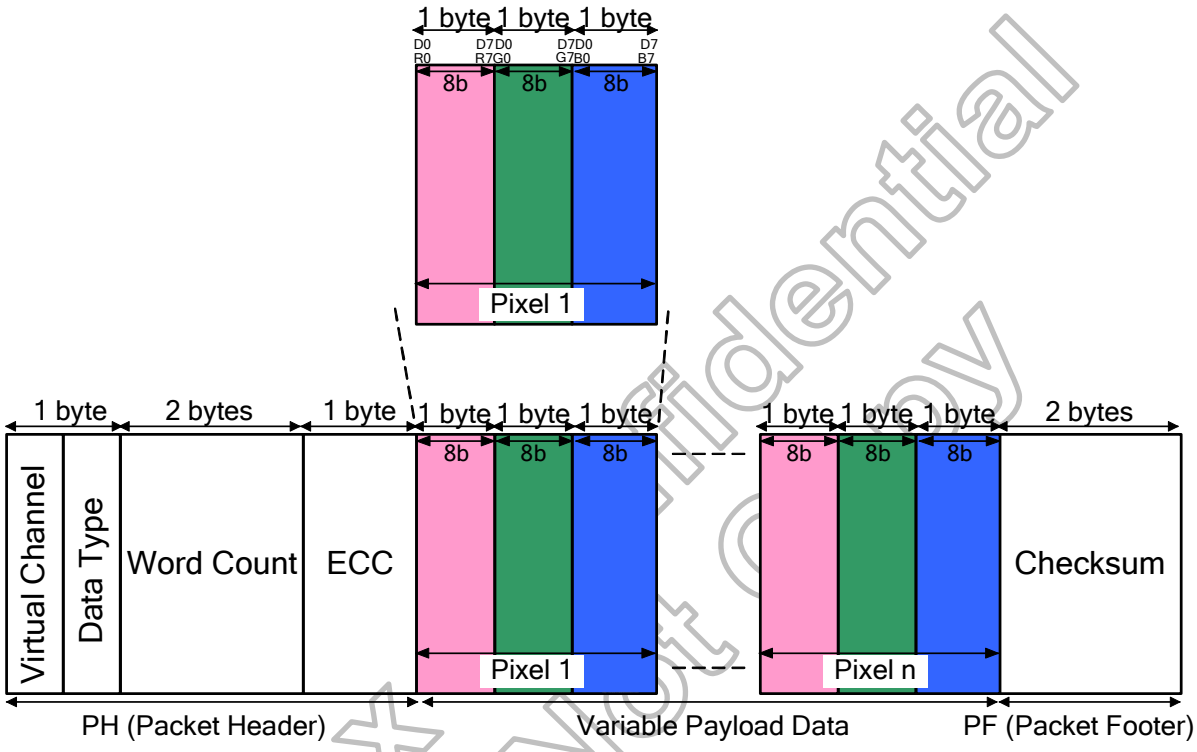
Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Packed pixel stream, 24-bit format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

4.2.4 Peripheral to processor (reverse direction) packet data type

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets shall use ECC and may use Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

A. Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
B. Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication is received by the peripheral with no errors.
C. Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
D. Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

A. “Acknowledge” is sent using a Trigger message which is one byte: 00100001
B. “Acknowledge with Error Report” include 4 bytes which are DI, 2 bytes Error report and ECC.
C. “Response to Read Request” are Long packet format.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.4 shows the Error Report Bit Definitions. And Table 4.5 list complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Table 4.4: Shows the error report bit definitions.

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)		Reserved	-

Table 4.5: The complete set of peripheral-to-processor data types.

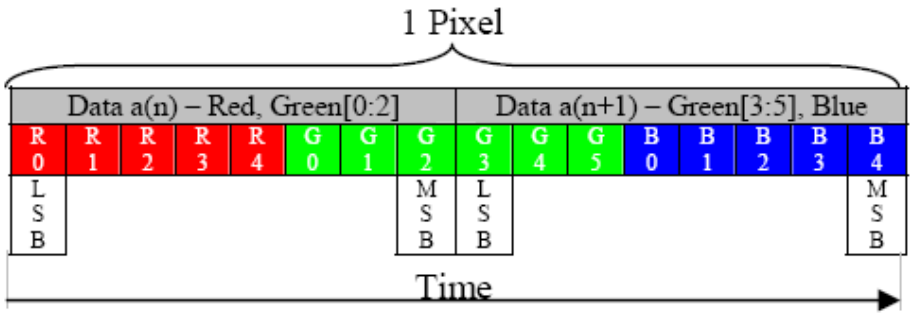
Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error→Acknowledge with error report(Short packet), Without error→ request READ data or Acknowledge(trigger message).		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
1Ch	This is the Long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
Note: (1)If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent. (2)There is no dummy read byte in the read response packet.		

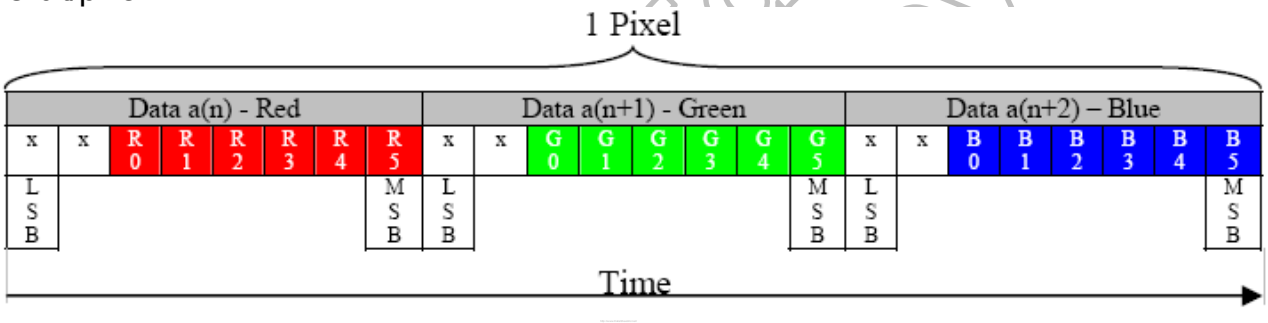
4.2.5 Data format for Command mode

HX8392-A also support display data write into GRAM by DSI Command mode. The Figure 4.8 is show of display data format.

16-bit/pixel



18-bit/pixel



x = Don't Care

24-bit/pixel

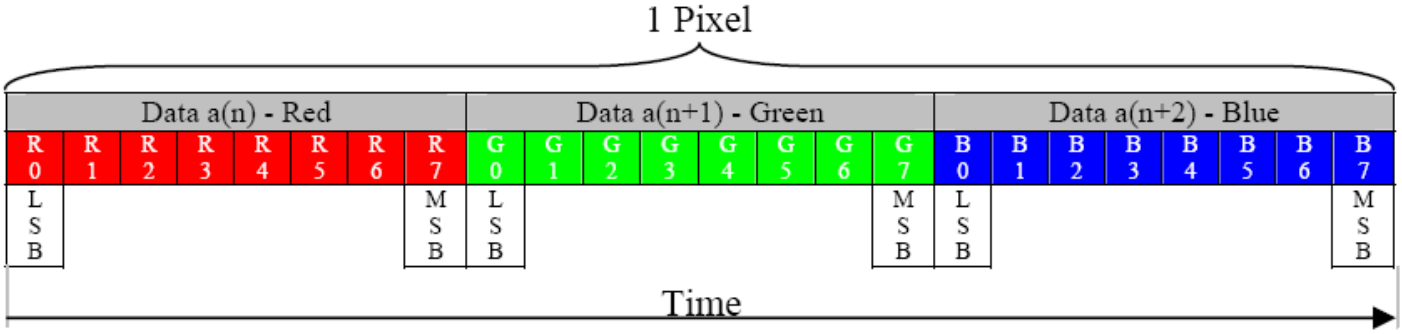


Figure 4.8: Data format of DSI command mode

5. Function Description

5.1 Display data GRAM

HX8392-A support the display data RAM that stores display dots. There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

5.2 Address counter (AC)

The HX8392-A contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

RES_SEL2	RES_SEL 1	RES_SEL 0	MV	X range	Y range	Panel resolution
0	0	0	0	0~799d.	0~1279d.	800RGBX1280 dot
			1	0~1279d.	0~799d.	
0	0	1	0	0~767d..	0~1279d.	768RGBX1280 dot
			1	0~1279d.	0~767d.	
0	1	0	0	0~719d.	0~1279d.	720RGBX1280 dot
			1	0~1279d.	0~719d.	
0	1	1	0	0~599d.	0~1023d.	600RGBX024 dot
			1	0~1023d.	0~599d.	

Table 5.1: Addresses counter range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.3 Source, gate and memory map

5.3.1 800RGB x 1280 resolution

R36h: B5=0

Source Out		S1			---	S400			S401			---	S800			SA	
RA		RGB=0 / RGB=1				RGB=0 / RGB=1			RGB=0 / RGB=1				RGB=0 / RGB=1				
MY=0	MY=1															ML=0	ML=1
0	1279	R0 7-0	G0 7-0	B0 7-0	---	R399 7-0	G399 7-0	B399 7-0	R400 7-0	G400 7-0	B400 7-0	---	R799 7-0	G799 7-0	B799 7-0	0	1279
1	1278				---							---				1	1278
2	1277				---							---				2	1277
3	1276				---							---				3	1276
4	1275				---							---				4	1275
5	1274				---							---				5	1274
6	1273				---							---				6	1273
7	1272				---							---				7	1272
8	1271				---							---				8	1271
9	1270				---							---				9	1270
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
1272	7				---							---				1272	7
1273	6				---							---				1273	6
1274	5				---							---				1274	5
1275	4				---							---				1275	4
1276	3				---							---				1276	3
1277	2				---							---				1277	2
1278	1				---							---				1278	1
1279	0				---							---				1279	0
CA	MX=0	0			---	399			400			---	799				
	MX=1	799			---	400			399			---	0				

Note: RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB= Red, Green and Blue pixel position change

Table 5.2: Memory map of 800RGB x 1280 resolution

5.3.2 768RGB x 1280 resolution

R36h: B5=0

Source Out		S1			---	S384			S417			---	S800			SA	
RA		RGB=0 / RGB=1				RGB=0 / RGB=1			RGB=0 / RGB=1				RGB=0 / RGB=1				
MY=0	MY=1															ML=0	ML=1
0	1279	R0 7-0	G0 7-0	B0 7-0	---	R383 7-0	G383 7-0	B383 7-0	R384 7-0	G384 7-0	B384 7-0	---	R767 7-0	G767 7-0	B767 7-0	0	1279
1	1278				---							---				1	1278
2	1277				---							---				2	1277
3	1276				---							---				3	1276
4	1275				---							---				4	1275
5	1274				---							---				5	1274
6	1273				---							---				6	1273
7	1272				---							---				7	1272
8	1271				---							---				8	1271
9	1270				---							---				9	1270
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1272	7				---							---				1272	7
1273	6				---							---				1273	6
1274	5				---							---				1274	5
1275	4				---							---				1275	4
1276	3				---							---				1276	3
1277	2				---							---				1277	2
1278	1				---							---				1278	1
1279	0				---							---				1279	0
CA	MX=0	0			---	383			384			---	767				
	MX=1	767			---	384			383			---	0				

Note: RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB= Red, Green and Blue pixel position change

Table 5.3: Memory map of 768RGB x 1280 resolution

5.3.3 720RGB x 1280 resolution

R36h: B5=0

Source Out		S1			---	S360			S441			---	S800			SA	
		RGB=0		RGB=1		RGB=0		RGB=1	RGB=0		RGB=1		RGB=0		RGB=1		
RA																	
MY=0	MY=1															ML=0	ML=1
0	1279	R0 7-0	G0 7-0	B0 7-0	---	R359 7-0	G359 7-0	B359 7-0	R360 7-0	G360 7-0	B360 7-0	---	R719 7-0	G719 7-0	B719 7-0	0	1279
1	1278				---							---				1	1278
2	1277				---							---				2	1277
3	1276				---							---				3	1276
4	1275				---							---				4	1275
5	1274				---							---				5	1274
6	1273				---							---				6	1273
7	1272				---							---				7	1272
8	1271				---							---				8	1271
9	1270				---							---				9	1270
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1272	7				---							---				1272	7
1273	6				---							---				1273	6
1274	5				---							---				1274	5
1275	4				---							---				1275	4
1276	3				---							---				1276	3
1277	2				---							---				1277	2
1278	1				---							---				1278	1
1279	0				---							---				1279	0
CA	MX=0	0			---	359			360			---	719				
	MX=1	719			---	360			359			---	0				

Note: RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB= Red, Green and Blue pixel position change

Table 5.4: Memory map of 720RGB x 1280 resolution

5.3.4 600RGB x 1024 resolution

R36h: B5=0

Source Out		S1			---	S300			S501			---	S800			SA	
RA		RGB=0 / RGB=1				RGB=0 / RGB=1			RGB=0 / RGB=1				RGB=0 / RGB=1				
MY=0	MY=1															ML=0	ML=1
0	1023	R0 7-0	G0 7-0	B0 7-0	---	R299 7-0	G299 7-0	B299 7-0	R300 7-0	G300 7-0	B300 7-0	---	R599 7-0	G599 7-0	B599 7-0	0	1023
1	1022				---							---				1	1022
2	1021				---							---				2	1021
3	1020				---							---				3	1020
4	1019				---							---				4	1019
5	1018				---							---				5	1018
6	1017				---							---				6	1017
7	1016				---							---				7	1016
8	1015				---							---				8	1015
9	1014				---							---				9	1014
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1016	7				---							---				1016	7
1017	6				---							---				1017	6
1018	5				---							---				1018	5
1019	4				---							---				1019	4
1020	3				---							---				1020	3
1021	2				---							---				1021	2
1022	1				---							---				1022	1
1023	0				---							---				1023	0
CA	MX=0	0			---	299			300			---	599				
	MX=1	599			---	300			299			---	0				

Note: RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB= Red, Green and Blue pixel position change

Table 5.5: Memory map of 600RGB x 1024 resolution

5.4 MCU to memory write / read direction

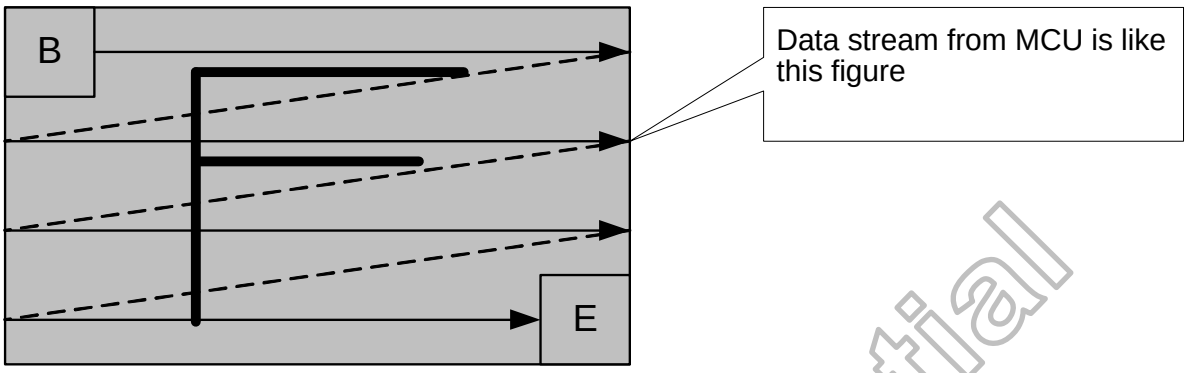


Figure 5.1: MCU to Memory write / read direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by "Memory Access Control" Command, Bits MY, MX, MV as described below.

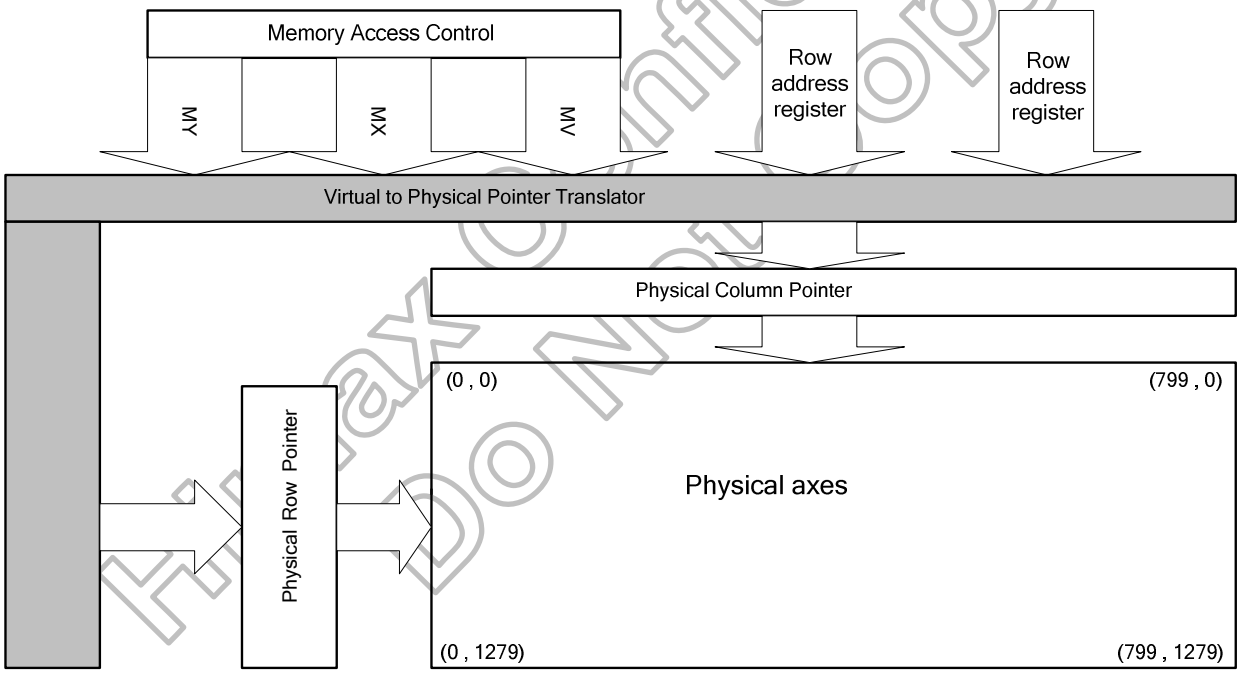


Figure 5.2: MY, MX, MV setting of 800RGB x 1280 dot

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (1279-Physical Row Pointer) with SC
0	1	0	Direct to (799-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (799-Physical Column Pointer)	Direct to (1279Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (1279-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (799-Physical Column Pointer)
1	1	1	Direct to (1279-Physical Row Pointer)	Direct to (799-Physical Column Pointer)

Figure 5.3: MY, MX, MV setting of 800RGB x 1280 dot

The following figure depicts the update method set by MV, MX and MY bit.

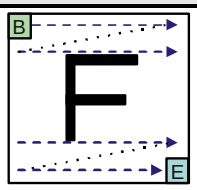
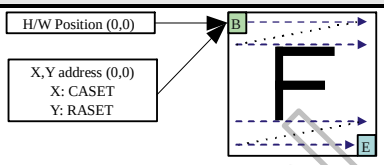
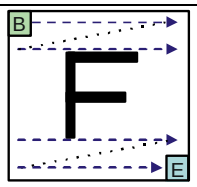
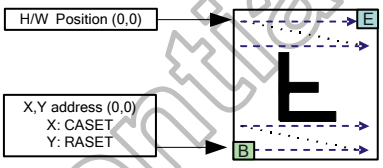
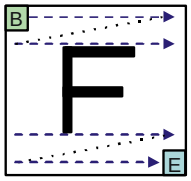
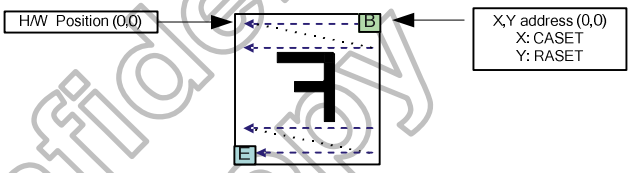
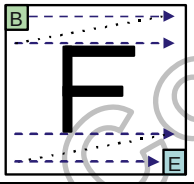
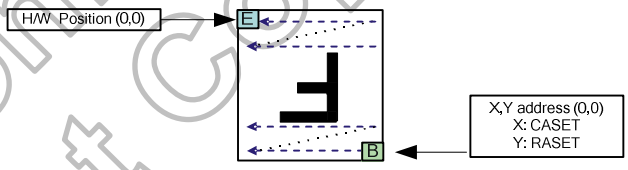
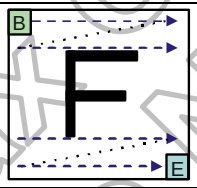
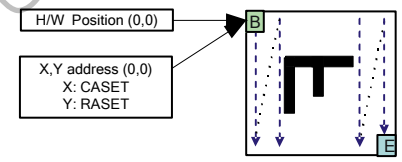
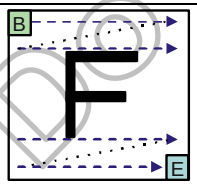
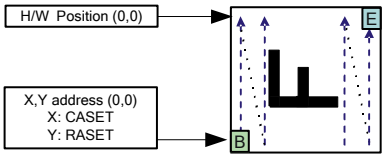
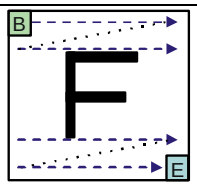
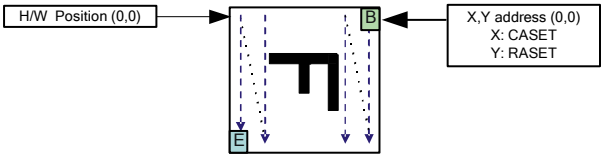
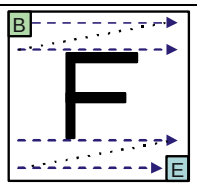
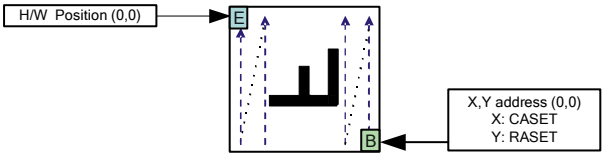
Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5.4: Address direction settings

5.5 Fully display, partial display, vertical scrolling display

5.5.1 Fully display

Example: (1) 800RGBx1280 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x31Fh (R2Ah) and SP=0x000h, EP=0x4FFh (R2Bh), ML=0.

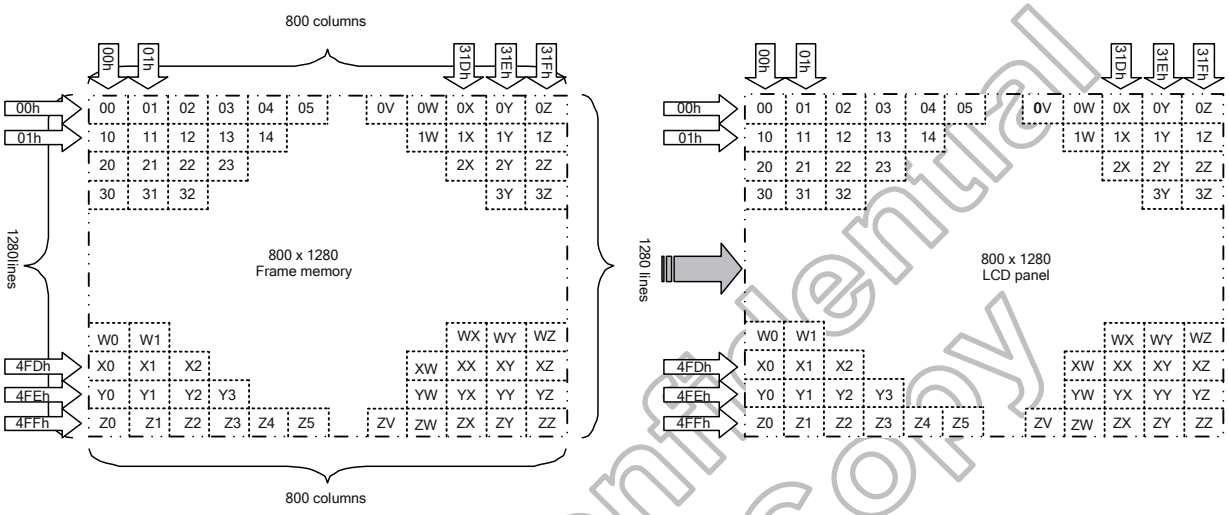


Figure 5.5: 800RGB x 1280 resolution

Example: (1) 768RGBx1280 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x2FFh (R2Ah) and SP=0x000h, EP=0x4FFh (R2Bh), ML=0.

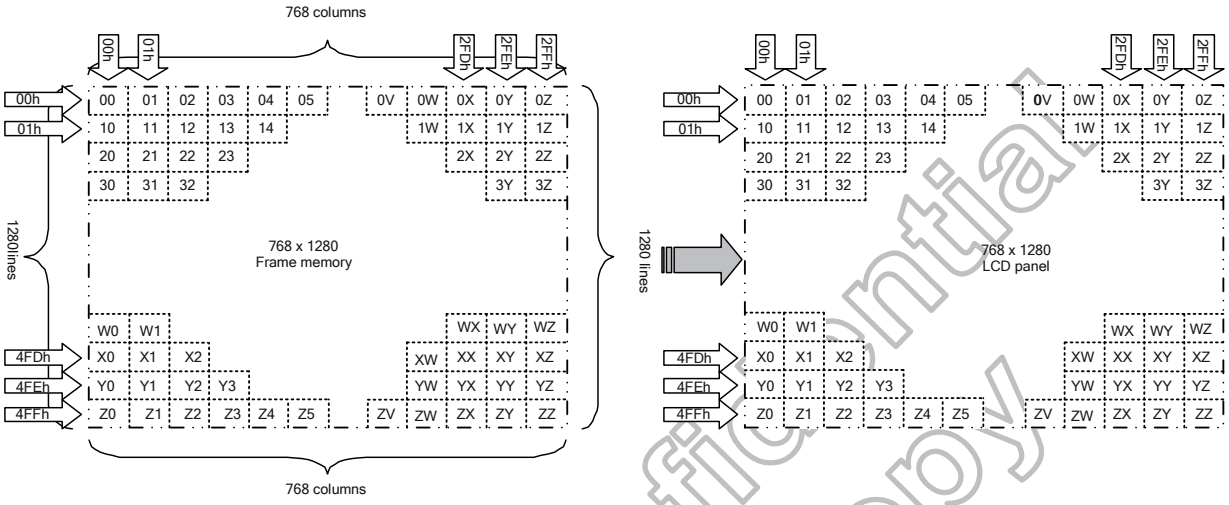


Figure 5.6: 768RGB x 1280 resolution

Example: (1) 72RGBx1280 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x2CFh (R2Ah) and SP=0x000h, EP=0x4FFh (R2Bh), ML=0.

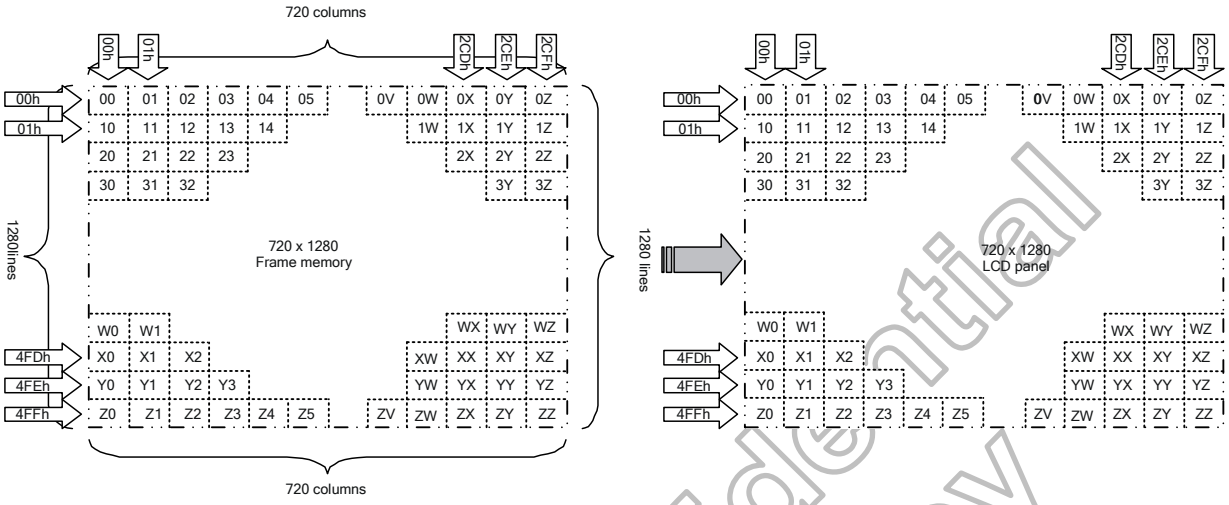


Figure 5.7: 720RGB x 1280 resolution

Example: (1) 600RGBx1024 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x257h (R2Ah) and SP=0x000h, EP=0x3FFh (R2Bh), ML=0.

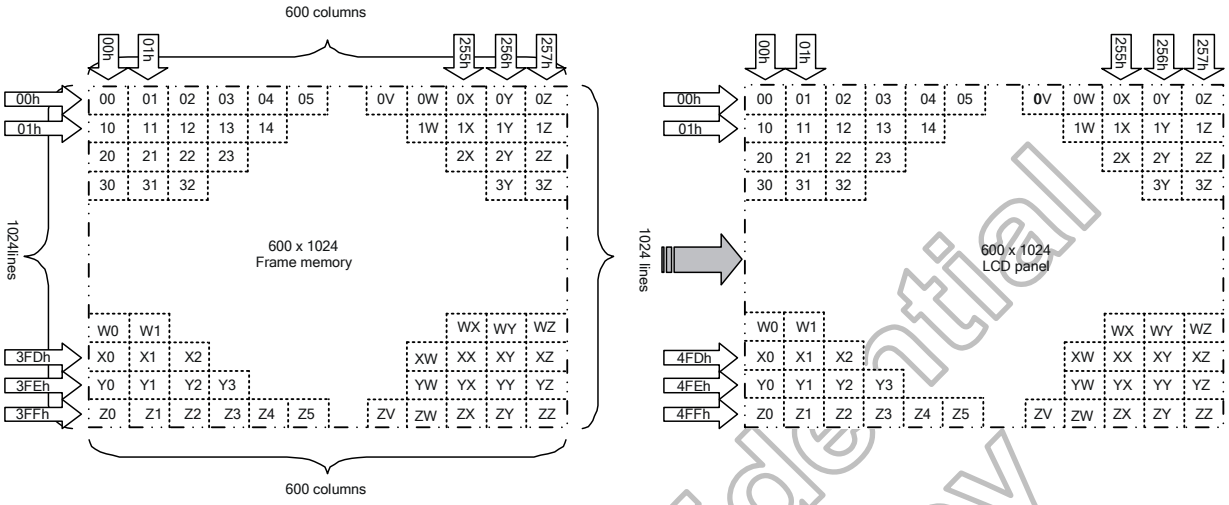


Figure 5.8: 600RGB x 1024 resolution

5.5.2 Vertical scrolling display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

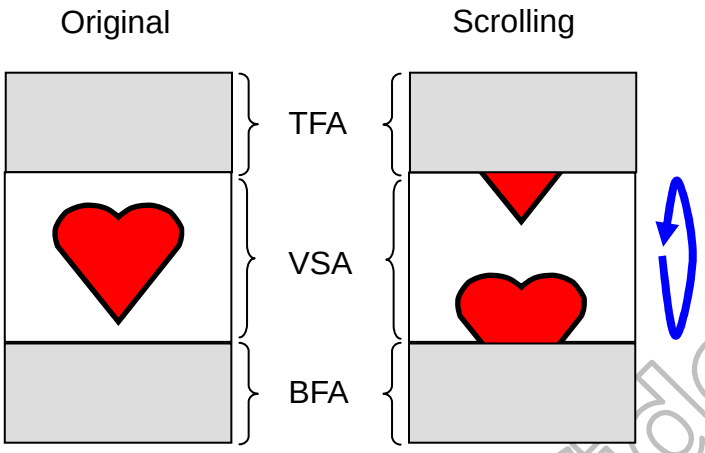


Figure 5.9: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

5.5.2.1 Example: 800RGB X 1280

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=1280. In this case, scrolling is applied as shown below.

Example (1) TFA=2, VSA=1278, BFA=0 when MADCTL B4=0

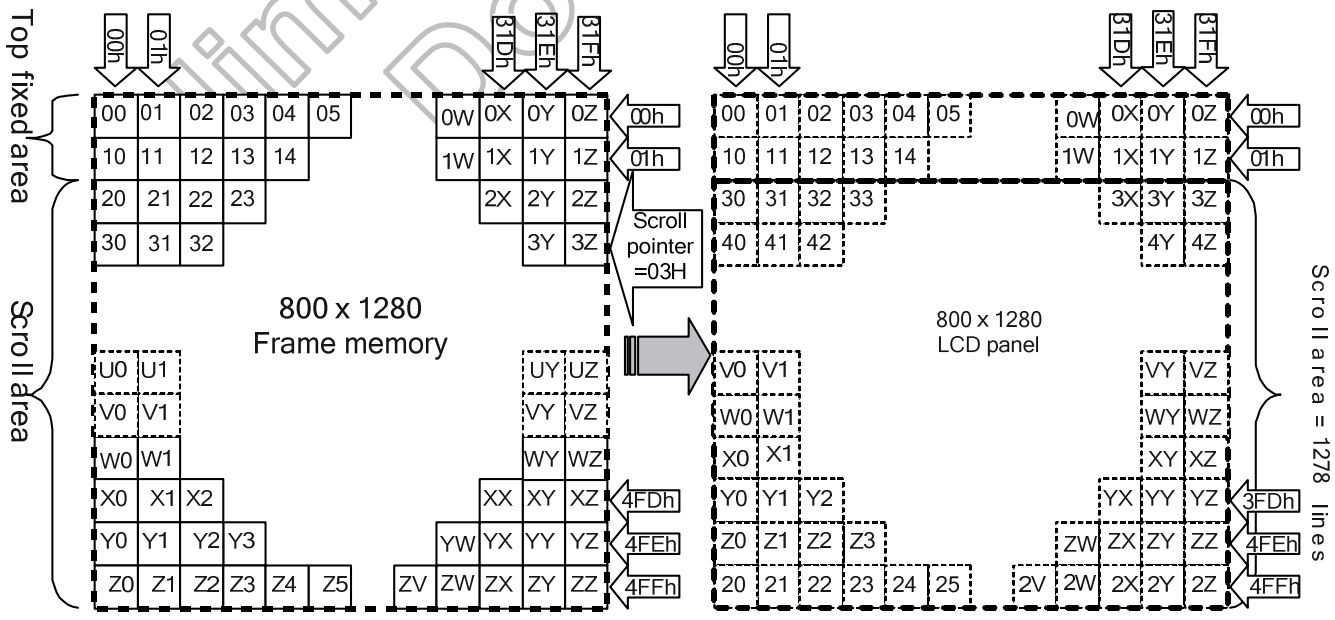


Figure 5.10: Memory map of vertical scrolling 1 for 800RGB x 1280 resolution

Example (2) TFA=2, VSA=1276, BFA=2 when MADCTL B4=0

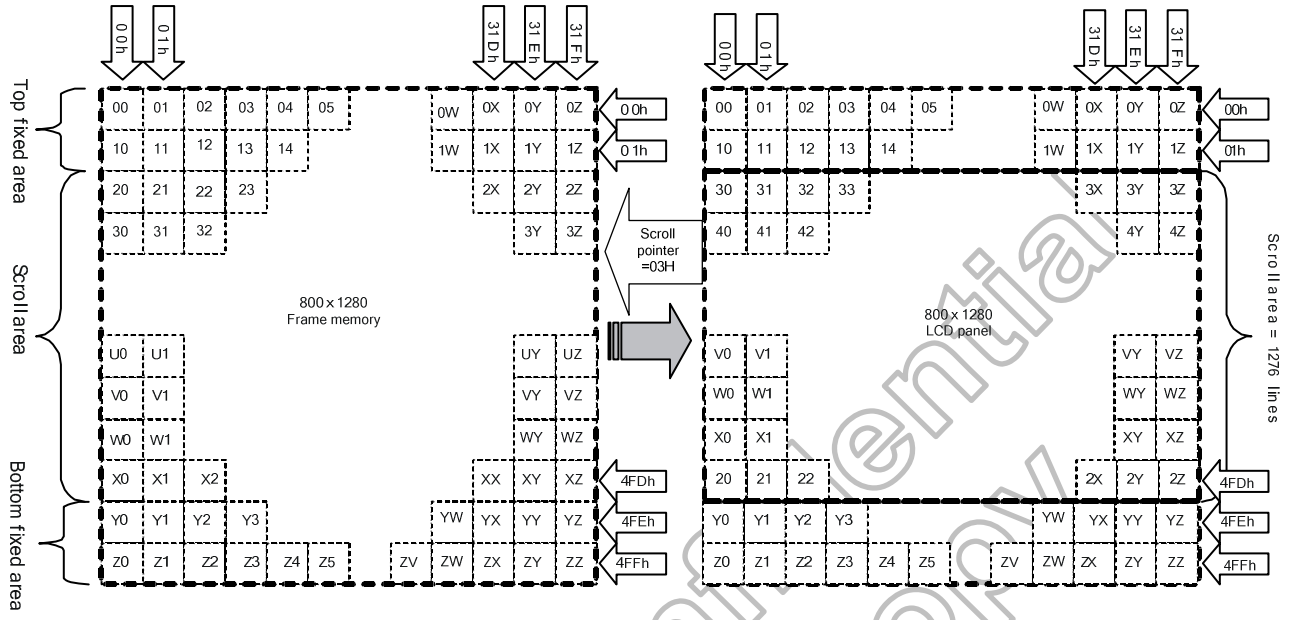


Figure 5.11: Memory map of vertical scrolling 2 for 800RGB x 1280 resolution

5.5.2.2 Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA≠1280
Do not set TFA + VSA + BFA≠1280. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=1280 (Scrolling)
Example (1) When TFA=0, VSA=1280, BFA=0 and VSCRSADD=40.MADCTL parameter B4="0"

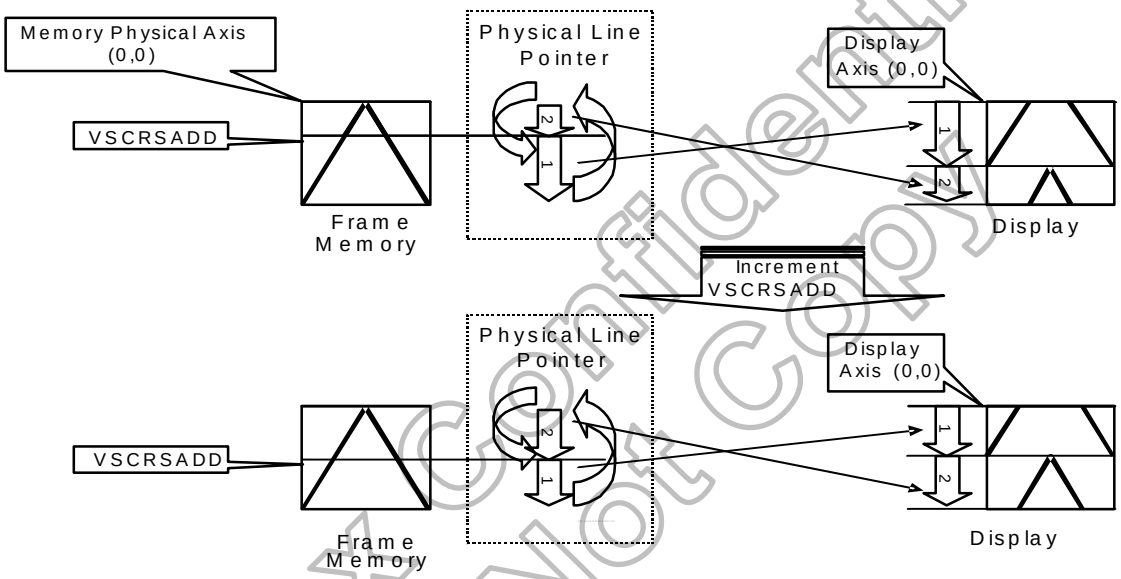


Figure 5.12: Vertical scroll example 1

Example (2) TFA=30, VSA=1250, BFA=0 and VSCRSADD =80. MADCTRL parameter B4="1"

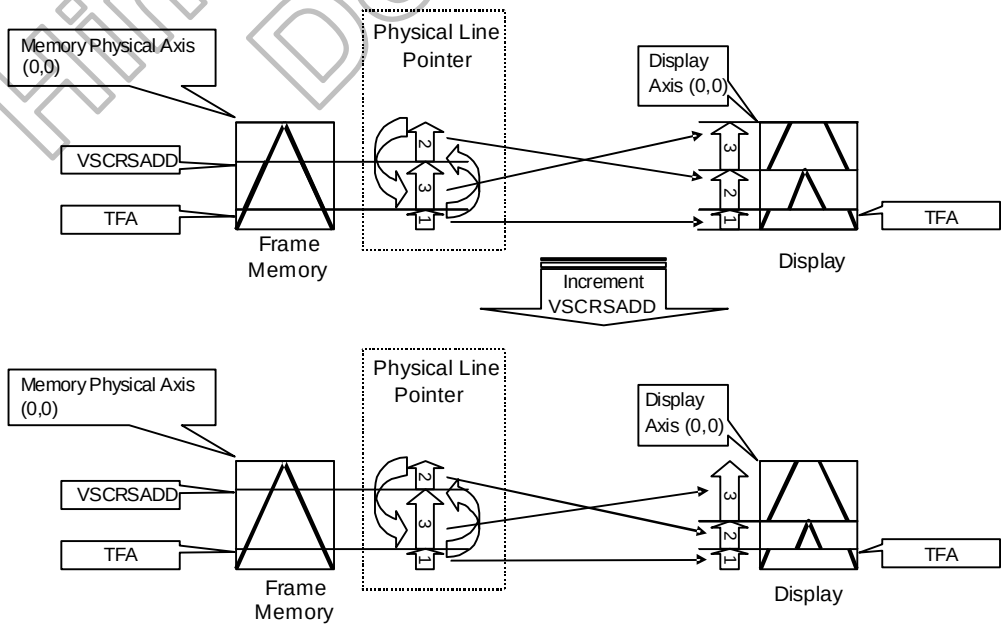


Figure 5.13: Vertical scroll example 2

5.5.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

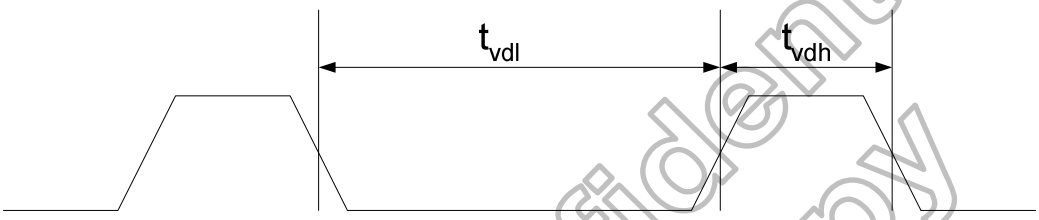


Figure 5.14: Tearing Effect Output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TEP[10:0] setting.

Ex: 1. FB=BP=0x01h (3 line) .
TEP[10:0]=0, then TE signal will output after last line finished.
TEP[10:0]=7, then TE signal will output at second line start.

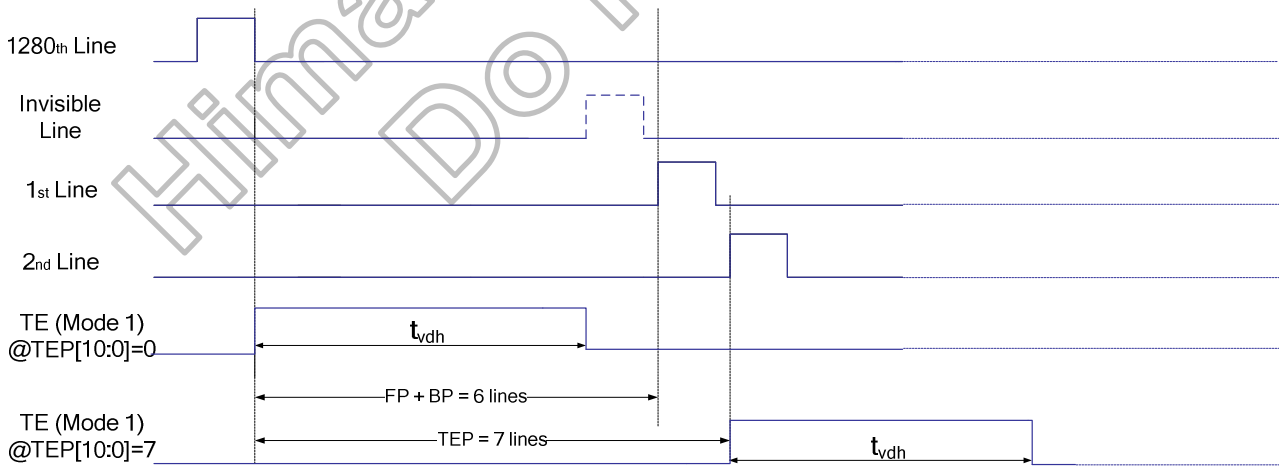


Figure 5.15: TE Delay Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field.

N: If RES_SEL [2:0] set to = 3'b000, the resolution is 800 RGB X 1280, the N=1280.

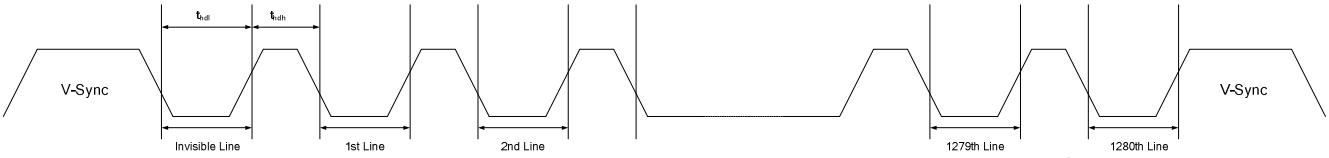


Figure 5.16: Tearing Effect Output signal mode 2

thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Under Mode2, the H-sync pulses output amount will be defined by TESL[15:0] setting.

Ex: 1. TESL[15:0]=0, then TE signal will like TE mode 1.

TESL[15:0]=1, then TE signal will output 1280 H-sync.

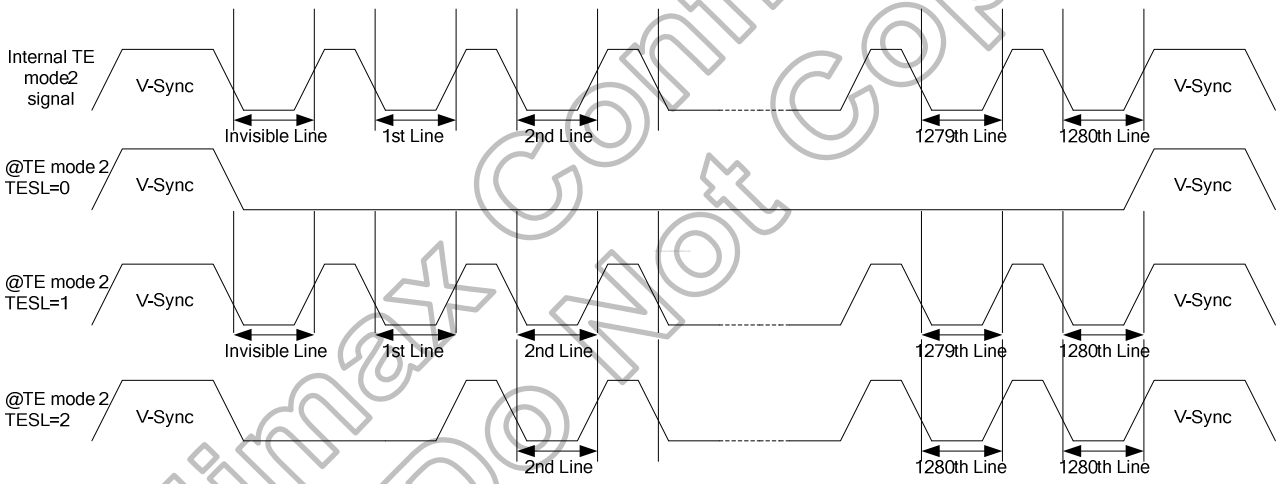


Figure 5.17: TE Output for TELINE setting

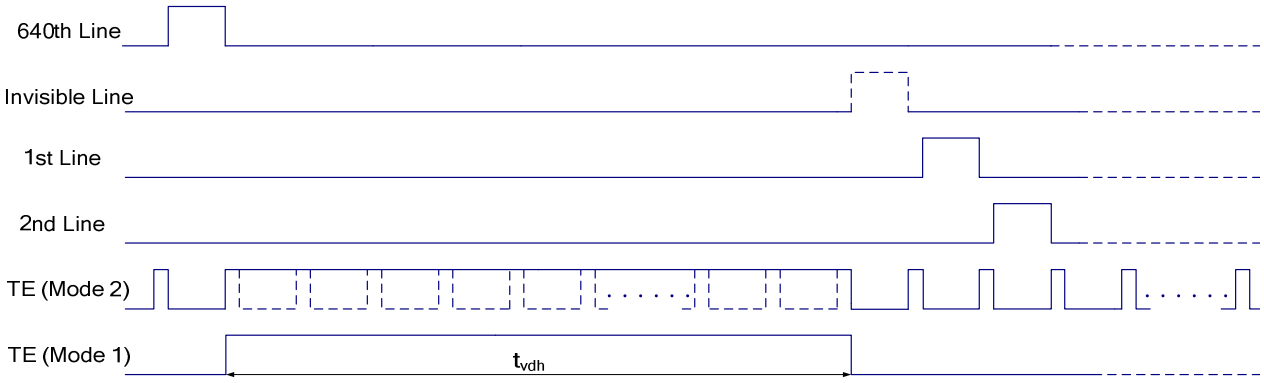


Figure 5.18: Tearing Effect Output signal

Note: During Sleep In Mode, the Tearing Output Pin is active Low

5.5.3.1 Tearing effect line timing

The Tearing Effect signal is described below:

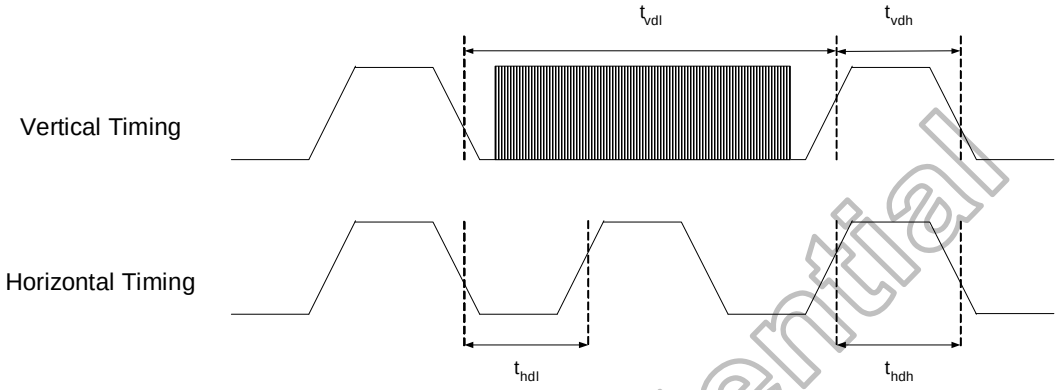


Figure 5.19: Tearing effect output line –tearing effect line timing

Idle Mode Off (Resolution 800x1280 RGB, Frame Rate = 60Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	-	-	ms
tvdh	Vertical Timing High Duration	-	BP+FP	us
thdl	Horizontal Timing Low Duration	-	-	us
thdh	Horizontal Timing High Duration	-	-	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	ns

Note: The timings in Table 5.13 apply when MADCTL ML=0 and ML=1

Table 5.6: AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

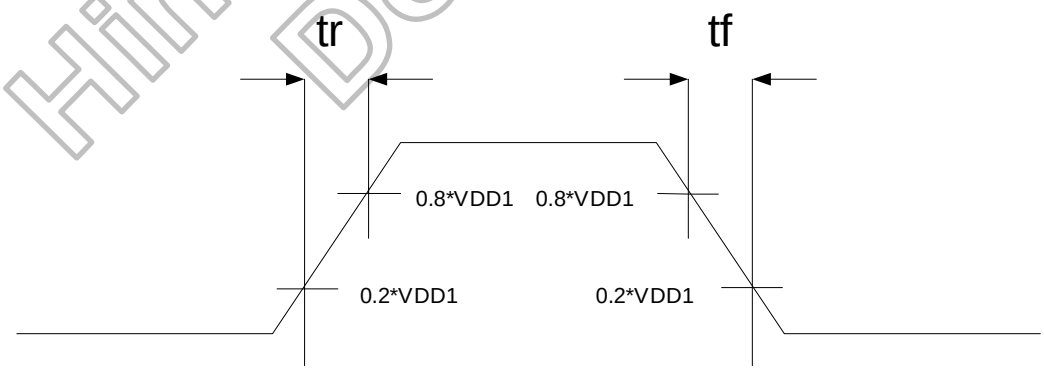


Figure 5.20: Tearing effect output line–definition of tf, tr

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect.

Example 1: MPU write is faster than panel read.

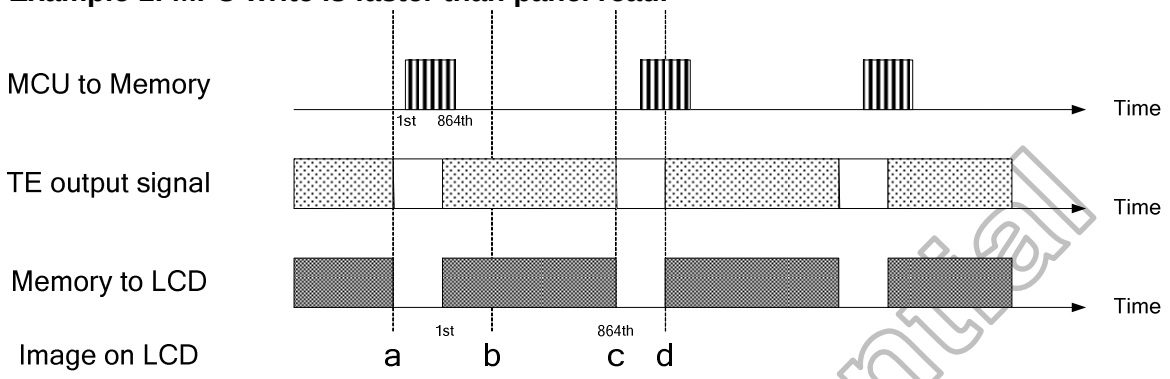


Figure 5.21: Tearing effect output line–example 1 (Timing)

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

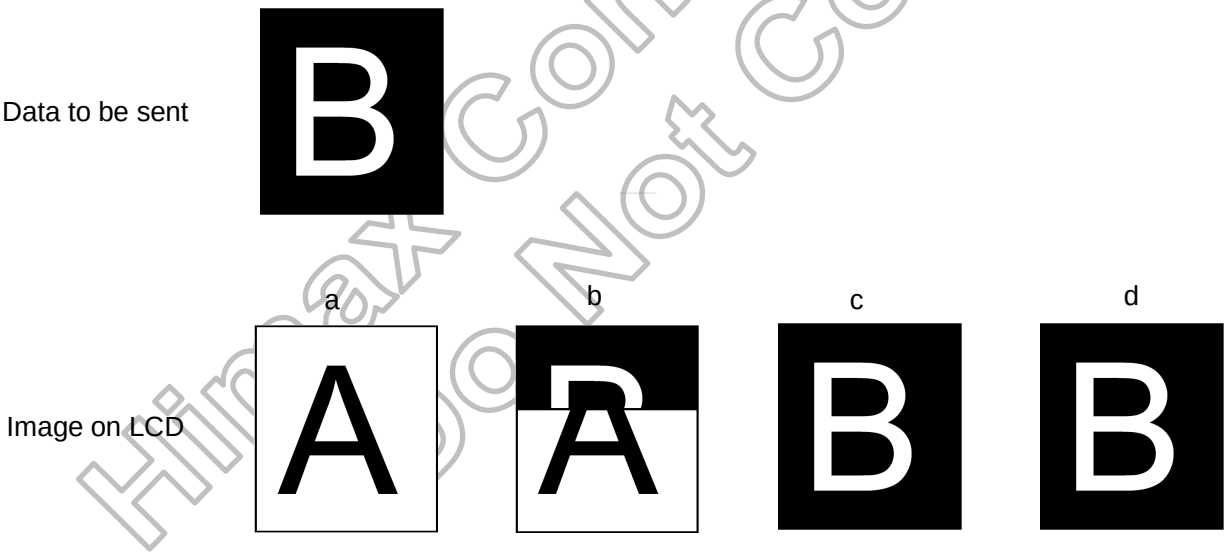


Figure 5.22: Tearing effect output line–example 1 (Image)

Example 2: MPU write is slower than panel read.

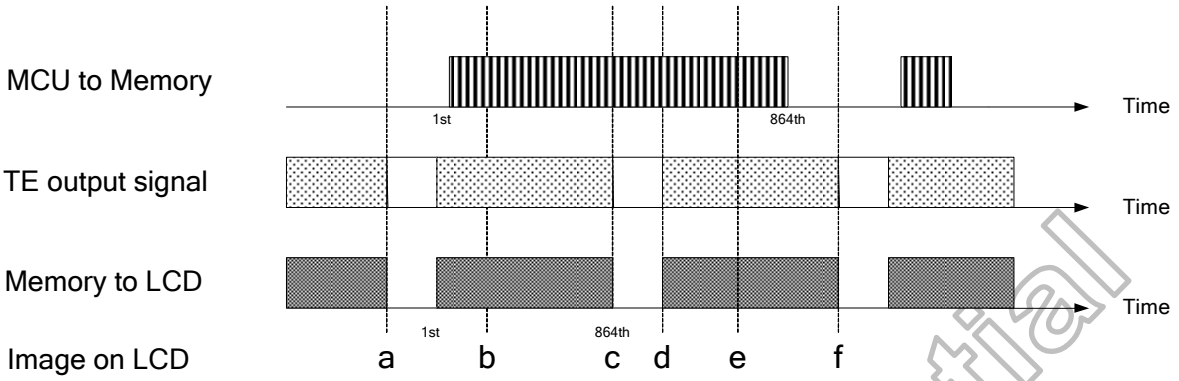


Figure 5.23: Tearing effect output line–example 2 (Timing)

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

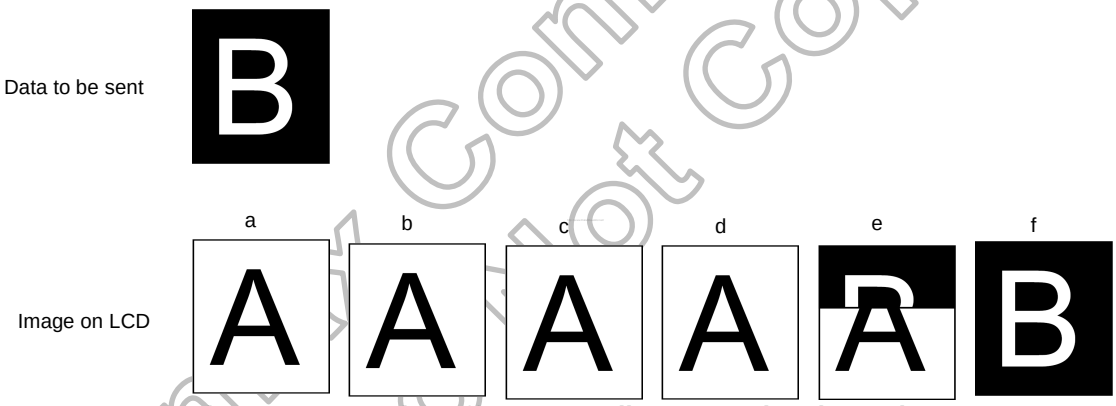


Figure 5.24: Tearing effect output line–example 2 (Image)

5.6 Oscillator

The HX8392-A can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to OSC control register (RB0h). The default frequency is 48MHz. The oscillation frequency tolerance is ±5%.

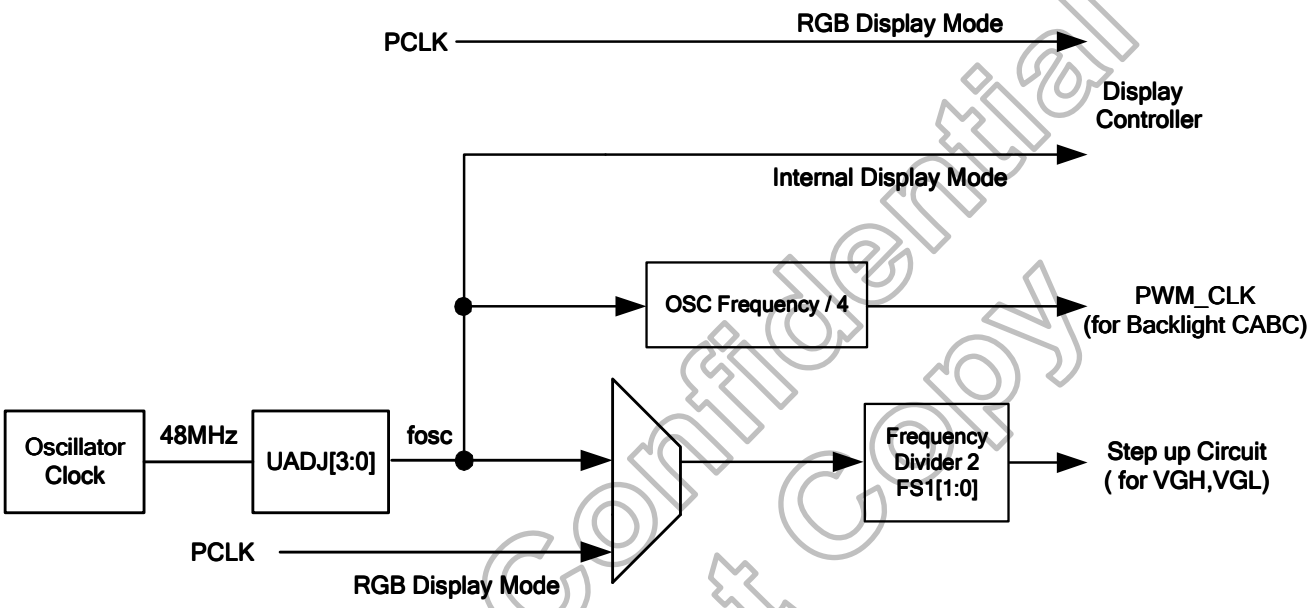


Figure 5.25: OSC aritecture

5.7 Source driver

The HX8392-A contains a 800 channels of source driver which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 800 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

RES_SEL[2:0]	Resolution	Source channels
000	800RGBX1280 dot	S1 ~ S800
001	768RGBX1280 dot	S1 ~ S384, S417~S800
010	720RGBX1280 dot	S1 ~ S360, S441~S800
011	600RGBX1024 dot	S1 ~ S300, S501~S800

Table 5.7: Source output for Panel resolution

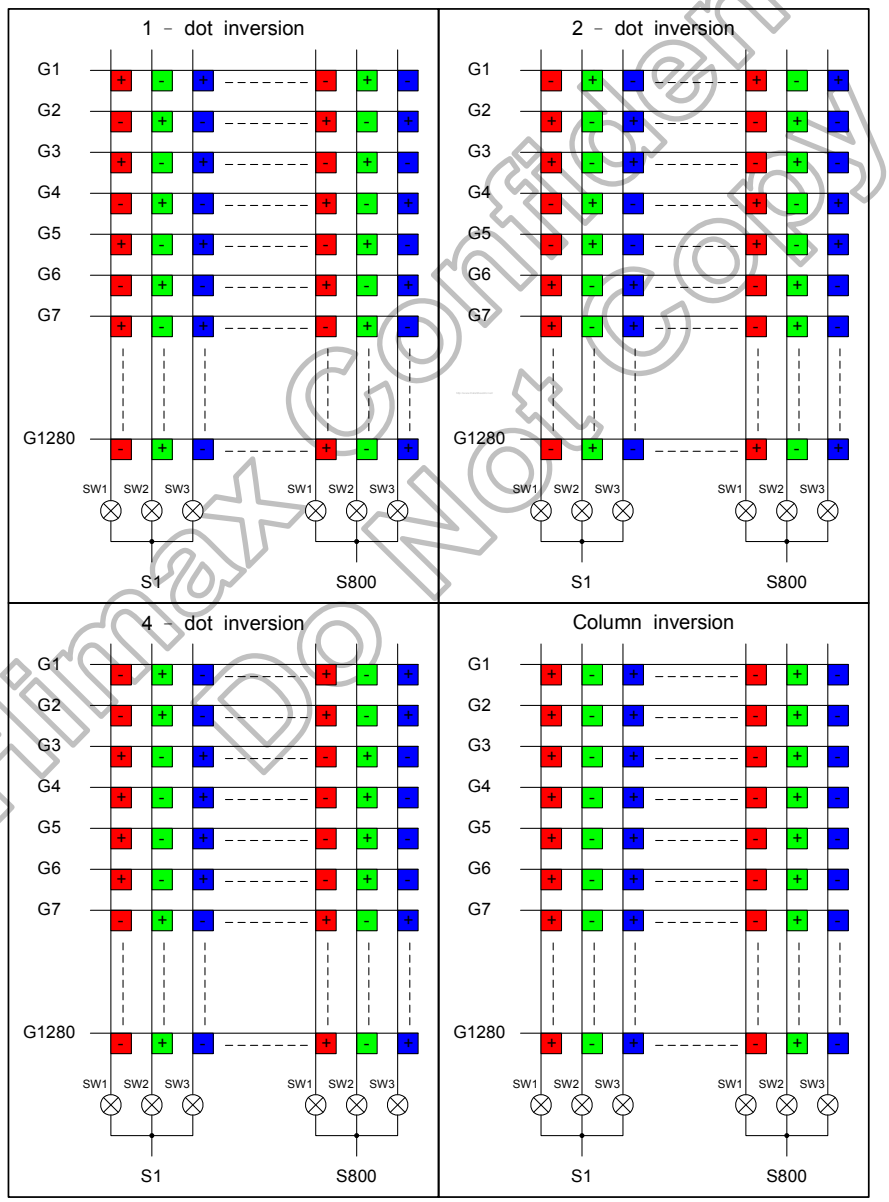


Figure 5.26: Inversion mode

5.8 LCD power generation scheme

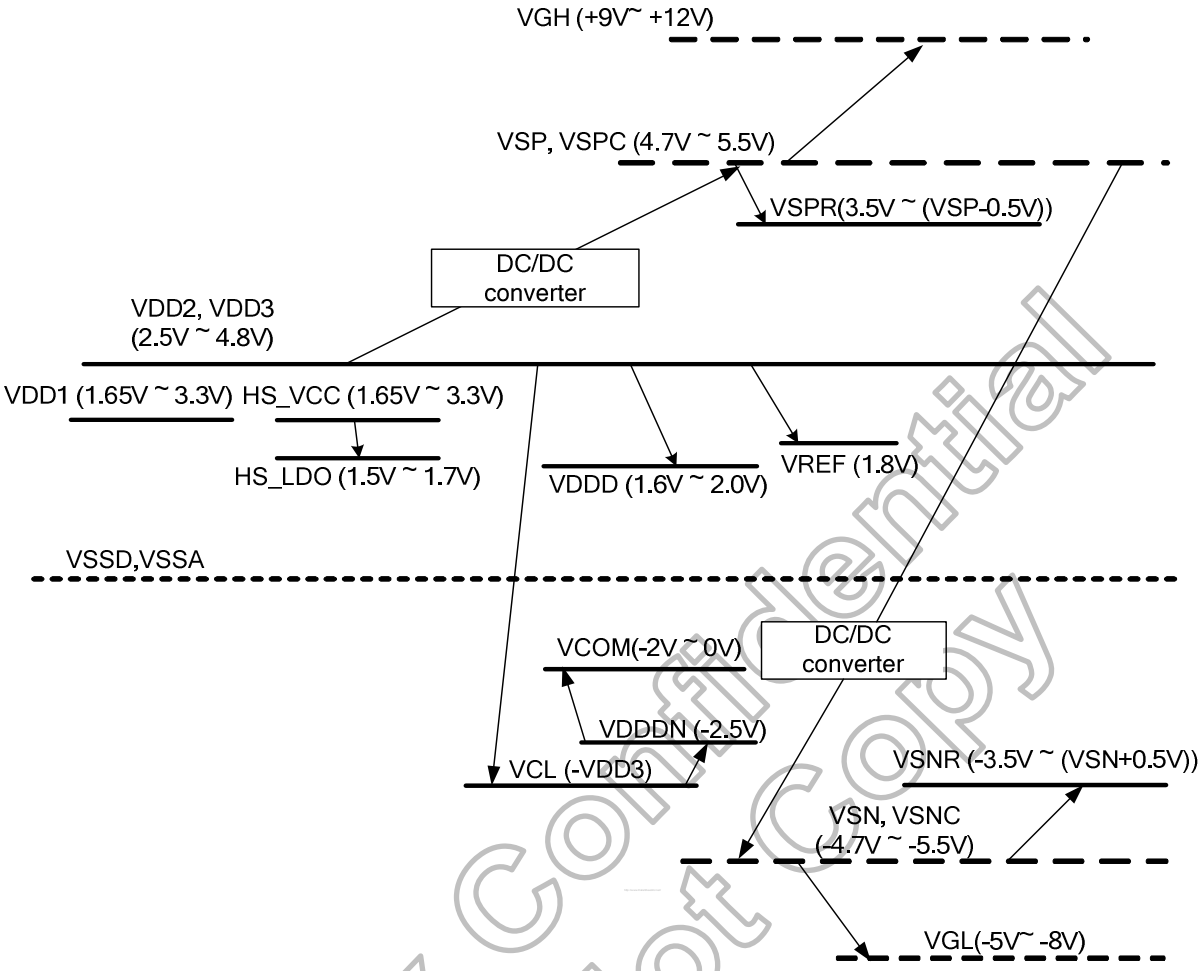


Figure 5.27: LCD power generation scheme

Voltage configuration

HX8392-A has an internal power supply circuit to drive LTPS LCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VREF	Reference voltage from internal band gap circuit	1.8V	-
VSP	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSN	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPC	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSNC	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPR	Reference voltage for gamma circuit	3.5V ~ (VSP – 0.5V)	Reference register
VSNR	Reference voltage for gamma circuit	-3.5V ~ (VSN + 0.5V)	Reference register
VDDDN	Logic power supply	-2.5V	-
VGH	Positive gate driver output voltage level	+9V ~+12V	Depend on VSP and VSN
VGL	Negative gate driver output voltage level	-5V ~ -8V	Depend on VSP and VSN
VCL	DC/DC converter circuit output	-VDD3	Depend on VDD3
VCOM	VCOM DC voltage	-2V ~ 0V	-
HS_LDO	Analog power for Hifh speeg interface circuit	1.5V	Depend on DSI I/F

Table 5.8: Voltage configuration

5.9 DC/DC converter circuit

5.9.1 Use charge pump step up circuit

Use C11P/N,C12P/N,C13P/N,C14P/N C15P/N,C16P/N,C17P/N,C18P/N for VSP generation, and use C23P/N,C24P/N,C31P/N,C32P/N for VSN generation. The output voltage can be set from 4.7 to 5.5V (VSP) and -4.7 to -5.5V (VSN).

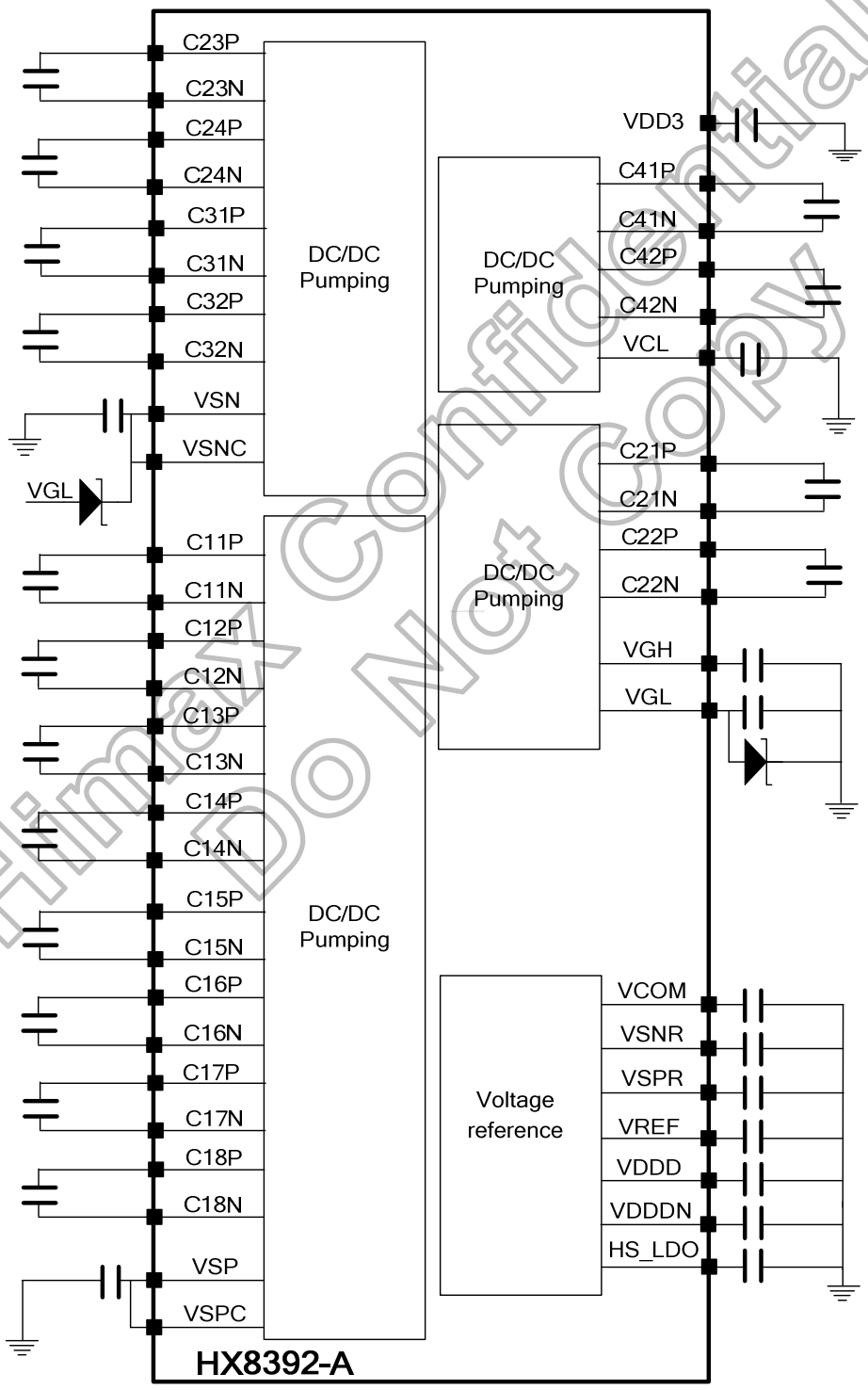


Figure 5.28: DC/DC converter circuit of Internal charge pump

5.9.2 Use HX5186-A

The HX5186-A is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8392-A contains Charge Pump Controller for HX5186-A, including a comparator for VSP/VSN feedback control. HX5186-A can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 4.7 to 5.5 (VSP) and -4.7 to -5.5V (VSN)

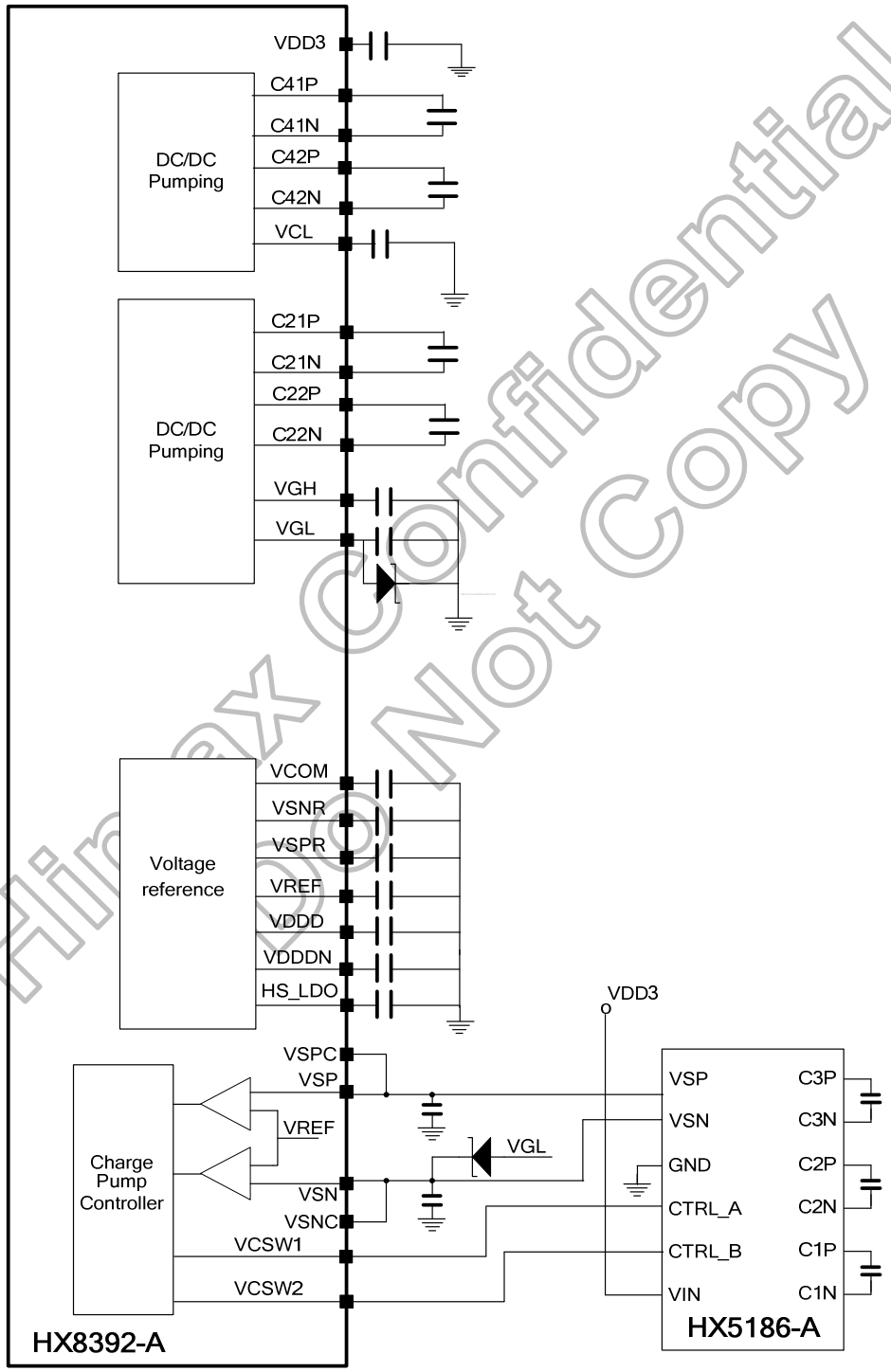


Figure 5.29: DC/DC converter circuit of HX5186-A

5.10 Idle display

The HX8392-A supports an idle display mode. The grayscale level to be used is V0 and V64 with R7, G7, B7 decoding, and the other levels (V1-V63) are halted to reduce power consumption. In idle display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

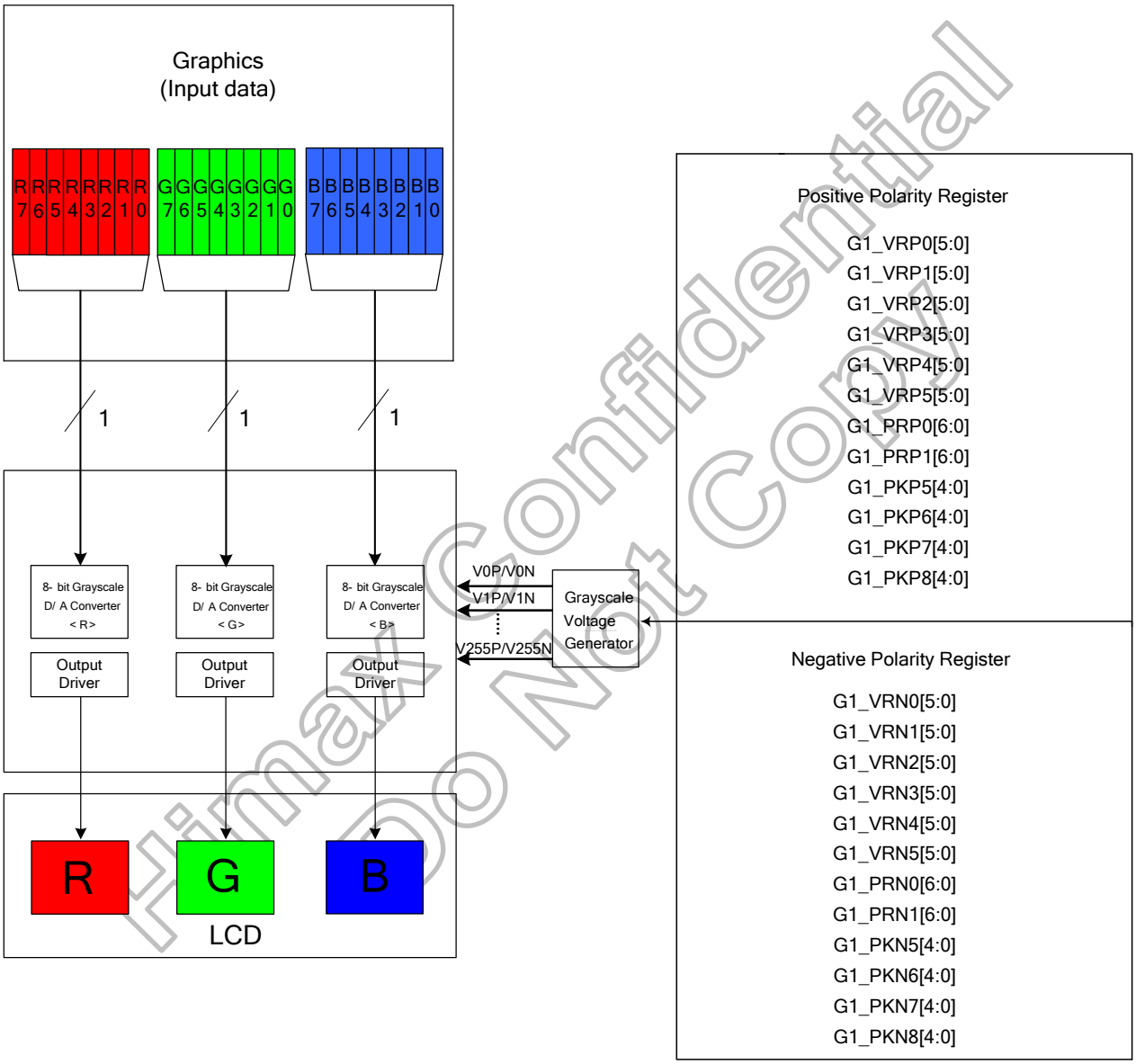


Figure 5.30: Idle mode grayscale control

5.11 Gamma characteristic correction function

The HX8392-A incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

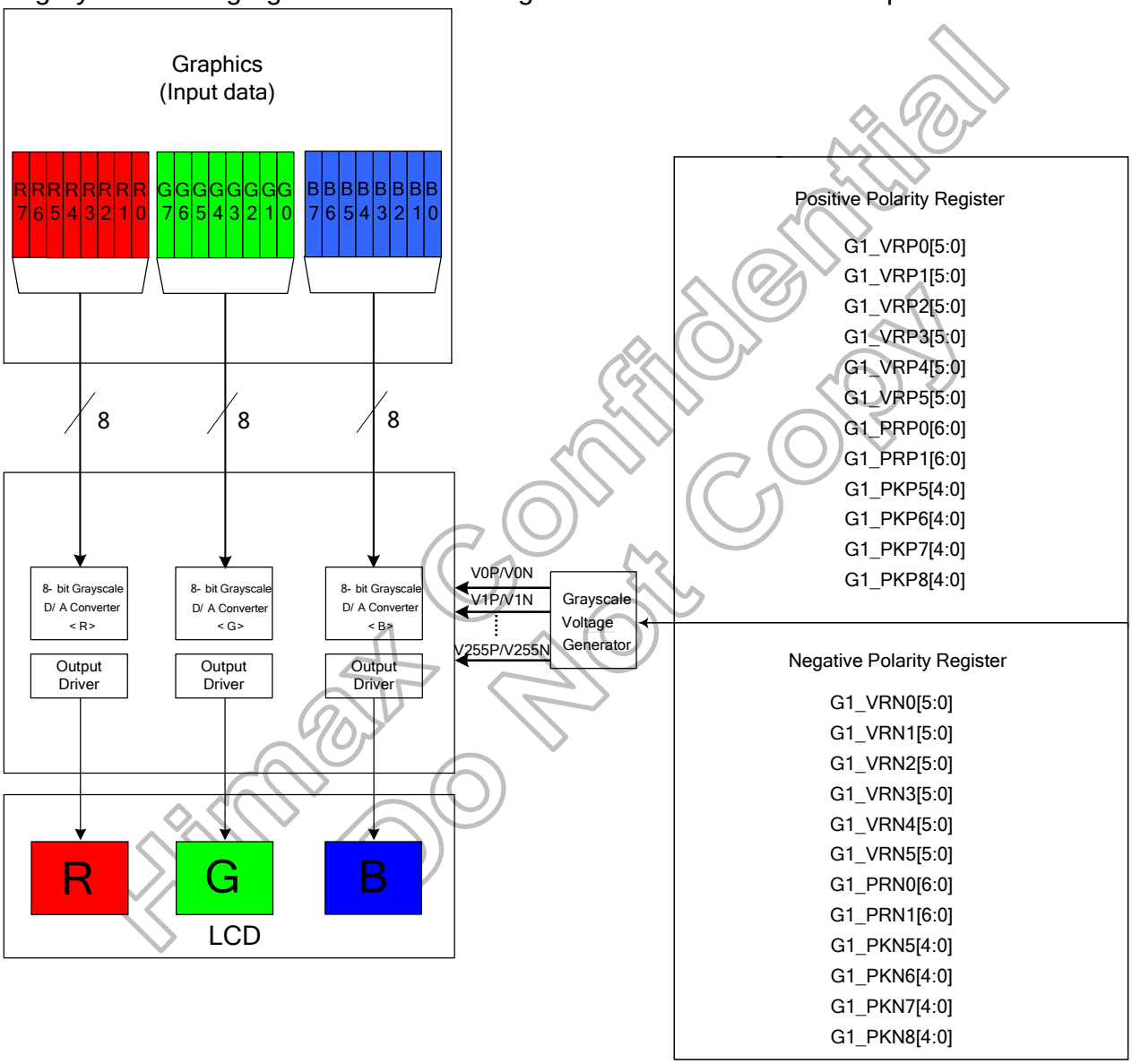


Figure 5.31: Grayscale control

5.11.1 Gamma-Characteristics adjustment register

This HX8392-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

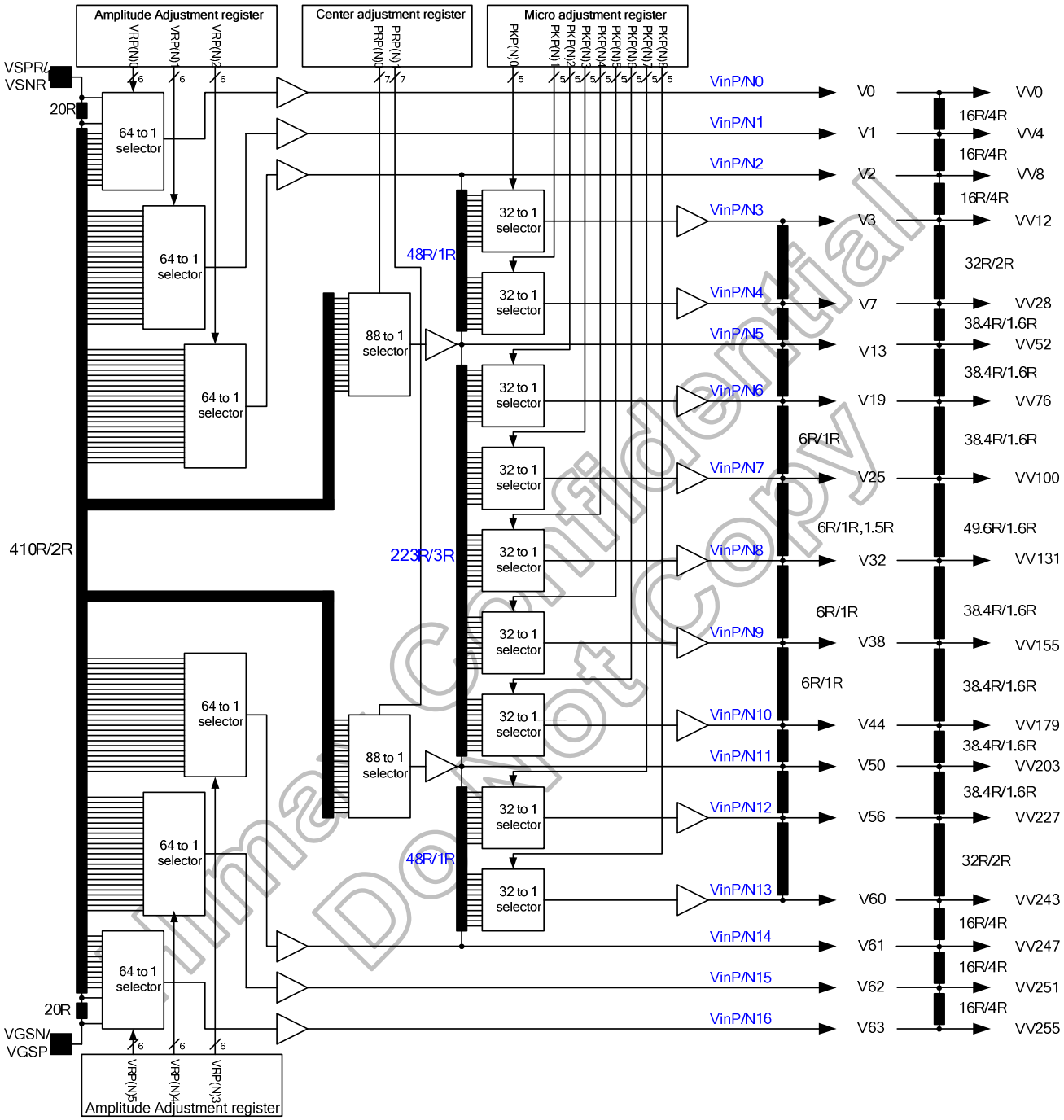
(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N)3, 7, 19, 25, 32, 38, 44, 56, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Table 5.9: Gamma-Adjustment registers

Gamma resister stream and 8 to 1 selector



Note: 1. VV0~VV63 > 1/2VSP of positive output
2. VV193~VV255 > 1/2 VSN of negative output

Figure 5.32: Gamma resister stream and gamma reference voltage

Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0	Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1	Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	20R	000001	2R	000001	2R
000010	22R	000010	4R	000010	4R
000011	24R	000011	6R	000011	6R
• •	• •	• •	• •	• •	• •
011101	76R	011101	58R	011101	58R
011110	78R	011110	60R	011110	60R
011111	80R	011111	62R	011111	62R
100000	82R	100000	64R	100000	64R
100001	84R	100001	66R	100001	66R
100010	86R	100010	68R	100010	68R
• •	• •	• •	• •	• •	• •
111101	140R	111101	122R	111101	122R
111110	142R	111110	124R	111110	124R
111111	144R	111111	126R	111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3	Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4	Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	2R	000001	2R	000001	2R
000010	4R	000010	4R	000010	4R
• •	• •	• •	• •	• •	• •
011101	58R	011101	58R	011101	58R
011110	60R	011110	60R	011110	60R
011111	62R	011111	62R	011111	62R
100000	64R	100000	64R	100000	64R
100001	66R	100001	66R	100001	66R
100010	68R	100010	68R	100010	68R
• •	• •	• •	• •	• •	• •
111100	120R	111100	120R	111100	120R
111101	122R	111101	122R	111101	122R
111110	124R	111110	124R	111110	124R
111111	126R	111111	126R	111111	144R

Table 5.10: Offset adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0	Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R	0000000	0R
0000001	2R	0000001	2R
0000010	4R	0000010	4R
• •	• •	• •	• •
1010101	170R	1010101	170R
1010110	172R	1010110	172R
1010111	174R	1010111	174R

Table 5.11: Center adjustment

The grayscale levels are determined by the following formulas:

Reference voltage	Macro adjustment value	VinP0 formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110000	((450R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110001	((450R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110010	((450R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110011	((450R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110100	((450R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110101	((450R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110110	((450R - 126R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110111	((450R - 128R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111000	((450R - 130R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111001	((450R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111010	((450R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111011	((450R - 136R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111100	((450R - 138R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111101	((450R - 140R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111110	((450R - 142R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111111	((450R - 144R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.12: VinP0

Reference voltage	Macro adjustment value	VinP1 formula
VinP1	VRP1 5-0 = 000000	(430R / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000001	((430R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000010	((430R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000011	((430R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000100	((430R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000101	((430R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000110	((430R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000111	((430R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001000	((430R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001001	((430R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001010	((430R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001011	((430R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001100	((430R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001101	((430R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001110	((430R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001111	((430R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010000	((430R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010001	((430R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010010	((430R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010011	((430R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010100	((430R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010101	((430R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010110	((430R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010111	((430R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011000	((430R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011001	((430R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011010	((430R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011011	((430R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011100	((430R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011101	((430R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011110	((430R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011111	((430R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100000	((430R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100001	((430R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100010	((430R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100011	((430R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100100	((430R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100101	((430R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100110	((430R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100111	((430R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101000	((430R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101001	((430R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101010	((430R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101011	((430R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101100	((430R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101101	((430R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101110	((430R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101111	((430R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110000	((430R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110001	((430R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110010	((430R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110011	((430R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110100	((430R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110101	((430R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110110	((430R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110111	((430R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111000	((430R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111001	((430R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111010	((430R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111011	((430R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111100	((430R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111101	((430R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111110	((430R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111111	((430R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.13: VinP1

Reference voltage	Macro adjustment value	VinP2 formula
VinP2	VRP2 5-0 = 000000	(420R / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000001	((420R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000010	((420R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000011	((420R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000100	((420R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000101	((420R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000110	((420R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000111	((420R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001000	((420R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001001	((420R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001010	((420R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001011	((420R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001100	((420R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001101	((420R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001110	((420R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001111	((420R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010000	((420R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010001	((420R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010010	((420R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010011	((420R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010100	((420R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010101	((420R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010110	((420R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010111	((420R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011000	((420R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011001	((420R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011010	((420R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011011	((420R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011100	((420R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011101	((420R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011110	((420R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011111	((420R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100000	((420R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100001	((420R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100010	((420R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100011	((420R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100100	((420R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100101	((420R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100110	((420R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100111	((420R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101000	((420R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101001	((420R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101010	((420R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101011	((420R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101100	((420R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101101	((420R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101110	((420R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101111	((420R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110000	((420R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110001	((420R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110010	((420R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110011	((420R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110100	((420R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110101	((420R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110110	((420R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110111	((420R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111000	((420R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111001	((420R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111010	((420R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111011	((420R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111100	((420R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111101	((420R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111110	((420R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111111	((420R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.14: VinP2

Reference voltage	Macro adjustment value	VinP14 formula
VinP14	VRP3 5-0 = 000000	(156R / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000001	((156R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000010	((156R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000011	((156R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000100	((156R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000101	((156R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000110	((156R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000111	((156R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001000	((156R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001001	((156R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001010	((156R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001011	((156R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001100	((156R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001101	((156R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001110	((156R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001111	((156R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010000	((156R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010001	((156R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010010	((156R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010011	((156R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010100	((156R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010101	((156R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010110	((156R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010111	((156R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011000	((156R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011001	((156R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011010	((156R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011011	((156R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011100	((156R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011101	((156R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011110	((156R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011111	((156R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100000	((156R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100001	((156R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100010	((156R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100011	((156R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100100	((156R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100101	((156R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100110	((156R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100111	((156R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101000	((156R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101001	((156R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101010	((156R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101011	((156R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101100	((156R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101101	((156R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101110	((156R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101111	((156R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110000	((156R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110001	((156R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110010	((156R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110011	((156R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110100	((156R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110101	((156R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110110	((156R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110111	((156R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111000	((156R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111001	((156R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111010	((156R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111011	((156R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111100	((156R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111101	((156R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111110	((156R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111111	((156R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.15: VinP14

Reference voltage	Macro adjustment value	VinP15 formula
VinP15	VRP4 5-0 = 000000	(146R / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000001	((146R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000010	((146R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000011	((146R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000100	((146R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000101	((146R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000110	((146R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000111	((146R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001000	((146R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001001	((146R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001010	((146R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001011	((146R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001100	((146R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001101	((146R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001110	((146R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001111	((146R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010000	((146R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010001	((146R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010010	((146R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010011	((146R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010100	((146R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010101	((146R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010110	((146R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010111	((146R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011000	((146R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011001	((146R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011010	((146R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011011	((146R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011100	((146R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011101	((146R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011110	((146R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011111	((146R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100000	((146R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100001	((146R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100010	((146R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100011	((146R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100100	((146R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100101	((146R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100110	((146R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100111	((146R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101000	((146R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101001	((146R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101010	((146R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101011	((146R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101100	((146R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101101	((146R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101110	((146R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101111	((146R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110000	((146R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110001	((146R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110010	((146R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110011	((146R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110100	((146R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110101	((146R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110110	((146R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110111	((146R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111000	((146R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111001	((146R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111010	((146R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111011	((146R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111100	((146R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111101	((146R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111110	((146R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111111	((146R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.16: VinP15

Reference voltage	Macro adjustment value	VinP16 formula
VinP16	VRP5 5-0 = 000000	(144R / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000001	((144R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000010	((144R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000011	((144R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000100	((144R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000101	((144R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000110	((144R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000111	((144R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001000	((144R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001001	((144R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001010	((144R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001011	((144R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001100	((144R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001101	((144R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001110	((144R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001111	((144R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010000	((144R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010001	((144R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010010	((144R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010011	((144R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010100	((144R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010101	((144R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010110	((144R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010111	((144R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011000	((144R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011001	((144R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011010	((144R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011011	((144R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011100	((144R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011101	((144R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011110	((144R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011111	((144R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100000	((144R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100001	((144R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100010	((144R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100011	((144R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100100	((144R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100101	((144R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100110	((144R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100111	((144R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101000	((144R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101001	((144R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101010	((144R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101011	((144R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101100	((144R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101101	((144R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101110	((144R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101111	((144R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110000	((144R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110001	((144R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110010	((144R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110011	((144R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110100	((144R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110101	((144R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110110	((144R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110111	((144R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111000	((144R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111001	((144R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111010	((144R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111011	((144R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111100	((144R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111101	((144R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111110	((144R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111111	VGSP

Table 5.17: VinP16

Reference voltage	Macro adjustment value	VinP5 formula
VinP5	PRP0 6-0 = 0000000	(350R / 450R) (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000011	((350R – 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000100	((350R – 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000101	((350R – 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000110	((350R – 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000111	((350R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001000	((350R – 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001001	((350R – 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001010	((350R – 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001011	((350R – 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001100	((350R – 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001101	((350R – 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001110	((350R – 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001111	((350R – 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010000	((350R – 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010010	((350R – 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010011	((350R – 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010100	((350R – 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010101	((350R – 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010110	((350R – 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010111	((350R – 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011000	((350R – 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011001	((350R – 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011010	((350R – 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011100	((350R – 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011101	((350R – 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011110	((350R – 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011111	((350R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100001	((350R – 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100010	((350R – 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100011	((350R – 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100100	((350R – 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100101	((350R – 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100110	((350R – 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100111	((350R – 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101000	((350R – 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101001	((350R – 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101011	((350R – 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101100	((350R – 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101101	((350R – 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101110	((350R – 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101111	((350R – 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110000	((350R – 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110001	((350R – 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110010	((350R – 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110011	((350R – 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110100	((350R – 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110101	((350R – 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110110	((350R – 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110111	((350R – 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111000	((350R – 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111001	((350R – 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111010	((350R – 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111011	((350R – 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111100	((350R – 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111101	((350R – 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111110	((350R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111111	((350R – 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000000	((350R – 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000001	((350R – 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000010	((350R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000011	((350R – 134R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000100	((350R – 136R) / 450R) * (VSPR - VGSP) + VGSP

	PRP0 6-0 = 1000101	((350R – 138R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000110	((350R – 140R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000111	((350R – 142R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001000	((350R – 144R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001001	((350R – 146R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001010	((350R – 148R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001011	((350R – 150R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001100	((350R - 152R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001101	((350R – 154R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001110	((350R – 156R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001111	((350R – 158R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010000	((350R – 160R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010001	((350R – 162R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010010	((350R – 164R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010011	((350R – 166R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010100	((350R – 168R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010101	((350R – 170R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010110	((350R – 172R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010111	((350R - 174R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1011000	inhibit
	PRP0 6-0 = 1011001	inhibit
	PRP0 6-0 = 1011010	inhibit
	PRP0 6-0 = 1011011	inhibit
	PRP0 6-0 = 1011100	inhibit
	PRP0 6-0 = 1011101	inhibit
	PRP0 6-0 = 1011110	inhibit
	PRP0 6-0 = 1011111	inhibit
	PRP0 6-0 = 1100000	inhibit
	PRP0 6-0 = 1100001	inhibit
	PRP0 6-0 = 1100010	inhibit
	PRP0 6-0 = 1100011	inhibit
	PRP0 6-0 = 1100100	inhibit
	PRP0 6-0 = 1100101	inhibit
	PRP0 6-0 = 1100110	inhibit
	PRP0 6-0 = 1100111	inhibit
	PRP0 6-0 = 1101000	inhibit
	PRP0 6-0 = 1101001	inhibit
	PRP0 6-0 = 1101010	inhibit
	PRP0 6-0 = 1101011	inhibit
	PRP0 6-0 = 1101100	inhibit
	PRP0 6-0 = 1101101	inhibit
	PRP0 6-0 = 1101110	inhibit
	PRP0 6-0 = 1101111	inhibit
	PRP0 6-0 = 1110000	inhibit
	PRP0 6-0 = 1110001	inhibit
	PRP0 6-0 = 1110010	inhibit
	PRP0 6-0 = 1110011	inhibit
	PRP0 6-0 = 1110100	inhibit
	PRP0 6-0 = 1110101	inhibit
	PRP0 6-0 = 1110110	inhibit
	PRP0 6-0 = 1110111	inhibit
	PRP0 6-0 = 1111000	inhibit
	PRP0 6-0 = 1111001	inhibit
	PRP0 6-0 = 1111010	inhibit
	PRP0 6-0 = 1111011	inhibit
	PRP0 6-0 = 1111100	inhibit
	PRP0 6-0 = 1111101	inhibit
	PRP0 6-0 = 1111110	inhibit
	PRP0 6-0 = 1111111	inhibit

Table 5.18: VinP5

Reference voltage	Macro adjustment value	VinP11 formula
VinP11	PRP1 6-0 = 0000000	(274R / 450R) (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000011	((274R – 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000100	((274R – 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000101	((274R – 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000110	((274R – 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000111	((274R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001000	((274R – 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001001	((274R – 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001010	((274R – 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001011	((274R – 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001100	((274R – 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001101	((274R – 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001110	((274R – 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001111	((274R – 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010000	((274R – 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010010	((274R – 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010011	((274R – 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010100	((274R – 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010101	((274R – 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010110	((274R – 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010111	((274R – 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011000	((274R – 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011001	((274R – 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011010	((274R – 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011100	((274R – 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011101	((274R – 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011110	((274R – 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011111	((274R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100001	((274R – 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100010	((274R – 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100011	((274R – 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100100	((274R – 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100101	((274R – 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100110	((274R – 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100111	((274R – 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101000	((274R – 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101001	((274R – 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101011	((274R – 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101100	((274R – 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101101	((274R – 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101110	((274R – 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101111	((274R – 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110000	((274R – 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110001	((274R – 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110010	((274R – 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110011	((274R – 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110100	((274R – 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110101	((274R – 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110110	((274R – 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110111	((274R – 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111000	((274R – 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111001	((274R – 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111010	((274R – 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111011	((274R – 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111100	((274R – 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111101	((274R – 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111111	((274R – 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000000	((274R – 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000001	((274R – 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000011	((274R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000100	((274R – 136R) / 450R) * (VSPR - VGSP) + VGSP

	PRP1 6-0 = 1000101	((274R – 138R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000110	((274R – 140R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000111	((274R – 142R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001000	((274R – 144R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001001	((274R – 146R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001010	((274R – 148R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001011	((274R – 150R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001100	((274R - 152R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001101	((274R – 154R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001110	((274R – 156R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001111	((274R – 158R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010000	((274R – 160R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010001	((274R – 162R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010010	((274R – 164R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010011	((274R – 166R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010100	((274R – 168R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010101	((274R – 170R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010110	((274R – 172R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010111	((274R - 174R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1011000	inhibit
	PRP1 6-0 = 1011001	inhibit
	PRP1 6-0 = 1011010	inhibit
	PRP1 6-0 = 1011011	inhibit
	PRP1 6-0 = 1011100	inhibit
	PRP1 6-0 = 1011101	inhibit
	PRP1 6-0 = 1011110	inhibit
	PRP1 6-0 = 1011111	inhibit
	PRP1 6-0 = 1100000	inhibit
	PRP1 6-0 = 1100001	inhibit
	PRP1 6-0 = 1100010	inhibit
	PRP1 6-0 = 1100011	inhibit
	PRP1 6-0 = 1100100	inhibit
	PRP1 6-0 = 1100101	inhibit
	PRP1 6-0 = 1100110	inhibit
	PRP1 6-0 = 1100111	inhibit
	PRP1 6-0 = 1101000	inhibit
	PRP1 6-0 = 1101001	inhibit
	PRP1 6-0 = 1101010	inhibit
	PRP1 6-0 = 1101011	inhibit
	PRP1 6-0 = 1101100	inhibit
	PRP1 6-0 = 1101101	inhibit
	PRP1 6-0 = 1101110	inhibit
	PRP1 6-0 = 1101111	inhibit
	PRP1 6-0 = 1110000	inhibit
	PRP1 6-0 = 1110001	inhibit
	PRP1 6-0 = 1110010	inhibit
	PRP1 6-0 = 1110011	inhibit
	PRP1 6-0 = 1110100	inhibit
	PRP1 6-0 = 1110101	inhibit
	PRP1 6-0 = 1110110	inhibit
	PRP1 6-0 = 1110111	inhibit
	PRP1 6-0 = 1111000	inhibit
	PRP1 6-0 = 1111001	inhibit
	PRP1 6-0 = 1111010	inhibit
	PRP1 6-0 = 1111011	inhibit
	PRP1 6-0 = 1111100	inhibit
	PRP1 6-0 = 1111101	inhibit
	PRP1 6-0 = 1111110	inhibit
	PRP1 6-0 = 1111111	inhibit

Table 5.19: VinP11

Reference voltage	Macro adjustment value	VinP3 formula
VinP3	PKP0 4-0 = 00000	(47R / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00001	((47R – 1R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00010	((47R – 2R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00011	((47R – 3R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00100	((47R – 4R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00101	((47R – 5R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00110	((47R – 6R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00111	((47R – 7R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01000	((47R – 8R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01001	((47R – 9R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01010	((47R - 10R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01011	((47R - 11R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01100	((47R - 12R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01101	((47R - 13R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01110	((47R - 14R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01111	((47R - 15R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10000	((47R - 16R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10001	((47R - 17R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10010	((47R - 18R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10011	((47R - 19R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10100	((47R - 20R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10101	((47R - 21R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10110	((47R - 22R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10111	((47R - 23R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11000	((47R - 24R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11001	((47R - 25R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11010	((47R - 26R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11011	((47R - 27R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11100	((47R - 28R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11101	((47R - 29R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11110	((47R - 30R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11111	((47R - 31R) / 48R) * (VinP2 - VinP5) + VinP5

Table 5.20: VinP3

Reference voltage	Macro adjustment value	VinP4 formula
VinP4	PKP1 4-0 = 00000	(32R / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00001	((32R - 1R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00010	((32R - 2R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00011	((32R - 3R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00100	((32R - 4R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00101	((32R - 5R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00110	((32R - 6R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00111	((32R - 7R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01000	((32R - 8R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01001	((32R - 9R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01010	((32R - 10R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01011	((32R - 11R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01100	((32R - 12R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01101	((32R - 13R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01110	((32R - 14R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01111	((32R - 15R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10000	((32R - 16R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10001	((32R - 17R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10010	((32R - 18R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10011	((32R - 19R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10100	((32R - 20R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10101	((32R - 21R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10110	((32R - 22R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10111	((32R - 23R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11000	((32R - 24R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11001	((32R - 25R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11010	((32R - 26R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11011	((32R - 27R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11100	((32R - 28R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11101	((32R - 29R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11110	((32R - 30R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11111	((32R - 31R) / 48R) * (VinP2 - VinP5) + VinP5

Table 5.21: VinP4

Reference voltage	Macro adjustment value	VinP6 formula
VinP6	PKP2 4-0 = 00000	(220R / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00001	((220R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00010	((220R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00011	((220R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00100	((220R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00101	((220R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00110	((220R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00111	((220R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01000	((220R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01001	((220R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01010	((220R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01011	((220R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01100	((220R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01101	((220R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01110	((220R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01111	((220R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10000	((220R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10001	((220R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10010	((220R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10011	((220R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10100	((220R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10101	((220R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10110	((220R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10111	((220R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11000	((220R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11001	((220R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11010	((220R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11011	((220R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11100	((220R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11101	((220R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11110	((220R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11111	((220R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.22: VinP6

Reference voltage	Macro adjustment value	VinP7 formula
VinP7	PKP3 4-0 = 00000	(193R / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00001	((193R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00010	((193R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00011	((193R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00100	((193R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00101	((193R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00110	((193R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00111	((193R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01000	((193R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01001	((193R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01010	((193R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01011	((193R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01100	((193R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01101	((193R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01110	((193R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01111	((193R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10000	((193R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10001	((193R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10010	((193R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10011	((193R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10100	((193R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10101	((193R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10110	((193R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10111	((193R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11000	((193R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11001	((193R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11010	((193R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11011	((193R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11100	((193R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11101	((193R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11110	((193R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11111	((193R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.23: VinP7

Reference voltage	Macro adjustment value	VinP8 formula
VinP8	PKP4 4-0 = 00000	(158R / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00001	((158R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00010	((158R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00011	((158R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00100	((158R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00101	((158R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00110	((158R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00111	((158R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01000	((158R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01001	((158R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01010	((158R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01011	((158R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01100	((158R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01101	((158R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01110	((158R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01111	((158R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10000	((158R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10001	((158R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10010	((158R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10011	((158R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10100	((158R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10101	((158R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10110	((158R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10111	((158R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11000	((158R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11001	((158R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11010	((158R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11011	((158R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11100	((158R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11101	((158R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11110	((158R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11111	((158R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.24: VinP8

Reference voltage	Macro adjustment value	VinP9 formula
VinP9	PKP5 4-0 = 00000	(123R / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00001	((123R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00010	((123R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00011	((123R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00100	((123R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00101	((123R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00110	((123R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00111	((123R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01000	((123R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01001	((123R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01010	((123R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01011	((123R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01100	((123R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01101	((123R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01110	((123R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01111	((123R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10000	((123R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10001	((123R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10010	((123R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10011	((123R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10100	((123R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10101	((123R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10110	((123R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10111	((123R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11000	((123R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11001	((123R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11010	((123R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11011	((123R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11100	((123R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11101	((123R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11110	((123R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11111	((123R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.25: VinP9

Reference voltage	Macro adjustment value	VinP10 formula
VinP10	PKP6 4-0 = 00000	(96R / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00001	((96R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00010	((96R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00011	((96R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00100	((96R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00101	((96R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00110	((96R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00111	((96R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01000	((96R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01001	((96R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01010	((96R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01011	((96R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01100	((96R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01101	((96R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01110	((96R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01111	((96R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10000	((96R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10001	((96R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10010	((96R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10011	((96R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10100	((96R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10101	((96R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10110	((96R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10111	((96R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11000	((96R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11001	((96R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11010	((96R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11011	((96R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11100	((96R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11101	((96R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11110	((96R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11111	((96R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.26: VinP10

Reference voltage	Macro adjustment value	VinP12 formula
VinP12	PKP7 4-0 = 00000	(47R / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00001	((47R - 1R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00010	((47R - 2R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00011	((47R - 3R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00100	((47R - 4R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00101	((47R - 5R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00110	((47R - 6R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00111	((47R - 7R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01000	((47R - 8R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01001	((47R - 9R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01010	((47R - 10R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01011	((47R - 11R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01100	((47R - 12R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01101	((47R - 13R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01110	((47R - 14R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01111	((47R - 15R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10000	((47R - 16R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10001	((47R - 17R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10010	((47R - 18R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10011	((47R - 19R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10100	((47R - 20R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10101	((47R - 21R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10110	((47R - 22R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10111	((47R - 23R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11000	((47R - 24R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11001	((47R - 25R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11010	((47R - 26R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11011	((47R - 27R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11100	((47R - 28R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11101	((47R - 29R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11110	((47R - 30R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11111	((47R - 31R) / 48R) * (VinP11 - VinP14) + VinP14

Table 5.27: VinP12

Reference voltage	Macro adjustment value	VinP13 formula
VinP13	PKP8 4-0 = 00000	(32R / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00001	((32R - 1R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00010	((32R - 2R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00011	((32R - 3R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00100	((32R - 4R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00101	((32R - 5R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00110	((32R - 6R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00111	((32R - 7R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01000	((32R - 8R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01001	((32R - 9R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01010	((32R - 10R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01011	((32R - 11R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01100	((32R - 12R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01101	((32R - 13R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01110	((32R - 14R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01111	((32R - 15R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10000	((32R - 16R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10001	((32R - 17R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10010	((32R - 18R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10011	((32R - 19R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10100	((32R - 20R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10101	((32R - 21R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10110	((32R - 22R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10111	((32R - 23R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11000	((32R - 24R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11001	((32R - 25R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11010	((32R - 26R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11011	((32R - 27R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11100	((32R - 28R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11101	((32R - 29R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11110	((32R - 30R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11111	((32R - 31R) / 48R) * (VinP11 - VinP14) + VinP14

Table 5.28: VinP13

Reference voltage	Macro adjustment value	VinN0 formula
VinN0	VRN0 5-0 = 000000	VSNR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.29: VinN0

Reference voltage	Macro adjustment value	VinN1 formula
VinN1	VRN1 5-0 = 000000	(430R / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000001	((430R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000010	((430R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000011	((430R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000100	((430R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000101	((430R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000110	((430R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000111	((430R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001000	((430R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001001	((430R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001010	((430R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001011	((430R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001100	((430R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001101	((430R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001110	((430R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001111	((430R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010000	((430R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010001	((430R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010010	((430R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010011	((430R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010100	((430R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010101	((430R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010110	((430R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010111	((430R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011000	((430R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011001	((430R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011010	((430R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011011	((430R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011100	((430R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011101	((430R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011110	((430R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011111	((430R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100000	((430R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100001	((430R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100010	((430R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100011	((430R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100100	((430R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100101	((430R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100110	((430R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100111	((430R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101000	((430R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101001	((430R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101010	((430R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101011	((430R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101100	((430R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101101	((430R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101110	((430R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101111	((430R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110000	((430R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110001	((430R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110010	((430R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110011	((430R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110100	((430R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110101	((430R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110110	((430R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110111	((430R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111000	((430R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111001	((430R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111010	((430R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111011	((430R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111100	((430R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111101	((430R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111110	((430R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111111	((430R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.30: VinN1

Reference voltage	Macro adjustment value	VinN2 formula
VinN2	VRN2 5-0 = 000000	(420R / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000001	((420R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000010	((420R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000011	((420R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000100	((420R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000101	((420R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000110	((420R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000111	((420R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001000	((420R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001001	((420R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001010	((420R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001011	((420R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001100	((420R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001101	((420R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001110	((420R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001111	((420R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010000	((420R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010001	((420R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010010	((420R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010011	((420R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010100	((420R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010101	((420R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010110	((420R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010111	((420R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011000	((420R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011001	((420R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011010	((420R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011011	((420R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011100	((420R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011101	((420R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011110	((420R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011111	((420R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100000	((420R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100001	((420R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100010	((420R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100011	((420R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100100	((420R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100101	((420R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100110	((420R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100111	((420R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101000	((420R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101001	((420R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101010	((420R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101011	((420R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101100	((420R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101101	((420R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101110	((420R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101111	((420R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110000	((420R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110001	((420R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110010	((420R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110011	((420R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110100	((420R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110101	((420R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110110	((420R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110111	((420R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111000	((420R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111001	((420R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111010	((420R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111011	((420R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111100	((420R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111101	((420R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111110	((420R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111111	((420R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.31: VinN2

Reference voltage	Macro adjustment value	VinN14 formula
VinN14	VRN3 5-0 = 000000	(156R / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000001	((156R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000010	((156R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000011	((156R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000100	((156R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000101	((156R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000110	((156R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000111	((156R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001000	((156R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001001	((156R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001010	((156R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001011	((156R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001100	((156R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001101	((156R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001110	((156R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001111	((156R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010000	((156R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010001	((156R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010010	((156R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010011	((156R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010100	((156R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010101	((156R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010110	((156R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010111	((156R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011000	((156R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011001	((156R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011010	((156R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011011	((156R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011100	((156R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011101	((156R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011110	((156R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011111	((156R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100000	((156R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100001	((156R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100010	((156R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100011	((156R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100100	((156R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100101	((156R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100110	((156R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100111	((156R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101000	((156R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101001	((156R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101010	((156R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101011	((156R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101100	((156R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101101	((156R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101110	((156R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101111	((156R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110000	((156R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110001	((156R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110010	((156R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110011	((156R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110100	((156R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110101	((156R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110110	((156R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110111	((156R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111000	((156R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111001	((156R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111010	((156R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111011	((156R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111100	((156R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111101	((156R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111110	((156R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111111	((156R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.32: VinN14

Reference voltage	Macro adjustment value	VinN15 formula
VinN15	VRN4 5-0 = 000000	(146R / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000001	((146R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000010	((146R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000011	((146R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000100	((146R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000101	((146R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000110	((146R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000111	((146R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001000	((146R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001001	((146R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001010	((146R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001011	((146R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001100	((146R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001101	((146R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001110	((146R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001111	((146R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010000	((146R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010001	((146R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010010	((146R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010011	((146R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010100	((146R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010101	((146R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010110	((146R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010111	((146R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011000	((146R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011001	((146R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011010	((146R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011011	((146R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011100	((146R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011101	((146R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011110	((146R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011111	((146R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100000	((146R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100001	((146R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100010	((146R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100011	((146R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100100	((146R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100101	((146R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100110	((146R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100111	((146R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101000	((146R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101001	((146R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101010	((146R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101011	((146R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101100	((146R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101101	((146R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101110	((146R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101111	((146R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110000	((146R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110001	((146R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110010	((146R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110011	((146R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110100	((146R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110101	((146R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110110	((146R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110111	((146R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111000	((146R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111001	((146R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111010	((146R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111011	((146R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111100	((146R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111101	((146R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111110	((146R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111111	((146R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.33: VinN15

Reference voltage	Macro adjustment value	VinN16 formula
VinN16	VRN5 5-0 = 000000	(144R / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000001	((144R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000010	((144R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000011	((144R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000100	((144R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000101	((144R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000110	((144R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000111	((144R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001000	((144R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001001	((144R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001010	((144R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001011	((144R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001100	((144R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001101	((144R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001110	((144R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001111	((144R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010000	((144R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010001	((144R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010010	((144R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010011	((144R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010100	((144R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010101	((144R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010110	((144R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010111	((144R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011000	((144R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011001	((144R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011010	((144R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011011	((144R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011100	((144R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011101	((144R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011110	((144R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011111	((144R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100000	((144R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100001	((144R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100010	((144R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100011	((144R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100100	((144R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100101	((144R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100110	((144R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100111	((144R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101000	((144R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101001	((144R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101010	((144R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101011	((144R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101100	((144R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101101	((144R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101110	((144R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101111	((144R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110000	((144R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110001	((144R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110010	((144R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110011	((144R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110100	((144R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110101	((144R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110110	((144R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110111	((144R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111000	((144R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111001	((144R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111010	((144R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111011	((144R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111100	((144R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111101	((144R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111110	((144R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111111	VGSN

Table 5.34: VinN16

Reference voltage	Macro adjustment value	VinN5 formula
VinN5	PRN0 6-0 = 0000000	(350R / 450R) (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000001	((350R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000010	((350R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000011	((350R – 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000100	((350R – 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000101	((350R – 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000110	((350R – 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000111	((350R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001000	((350R – 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001001	((350R – 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001010	((350R – 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001011	((350R – 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001100	((350R – 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001101	((350R – 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001110	((350R – 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001111	((350R – 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010000	((350R – 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010001	((350R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010010	((350R – 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010011	((350R – 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010100	((350R – 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010101	((350R – 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010110	((350R – 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010111	((350R – 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011000	((350R – 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011001	((350R – 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011010	((350R – 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011011	((350R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011100	((350R – 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011101	((350R – 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011110	((350R – 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011111	((350R – 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100000	((350R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100001	((350R – 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100010	((350R – 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100011	((350R – 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100100	((350R – 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100101	((350R – 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100110	((350R – 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100111	((350R – 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101000	((350R – 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101001	((350R – 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101010	((350R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101011	((350R – 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101100	((350R – 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101101	((350R – 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101110	((350R – 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101111	((350R – 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110000	((350R – 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110001	((350R – 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110010	((350R – 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110011	((350R – 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110100	((350R – 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110101	((350R – 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110110	((350R – 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110111	((350R – 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111000	((350R – 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111001	((350R – 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111010	((350R – 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111011	((350R – 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111100	((350R – 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111101	((350R – 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111110	((350R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111111	((350R – 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000000	((350R – 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000001	((350R – 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000010	((350R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000011	((350R – 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000100	((350R – 136R) / 450R) * (VSNR - VGSN) + VGSN

	PRN0 6-0 = 1000101	((350R – 138R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000110	((350R – 140R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000111	((350R – 142R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001000	((350R – 144R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001001	((350R – 146R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001010	((350R – 148R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001011	((350R – 150R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001100	((350R - 152R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001101	((350R – 154R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001110	((350R – 156R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001111	((350R – 158R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010000	((350R – 160R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010001	((350R – 162R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010010	((350R – 164R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010011	((350R – 166R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010100	((350R – 168R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010101	((350R – 170R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010110	((350R – 172R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010111	((350R - 174R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1011000	inhibit
	PRN0 6-0 = 1011001	inhibit
	PRN0 6-0 = 1011010	inhibit
	PRN0 6-0 = 1011011	inhibit
	PRN0 6-0 = 1011100	inhibit
	PRN0 6-0 = 1011101	inhibit
	PRN0 6-0 = 1011110	inhibit
	PRN0 6-0 = 1011111	inhibit
	PRN0 6-0 = 1100000	inhibit
	PRN0 6-0 = 1100001	inhibit
	PRN0 6-0 = 1100010	inhibit
	PRN0 6-0 = 1100011	inhibit
	PRN0 6-0 = 1100100	inhibit
	PRN0 6-0 = 1100101	inhibit
	PRN0 6-0 = 1100110	inhibit
	PRN0 6-0 = 1100111	inhibit
	PRN0 6-0 = 1101000	inhibit
	PRN0 6-0 = 1101001	inhibit
	PRN0 6-0 = 1101010	inhibit
	PRN0 6-0 = 1101011	inhibit
	PRN0 6-0 = 1101100	inhibit
	PRN0 6-0 = 1101101	inhibit
	PRN0 6-0 = 1101110	inhibit
	PRN0 6-0 = 1101111	inhibit
	PRN0 6-0 = 1110000	inhibit
	PRN0 6-0 = 1110001	inhibit
	PRN0 6-0 = 1110010	inhibit
	PRN0 6-0 = 1110011	inhibit
	PRN0 6-0 = 1110100	inhibit
	PRN0 6-0 = 1110101	inhibit
	PRN0 6-0 = 1110110	inhibit
	PRN0 6-0 = 1110111	inhibit
	PRN0 6-0 = 1111000	inhibit
	PRN0 6-0 = 1111001	inhibit
	PRN0 6-0 = 1111010	inhibit
	PRN0 6-0 = 1111011	inhibit
	PRN0 6-0 = 1111100	inhibit
	PRN0 6-0 = 1111101	inhibit
	PRN0 6-0 = 1111110	inhibit
	PRN0 6-0 = 1111111	inhibit

Table 5.35: VinN5

Reference voltage	Macro adjustment value	VinN11 formula
VinN11	PRN1 6-0 = 0000000	(274R / 450R) (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000011	((274R – 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000100	((274R – 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000101	((274R – 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000110	((274R – 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000111	((274R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001000	((274R – 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001001	((274R – 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001010	((274R – 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001011	((274R – 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001100	((274R – 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001101	((274R – 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001110	((274R – 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001111	((274R – 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010000	((274R – 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010010	((274R – 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010011	((274R – 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010100	((274R – 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010101	((274R – 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010110	((274R – 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010111	((274R – 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011000	((274R – 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011001	((274R – 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011010	((274R – 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011100	((274R – 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011101	((274R – 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011110	((274R – 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011111	((274R – 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100001	((274R – 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100010	((274R – 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100011	((274R – 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100100	((274R – 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100101	((274R – 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100110	((274R – 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100111	((274R – 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101000	((274R – 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101001	((274R – 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101011	((274R – 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101100	((274R – 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101101	((274R – 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101110	((274R – 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101111	((274R – 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110000	((274R – 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110001	((274R – 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110010	((274R – 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110011	((274R – 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110100	((274R – 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110101	((274R – 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110110	((274R – 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110111	((274R – 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111000	((274R – 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111001	((274R – 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111010	((274R – 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111011	((274R – 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111100	((274R – 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111101	((274R – 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111111	((274R – 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000000	((274R – 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000001	((274R – 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000011	((274R – 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000100	((274R – 136R) / 450R) * (VSNR - VGSN) + VGSN

	PRN1 6-0 = 1000101	((274R – 138R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000110	((274R – 140R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000111	((274R – 142R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001000	((274R – 144R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001001	((274R – 146R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001010	((274R – 148R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001011	((274R – 150R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001100	((274R - 152R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001101	((274R – 154R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001110	((274R – 156R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001111	((274R – 158R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010000	((274R – 160R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010001	((274R – 162R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010010	((274R – 164R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010011	((274R – 166R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010100	((274R – 168R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010101	((274R – 170R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010110	((274R – 172R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010111	((274R - 174R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1011000	inhibit
	PRN1 6-0 = 1011001	inhibit
	PRN1 6-0 = 1011010	inhibit
	PRN1 6-0 = 1011011	inhibit
	PRN1 6-0 = 1011100	inhibit
	PRN1 6-0 = 1011101	inhibit
	PRN1 6-0 = 1011110	inhibit
	PRN1 6-0 = 1011111	inhibit
	PRN1 6-0 = 1100000	inhibit
	PRN1 6-0 = 1100001	inhibit
	PRN1 6-0 = 1100010	inhibit
	PRN1 6-0 = 1100011	inhibit
	PRN1 6-0 = 1100100	inhibit
	PRN1 6-0 = 1100101	inhibit
	PRN1 6-0 = 1100110	inhibit
	PRN1 6-0 = 1100111	inhibit
	PRN1 6-0 = 1101000	inhibit
	PRN1 6-0 = 1101001	inhibit
	PRN1 6-0 = 1101010	inhibit
	PRN1 6-0 = 1101011	inhibit
	PRN1 6-0 = 1101100	inhibit
	PRN1 6-0 = 1101101	inhibit
	PRN1 6-0 = 1101110	inhibit
	PRN1 6-0 = 1101111	inhibit
	PRN1 6-0 = 1110000	inhibit
	PRN1 6-0 = 1110001	inhibit
	PRN1 6-0 = 1110010	inhibit
	PRN1 6-0 = 1110011	inhibit
	PRN1 6-0 = 1110100	inhibit
	PRN1 6-0 = 1110101	inhibit
	PRN1 6-0 = 1110110	inhibit
	PRN1 6-0 = 1110111	inhibit
	PRN1 6-0 = 1111000	inhibit
	PRN1 6-0 = 1111001	inhibit
	PRN1 6-0 = 1111010	inhibit
	PRN1 6-0 = 1111011	inhibit
	PRN1 6-0 = 1111100	inhibit
	PRN1 6-0 = 1111101	inhibit
	PRN1 6-0 = 1111110	inhibit
	PRN1 6-0 = 1111111	inhibit

Table 5.36: VinN11

Reference voltage	Macro adjustment value	VinN3 formula
VinN3	PKN0 4-0 = 00000	(47R / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00001	((47R – 1R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00010	((47R – 2R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00011	((47R – 3R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00100	((47R – 4R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00101	((47R – 5R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00110	((47R – 6R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00111	((47R – 7R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01000	((47R – 8R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01001	((47R – 9R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01010	((47R - 10R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01011	((47R - 11R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01100	((47R - 12R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01101	((47R - 13R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01110	((47R - 14R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01111	((47R - 15R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10000	((47R - 16R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10001	((47R - 17R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10010	((47R - 18R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10011	((47R - 19R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10100	((47R - 20R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10101	((47R - 21R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10110	((47R - 22R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10111	((47R - 23R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11000	((47R - 24R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11001	((47R - 25R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11010	((47R - 26R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11011	((47R - 27R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11100	((47R - 28R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11101	((47R - 29R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11110	((47R - 30R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11111	((47R - 31R) / 48R) * (VinN2 - VinN5) + VinN5

Table 5.37: VinN3

Reference voltage	Macro adjustment value	VinN4 formula
VinN4	PKN1 4-0 = 00000	(32R / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00001	((32R - 1R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00010	((32R - 2R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00011	((32R - 3R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00100	((32R - 4R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00101	((32R - 5R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00110	((32R - 6R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00111	((32R - 7R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01000	((32R - 8R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01001	((32R - 9R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01010	((32R - 10R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01011	((32R - 11R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01100	((32R - 12R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01101	((32R - 13R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01110	((32R - 14R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01111	((32R - 15R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10000	((32R - 16R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10001	((32R - 17R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10010	((32R - 18R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10011	((32R - 19R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10100	((32R - 20R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10101	((32R - 21R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10110	((32R - 22R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10111	((32R - 23R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11000	((32R - 24R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11001	((32R - 25R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11010	((32R - 26R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11011	((32R - 27R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11100	((32R - 28R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11101	((32R - 29R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11110	((32R - 30R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11111	((32R - 31R) / 48R) * (VinN2 - VinN5) + VinN5

Table 5.38: VinN4

Reference voltage	Macro adjustment value	VinN6 formula
VinN6	PKN2 4-0 = 00000	(220R / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00001	((220R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00010	((220R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00011	((220R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00100	((220R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00101	((220R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00110	((220R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00111	((220R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01000	((220R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01001	((220R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01010	((220R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01011	((220R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01100	((220R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01101	((220R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01110	((220R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01111	((220R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10000	((220R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10001	((220R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10010	((220R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10011	((220R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10100	((220R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10101	((220R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10110	((220R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10111	((220R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11000	((220R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11001	((220R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11010	((220R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11011	((220R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11100	((220R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11101	((220R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11110	((220R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11111	((220R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.39: VinN6

Reference voltage	Macro adjustment value	VinN7 formula
VinN7	PKN3 4-0 = 00000	(193R / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00001	((193R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00010	((193R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00011	((193R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00100	((193R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00101	((193R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00110	((193R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00111	((193R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01000	((193R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01001	((193R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01010	((193R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01011	((193R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01100	((193R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01101	((193R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01110	((193R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01111	((193R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10000	((193R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10001	((193R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10010	((193R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10011	((193R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10100	((193R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10101	((193R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10110	((193R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10111	((193R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11000	((193R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11001	((193R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11010	((193R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11011	((193R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11100	((193R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11101	((193R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11110	((193R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11111	((193R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.40: VinN7

Reference voltage	Macro adjustment value	VinN8 formula
VinN8	PKN4 4-0 = 00000	(158R / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00001	((158R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00010	((158R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00011	((158R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00100	((158R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00101	((158R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00110	((158R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00111	((158R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01000	((158R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01001	((158R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01010	((158R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01011	((158R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01100	((158R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01101	((158R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01110	((158R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01111	((158R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10000	((158R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10001	((158R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10010	((158R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10011	((158R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10100	((158R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10101	((158R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10110	((158R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10111	((158R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11000	((158R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11001	((158R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11010	((158R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11011	((158R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11100	((158R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11101	((158R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11110	((158R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11111	((158R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.41: VinN8

Reference voltage	Macro adjustment value	VinN9 formula
VinN9	PKN5 4-0 = 00000	(123R / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00001	((123R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00010	((123R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00011	((123R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00100	((123R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00101	((123R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00110	((123R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00111	((123R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01000	((123R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01001	((123R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01010	((123R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01011	((123R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01100	((123R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01101	((123R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01110	((123R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01111	((123R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10000	((123R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10001	((123R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10010	((123R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10011	((123R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10100	((123R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10101	((123R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10110	((123R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10111	((123R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11000	((123R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11001	((123R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11010	((123R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11011	((123R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11100	((123R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11101	((123R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11110	((123R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11111	((123R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.42: VinN9

Reference voltage	Macro adjustment value	VinN10 formula
VinN10	PKN6 4-0 = 00000	(96R / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00001	((96R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00010	((96R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00011	((96R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00100	((96R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00101	((96R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00110	((96R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00111	((96R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01000	((96R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01001	((96R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01010	((96R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01011	((96R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01100	((96R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01101	((96R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01110	((96R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01111	((96R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10000	((96R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10001	((96R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10010	((96R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10011	((96R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10100	((96R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10101	((96R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10110	((96R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10111	((96R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11000	((96R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11001	((96R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11010	((96R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11011	((96R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11100	((96R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11101	((96R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11110	((96R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11111	((96R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.43: VinN10

Reference voltage	Macro adjustment value	VinN12 formula
VinN12	PKN7 4-0 = 00000	(47R / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00001	((47R - 1R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00010	((47R - 2R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00011	((47R - 3R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00100	((47R - 4R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00101	((47R - 5R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00110	((47R - 6R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00111	((47R - 7R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01000	((47R - 8R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01001	((47R - 9R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01010	((47R - 10R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01011	((47R - 11R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01100	((47R - 12R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01101	((47R - 13R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01110	((47R - 14R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01111	((47R - 15R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10000	((47R - 16R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10001	((47R - 17R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10010	((47R - 18R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10011	((47R - 19R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10100	((47R - 20R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10101	((47R - 21R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10110	((47R - 22R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10111	((47R - 23R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11000	((47R - 24R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11001	((47R - 25R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11010	((47R - 26R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11011	((47R - 27R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11100	((47R - 28R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11101	((47R - 29R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11110	((47R - 30R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11111	((47R - 31R) / 48R) * (VinN11 - VinN14) + VinN14

Table 5.44: VinN12

Reference voltage	Macro adjustment value	VinN13 formula
VinN13	PKN8 4-0 = 00000	(32R / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00001	((32R - 1R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00010	((32R - 2R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00011	((32R - 3R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00100	((32R - 4R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00101	((32R - 5R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00110	((32R - 6R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00111	((32R - 7R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01000	((32R - 8R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01001	((32R - 9R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01010	((32R - 10R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01011	((32R - 11R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01100	((32R - 12R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01101	((32R - 13R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01110	((32R - 14R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01111	((32R - 15R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10000	((32R - 16R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10001	((32R - 17R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10010	((32R - 18R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10011	((32R - 19R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10100	((32R - 20R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10101	((32R - 21R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10110	((32R - 22R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10111	((32R - 23R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11000	((32R - 24R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11001	((32R - 25R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11010	((32R - 26R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11011	((32R - 27R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11100	((32R - 28R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11101	((32R - 29R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11110	((32R - 30R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11111	((32R - 31R) / 48R) * (VinN11 - VinN14) + VinN14

Table 5.45: VinN13

Grayscale voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	VinP3 - (VinP3 - VinP4)*(1R/4R)
V5	VinP3 - (VinP3 - VinP4)*(2R/4R)
V6	VinP3 - (VinP3 - VinP4)*(3R/4R)
V7	VinP4
V8	VinP4 - (VinP4 - VinP5)*(1R/6R)
V9	VinP4 - (VinP4 - VinP5)*(2R/6R)
V10	VinP4 - (VinP4 - VinP5)*(3R/6R)
V11	VinP4 - (VinP4 - VinP5)*(4R/6R)
V12	VinP4 - (VinP4 - VinP5)*(5R/6R)
V13	VinP5
V14	VinP5 - (VinP5 - VinP6)*(1R/6R)
V15	VinP5 - (VinP5 - VinP6)*(2R/6R)
V16	VinP5 - (VinP5 - VinP6)*(3R/6R)
V17	VinP5 - (VinP5 - VinP6)*(4R/6R)
V18	VinP5 - (VinP5 - VinP6)*(5R/6R)
V19	VinP6
V20	VinP6 - (VinP6 - VinP7)*(1R/6R)
V21	VinP6 - (VinP6 - VinP7)*(2R/6R)
V22	VinP6 - (VinP6 - VinP7)*(3R/6R)
V23	VinP6 - (VinP6 - VinP7)*(4R/6R)
V24	VinP6 - (VinP6 - VinP7)*(5R/6R)
V25	VinP7
V26	VinP7 - (VinP7 - VinP8)*(1R/7.5R)
V27	VinP7 - (VinP7 - VinP8)*(2R/7.5R)
V28	VinP7 - (VinP7 - VinP8)*(3R/7.5R)
V29	VinP7 - (VinP7 - VinP8)*(4R/7.5R)
V30	VinP7 - (VinP7 - VinP8)*(5R/7.5R)
V31	VinP7 - (VinP7 - VinP8)*(6R/7.5R)
V32	VinP8
V33	VinP8 - (VinP8 - VinP9)*(1R/6R)
V34	VinP8 - (VinP8 - VinP9)*(2R/6R)
V35	VinP8 - (VinP8 - VinP9)*(3R/6R)
V36	VinP8 - (VinP8 - VinP9)*(4R/6R)
V37	VinP8 - (VinP8 - VinP9)*(5R/6R)
V38	VinP9
V39	VinP9 - (VinP9 - VinP10)*(1R/6R)
V40	VinP9 - (VinP9 - VinP10)*(2R/6R)
V41	VinP9 - (VinP9 - VinP10)*(3R/6R)
V42	VinP9 - (VinP9 - VinP10)*(4R/6R)
V43	VinP9 - (VinP9 - VinP10)*(5R/6R)
V44	VinP10
V45	VinP10 - (VinP10 - VinP11)*(1R/6R)
V46	VinP10 - (VinP10 - VinP11)*(2R/6R)
V47	VinP10 - (VinP10 - VinP11)*(3R/6R)
V48	VinP10 - (VinP10 - VinP11)*(4R/6R)
V49	VinP10 - (VinP10 - VinP11)*(5R/6R)
V50	VinP11
V51	VinP11 - (VinP11 - VinP12)*(1R/6R)
V52	VinP11 - (VinP11- VinP12)*(2R/6R)
V53	VinP11 - (VinP11 - VinP12)*(3R/6R)
V54	VinP11 - (VinP11 - VinP12)*(4R/6R)
V55	VinP11 - (VinP11- VinP12)*(5R/6R)
V56	VinP12
V57	VinP12 - (VinP12 – VinP13)*(1R/4R)
V58	VinP12 - (VinP12 – VinP13)*(2R/4R)
V59	VinP12 - (VinP12 – VinP13)*(3R/4R)
V60	VinP13
V61	VinP14
V62	VinP15
V63	VinP16

Table 5.46: Voltage calculation formula of 64-grayscale voltage (positive polarity)

Grayscale voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	VinN3 - (VinN3 - VinN4)*(1R/4R)
V5	VinN3 - (VinN3 - VinN4)*(2R/4R)
V6	VinN3 - (VinN3 - VinN4)*(3R/4R)
V7	VinN4
V8	VinN4 - (VinN4 - VinN5)*(1R/6R)
V9	VinN4 - (VinN4 - VinN5)*(2R/6R)
V10	VinN4 - (VinN4 - VinN5)*(3R/6R)
V11	VinN4 - (VinN4 - VinN5)*(4R/6R)
V12	VinN4 - (VinN4 - VinN5)*(5R/6R)
V13	VinN5
V14	VinN5 - (VinN5 - VinN6)*(1R/6R)
V15	VinN5 - (VinN5 - VinN6)*(2R/6R)
V16	VinN5 - (VinN5 - VinN6)*(3R/6R)
V17	VinN5 - (VinN5 - VinN6)*(4R/6R)
V18	VinN5 - (VinN5 - VinN6)*(5R/6R)
V19	VinN6
V20	VinN6 - (VinN6 - VinN7)*(1R/6R)
V21	VinN6 - (VinN6 - VinN7)*(2R/6R)
V22	VinN6 - (VinN6 - VinN7)*(3R/6R)
V23	VinN6 - (VinN6 - VinN7)*(4R/6R)
V24	VinN6 - (VinN6 - VinN7)*(5R/6R)
V25	VinN7
V26	VinN7 - (VinN7 - VinN8)*(1R/7.5R)
V27	VinN7 - (VinN7 - VinN8)*(2R/7.5R)
V28	VinN7 - (VinN7 - VinN8)*(3R/7.5R)
V29	VinN7 - (VinN7 - VinN8)*(4R/7.5R)
V30	VinN7 - (VinN7 - VinN8)*(5R/7.5R)
V31	VinN7 - (VinN7 - VinN8)*(6R/7.5R)
V32	VinN8
V33	VinN8 - (VinN8 - VinN9)*(1R/6R)
V34	VinN8 - (VinN8 - VinN9)*(2R/6R)
V35	VinN8 - (VinN8 - VinN9)*(3R/6R)
V36	VinN8 - (VinN8 - VinN9)*(4R/6R)
V37	VinN8 - (VinN8 - VinN9)*(5R/6R)
V38	VinN9
V39	VinN9 - (VinN9 - VinN10)*(1R/6R)
V40	VinN9 - (VinN9 - VinN10)*(2R/6R)
V41	VinN9 - (VinN9 - VinN10)*(3R/6R)
V42	VinN9 - (VinN9 - VinN10)*(4R/6R)
V43	VinN9 - (VinN9 - VinN10)*(5R/6R)
V44	VinN10
V45	VinN10 - (VinN10 - VinN11)*(1R/6R)
V46	VinN10 - (VinN10 - VinN11)*(2R/6R)
V47	VinN10 - (VinN10 - VinN11)*(3R/6R)
V48	VinN10 - (VinN10 - VinN11)*(4R/6R)
V49	VinN10 - (VinN10 - VinN11)*(5R/6R)
V50	VinN11
V51	VinN11 - (VinN11 - VinN12)*(1R/6R)
V52	VinN11 - (VinN11- VinN12)*(2R/6R)
V53	VinN11 - (VinN11 - VinN12)*(3R/6R)
V54	VinN11 - (VinN11 - VinN12)*(4R/6R)
V55	VinN11 - (VinN11- VinN12)*(5R/6R)
V56	VinN12
V57	VinN12 - (VinN12 – VinN13)*(1R/4R)
V58	VinN12 - (VinN12 – VinN13)*(2R/4R)
V59	VinN12 - (VinN12 – VinN13)*(3R/4R)
V60	VinN13
V61	VinN14
V62	VinN15
V63	VinN16

Table 5.47: Voltage calculation formula of 64-grayscale voltage (negative polarity)

Grayscale voltage	Formula
VV0	V0
VV1	V0 - (V0 - V1)*(4R/16R)
VV2	V0 - (V0 - V1)*(8R/16R)
VV3	V0 - (V0 - V1)*(12R/16R)
VV4	V1
VV5	V1 - (V1 - V2)*(4R/16R)
VV6	V1 - (V1 - V2)*(8R/16R)
VV7	V1 - (V1 - V2)*(12R/16R)
VV8	V2
VV9	V2 - (V2 - V3)*(4R/16R)
VV10	V2 - (V2 - V3)*(8R/16R)
VV11	V2 - (V2 - V3)*(12R/16R)
VV12	V3
VV13	V3 - (V3 - V4)*(2R/8R)
VV14	V3 - (V3 - V4)*(4R/8R)
VV15	V3 - (V3 - V4)*(6R/8R)
VV16	V4
VV17	V4 - (V4 - V5)*(2R/8R)
VV18	V4 - (V4 - V5)*(4R/8R)
VV19	V4 - (V4 - V5)*(6R/8R)
VV20	V5
VV21	V5 - (V5 - V6)*(2R/8R)
VV22	V5 - (V5 - V6)*(4R/8R)
VV23	V5 - (V5 - V6)*(6R/8R)
VV24	V6
VV25	V6 - (V6 - V7)*(2R/8R)
VV26	V6 - (V6 - V7)*(4R/8R)
VV27	V6 - (V6 - V7)*(6R/8R)
VV28	V7
VV29	V7 - (V7 - V8)*(1.6R/6.4R)
VV30	V7 - (V7 - V8)*(3.2R/6.4R)
VV31	V7 - (V7 - V8)*(4.8R/6.4R)
VV32	V8
VV33	V8 - (V8 - V9)*(1.6R/6.4R)
VV34	V8 - (V8 - V9)*(3.2R/6.4R)
VV35	V8 - (V8 - V9)*(4.8R/6.4R)
VV36	V9
VV37	V9 - (V9 - V10)*(1.6R/6.4R)
VV38	V9 - (V9 - V10)*(3.2R/6.4R)
VV39	V9 - (V9 - V10)*(4.8R/6.4R)
VV40	V10
VV41	V10 - (V10 - V11)*(1.6R/6.4R)
VV42	V10 - (V10 - V11)*(3.2R/6.4R)
VV43	V10 - (V10 - V11)*(4.8R/6.4R)

Grayscale voltage	Formula
VV44	V11
VV45	V11 - (V11 - V12)*(1.6R/6.4R)
VV46	V11 - (V11 - V12)*(3.2R/6.4R)
VV47	V11 - (V11 - V12)*(4.8R/6.4R)
VV48	V12
VV49	V12 - (V12 - V13)*(1.6R/6.4R)
VV50	V12 - (V12 - V13)*(3.2R/6.4R)
VV51	V12 - (V12 - V13)*(4.8R/6.4R)
VV52	V13
VV53	V13 - (V13 - V14)*(1.6R/6.4R)
VV54	V13 - (V13 - V14)*(3.2R/6.4R)
VV55	V13 - (V13 - V14)*(4.8R/6.4R)
VV56	V14
VV57	V14 - (V14 - V15)*(1.6R/6.4R)
VV58	V14 - (V14 - V15)*(3.2R/6.4R)
VV59	V14 - (V14 - V15)*(4.8R/6.4R)
VV60	V15
VV61	V15 - (V15 - V16)*(1.6R/6.4R)
VV62	V15 - (V15 - V16)*(3.2R/6.4R)
VV63	V15 - (V15 - V16)*(4.8R/6.4R)
VV64	V16
VV65	V16 - (V16 - V17)*(1.6R/6.4R)
VV66	V16 - (V16 - V17)*(3.2R/6.4R)
VV67	V16 - (V16 - V17)*(4.8R/6.4R)
VV68	V17
VV69	V17 - (V17 - V18)*(1.6R/6.4R)
VV70	V17 - (V17 - V18)*(3.2R/6.4R)
VV71	V17 - (V17 - V18)*(4.8R/6.4R)
VV72	V18
VV73	V18 - (V18 - V19)*(1.6R/6.4R)
VV74	V18 - (V18 - V19)*(3.2R/6.4R)
VV75	V18 - (V18 - V19)*(4.8R/6.4R)
VV76	V19
VV77	V19 - (V19 - V20)*(1.6R/6.4R)
VV78	V19 - (V19 - V20)*(3.2R/6.4R)
VV79	V19 - (V19 - V20)*(4.8R/6.4R)
VV80	V20
VV81	V20 - (V20 - V21)*(1.6R/6.4R)
VV82	V20 - (V20 - V21)*(3.2R/6.4R)
VV83	V20 - (V20 - V21)*(4.8R/6.4R)
VV84	V21
VV85	V21 - (V21 - V22)*(1.6R/6.4R)
VV86	V21 - (V21 - V22)*(3.2R/6.4R)
VV87	V21 - (V21 - V22)*(4.8R/6.4R)

Grayscale voltage	Formula
VV88	V22
VV89	V22 - (V22 - V23)*(1.6R/6.4R)
VV90	V22 - (V22 - V23)*(3.2R/6.4R)
VV91	V22 - (V22 - V23)*(4.8R/6.4R)
VV92	V23
VV93	V23 - (V23 - V24)*(1.6R/6.4R)
VV94	V23 - (V23 - V24)*(3.2R/6.4R)
VV95	V23 - (V23 - V24)*(4.8R/6.4R)
VV96	V24
VV97	V24 - (V24 - V25)*(1.6R/6.4R)
VV98	V24 - (V24 - V25)*(3.2R/6.4R)
VV99	V24 - (V24 - V25)*(4.8R/6.4R)
VV100	V25
VV101	V25 - (V25 - V26)*(1.6R/6.4R)
VV102	V25 - (V25 - V26)*(3.2R/6.4R)
VV103	V25 - (V25 - V26)*(4.8R/6.4R)
VV104	V26
VV105	V26 - (V26 - V27)*(1.6R/6.4R)
VV106	V26 - (V26 - V27)*(3.2R/6.4R)
VV107	V26 - (V26 - V27)*(4.8R/6.4R)
VV108	V27
VV109	V27 - (V27 - V28)*(1.6R/6.4R)
VV110	V27 - (V27 - V28)*(3.2R/6.4R)
VV111	V27 - (V27 - V28)*(4.8R/6.4R)
VV112	V28
VV113	V28 - (V28 - V29)*(1.6R/6.4R)
VV114	V28 - (V28 - V29)*(3.2R/6.4R)
VV115	V28 - (V28 - V29)*(4.8R/6.4R)
VV116	V29
VV117	V29 - (V29 - V30)*(1.6R/6.4R)
VV118	V29 - (V29 - V30)*(3.2R/6.4R)
VV119	V29 - (V29 - V30)*(4.8R/6.4R)
VV120	V30
VV121	V30 - (V30 - V31)*(1.6R/6.4R)
VV122	V30 - (V30 - V31)*(3.2R/6.4R)
VV123	V30 - (V30 - V31)*(4.8R/6.4R)
VV124	V31
VV125	V31 - (V31 - V32)*(1.6R/11.2R)
VV126	V31 - (V31 - V32)*(3.2R/11.2R)
VV127	V31 - (V31 - V32)*(4.8R/11.2R)
VV128	V31 - (V31 - V32)*(6.4R/11.2R)
VV129	V31 - (V31 - V32)*(8R/11.2R)
VV130	V31 - (V31 - V32)*(9.6R/11.2R)
VV131	V32

Grayscale voltage	Formula
VV132	V32 - (V32 - V33)*(1.6R/6.4R)
VV133	V32 - (V32 - V33)*(3.2R/6.4R)
VV134	V32 - (V32 - V33)*(4.8R/6.4R)
VV135	V33
VV136	V33 - (V33 - V34)*(1.6R/6.4R)
VV137	V33 - (V33 - V34)*(3.2R/6.4R)
VV138	V33 - (V33 - V34)*(4.8R/6.4R)
VV139	V34
VV140	V34 - (V34 - V35)*(1.6R/6.4R)
VV141	V34 - (V34 - V35)*(3.2R/6.4R)
VV142	V34 - (V34 - V35)*(4.8R/6.4R)
VV143	V35
VV144	V35 - (V35 - V36)*(1.6R/6.4R)
VV145	V35 - (V35 - V36)*(3.2R/6.4R)
VV146	V35 - (V35 - V36)*(4.8R/6.4R)
VV147	V36
VV148	V36 - (V36 - V37)*(1.6R/6.4R)
VV149	V36 - (V36 - V37)*(3.2R/6.4R)
VV150	V36 - (V36 - V37)*(4.8R/6.4R)
VV151	V37
VV152	V37 - (V37 - V38)*(1.6R/6.4R)
VV153	V37 - (V37 - V38)*(3.2R/6.4R)
VV154	V37 - (V37 - V38)*(4.8R/6.4R)
VV155	V38
VV156	V38 - (V38 - V39)*(1.6R/6.4R)
VV157	V38 - (V38 - V39)*(3.2R/6.4R)
VV158	V38 - (V38 - V39)*(4.8R/6.4R)
VV159	V39
VV160	V39 - (V39 - V40)*(1.6R/6.4R)
VV161	V39 - (V39 - V40)*(3.2R/6.4R)
VV162	V39 - (V39 - V40)*(4.8R/6.4R)
VV163	V40
VV164	V40 - (V40 - V41)*(1.6R/6.4R)
VV165	V40 - (V40 - V41)*(3.2R/6.4R)
VV166	V40 - (V40 - V41)*(4.8R/6.4R)
VV167	V41
VV168	V41 - (V41 - V42)*(1.6R/6.4R)
VV169	V41 - (V41 - V42)*(3.2R/6.4R)
VV170	V41 - (V41 - V42)*(4.8R/6.4R)
VV171	V42
VV172	V42 - (V42 - V43)*(1.6R/6.4R)
VV173	V42 - (V42 - V43)*(3.2R/6.4R)
VV174	V42 - (V42 - V43)*(4.8R/6.4R)
VV175	V43

Grayscale voltage	Formula
VV176	V43 - (V43 - V44)*(1.6R/6.4R)
VV177	V43 - (V43 - V44)*(3.2R/6.4R)
VV178	V43 - (V43 - V44)*(4.8R/6.4R)
VV179	V44
VV180	V44 - (V44 - V45)*(1.6R/6.4R)
VV181	V44 - (V44 - V45)*(3.2R/6.4R)
VV182	V44 - (V44 - V45)*(4.8R/6.4R)
VV183	V45
VV184	V45 - (V45 - V46)*(1.6R/6.4R)
VV185	V45 - (V45 - V46)*(3.2R/6.4R)
VV186	V45 - (V45 - V46)*(4.8R/6.4R)
VV187	V46
VV188	V46 - (V46 - V47)*(1.6R/6.4R)
VV189	V46 - (V46 - V47)*(3.2R/6.4R)
VV190	V46 - (V46 - V47)*(4.8R/6.4R)
VV191	V47
VV192	V47 - (V47 - V48)*(1.6R/6.4R)
VV193	V47 - (V47 - V48)*(3.2R/6.4R)
VV194	V47 - (V47 - V48)*(4.8R/6.4R)
VV195	V48
VV196	V48 - (V48 - V49)*(1.6R/6.4R)
VV197	V48 - (V48 - V49)*(3.2R/6.4R)
VV198	V48 - (V48 - V49)*(4.8R/6.4R)
VV199	V49
VV200	V49 - (V49 - V50)*(1.6R/6.4R)
VV201	V49 - (V49 - V50)*(3.2R/6.4R)
VV202	V49 - (V49 - V50)*(4.8R/6.4R)
VV203	V50
VV204	V50 - (V50 - V51)*(1.6R/6.4R)
VV205	V50 - (V50 - V51)*(3.2R/6.4R)
VV206	V50 - (V50 - V51)*(4.8R/6.4R)
VV207	V51
VV208	V51 - (V51 - V52)*(1.6R/6.4R)
VV209	V51 - (V51 - V52)*(3.2R/6.4R)
VV210	V51 - (V51 - V52)*(4.8R/6.4R)
VV211	V52
VV212	V52 - (V52 - V53)*(1.6R/6.4R)
VV213	V52 - (V52 - V53)*(3.2R/6.4R)
VV214	V52 - (V52 - V53)*(4.8R/6.4R)
VV215	V53

Grayscale voltage	Formula
VV216	V53 - (V53 - V54)*(1.6R/6.4R)
VV217	V53 - (V53 - V54)*(3.2R/6.4R)
VV218	V53 - (V53 - V54)*(4.8R/6.4R)
VV219	V54
VV220	V54 - (V54 - V55)*(1.6R/6.4R)
VV221	V54 - (V54 - V55)*(3.2R/6.4R)
VV222	V54 - (V54 - V55)*(4.8R/6.4R)
VV223	V55
VV224	V55 - (V55 - V56)*(1.6R/6.4R)
VV225	V55 - (V55 - V56)*(3.2R/6.4R)
VV226	V55 - (V55 - V56)*(4.8R/6.4R)
VV227	V56
VV228	V56 - (V56 - V57)*(2R/8R)
VV229	V56 - (V56 - V57)*(4R/8R)
VV230	V56 - (V56 - V57)*(6R/8R)
VV231	V57
VV232	V57 - (V57 - V58)*(2R/8R)
VV233	V57 - (V57 - V58)*(4R/8R)
VV234	V57 - (V57 - V58)*(6R/8R)
VV235	V58
VV236	V58 - (V58 - V59)*(2R/8R)
VV237	V58 - (V58 - V59)*(4R/8R)
VV238	V58 - (V58 - V59)*(6R/8R)
VV239	V59
VV240	V59 - (V59 - V60)*(2R/8R)
VV241	V59 - (V59 - V60)*(4R/8R)
VV242	V59 - (V59 - V60)*(6R/8R)
VV243	V60
VV244	V60 - (V60 - V61)*(4R/16R)
VV245	V60 - (V60 - V61)*(8R/16R)
VV246	V60 - (V60 - V61)*(12R/16R)
VV247	V61
VV248	V61 - (V61 - V62)*(4R/16R)
VV249	V61 - (V61 - V62)*(8R/16R)
VV250	V61 - (V61 - V62)*(12R/16R)
VV251	V62
VV252	V62 - (V62 - V63)*(4R/16R)
VV253	V62 - (V62 - V63)*(8R/16R)
VV254	V62 - (V62 - V63)*(12R/16R)
VV255	V63

Table 5.48: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

5.12 Characteristics of I/O

5.12.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE	Low	Low	Low
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low

Table 5.49: Characteristics of output or bi-directional (I/O) pins

5.12.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Setion.5.18	Input valid	Input valid	Input valid	Setion.5.18
CSX	Input valid	Input valid	Input valid	Input valid	Input valid
DCX	Input valid	Input valid	Input valid	Input valid	Input valid
WRX_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
RDX	Input valid	Input valid	Input valid	Input valid	Input valid
DB23 to DB0 SDI	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
PCLK	Input valid	Input valid	Input valid	Input valid	Input valid
DE	Input valid	Input valid	Input valid	Input valid	Input valid
OSC, BS3, BS2, BS1, BS0,	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2-0	Low	Low	Low	Low	Low

Table 5.50: Characteristics of input pins

5.13 Sleep Out –command and self-diagnostic functions of the display module

5.13.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).
The flow chart for this internal function is following:

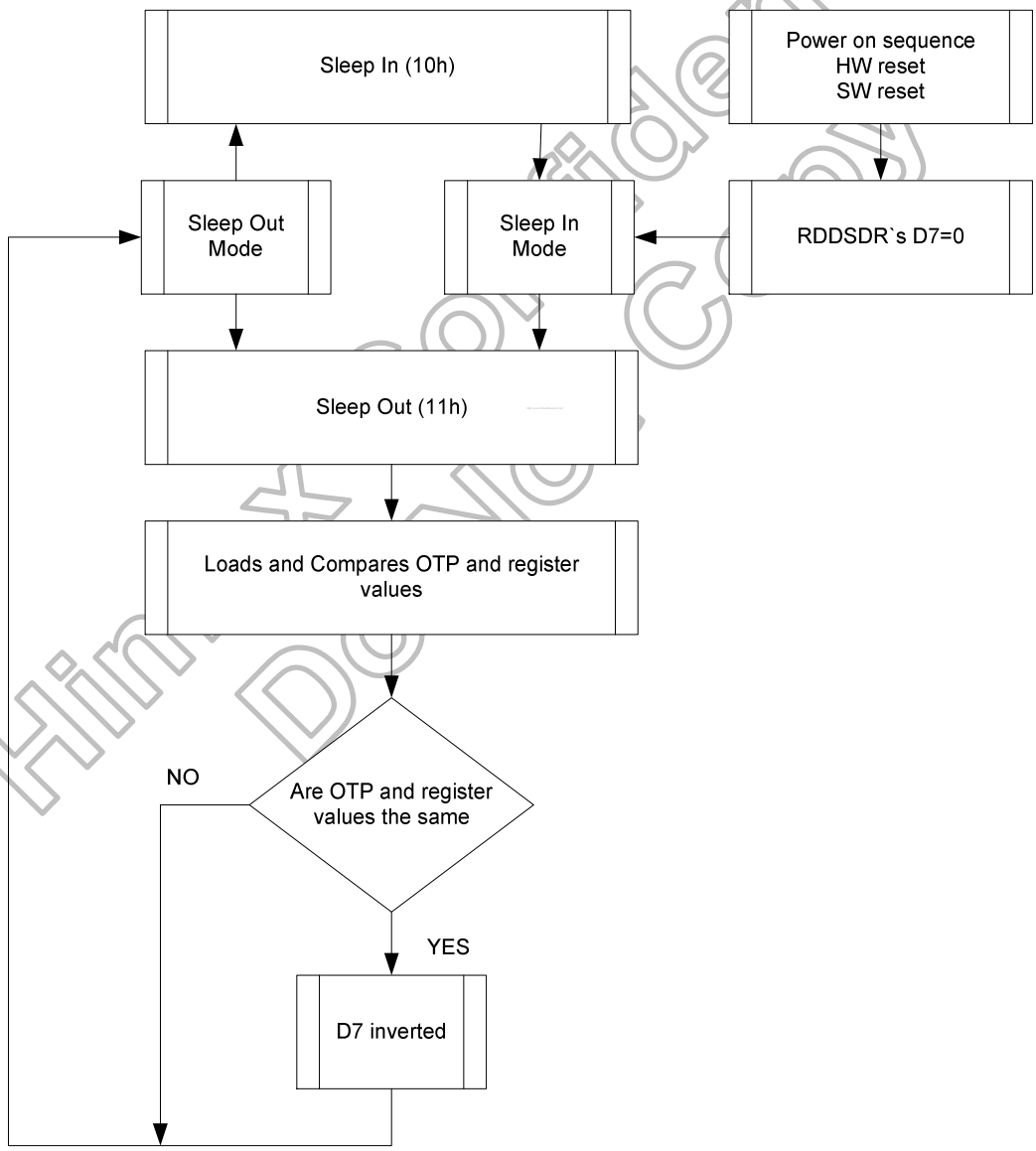
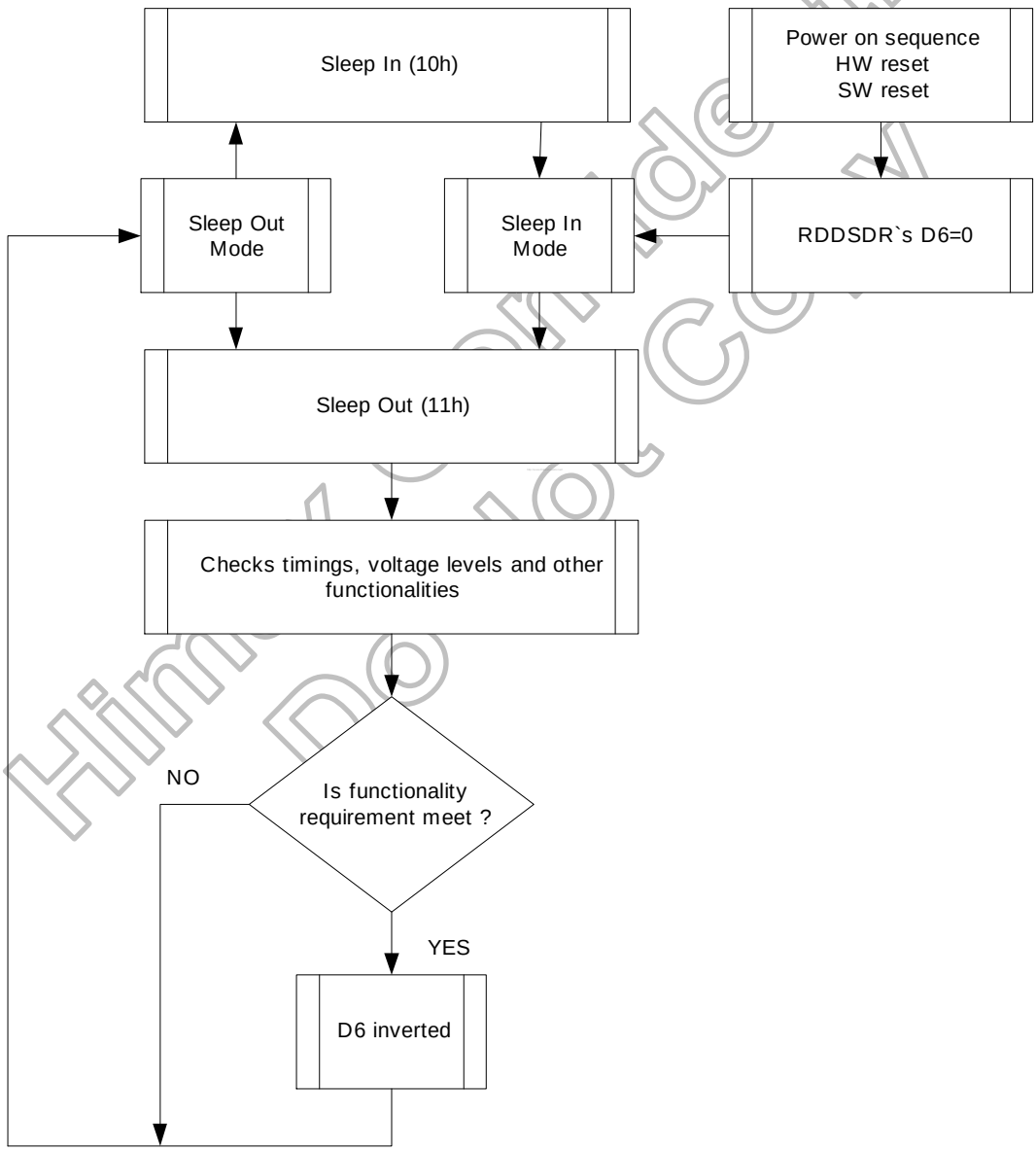


Figure 5.33: Sleep out flow chart–command and self-diagnostic functions

5.13.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.
The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In–mode toSleep Out -mode, before there is possible to check if Customer’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.34: Sleep out flow chart internal function detection

5.14 Power on/off sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.16.1 and 5.16.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.14.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

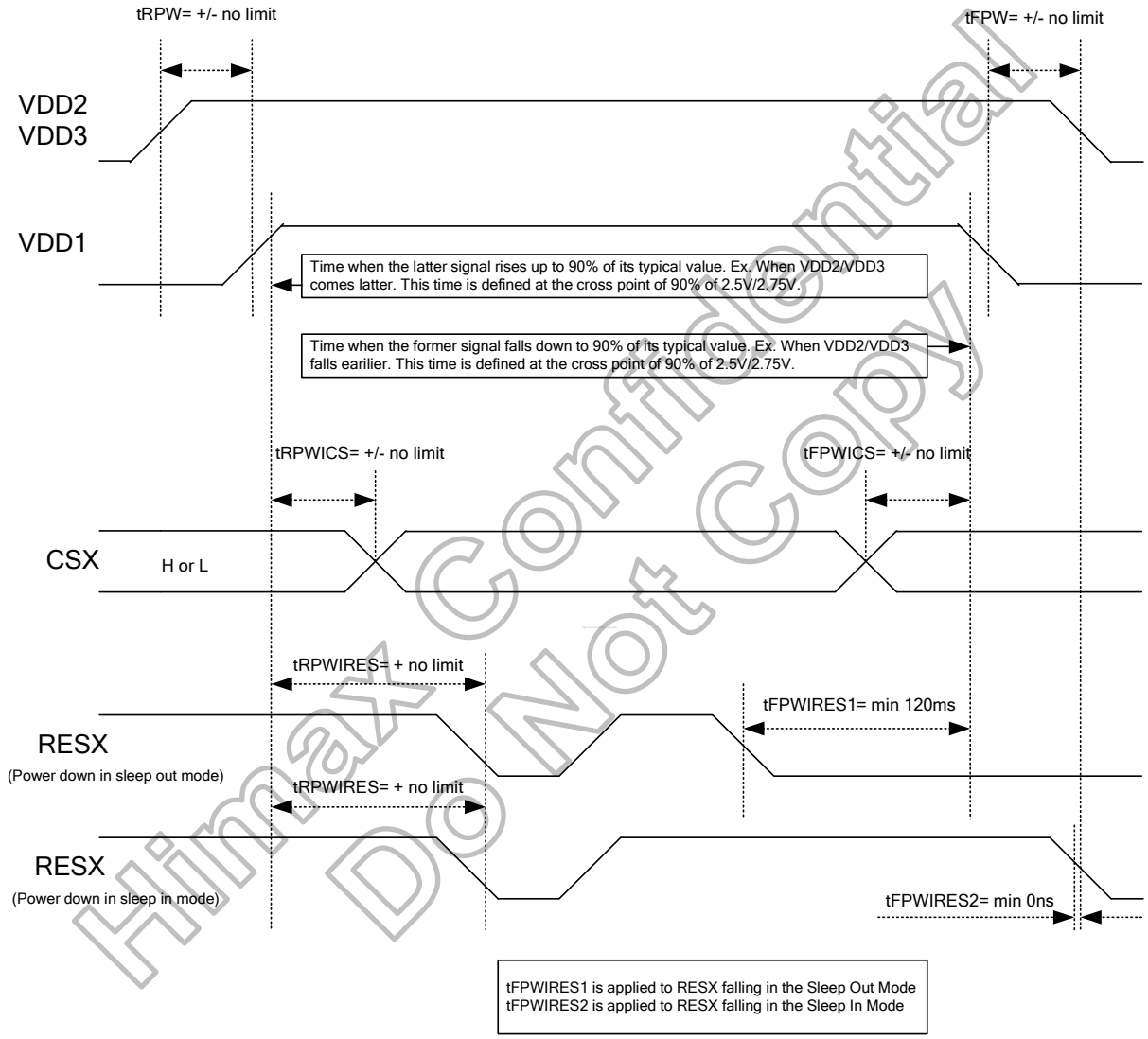


Figure 5.35: Case 1: RESX line is held high or unstable by host at power on

5.14.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.

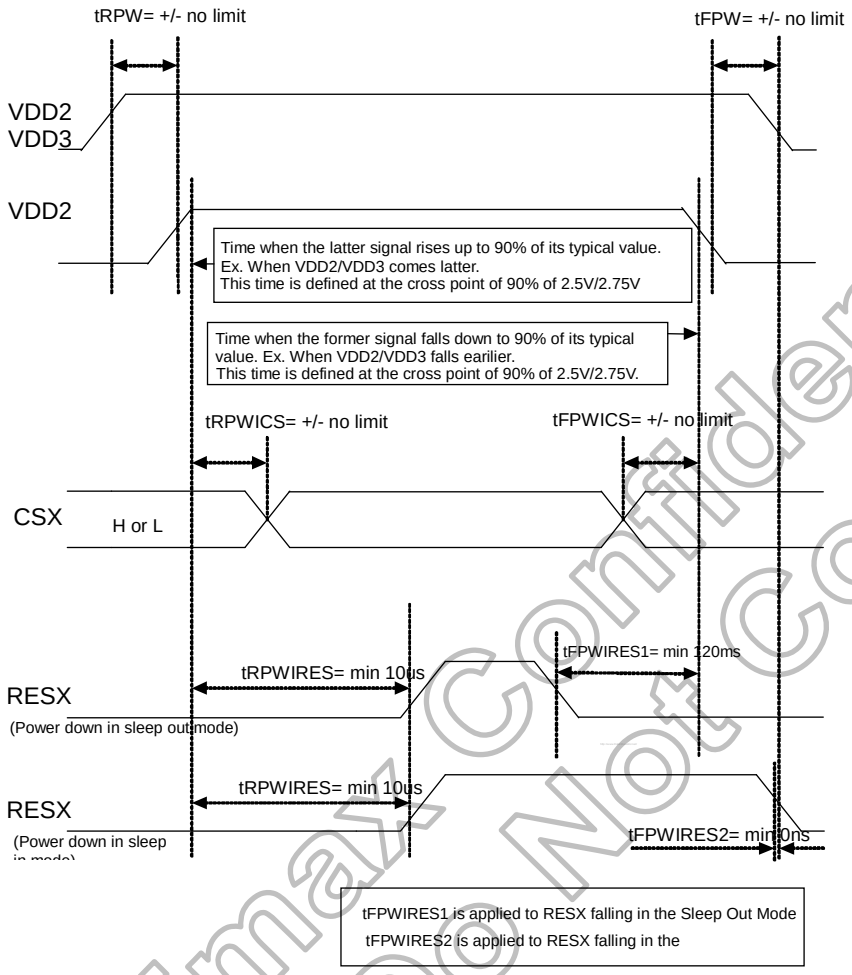
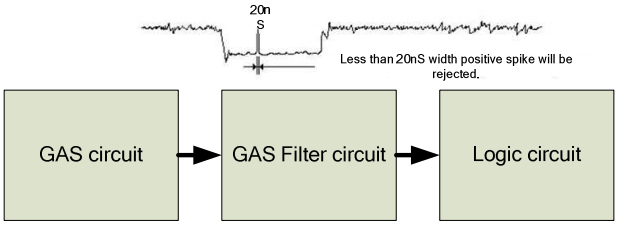


Figure 5.36: Case 2: RESX line is held low by host at power on

5.15 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

Note: HX8392-A is support the noise reject filter (20ns) to reject spike or noise.



5.16 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

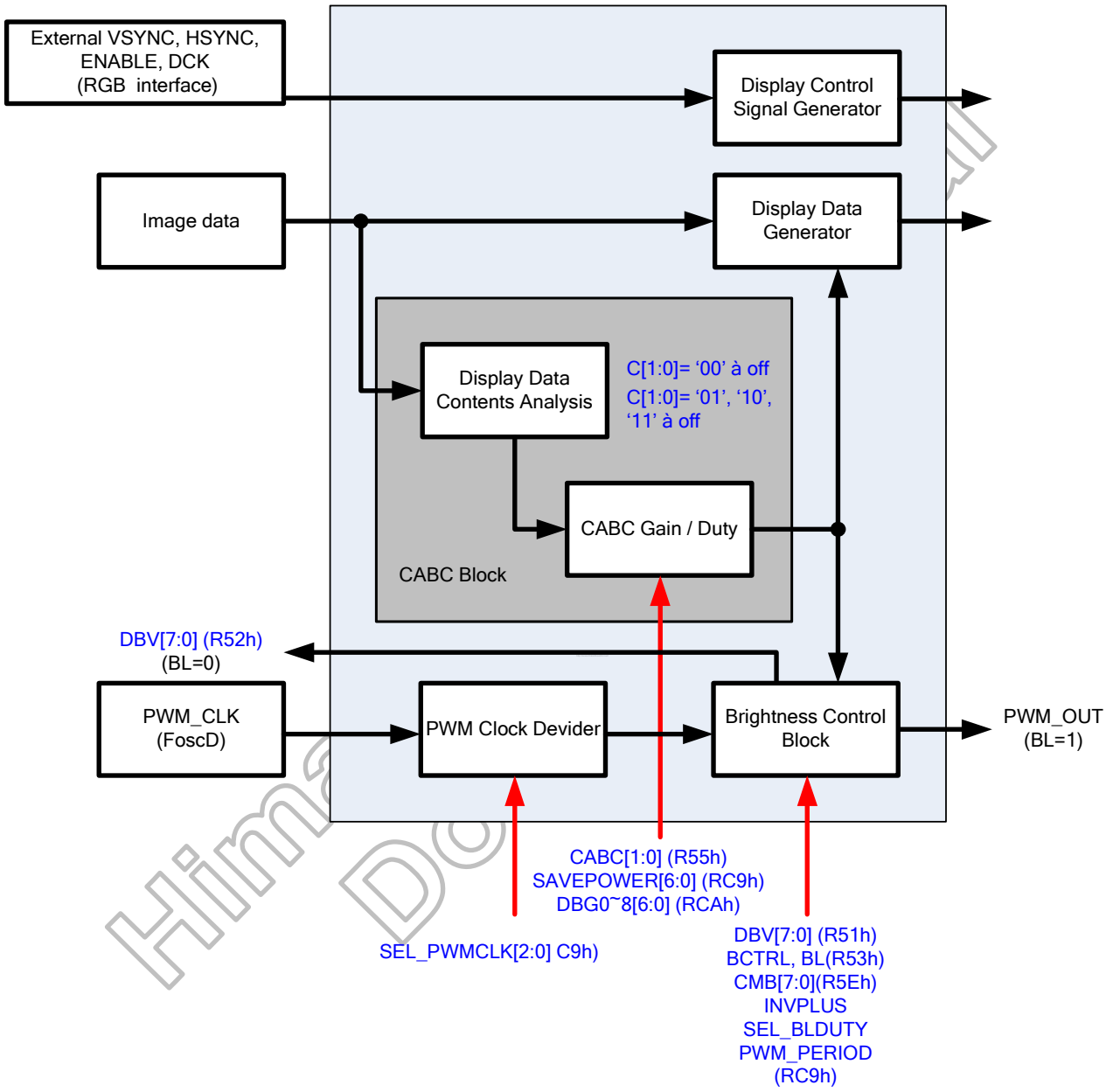
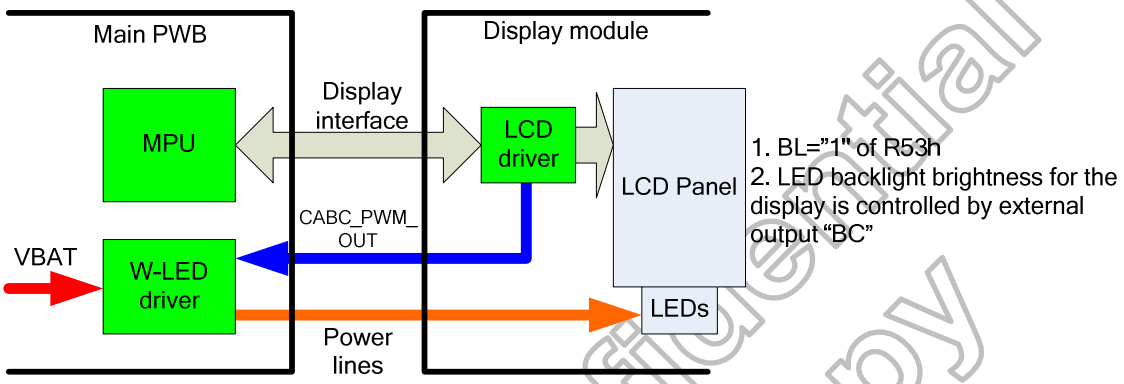


Figure 5.37: CABC block diagram

5.16.1 Module architectures

HX8392-A can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



- Architecture II

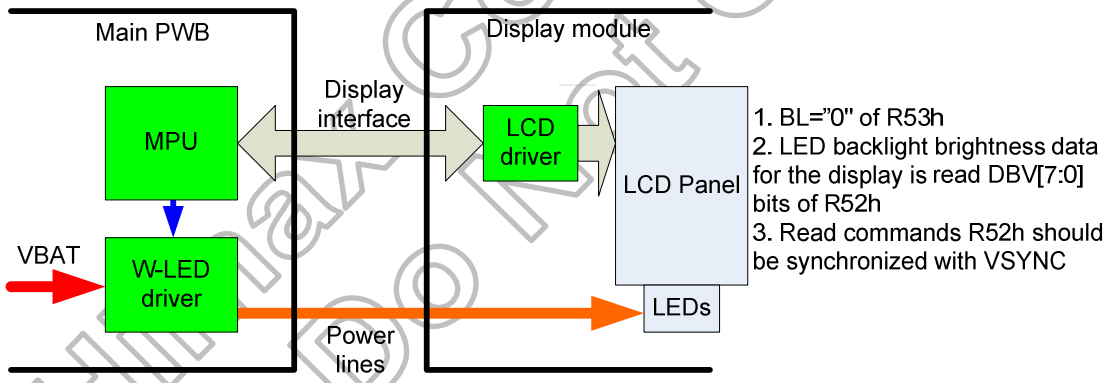


Figure 5.38: Module architecture

5.16.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that : Duty (valid level period (LED on) / one complete period)=1/ gain.

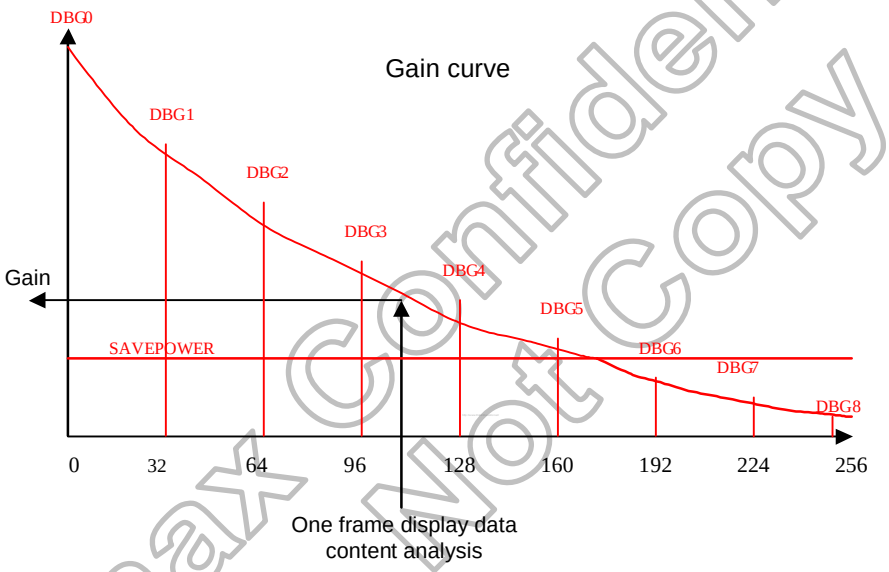


Figure 5.39: CABC gain / CABC duty generation

For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

5.16.3 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV[7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period=2.95 ms, and DBV[7:0](R51h)='228DEC' and CABC duty is 74%. Then CABC_PWM_OUT duty=(228) / 255 x 74.42%≡66.54%. Correspond to the CABC_PWM_OUT period=2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT =0.99ms.

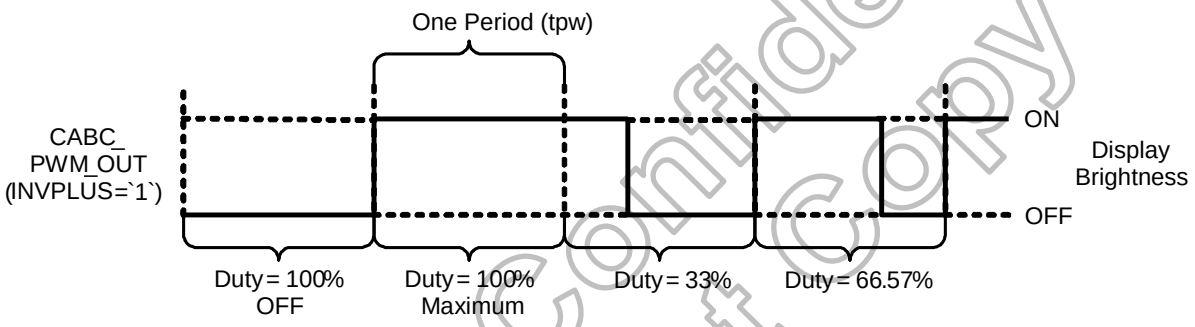


Figure 5.40: CABC_PWM_OUT output duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Table 5.51: CABC timing table

Note1: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
Note2: The pulse width range by setting CABC related registers is locate between 0.0333ms to 8.33ms.

When Architecture II module is used (BL='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R51h) will be read a value as 169DEC ((169)/255≡ 66.27%).

5.16.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL='0' of R53h), CABC minimum brightness setting is ignored. "CMB[7:0], Read CABC minimum brightness (R5Fh)" always read the setting value of "CMB[7:0], Write CABC minimum brightness (R5Eh)"

5.17 OTP programing

5.17.1 OTP table

OTP_INDEX (HEX)	Ref. Command	B7	B6	B5	B4	B3	B2	B1	B0
49	SETMIPI	**NVALID_28**	-	-	TX_OSC	-	-	LAN_NUM[1:0]	
4A		-	-	-	-	-	-	TX_DELAY[1:0]	
4C	SETCABC	**NVALID_14**	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY
4D		PWM_PERIOD[7:0]							
4E		CABC_FSYNC	DIM_FRAME[6:0]						
4F		CABC_STEP[7:0]							
50		CABC_CLKEN[7:0]							
51	SETCABCGAIN_UI	**NVALID_15**	DBG0[6:0]						
52		-	DBG1[6:0]						
53		-	DBG2[6:0]						
54		-	DBG3[6:0]						
55		-	DBG4[6:0]						
56		-	DBG5[6:0]						
57		-	DBG6[6:0]						
58		-	DBG7[6:0]						
59		-	DBG8[6:0]						
5A		CABC_DD0	SAVEPOWER0[6:0]						
5B	SETCABCGAIN_ST	**NVALID_16**	DBG0[6:0]						
5C		-	DBG1[6:0]						
5D		-	DBG2[6:0]						
5E		-	DBG3[6:0]						
5F		-	DBG4[6:0]						
60		-	DBG5[6:0]						
61		-	DBG6[6:0]						
62		-	DBG7[6:0]						
63		-	DBG8[6:0]						
64		CABC_DD1	SAVEPOWER1[6:0]						
65	SETCABCGAIN_MV	**NVALID_17**	DBG0[6:0]						
66		-	DBG1[6:0]						
67		-	DBG2[6:0]						
68		-	DBG3[6:0]						
69		-	DBG4[6:0]						
6A		-	DBG5[6:0]						
6B		-	DBG6[6:0]						
6C		-	DBG7[6:0]						
6D		-	DBG8[6:0]						
6E		CABC_DD2	SAVEPOWER2[6:0]						
7C	SETVCMC_1	**NVALID_VCM1**	-	-	-	-	-	-	-
7D		VCMC_1[7:0]							
7E	SETVCMC_2	**NVALID_VCM2**	-	-	-	-	-	-	-
7F		VCMC_2[7:0]							
80	SETVCMC_3	**NVALID_VCM3**	-	-	-	-	-	-	-
81		VCMC_3[7:0]							
82	SETID_1	**NVALID_ID1**	-	-	-	-	-	-	-
83		ID1_1[7:0]							
84		ID2_1[7:0]							
85		ID3_1[7:0]							
86	SETID_2	**NVALID_ID2**	-	-	-	-	-	-	-
87		ID1_2[7:0]							
88		ID2_2[7:0]							
89		ID3_2[7:0]							
8A	SETID_3	**NVALID_ID3**	-	-	-	-	-	-	-
8B		ID1_3[7:0]							
8C		ID2_3[7:0]							
8D		ID3_3[7:0]							
8E	SETPANEL	**NVALID_20**	-	-	-	SS_PANEL	GS_PANEL	REV_PANE	BGR_PANEL
8F	SETRGBIF	**NVALID_21**	-	-	-	DPL	HSPL	VSPL	EPL
90	SETOSC	**NVALID_22**	-	-	-	UADJ[3:0]			
91	SETPOWER	**NVALID_23**	-	-	-	-	-	-	DSTB
92		-	FS1[2:0]			-	AP[2:0]		
93		VGHS[3:0]				VGLS[3:0]			
94		DT[1:0]		-	-	-	-	-	-
95		-	-	-	BTP[4:0]				
96		-	-	-	BTN[4:0]				
97		VRHP[7:0]							
98		VRHN[7:0]							
99		-	-	VRMP[5:0]					
9A		-	-	VRMN[5:0]					

9B		-	APF_EN	DD_TU	VPNL_EN	-	-	PCCS[1:0]	
9C		-	DC86_DIV3	DC86_DIV2	DC86_DIV1	DC86_DIV0	XDK1	XDK0	AUTO_XDK
A3	SETDISP	**NVALID_24**	-	-	-	-	-	-	-
A4		NL[7:0]							
A5		BP [7:0]							
A6		FP [7:0]							
A7		RTN[7:0]							
A8		SAP[3:0]				INIT_DISP	INIT_SET[2:0]		
A9		GEN_ON[7:0]							
AA		GEN_OFF[7:0]							
AB		BP_PE [7:0]							
AC		FP_PE [7:0]							
AD		RTN_PE[7:0]							
AE		-	RES_SEL[2:0]			TGS[3:0]			
AF	SETTE	**NVALID_25**	-	-	-	TEI[3:0]			
B0		-	-	-	-	-	TEP[10:8]		
B1		TEP[7:0]							
B2	SETMPUCYC	**NVALID_26**	-	NW_PE[2:0]		NW[2:0]			
B3		-	-	-	-	SHR[11:8]			
B4		SHR[7:0]							
B5		SON[7:0]							
B6		SOFF[7:0]							
B7		CHR[7:0]							
B8		CON[7:0]							
B9		COFF[7:0]							
BA		SHP[3:0]				-	-	-	-
BB		CHP[3:0]				CCP[3:0]			
BC		N_t1[7:0]							
BD		N_t2[7:0]							
BE		N_t3[7:0]							
BF		N_t4[7:0]							
C0		N_t5[7:0]							
C1		N_t6[7:0]							
C2		N_t7[7:0]							
C3		N_t8[7:0]							
C4		N_t9[7:0]							
C5		-	-	-	-	EQT[3:0]			
C9	SETRGBCYC	**NVALID_27**	-	NW_PE[2:0]		NW[2:0]			
CA		-	-	-	-	SHR[11:8]			
CB		SHR[7:0]							
CC		SON[7:0]							
CD		SOFF[7:0]							
CE		CHR[7:0]							
CF		CON[7:0]							
D0		COFF[7:0]							
D1		SHP[3:0]				-	-	-	-
D2		CHP[3:0]				CCP[3:0]			
D3		N_t1[7:0]							
D4		N_t2[7:0]							
D5		N_t3[7:0]							
D6		N_t4[7:0]							
D7		N_t5[7:0]							
D8		N_t6[7:0]							
D9		N_t7[7:0]							
DA		N_t8[7:0]							
DB		N_t9[7:0]							
DC		-	-	-	-	EQT[3:0]			
F7	SETRGAMMA (GC0)	**NVALID_30**	-	G0_R_VRP0[5:0]					
F8		-	-	G0_R_VRP1[5:0]					
F9		-	-	G0_R_VRP2[5:0]					
FA		-	-	G0_R_VRP3[5:0]					
FB		-	-	G0_R_VRP4[5:0]					
FC		-	-	G0_R_VRP5[5:0]					
FD		-	G1_R_PRP0[6:0]						
FE		-	G0_R_PRP1[6:0]						
FF		-	-	-	G0_R_ PKP0[4:0]				
100		-	-	-	G0_R_PKP1[4:0]				
101		-	-	-	G0_R_PKP2[4:0]				
102		-	-	-	G0_R_PKP3[4:0]				
103		-	-	-	G0_R_PKP4[4:0]				
104		-	-	-	G0_R_PKP5[4:0]				
105		-	-	-	G0_R_PKP6[4:0]				
106		-	-	-	G0_R_PKP7[4:0]				
107		-	-	-	G0_R_PKP8[4:0]				

108		-	-	G0_R_VRN0[5:0]		
109		-	-	G0_R_VRN1[5:0]		
10A		-	-	G0_R_VRN2[5:0]		
10B		-	-	G0_R_VRN3[5:0]		
10C		-	-	G0_R_VRN4[5:0]		
10D		-	-	G0_R_VRN5[5:0]		
10E		-	G0_R_PRN0[6:0]			
10F		-	G0_R_PRN1[6:0]			
110		-	-	-	G0_R_PKN0[4:0]	
111		-	-	-	G0_R_PKN1[4:0]	
112		-	-	-	G0_R_PKN2[4:0]	
113		-	-	-	G0_R_PKN3[4:0]	
114		-	-	-	G0_R_PKN4[4:0]	
115		-	-	-	G0_R_PKN5[4:0]	
116		-	-	-	G0_R_PKN6[4:0]	
117		-	-	-	G0_R_PKN7[4:0]	
118		-	-	-	G0_R_PKN8[4:0]	
119	SETGGAMMA (GC0)	**NVALID_31**	-	G0_G_VRP0[5:0]		
11A		-	-	G0_G_VRP1[5:0]		
11B		-	-	G0_G_VRP2[5:0]		
11C		-	-	G0_G_VRP3[5:0]		
11D		-	-	G0_G_VRP4[5:0]		
11E		-	-	G0_G_VRP5[5:0]		
11F		-	G0_G_PRP0[6:0]			
120		-	G0_G_PRP1[6:0]			
121		-	-	-	G0_G_ PKP0[4:0]	
122		-	-	-	G0_G_PKP1[4:0]	
123		-	-	-	G0_G_PKP2[4:0]	
124		-	-	-	G0_G_PKP3[4:0]	
125		-	-	-	G0_G_PKP4[4:0]	
126		-	-	-	G0_G_PKP5[4:0]	
127		-	-	-	G0_G_PKP6[4:0]	
128		-	-	-	G0_G_PKP7[4:0]	
129		-	-	-	G0_G_PKP8[4:0]	
12A		-	-	G0_G_VRN0[5:0]		
12B		-	-	G0_G_VRN1[5:0]		
12C		-	-	G0_G_VRN2[5:0]		
12D		-	-	G0_G_VRN3[5:0]		
12E		-	-	G0_G_VRN4[5:0]		
12F		-	-	G0_G_VRN5[5:0]		
130		-	G0_G_PRN0[6:0]			
131		-	G0_G_PRN1[6:0]			
132		-	-	-	G0_G_PKN0[4:0]	
133		-	-	-	G0_G_PKN1[4:0]	
134		-	-	-	G0_G_PKN2[4:0]	
135		-	-	-	G0_G_PKN3[4:0]	
136		-	-	-	G0_G_PKN4[4:0]	
137		-	-	-	G0_G_PKN5[4:0]	
138		-	-	-	G0_G_PKN6[4:0]	
139		-	-	-	G0_G_PKN7[4:0]	
13A		-	-	-	G0_G_PKN8[4:0]	
13B	SETBGAMMA (GC0)	**NVALID_32**	-	G0_B_VRP0[5:0]		
13C		-	-	G0_B_VRP1[5:0]		
13D		-	-	G0_B_VRP2[5:0]		
13E		-	-	G0_B_VRP3[5:0]		
13F		-	-	G0_B_VRP4[5:0]		
140		-	-	G0_B_VRP5[5:0]		
141		-	G0_B_PRP0[6:0]			
142		-	G0_B_PRP1[6:0]			
143		-	-	-	G0_B_ PKP0[4:0]	
144		-	-	-	G0_B_PKP1[4:0]	
145		-	-	-	G0_B_PKP2[4:0]	
146		-	-	-	G0_B_PKP3[4:0]	
147		-	-	-	G0_B_PKP4[4:0]	
148		-	-	-	G0_B_PKP5[4:0]	
149		-	-	-	G0_B_PKP6[4:0]	
14A		-	-	-	G0_B_PKP7[4:0]	
14B		-	-	-	G0_B_PKP8[4:0]	
14C		-	-	G0_B_VRN0[5:0]		
14D		-	-	G0_B_VRN1[5:0]		
14E		-	-	G0_B_VRN2[5:0]		
14F		-	-	G0_B_VRN3[5:0]		
150		-	-	G0_B_VRN4[5:0]		
151		-	-	G0_B_VRN5[5:0]		
152		-	G0_B_PRN0[6:0]			

153		-	G0_B_PRN1[6:0]		
154		-	-	-	G0_B_PKN0[4:0]
155		-	-	-	G0_B_PKN1[4:0]
156		-	-	-	G0_B_PKN2[4:0]
157		-	-	-	G0_B_PKN3[4:0]
158		-	-	-	G0_B_PKN4[4:0]
159		-	-	-	G0_B_PKN5[4:0]
15A		-	-	-	G0_B_PKN6[4:0]
15B		-	-	-	G0_B_PKN7[4:0]
15C		-	-	-	G0_B_PKN8[4:0]
15D		**NVALID_33**	-	G1_R_VRP0[5:0]	
15E		-	-	G1_R_VRP1[5:0]	
15F		-	-	G1_R_VRP2[5:0]	
160		-	-	G1_R_VRP3[5:0]	
161		-	-	G1_R_VRP4[5:0]	
162		-	-	G1_R_VRP5[5:0]	
163		-	G1_R_PRP0[6:0]		
164		-	G1_R_PRP1[6:0]		
165		-	-	-	G1_R_ PKP0[4:0]
166		-	-	-	G1_R_PKP1[4:0]
167		-	-	-	G1_R_PKP2[4:0]
168		-	-	-	G1_R_PKP3[4:0]
169		-	-	-	G1_R_PKP4[4:0]
16A		-	-	-	G1_R_PKP5[4:0]
16B		-	-	-	G1_R_PKP6[4:0]
16C		-	-	-	G1_R_PKP7[4:0]
16D	SETRGAMMA (GC1)	-	-	-	G1_R_PKP8[4:0]
16E		-	-	G1_R_VRN0[5:0]	
16F		-	-	G1_R_VRN1[5:0]	
170		-	-	G1_R_VRN2[5:0]	
171		-	-	G1_R_VRN3[5:0]	
172		-	-	G1_R_VRN4[5:0]	
173		-	-	G1_R_VRN5[5:0]	
174		-	G1_R_PRN0[6:0]		
175		-	G1_R_PRN1[6:0]		
176		-	-	-	G1_R_PKN0[4:0]
177		-	-	-	G1_R_PKN1[4:0]
178		-	-	-	G1_R_PKN2[4:0]
179		-	-	-	G1_R_PKN3[4:0]
17A			-	-	G1_R_PKN4[4:0]
17B		-	-	-	G1_R_PKN5[4:0]
17C		-	-	-	G1_R_PKN6[4:0]
17D		-	-	-	G1_R_PKN7[4:0]
17E		-	-	-	G1_R_PKN8[4:0]
17F	SETGGAMMA (GC1)	**NVALID_34**	-	G1_G_VRP0[5:0]	
180		-	-	G1_G_VRP1[5:0]	
181		-	-	G1_G_VRP2[5:0]	
182		-	-	G1_G_VRP3[5:0]	
183		-	-	G1_G_VRP4[5:0]	
184		-	-	G1_G_VRP5[5:0]	
185		-	G1_G_PRP0[6:0]		
186		-	G1_G_PRP1[6:0]		
187		-	-	-	G1_G_ PKP0[4:0]
188		-	-	-	G1_G_PKP1[4:0]
189		-	-	-	G1_G_PKP2[4:0]
18A		-	-	-	G1_G_PKP3[4:0]
18B		-	-	-	G1_G_PKP4[4:0]
18C		-	-	-	G1_G_PKP5[4:0]
18D		-	-	-	G1_G_PKP6[4:0]
18E		-	-	-	G1_G_PKP7[4:0]
18F		-	-	-	G1_G_PKP8[4:0]
190		-	-	G1_G_VRN0[5:0]	
191		-	-	G1_G_VRN1[5:0]	
192		-	-	G1_G_VRN2[5:0]	
193		-	-	G1_G_VRN3[5:0]	
194		-	-	G1_G_VRN4[5:0]	
195		-	-	G1_G_VRN5[5:0]	
196		-	G1_G_PRN0[6:0]		
197		-	G1_G_PRN1[6:0]		
198		-	-	-	G1_G_PKN0[4:0]
199		-	-	-	G1_G_PKN1[4:0]
19A		-	-	-	G1_G_PKN2[4:0]
19B		-	-	-	G1_G_PKN3[4:0]
19C		-	-	-	G1_G_PKN4[4:0]
19D		-	-	-	G1_G_PKN5[4:0]

19E		-	-	-	G1_G_PKN6[4:0]
19F		-	-	-	G1_G_PKN7[4:0]
1A0		-	-	-	G1_G_PKN8[4:0]
1A1	SETBGAMMA (GC1)	**NVALID_35**	-	G1_B_VRP0[5:0]	
1A2		-	-	G1_B_VRP1[5:0]	
1A3		-	-	G1_B_VRP2[5:0]	
1A4		-	-	G1_B_VRP3[5:0]	
1A5		-	-	G1_B_VRP4[5:0]	
1A6		-	-	G1_B_VRP5[5:0]	
1A7		-	G1_B_PRP0[6:0]		
1A8		-	G1_B_PRP1[6:0]		
1A9		-	-	-	G1_B_ PKP0[4:0]
1AA		-	-	-	G1_B_PKP1[4:0]
1AB		-	-	-	G1_B_PKP2[4:0]
1AC		-	-	-	G1_B_PKP3[4:0]
1AD		-	-	-	G1_B_PKP4[4:0]
1AE		-	-	-	G1_B_PKP5[4:0]
1AF		-	-	-	G1_B_PKP6[4:0]
1B0		-	-	-	G1_B_PKP7[4:0]
1B1		-	-	-	G1_B_PKP8[4:0]
1B2		-	-	G1_B_VRN0[5:0]	
1B3		-	-	G1_B_VRN1[5:0]	
1B4		-	-	G1_B_VRN2[5:0]	
1B5		-	-	G1_B_VRN3[5:0]	
1B6		-	-	G1_B_VRN4[5:0]	
1B7		-	-	G1_B_VRN5[5:0]	
1B8		-	G1_B_PRN0[6:0]		
1B9		-	G1_B_PRN1[6:0]		
1BA		-	-	-	G1_B_PKN0[4:0]
1BB		-	-	-	G1_B_PKN1[4:0]
1BC		-	-	-	G1_B_PKN2[4:0]
1BD		-	-	-	G1_B_PKN3[4:0]
1BE		-	-	-	G1_B_PKN4[4:0]
1BF		-	-	-	G1_B_PKN5[4:0]
1C0		-	-	-	G1_B_PKN6[4:0]
1C1		-	-	-	G1_B_PKN7[4:0]
1C2		-	-	-	G1_B_PKN8[4:0]
1C3	SETRGAMMA (GC2)	**NVALID_36**	-	G2_R_VRP0[5:0]	
1C4		-	-	G2_R_VRP1[5:0]	
1C5		-	-	G2_R_VRP2[5:0]	
1C6		-	-	G2_R_VRP3[5:0]	
1C7		-	-	G2_R_VRP4[5:0]	
1C8		-	-	G2_R_VRP5[5:0]	
1C9		-	G2_R_PRP0[6:0]		
1CA		-	G2_R_PRP1[6:0]		
1CB		-	-	-	G2_R_ PKP0[4:0]
1CC		-	-	-	G2_R_PKP1[4:0]
1CD		-	-	-	G2_R_PKP2[4:0]
1CE		-	-	-	G2_R_PKP3[4:0]
1CF		-	-	-	G2_R_PKP4[4:0]
1D0		-	-	-	G2_R_PKP5[4:0]
1D1		-	-	-	G2_R_PKP6[4:0]
1D2		-	-	-	G2_R_PKP7[4:0]
1D3		-	-	-	G2_R_PKP8[4:0]
1D4		-	-	G2_R_VRN0[5:0]	
1D5		-	-	G2_R_VRN1[5:0]	
1D6		-	-	G2_R_VRN2[5:0]	
1D7		-	-	G2_R_VRN3[5:0]	
1D8		-	-	G2_R_VRN4[5:0]	
1D9		-	-	G2_R_VRN5[5:0]	
1DA		-	G2_R_PRN0[6:0]		
1DB		-	G2_R_PRN1[6:0]		
1DC		-	-	-	G2_R_PKN0[4:0]
1DD		-	-	-	G2_R_PKN1[4:0]
1DE		-	-	-	G2_R_PKN2[4:0]
1DF		-	-	-	G2_R_PKN3[4:0]
1E0		-	-	-	G2_R_PKN4[4:0]
1E1		-	-	-	G2_R_PKN5[4:0]
1E2		-	-	-	G2_R_PKN6[4:0]
1E3		-	-	-	G2_R_PKN7[4:0]
1E4		-	-	-	G2_R_PKN8[4:0]
1E5	SETGGAMMA (GC2)	**NVALID_37**	-	G2_G_VRP0[5:0]	
1E6		-	-	G2_G_VRP1[5:0]	
1E7		-	-	G2_G_VRP2[5:0]	

1E8		-	-	G2_G_VRP3[5:0]	
1E9		-	-	G2_G_VRP4[5:0]	
1EA		-	-	G2_G_VRP5[5:0]	
1EB		-	G2_G_PRP0[6:0]		
1EC		-	G2_G_PRP1[6:0]		
1ED		-	-	-	G2_G_ PKP0[4:0]
1EE		-	-	-	G2_G_PKP1[4:0]
1EF		-	-	-	G2_G_PKP2[4:0]
1F0		-	-	-	G2_G_PKP3[4:0]
1F1		-	-	-	G2_G_PKP4[4:0]
1F2		-	-	-	G2_G_PKP5[4:0]
1F3		-	-	-	G2_G_PKP6[4:0]
1F4		-	-	-	G2_G_PKP7[4:0]
1F5		-	-	-	G2_G_PKP8[4:0]
1F6		-	-	G2_G_VRN0[5:0]	
1F7		-	-	G2_G_VRN1[5:0]	
1F8		-	-	G2_G_VRN2[5:0]	
1F9		-	-	G2_G_VRN3[5:0]	
1FA		-	-	G2_G_VRN4[5:0]	
1FB		-	-	G2_G_VRN5[5:0]	
1FC		-	G2_G_PRN0[6:0]		
1FD		-	G2_G_PRN1[6:0]		
1FE		-	-	-	G2_G_PKN0[4:0]
1FF		-	-	-	G2_G_PKN1[4:0]
200		-	-	-	G2_G_PKN2[4:0]
201		-	-	-	G2_G_PKN3[4:0]
202		-	-	-	G2_G_PKN4[4:0]
203		-	-	-	G2_G_PKN5[4:0]
204		-	-	-	G2_G_PKN6[4:0]
205		-	-	-	G2_G_PKN7[4:0]
206		-	-	-	G2_G_PKN8[4:0]
207		**NVALID_38**	-	G2_B_VRP0[5:0]	
208		-	-	G2_B_VRP1[5:0]	
209		-	-	G2_B_VRP2[5:0]	
20A		-	-	G2_B_VRP3[5:0]	
20B		-	-	G2_B_VRP4[5:0]	
20C		-	-	G2_B_VRP5[5:0]	
20D		-	G2_B_PRP0[6:0]		
20E		-	G2_B_PRP1[6:0]		
20F		-	-	-	G2_B_ PKP0[4:0]
210		-	-	-	G2_B_PKP1[4:0]
211		-	-	-	G2_B_PKP2[4:0]
212		-	-	-	G2_B_PKP3[4:0]
213		-	-	-	G2_B_PKP4[4:0]
214		-	-	-	G2_B_PKP5[4:0]
215		-	-	-	G2_B_PKP6[4:0]
216		-	-	-	G2_B_PKP7[4:0]
217	SETBGAMMA (GC2)	-	-	-	G2_B_PKP8[4:0]
218		-	-	G2_B_VRN0[5:0]	
219		-	-	G2_B_VRN1[5:0]	
21A		-	-	G2_B_VRN2[5:0]	
21B		-	-	G2_B_VRN3[5:0]	
21C		-	-	G2_B_VRN4[5:0]	
21D		-	-	G2_B_VRN5[5:0]	
21E		-	G2_B_PRN0[6:0]		
21F		-	G2_B_PRN1[6:0]		
220		-	-	-	G2_B_PKN0[4:0]
221		-	-	-	G2_B_PKN1[4:0]
222		-	-	-	G2_B_PKN2[4:0]
223		-	-	-	G2_B_PKN3[4:0]
224		-	-	-	G2_B_PKN4[4:0]
225		-	-	-	G2_B_PKN5[4:0]
226		-	-	-	G2_B_PKN6[4:0]
227		-	-	-	G2_B_PKN7[4:0]
228		-	-	-	G2_B_PKN8[4:0]
229	SETRGAMMA (GC3)	**NVALID_39**	-	G3_R_VRP0[5:0]	
22A		-	-	G3_R_VRP1[5:0]	
22B		-	-	G3_R_VRP2[5:0]	
22C		-	-	G3_R_VRP3[5:0]	
22D		-	-	G3_R_VRP4[5:0]	
22E		-	-	G3_R_VRP5[5:0]	
22F		-	G3_R_PRP0[6:0]		
230		-	G3_R_PRP1[6:0]		
231		-	-	-	G3_R_ PKP0[4:0]
232		-	-	-	G3_R_PKP1[4:0]

233		-	-	-	G3_R_PKP2[4:0]
234		-	-	-	G3_R_PKP3[4:0]
235		-	-	-	G3_R_PKP4[4:0]
236		-	-	-	G3_R_PKP5[4:0]
237		-	-	-	G3_R_PKP6[4:0]
238		-	-	-	G3_R_PKP7[4:0]
239		-	-	-	G3_R_PKP8[4:0]
23A		-	-	G3_R_VRN0[5:0]	
23B		-	-	G3_R_VRN1[5:0]	
23C		-	-	G3_R_VRN2[5:0]	
23D		-	-	G3_R_VRN3[5:0]	
23E		-	-	G3_R_VRN4[5:0]	
23F		-	-	G3_R_VRN5[5:0]	
240		-	G3_R_PRN0[6:0]		
241		-	G3_R_PRN1[6:0]		
242		-	-	-	G3_R_PKN0[4:0]
243		-	-	-	G3_R_PKN1[4:0]
244		-	-	-	G3_R_PKN2[4:0]
245		-	-	-	G3_R_PKN3[4:0]
246		-	-	-	G3_R_PKN4[4:0]
247		-	-	-	G3_R_PKN5[4:0]
248		-	-	-	G3_R_PKN6[4:0]
249		-	-	-	G3_R_PKN7[4:0]
24A		-	-	-	G3_R_PKN8[4:0]
24B		**NVALID_40**	-	G3_G_VRP0[5:0]	
24C		-	-	G3_G_VRP1[5:0]	
24D		-	-	G3_G_VRP2[5:0]	
24E		-	-	G3_G_VRP3[5:0]	
24F		-	-	G3_G_VRP4[5:0]	
250		-	-	G3_G_VRP5[5:0]	
251		-	G3_G_PRP0[6:0]		
252		-	G3_G_PRP1[6:0]		
253		-	-	-	G3_G_ PKP0[4:0]
254		-	-	-	G3_G_PKP1[4:0]
255		-	-	-	G3_G_PKP2[4:0]
256		-	-	-	G3_G_PKP3[4:0]
257		-	-	-	G3_G_PKP4[4:0]
258		-	-	-	G3_G_PKP5[4:0]
259		-	-	-	G3_G_PKP6[4:0]
25A		-	-	-	G3_G_PKP7[4:0]
25B	SETGGAMMA (GC3)	-	-	-	G3_G_PKP8[4:0]
25C		-	-	G3_G_VRN0[5:0]	
25D		-	-	G3_G_VRN1[5:0]	
25E		-	-	G3_G_VRN2[5:0]	
25F		-	-	G3_G_VRN3[5:0]	
260		-	-	G3_G_VRN4[5:0]	
261		-	-	G3_G_VRN5[5:0]	
262		-	G3_G_PRN0[6:0]		
263		-	G3_G_PRN1[6:0]		
264		-	-	-	G3_G_PKN0[4:0]
265		-	-	-	G3_G_PKN1[4:0]
266		-	-	-	G3_G_PKN2[4:0]
267		-	-	-	G3_G_PKN3[4:0]
268		-	-	-	G3_G_PKN4[4:0]
269		-	-	-	G3_G_PKN5[4:0]
26A		-	-	-	G3_G_PKN6[4:0]
26B		-	-	-	G3_G_PKN7[4:0]
26C		-	-	-	G3_G_PKN8[4:0]
26D	SETBGAMMA (GC3)	**NVALID_41**	-	G3_B_VRP0[5:0]	
26E		-	-	G3_B_VRP1[5:0]	
26F		-	-	G3_B_VRP2[5:0]	
270		-	-	G3_B_VRP3[5:0]	
271		-	-	G3_B_VRP4[5:0]	
272		-	-	G3_B_VRP5[5:0]	
273		-	G3_B_PRP0[6:0]		
274		-	G3_B_PRP1[6:0]		
275		-	-	-	G3_B_ PKP0[4:0]
276		-	-	-	G3_B_PKP1[4:0]
277		-	-	-	G3_B_PKP2[4:0]
278		-	-	-	G3_B_PKP3[4:0]
279		-	-	-	G3_B_PKP4[4:0]
27A		-	-	-	G3_B_PKP5[4:0]
27B		-	-	-	G3_B_PKP6[4:0]
27C		-	-	-	G3_B_PKP7[4:0]
27D		-	-	-	G3_B_PKP8[4:0]

27E		-	-	G3_B_VRN0[5:0]				
27F		-	-	G3_B_VRN1[5:0]				
280		-	-	G3_B_VRN2[5:0]				
281		-	-	G3_B_VRN3[5:0]				
282		-	-	G3_B_VRN4[5:0]				
283		-	-	G3_B_VRN5[5:0]				
284		-	G3_B_PRN0[6:0]					
285		-	G3_B_PRN1[6:0]					
286		-	-	-	G3_B_PKN0[4:0]			
287		-	-	-	G3_B_PKN1[4:0]			
288		-	-	-	G3_B_PKN2[4:0]			
289		-	-	-	G3_B_PKN3[4:0]			
28A		-	-	-	G3_B_PKN4[4:0]			
28B		-	-	-	G3_B_PKN5[4:0]			
28C		-	-	-	G3_B_PKN6[4:0]			
28D		-	-	-	G3_B_PKN7[4:0]			
28E		-	-	-	G3_B_PKN8[4:0]			
2A7	SETDISMO	**NVALID_45**	0	-	-	RM	-	DM[1:0]

Note 1: The default value of OTP memory bits are all “1”.

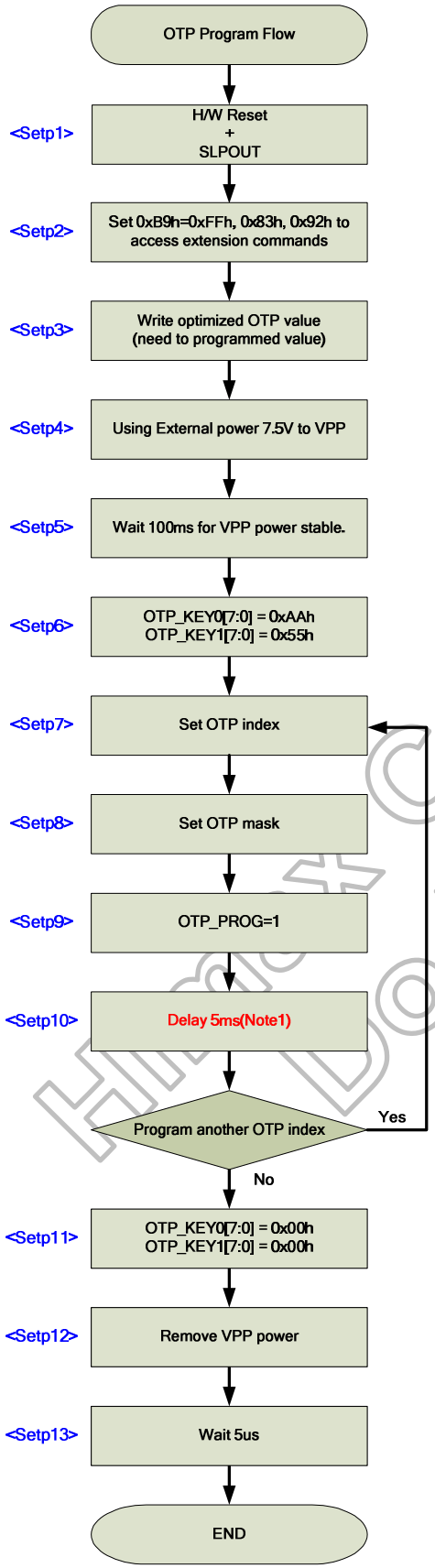
Note 2: VALID_xxx bit decide the OPT reload Enable/Disable, the default value is “1”. If the own OTP area of VALID_xxx bit had been programmed, the VALID_xxx bit will be changed to “0” automatically and execute the OTP reload.

Note 3: There are some conditions that HX8392-A can reload OTP.

a. Hardware reset
b. Software reset
c. SLPOUT command.

Table 5.52: OTP table

5.17.2 OTP programming flow



OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	1. If HX8392-A operate on OTP program mode, then keep on OTP program mode. 2. If HX8392-A operate on non-OTP program mode, then keep on non-OTP program mode.

Note:1. When do the OTP programming process, it must be added 5ms delay time and block program area need 20ms delay time after setting OTP PROG=1

Figure 5.41: OTP programming sequence

5.17.3 Programming sequence

Step	Operation
1	Power on and reset the module.
2	SLPOUT and set 0xB9h = 0xFFh, 0x83h, 0x92h to access the extension commands.
3	Write optimized values to related registers.
4	Set VGH power to 7.5V for OTP programming state for using internal power mode. Or using the external power 7.5V to VPP.
5	Wait 100ms for VPP power stable.
6	Set OTP_KEY1[7:0] (RE9h)=0xAAh and OTP_KEY1[7:0] (RE9h)=0x55h to enter OTP program mode.
7	Specify OTP_index, please refer to the OTP table.
8	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
9	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
10	Wait 5 ms (**Note 1,4**)
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (7). Otherwise, Set OTP_KEY1[7:0] (RE9h)=0x00h and OTP_KEY1[7:0] (RE9h)=0x00h to leave OTP program mode.
12	Remove the external power on VPP pin.
13	Wait 5us

Note 1: When do the OTP programming process, it must be added 5ms delay time and block program area need 20ms delay time after setting OTP_PROG=1

Note 2: When do the OTP program onVCMC setting (SETVCMC_1: 7Dh, SETVCMC_2: 7Fh, SETVCMC_3: 81h), user just specify the 7Ch, the all settings of DDB will be programmed to SETVCMC_1, SETVCMC_2 and SETVCMC_3 automatically.

Note 3: When do the OTP program on ID1~3 setting (SETID_1: 83h~85h, SETID_2: 87h~89h, SETID_3: 8Bh~8Dh), user just specify the 82h, the all settings of ID1~3 will be programmed to SETID_1, SETID_2 and SETID_3 automatically.

Note 4: Some OTP can block program, user just specify the OTP_INDEX, the all settings of specially block will be programmed automatically. The block program area need 20ms delay tim

Ref. Command	OTP_INDEX of Program	OTP Area of Block program	Delay time
SETCABCGAIN_UI	51h	51h~5Ah	20ms
SETCABCGAIN_ST	5Bh	5Bh~64h	20ms
SETCABCGAIN_MV	65h	65h~6Eh	20ms
SETRGAMMA(GC0)	F7h	F7h~118h	20ms
SETGGAMMA(GC0)	119h	119h~13Ah	20ms
SETBGAMMA(GC0)	13Bh	13Bh~15Ch	20ms
SETRGAMMA(GC1)	15Dh	15Dh~17Eh	20ms
SETGGAMMA(GC1)	17Fh	17Fh~1A0h	20ms
SETBGAMMA(GC1)	1A1h	1A1h~1C2h	20ms
SETRGAMMA(GC2)	1C3h	1C3h~1E4h	20ms
SETGGAMMA(GC2)	1E5h	1E5h~206h	20ms
SETBGAMMA(GC2)	207h	207h~228h	20ms
SETRGAMMA(GC3)	229h	229h~24Ah	20ms
SETGGAMMA(GC3)	24Bh	24Bh~26Ch	20ms
SETBGAMMA(GC3)	26Dh	26Dh~28Eh	20ms

Table 5.53: OTP Programming sequence

5.17.4 OTP Programming example of VCOM setting VCMC

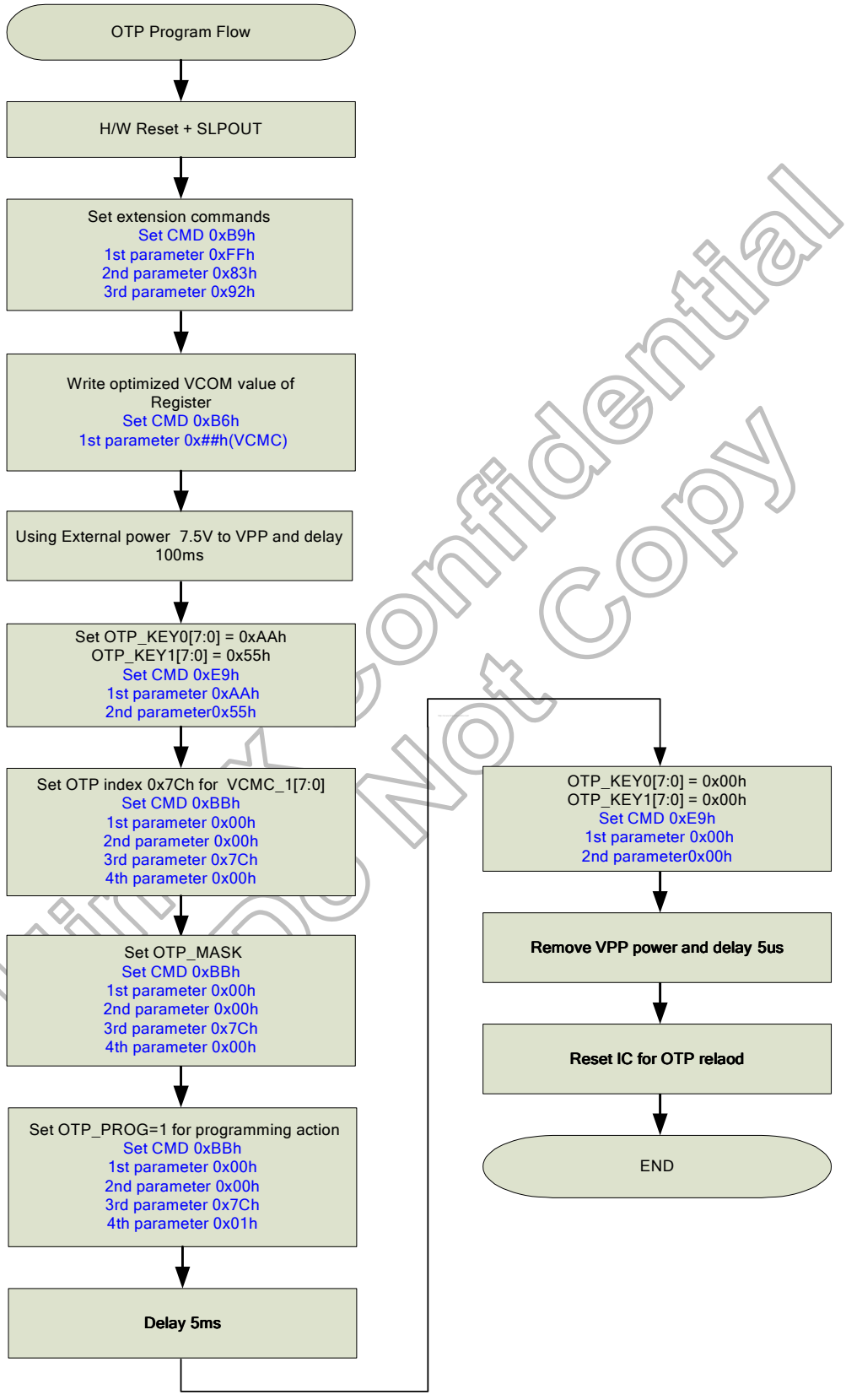


Figure 5.42: OTP programming sequence example 1

5.17.5 OTP Programming example of ID1, ID2 and ID3

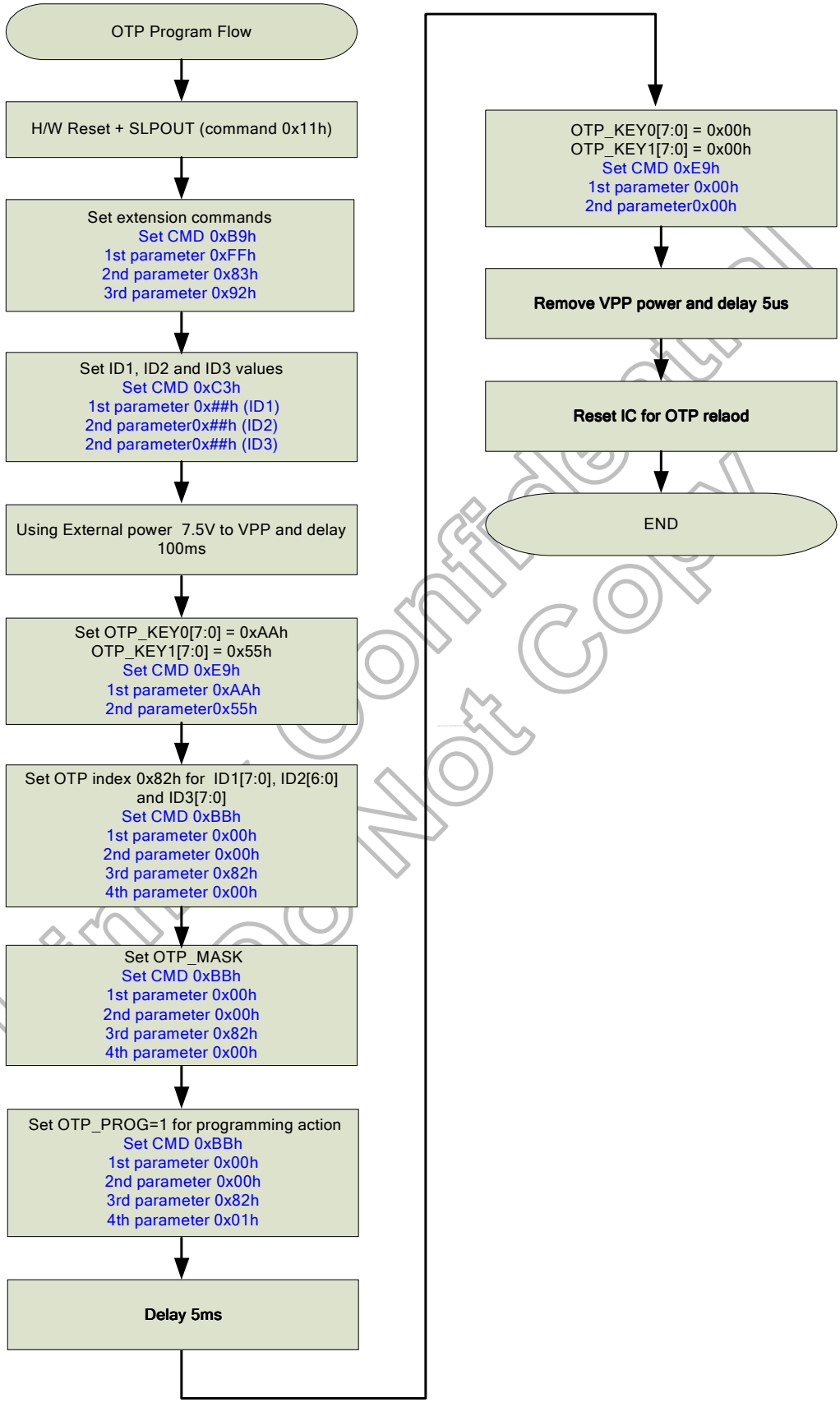


Figure 5.43: OTP programming sequence example 2

5.17.6 OTP read example of 0x7Dh (VCMC_1)

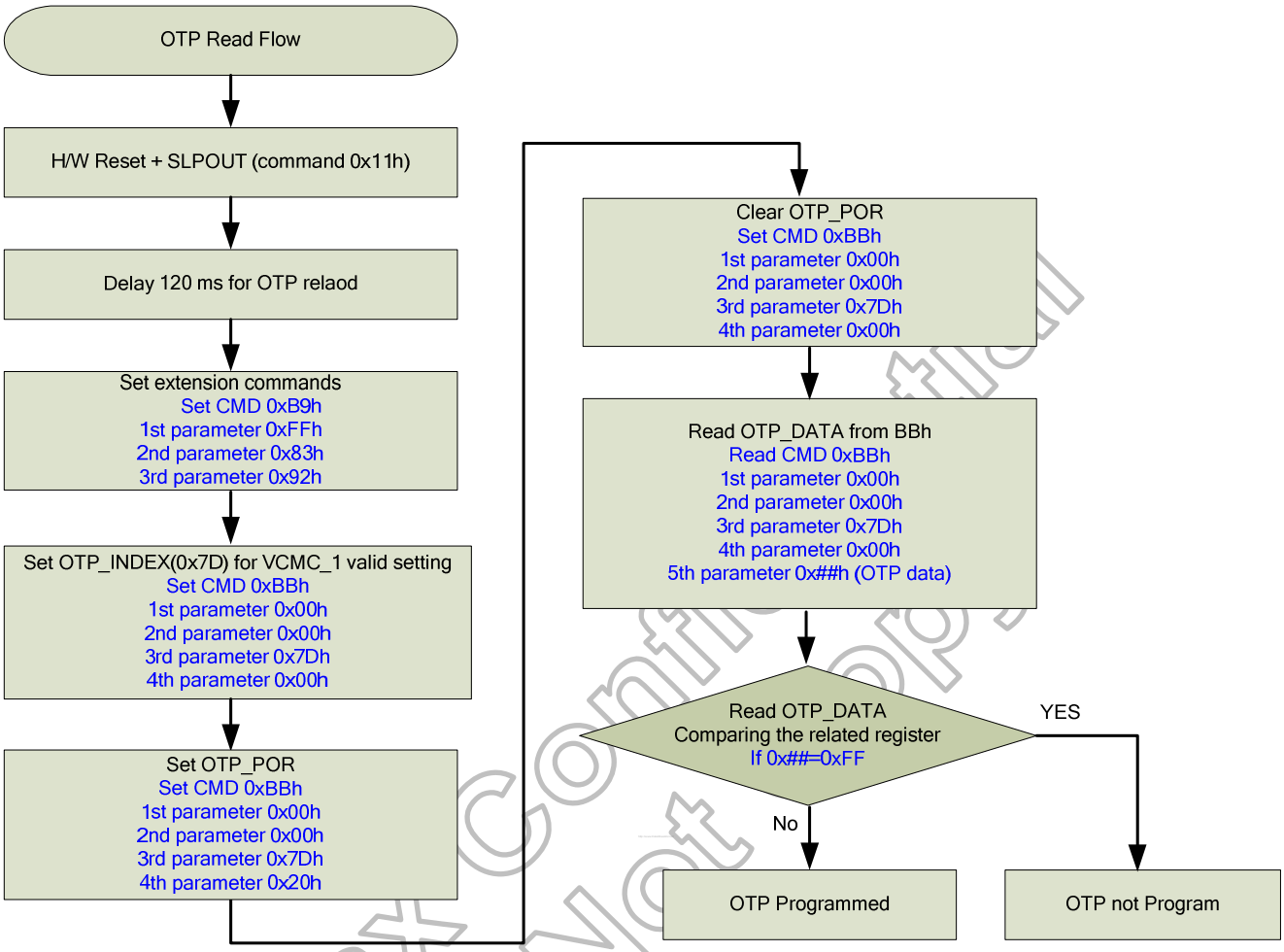


Figure 5.44: OTP read sequence flow of index 0x7Dh

6. Command

6.1 Command list

6.1.1 Standard command

(Hex)	Operation code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	Video mode
00	NOP	0	1	↑	0	0	0	0	0	0	0	0	No Operation	-	Yes
01	SWRESET	0	1	↑	0	0	0	0	0	0	0	1	Software Reset	-	Yes
04	RDDIDIF	0	1	↑	0	0	0	0	0	1	0	0	Read Display Identification Information	-	Yes
		1	↑	1	ID1[7:0]								-	-	-
		1	↑	1	ID2[7:0]								-	-	-
		1	↑	1	ID3[7:0]								-	-	-
05	RDNUMPE	0	1	↑	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	-	-
		1	↑	1	P[7:0]								-	-	-
09	RDDST	0	1	↑	0	0	0	0	1	0	0	1	Read Display Status	-	Yes
		1	↑	1	D[31:24]								-	-	-
		1	↑	1	D[23:16]								-	-	-
		1	↑	1	D[15:8]								-	-	-
		1	↑	1	D[7:0]								-	-	-
0A	RDDPM	0	1	↑	0	0	0	0	1	0	1	0	Read display power mode	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	D5	D4	D3	D2	0	0	-	-	-
0B	RDDMADCTL	0	1	↑	0	0	0	0	1	0	1	1	Read display MADCTL	-	Yes
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-
0C	RDDCOLMOD	0	1	↑	0	0	0	0	1	1	0	0	Read display pixel format	-	Yes
		1	↑	1	-	D6	D5	D4	-	D2	D1	D0	-	-	-
0D	RDDIM	0	1	↑	0	0	0	0	1	1	0	1	Read display image mode	-	Yes
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-
0E	RDDSM	0	1	↑	0	0	0	0	1	1	1	0	Read display signal mode	-	Yes
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-
0F	RDDSDR	0	1	↑	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-	Yes
		1	↑	1	D7	D6	D5	D4	0	0	0	0	-	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	Video mode
10	SLPIN	0	1	↑	0	0	0	1	0	0	0	0	Sleep In	-	Yes
11	SLPOUT	0	1	↑	0	0	0	1	0	0	0	1	Sleep Out	-	Yes
12	PTLON	0	1	↑	0	0	0	1	0	0	1	0	Partial Mode On	-	No
13	NORON	0	1	↑	0	0	0	1	0	0	1	1	Normal display mode on	-	No
20	INVOFF	0	1	↑	0	0	1	0	0	0	0	0	Display inversion off	-	Yes
21	INVON	0	1	↑	0	0	1	0	0	0	0	1	Display inversion on	-	Yes
22	ALLPOFF	0	1	↑	0	0	1	0	0	0	1	0	All Pixel Off	-	Yes
23	ALLPON	0	1	↑	0	0	1	0	0	0	1	1	All Pixel On	-	Yes
26	GAMSET	0	1	↑	0	0	1	0	0	1	1	0	Gamma set	-	Yes
		1	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-	-	
28	DISPOFF	0	1	↑	0	0	1	0	1	0	0	0	Display off	-	Yes
29	DISPON	0	1	↑	0	0	1	0	1	0	0	1	Display on	-	Yes
2A	CASET	0	1	↑	0	0	1	0	1	0	1	0	Column Address Set	-	No
		1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Column address start	-	-
		1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Column address start	-	-
		1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Column address end	-	-
		1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Column address end	-	-
2B	PASET	0	1	↑	0	0	1	0	1	0	1	1	Row address set	-	No
		1	1	↑	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Row address start	-	-
		1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Row address start	-	-
		1	1	↑	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Row address end	-	-
		1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Row address end	-	-
2C	RAMWR	0	1	↑	0	0	1	0	1	1	0	0	Memory Write	-	No
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	Write data		
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Write data	-	
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	Write data	-	
2E	RAMRD	0	1	↑	0	0	1	0	1	1	1	0	Memory read	-	No
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	Read data	-	-
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Read data	-	-
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
30	PLTAR	0	1	↑	0	0	1	1	0	0	0	0	Partial Area	-	No
		1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	Start row	-	-
		1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	Start row	-	-
		1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	End row	-	-
		1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	End row	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	Video mode
33	VSCRDEF	0	1	↑	0	0	1	1	0	0	1	1	Vertical scrolling definition	-	No
		1	1	↑	TFA[15:8]								-	-	-
		1	1	↑	TFA[7:0]								-	-	-
		1	1	↑	VSA[15:8]								-	-	-
		1	1	↑	VSA[7:0]								-	-	-
		1	1	↑	BFA[15:8]								-	-	-
		1	1	↑	BFA[7:0]								-	-	-
34	TEOFF	0	1	↑	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-	Yes
35	TEON	0	1	↑	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-	Yes
		1	1	↑	X	X	X	X	X	X	X	M	-	-	-
36	MADCTL	0	1	↑	0	0	1	1	0	1	1	0	Memory Access Control	-	Yes
		1	1	↑	B7	B6	B5	B4	B3	B2	X	X	-	-	-
37	VSCRSADD	0	1	↑	0	0	1	1	0	1	1	1	Vertical scrolling start address	-	No
		1	1	↑	VSP[15:8]								-	-	-
		1	1	↑	VSP[7:0]								-	-	-
38	IDMOFF	0	1	↑	0	0	1	1	1	0	0	0	Idle mode off	-	Yes
39	IDMON	0	1	↑	0	0	1	1	1	0	0	1	Idle mode on	-	Yes
3A	COLMOD	0	1	↑	0	0	1	1	1	0	1	0	-	-	Yes
		1	1	↑	X	D6	D5	D4	X	D2	D1	D0	-	-	-
3C	RAMWRCON	0	1	↑	0	0	1	1	1	1	0	0	Memory write	-	No
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	-	-	-
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-	-
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
3E	RAMRDCON	0	1	↑	0	0	1	1	1	1	1	0	Memory read	-	No
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	-	-	-
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-	-
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
44	TESL	0	1	↑	0	1	0	0	0	1	0	0	TESL	-	Yes
		1	1	↑	TELINE[15:8](8'b0)								-	-	-
		1	1	↑	TELINE[7:0](8'b0)								-	-	-
45	GETSCAN	0	1	↑	0	1	0	0	0	1	0	1	Reture the current scanline SLN[15:0]	-	Yes
		1	1	↑	SLN[15:8]								-	-	-
		1	1	↑	SLN[7:0]								-	-	-
51	WRDISBV	0	1	↑	0	1	0	1	0	0	0	1	Write Display Brightness	-	Yes
		1	1	↑	DBV[7:0]								-	-	-
52	RDDISBV	0	1	↑	0	1	0	1	0	0	1	0	Read Display Brightness Value	-	Yes
		1	↑	1	DBV[7:0]								-	-	-
53	WRCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Write CTRL Display	-	Yes
		1	1	↑	xx	xx	BCTRL	xx	DD	BL	xx	xx		-	-
54	RDCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Read Control Value Display	-	Yes
		1	↑	1	0	0	BCTRL	0	DD	BL	0	0	-	-	-
55	WRCABC	0	1	↑	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-	Yes
		1	1	↑	xx	xx	xx	xx	xx	xx	C1	C0	-	-	-
56	RDCABC	0	1	↑	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-	Yes
		1	↑	1	0	0	0	0	0	0	C1	C0	-	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	Video mode
5E	WRCABCMB	0	1	↑	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-	Yes
		1	1	↑	CMB[7:0]								-	-	-
5F	RDCABCMB	0	1	↑	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-	Yes
		1	↑	1	CMB[7:0]								-	-	-
68	RDABCSDR	0	1	↑	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-	Yes
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	-	-	-
		1	↑	1	D[7:6]		0	0	0	0	0	0	-	-	-
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1	-	Yes
		1	1	↑	module's manufacturer[7:0]								-	-	-
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2	-	Yes
		1	1	↑	LCD module/driver version [7:0]								-	-	-
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3	-	Yes
		1	1	↑	LCD module/driver ID[7:0]								-	-	-
A1	Read_DDB_start	0	1	↑	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
A8	Read_DDB_continue	0	1	↑	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-

Note: (1) Undefined commands are treated as NOP (00.H.) command.
(2) B0.H. to D9.H. and DE.H. to FF.H. are for factory use of display supplier. Customer can decide if these commands are available or they are treated as NOP (00.H.) commands before shipping to customer. Default value is NOP (00.H.).

6.1.2 User define command list table

User define command list is available only set “SETEXC” command.

Hex	Operation Code	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
B0	SETOSC	0	1	↑	1	0	1	1	0	0	0	0	Set Internal oscillator	-
		1	1	↑	-	-	-	-	-	-	-	OSC_EN	-	(00h)
		1	1	↑	-	-	-	-	UADJ[3:0]				-	(07h)
B1	SETPOWER	0	1	↑	1	0	1	1	0	0	0	1	Set power related setting	-
		1	1	↑	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_HZ	STB	-	(01h)
		1	1	↑	-	-	-	-	-	-	-	DSTB	-	(00h)
		1	1	↑	-	FS1[2:0]			-	AP[2:0]			-	(44h)
		1	1	↑	VGHS[3:0]				VGLS[3:0]				-	(77h)
		1	1	↑	DT[1:0]		-	-	-	-	-	-	-	(01h)
		1	1	↑	-	-	-	BTP[4:0]					-	(11h)
		1	1	↑	-	-	-	BTN[4:0]					-	(11h)
		1	1	↑	VRHP[7:0]								-	(36h)
		1	1	↑	VRHN[7:0]								-	(30h)
		1	1	↑	-	-	VRMP[5:0]						-	(2Bh)
		1	1	↑	-	-	VRMN[5:0]						-	(24h)
		1	1	↑	-	APF_EN	DD_TU	VPNL_EN	-	-	PCCS[1:0]		-	(42h)
		1	1	↑	-	DC86_DIV[3:0]				XDK1	XDK0	AUTO_XDK	-	(72h)
B2	SETDISP	0	1	↑	1	0	1	1	0	0	1	0	Set display related register	-
		1	1	↑	-	-	-	-	GON	DTE	D[1:0]		-	(08h)
		1	1	↑	NL[7:0]								-	(C8h)
		1	1	↑	BP[7:0]								-	(00h)
		1	1	↑	FP[7:0]								-	(00h)
		1	1	↑	RTN[7:0]								-	(05h)
		1	1	↑	SAP[3:0]				INIT_DISP	INIT_SET[2:0]			-	(A1h)
		1	1	↑	GEN_ON[7:0]								-	(00h)
		1	1	↑	GEN_OFF[7:0]								-	(FFh)
		1	1	↑	BP_PE [7:0]								-	(00h)
		1	1	↑	FP_PE [7:0]								-	(00h)
		1	1	↑	RTN_PE[7:0]								-	(05h)
		1	1	↑	-	RES_SEL[2:0]			-	-	TGS[1:0]			(20h)
B3	SETRGBIF	0	1	↑	1	0	1	1	0	0	1	1	Set RGB interface related register)	-
		1	1	↑	-	-	-	-	DPL	HSPL	VSPL	EPL		(01h)
B4	SETCYC	0	1	↑	1	0	1	0	0	1	0	0	Set Display waveform cycles	-
		1	1	↑	-	-	NW_PE[2:0]			NW[2:0]			-	(12h)
		1	1	↑	-	-	-	-	SHR[11:8]					(00h)
		1	1	↑	SHR[7:0]									(01h)
		1	1	↑	SPON[7:0]								-	(06h)
		1	1	↑	SPOFF[7:0]								-	(85h)
		1	1	↑	CHR[7:0]								-	(01h)
		1	1	↑	CON[7:0]								-	(0Ch)
		1	1	↑	COFF[7:0]								-	(82h)
		1	1	↑	SHP[3:0]				-	-	-	-		(00h)
		1	1	↑	CPH[3:0]				CCP[3:0]					(01h)
		1	1	↑	N_t1[7:0]									(00h)
		1	1	↑	N_t2[7:0]									(0Ch)
		1	1	↑	N_t3[7:0]									(04h)
		1	1	↑	N_t4[7:0]									(04h)
		1	1	↑	N_t5[7:0]									(08h)
		1	1	↑	N_t6[7:0]									(1Eh)
		1	1	↑	N_t7[7:0]									(09h)
		1	1	↑	N_t8[7:0]									(0Ch)
		1	1	↑	N_t9[7:0]									(0Ch)

		1	1	↑	-	-	-	-	EQT[3:0]						(01h)
B6	SETVCOM (OTPx3)	0	1	↑	1	0	1	1	0	1	1	0	Set VCOM Voltage	-	
		1	1	↑	VCMC[7:0]										(5Eh)
B7	SETTE	0	1	↑	1	0	1	1	0	1	1	1	Set TE Function	-	
		1	1	↑	-	-	-	-	TEI[3:0]						(00h)
		1	1	↑	-	-	-	-	-	TEP[10:8]					(00h)
		1	1	↑	TEP[7:0]										(00h)
B9	SETEXTC	0	1	↑	1	0	1	1	1	0	0	1	Set extended command set	-	
		1	1	↑	EXTC1[7:0]								-		(00h/FFh)
		1	1	↑	EXTC2[7:0]								-		(00h/83h)
		1	1	↑	EXTC3[7:0]								-		(00h/92h)
BA	SETMIPI	0	1	↑	1	1	0	0	1	0	0	1	Set MIPI Control	-	
		1	1	↑	0	0	0	TX_OSC	0	0	LAN_NUM[1:0]		-		(01h)
		1	1	↑	1	0	0	0	0	0	TX_DELAY[1:0]				(82h)
BB	SETOTP	0	1	↑	1	0	1	1	1	0	1	1	Set OTP	-	
		1	1	↑	OTP_MASK[7:0]								-		(00h)
		1	1	↑	-	-	-	-	-	-	OTP_INDEX[9:8]		-		(00h)
		1	1	↑	OTP_INDEX[7:0]								-		(3Bh)
		1	1	↑	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		OTP_PWR_SEL	OTP_PROG	-		(00h)
		1	1	↑	OTP_DATA[7:0]								OTP read / write		(xxh)
BF	SETPTBA	0	1	↑	1	1	0	0	0	0	1	0	Set PTBA mode		
		1	1	↑	0	0	0	0	0	1	0	1			(05h)
		1	1	↑	PTBA[23:16]										(60h)
		1	1	↑	PTBA[15:8]										(04h)
		1	1	↑	PTBA[7:0]										(00h)
C2	SETDISMO	0	1	↑	1	1	0	0	0	0	1	0	Set display mode		
		1	1	↑	-	-	-	-	RM	-	DM[1:0]				(00h)
C3	SETID (OTPx3)	0	1	↑	1	1	0	0	0	0	1	1	Set ID	-	
		1	1	↑	ID1[7:0]								-		(00h)
		1	1	↑	ID2[7:0]								-		(00h)
		1	1	↑	ID3[7:0]								-		(00h)
C4	SETDDB	0	1	↑	1	1	0	0	0	1	0	0	Set DDB	-	
		1	1	↑	DDB1[7:0]								-		(00h)
		1	1	↑	DDB2[7:0]								-		(00h)
		1	1	↑	DDB3[7:0]								-		(00h)
		1	1	↑	DDB4[7:0]								-		(00h)
C9	SETCABC	0	1	↑	1	1	0	0	1	0	0	1	Set CABC Control	-	
		1	1	↑	-	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS (1)	SEL_BLDUTY (1)			(2Fh)
		1	1	↑	PWM_PERIOD[7:0]								-		(2Bh)
		1	1	↑	CABC_FSYNC	DIM_FRAME[6:0]									(1Eh)
		1	1	↑	CABC_STEP[7:0]										(1Eh)
		1	1	↑	CABC_CLKEN[7:0]										(00h)
		1	1	↑	CABC_DD	SAVEPOWER[6:0]									(00h)
		1	1	↑	MEAN_OFFSET[7:0]								-		(00h)
		1	1	↑	-	-	-	-	CABC_FLM[3:0]				-		(01h)
		1	1	↑	-	-	EN_DIM_MIX	EN_COST_MEAN	EN_COST	EN_NLN_GAIN	EN_JUDGE	EN_TEMP	-		(3Eh)
CA	SETCABCGAIN	0	1	↑	1	1	0	0	1	0	1	0	Set CABC related registe	-	
		1	1	↑	0	DBG0[6:0]							-		(40h)
		1	1	↑	0	DBG1[6:0]							-		(3Ch)
		1	1	↑	0	DBG2[6:0]							-		(38h)
		1	1	↑	0	DBG3[6:0]							-		(34h)
		1	1	↑	0	DBG4[6:0]							-		(33h)
		1	1	↑	0	DBG5[6:0]							-		(32h)
		1	1	↑	0	DBG6[6:0]							-		(2bh)
		1	1	↑	0	DBG7[6:0]							-		(24h)

		1	1	↑	0	DBG8[6:0]								-	(22h)
CC	SETPANEL	0	1	↑	1	1	0	1	1	1	0	0		Set panel related register	
		1	1	↑	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANE	BGR_PANEL		-	(02h)
D4	SETGIPEQ	0	1	↑	1	1	0	1	0	1	0	0		Set EQ function	
		1	1	↑	0	0	0	0	EQ_GR	EG_GF	0	0		-	(0Ch)
D5	SETGCKEQ	0	1	↑	1	1	0	1	0	1	0	1		Set GCK EQ function	
		1	1	↑	0	0	0	0	0	0	0	0			(00h)
		1	1	↑	0	0	0	0	0	0	0	0			(00h)
		1	1	↑	EQ_DELAY[7:0]										(08h)
D8	SETRGBCYC	0	1	↑	1	1	0	1	1	0	0	0		Set RGB/Video cycle	
		1	1	↑	-	-	NW_PE[2:0]			NW[2:0]				-	(12h)
		1	1	↑	-	-	-	-	SHR[11:8]					-	(00h)
		1	1	↑	SHR[7:0]									-	(03h)
		1	1	↑	SPON[7:0]									-	(06h)
		1	1	↑	SPOFF[7:0]									-	(85h)
		1	1	↑	CHR[7:0]									-	(03h)
		1	1	↑	CON[7:0]									-	(0Ch)
		1	1	↑	COFF[7:0]									-	(82h)
		1	1	↑	SHP[3:0]				-	-	-	-		-	(00h)
		1	1	↑	CPH[3:0]				CCP[3:0]					-	(01h)
		1	1	↑	N_t1[7:0]									-	(00h)
		1	1	↑	N_t2[7:0]									-	(0Ch)
		1	1	↑	N_t3[7:0]									-	(04h)
		1	1	↑	N_t4[7:0]									-	(04h)
		1	1	↑	N_t5[7:0]									-	(08h)
		1	1	↑	N_t6[7:0]									-	(1Eh)
		1	1	↑	N_t7[7:0]									-	(09h)
		1	1	↑	N_t8[7:0]									-	(0Ch)
		1	1	↑	N_t9[7:0]									-	(0Ch)
		1	1	↑	-	-	-	-	EQT[3:0]					-	(01h)
E0	SETRGAMMA	0	1	↑	1	1	1	0	0	0	0	0		Set Red Gamma Curve Related Setting	
		1	1	↑	-	-	R_VRP0[5:0]							-	(04h)
		1	1	↑	-	-	R_VRP1[5:0]							-	(0Ch)
		1	1	↑	-	-	R_VRP2[5:0]							-	(0Dh)
		1	1	↑	-	-	R_VRP3[5:0]							-	(0Ah)
		1	1	↑	-	-	R_VRP4[5:0]							-	(15h)
		1	1	↑	-	-	R_VRP5[5:0]							-	(21h)
		1	1	↑	-	R_PRP0[6:0]								-	(0Dh)
		1	1	↑	-	R_PRP1[6:0]								-	(19h)
		1	1	↑			-	R_PKP0[4:0]						-	(06h)
		1	1	↑	-	-	-	R_PKP1[4:0]						-	(0Ch)
		1	1	↑	-	-	-	R_PKP2[4:0]						-	(0Fh)
		1	1	↑	-	-	-	R_PKP3[4:0]						-	(13h)
		1	1	↑	-	-	-	R_PKP4[4:0]						-	(16h)
		1	1	↑	-	-	-	R_PKP5[4:0]						-	(14h)
		1	1	↑	-	-	-	R_PKP6[4:0]						-	(15h)
		1	1	↑	-	-	-	R_PKP7[4:0]						-	(0Dh)
		1	1	↑	-	-	-	R_PKP8[4:0]						-	(13h)
		1	1	↑	-	-	R_VRN0[5:0]							-	(04h)
		1	1	↑	-	-	R_VRN1[5:0]							-	(0Ch)
		1	1	↑	-	-	R_VRN2[5:0]							-	(0Dh)
		1	1	↑	-	-	R_VRN3[5:0]							-	(0Ah)
		1	1	↑	-	-	R_VRN4[5:0]							-	(15h)
		1	1	↑	-	-	R_VRN5[5:0]							-	(21h)
		1	1	↑	-	R_PRN0[6:0]								-	(0Dh)
		1	1	↑	-	R_PRN1[6:0]								-	(19h)
		1	1	↑	-	-	-	R_PKN0[4:0]						-	(06h)
		1	1	↑	-	-	-	R_PKN1[4:0]						-	(0Ch)
		1	1	↑	-	-	-	R_PKN2[4:0]						-	(0Fh)

		1	1	↑	-	-	-	R_PKN3[4:0]					-	**(13h)**
		1	1	↑	-	-	-	R_PKN4[4:0]					-	**(16h)**
		1	1	↑	-	-	-	R_PKN5[4:0]					-	**(14h)**
		1	1	↑	-	-	-	R_PKN6[4:0]					-	**(15h)**
		1	1	↑	-	-	-	R_PKN7[4:0]					-	**(0Dh)**
		1	1	↑	-	-	-	R_PKN8[4:0]					-	**(13h)**
E1	SETGGAMMA	0	1	↑	1	1	1	0	0	0	0	1	Set Green Gamma Curve Related Setting	-
		1	1	↑	-	-	G_VRP0[5:0]						-	**(04h)**
		1	1	↑	-	-	G_VRP1[5:0]						-	**(0Ch)**
		1	1	↑	-	-	G_VRP2[5:0]						-	**(0Dh)**
		1	1	↑	-	-	G_VRP3[5:0]						-	**(0Ah)**
		1	1	↑	-	-	G_VRP4[5:0]						-	**(15h)**
		1	1	↑	-	-	G_VRP5[5:0]						-	**(21h)**
		1	1	↑	-	G_PRP0[6:0]							-	**(0Dh)**
		1	1	↑	-	G_PRP1[6:0]							-	**(19h)**
		1	1	↑	-	-	-	G_PKP0[4:0]					-	**(06h)**
		1	1	↑	-	-	-	G_PKP1[4:0]					-	**(0Ch)**
		1	1	↑	-	-	-	G_PKP2[4:0]					-	**(0Fh)**
		1	1	↑	-	-	-	G_PKP3[4:0]					-	**(13h)**
		1	1	↑	-	-	-	G_PKP4[4:0]					-	**(16h)**
		1	1	↑	-	-	-	G_PKP5[4:0]					-	**(14h)**
		1	1	↑	-	-	-	G_PKP6[4:0]					-	**(15h)**
		1	1	↑	-	-	-	G_PKP7[4:0]					-	**(0Dh)**
		1	1	↑	-	-	-	G_PKP8[4:0]					-	**(13h)**
		1	1	↑	-	-	G_VRN0[5:0]						-	**(04h)**
		1	1	↑	-	-	G_VRN1[5:0]						-	**(0Ch)**
		1	1	↑	-	-	G_VRN2[5:0]						-	**(0Dh)**
		1	1	↑	-	-	G_VRN3[5:0]						-	**(0Ah)**
		1	1	↑	-	-	G_VRN4[5:0]						-	**(15h)**
		1	1	↑	-	-	G_VRN5[5:0]						-	**(21h)**
		1	1	↑	-	G_PRN0[6:0]							-	**(0Dh)**
		1	1	↑	-	G_PRN1[6:0]							-	**(19h)**
		1	1	↑	-	-	-	G_PKN0[4:0]					-	**(06h)**
		1	1	↑	-	-	-	G_PKN1[4:0]					-	**(0Ch)**
		1	1	↑	-	-	-	G_PKN2[4:0]					-	**(0Fh)**
		1	1	↑	-	-	-	G_PKN3[4:0]					-	**(13h)**
		1	1	↑	-	-	-	G_PKN4[4:0]					-	**(16h)**
		1	1	↑	-	-	-	G_PKN5[4:0]					-	**(14h)**
		1	1	↑	-	-	-	G_PKN6[4:0]					-	**(15h)**
		1	1	↑	-	-	-	G_PKN7[4:0]					-	**(0Dh)**
		1	1	↑	-	-	-	G_PKN8[4:0]					-	**(13h)**
E2	SETBGAMMA	0	1	↑	1	1	1	0	0	0	1	0	Set Blue Gamma Curve Related Setting	-
		1	1	↑	-	-	B_VRP0[5:0]						-	**(04h)**
		1	1	↑	-	-	B_VRP1[5:0]						-	**(0Ch)**
		1	1	↑	-	-	B_VRP2[5:0]						-	**(0Dh)**
		1	1	↑	-	-	B_VRP3[5:0]						-	**(0Ah)**
		1	1	↑	-	-	B_VRP4[5:0]						-	**(15h)**
		1	1	↑	-	-	B_VRP5[5:0]						-	**(21h)**
		1	1	↑	-	B_PRP0[6:0]							-	**(0Dh)**
		1	1	↑	-	B_PRP1[6:0]							-	**(19h)**
		1	1	↑	-	-	-	B_PKP0[4:0]					-	**(06h)**
		1	1	↑	-	-	-	B_PKP1[4:0]					-	**(0Ch)**
		1	1	↑	-	-	-	B_PKP2[4:0]					-	**(0Fh)**
		1	1	↑	-	-	-	B_PKP3[4:0]					-	**(13h)**
		1	1	↑	-	-	-	B_PKP4[4:0]					-	**(16h)**
		1	1	↑	-	-	-	B_PKP5[4:0]					-	**(14h)**
		1	1	↑	-	-	-	B_PKP6[4:0]					-	**(15h)**
		1	1	↑	-	-	-	B_PKP7[4:0]					-	**(0Dh)**
		1	1	↑	-	-	-	B_PKP8[4:0]					-	**(13h)**
		1	1	↑	-	-	B_VRN0[5:0]						-	**(04h)**
		1	1	↑	-	-	B_VRN1[5:0]						-	**(0Ch)**
		1	1	↑	-	-	B_VRN2[5:0]						-	**(0Dh)**

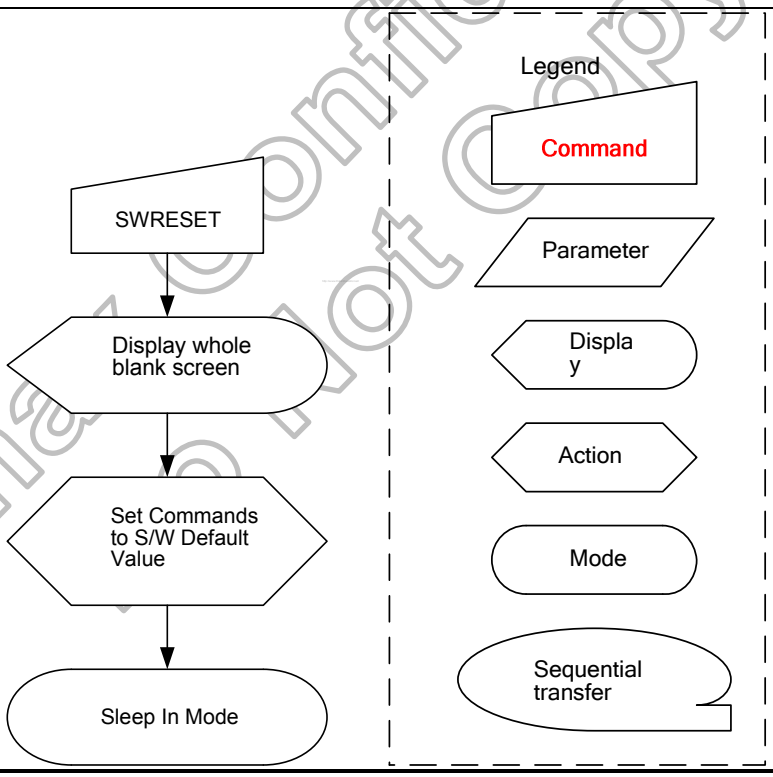
		1	1	↑	-	-	B_VRN3[5:0]							-	**(0Ah)**
		1	1	↑	-	-	B_VRN4[5:0]							-	**(15h)**
		1	1	↑	-	-	B_VRN5[5:0]							-	**(21h)**
		1	1	↑	-	B_PRN0[6:0]								-	**(0Dh)**
		1	1	↑	-	B_PRN1[6:0]								-	**(19h)**
		1	1	↑	-	-	-	B_PKN0[4:0]						-	**(06h)**
		1	1	↑	-	-	-	B_PKN1[4:0]						-	**(0Ch)**
		1	1	↑	-	-	-	B_PKN2[4:0]						-	**(0Fh)**
		1	1	↑	-	-	-	B_PKN3[4:0]						-	**(13h)**
		1	1	↑	-	-	-	B_PKN4[4:0]						-	**(16h)**
		1	1	↑	-	-	-	B_PKN5[4:0]						-	**(14h)**
		1	1	↑	-	-	-	B_PKN6[4:0]						-	**(15h)**
		1	1	↑	-	-	-	B_PKN7[4:0]						-	**(0Dh)**
		1	1	↑	-	-	-	B_PKN8[4:0]						-	**(13h)**
E3	SETCHEMODE	0	1	↑	1	1	1	0	0	0	1	1		Set color enhancement mode	
		1	1	↑	-	-	SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]				**(00h)**
E9	SETOTPKEY	0	1	↑	1	1	1	0	1	0	0	1		-	
		1	1	↑	OTP_KEY0[7:0]									-	**(00/AAh)**
		1	1	↑	OTP_KEY1[7:0]									-	**(00/55h)**
F4	GETHXID	0	1	↑	1	1	1	1	0	1	0	0		Get Himax ID code	
		1	↑	1	Himax ID[7:0]									-	**(92h)**
F7	GETDB	0	1	↑	1	1	1	1	0	1	1	1		Get DB[7:0] status	
		1	↑	1	DB[7:0]									-	**-**

6.2 Command description

6.2.1 NOP (00h)

00H	NOP (No Operation)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.												
Restriction	-												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Default	N/A												
Flow Chart	-												

6.2.2 Software reset (01h)

01H	SWRESET (Software Reset)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command It will be necessary to wait 5msec before sending new command following software reset.												
Restriction	The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Default	N/A												
Flow Chart													

6.2.3 Read Display Identification Information (04h)

04H	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	0	04
1st parameter	1	↑	1	-	ID1[7:0]								xx
2nd parameter	1	↑	1	-	ID2[7:0]								xx
3rd parameter	1	↑	1	-	ID3[7:0]								xx

Description

This read byte returns 24-bit display identification information. The 1st Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX. The 2nd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6..0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value V[7:0]	Version	Changes
80h	--	--
81h	--	--
82h	--	--
83h	--	--
84h	--	--
85h	--	--

The 3rd parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.

Restriction

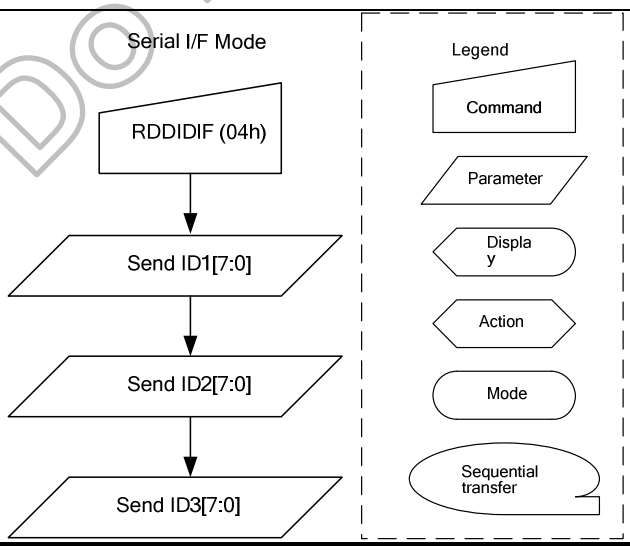
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default Value
Power On Sequence	OTP Value
S/W Reset	OTP Value

Flow Chart



6.2.4 RDNUMPE: Read number of the parity errors (05h)

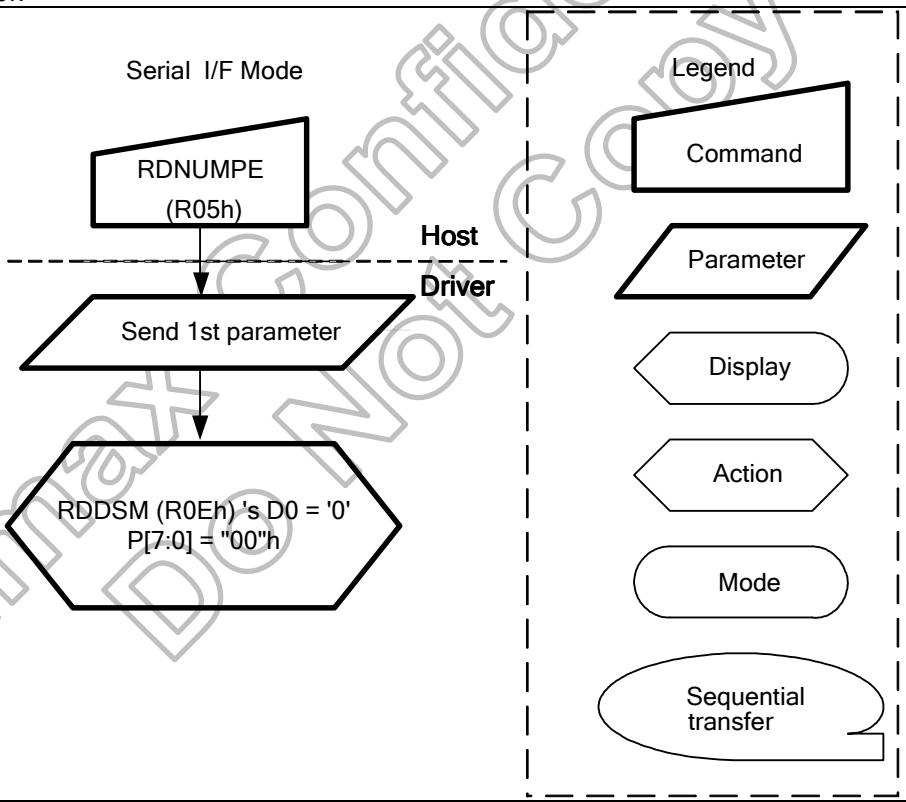
05H	RDNUMPE (Read Number of the Parity Errors)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	1	05
1st parameter	1	↑	1	-	P7	P6	P5	P4	P3	P2	P1	P0	xx
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the parameter information (= The read function is completed).												
Restriction	SETEXTC turn on to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default: P[7:0] = 0x00h

Flow Chart



6.2.5 Read Display Status (09h)

09H	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	0	1	09
1st parameter	1	↑	1	-	D[31:24]								xx
2nd parameter	1	↑	1	-	D[23:16]								xx
3rd parameter	1	↑	1	-	D[15:8]								xx
4th parameter	1	↑	1	-	D[7:0]								xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D31	Booster Voltage Status	
D30	Page Address Order	
D29	Column Address Order	
D28	Page/Column Order	
D27	Display Device Line Refresh Order	
D26	RGB/BGR Order	
D25	Display Data Latch Data Order	
D24	Source san sequence	
D23	Gate san sequence	
D22	Interface Colour Pixel Format Definition	
D21		
D20		
D19	Idle Mode On/Off	
D18	Partial Mode On/Off	
D17	Sleep In/Out	
D16	Display Normal Mode On/Off	
D15	Vertical Scrolling Status	
D14	Horizontal Scrolling Status	Set to '0'
D13	Inversion Status	
D12	All Pixels On	
D11	All Pixels Off	
D10	Display On/Off	
D9	Tearing Effect Line On/Off	
D8	Gamma Curve Selection	
D7		
D6		
D5	Tearing Effect Output Line Mode	
D4	Horizontal Sync. (HSYNC, DPI I/F)	
D3	Vertical Sync. (VSYNC, DPI I/F)	
D2	Pixel Clock (DCK, DPI I/F)	
D1	Data Enable (ENABLE, DPI I/F)	
D0	Parity Error on DSI	

Bit Values are explained overleaf.
Bit D31 – Booster Voltage Status
'0' = Booster Off.
'1' = Booster On.
Bit D30 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit D29 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit D28 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Rotation (When MADCTL B5='1').
Bit D27 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit D26 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').

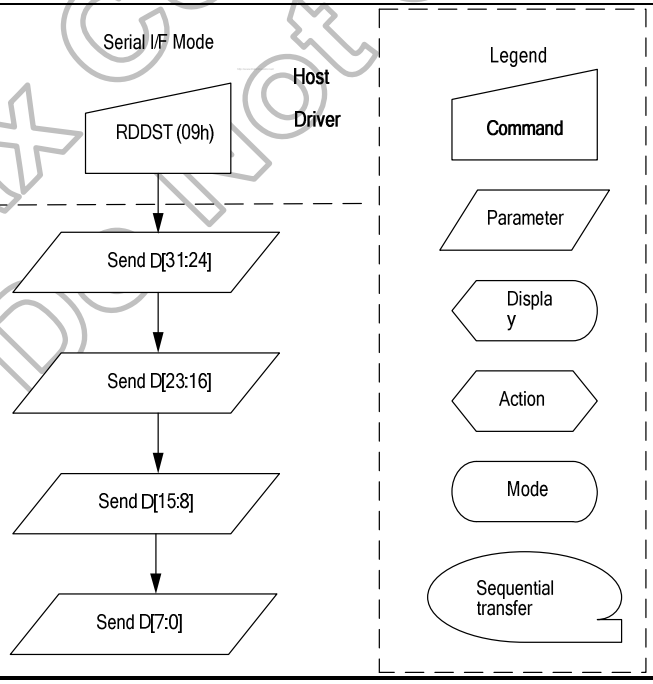
Bit D25 – Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit D24 – Source san sequence
'0' = Source output Left to Right (When MADCTL B1='0').
'1' = Source output Right to Left (When MADCTL B1='1').
Bit D23 – Gate san sequence
'0' = Gate output Top to Bottom (When MADCTL B0='0').
'1' = Gate output Bottom to Top (When MADCTL B0='1').
Bits D22, D21, D20 – Interface Colour Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Bit D19 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D18 – Partial Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit D17 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D16 – Display Normal Mode On/Off
'0' = Partial or Scrolling Mode.
'1' = Normal Mode.
Bit D15 – Vertical Scrolling On/Off
'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.
Bit D14 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to '0'
Bit D13 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
Bit D12 – All Pixels On.
'0' = Nornal mode.
'1' = All Pixels On.
Bit D11 – All Pixels Off.
0' = Nornal mode.
'1' = All Pixels Off.
Bit D10 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D9 – Tearing Effect Line On/Off
'0' =Tearing Effect Line Off.
'1' = Tearing Effect On.
Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	Reserved
Gamma Curve 2	0	0	1	Reserved
Gamma Curve 3	0	1	0	Reserved
Gamma Curve 4	0	1	1	Reserved
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

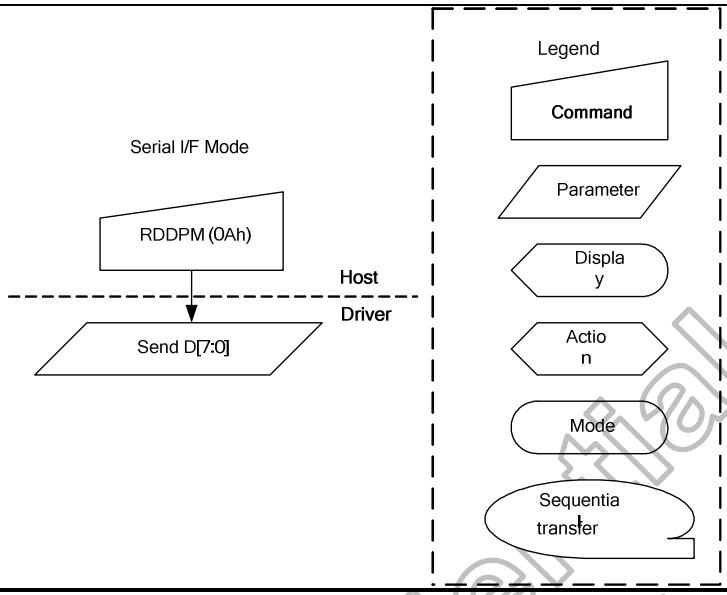
Bit D5 – Tearing Effect Line Output Mode.
'0' = Mode 1, V-Blanking only.

	Bit D4 – Horizontal Sync. (DPI I/F) On/Off,Note 1. '0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High"). Bit D3 – Vertical Sync. (DPI I/F) On/Off,Note 1. '0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High"). Bit D2 – Pixel Clock (PCLK, DPI I/F) On/Off,Note 1. '0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High"). Bit D1 – Data Enable (DE, DPI I/F)) On/Off,Note 1. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0–Parity Error on DSI. '0'=No Parity Error. '1'=Parity Error. **Note:** This bit indicates current status of the line when this command has been sent.
Restriction	
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes
Default	Status / Default Value Power On Sequence: See description S/W Reset: See description
Flow Chart	

6.2.6 Get_power_mode (0Ah)

<table>
<tr><th rowspan="2">0AH</th><th colspan="13">RDDPM (Read Display Power Mode)</th></tr>
<tr><th>D/CX</th><th>RDX</th><th>WRX</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>-</td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td>-</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>-</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>-</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>-</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table>
Bits D7 for future use and are set to ‘0’.
Bit D6 – Idle Mode On/Off
‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.
Bit D5 – Partial Mode On/Off
‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.
Bit D4 – Sleep In/Out
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.
Bit D3 – Display Normal Mode On/Off
‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.
Bit D2 – Display On/Off
‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>Restrictions</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">D[7:0] = 0x08h</td></tr>
</table>

Flow Chart



6.2.7 Read display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	-
D1	Source san sequence	-
D0	Gate san sequence	-

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit D5 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Roration (When MADCTL B5='1').
Note: For Bits D7 to D5, also refer to Section 5.3 MCU to memory write/read direction.
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').
Note: For Bits D4 and D3 also refer to Section 6.2.31 Set_address_mode (36h).
Bit D2 – Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit D1 – Source san sequence
'0' = Source output Left to Right (When MADCTL B1='0').
'1' = Source output Right to Left (When MADCTL B1='1').
Bit D0 – Gate san sequence
'0' = Gate output Top to Bottom (When MADCTL B0='0').

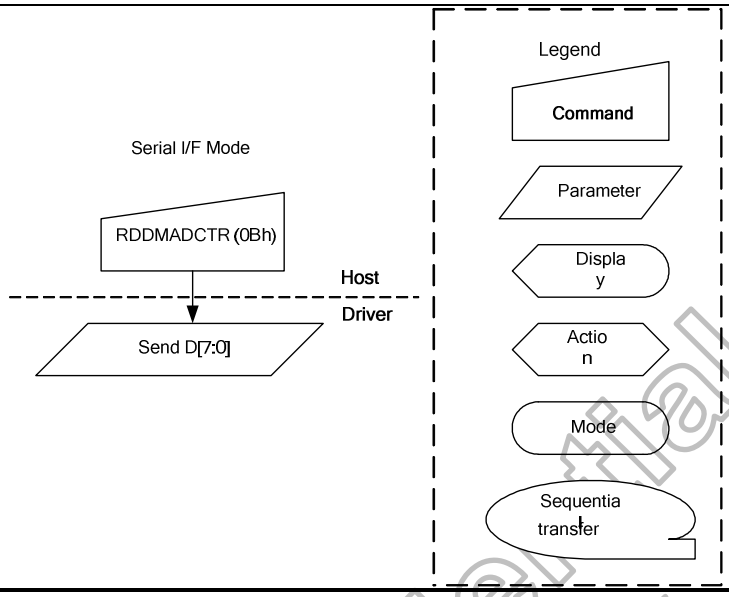
Restrictions: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: D[7:0] = 0x00h

Flow Chart



6.2.8 Get_pixel_format (0Ch)

0CH	RDDCOLMOD (Read Display COLMOD)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	↑	1	-	-	D6	D5	D4	-	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	-
D5		-
D4		-
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format	-
D1		-
D0		-

Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition.
For Setting pixel format, see section 6.2.35 Set_pixel_format (3Ah)".

Interface Colour Format	D6 D2	D5 D1	D4 D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.

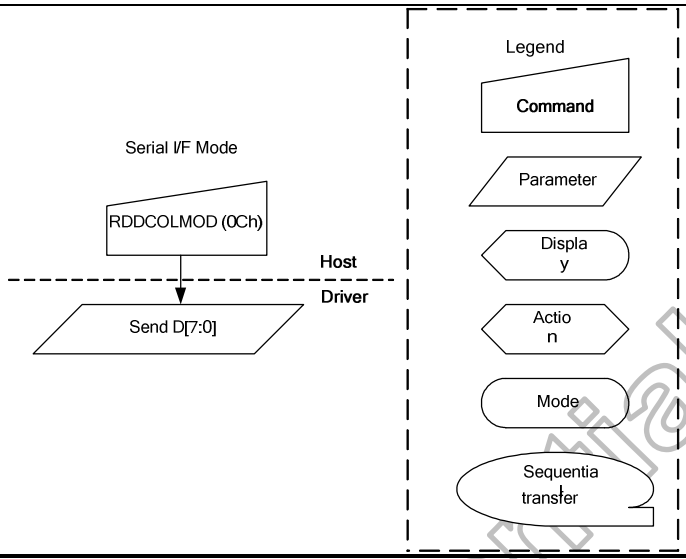
Restrictions: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: D[7:0] = 0x07h

Flow Chart



6.2.9 Get_display_mode (0Dh)

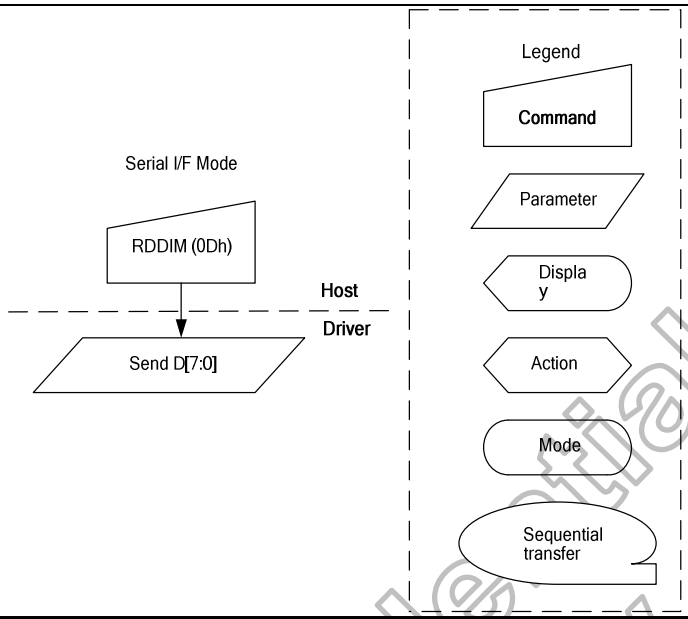
0DH	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off '0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On. Bit D6 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to '0' Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bit D4 – All Pixels On '0' = Normal Display '1' = White Display Bit D3 – All Pixels Off '0' = Normal Display '1' = Black Display Bits D2, D1, D0 – Gamma Curve Selection												
Restrictions	-												
Default	D[7:0] = 0x00h												

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined

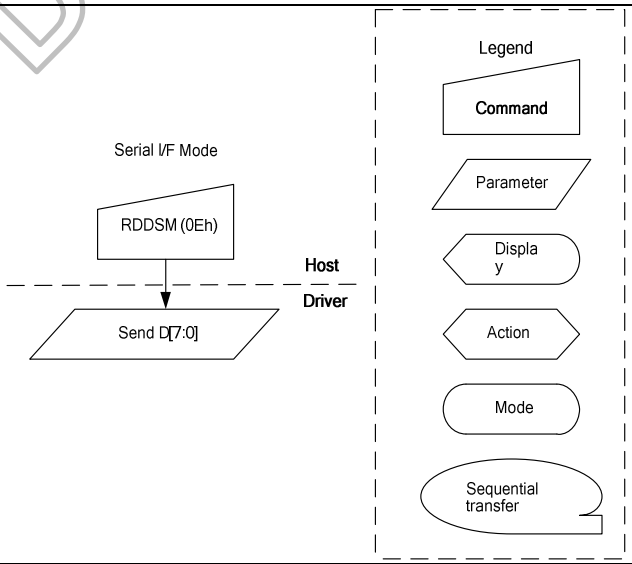
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

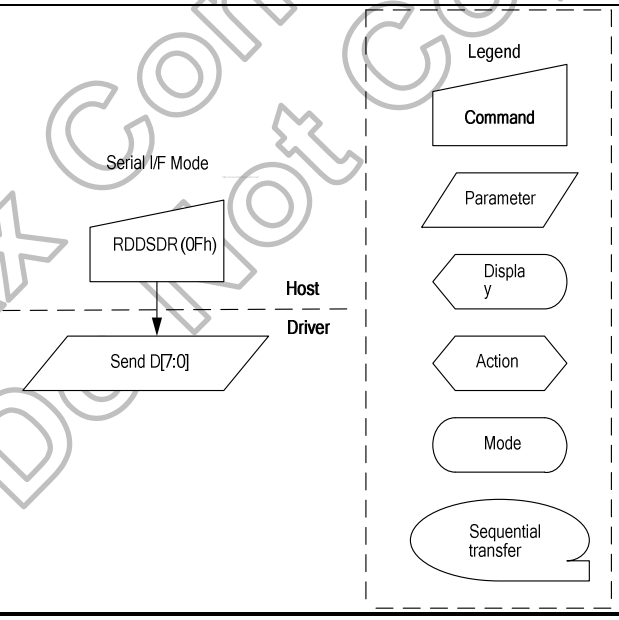
Flow Chart



6.2.10 Get_signal_mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx
Description	T This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 5.5.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. Bit D5 – Horizontal Sync. (RGB I/F) On/Off. '0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High"). Bit D4 – Vertical Sync. (RGB I/F) On/Off. '0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High"). Bit D3 – Pixel Clock (PCLK, RGB I/F) On/Off. '0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High"). Bit D2 – Data Enable (DE, RGB I/F)) On/Off. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0–Parity Error on DSI, see "Read number of the parity errors (05h)". '0'=No Parity Error. '1'=Parity Error. D1 – are for future use and are set to '0'.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

6.2.11 Get_diagnostic_result (0Fh)

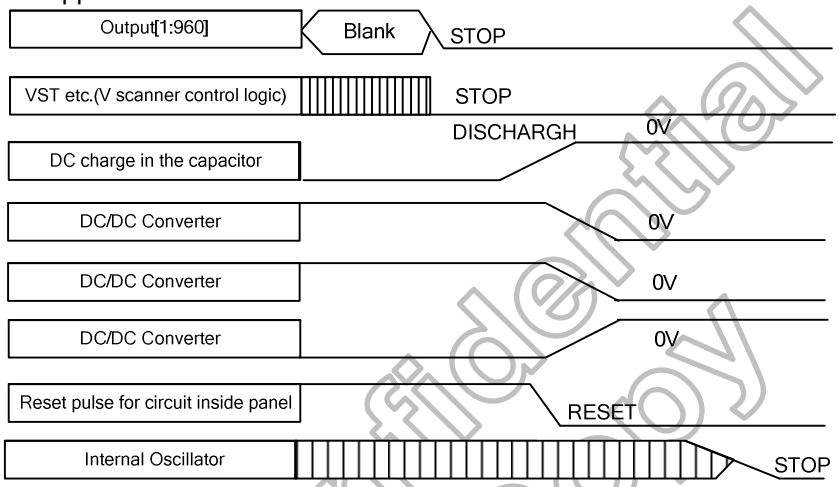
0FH	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	↑	1	-	D7	D6	D5	D4	0	0	0	0	xx
Description	The display module returns the self-diagnostic results following a Sleep Out command. See section 5.15 for a description of the status results. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved Set to '0'.												
Restrictions	-												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In or Booster Off — Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

6.2.12 Enter_sleep_mode (10h)

10H	SLPIN (Sleep In)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER												

Description

This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.



MCU interface and memory are still working and the memory keeps its contents.

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

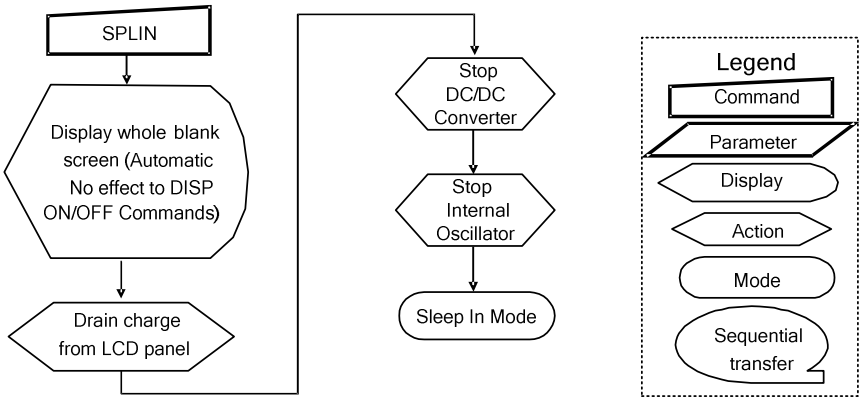
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

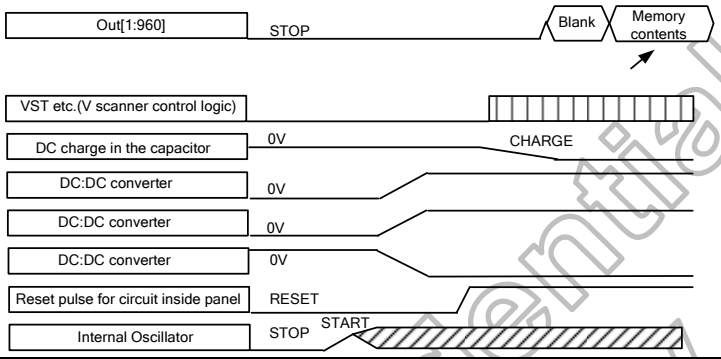
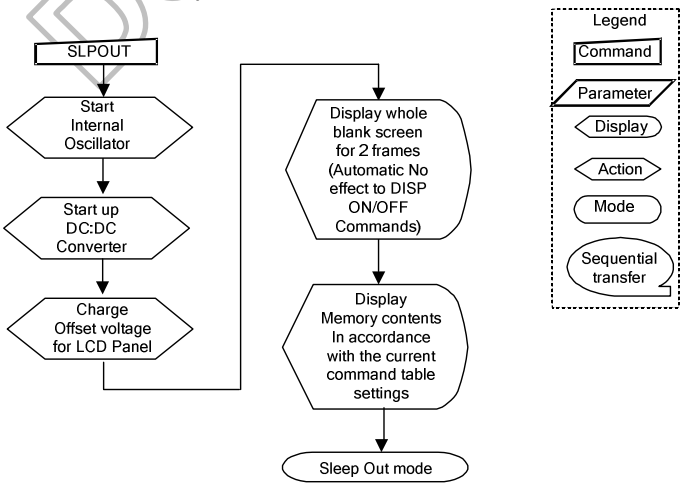
N/A

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



6.2.13 Exit_sleep_omde (11h)

11H	SLPOUT (Sleep Out)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	N/A												
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 												

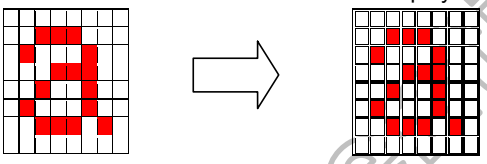
6.2.14 Enter_partial_mode (12h)

12H	PTLON (Partial Mode On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER												
Description	This command turns on partial mode The partial mode window is described by the “Set_partial_area” command (30H). To leave Partial mode, the “Enter_norma_mode” command (13H) should be written.												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	N/A												
Flow Chart	See Partial Area (30h)												

6.2.15 Enter_normal_mode (13h)

13H	NORON (Normal Display Mode On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	N/A												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

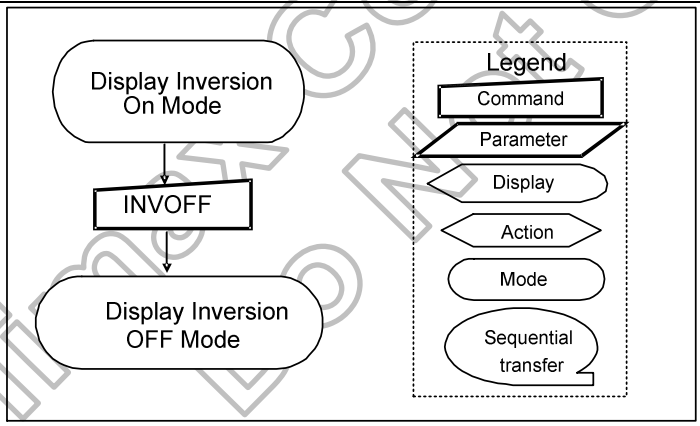
6.2.16 Exit_inversion_mode (20h)

20H	INVOFF (Display Inversion Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	No parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory (Example) Display 												
Restriction	This command has no effect when module is already in inversion off mode.												

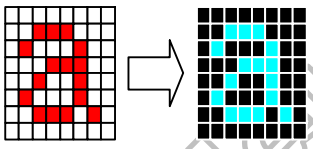
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

Flow Chart:



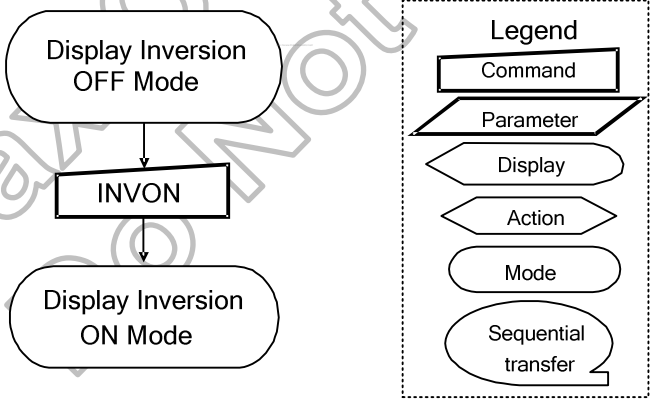
6.2.17 Enter_inversion_mode (21h)

21H	INVON (Display Inversion On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

Flow Chart



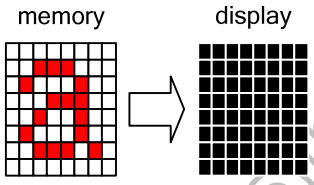
6.2.18 All_Pixel_Off (22h)

22H	ALLPOFF (All Pixel Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	0	22
Parameter	NO PARAMETER												

Description

This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'.
This command makes no change of contents of frame memory.
This command does not change any other status

(Example)



'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.

Restriction

This command has no effect when module is already in inversion on mode.

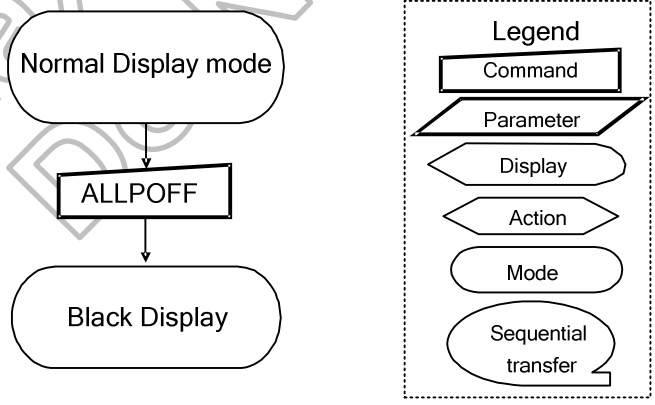
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off

Flow Chart



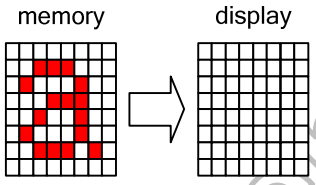
6.2.19 All_Pixel_On (23h)

23H	ALLPON(All Pixel On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	1	1	23
Parameter	NO PARAMETER												

Description

This command turns the display panel white in ‘Sleep out ‘ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



‘All Pixels Off’, ’Normal Display Mode On’ or ’Partial Mode On’ – commands are used to leave this mode. The display is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands.

Restriction

This command has no effect when module is already in inversion on mode.

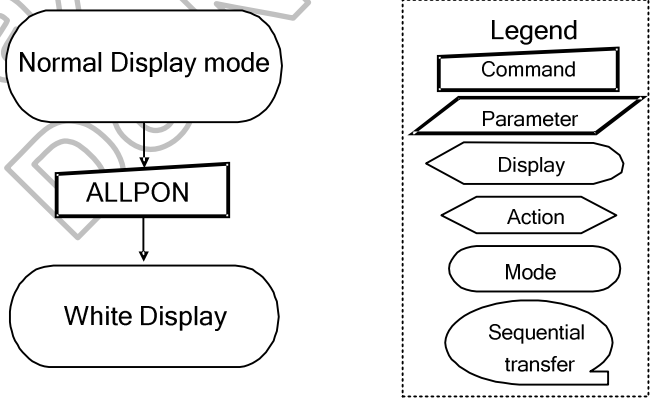
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off

Flow Chart



6.2.20 Set_gamma_curve (26h)

26H	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	1	1	0	26
Parameter	1	1	↑	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1..08

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[7..0]	Parameter	Curve selected
01h	GC0	Gamma Curve 1 (Gamma 2.2)
02h	GC1	Gamma Curve 2 (Gamma 1.8)
04h	GC2	Gamma Curve 3 (Gamma 2.5)
08h	GC3	Gamma Curve 4 (Gamma 1.0)

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

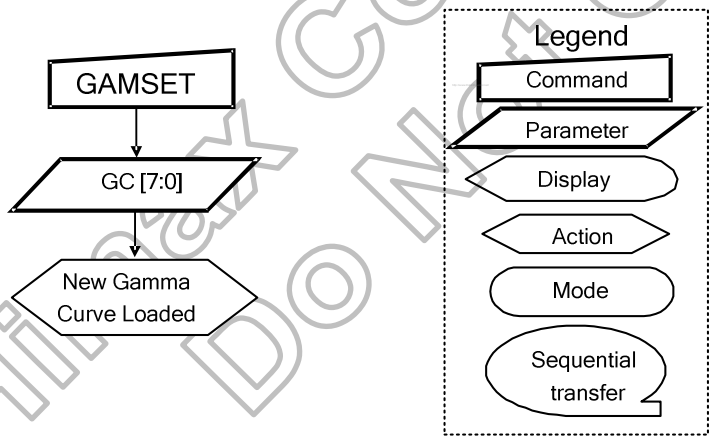
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

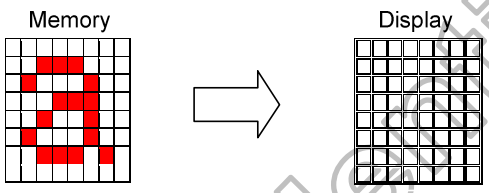
Default

GC[7:0] = 0x01h

Flow Chart



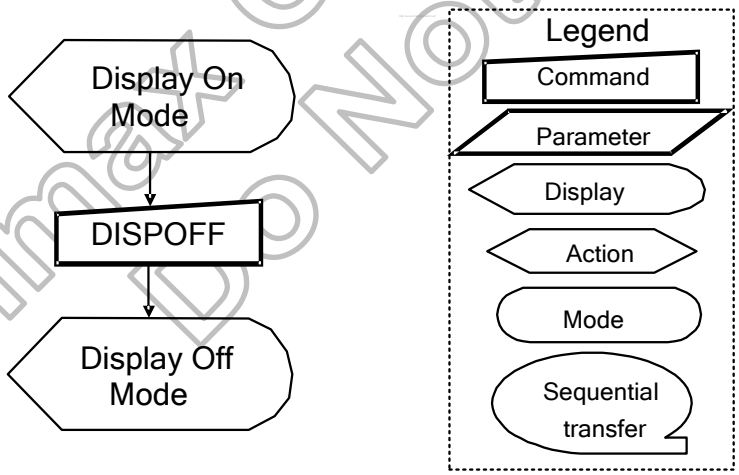
6.2.21 Set_display_off (28h)

28H	DISPOFF (Display Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example 												
Restriction	This command has no effect when module is already in display off mode.												

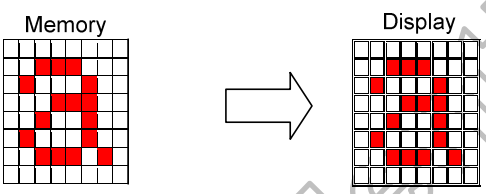
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

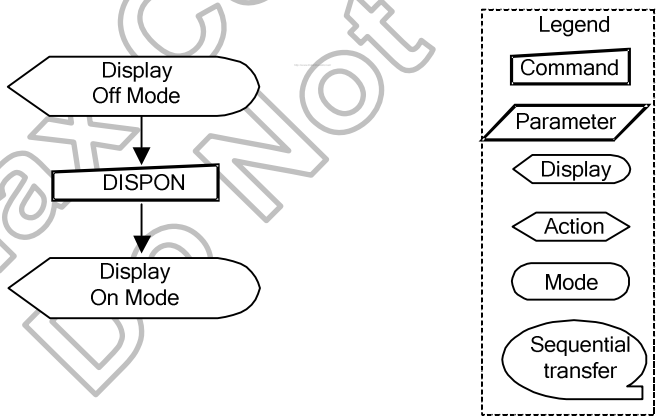
Flow Chart



6.2.22 Set_display_on (29h)

29H	DISPON (Display On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 												
Restriction	This command has no effect when module is already in display on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	N/A
Flow Chart	

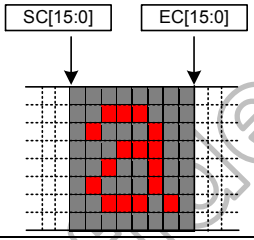
6.2.23 Set_clumn_address (2Ah)

2AH	CASET (Column Address Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00..
2nd parameter	1	1	↑	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Note 1
3rd parameter	1	1	↑	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	00 ..
4th parameter	1	1	↑	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Note 1

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]
The SC[15] and EC[15]-SC[15]+1 must can be divisible by 2.
Note 1: When SC[15:0] or EC[15:0] is greater than horizontal line (when MADCTL's B5=0) or vertical line (when MADCTL's B5=1), data of out of range will be ignored.

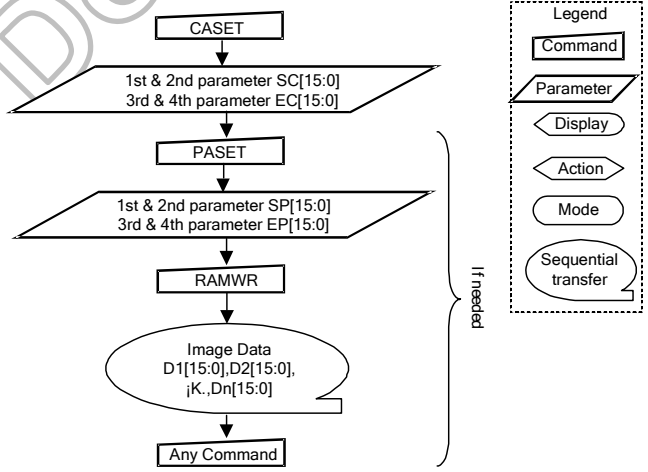
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

RES_SEL[2:0]=000, Resoultion 800RGBx1280: SC[15:0] = 0x0000h, EC[15:0] = 0x031Fh
RES_SEL[2:0]=001, Resoultion 768RGBx1280: SC[15:0] = 0x0000h, EC[15:0] = 0x02FFh
RES_SEL[2:0]=010, Resoultion 720RGBx1280: SC[15:0] = 0x0000h, EC[15:0] = 0x02CFh
RES_SEL[2:0]=011, Resoultion 600RGBx1024: SC[15:0] = 0x0000h, EC[15:0] = 0x0257h

Flow Chart



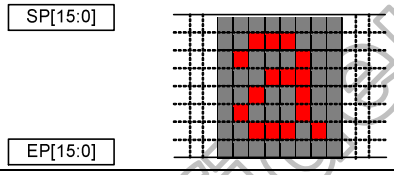
6.2.24 Set_page_address (2Bh)

2BH	PASET (Page Address Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00 ..
2nd parameter	1	1	↑	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Note 1
3rd parameter	1	1	↑	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	00 .. Note 1
4th parameter	1	1	↑	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]
The SP[15] and EP[15]-SP[15]+1 must can be divisible by 2.
Note 1: When SP[15:0] or EP[15:0] is greater than vertical line (When MADCTL's B5=0) or horizontal line (When MADCTL's B5=1), data of out of range will be ignored.

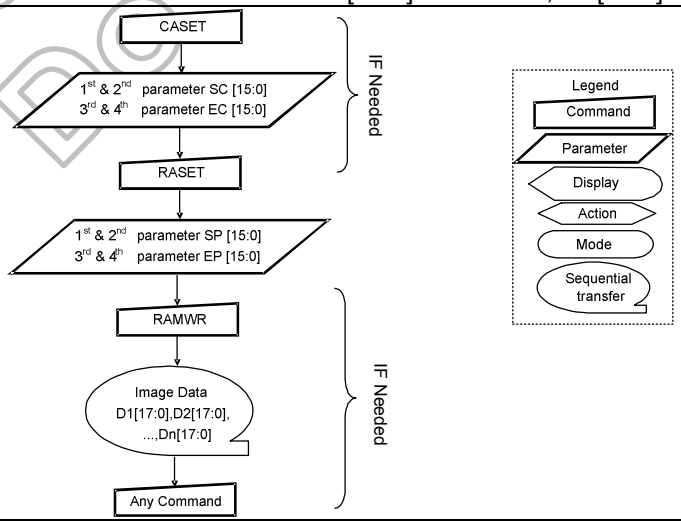
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

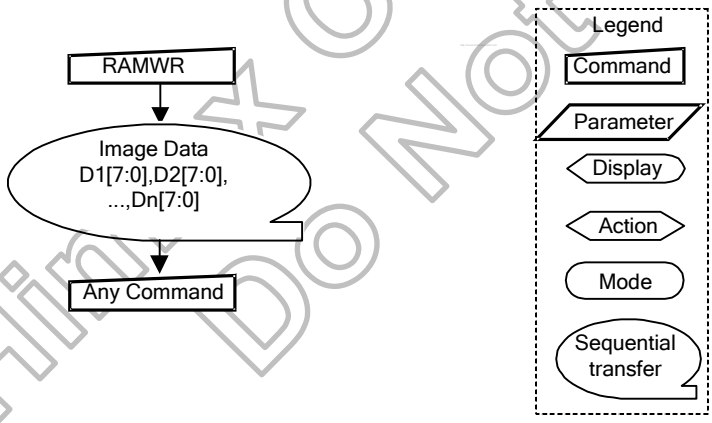
Default

RES_SEL[2:0]=000, Resoultion 800RGBx1280: SP[15:0] = 0x0000h, EP[15:0] = 0x04FFh
RES_SEL[2:0]=001, Resoultion 768RGBx1280: SP[15:0] = 0x0000h, EP[15:0] = 0x04FFh
RES_SEL[2:0]=010, Resoultion 720RGBx1280: SP[15:0] = 0x0000h, EP[15:0] = 0x04FFh
RES_SEL[2:0]=011, Resoultion 600RGBx1024: SP[15:0] = 0x0000h, EP[15:0] = 0x03FFh

Flow Chart



6.2.25 Write_memory_start (2Ch)

2CH	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.												
Restriction	In all colour modes, there is no restriction on length of parameters. The transfer pixel number must can be divisible by 2.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	Contents of memory is set randomly and not cleared.												
Flow Chart													

6.2.26 Raed_memory_start (2Eh)

2EH	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.												
Restriction	In all colour modes, the Frame Read is always 24bit so there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.												

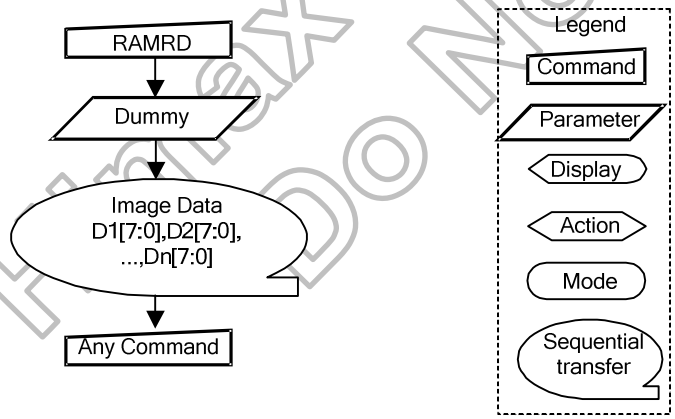
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

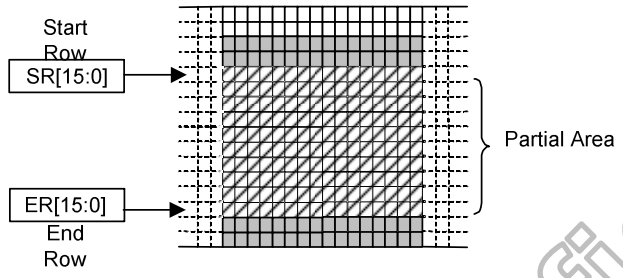
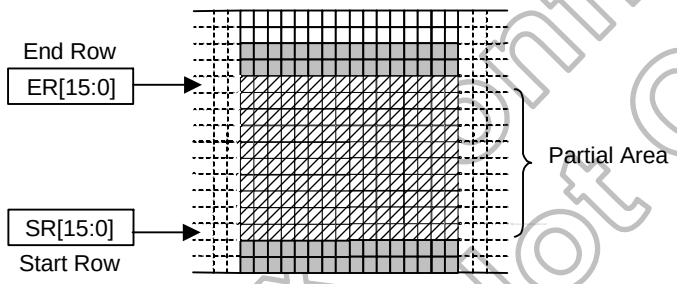
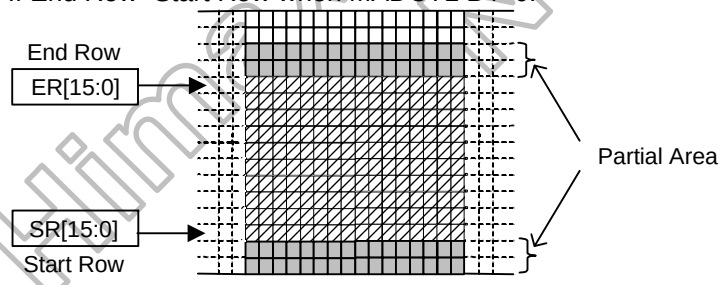
Default

Contents of memory is set randomly and not cleared.

Flow Chart

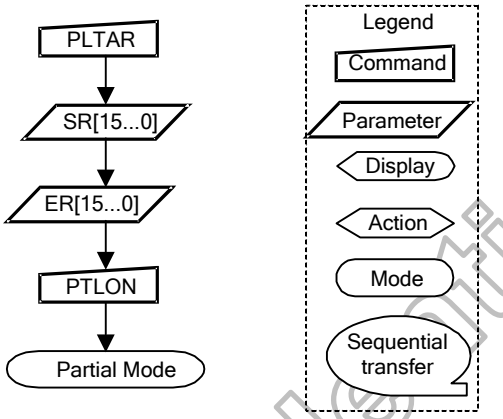
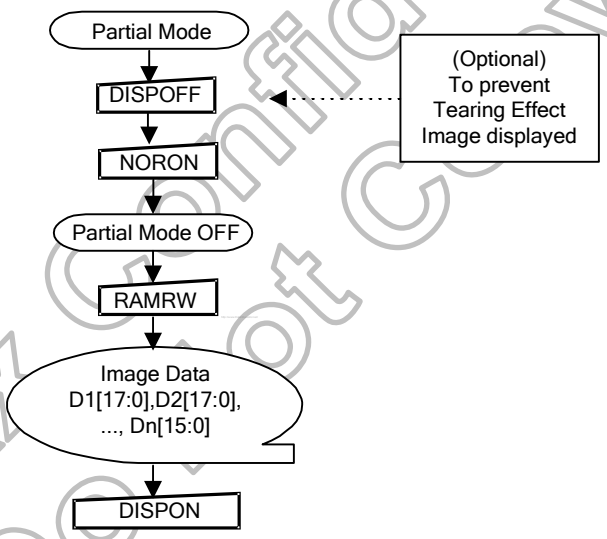


6.2.27 Set_partial_area (30h)

30H	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	xx
2nd parameter	1	1	↑	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	xx
3rd parameter	1	1	↑	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	xx
4th parameter	1	1	↑	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	xx
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-  If End Row = Start Row then the Partial Area will be one row deep.												
Restriction	SR[15..0] and ER[15..0] cannot be greater than horizontal line number.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

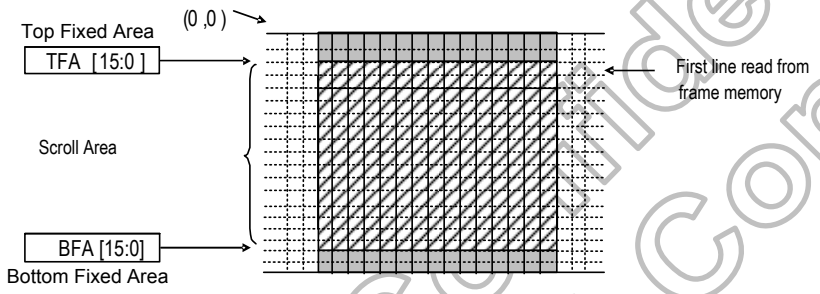
Default	RES_SEL[2:0]=000, Resoultion 800RGBx1280: SR[15:0] = 0x0000h, ER[15:0] = 0x04FFh RES_SEL[2:0]=001, Resoultion 768RGBx1280: SR[15:0] = 0x0000h, ER[15:0] = 0x04FFh RES_SEL[2:0]=010, Resoultion 720RGBx1280: SR[15:0] = 0x0000h, ER[15:0] = 0x04FFh RES_SEL[2:0]=011, Resoultion 600RGBx1024: SR[15:0] = 0x0000h, ER[15:0] = 0x03FFh
Flow Chart	1. To Enter Partial Mode:-  2. To Leave Partial Mode 

6.2.28 Set_scroll_area (33h)

33H	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	xx
2nd parameter	1	1	↑	-	TFA7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA1	TFA0	xx
3rd parameter	1	1	↑	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	xx
4th parameter	1	1	↑	-	VSA7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA1	VSA0	xx
5th parameter	1	1	↑	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	xx
6th parameter	1	1	↑	-	BFA7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA1	BFA0	xx

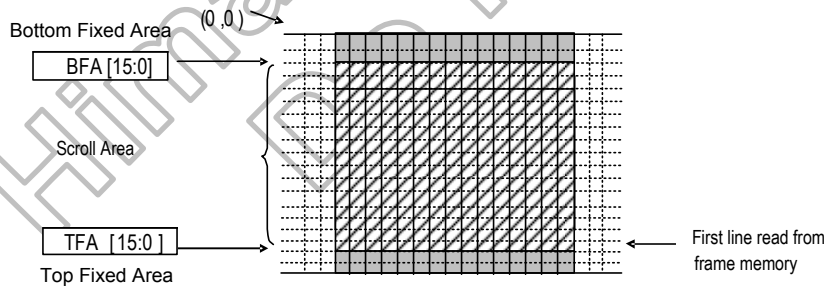
Description

This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When MADCTL B4=1

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction

The condition is (TFA+VSA+BFA)= Vertical line number, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

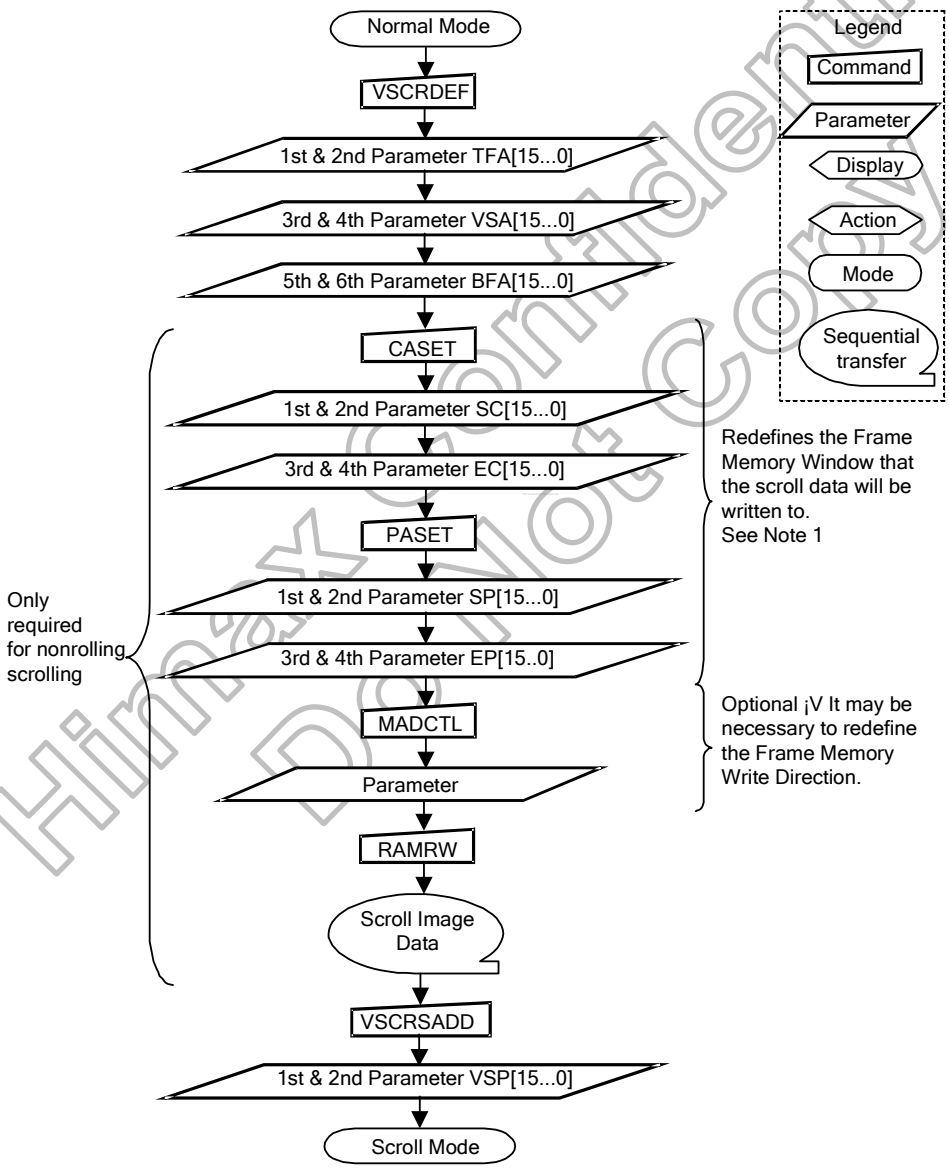
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value		
RES_SEL[2:0]=000, 800RGBx1280	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0500h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=001, 768RGBx1280	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0500h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=010, 720RGBx1280	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0500h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=011, 600RGBx1024	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0400h	BFA[15..0]= 0x0000h

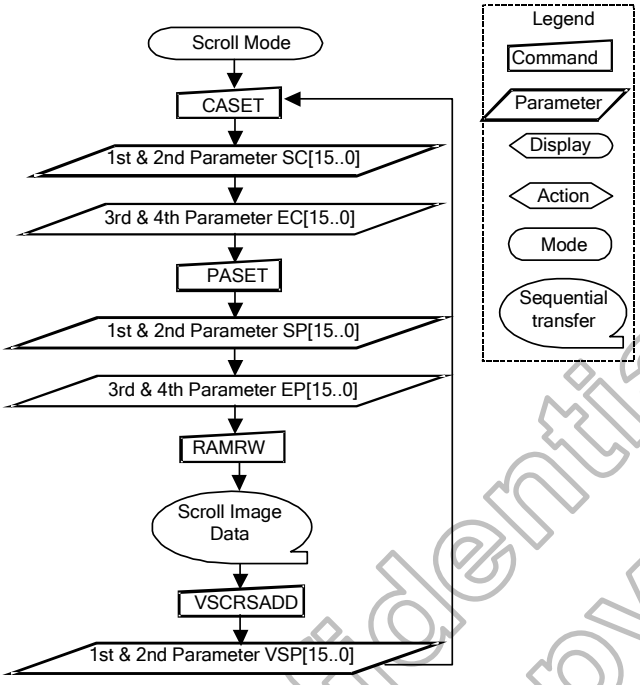
Flow Charts

1.To enter Vertical Scroll Mode:

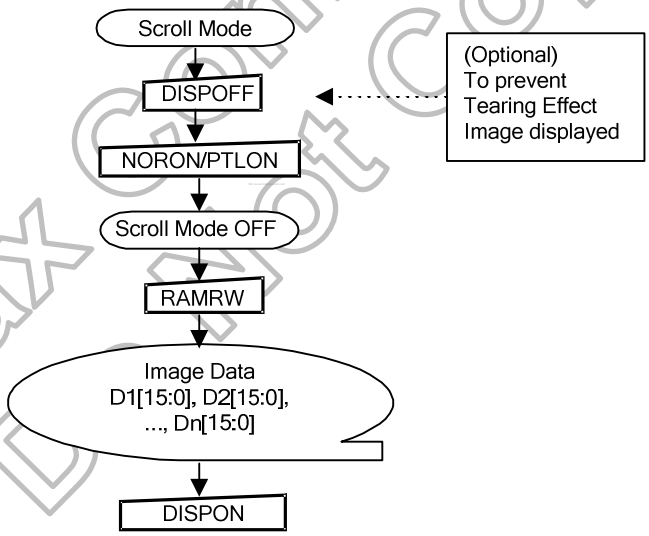


Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:

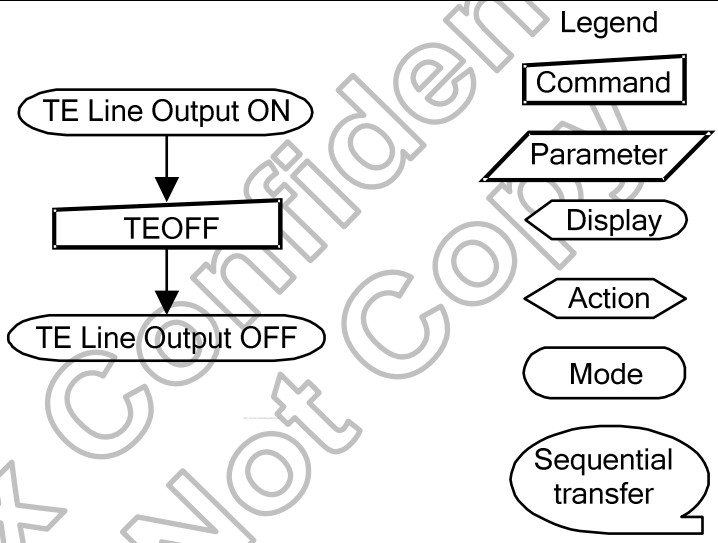


3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

6.2.29 Tearing effect line off (34h)

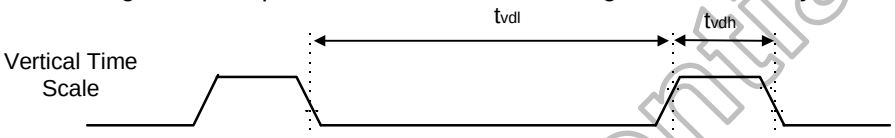
34H	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	OFF												
Flow Chart													

6.2.30 Set_tear_on (35h)

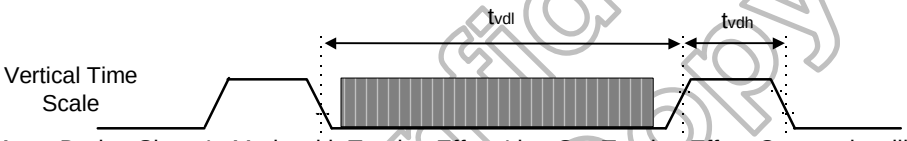
35H	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal
line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

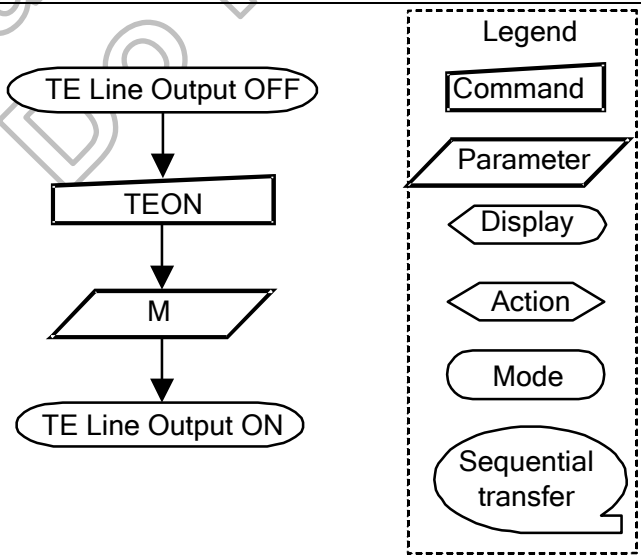
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

OFF

Flow Chart



6.2.31 Set_address_mode (36h)

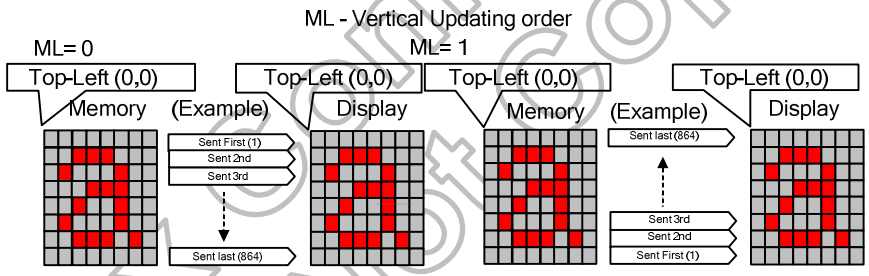
36H	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	-	B7	B6	B5	B4	B3	B2	B1	B0	XX

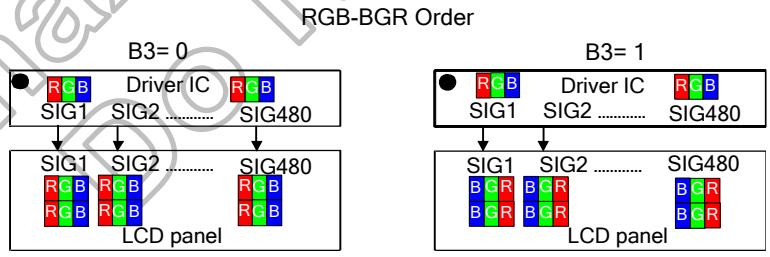
Description

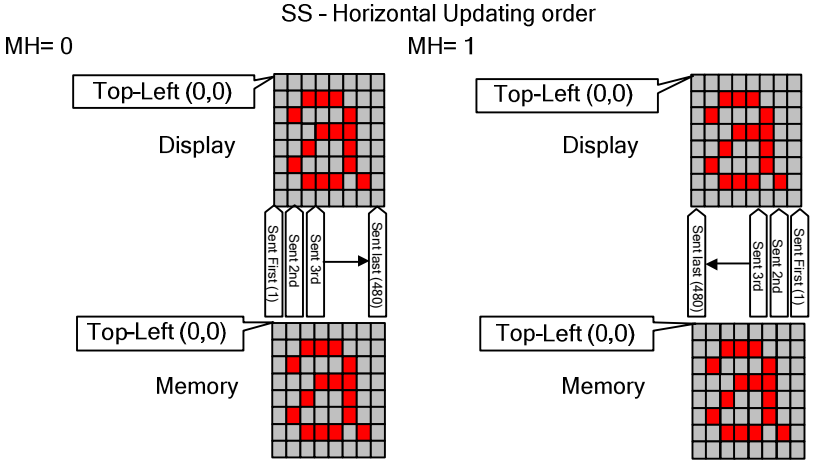
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

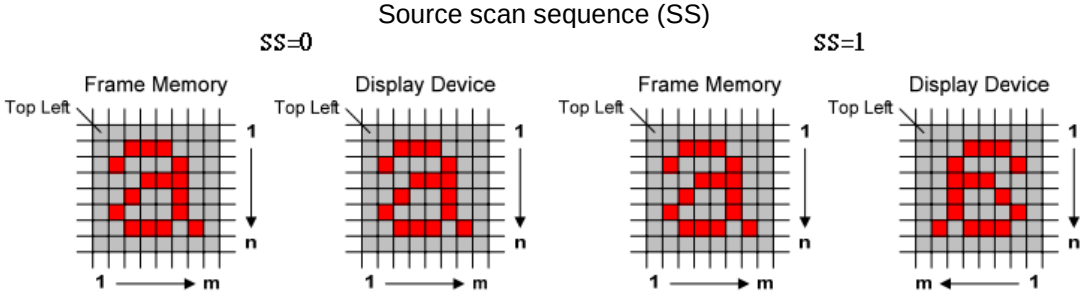
Bit Assignment

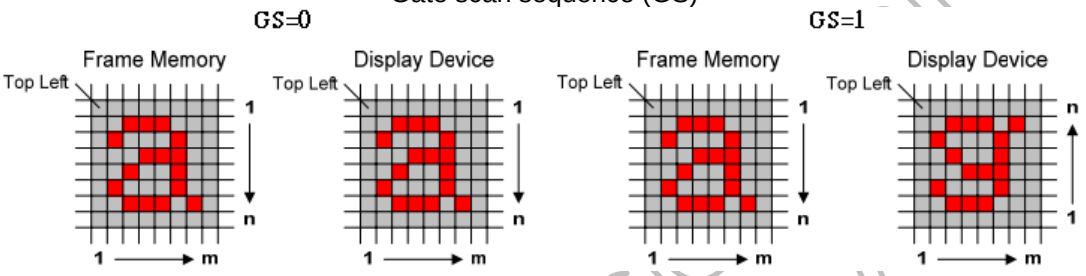
BIT	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2	Horizontal ORDER (MH)	LCD horizontal refresh direction control
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module

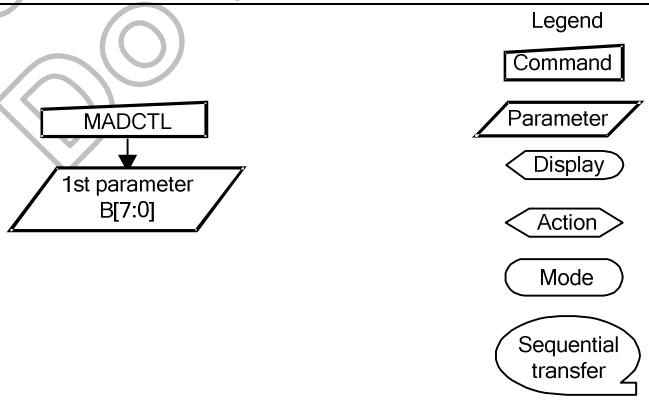






<table>
<tr><td></td><td>
Source scan sequence (SS)


Gate scan sequence (GS)


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default value</th></tr>
<tr><td>Power On Sequence</td><td>B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

6.2.32 Set_scroll_start (37h)

37H	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	00.. 4FF
2nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

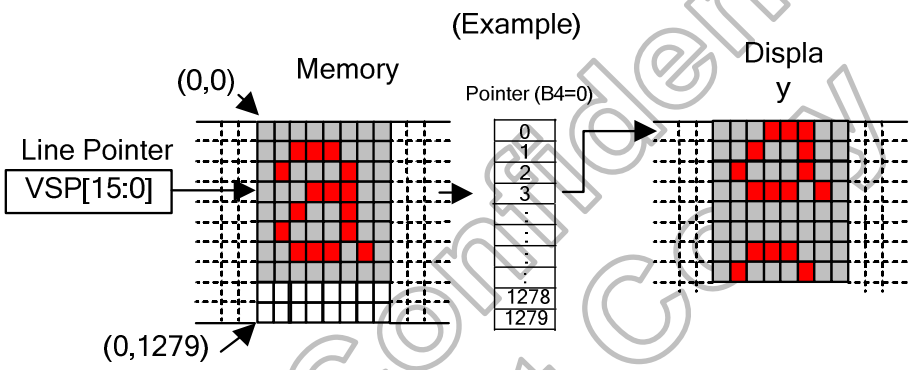
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

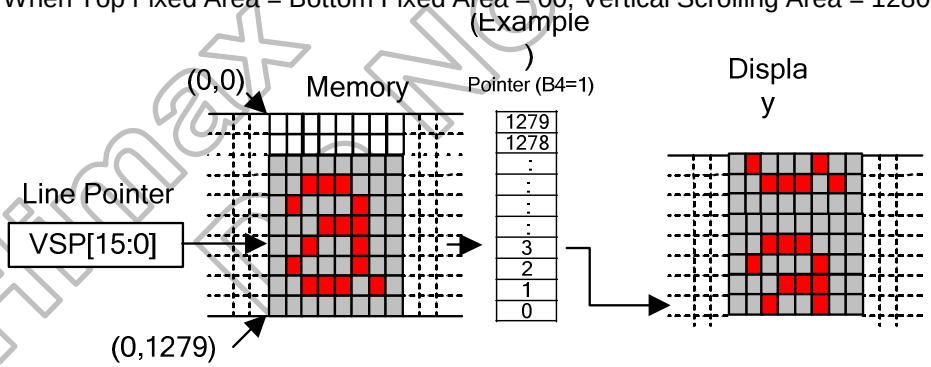
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 1280(DM=10) and



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 1280(DM=10) and



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No

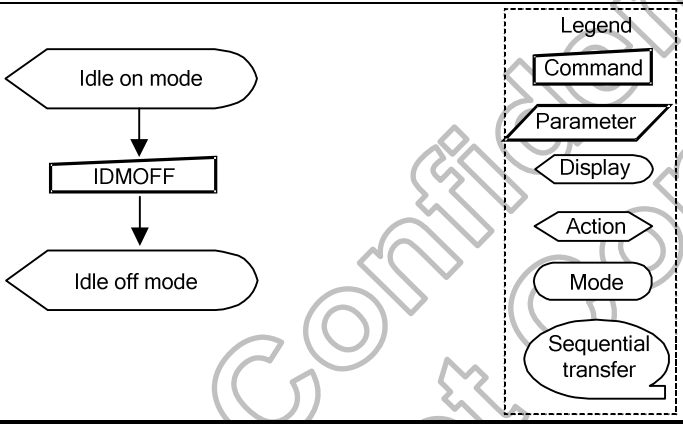
Default

VSP[15:0]= 0x0000h

Flow Chart

See Vertical Scrolling Definition (33h) description.

6.2.33 Idle mode off (38h)

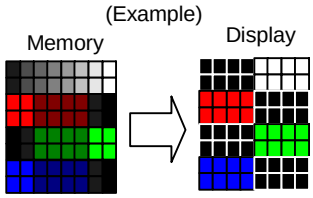
38H	IDMOFF (Idle mode off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	Idle mode is OFF.												
Flow Chart													

6.2.34 Enter_Idle_mode (39h)

39H	IDMON (Idle mode on)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.



Memory contents vs. Display Colour

	R7 - R0	G7 - G0	B7 - B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magent	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X=don't care

Restriction

This command has no effect when module is already in idle on mode.

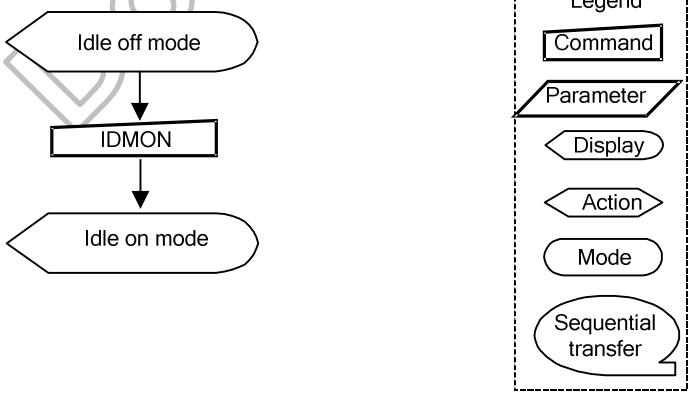
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Idle mode is OFF.

Flow Chart



6.2.35 Set_pixel_format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	-	X	D6	D5	D4	X	D2	D1	D0	XX

Description

This command is used to define the format of RGB picture data.
D6~D4 : DPI Pixel format Definition.
D2~D0 : DBI Pixel format Definition.
The formats are shown in the table:

Pixel Format	D6/D2	D5/D1	D4/D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

If a particular interface, enter DBI or DPI, is not used then the correspondind bits in the parameter returned from the display module undefined.

Restriction

There is no visible effect until the Frame Memory is written to.

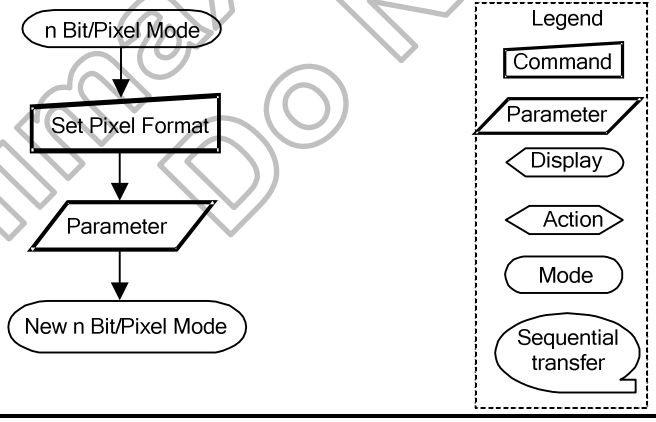
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value
Power On Sequence	24 Bit/Pixel

Flow Chart



6.2.36 Write_memory_contiune (3Ch)

3CH	Write_memory_contiune												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Sending any other command can stop frame Write.
If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

In all colour modes, there is no restriction on length of parameters.
The transfer pixel number must can be divisible by 2.

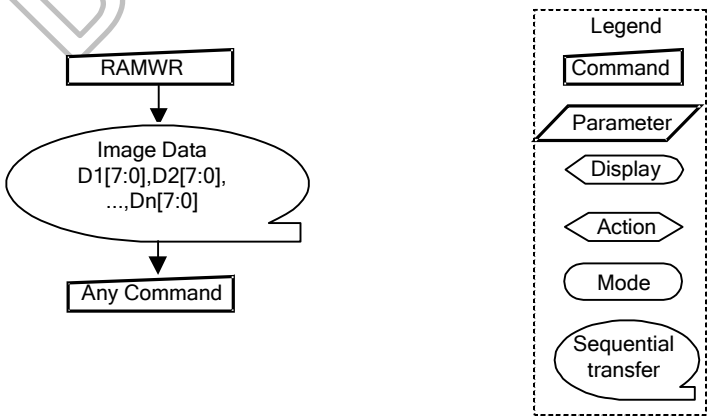
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

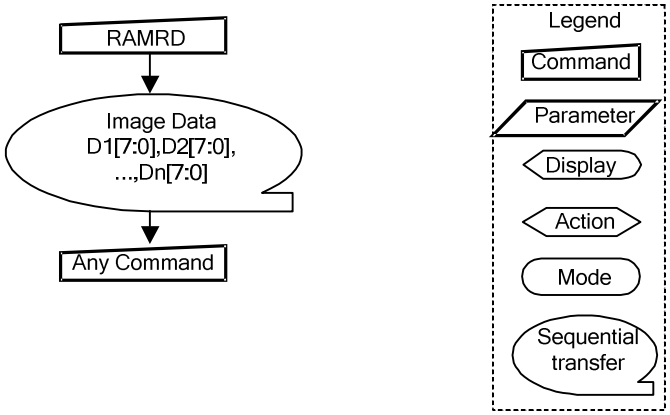
Default

Status	Default value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly

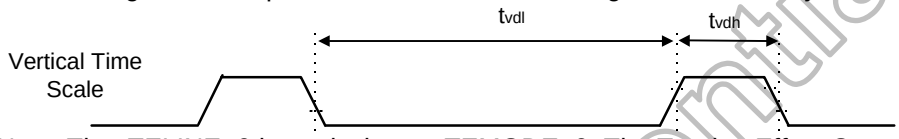
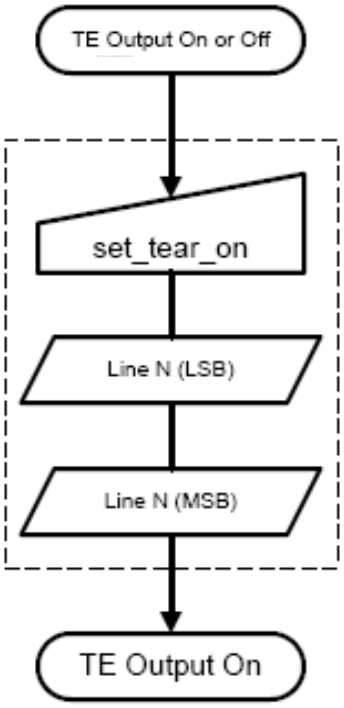
Flow Chart



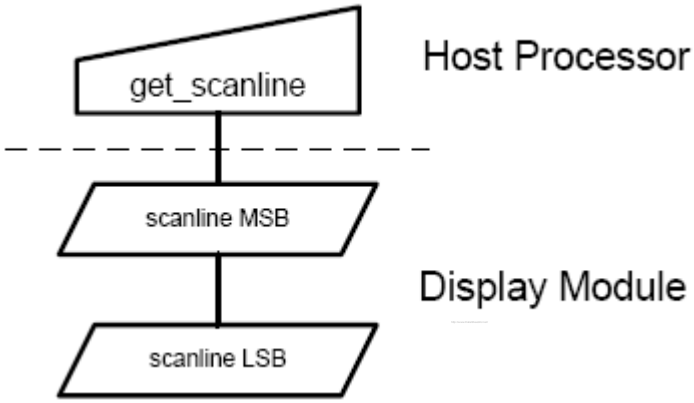
6.2.37 Raed_memory_continue (3Eh)

3EH	Raed_memory_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If set_address_mode B5=0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If set_address_mode B5=1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
Default	Status	Default value											
	Power On Sequence	Contents of memory is set randomly											
Flow Chart													

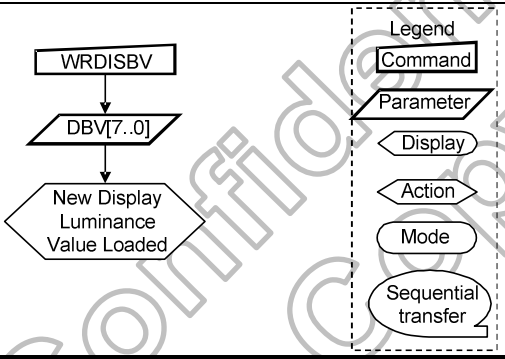
6.2.38 Set tear scan lines (44h)

44H	TESL (Tear Effect Scan Lines)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.												
Restriction	The command has no effect when Tearing Effect output is already ON.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	TELINE[15:0]=0x0000h												
Flow Chart	 												

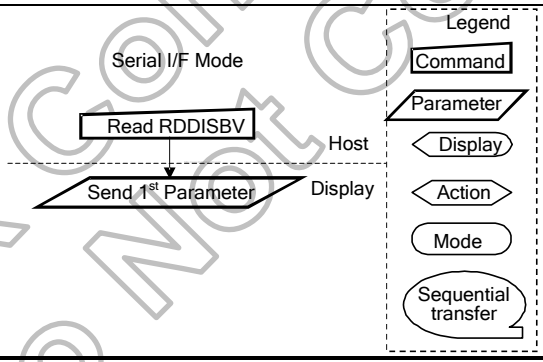
6.2.39 Get the current scanline(45h)

45H	GETSCAN (Get the current scanline)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	1	45
1st parameter	1	1	↑	-	SLN[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	SLN[7:0](8'b0)								00..FF
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes												
Default	SLN[15:0]= 0x0000h												
Flow Chart													

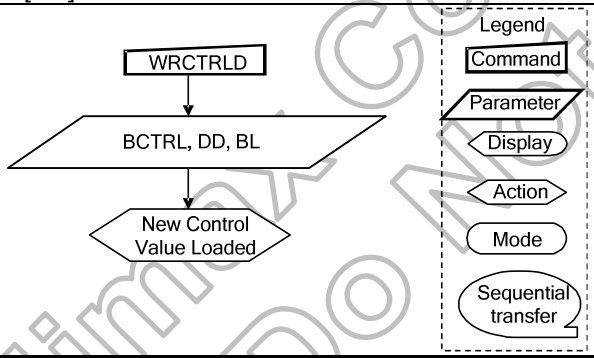
6.2.40 Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	-	DBV[7:0]								00 .. FF
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “5.17.3 Brightness Control Block”.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

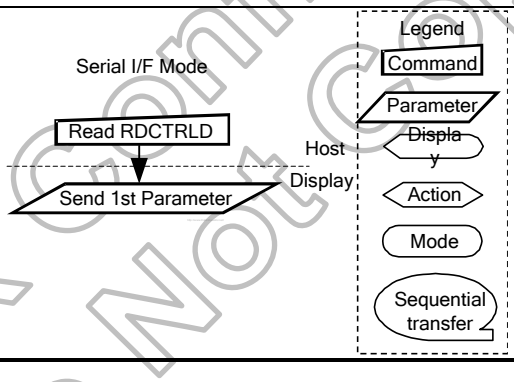
6.2.41 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	-	DBV[7:0]								xx
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display modulespecification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: “5.17.3 Brightness Control Block”, and “6.2.40 Write Display Brightness (51h)” DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is ‘0’ when bit BCTRL of “6.2.42 Write CTRL Display (53h)” command is ‘0’. DBV[7:0] is manual set brightness specified with “6.2.42 Write CTRL Display (53h)” command when bit BCTRL is ‘1’. When bit BCTRL of “6.2.42 Write CTRL Display (53h)” command is ‘1’ and bit C1/C0 of “6.2.44 Write Content Adaptive Brightness Control (55h)” are ‘0’, DBV[7:0] output is the brightness value specified with “6.2.40 Write Display Brightness (51h)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

6.2.42 Write CTRL display (53h)

53H	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00 .. FF
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

6.2.43 Read CTRL value display (54h)

54H	RDCTRLD (Read Control Value Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	0	54
1st parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command returns ambient light and brightness control values, see chapter: "6.2.42 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

6.2.44 Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	-	xx	xx	xx	xx	xx	xx	C1	C0	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “5.17 Content Adaptive Brightness Control (CABC)”.

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don’t care.

Restriction

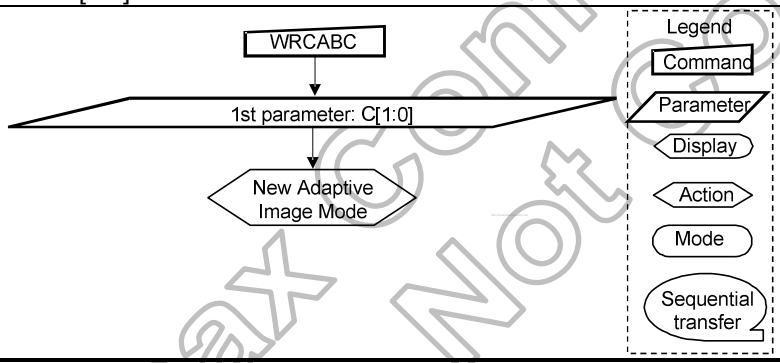
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

CABC[1:0] = 00

Flow Chart



6.2.45 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.17 Content Adaptive Brightness Control (CABC)".

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

Restriction

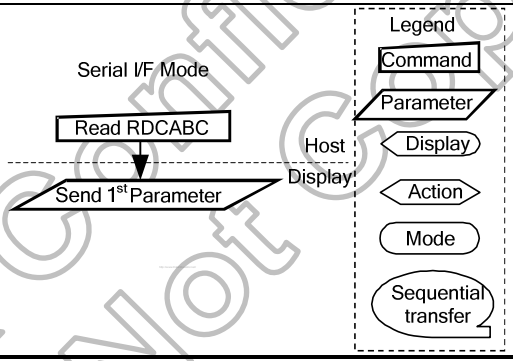
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

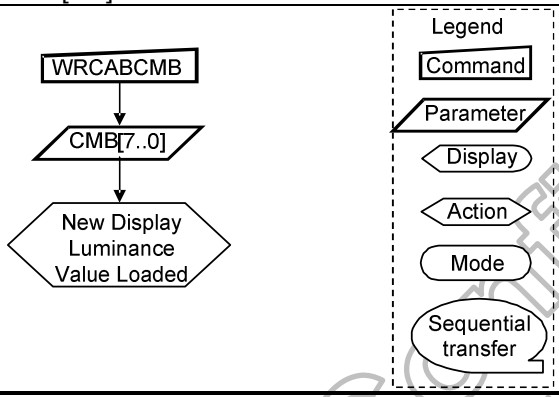
Default

C[1:0] = 00

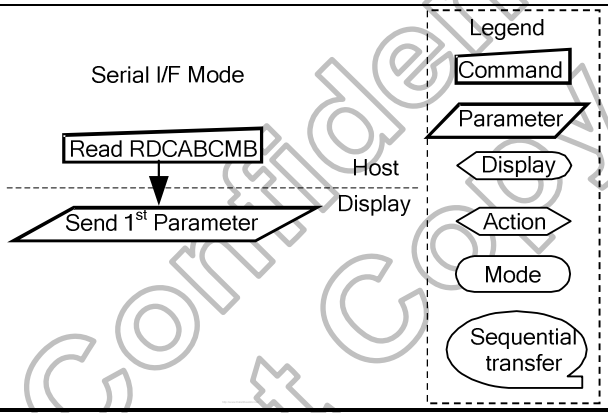
Flow Chart



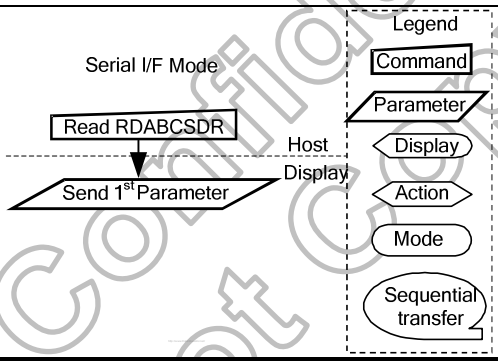
6.2.46 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	1	-	CMB[7:0]								00 .. FF
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "5.17.4 Minimum brightness setting of CABC function".												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00h												
Flow Chart													

6.2.47 Read CABC minimum brightness (5Fh)

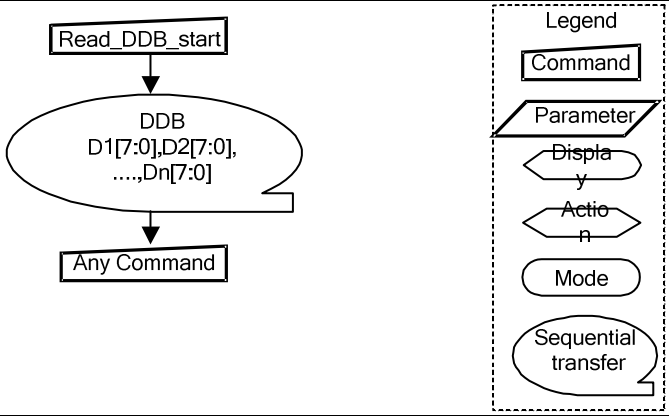
5FH	RDCABCMB (Read CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	↑	1	-	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “5.17.4 Minimum brightness setting of CABC function”. CMB[7:0] is CABC minimum brightness specified with “6.2.46 Write CABC minimum brightness (5Eh)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00h												
Flow Chart													

6.2.48 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68
1st parameter	1	↑	1	-	D[7:6]		0	0	0	0	0	0	xx
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: ● Bit D7 – Register Loading Detection See section “5.15.1 Register loading Detection”. ● Bit D6 – Functionality Detection See section “5.15.2 Functionality Detection “. ● Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

6.2.49 Read_DDB_start (A1h)

A1H	Read_DDB_start												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data. The format of returned data is as follows: Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2: MS (most significant) byte of Supplier ID. Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 4: MS (most significant) byte of Supplier Elective Data Parameter 5: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows: - FFh - Exit code – there is no more data in the Descriptor Block - 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard) - Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in *MIPI Alliance Standard for Device Descriptor Block (DDB)*. DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token. The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command. The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB. Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	D[7:0] = 0x00h												

Flow Chart	

6.2.50 Read_DDB_continue (A8h)

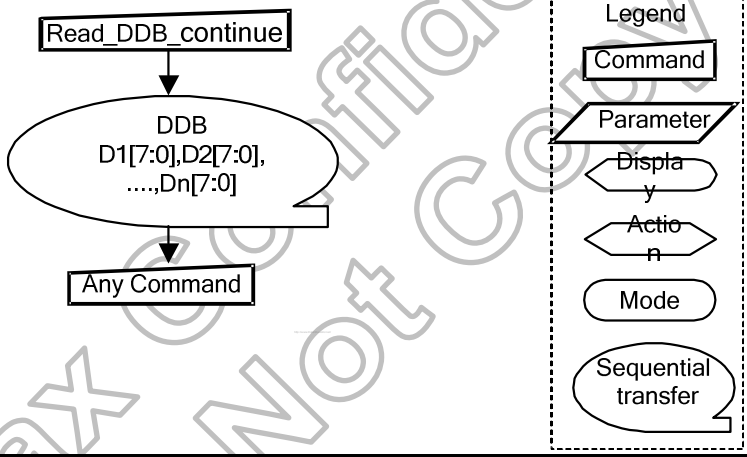
A8H	Read_DDB_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	0	0	0	A8
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.												
Restrictions	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default: D[7:0] = 0x00h

Flow Chart



6.2.51 Read ID1 (DAh)

DAH	RDID1 (Read ID1)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	-	module's manufacturer[7:0]								xx
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.												
Restriction	-												

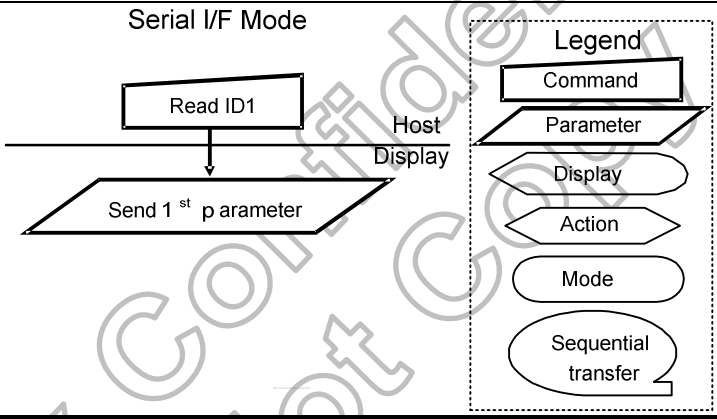
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

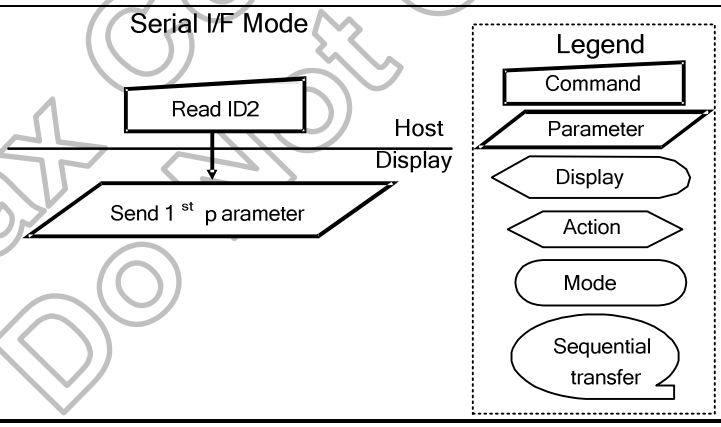
Default

Default value	OTP value
ID1[7:0]=0x00h	Define by customer

Flow Chart



6.2.52 Read ID2 (DBh)

DBH	RDID2 (Read ID2)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	1	1	DB
1st parameter	1	↑	1	-	LCD module/driver version [7:0]								-
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table: ID Byte Value V[7:0] / Version / Changes 80h 81h 82h 83h 84h 85h X= Don't care												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	Default value: ID2[7:0]=0x00h OTP value: Define by customer												
Flow Chart													

6.2.53 Read ID3 (DCh)

DCH	RDID3 (Read ID3)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	-	LCD module/driver ID[7:0]								xx
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.												
Restrictions	-												

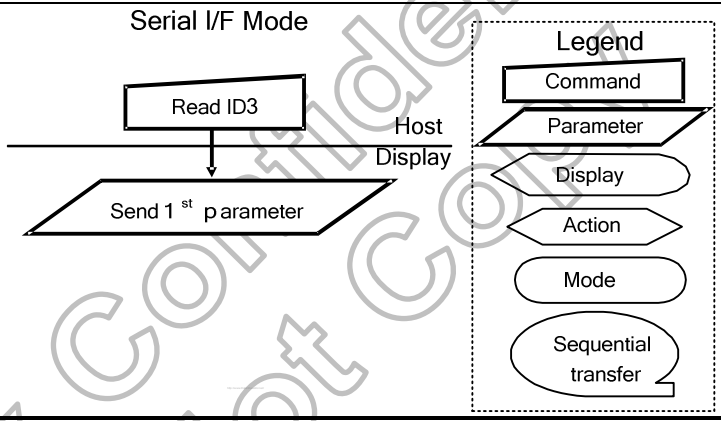
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Default value	OTP value
ID3[7:0]=0x00h	Define by customer

Flow Chart



6.2.54 SETOSC: Set internal oscillator (B0h)

B0H	SETOSC(Set Internal Oscillator)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	OSC_EN	-
2nd parameter	1	1	↑	-	-	-	-	-	UADJ[3:0]				-

Description

This command is used to set internal oscillator related setting

OSC_EN: Enable internal oscillator, High active.
If send Sleep out command(11h), OSC_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), OSC_EN will set "0" by IC internal circuit.

UADJ[3:0]: For User to adjust OSC frequency, default is 48 MHZ.

UADJ				Internal oscillator frequency
0	0	0	0	41%
0	0	0	1	50%
0	0	1	0	59%
0	0	1	1	68%
0	1	0	0	77%
0	1	0	1	85%
0	1	1	0	92%
0	1	1	1	100%
1	0	0	0	109%
1	0	0	1	115%
1	0	1	0	123%
1	0	1	1	130%
1	1	0	0	136%
1	1	0	1	145%
1	1	1	0	151%
1	1	1	1	158%

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	OSC_EN=0, UADJ[3:0]= 4b'0111	UADJ[3:0]

6.2.55 SETPOWER: Set power (B1h)

B1H	SETPOWER(Set power related setting)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	1	↑	-	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_HZ	STB	-
2nd parameter	1	1	↑	-	-	-	-	-	-	-	-	DSTB	-
3rd parameter	1	1	↑	-	-	FS1[2:0]			-	AP[2:0]			-
4th parameter	1	1	↑	-	VGHS[3:0]				VGLS[3:0]				-
5th parameter	1	1	↑	-	DT[1:0]		-	-	-	-	-	-	-
6th parameter	1	1	↑	-	-	-	-	BTP[4:0]					-
7th parameter	1	1	↑	-	-	-	-	BTN[4:0]					-
8th parameter	1	1	↑	-	VRHP[7:0]								-
9th parameter	1	1	↑	-	VRHN[7:0]								-
10th parameter	1	1	↑	-	-	-	VRMP[5:0]						-
11th parameter	1	1	↑	-	-	-	VRMN[5:0]						-
12th parameter	1	1	↑	-	-	APF_EN	DD_TU	VPNL_EN	-	-	PCCS[1:0]		-
13th parameter	1	1	↑	-	-	DC86_DIV[3:0]				XDK1	XDK0	AUTO_XDK	-

Description

This command is used to set related setting of power.

STB: When STB = "1", the HX8392-A enters the standby mode, where all display operation stops, suspend all the internal operations. But the internal R-C oscillator stop or not is determined by OSC_EN bit. To minimize the standby power, please set OSC_EN to 0. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0")
b. Enable or disable the oscillation
c. Software reset

If send Sleep out command(11h), STB will set"0" by IC internal circuit.
If send Sleep in command(10h), STB will set "1" by IC internal circuit.

DSTB: Standby mode select.
When STB = "1" and DSTB = "0", the HX8392-A enters the standby mode.
When STB = "1" and DSTB = "1", the HX8392-A enters the deep standby mode.
The HX8392-A into the deep_standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator.
In the deep standby mode, the GRAM data and register content may be lost. For preventing this, they have to reset again after the deep standby mode cancel.

VSP_EN: ON/OFF the operation of VSP circuit.

VSP_EN	Operation of VSP DC/DC circuit
0	OFF
1	ON

If send Sleep out command(11h), VSP_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), VSP_EN will set "0" by IC internal circuit.

VSN_EN: ON/OFF the operation of VSN circuit.

VSN_EN	Operation of VSN DC/DC circuit
0	OFF
1	ON

If send Sleep out command(11h), VSN_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), VSN_EN will set "0" by IC internal circuit.

VGH_EN: ON/OFF the operation of VGH charge bump circuit.

VGH_EN	Operation of VGH charge bump circuit
0	OFF
1	ON

If send Sleep out command(11h), VGH_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), VGH_EN will set "0" by IC internal circuit.

VGL_EN : ON/OFF the operation of VGL charge bump circuit.

VGL_EN	Operation of VGL charge bump circuit
0	OFF
1	ON

If send Sleep out command(11h), VGL_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), VGL_EN will set "0" by IC internal circuit.

VCL_EN : ON/OFF the operation of VCL charge bump circuit.

VCL_EN	Operation of VCL charge bump circuit
0	OFF
1	ON

If send Sleep out command(11h), VCL_EN will set"1" by IC internal circuit.
If send Sleep in command(10h), VCL_EN will set "0" by IC internal circuit.

VDDDN_HZ: Choose external or internal VDDDN power.
VDDDN_HZ=0, VDDDN= -2.5V.
VDDDN_HZ=1, VDDDN output HZ. (For external VDDDN.)

FS1[2:0]: Set the operating frequency of the step-up circuit for VGH and VGL voltage generation.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit
0	0	0	Inhibit
0	0	1	Fosc/64
0	1	0	Fosc/128
0	1	1	Fosc/256
1	0	0	Fosc/512
1	0	1	Fosc/1024
1	1	0	Fosc/2048
1	1	1	Fosc/4096

AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.5μA
0	1	0	1μA
0	1	1	1.5μA
1	0	0	2μA
1	0	1	2.5μA
1	1	0	3μA
1	1	1	3.5μA

VGHS[3:0] : Switch the output factor for DC/DC circuit for VGH voltage generation. The LCD drive voltage level VGH can be selected according to the characteristic of liquid crystal which panel used**.**

VGHS3	VGHS2	VGHS1	VGHS0	VGH
0	0	0	0	Inhibit
0	0	0	1	9.2
0	0	1	0	9.4
0	0	1	1	9.6
0	1	0	0	9.8
0	1	0	1	10.0
0	1	1	0	10.2
0	1	1	1	10.4
1	0	0	0	10.6
1	0	0	1	10.8
1	0	1	0	11.0
1	0	1	1	11.2
1	1	0	0	11.4

1	1	0	1	11.6
1	1	1	0	11.8
1	1	1	1	12.0

VGLS[3:0] : Switch the output factor for DC/DC circuit for VGL voltage generation. The LCD drive voltage level VGL can be selected according to the characteristic of liquid crystal which panel used**.**

VGLS3	VGLS2	VGLS1	VGLS0	VGL
0	0	0	0	-5.0
0	0	0	1	-5.2
0	0	1	0	-5.4
0	0	1	1	-5.6
0	1	0	0	-5.8
0	1	0	1	-6.0
0	1	1	0	-6.2
0	1	1	1	-6.4
1	0	0	0	-6.6
1	0	0	1	-6.8
1	0	1	0	-7.0
1	0	1	1	-7.2
1	1	0	0	-7.4
1	1	0	1	-7.6
1	1	1	0	-7.8
1	1	1	1	-8.0

DT[1:0]: Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on (ms)
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used. While using Intermal charge pump mode (PCCS1-0 = 10) or HX5186-A mode (PCCS1-0 = 11), VSN = -VSP.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP
0	0	0	0	0	3.01
0	0	0	0	1	3.15
0	0	0	1	0	3.29
0	0	0	1	1	3.46
0	0	1	0	0	3.60
0	0	1	0	1	3.74
0	0	1	1	0	3.91
0	0	1	1	1	4.05
0	1	0	0	0	4.19
0	1	0	0	1	4.36
0	1	0	1	0	4.50
0	1	0	1	1	4.64
0	1	1	0	0	4.81
0	1	1	0	1	4.95
0	1	1	1	0	5.09
0	1	1	1	1	5.26
1	0	0	0	0	5.40
1	0	0	0	1	5.54
1	0	0	1	0	5.71
1	0	0	1	1	Inhibit
. . . . .					Inhibit
1	1	1	1	1	Inhibit

BTN[4:0]: For PCCS1-0 = 00(Internal used, not open) only. Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

While using Intermal charge pump mode (PCCS1-0 = 10) or HX5186-A mode (PCCS1-0 = 11), VSN = -VSP

BTN4	BTN3	BTN2	BTN1	BTN0	VSN
0	0	0	0	0	-3.01
0	0	0	0	1	-3.15
0	0	0	1	0	-3.29
0	0	0	1	1	-3.46
0	0	1	0	0	-3.60
0	0	1	0	1	-3.74
0	0	1	1	0	-3.91
0	0	1	1	1	-4.05
0	1	0	0	0	-4.19
0	1	0	0	1	-4.36
0	1	0	1	0	-4.50
0	1	0	1	1	-4.64
0	1	1	0	0	-4.81
0	1	1	0	1	-4.95
0	1	1	1	0	-5.09
0	1	1	1	1	-5.26
1	0	0	0	0	-5.40
1	0	0	0	1	-5.54
1	0	0	1	0	-5.71
1	0	0	1	1	Inhibit
. . . . .					Inhibit
1	1	1	1	1	Inhibit

VRHP[7:0]: VSPR regulator output control setting for source data output driving.

VRHP[7:0]								VSPR
0	0	0	0	0	0	0	0	3.488
0	0	0	0	0	0	0	1	3.516
0	0	0	0	0	0	1	0	3.544
0	0	0	0	0	0	1	1	3.572
0	0	0	0	0	1	0	0	3.600
0	0	0	0	0	1	0	1	3.628
0	0	0	0	0	1	1	0	3.656
0	0	0	0	0	1	1	1	3.684
0	0	0	0	1	0	0	0	3.713
0	0	0	0	1	0	0	1	3.741
0	0	0	0	1	0	1	0	3.769
0	0	0	0	1	0	1	1	3.797
0	0	0	0	1	1	0	0	3.825
0	0	0	0	1	1	0	1	3.853
0	0	0	0	1	1	1	0	3.881
0	0	0	0	1	1	1	1	3.909
0	0	0	1	0	0	0	0	3.938
0	0	0	1	0	0	0	1	3.966
0	0	0	1	0	0	1	0	3.994
0	0	0	1	0	0	1	1	4.022
0	0	0	1	0	1	0	0	4.050
0	0	0	1	0	1	0	1	4.078
0	0	0	1	0	1	1	0	4.106
0	0	0	1	0	1	1	1	4.134
0	0	0	1	1	0	0	0	4.163
0	0	0	1	1	0	0	1	4.191
0	0	0	1	1	0	1	0	4.219
0	0	0	1	1	0	1	1	4.247

0	0	0	1	1	1	0	0	4.275
0	0	0	1	1	1	0	1	4.303
0	0	0	1	1	1	1	0	4.331
0	0	0	1	1	1	1	1	4.359
0	0	1	0	0	0	0	0	4.388
0	0	1	0	0	0	0	1	4.416
0	0	1	0	0	0	1	0	4.444
0	0	1	0	0	0	1	1	4.472
0	0	1	0	0	1	0	0	4.500
0	0	1	0	0	1	0	1	4.528
0	0	1	0	0	1	1	0	4.556
0	0	1	0	0	1	1	1	4.584
0	0	1	0	1	0	0	0	4.613
0	0	1	0	1	0	0	1	4.641
0	0	1	0	1	0	1	0	4.669
0	0	1	0	1	0	1	1	4.697
0	0	1	0	1	1	0	0	4.725
0	0	1	0	1	1	0	1	4.753
0	0	1	0	1	1	1	0	4.781
0	0	1	0	1	1	1	1	4.809
0	0	1	1	0	0	0	0	4.838
0	0	1	1	0	0	0	1	4.866
0	0	1	1	0	0	1	0	4.894
0	0	1	1	0	0	1	1	4.922
0	0	1	1	0	1	0	0	4.950
0	0	1	1	0	1	0	1	4.978
0	0	1	1	0	1	1	0	5.006
0	0	1	1	0	1	1	1	5.034
0	0	1	1	1	0	0	0	5.063
0	0	1	1	1	0	0	1	5.091
0	0	1	1	1	0	1	0	5.119
00111011 ~ 01111110								Inhibit
0	1	1	1	1	1	1	1	VSP
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

VRHN[7:0]: VSNR regulator output control setting for source data output driving.

VRHN[7:0]								VSNR
0	0	0	0	0	0	0	0	-3.263
0	0	0	0	0	0	0	1	-3.291
0	0	0	0	0	0	1	0	-3.319
0	0	0	0	0	0	1	1	-3.347
0	0	0	0	0	1	0	0	-3.375
0	0	0	0	0	1	0	1	-3.403
0	0	0	0	0	1	1	0	-3.431
0	0	0	0	0	1	1	1	-3.459
0	0	0	0	1	0	0	0	-3.488
0	0	0	0	1	0	0	1	-3.516
0	0	0	0	1	0	1	0	-3.544
0	0	0	0	1	0	1	1	-3.572
0	0	0	0	1	1	0	0	-3.600
0	0	0	0	1	1	0	1	-3.628
0	0	0	0	1	1	1	0	-3.656
0	0	0	0	1	1	1	1	-3.684
0	0	0	1	0	0	0	0	-3.713
0	0	0	1	0	0	0	1	-3.741
0	0	0	1	0	0	1	0	-3.769
0	0	0	1	0	0	1	1	-3.797
0	0	0	1	0	1	0	0	-3.825
0	0	0	1	0	1	0	1	-3.853
0	0	0	1	0	1	1	0	-3.881
0	0	0	1	0	1	1	1	-3.909
0	0	0	1	1	0	0	0	-3.938
0	0	0	1	1	0	0	1	-3.966
0	0	0	1	1	0	1	0	-3.994

0	0	0	1	1	0	1	1	-4.022
0	0	0	1	1	1	0	0	-4.050
0	0	0	1	1	1	0	1	-4.078
0	0	0	1	1	1	1	0	-4.106
0	0	0	1	1	1	1	1	-4.134
0	0	1	0	0	0	0	0	-4.163
0	0	1	0	0	0	0	1	-4.191
0	0	1	0	0	0	1	0	-4.219
0	0	1	0	0	0	1	1	-4.247
0	0	1	0	0	1	0	0	-4.275
0	0	1	0	0	1	0	1	-4.303
0	0	1	0	0	1	1	0	-4.331
0	0	1	0	0	1	1	1	-4.359
0	0	1	0	1	0	0	0	-4.388
0	0	1	0	1	0	0	1	-4.416
0	0	1	0	1	0	1	0	-4.444
0	0	1	0	1	0	1	1	-4.472
0	0	1	0	1	1	0	0	-4.500
0	0	1	0	1	1	0	1	-4.528
0	0	1	0	1	1	1	0	-4.556
0	0	1	0	1	1	1	1	-4.584
0	0	1	1	0	0	0	0	-4.613
0	0	1	1	0	0	0	1	-4.641
0	0	1	1	0	0	1	0	-4.669
0	0	1	1	0	0	1	1	-4.697
0	0	1	1	0	1	0	0	-4.725
0	0	1	1	0	1	0	1	-4.753
0	0	1	1	0	1	1	0	-4.781
0	0	1	1	0	1	1	1	-4.809
0	0	1	1	1	0	0	0	-4.838
0	0	1	1	1	0	0	1	-4.866
0	0	1	1	1	0	1	0	-4.894
0	0	1	1	1	0	1	1	-4.922
0	0	1	1	1	1	0	0	-4.950
0	0	1	1	1	1	0	1	-4.978
0	0	1	1	1	1	1	0	-5.006
0	0	1	1	1	1	1	1	-5.034
0	1	0	0	0	0	0	0	-5.063
0	1	0	0	0	0	0	1	-5.091
0	1	0	0	0	0	1	0	-5.119
01000011 ~ 01111110								Inhibit
0	1	1	1	1	1	1	1	VSN
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

VRMP[5:0]: The positive polarity gamma amplitude voltage setting (VSPR-VGSP).

VRMP[5:0]						VSPR-VGSP
0	0	0	0	0	0	2.588
0	0	0	0	0	1	2.644
0	0	0	0	1	0	2.700
0	0	0	0	1	1	2.756
0	0	0	1	0	0	2.813
0	0	0	1	0	1	2.869
0	0	0	1	1	0	2.925
0	0	0	1	1	1	2.981
0	0	1	0	0	0	3.038
0	0	1	0	0	1	3.094
0	0	1	0	1	0	3.150
0	0	1	0	1	1	3.206
0	0	1	1	0	0	3.263
0	0	1	1	0	1	3.319
0	0	1	1	1	0	3.375
0	0	1	1	1	1	3.431
0	1	0	0	0	0	3.488
0	1	0	0	0	1	3.544

0	1	0	0	1	0	3.600
0	1	0	0	1	1	3.656
0	1	0	1	0	0	3.713
0	1	0	1	0	1	3.769
0	1	0	1	1	0	3.825
0	1	0	1	1	1	3.881
0	1	1	0	0	0	3.938
0	1	1	0	0	1	3.994
0	1	1	0	1	0	4.050
0	1	1	0	1	1	4.106
0	1	1	1	0	0	4.163
0	1	1	1	0	1	4.219
0	1	1	1	1	0	4.275
0	1	1	1	1	1	4.331
1	0	0	0	0	0	4.388
1	0	0	0	0	1	4.444
1	0	0	0	1	0	4.500
1	0	0	0	1	1	4.556
1	0	0	1	0	0	4.613
1	0	0	1	0	1	4.669
1	0	0	1	1	0	4.725
1	0	0	1	1	1	4.781
1	0	1	0	0	0	4.838
1	0	1	0	0	1	4.894
1	0	1	0	1	0	4.950
1	0	1	0	1	1	5.006
1	0	1	1	0	0	5.063
1	0	1	1	0	1	5.119
1	0	1	1	1	0	Inhibit
. . . . .						Inhibit
1	1	1	1	1	0	Inhibit
1	1	1	1	1	1	VSPR(VGSP=VSSA)

VRMN[5:0]: The negitive polarity gamma amplitude voltage setting (VSNR-VGSN).

VRMN[5:0]						VSNR-VGSN
0	0	0	0	0	0	-2.588
0	0	0	0	0	1	-2.644
0	0	0	0	1	0	-2.700
0	0	0	0	1	1	-2.756
0	0	0	1	0	0	-2.813
0	0	0	1	0	1	-2.869
0	0	0	1	1	0	-2.925
0	0	0	1	1	1	-2.981
0	0	1	0	0	0	-3.038
0	0	1	0	0	1	-3.094
0	0	1	0	1	0	-3.150
0	0	1	0	1	1	-3.206
0	0	1	1	0	0	-3.263
0	0	1	1	0	1	-3.319
0	0	1	1	1	0	-3.375
0	0	1	1	1	1	-3.431
0	1	0	0	0	0	-3.488
0	1	0	0	0	1	-3.544
0	1	0	0	1	0	-3.600
0	1	0	0	1	1	-3.656
0	1	0	1	0	0	-3.713
0	1	0	1	0	1	-3.769
0	1	0	1	1	0	-3.825
0	1	0	1	1	1	-3.881
0	1	1	0	0	0	-3.938
0	1	1	0	0	1	-3.994
0	1	1	0	1	0	-4.050
0	1	1	0	1	1	-4.106
0	1	1	1	0	0	-4.163
0	1	1	1	0	1	-4.219

0	1	1	1	1	0	-4.275
0	1	1	1	1	1	-4.331
1	0	0	0	0	0	-4.388
1	0	0	0	0	1	-4.444
1	0	0	0	1	0	-4.500
1	0	0	0	1	1	-4.556
1	0	0	1	0	0	-4.613
1	0	0	1	0	1	-4.669
1	0	0	1	1	0	-4.725
1	0	0	1	1	1	-4.781
1	0	1	0	0	0	-4.838
1	0	1	0	0	1	-4.894
1	0	1	0	1	0	-4.950
1	0	1	0	1	1	-5.006
1	0	1	1	0	0	-5.063
1	0	1	1	0	1	-5.119
1	0	1	1	1	0	Inhibit
• • • • •						Inhibit
1	1	1	1	1	0	Inhibit
1	1	1	1	1	1	VSNR(VGSN=VSSA)

APF_EN: Abnormal power-off detection enable.

DD_TU: In-house function, and not open.

VPNL_EN: Enable VPNL function.

PCCS[1:0]: Select the VSP/VSN bumping method as listed below

PCCS1	PCCS0	Driving mode
0	0	Inhibit
0	1	Inhibit
1	0	Internal Charge pump Mode
1	1	External Charge pump Mode (Use HX5186-A)

DC86_DIV[3:0]: Frequency for Charge Pump Mode (HX5186-A)

DC86_DIV[3:0]	Frequency	
	External Charge Pump Mode (HX5186-A)	Internal Charge Pump Mode
000	Fosc/8	Fosc/8
0001	Fosc/16	Fosc/16
0010	Fosc/32	Fosc/32
0011	Fosc/64	Fosc/64
0100	Fosc/96	Fosc/96
0101	Fosc/128	Fosc/128
0110	Fosc/160	Fosc/160
0111	Fosc/192	Fosc/192
1000	Fosc/224	Fosc/224
1001	Fosc/256	Fosc/256
1010	Fosc/288	Fosc/288
1011	Fosc/320	Fosc/320
1100	Fosc/352	Fosc/352
1101	Fosc/384	Fosc/384
1110	Fosc/416	Fosc/512
1111	Fosc/448	Fosc/1024

XDK[1:0]: Setting charge pump mode of Internal / External charge pump.

XDK[1]	XDK[0]	External charge pump	Internal charge pump
0	0	X1.5 Pump	X1.5 Pump
0	1	X2 Pump	X2 Pump
1	0	X3 Pump	X3 Pump
1	1	Inhibited	X2.5 Pump

AUTO_XDK: Auto XDK function enable of Internal / External charge pump.

Auto_XDK=1	Charge pump mode

		VDD3 x 1.5 > VSPtarget	X1.5
		VDD3 x 2 > VSPtarget	X2
		VDD3 x 2 < VSPtarget	X3
		Auto_XDK=0	Depend on XDK[2:0]

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	VSN_EN=0, VSP_EN=0, VGL_EN=0, VGH_EN=0, VCL_EN=0, VDDDN_HZ=0, STB=1, DSTB=0, FS1[2:0]=100, AP[2:0]=100, VGHS[3 :0]=0111, VGLS[3 :0]=0111, DT[1:0] =00, BTP[4:0]=10001, BTN[4:0]=10001, VRHP[7:0]=0x36h, VRHN[7:0]=0x30h, VRMP[5:0]=0x2Bh, VRMN[5:0]=0x24h, APF_EN=1, DD_TU= 0, VPNL_EN=0, PCCS[1 :0]=10, DC86_DIV[3:0]=1000, XDK1=1, XDK0=0, AUTO_XDK=0	FS1[2:0], AP[2:0], VGHS[3 :0], VGLS[3 :0], DSTB, DT[1:0], BTP[4:0], BTN[4:0], VRHP[7:0], VRHN[7:0], VRMP[5:0], VRMN[5:0], APF_EN, DD_TU, VPNL_EN, PCCS[1 :0], DC86_DIV[3:0], XDK1, XDK0, AUTO_XDK,

6.2.56 SETDISP: Set display related register (B2h)

B2H	SETDISP(Set display related register)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	1	0	B2
1st parameter	1	1	↑	-	-	-	-	-	GON	DTE	D[1:0]		
2nd parameter	1	1	↑	-	NL[7:0]								
3rd parameter					BP [7:0]								
4th parameter	1	1	↑	-	FP [7:0]								
5th parameter	1	1	↑		RTN[7:0]								
6th parameter	1	1	↑	-	SAP[3:0]				INIT_DIS	INIT_SET[2:0]			
7th parameter	1	1	↑	-	GEN_ON[7:0]								
8th parameter	1	1	↑	-	GEN_OFF[7:0]								
9th parameter	1	1	↑	-	BP_PE[7:0]								
10th parameter	1	1	↑	-	FP_PE[7:0]								
11th parameter	1	1	↑	-	RTN_PE[7:0]								
12th parameter	1	1	↑	-	-	RES_SEL[2:0]			-	-	TGS[1:0]		

Description

This command is used to set display related register

D1–0: Setting Source driver output

D1	D0	Source Output	HX8392-A Internal Display Operations
0	0	VSSD	Halt
0	1	Inhibit	Inhibit
1	0	V255	Operate
1	1	Display	Operate

If send Display on command(29h), D[1:0] will set"11" by IC internal circuit.
If send Display off command(28h), D[1:0] will set "10" by IC internal circuit.
If send Sleep in command(10h), D[1:0] will set "00" by IC internal circuit.

GON, DTE: Setting Gate driver output

GON	DTE	Gate Output
0	X	Inhibit
1	0	VGL
1	1	VGH/VGL

If send Sleep out command(11h), GON, DTE will set"11" by IC internal circuit.
If send Sleep in command(10h), GON, DTE will set "10" by IC internal circuit.

FP[7:0]: Specify the amount of scan line for front porch (FP).
BP[7:0] : Specify the amount of scan line for back porch(BP).
FP_PE[7:0]: Specify the amount of scan line for front porch (FP) on partial idle mode.
BP_PE[7:0] : Specify the amount of scan line for back porch(BP) on partial idle mode.

FP[7:0] / FP_PE[7:0] BP[7:0] / BP_PE[7:0]	Number of FP Line	Number of BP Line
8h'00	Inhibit	
8h'01	3 lines	
8h'02	4 lines	
8h'03	5 lines	
8h'04	6 lines	
8h'05	7 lines	
• • •	• • •	
8h'FB	253 lines	
8h'FC	254 lines	
8h'FD	255 lines	
8h'FE	256 lines	
8h'FF	257 lines	

SAP[3:0]: Set Current of Operational Amplifier

SAP3	SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	0	1 * Iref
0	0	0	1	2 * Iref
0	0	1	0	3 * Iref
0	0	1	1	4 * Iref
0	1	0	0	5 * Iref
0	1	0	1	6 * Iref
0	1	1	0	7 * Iref
0	1	1	1	8 * Iref
. . . . .				
1	1	1	1	16 * Iref

INIT_DISP: Internal used, not open. Please set “0”.

INIT_SET[2:0]: INIT Pulse width

INIT_SET[2:0]	INIT Pulse width
000	1ms
001	2ms
010	3ms
011	4ms
100	5ms
Othet setting	Inhibit

GEN_ON[7:0]: Gamma OP turned on timing and in-house function not open.

GEN_OFF[7:0]: Gamma OP turned off timing and in-house function not open.

RTN[7:0]: A cycle time of line width, in-house function not open.
RTN_PE[7:0]: A cycle time of line width on partial idle mode, in-house function not open.

RTN[7:0]/ RTN_PE[7:0]	Clock per Line
8h’00	600 clocks
8h’01	604 clocks
8h’02	608 clocks
8h’03	612 clocks
. . .	. . .
8’hFD	1612 clocks
8’hFE	1616 clocks
8’hFF	1620 clocks

NL[7:0]: Sets the number of lines to drive the LCD at an interval of 4 lines. The GRAM address mapping is not affected by the number of lines set by NL[7:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[7:0]								Line
0	0	0	0	0	0	0	0	480
0	0	0	0	0	0	0	1	484
0	0	0	0	0	0	1	0	488
0	0	0	0	0	0	1	1	492
..	..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..	..
1	1	0	1	1	1	0	0	1360
1	1	0	1	1	1	0	1	1364
1	1	0	1	1	1	1	0	1368
1	1	0	1	1	1	1	1	Inhibit
..	..	..	..	..	..	..	..	..
1	1	1	1	1	1	1	1	Inhibit

Note: 1. If NL[7:0] > 130, only support DSI video mode.

TGS[1:0]: Source switch sequence select.

TGS1	TGS0	TG sequence
0	0	SW1→ SW2→ SW3
0	1	SW2→ SW3→ SW1
1	0	SW2→ SW1→ SW3
1	1	SW3→ SW1→ SW2

RES_SEL[2:0]: Panel resolution select

RES_SEL[2:0]	Resolution	Source channels
000	800RGBX1280 dot	S1 ~ S800
001	768RGBX1280 dot	S1 ~ S384, S417~S800
010	720RGBX1280 dot	S1 ~ S360, S441~S800
011	600RGBX1024 dot	S1 ~ S300, S501~S800

Restrictions

SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	GON=1, DET=0, D[1:0]=00, BP[7:0]=0x00h, FP[7:0]=0x00h, RTN[7:0]=0x05h, SAP[3:0]=0111, GEN_ON=0x00h, GEN_OFF=0xFFh, BP_PE[7:0]=0x00h, FP_PE[7:0]=0x00h, RTN_PE[7:0]=0x05h, NL[7:0]=0xC8h, RES_SEL[2:0]=010, TGS[1:0]=00	BP[7:0], FP[7:0], SAP[3:0], GEN_ON[7:0], GEN_OFF[7:0], RTN[7:0], BP_PE[7:0], FP_PE[7:0], RTN_PE[7:0], NL[7:0], RES_SEL[2:0], TGS[1:0]

6.2.57 SETRGBIF: Set RGB interface related register (B3h)

B3H	SETRGBIF(Set RGB interface related register)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	1	↑	-	-	-	-	-	DPL	HSPL	VSPL	EPL	-

Description

This command is used to set RGB interface related register.

EPL: Specify the polarity of ENABLE pin in RGB interface mode.

EPL	ENABLE pin	Display
0	0	Enable
0	1	Disable
1	0	Disable
1	1	Enable

VSPL: The polarity of VS pin. When VSPL=0, the VS pin is Low active. When VSPL=1, the VS pin is High active.

HSPL: The polarity of HS pin. When HSPL=0, the HS pin is Low active. When HSPL=1, the HS pin is High active.

DPL: The polarity of DCK pin. When DPL=0, the data is read on the rising edge of DCK signal. When DPL=1, the data is read on the falling edge of DCK signal.

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	DPL=0,HSPL=0,VSPL=0,EPL=1	DPL,HSPL,VSPL,EPL

6.2.58 SETMPUCYC: Set MPU/Command mode panel driving timing(RB4h)

B4H	SETMPUCYC(Set MPU/Command mode panel driving timing)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	1	0	0	B4
1st Parameter	1	1	↑	-	-	-	NW_PE[2:0]			NW[2:0]			-
2nd Parameter					-	-	-	-	SHR[11:8]				
3rd Parameter	1	1	↑	-	SHR[7:0]								-
4th Parameter	1	1	↑	-	SPON[7:0]								-
5th Parameter	1	1	↑	-	SPOFF[7:0]								-
6th Parameter	1	1	↑	-	CHR[7:0]								-
7th Parameter	1	1	↑	-	CON[7:0]								
8th Parameter	1	1	↑	-	COFF[7:0]								-
9th Parameter	1	1	↑	-	SHP[3:0]				-	-	-	-	
10th Parameter	1	1	↑	-	CHP[3:0]				CCP[3:0]				-
11th Parameter	1	1	↑	-	N_t1[7:0]								-
12th Parameter	1	1	↑	-	N_t2[7:0]								-
13th Parameter	1	1	↑	-	N_t3[7:0]								-
14th Parameter	1	1	↑	-	N_t4[7:0]								-
15th Parameter	1	1	↑	-	N_t5[7:0]								-
16th Parameter	1	1	↑	-	N_t6[7:0]								-
17th Parameter	1	1	↑	-	N_t7[7:0]								-
18th Parameter	1	1	↑	-	N_t8[7:0]								-
19th Parameter	1	1	↑	-	N_t9[7:0]								-
20th Parameter	1	1	↑	-	-	-	-	-	EOT[3:0]				-

Description

This command is used to get setting of display waveform cycles for MPU mode or Command mode.

NW[2:0]: Inversion type setting.
NW_PE[2:0]: Inversion type setting on partial idle mode.

NW2	NW1	NW0	Inversion type
0	0	0	Column inversion
0	0	1	1-dot inversion
0	1	0	2-dot inversion
0	1	1	4-dot inversion
1	0	0	Inhibit
1	0	1	Inhibit
1	1	0	Inhibit
1	1	1	Inhibit

SHR[11:0]: GSP Hsync Rise.

SHR_0[7:0]	Start Pulse Output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFFEh	1022 x HSYNC
0xFFFh	1023 x HSYNC

SPON[7:0]: GSP Pulse Delay.

SPON[7:0]	Start Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •

0xFEh	1016 OSC CLK
0xFFh	1020 OSC CLK

Note: 1. SPON[7:0] < SPOFF ≤ RTN[7:0]

SPOFF[7:0]: GSP Pulse width.

SPON[7:0]	Start Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 x OSC CLK
0xFFh	1020 x OSC CLK

Note: 1. SPON[7:0] < SPOFF ≤ RTN[7:0]

SHP[3:0]: Width of GSP High pulse.

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		• • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CHR[7:0]: CK Hsync Rise.

CHR[7:0]	CK Pulse start output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFEh	510 x HSYNC
0xFFh	511 x HSYNC

CON[7:0]: CK Pulse Delay.

CON[7:0]	CK Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 OSC CLK
0xFFh	1020 OSC CLK

Note: 1. CON[7:0] < COFF ≤ RTN[7:0]

COFF[7:0]: CK Pulse width.

COFF[7:0]	CK Pulse Output
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 OSC CLK

0xFFh	1020 OSC CLK

Note: 1. CON[7:0] < COFF ≤ RTN[7:0]

CHP[3:0]: Width of CK High pulse.

CHP3	CHP2	CHP1	CHP0	CK Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		. . . . .		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CCP[3:0]: A Cycle of CK pulse.

CCP3	CCP2	CCP1	CCP0	CK Pulse cycle
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		. . . . .		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

N_t1[7:0]: The timing definition of t1.

N_t1[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t2[7:0]: The timing definition of t2.

N_t2[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t3[7:0]: The timing definition of t3.

N_t3[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK

. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t4[7:0]: The timing definition of t4.

N_t4[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t5[7:0]: The timing definition of t5.

N_t5[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t6[7:0]: The timing definition of t6.

N_t6[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t7[7:0] : The timing definition of t7.

N_t1[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t8[7:0]: The timing definition of t8.

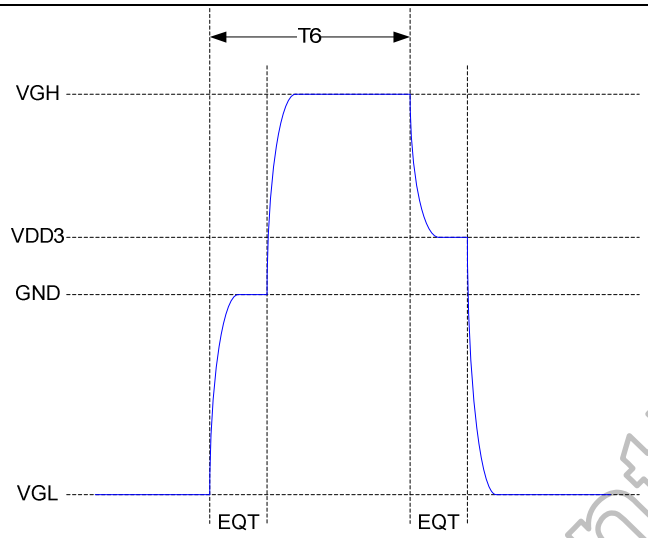
N_t8[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t9[7:0]: The timing definition of t9.

N_t9[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

EQT[3:0]: Equalizing period of TG output

EQT3	EQT2	EQT1	EQT0	Clock cycles
0	0	0	0	0
0	0	0	1	4
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	20
0	1	1	0	24
0	1	1	1	28
1	0	0	0	32
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

	
Restrictions	-
Register Availability	
Default	
Flow Chart	

6.2.59 SETVCOM: Set VCOM voltage (B6h)

B6 H	SETVCOM (Set VCOM Voltage)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	1	1	0	B6
1st parameter	1	1	↑	-	VCMC[7:0]								-

Description

This command is used to set VCOM Voltage.

VCMC[7:0]: DC VCOM voltage setting for forward scan.

VCMC[7:0]								VCOM (V)
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	-2
0	0	0	0	0	0	0	1	-1.984
0	0	0	0	0	0	1	0	-1.968
0	0	0	0	0	0	1	1	-1.952
0	0	0	0	0	1	0	0	-1.936
0	0	0	0	0	1	0	1	-1.92
0	0	0	0	0	1	1	0	-1.904
0	0	0	0	0	1	1	1	-1.888
0	0	0	0	1	0	0	0	-1.872
0	0	0	0	1	0	0	1	-1.856
0	0	0	0	1	0	1	0	-1.84
0	0	0	0	1	0	1	1	-1.824
0	0	0	0	1	1	0	0	-1.808
0	0	0	0	1	1	0	1	-1.792
0	0	0	0	1	1	1	0	-1.776
0	0	0	0	1	1	1	1	-1.76
0	0	0	1	0	0	0	0	-1.744
0	0	0	1	0	0	0	1	-1.728
0	0	0	1	0	0	1	0	-1.712
0	0	0	1	0	0	1	1	-1.696
0	0	0	1	0	1	0	0	-1.68
0	0	0	1	0	1	0	1	-1.664
0	0	0	1	0	1	1	0	-1.648
0	0	0	1	0	1	1	1	-1.632
0	0	0	1	1	0	0	0	-1.616
0	0	0	1	1	0	0	1	-1.6
0	0	0	1	1	0	1	0	-1.584
0	0	0	1	1	0	1	1	-1.568
0	0	0	1	1	1	0	0	-1.552
0	0	0	1	1	1	0	1	-1.536
0	0	0	1	1	1	1	0	-1.52
0	0	0	1	1	1	1	1	-1.504
0	0	1	0	0	0	0	0	-1.488
0	0	1	0	0	0	0	1	-1.472
0	0	1	0	0	0	1	0	-1.456
0	0	1	0	0	0	1	1	-1.44
0	0	1	0	0	1	0	0	-1.424
0	0	1	0	0	1	0	1	-1.408
0	0	1	0	0	1	1	0	-1.392
0	0	1	0	0	1	1	1	-1.376
0	0	1	0	1	0	0	0	-1.36
0	0	1	0	1	0	0	1	-1.344
0	0	1	0	1	0	1	0	-1.328
0	0	1	0	1	0	1	1	-1.312
0	0	1	0	1	1	0	0	-1.296
0	0	1	0	1	1	0	1	-1.28
0	0	1	0	1	1	1	0	-1.264
0	0	1	0	1	1	1	1	-1.248
0	0	1	1	0	0	0	0	-1.232
0	0	1	1	0	0	0	1	-1.216
0	0	1	1	0	0	1	0	-1.2
0	0	1	1	0	0	1	1	-1.184

		0	0	1	1	0	1	0	0	-1.168
		0	0	1	1	0	1	0	1	-1.152
		0	0	1	1	0	1	1	0	-1.136
		0	0	1	1	0	1	1	1	-1.12
		0	0	1	1	1	0	0	0	-1.104
		0	0	1	1	1	0	0	1	-1.088
		0	0	1	1	1	0	1	0	-1.072
		0	0	1	1	1	0	1	1	-1.056
		0	0	1	1	1	1	0	0	-1.04
		0	0	1	1	1	1	0	1	-1.024
		0	0	1	1	1	1	1	0	-1.008
		0	0	1	1	1	1	1	1	-0.992
		0	1	0	0	0	0	0	0	-0.976
		0	1	0	0	0	0	0	1	-0.96
		0	1	0	0	0	0	1	0	-0.944
		0	1	0	0	0	0	1	1	-0.928
		0	1	0	0	0	1	0	0	-0.912
		0	1	0	0	0	1	0	1	-0.896
		0	1	0	0	0	1	1	0	-0.88
		0	1	0	0	0	1	1	1	-0.864
		0	1	0	0	1	0	0	0	-0.848
		0	1	0	0	1	0	0	1	-0.832
		0	1	0	0	1	0	1	0	-0.816
		0	1	0	0	1	0	1	1	-0.8
		0	1	0	0	1	1	0	0	-0.784
		0	1	0	0	1	1	0	1	-0.768
		0	1	0	0	1	1	1	0	-0.752
		0	1	0	0	1	1	1	1	-0.736
		0	1	0	1	0	0	0	0	-0.72
		0	1	0	1	0	0	0	1	-0.704
		0	1	0	1	0	0	1	0	-0.688
		0	1	0	1	0	0	1	1	-0.672
		0	1	0	1	0	1	0	0	-0.656
		0	1	0	1	0	1	0	1	-0.64
		0	1	0	1	0	1	1	0	-0.624
		0	1	0	1	0	1	1	1	-0.608
		0	1	0	1	1	0	0	0	-0.592
		0	1	0	1	1	0	0	1	-0.576
		0	1	0	1	1	0	1	0	-0.56
		0	1	0	1	1	0	1	1	-0.544
		0	1	0	1	1	1	0	0	-0.528
		0	1	0	1	1	1	0	1	-0.512
		0	1	0	1	1	1	1	0	-0.496
		0	1	0	1	1	1	1	1	-0.48
		0	1	1	0	0	0	0	0	-0.464
		0	1	1	0	0	0	0	1	-0.448
		0	1	1	0	0	0	1	0	-0.432
		0	1	1	0	0	0	1	1	-0.416
		0	1	1	0	0	1	0	0	-0.4
		0	1	1	0	0	1	0	1	-0.384
		0	1	1	0	0	1	1	0	-0.368
		0	1	1	0	0	1	1	1	-0.352
		0	1	1	0	1	0	0	0	-0.336
		0	1	1	0	1	0	0	1	-0.32
		0	1	1	0	1	0	1	0	-0.304
		0	1	1	0	1	0	1	1	-0.288
		0	1	1	0	1	1	0	0	-0.272
		0	1	1	0	1	1	0	1	-0.256
		0	1	1	0	1	1	1	0	-0.24
		0	1	1	0	1	1	1	1	-0.224
		0	1	1	1	0	0	0	0	-0.208
		0	1	1	1	0	0	0	1	-0.192
		0	1	1	1	0	0	1	0	-0.176
		0	1	1	1	0	0	1	1	-0.16
		0	1	1	1	0	1	0	0	-0.144

	0	1	1	1	0	1	0	1	-0.128
	0	1	1	1	0	1	1	0	-0.112
	0	1	1	1	0	1	1	1	-0.096
	0	1	1	1	1	0	0	0	-0.08
	0	1	1	1	1	0	0	1	-0.064
	0	1	1	1	1	0	1	0	-0.048
	0	1	1	1	1	0	1	1	-0.032
	0	1	1	1	1	1	0	0	-0.016
	01111101								Inhibit
	0	1	1	1	1	1	1	0	VCOMR
	0	1	1	1	1	1	1	1	VSSA
	10000000 ~ 11111110								Inhibit
	1	1	1	1	1	1	1	1	HZ

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	VCMC[7:0]=0x5Eh	VCMC[7:0]

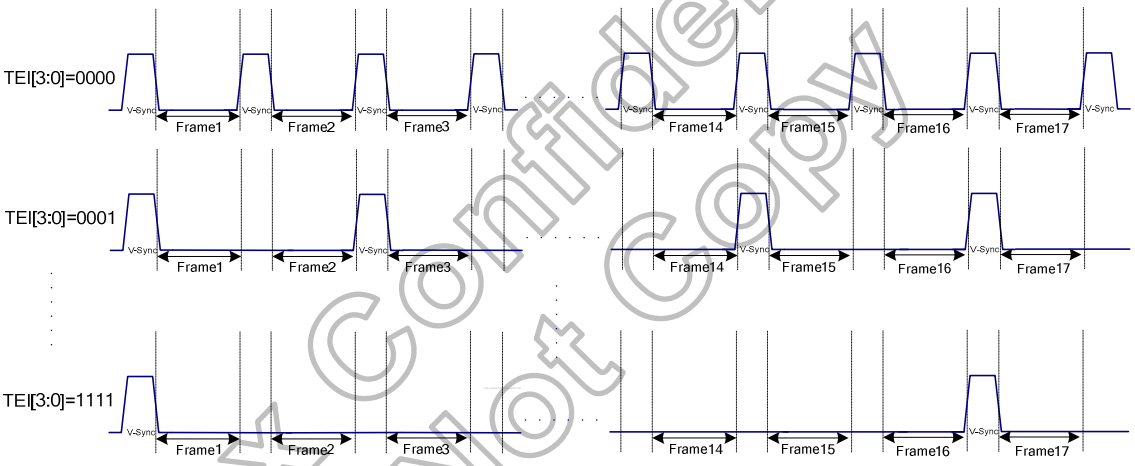
6.2.60 SETTE: Set internal TE function (B7h)

B7H	SETTE (Set internal TE function)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	1	1	1	B7
1st parameter	1	1	↑	-	-	-	-	-	TEI[3:0]				
2nd parameter	1	1	↑	-	-	-	-	-	-	TEP[10:8]			
3rd parameter	1	1	↑	-	TEP[7:0]								-

Description

TEI[3:0]: Sets the output interval of TE signal according to the display data rewrite cycle and data transfer rate.

TEI3	TEI2	TEI1	TEI0	Output Interval
0	0	0	0	1 frame
0	0	0	1	2 frames
0	0	1	0	3 frames
• • • • • • • •				• •
1	1	1	0	15 frames
1	1	1	1	16 frames



TEP[10:0]: Sets the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation.
Make sure the setting restriction 11'h000 ≤ TEP[10:0] ≤ Numbers of Line-1.

TEP[10:0]	Output position
000h	0th line
001h	1st line
002h	2nd line
003h	3rd line
• • •	• • •
556h	1366th line
557h	1367th line
558h	1368th line

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	TEI[3:0]=0000, TEP[10:0]= 0x000h	TEI[3:0], TEP[9:0]

6.2.61 SETEXTC: Set extension command (B9h)

B9H	SETEXTC (Set extended command set)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	0	0	1	B9
1st parameter	1	1	↑	-	EXTC1[7:0]								FF
2nd parameter	1	1	↑	-	EXTC2[7:0]								83
3rd parameter	1	1	↑	-	EXTC3[7:0]								92

Description

This command is used to set extended command set access enable.

Extend cmd	Command description
Enable	After command (B9h), must write 3 parameters (FFh,83h,92h) by order
Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh,83h,92h)

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	EXTC1[7:0]=0x00h, EXTC2[7:0]=0x00h, EXTC3[7:0]=0x00h,	N/A

6.2.62 SETMIPI: (BAh)

BAH	SETMIPI (Set extended command set)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	0	1	0	BA
1st parameter	1	1	↑	-	0	0	0	TX_OSC	0	0	LAN_NUM [1:0]		-
2nd parameter	1	1	↑	-	1	0	0	0	0	0	TX_DELAY[1:0]		-

Description

This command is used to set DSI I/F setting.

LAN_NUM[1:0]: Data lane number of DSI interface

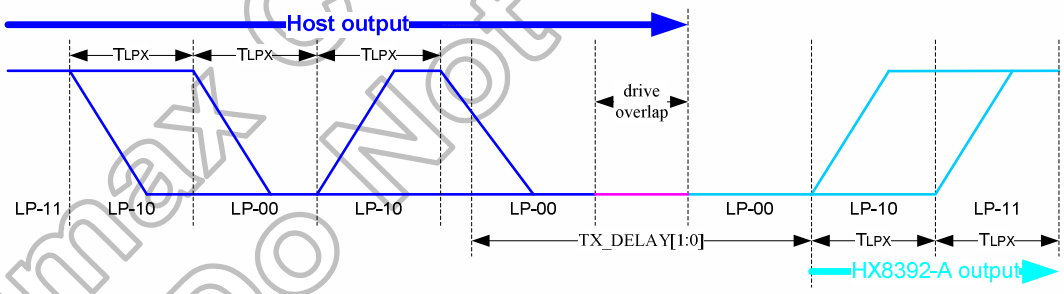
LAN_NUM[1:0]	Lane number	Used DSI data lane
00	1	HS_D0P/N
01	2	HS_D0P/N, HS_D1P/N
10	3	HS_D0P/N, HS_D1P/N, HS_D2P/N
11	4	HS_D0P/N, HS_D1P/N, HS_D2P/N, HS_D3P/N

TX_OSC: Select Low Power Transmitter oscillator.

TX_OSC	Oscillator frequency
0	12MHz
1	6MHz

TX_DELAY[1:0]: Set DSI TX output delay time.

TX_DELAY[1:0]	Delay cycle(TLPX)
00	Inhibit
01	3~5
10	5~7
11	7~9



Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	LAN_NUM[1:0]=01 TX_OSC=0, TX_DELAY[1:0]=10	LAN_NUM[1:0], TX_OSC, TX_DELAY[1:0]

6.2.63 SETOTP: Set OTP (BBh)

BBH	SETOTP(Set OTP Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	0	1	1	BB
1st parameter	1	1	↑	-	OTP_MASK[7:0] (8'b0)								-
2nd parameter	1	1	↑	-	-	-	-	-	-	-	OTP_INDEX[9:8]		-
3rd parameter	1	1	↑	-	OTP_INDEX[7:0]								-
4th parameter	1	1	↑	-	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		OTP_PWR_SEL	OTP_PROG	-
5th parameter	1	1	↑	-	OTP_DATA[7:0]								-

Description

This command is used to set OTP Related Setting.
OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed.
OTP_INDEX[7:0]: Set index of OTP table for programming.
OTP_INDEX[9:8]: For farther use. The register value should be 0. Not open.
OTP_PWE: OTP program write enable, if 1, means OTP is able to be programmed.
OTP_PROG: When set to 1, the register content of OTP index is programmed.
OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLPOUT command is received. Nevertheless, if this bit is set to 1, it will disable the auto loading function when the SLPOUT command was received. In general, this bit is used when OTP is not yet programmed.
OTP_PTM[1:0]: Not open, internal use.
OTP_PWR_SEL: When written to 1, OTP_PWR voltage is fed to OTP
OTP_DATA[7:0]: Read back the OTP index data.

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	OTP_MASK[7:0]=0x00h, OTP_INDEX[9:0]=0x03Bh, OTP_LOAD_DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=00, OTP_PWR_SEL=0, OTP_PROG=0, OTP_DATA[7:0]=xxh	N/A

6.2.64 SETPTBA: Set internal power(BFh)

BFH	SETPTBA (Set internal power)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	1	1	1	BF
1st parameter	1	1	↑	-	0	0	0	0	0	1	0	1	05
2nd parameter	1	1	↑	-	PTBA[23:16]								60
3rd parameter	1	1	↑	-	PTBA[15:8]								-
4th parameter	1	1	↑	-	PTBA[7:0]								00

Description

PTBA[23:16]: Internal use, not open. Please set 0x60.
PTBA[15:11]: Internal use, not open. Please set "00000"
PTBA[10:9]: Set regulated current source.

PTBA[10:9]	Level
00	Inhibit
01	Small
10	Middle
11	Large

PTBA[8]: Internal use, not open. Please set "0".
PTBA[7:0]: Internal use, not open. Please set 0x00.

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	PTBA[23:16]=0x60h, PTBA[15:8]=0x04h, PTBA[7:0]=0x00h,	-

6.2.65 SETDSIMO: Set display mode (C2h)

C2H	SETRGBIF(Set RGB interface related register)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	-	-	-	-	-	RM	-	DM[1:0]		-

Description

This command is used to set display source and mode related register

RM The bit is used to enable or disable for the Frame Memory access operation.
RM setting is enabled from the next frame of Video mode. Wait 1 frame to transfer data after setting .

RM	GRAM access
0	Disable
1	Enable

DM[1:0] The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, VSYNC+HSYNC. Note that switching between VSYNC and display operation is prohibited.

DM 1	DM 0	Display Mode
0	0	Internal oscillation clock
0	1	VSYNC+HSYNC
1	0	VSYNC signal
1	1	Video mode display data bypass GRAM mode

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	RM=0, DM[1:0]=00	RM, DM[1:0]

6.2.66 SETID: Set ID (C3h)

C3H	SETID (Set ID)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	-	ID1[7:0]								-
2nd parameter	1	1	↑	-	ID2[7:0]								-
3rd parameter	1	1	↑	-	ID3[7:0]								-
Description	This command is used to set ID (RDAh, RDBh, RDCh) value.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	ID1[7:0]=0x00h, ID2[7:0]=0x00h, ID3[7:0]=0x00h,	ID1[7:0], ID2[7:0], ID3[7:0]

6.2.67 SETDDB: Set DDB (C4h)

C4H	SETDDB (Set DDB)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	-	DDB1[7:0](8'b0)								-
2nd parameter	1	1	↑	-	DDB2[7:0](8'b0)								-
3rd parameter	1	1	↑	-	DDB3[7:0](8'b0)								-
4th parameter	1	1	↑	-	DDB4[7:0](8'b0)								-
Description	This command is used to set A1h DDB1~4 value.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	DDB1[7:0]=0x00h, DDB2[7:0]=0x00h, DDB3[7:0]=0x00h, DDB4[7:0]=0x00h	DDB1[7:0], DDB2[7:0], DDB3[7:0], DDB4[7:0]

6.2.68 SETCABC: Set CABC control (C9h)

C9H	SETCABC (Set CABC Control)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	0	0	1	C9
1st Parameter	1	1	↑	-	-	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY	(Depend on OSC speed)
2nd Parameter	1	1	↑	-	PWM_PERIOD[7:0]								-
3rd Parameter	1	1	↑	-	CABC_FSYNC	DIM_FRAME[6:0]							-
4th Parameter	1	1	↑	-		CABC_STEP[7:0]							-
5th Parameter	1	1	↑	-	CABC_CLKEN[7:0]								-
6th Parameter	1	1	↑	-	CABC_DD	SAVEPOWER[6:0]							-
7th Parameter	1	1	↑	-	MEAN_OFFSET[7:0]								
8th Parameter	1	1	↑	-	-	-	-	-	CABC_FLM[3:0]				
9th Parameter	1	1	↑	-	-	-	EN_DIM_MIX	EN_COST_MEAN	EN_COST	EN_NLN_GAIN	EN_JUDGE	EN_TEMP	

Description

This command is used to set CABC parameter.

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

SEL_BLDUTY: The backlight PWM output duty on/off control when CABC operated.
'0', The backlight PWM output duty is 100%.
'1', The backlight PWM output duty is calculated from CABC operation.

SEL_PWMCLK[2:0] : Internal PWM_CLK divider for CABC clock.

SEL_PWMCLK[2:0]/ DC_DIV1/ DC_DIV0			Brightness Control Clock
0	0	0	PWM_CLK / 1
0	0	1	PWM_CLK / 2
0	1	0	PWM_CLK / 4
0	1	1	PWM_CLK / 8
1	0	0	PWM_CLK / 16
1	0	1	PWM_CLK / 32
1	1	0	PWM_CLK / 64
1	1	1	PWM_CLK / 128

Note: PWM_CLK = OSC frequency / 4

PWM_PERIOD[7:0] : The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (SEL_PWMCLK)) x (255x(PWM_PERIOD[7:0])).

CABC_FSYNC: PWM output synchronize to VSYNC.

SAVEPOWER[6:0] : Minimum CABC gain / maximum CABC duty output select.

SAVEPOWER [6:0]							Min. Gain	Max. Duty
0	0	x	x	x	x	x	Reserve	
0	1	0	0	0	0	0	1+0/32	100%
0	1	0	0	0	0	1	1+1/32	96.97%
0	1	0	0	0	1	0	1+2/32	94.12%
0	1	0	0	0	1	1	1+3/32	91.43%
0	1	0	0	1	0	0	1+4/32	88.89%
0	1	0	0	1	0	1	1+5/32	86.49%
0	1	0	0	1	1	0	1+6/32	84.21%
0	1	0	0	1	1	1	1+7/32	82.05%

0	1	0	1	0	0	0	1+8/32	80%
0	1	0	1	0	0	1	1+9/32	78.05%
0	1	0	1	0	1	0	1+10/32	76.19%
0	1	0	1	0	1	1	1+11/32	74.42%
0	1	0	1	1	0	0	1+12/32	72.73%
0	1	0	1	1	0	1	1+13/32	71.11%
0	1	0	1	1	1	0	1+14/32	69.57%
0	1	0	1	1	1	1	1+15/32	68.09%
0	1	1	0	0	0	0	1+16/32	66.67%
0	1	1	0	0	0	1	1+17/32	65.31%
0	1	1	0	0	1	0	1+18/32	64%
0	1	1	0	0	1	1	1+19/32	62.75%
0	1	1	0	1	0	0	1+20/32	61.54%
0	1	1	0	1	0	1	1+21/32	60.38%
0	1	1	0	1	1	0	1+22/32	59.26%
0	1	1	0	1	1	1	1+23/32	58.18%
0	1	1	1	0	0	0	1+24/32	57.14%
0	1	1	1	0	0	1	1+25/32	56.14%
0	1	1	1	0	1	0	1+26/32	55.17%
0	1	1	1	0	1	1	1+27/32	54.24%
0	1	1	1	1	0	0	1+28/32	53.33%
0	1	1	1	1	0	1	1+29/32	52.46%
0	1	1	1	1	1	0	1+30/32	51.61%
0	1	1	1	1	1	1	1+31/32	50.79%
1	0	0	0	0	0	0	1+32/32	50%

For details, please refer to chapter “5.14 CABC Block”.

CABC_FLM[3:0]: CABC dimming frame number for each step.
CABC_DD_S: CABC dimming function enable bit.(Still mode)
‘0’, Disable CABC dimming.
‘1’, Enable CABC dimming.

CABC_DD_M: CABC dimming function enable bit.(Moving mode)
‘0’, Disable CABC dimming.
‘1’, Enable CABC dimming.

CABC_DD_U: CABC dimming function enable bit.(User Interface mode)
‘0’, Disable CABC dimming.
‘1’, Enable CABC dimming.

SEL_GAIN[1:0]: CABC gain select. **(Not Open)**
INVPULS: The backlight PWM output polarity select. **(Not Open)**
EN_DIX_MIX: (Not Open)
EN_COST: Cost adjust enable bit. **(Not Open)**
EN_COST_MEAN: (Not Open)
EN_NLN_GAIN: Non-linear gain enable bit. **(Not Open)**
EN_JUDGE: (Not Open)
EN_TEMP: Temporal weighting enable bit. **(Not Open)**
DIM_FRAME[6:0] : Manual brightness setting dimming period. **(Not Open)**
MEAN_OFFSET[7:0]: Increase calculated frame mean. **(Not Open)**
CABC_STEP[7:0]: (Not Open)
CABC_CLKEN[7:0]: (Not Open)
CABC_FSYNC: (Not Open)

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default		Status	Default value	OTP value		
		Power On Sequence S/W Reset H/W Reset	EN_DIM_MIX=1,EN_COST_MEAN=1,EN_COST=1 EN_NLN_GAIN=1, EN_JUDGE=1,EN_TEMP=0, CABC_DD=0, SAVEPOWER[6:0]=0x00h, MEAN_OFFSET[7:0]=0x00h, CABC_FLM[3:0]=4b'0001, SEL_PWMCLK[2:0]=3b'010, SEL_GAIN[1:0]=2b'11, CABC_FSYNC=0, INVPULS=1,SEL_BLDUTY=1, PWM_PERIOD[7:0]=0x2Bh, DIM_FRAME[6:0]=0x1Eh, CABC_STEP[7:0]=0x1Eh, CABC_CLKEN[7:0]=0x00h	CABC_DD, SAVEPOWER[6:0], SEL_PWMCLK[2:0], SEL_GAIN[1:0], CABC_FSYNC, INVPULS, SEL_BLDUTY, PWM_PERIOD[7:0], DIM_FRAME[6:0], CABC_STEP[7:0], CABC_CLKEN[7:0]		

6.2.69 SETCABCGAIN (CAh)

CAH	SETCABCGAIN												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	0	1	0	CA
1st Parameter	1	1	↑	-	0	DBG0[6:0]							-
2nd parameter	1	1	↑	-	0	DBG1[6:0]							-
3rd parameter	1	1	↑	-	0	DBG2[6:0]							-
4th parameter	1	1	↑	-	0	DBG3[6:0]							-
5th parameter	1	1	↑	-	0	DBG4[6:0]							-
6th parameter	1	1	↑	-	0	DBG5[6:0]							-
7th parameter	1	1	↑	-	0	DBG6[6:0]							-
8th parameter	1	1	↑	-	0	DBG7[6:0]							-
9th parameter	1	1	↑	-	0	DBG8[6:0]							-

Description

DBG0~8[6:0] : Gain select register 0~8.

DBG0~8[6:0]							CABC Gain	CABC Duty
0	0	x	x	x	x	x	Reserve	
0	1	0	0	0	0	0	1+0/32	100%
0	1	0	0	0	0	1	1+1/32	96.97%
0	1	0	0	0	1	0	1+2/32	94.12%
0	1	0	0	0	1	1	1+3/32	91.43%
0	1	0	0	1	0	0	1+4/32	88.89%
0	1	0	0	1	0	1	1+5/32	86.49%
0	1	0	0	1	1	0	1+6/32	84.21%
0	1	0	0	1	1	1	1+7/32	82.05%
0	1	0	1	0	0	0	1+8/32	80%
0	1	0	1	0	0	1	1+9/32	78.05%
0	1	0	1	0	1	0	1+10/32	76.19%
0	1	0	1	0	1	1	1+11/32	74.42%
0	1	0	1	1	0	0	1+12/32	72.73%
0	1	0	1	1	0	1	1+13/32	71.11%
0	1	0	1	1	1	0	1+14/32	69.57%
0	1	0	1	1	1	1	1+15/32	68.09%
0	1	1	0	0	0	0	1+16/32	66.67%
0	1	1	0	0	0	1	1+17/32	65.31%
0	1	1	0	0	1	0	1+18/32	64%
0	1	1	0	0	1	1	1+19/32	62.75%
0	1	1	0	1	0	0	1+20/32	61.54%
0	1	1	0	1	0	1	1+21/32	60.38%
0	1	1	0	1	1	0	1+22/32	59.26%
0	1	1	0	1	1	1	1+23/32	58.18%
0	1	1	1	0	0	0	1+24/32	57.14%
0	1	1	1	0	0	1	1+25/32	56.14%
0	1	1	1	0	1	0	1+26/32	55.17%
0	1	1	1	0	1	1	1+27/32	54.24%
0	1	1	1	1	0	0	1+28/32	53.33%
0	1	1	1	1	0	1	1+29/32	52.46%
0	1	1	1	1	1	0	1+30/32	51.61%
0	1	1	1	1	1	1	1+31/32	50.79%
1	0	0	0	0	0	0	1+32/32	50%

For details, please refer to chapter “5.14 CABC Block”.

Restrictions	SETEXTC turn on to enable this command.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default value</th><th>OTP value</th></tr>
<tr><td>Power On Sequence
S/W Reset
H/W Reset</td><td>DBG0[6:0]=0x40h,
DBG1[6:0]=0x3Ch,
DBG2[6:0]=0x38h,
DBG3[6:0]=0x34h,
DBG4[6:0]=0x33h,
DBG5[6:0]=0x32h,
DBG6[6:0]=0x2Bh,
DBG7[6:0]=0x24h,
DBG8[6:0]=0x22h</td><td>DBG0[6:0], DBG1[6:0],
DBG2[6:0], DBG3[6:0],
DBG4[6:0], DBG5[6:0],
DBG6[6:0], DBG7[6:0],
DBG8[6:0]</td></tr>
</table>
</td></tr>
</table>

6.2.70 SETPANEL (CCh)

CCH	SETPANEL(Set panel related register)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	1	0	0	CC
1st parameter	1	1	↑	-	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	-
Description0	This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user **BGR_PANEL**: The order of <R><G><B> dot color for module supplier, default value is stored in OTP. If color filter of panel is <B><G><R> type, setting BGR_PANEL = 1, if color filter of panel is <R><G><B> type, setting BGR_PANEL = 0. This bit is to make panel module look like a <R><G><B> type panel form the user viewpoint. **GS_PANEL**: Specify the shift direction of gate driver output. When GS_PANEL = 0, the LTPS control signal is normal scan. When GS_PANEL = 1, the LTPS control signal is reverse scan. **SS_PANEL**: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S800 When SS_PANEL = 1, the shift direction from S800 to S1. **REV_PANEL:** Select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally-white and normally-black panels. REV_PANEL = 1 normal-white panel REV_PANEL = 0 normal-black panel												
Restrictions	SETEXTC turn on to enable this command												
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Status: Default value: OTP value Power On Sequence S/W Reset H/W Reset: SS_PANEL=0, GS_PANEL=0, REV_PANE=0, BGR_PANEL=0: SS_PANEL, GS_PANEL, REV_PANE, BGR_PANEL												

6.2.71 SETEQ (D4h)

D4H	SETEQ(Set EQ function)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	1	0	0	D4
1st parameter	1	1	↑	-	-	-	-	-	EQ_GR	EQ_GF	-	-	-
Description0	This command is used to set setting of EQ function for gate driver control signal. **EQ_GR:** The bit is set rise time EQ function. **EQ_GR** / **EQ of rise time**: 0 = Enable; 1 = Disable **EQ_GF:** The bit is set fall time EQ function. **EQ_GF** / **EQ of fall time**: 0 = Enable; 1 = Disable												
Restrictions	SETEXTC turn on to enable this command												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence, S/W Reset, H/W Reset — Default value: EQ_GR=1, EQ_GF=1 — OTP value: -												

6.2.72 SEGCKEQ: Set GCK EQ function (D5h)

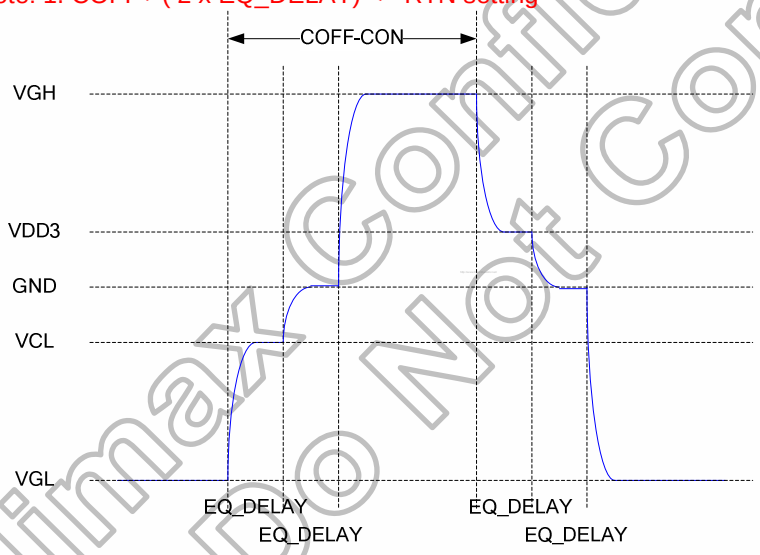
D5H	SETTE (Set internal TE function)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	1	0	1	D5
1st parameter	1	1	↑	-	0	0	0	0	0	0	0	0	00
2nd parameter	1	1	↑	-	0	0	0	0	0	0	0	0	00
3rd parameter	1	1	↑	-	EQ_DELAY[7:0]								-

Description

EQ_DELAY[7:0]: The timing definition of GCK EQ.

N_t9[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

Note: 1. COFF+ (2 x EQ_DELAY) <= RTN setting



Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	EQ_DELAY[7:0]= 0x08h	-

6.2.73 SETRGBCYC: Set RGB/Video mode panel driving timing(RD8h)

D8H	SETRGBCYC(Set RGB/Video mode panel driving timing)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	0	0	EB
1st Parameter	1	1	↑	-	-	-	NW_PE[2:0]			NW[2:0]			-
2nd Parameter					-	-	-	-	SHR[11:8]				
3rd Parameter	1	1	↑	-	SHR[7:0]								-
4th Parameter	1	1	↑	-	SPON[7:0]								-
5th Parameter	1	1	↑	-	SPOFF[7:0]								-
6th Parameter	1	1	↑	-	CHR[7:0]								-
7th Parameter	1	1	↑	-	CON[7:0]								
8th Parameter	1	1	↑	-	COFF[7:0]								-
9th Parameter	1	1	↑	-	SHP[3:0]				-	-	-	-	
10th Parameter	1	1	↑	-	CHP[3:0]				CCP[3:0]				-
11th Parameter	1	1	↑	-	N_t1[7:0]								-
12th Parameter	1	1	↑	-	N_t2[7:0]								-
13th Parameter	1	1	↑	-	N_t3[7:0]								-
14th Parameter	1	1	↑	-	N_t4[7:0]								-
15th Parameter	1	1	↑	-	N_t5[7:0]								-
16th Parameter	1	1	↑	-	N_t6[7:0]								-
17th Parameter	1	1	↑	-	N_t7[7:0]								-
18th Parameter	1	1	↑	-	N_t8[7:0]								-
19th Parameter	1	1	↑	-	N_t9[7:0]								-
20th Parameter	1	1	↑	-	-	-	-	-	EOT[3:0]				-

Description

This command is used to get setting of display waveform cycles for RGB mode or Video mode.

NW[2:0]: Inversion type setting.
NW_PE[2:0]: Inversion type setting on partial idle mode.

NW2	NW1	NW0	Inversion type
0	0	0	Column inversion
0	0	1	1-dot inversion
0	1	0	2-dot inversion
0	1	1	4-dot inversion
1	0	0	Inhibit
1	0	1	Inhibit
1	1	0	Inhibit
1	1	1	Inhibit

SHR[11:0]: GSP Hsync Rise.

SHR_0[7:0]	Start Pulse Output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFFEh	1022 x HSYNC
0xFFFh	1023 x HSYNC

SPON[7:0]: GSP Pulse Delay.

SPON[7:0]	Start Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •

0xFEh	1016 x OSC CLK
0xFFh	1020 x OSC CLK

Note: 1. SPON[7:0] < SPOFF[7:0] ≤ RTN[7:0]

SPOFF[7:0]: GSP Pulse width.

SPON[7:0]	Start Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 x OSC CLK
0xFFh	1020 x OSC CLK

Note: 1. SPON[7:0] < SPOFF[7:0] ≤ RTN[7:0]

SHP[3:0]: Width of GSP High pulse.

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		• • • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CHR[7:0]: CK Hsync Rise.

CHR[7:0]	CK Pulse start output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFFEh	510 x HSYNC
0xFFFh	511 x HSYNC

CON[7:0]: CK Pulse Delay.

CON[7:0]	CK Pulse Output delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 x OSC CLK
0xFFh	1020 x OSC CLK

Note: 1. CON[7:0] < COFF[7:0] ≤ RTN[7:0]

COFF[7:0]: CK Pulse width.

COFF[7:0]	CK Pulse Output
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
	• • • • •
0xFEh	1016 x OSC CLK

0xFFh	1020 x OSC CLK

Note: 1. CON[7:0] < COFF[7:0] ≤ RTN[7:0]

CHP[3:0]: Width of CK High pulse.

CHP3	CHP2	CHP1	CHP0	CK Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
. . . . .				
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CCP[3:0]: A Cycle of CK pulse.

CCP3	CCP2	CCP1	CCP0	CK Pulse cycle
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
. . . . .				
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

N_t1[7:0]: The timing definition of t1.

N_t1[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t2[7:0]: The timing definition of t2.

N_t2[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t3[7:0]: The timing definition of t3.

N_t3[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK

. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t4[7:0]: The timing definition of t4.

N_t4[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t5[7:0]: The timing definition of t5.

N_t5[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t6[7:0]: The timing definition of t6.

N_t6[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t7[7:0] : The timing definition of t7.

N_t1[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t8[7:0]: The timing definition of t8.

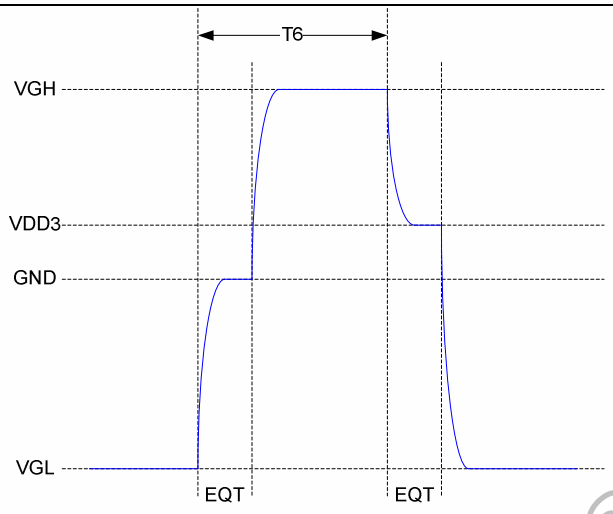
N_t8[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

N_t9[7:0]: The timing definition of t9.

N_t9[7:0]								Clock cycles
0	0	0	0	0	0	0	0	0 x OSC CLK
0	0	0	0	0	0	0	1	4 x OSC CLK
0	0	0	0	0	0	1	0	8 x OSC CLK
0	0	0	0	0	0	1	1	12 x OSC CLK
0	0	0	0	0	1	0	0	16 x OSC CLK
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	1	0	0	1008 x OSC CLK
1	1	1	1	1	1	0	1	1012 x OSC CLK
1	1	1	1	1	1	1	0	1016 x OSC CLK
1	1	1	1	1	1	1	1	1020 x OSC CLK

EQT[3:0]: Equalizing period of TG output

EQT3	EQT2	EQT1	EQT0	Clock cycles
0	0	0	0	0
0	0	0	1	4
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	20
0	1	1	0	24
0	1	1	1	28
1	0	0	0	32
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

	
Restrictions	-
Register Availability	
Default	
Flow Chart	

6.2.74 SETGAMMA: Set gamma curve related setting (E0h)

E0H	SETGAMMAR (Set Gamma Curve Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	1	↑	-	-	-	R_VRP0[5:0]						xx
2nd parameter	1	1	↑	-	-	-	R_VRP1[5:0]						xx
3rd Parameter	1	1	↑	-	-	-	R_VRP2[5:0]						xx
4th Parameter	1	1	↑	-	-	-	R_VRP3[5:0]						xx
5th Parameter	1	1	↑	-	-	-	R_VRP4[5:0]						xx
6th Parameter	1	1	↑	-	-	-	R_VRP5[5:0]						xx
7th Parameter	1	1	↑	-	-	R_PRP0[6:0]							xx
8th Parameter	1	1	↑	-	-	R_PRP1[6:0]							xx
9th Parameter	1	1	↑	-	-	-	-	R_PKP0[4:0]					xx
10th Parameter	1	1	↑	-	-	-	-	R_PKP1[4:0]					xx
11th Parameter	1	1	↑	-	-	-	-	R_PKP2[4:0]					xx
12th Parameter	1	1	↑	-	-	-	-	R_PKP3[4:0]					xx
13th Parameter	1	1	↑	-	-	-	-	R_PKP4[4:0]					xx
14th Parameter	1	1	↑	-	-	-	-	R_PKP5[4:0]					xx
15th Parameter	1	1	↑	-	-	-	-	R_PKP6[4:0]					xx
16th Parameter	1	1	↑	-	-	-	-	R_PKP7[4:0]					xx
17th Parameter	1	1	↑	-	-	-	-	R_PKP8[4:0]					xx
18th Parameter	1	1	↑	-	-	-	R_VRN0[5:0]						xx
19th Parameter	1	1	↑	-	-	-	R_VRN1[5:0]						xx
20th Parameter	1	1	↑	-	-	-	R_VRN2[5:0]						xx
21th Parameter	1	1	↑	-	-	-	R_VRN3[5:0]						xx
22th Parameter	1	1	↑	-	-	-	R_VRN4[5:0]						xx
23th Parameter	1	1	↑	-	-	-	R_VRN5[5:0]						xx
24th Parameter	1	1	↑	-	-	R_PRN0[6:0]							xx
25th Parameter	1	1	↑	-	-	R_PRN1[6:0]							xx
26th Parameter	1	1	↑	-	-	-	-	R_PKN0[4:0]					xx
27th Parameter	1	1	↑	-	-	-	-	R_PKN1[4:0]					xx
28th Parameter	1	1	↑	-	-	-	-	R_PKN2[4:0]					xx
29th Parameter	1	1	↑	-	-	-	-	R_PKN3[4:0]					xx
30th Parameter	1	1	↑	-	-	-	-	R_PKN4[4:0]					xx
31th Parameter	1	1	↑	-	-	-	-	R_PKN5[4:0]					xx
32th Parameter	1	1	↑	-	-	-	-	R_PKN6[4:0]					xx
33th Parameter	1	1	↑	-	-	-	-	R_PKN7[4:0]					xx
34th Parameter	1	1	↑	-	-	-	-	R_PKN8[4:0]					xx

Description

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	R_PRP0 6-0	R_PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	R_PRP1 6-0	R_PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	R_PKP0 4-0	R_PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	R_PKP1 4-0	R_PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	R_PKP2 4-0	R_PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	R_PKP3 4-0	R_PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	R_PKP4 4-0	R_PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	R_PKP5 4-0	R_PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	R_PKP6 4-0	R_PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	R_PKP7 4-0	R_PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	R_PKP8 4-0	R_PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	R_VRP0 5-0	R_VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	R_VRP1 5-0	R_VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	R_VRP2 5-0	R_VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	R_ VRP3 5-0	R_VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	R_VRP4 5-0	R_VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	R_VRP5 5-0	R_VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	R_VRP0[5:0]=0x04h, R_VRP1[5:0]=0x0Ch, R_VRP2[5:0]=0x0Dh, R_VRP3[5:0]=0x0Ah, R_VRP4[5:0]=0x15h, R_VRP5[5:0]=0x21h, R_PRP0[6:0]=0x0Dh, R_PRP1[6:0]=0x19h, R_ PKP0[4:0]=0x06h, R_ PKP1[4:0]=0x0Ch, R_ PKP2[4:0]=0x0Fh, R_ PKP3[4:0]=0x13h, R_ PKP4[4:0]=0x16h, R_ PKP5[4:0]=0x14h, R_ PKP6[4:0]=0x15h, R_ PKP7[4:0]=0x0Dh, R_ PKP8[4:0]=0x13h, R_VRN0[5:0]=0x04h, R_VRN1[5:0]=0x0Ch, R_VRN2[5:0]=0x0Dh, R_VRN3[5:0]=0x0Ah, R_VRN4[5:0]=0x15h, R_VRN5[5:0]=0x21h, R_PRN0[6:0]=0x0Dh, R_PRN1[6:0]=0x19h, R_ PKN0[4:0]=0x06h, R_ PKN1[4:0]=0x0Ch, R_ PKN2[4:0]=0x0Fh, R_ PKN3[4:0]=0x13h, R_ PKN4[4:0]=0x16h, R_ PKN5[4:0]=0x14h, R_ PKN6[4:0]=0x15h, R_ PKN7[4:0]=0x0Dh, R_ PKN8[4:0]=0x13h	R_VRP0[5:0], R_VRP1[5:0], R_VRP2[5:0], R_VRP3[5:0], R_VRP4[5:0], R_VRP5[5:0], R_PRP0[6:0], R_PRP1[6:0], R_ PKP0[4:0], R_ PKP1[4:0], R_ PKP2[4:0], R_ PKP3[4:0], R_ PKP4[4:0], R_ PKP5[4:0], R_ PKP6[4:0], R_ PKP7[4:0], R_ PKP8[4:0], R_VRN0[5:0], R_VRN1[5:0], R_VRN2[5:0], R_VRN3[5:0], R_VRN4[5:0], R_VRN5[5:0], R_PRP0[6:0], R_PRP1[6:0], R_ PKN0[4:0], R_ PKN1[4:0], R_ PKN2[4:0], R_ PKN3[4:0], R_ PKN4[4:0], R_ PKN5[4:0], R_ PKN6[4:0], R_ PKN7[4:0], R_ PKN8[4:0]

6.2.75 SETGGAMMA: Set green gamma curve related setting (E1h)

E1H	SETGAMMAR (Set Gamma Curve Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	0	1	E1
1st parameter	1	1	↑	-	-	-	G_VRP0[5:0]						xx
2nd parameter	1	1	↑	-	-	-	G_VRP1[5:0]						xx
3rd Parameter	1	1	↑	-	-	-	G_VRP2[5:0]						xx
4th Parameter	1	1	↑	-	-	-	G_VRP3[5:0]						xx
5th Parameter	1	1	↑	-	-	-	G_VRP4[5:0]						xx
6th Parameter	1	1	↑	-	-	-	G_VRP5[5:0]						xx
7th Parameter	1	1	↑	-	-	G_PRP0[6:0]							xx
8th Parameter	1	1	↑	-	-	G_PRP1[6:0]							xx
9th Parameter	1	1	↑	-	-	-	-	G_PKP0[4:0]					xx
10th Parameter	1	1	↑	-	-	-	-	G_PKP1[4:0]					xx
11th Parameter	1	1	↑	-	-	-	-	G_PKP2[4:0]					xx
12th Parameter	1	1	↑	-	-	-	-	G_PKP3[4:0]					xx
13th Parameter	1	1	↑	-	-	-	-	G_PKP4[4:0]					xx
14th Parameter	1	1	↑	-	-	-	-	G_PKP5[4:0]					xx
15th Parameter	1	1	↑	-	-	-	-	G_PKP6[4:0]					xx
16th Parameter	1	1	↑	-	-	-	-	G_PKP7[4:0]					xx
17th Parameter	1	1	↑	-	-	-	-	G_PKP8[4:0]					xx
18th Parameter	1	1	↑	-	-	-	G_VRN0[5:0]						xx
19th Parameter	1	1	↑	-	-	-	G_VRN1[5:0]						xx
20th Parameter	1	1	↑	-	-	-	G_VRN2[5:0]						xx
21th Parameter	1	1	↑	-	-	-	G_VRN3[5:0]						xx
22th Parameter	1	1	↑	-	-	-	G_VRN4[5:0]						xx
23th Parameter	1	1	↑	-	-	-	G_VRN5[5:0]						xx
24th Parameter	1	1	↑	-	-	G_PRN0[6:0]							xx
25th Parameter	1	1	↑	-	-	G_PRN1[6:0]							xx
26th Parameter	1	1	↑	-	-	-	-	G_PKN0[4:0]					xx
27th Parameter	1	1	↑	-	-	-	-	G_PKN1[4:0]					xx
28th Parameter	1	1	↑	-	-	-	-	G_PKN2[4:0]					xx
29th Parameter	1	1	↑	-	-	-	-	G_PKN3[4:0]					xx
30th Parameter	1	1	↑	-	-	-	-	G_PKN4[4:0]					xx
31th Parameter	1	1	↑	-	-	-	-	G_PKN5[4:0]					xx
32th Parameter	1	1	↑	-	-	-	-	G_PKN6[4:0]					xx
33th Parameter	1	1	↑	-	-	-	-	G_PKN7[4:0]					xx
34th Parameter	1	1	↑	-	-	-	-	G_PKN8[4:0]					xx

Description

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	G_PRP0 6-0	G_PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	G_PRP1 6-0	G_PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	G_PKP0 4-0	G_PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	G_PKP1 4-0	G_PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	G_PKP2 4-0	G_PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	G_PKP3 4-0	G_PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	G_PKP4 4-0	G_PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	G_PKP5 4-0	G_PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	G_PKP6 4-0	G_PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	G_PKP7 4-0	G_PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	G_PKP8 4-0	G_PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	G_VRP0 5-0	G_VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	G_VRP1 5-0	G_VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	G_VRP2 5-0	G_VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	G_ VRP3 5-0	G_VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	G_VRP4 5-0	G_VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	G_VRP5 5-0	G_VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	G_VRP0[5:0]=0x04h, G_VRP1[5:0]=0x0Ch, G_VRP2[5:0]=0x0Dh, G_VRP3[5:0]=0x0Ah, G_VRP4[5:0]=0x15h, G_VRP5[5:0]=0x21h, G_PRP0[6:0]=0x0Dh, G_PRP1[6:0]=0x19h, G_ PKP0[4:0]=0x06h, G_ PKP1[4:0]=0x0Ch, G_ PKP2[4:0]=0x0Fh, G_ PKP3[4:0]=0x13h, G_ PKP4[4:0]=0x16h, G_ PKP5[4:0]=0x14h, G_ PKP6[4:0]=0x15h, G_ PKP7[4:0]=0x0Dh, G_ PKP8[4:0]=0x13h, G_VRN0[5:0]=0x04h, G_VRN1[5:0]=0x0Ch, G_VRN2[5:0]=0x0Dh, G_VRN3[5:0]=0x0Ah, G_VRN4[5:0]=0x15h, G_VRN5[5:0]=0x21h, G_PRN0[6:0]=0x0Dh, G_PRN1[6:0]=0x19h, G_ PKN0[4:0]=0x06h, G_ PKN1[4:0]=0x0Ch, G_ PKN2[4:0]=0x0Fh, G_ PKN3[4:0]=0x13h, G_ PKN4[4:0]=0x16h, G_ PKN5[4:0]=0x14h, G_ PKN6[4:0]=0x15h, G_ PKN7[4:0]=0x0Dh, G_ PKN8[4:0]=0x13h	G_VRP0[5:0], G_VRP1[5:0], G_VRP2[5:0], G_VRP3[5:0], G_VRP4[5:0], G_VRP5[5:0], G_PRP0[6:0], G_PRP1[6:0], G_ PKP0[4:0], G_ PKP1[4:0], G_ PKP2[4:0], G_ PKP3[4:0], G_ PKP4[4:0], G_ PKP5[4:0], G_ PKP6[4:0], G_ PKP7[4:0], G_ PKP8[4:0], G_VRN0[5:0], G_VRN1[5:0], G_VRN2[5:0], G_VRN3[5:0], G_VRN4[5:0], G_VRN5[5:0], G_PRP0[6:0], G_PRP1[6:0], G_ PKN0[4:0], G_ PKN1[4:0], G_ PKN2[4:0], G_ PKN3[4:0], G_ PKN4[4:0], G_ PKN5[4:0], G_ PKN6[4:0], G_ PKN7[4:0], G_ PKN8[4:0]

6.2.76 SETBGAMMA: Set green blue curve related setting (E2h)

E2H	SETGAMMAR (Set Gamma Curve Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	1	0	E2
1st parameter	1	1	↑	-	-	-	B_VRP0[5:0]						xx
2nd parameter	1	1	↑	-	-	-	B_VRP1[5:0]						xx
3rd Parameter	1	1	↑	-	-	-	B_VRP2[5:0]						xx
4th Parameter	1	1	↑	-	-	-	B_VRP3[5:0]						xx
5th Parameter	1	1	↑	-	-	-	B_VRP4[5:0]						xx
6th Parameter	1	1	↑	-	-	-	B_VRP5[5:0]						xx
7th Parameter	1	1	↑	-	-	B_PRP0[6:0]							xx
8th Parameter	1	1	↑	-	-	B_PRP1[6:0]							xx
9th Parameter	1	1	↑	-	-	-	-	B_PKP0[4:0]					xx
10th Parameter	1	1	↑	-	-	-	-	B_PKP1[4:0]					xx
11th Parameter	1	1	↑	-	-	-	-	B_PKP2[4:0]					xx
12th Parameter	1	1	↑	-	-	-	-	B_PKP3[4:0]					xx
13th Parameter	1	1	↑	-	-	-	-	B_PKP4[4:0]					xx
14th Parameter	1	1	↑	-	-	-	-	B_PKP5[4:0]					xx
15th Parameter	1	1	↑	-	-	-	-	B_PKP6[4:0]					xx
16th Parameter	1	1	↑	-	-	-	-	B_PKP7[4:0]					xx
17th Parameter	1	1	↑	-	-	-	-	B_PKP8[4:0]					xx
18th Parameter	1	1	↑	-	-	-	B_VRN0[5:0]						xx
19th Parameter	1	1	↑	-	-	-	B_VRN1[5:0]						xx
20th Parameter	1	1	↑	-	-	-	B_VRN2[5:0]						xx
21th Parameter	1	1	↑	-	-	-	B_VRN3[5:0]						xx
22th Parameter	1	1	↑	-	-	-	B_VRN4[5:0]						xx
23th Parameter	1	1	↑	-	-	-	B_VRN5[5:0]						xx
24th Parameter	1	1	↑	-	-	B_PRN0[6:0]							xx
25th Parameter	1	1	↑	-	-	B_PRN1[6:0]							xx
26th Parameter	1	1	↑	-	-	-	-	B_PKN0[4:0]					xx
27th Parameter	1	1	↑	-	-	-	-	B_PKN1[4:0]					xx
28th Parameter	1	1	↑	-	-	-	-	B_PKN2[4:0]					xx
29th Parameter	1	1	↑	-	-	-	-	B_PKN3[4:0]					xx
30th Parameter	1	1	↑	-	-	-	-	B_PKN4[4:0]					xx
31th Parameter	1	1	↑	-	-	-	-	B_PKN5[4:0]					xx
32th Parameter	1	1	↑	-	-	-	-	B_PKN6[4:0]					xx
33th Parameter	1	1	↑	-	-	-	-	B_PKN7[4:0]					xx
34th Parameter	1	1	↑	-	-	-	-	B_PKN8[4:0]					xx

Description

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	B_PRP0 6-0	B_PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	B_PRP1 6-0	B_PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	B_PKP0 4-0	B_PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	B_PKP1 4-0	B_PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	B_PKP2 4-0	B_PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	B_PKP3 4-0	B_PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	B_PKP4 4-0	B_PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	B_PKP5 4-0	B_PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	B_PKP6 4-0	B_PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	B_PKP7 4-0	B_PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	B_PKP8 4-0	B_PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	B_VRP0 5-0	B_VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	B_VRP1 5-0	B_VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	B_VRP2 5-0	B_VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	B_ VRP3 5-0	B_VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	B_VRP4 5-0	B_VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	B_VRP5 5-0	B_VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	B_VRP0[5:0]=0x04h, B_VRP1[5:0]=0x0Ch, B_VRP2[5:0]=0x0Dh, B_VRP3[5:0]=0x0Ah, B_VRP4[5:0]=0x15h, B_VRP5[5:0]=0x21h, B_PRP0[6:0]=0x0Dh, B_PRP1[6:0]=0x19h, B_ PKP0[4:0]=0x06h, B_ PKP1[4:0]=0x0Ch, B_ PKP2[4:0]=0x0Fh, B_ PKP3[4:0]=0x13h, B_ PKP4[4:0]=0x16h, B_ PKP5[4:0]=0x14h, B_ PKP6[4:0]=0x15h, B_ PKP7[4:0]=0x0Dh, B_ PKP8[4:0]=0x13h, B_VRN0[5:0]=0x04h, B_VRN1[5:0]=0x0Ch, B_VRN2[5:0]=0x0Dh, B_VRN3[5:0]=0x0Ah, B_VRN4[5:0]=0x15h, B_VRN5[5:0]=0x21h, B_PRN0[6:0]=0x0Dh, B_PRN1[6:0]=0x19h, B_ PKN0[4:0]=0x06h, B_ PKN1[4:0]=0x0Ch, B_ PKN2[4:0]=0x0Fh, B_ PKN3[4:0]=0x13h, B_ PKN4[4:0]=0x16h, B_ PKN5[4:0]=0x14h, B_ PKN6[4:0]=0x15h, B_ PKN7[4:0]=0x0Dh, B_ PKN8[4:0]=0x13h	B_VRP0[5:0], B_VRP1[5:0], B_VRP2[5:0], B_VRP3[5:0], B_VRP4[5:0], B_VRP5[5:0], B_PRP0[6:0], B_PRP1[6:0], B_ PKP0[4:0], B_ PKP1[4:0], B_ PKP2[4:0], B_ PKP3[4:0], B_ PKP4[4:0], B_ PKP5[4:0], B_ PKP6[4:0], B_ PKP7[4:0], B_ PKP8[4:0], B_VRN0[5:0], B_VRN1[5:0], B_VRN2[5:0], B_VRN3[5:0], B_VRN4[5:0], B_VRN5[5:0], B_PRP0[6:0], B_PRP1[6:0], B_ PKN0[4:0], B_ PKN1[4:0], B_ PKN2[4:0], B_ PKN3[4:0], B_ PKN4[4:0], B_ PKN5[4:0], B_ PKN6[4:0], B_ PKN7[4:0], B_ PKN8[4:0]

6.2.77 SETCHEMODE (E3h)

E3H	SETCHEMODE (Set color enhancement mode)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	1	1	E3
1st parameter	1	1	↑	-	-	-	SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]		-

Description

This command is used to set setting of color enhancement function.

SE_MODE[1:0]: The bit is set sharpness enhancement function.

SE_MODE[1:0]	Sharpness enhancement
00	Disable
01	Lower
10	Middle
11	High

BE_MODE[1:0]: The bit is set brightness enhancement function.

BE_MODE[1:0]	Brightness enhancement
00	Disable
01	Lower
10	Middle
11	High

CE_MODE[1:0]: The bit is set color enhancement function.

CE_MODE[1:0]	Color enhancement
00	Disable
01	Lower
10	Middle
11	High

Restrictions

SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	SE_MODE[1:0]=00, BE_MODE[1:0]=00, CE_MODE[1:0]=00	-

6.2.78 SETOTPKEY (E9h)

E9H	SETOTPKEY												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	1	0	0	1	E9
1st parameter	1	1	↑	-	OTP_KEY0[7:0]								00h
2nd parameter	1	1	↑	-	OTP_KEY1[7:0]								00h

Description

This command is used to set OTP key to enter or leave OTP program mode.

OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	1. If HX8392-A operate on OTP program mode, Then keep on OTP program mode. 2. If HX8392-A operate on non-OTP program mode, Then keep on non-OTP program mode.

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	OTP_KEY0[7:0]=0x00h, OTP_KEY1[7:0]=0x00h	N/A

6.2.79 GETHXID (F4h)

F4H	GETHXIC												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	0	1	0	0	F4
1st parameter	1	↑	1	-	Himax ID[7:0]								92
Description	This command is used to get Driver IC ID code.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	Himax ID[7:0] = 0x92h	N/A

6.2.80 GETDB (F7h)

F7H	GETDB												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	0	1	1	1	F7
1st parameter	1	↑	1	-	DB[7:0]								xx
Description	This command is used to get DB[7:0] status.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	N/A	N/A

7. Layout Recommendation

7.1 Layout Recommendation

7.1.1 Architecture 1 – Internal charge pumping circuit

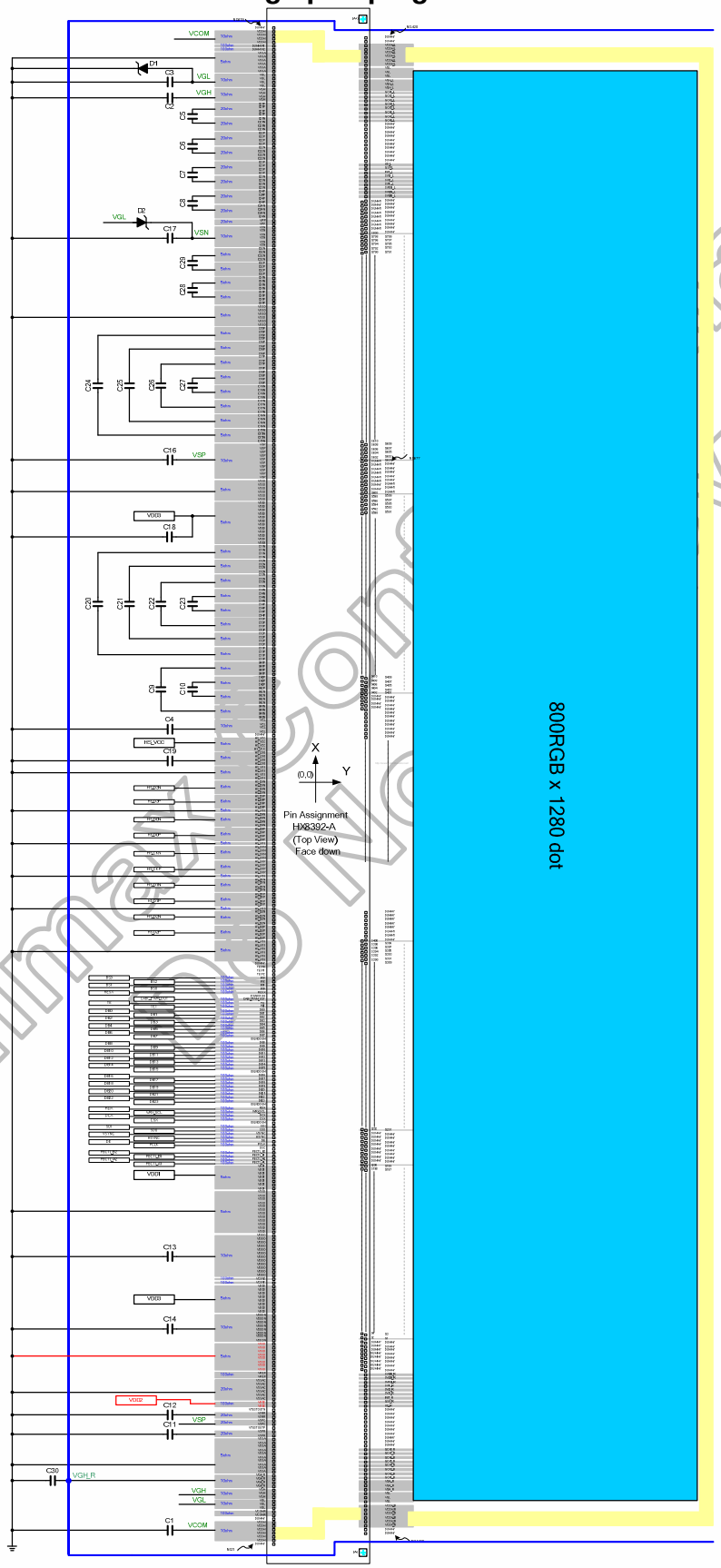


Figure 7.1: Layout Recommendation of Internal charge pumping circuit

7.1.2 Architecture 2 - HX5186-A

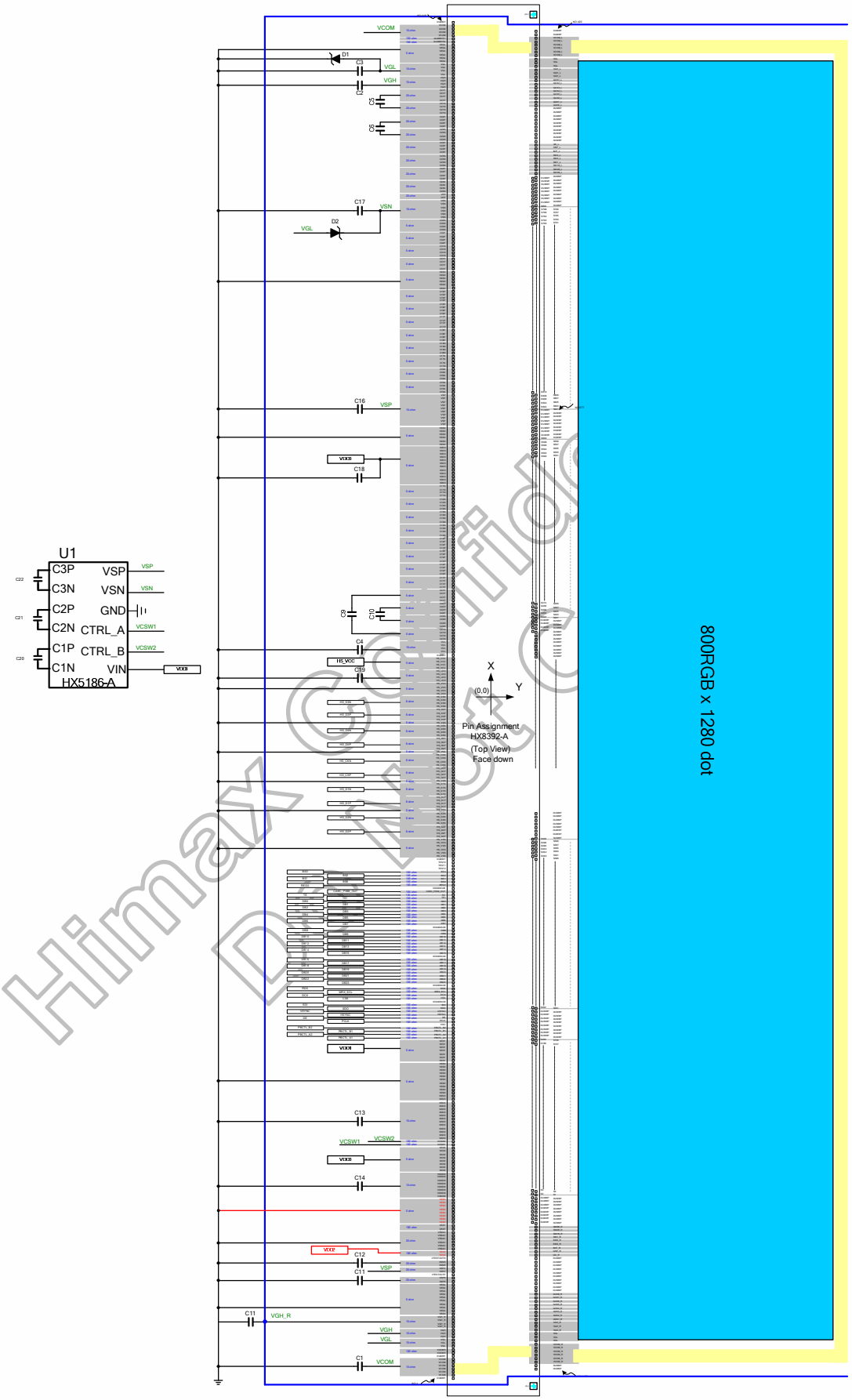


Figure 7.2: Layout Recommendation of HX5186-A

7.2 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	5	Ω
VDD2	Power supply	5	Ω
VDD3	Power supply	5	Ω
VSSD	Power supply	5	Ω
VSSA	Power supply	5	Ω
HS_VCC	Power supply	5	Ω
HS_VSS	Power supply	5	Ω
VSSAC	Power supply	20	Ω
BS[3:0]	Input	100	Ω
RDX, WRX_SCL, DCX, CSX, RESX	Input	100	Ω
HSYNC, VSYNC, DE, PCLK	Input	100	Ω
SDI	Input	100	Ω
SDO	Output	100	Ω
DB[23:0]	Input + Output	100	Ω
CABC_PWM_OUT, TE, TE1, PBCTL_A1, PBCTL_A2 PBCTL_B1, PBCTL_B2 VCSW1, VCSW2	Output	100	Ω
VCOM	Output	10	Ω
HS_CP, HS_CN	Input	6	Ω
HS_D0P, HS_D0N	Input + Output	6	Ω
HS_D1P, HS_D1N	Input	6	Ω
HS_D2P, HS_D2N	Input	6	Ω
HS_D3P, HS_D3N	Input	6	Ω
VDDD	Capacitor Connection	5	Ω
VDDDN	Capacitor Connection	10	Ω
VSP	Capacitor Connection	10	Ω
VSN	Capacitor Connection	10	Ω
VSPR, VSNR	Capacitor Connection	20	Ω
VREF, VPP	Capacitor Connection	20	Ω
VGH, VGL, VCL, VGH_R	Capacitor Connection	10	Ω
HS_LDO	Capacitor Connection	10	Ω
OSC	Input	100	Ω
C11P, C11N, C12P, C12N, C13P, C13N, C14P, C14N, C15P, C15N, C16P, C16N, C17P, C17N, C18P, C18N, C31P, C31N, C32P, C32N, C41P, C41N, C42P, C42N	Capacitor Connection	5	Ω
C21P, C21N, C22P, C22N C23P, C23N, C24P, C24N	Capacitor Connection	20	Ω
TEST[2:0]	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω

Table 7.1: Maximum Layout Resistance

7.3 External Components Connection

Internal charge pumping mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
VGL	C3	Connect to Capacitor (Max 16V): VGL ---(+)----| |--- (-)----- VSSA	1.0 µF
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VCL	C4	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	1.0 µF
C21P – C21N	C5	Connect to Capacitor (Max 16V): C21P ---(+)----| |--- (-)-----C21N	1.0 µF
C22P – C22N	C6	Connect to Capacitor (Max 16V): C22P ---(+)----| |--- (-)-----C22N	1.0 µF
C23P – C23N	C7	Connect to Capacitor (Max 16V): C23P ---(+)----| |--- (-)-----C23N	1.0 µF
C24P – C24N	C8	Connect to Capacitor (Max 16V): C24P ---(+)----| |--- (-)-----C24N	1.0 µF
C41P – C41N	C9	Connect to Capacitor (Max 6V): C41P ---(+)----| |--- (-)-----C41N	1.0 µF
C42P – C42N	C10	Connect to Capacitor (Max 6V): C42P ---(+)----| |--- (-)-----C42N	1.0 µF
VSPR	C11	Connect to Capacitor (Max 10V): VSPR ---(+)----| |--- (-)-----VSSA	1.0 µF
VSNR	C12	Connect to Capacitor (Max 10V): VSNR ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDD	C13	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDDN	C14	Connect to Capacitor (Max 6V): VDDDN ---(+)----| |--- (-)-----VSSA	1.0 µF
VREF	C15	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 µF
VSP	C16	Connect to Capacitor (Max 10V):VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VSN	C17	Connect to Capacitor (Max 10V):VSN ---(+)----| |--- (-)-----VSSA	2.2 µF
	D2	Connect to Schottky Diode(VR≥30V): VSN ---(-)----∫◄--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VDD3	C18	Connect to Capacitor (Max 10V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 µF
HS_LDO	C19	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HD_VSS	1.0 µF
C11P – C11N	C20	Connect to Capacitor (Max 6V): C11P ---(+)----| |--- (-)-----C11N	1.0 µF
C12P – C12N	C21	Connect to Capacitor (Max 6V): C12P ---(+)----| |--- (-)-----C12N	1.0 µF
C13P – C13N	C22	Connect to Capacitor (Max 6V): C13P ---(+)----| |--- (-)-----C13N	1.0 µF
C14P – C14N	C23	Connect to Capacitor (Max 6V): C14P ---(+)----| |--- (-)-----C14N	1.0 µF
C15P – C15N	C24	Connect to Capacitor (Max 6V): C15P ---(+)----| |--- (-)-----C15N	1.0 µF
C16P – C16N	C25	Connect to Capacitor (Max 6V): C16P ---(+)----| |--- (-)-----C16N	1.0 µF
C17P – C17N	C26	Connect to Capacitor (Max 6V): C17P ---(+)----| |--- (-)-----C17N	1.0 µF
C18P – C18N	C27	Connect to Capacitor (Max 6V): C18P ---(+)----| |--- (-)-----C18N	1.0 µF
C31P – C31N	C28	Connect to Capacitor (Max 10V): C23P ---(+)----| |--- (-)-----C23N	1.0 µF
C32P – C32N	C29	Connect to Capacitor (Max 10V): C24P ---(+)----| |--- (-)-----C24N	1.0 µF
VGH_R	C30	Connect to Capacitor (Max 25V): VGH_R ---(+)----| |--- (-)----- VSSA	1.0 µF

HX5186-A mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGH	C2	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
VGL	C3	Connect to Capacitor (Max 16V): VGL ---(+)----| |--- (-)----- VSSA	1.0 µF
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VCL	C4	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	1.0 µF
C21P – C21N	C5	Connect to Capacitor (Max 16V): C21P ---(+)----| |--- (-)-----C21N	1.0 µF
C22P – C22N	C6	Connect to Capacitor (Max 16V): C22P ---(+)----| |--- (-)-----C22N	1.0 µF
C41P – C41N	C9	Connect to Capacitor (Max 6V): C41P ---(+)----| |--- (-)-----C41N	1.0 µF
C42P – C42N	C10	Connect to Capacitor (Max 6V): C42P ---(+)----| |--- (-)-----C42N	1.0 µF
VSPR	C11	Connect to Capacitor (Max 10V): VSPR ---(+)----| |--- (-)-----VSSA	1.0 µF
VSNR	C12	Connect to Capacitor (Max 10V): VSNR ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDD	C13	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDDN	C14	Connect to Capacitor (Max 6V): VDDDN ---(+)----| |--- (-)-----VSSA	1.0 µF
VREF	C15	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 µF
VSP	C16	Connect to Capacitor (Max 10V):VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VSN	C17	Connect to Capacitor (Max 10V):VSN ---(+)----| |--- (-)-----VSSA	2.2 µF
	D2	Connect to Schottky Diode(VR≥30V): VSN ---(-)----∫◄--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VDD3	C18	Connect to Capacitor (Max 10V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 µF

HS_LDO	C19	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS	1.0 μF
HX5186-A	U1	Please refer HX5186-A datasheet	-
HX5186-A	C20	Please refer HX5186-A datasheet	1.0uF
HX5186-A	C21	Please refer HX5186-A datasheet	1.0uF
HX5186-A	C22	Please refer HX5186-A datasheet	1.0uF
VGH_R	C30	Connect to Capacitor (Max 25V): VGH_R ---(+)----| |--- (-)----- VSSA	1.0 μF

Table 7.2: Adoptability of component

8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~ VSSD	V	-0.3 to +3.6	Note(1),(2)
Power Supply Voltage 2	VDD2 ~ VSSA	V	-0.3 to +5.5	Note(1),(3)
Power Supply Voltage 3	VDD3 ~ VSSA	V	-0.3 to +5.5	Note(1) (4)
Power Supply Voltage 4	HS_VCC ~ HS_VSS	V	-0.3 to +3.6	Note(1) (5)
Power Supply Voltage 5	VSP ~ VSSA	V	-0.3 to +6.6	Note(6)
Power Supply Voltage 6	VSSA ~ VSN	V	0 to -6.6	Note(7)
Power Supply Voltage 7	VGH ~ VSSA	V	-0.3 to +25	Note(8)
Power Supply Voltage 8	VSSA ~ VGL	V	0 to -16	Note(9)
Operating Temperature	Topr	°C	-40 to +85	Note(10)
Storage Temperature	Tstg	°C	-55 to +110	Note(11)

Note: (1) VDD1, VSSD must be maintained.
(2) To make sure VDD1 ≥ VSSD.
(3) To make sure VDD2≥ VSSA.
(4) To make sure VDD3≥ VSSA.
(5) To make sure HS_VCC ≥ HS_VSS.
(6) To make sure VSP ≥ VSSA.
(7) To make sure VSSA ≥ VSN
(8) To make sure VGH ≥ VSSA.
(9) To make sure VSSA ≥ VGL
VGH +|VGL| < 30V
(10) For die and wafer products, specified up to +85℃.
(11) This temperature specifications apply to the TCP package.

Table 8.1: Absolute maximum rating

8.2 DC characteristics

(VDD2=2.5 ~ 4.8V, VDD3=2.5 ~ 4.8V, VDD1=1.65~3.3V, T_A=-40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VDD1= 1.65 ~ 3.3V VDD2= 2.5 ~ 3.3V VDD3= 2.5 ~ 3.3V	0.7 V_{DD1}	-	VDD1	V
Input low voltage	V_{IL}	V		0	-	0.3 V_{DD1}	V
VPP	V_{IH}	V	VPP	7.25V	7.5V	7.75V	V
	V_{IL}	V					
Output high voltage (SDO, CABC_PWM_OUT)	V_{OH1}	V	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V_{OL1}	V	VDD1= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V
Logic High level input current	I_{IH}	uA	VSYNC, HSYNC	-	-	1	uA
			RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	uA
	I_{IHD}	uA	DB[23…0], SDI, DCX	-	-	1	uA
			DB[23…0]	-	-	1	uA
Logic Low level input current	I_{IL}	uA	VSYNC, HSYNC	-1	-		uA
			RESX, DCX, CSX, RDX, WRX_SCL	-1	-		uA
	I_{ILD}	uA	DB[23…0], SDI, DCX	-1	-		uA
			DB[23…0]	-1	-		uA
Current consumption standby mode (VDD2/VDD3-VSSD)	$I_{ST(VDD)}$	µA	VDD2/VDD3=2.8V, VDD1=1.8V T_A =25°C	-	-	**100**	uA
Current consumption standby mode (VDD1– VSSD)	$I_{ST(VDD1)}$	µA		-	-	**3**	uA
Current consumption during Deep-standby mode (VDD2/VDD3-VSSD)	$I_{DP-ST(VDD)}$	µA	VDD2/VDD3=2.8V, VDD1=1.8V T_A =25°C	-	-	50	uA
Current consumption during Deep-standby mode (VDD1– VSSD)	$I_{DP-ST(VDD1)}$	µA		-	-	3	uA

Note: 1. The VPP pin is open on normal mode and in used while OTP programming condition.
2. The GRAM data is eliminated under the Deep standby mode.

Table 8.2: DC characteristic

8.3 AC characteristics

8.3.1 Reset input timing

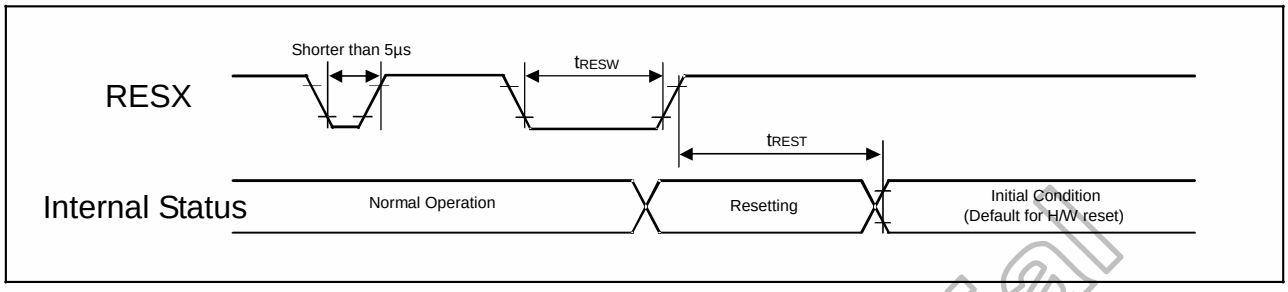


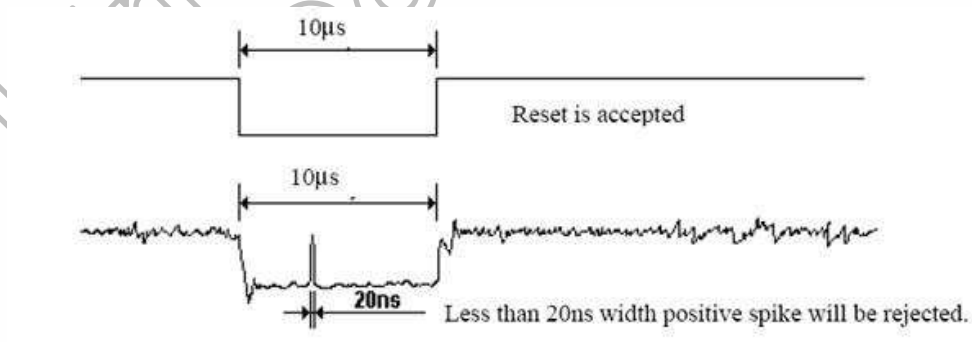
Figure 8.1: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.3: Reset timing

8.3.2 DSI D-PHY electrical characteristics

8.3.2.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.2 shows the complete set of electrical functions required for a fully featured PHY transceiver.

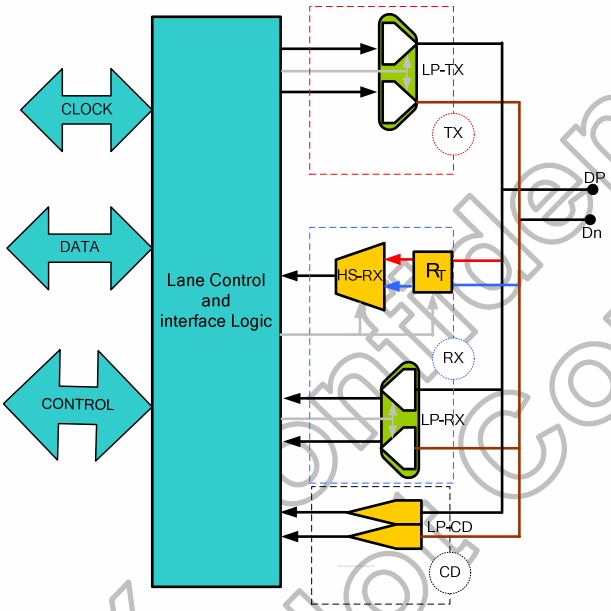


Figure 8.2: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.8 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

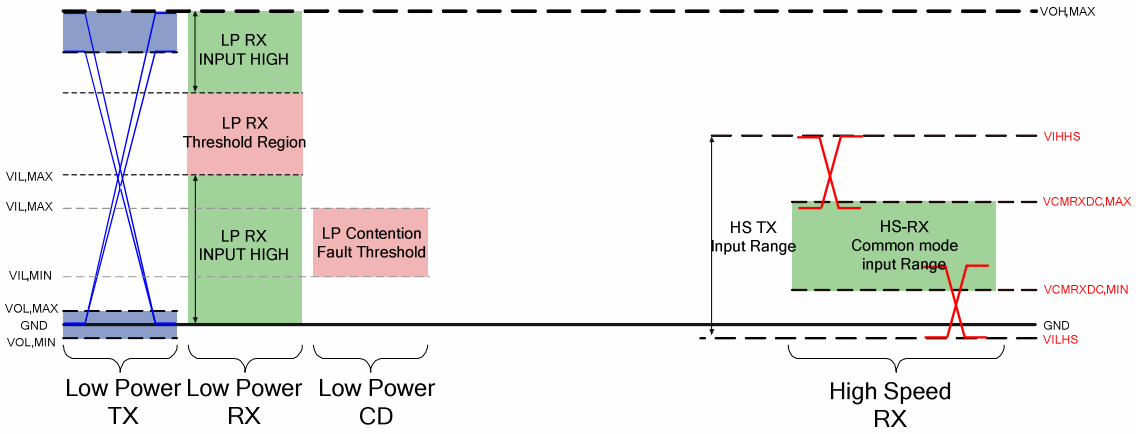


Figure 8.3: Shows both the HS and LP signal levels

8.3.2.2 The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.4: LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
T_{LPX}	Transmitted length of any Low –Power state period	83			ns	TX_OSC=1
		41.5			ns	TX_OSC=0
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Table 8.5: LP Transmitter AC Specifications

8.3.2.3 The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.3.2.4 High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.6: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.7: HS Receiver AC Specifications

8.3.2.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.4 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

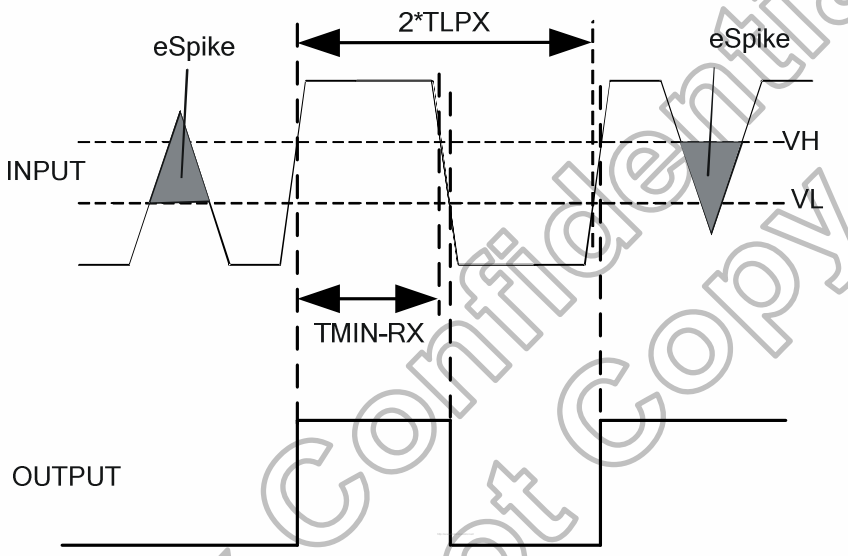


Figure 8.4: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.8: LP Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 8.9: LP Receiver AC Specifications

8.3.2.6 Line Contention Detection

Contention can be inferred from any of the following conditions:

A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than VIL.
B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VILF.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.10: Contention Detector DC Specifications

8.3.2.7 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.5.

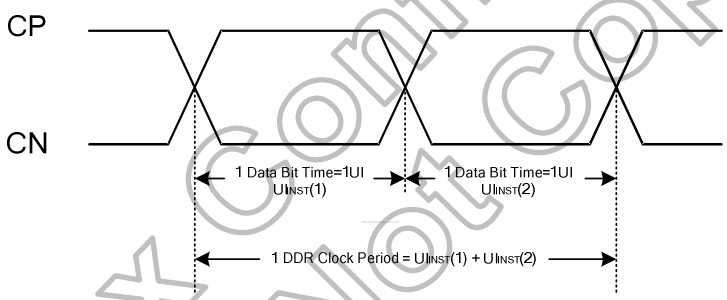


Figure 8.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.11.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850Mbps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 8.11: Re verse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.6. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

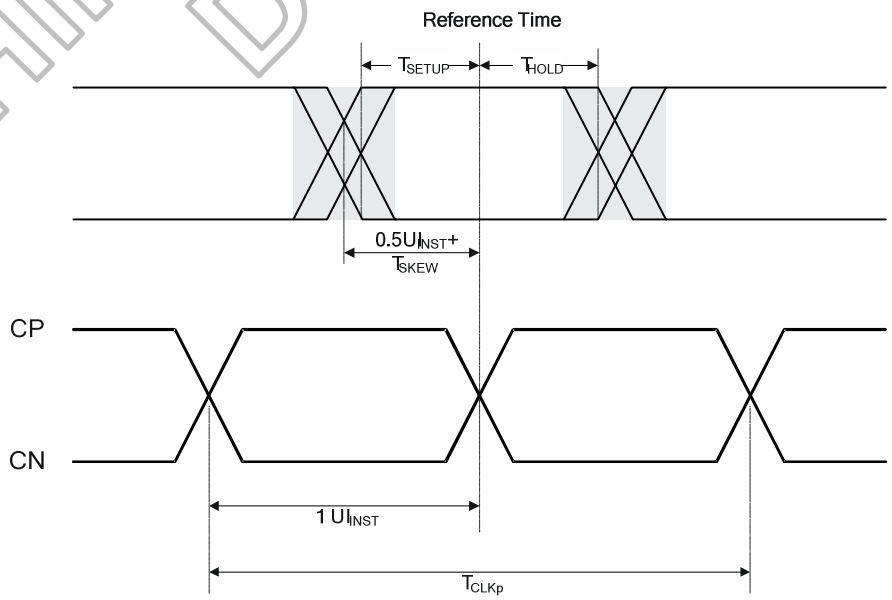


Figure 8.6: Data to Clock Timing Definitions

8.3.2.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.6. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.12 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UIINST, i.e. ±0.2*UIINST for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1,2
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1,2

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.
(2) The Vdiff is 150mV.

Table 8.12: Data to Clock Timing Specifications

8.3.3 Timings for DSI Video mode

8.3.3.1 Vertical Timings

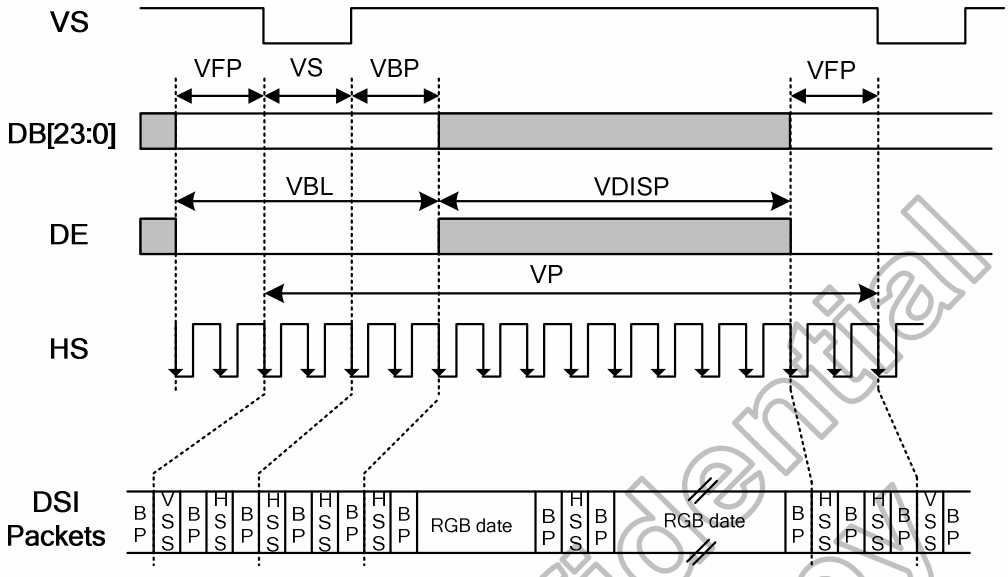


Figure 8.7: Vertical Timings for DSI Video mode I/F

Resolution=800x1280(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display. Also refer to setion 6.2.78 SETRGBCYC.

Resolution=768x1280 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display. Also refer to setion 6.2.78 SETRGBCYC.

Resolution=720x1280 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display. Also refer to setion 6.2.78 SETRGBCYC.

Resolution=600x1024 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1030	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1024	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display. Also refer to setion 6.2.78 SETRGBCYC.

Table 8.13: Vertical Timings for DSI Video mode I/F

8.3.3.2 Horizontal Timings

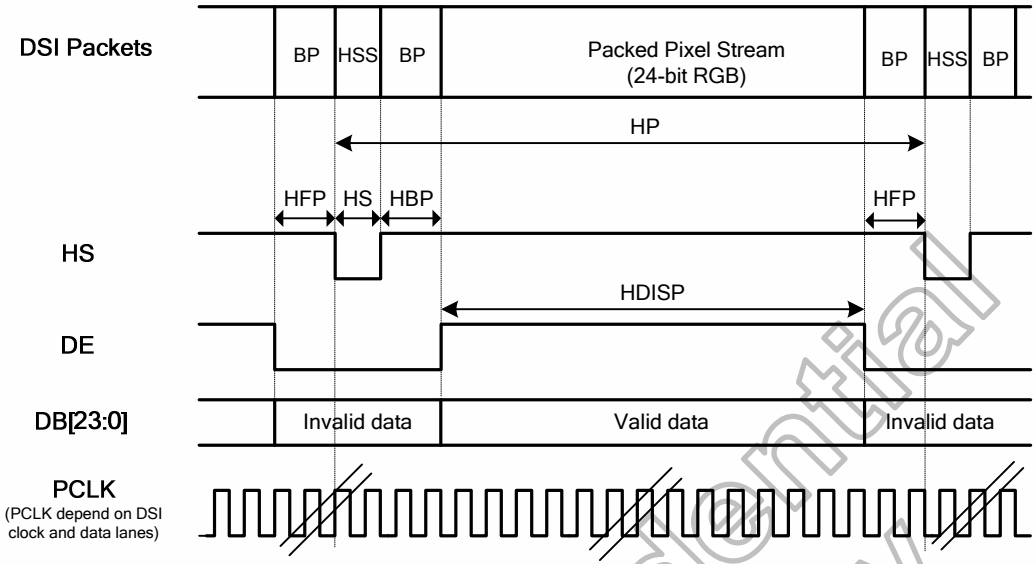


Figure 8.8: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=HS_VCC=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	5	-	-	DCK
Horizontal back porch	HBP	-	5	-	-	DCK
Horizontal front porch	HFP	-	5	-	-	DCK
Horizontal data start point	-	HS+HBP	2	-	-	us
Horizontal active area	HDISP	-	-	800	-	DCK

Resolution=768x1280 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	5	-	-	DCK
Horizontal back porch	HBP	-	5	-	-	DCK
Horizontal front porch	HFP	-	5	-	-	DCK
Horizontal data start point	-	HS+HBP	2	-	-	us
Horizontal active area	HDISP	-	-	768	-	DCK

Resolution=720x1280 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	5	-	-	DCK
Horizontal back porch	HBP	-	5	-	-	DCK
Horizontal front porch	HFP	-	5	-	-	DCK
Horizontal data start point	-	HS+HBP	2	-	-	us
Horizontal active area	HDISP	-	-	720	-	DCK

Resolution=600x1024 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	5	-	-	DCK
Horizontal back porch	HBP	-	5	-	-	DCK
Horizontal front porch	HFP	-	5	-	-	DCK
Horizontal data start point	-	HS+HBP	2	-	-	us
Horizontal active area	HDISP	-	-	600	-	DCK

Table 8.14: Horizontal Timings for DSI Video mode I/F

9. Ordering Information

Part No.	Package
HX8392-A000 PDxxx	PD: mean COG xxx: mean chip thickness (μm), (default: 250 μm)

10. Revision History

Version	Date	Description of Changes
01	2011/05/12	1. Remove “temporary” word and upgrade to Version 01. (All pages) 2. Update VDD2, VDD3, VSSD pin number.(P.15) 3. Change PAD name from VDD2 to VSSD.(P.17, P.18, P.255, P256) 4. Change PAD name from VSNC to VDD2.(P.17, P.18, P.255, P25). 5. Update Note description of Figure 5.33 Panel driving timing (P.107) 6. Update Register Default value.(P.135~P.139) 7. Update register description of STB, VSP_EN, VSN_EN, VGH_EN, VGL_EN, VCL_EN. (P.205~P.206) 8. Update register description of GON, DTE, D[1:0] (P.205~P.206) 9. Update register description of BTP[4:0] and BTN[4:0].(P.207~P.208) 10.Add TX_OSC bit in BAh command.(P.136, P.229) 11.Update description of C2h command (P.231) 12.Add D4 command.(P.136, P.240) 13.Update 7.1 Layout Recommendation.(P.255, P256) 14.Update Table 8.14 Hrizontal Timings for DSI Video mode I/F.(P.273, P.274)
	2011/06/14	1. Update 3.4.1 Bump arrangement.(P.24) 2. Update Figure 5.25: OSC aritecture(P.61) 3. Add note for PWM_CLK.(P.234) 4. Add E3h command of color enhancement function. (P.139, P.253) 5. Add F7h command of get DB[7:0] pin status. (P.139, P.256)
	2011/09/28	1. Add note for Gamma voltage.(P.69) 2. Update BP/ FP/ BP_PE/ FP_PE setting.(P.214) 3. Update TX_OSC setting.(P.229) 4. Remove 1 pcs HX5186-A for external charge pump circuit.(P.258, P261) 5. Update Table 8.2: DC characteristic.(P.263) 6. Add TLPX timing characteristic.(P.266) 7. Add note for Data to Clock Timing Specifications (P.272)
	2011/10/07	1. Add SETMIPI in OTP table.(P.117) 2. Add OTP programming delay time of block program.(P.126) 3. Update B2h and D8h default value.(P.134, P.136) 4. Add TX_DELAY[1:0] in BAh command.(P.135, P228) 5. Add BFh command.(P.135, P.230) 6. Update D4h default value.(P.136, P.240)

		7. Add D5h command.(P136, P.241)