DATA SHEET

(DOC No. HX8662-C-DS)

HX8662-C

480CH TFT LCD Gate Driver

Version 02 June, 2008

Himax Technologies, Inc.
http://www.himax.com.tw

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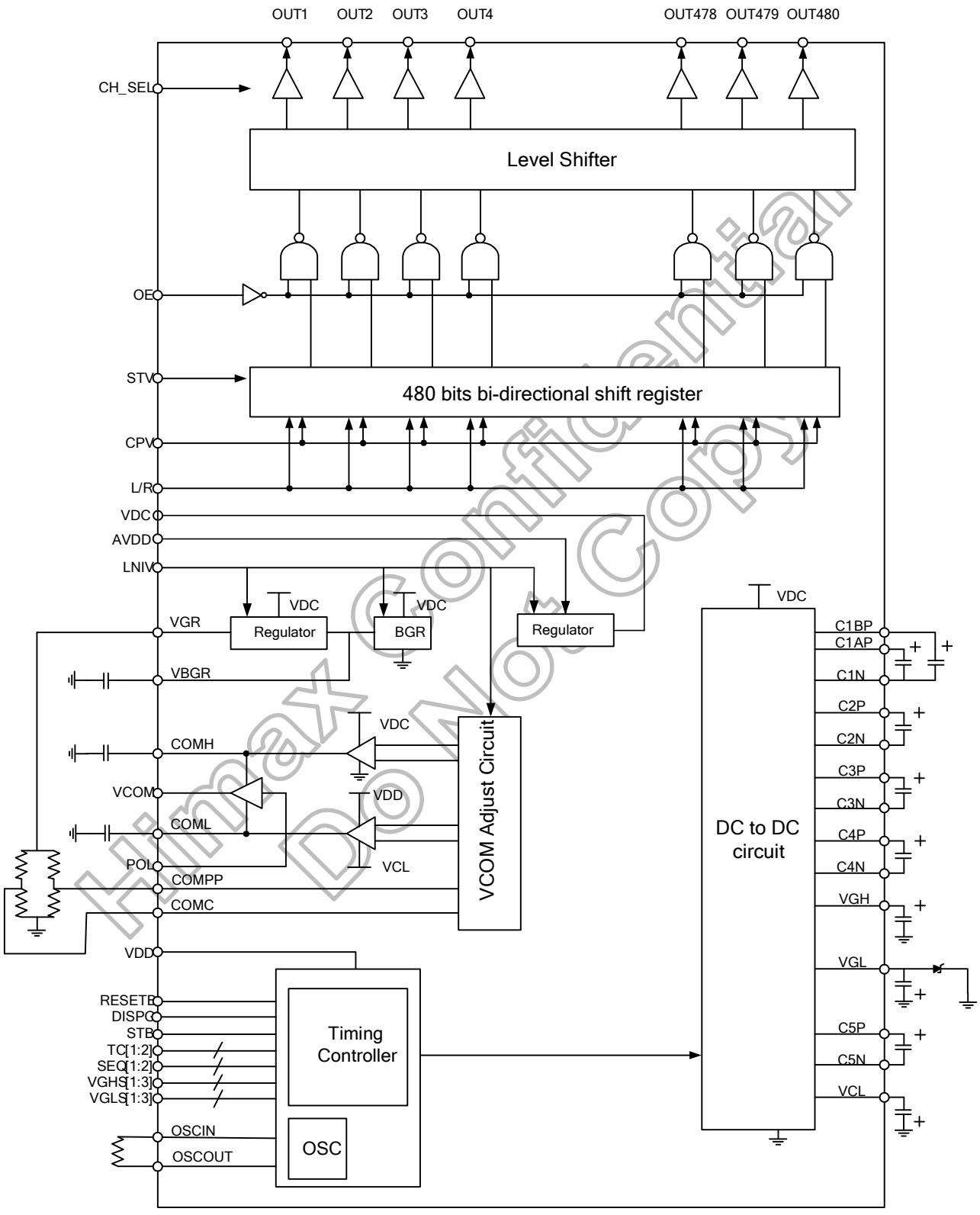
1. General Description

The HX8662-C is a TFT-LCD driver with 480-channel outputs. Each channel can output high/low voltage to turn on/off TFT switch on TFT LCD panel. It also has power supply circuit for Gate driving as well as common electrode driving.

2. Features

- CMOS level input (2.3 to 3.6V)
- 480/320 channel outputs selectable
- Support Line/Dot inversion COMMON voltage.
- DC/DC converter circuit for gate driving include (default setting VDC x [4], VDC x [-2], and adjustable)
  DC/DC converter circuit for COMMON L level regulator include (VDC x [-1])
- High-output voltage (VGH to VGL: 33V MAX)
- Including common electrode driving circuit
- Including voltage regulator for source driver gamma circuit
- COG package

3. Block Diagram



4. Pin Description

Pin name	I/O	Function	Description
CPV	In	Shift clock input	This is the clock input for chip internal shift register.
L/R	In	Shift direction control pin	The shift direction of device internal shift register is controlled by this pin as shown below: L/R=H, STV→OUT1→OUT2→ • • • →OUT480 L/R=L, STV→OUT480→OUT479→ • • • →OUT1
STV	In	Start pulse input pin	This pin is the device start pulse input pin.
OE	In	Output enable control	The OE signal controls the output enable. OE=H: All driver outputs are fixed to VGL regardless of CPV. However, the content of shift register is not cleared. OE=L: Normal operation
CH_SEL	In	Output channel select pin	Channel mode selection, default CH_SEL=L Output channel: 480 / Disable channel: - / CH_SEL: H Output channel: 320 / Disable channel: 1~80, 401~480 / CH_SEL: L
OUT1~ OUT480	Out	Driver output pins for driving gate electrode of LCD	The output is either VGH or VGL for driving the gate line of TFT LCD panel.
VGH	Out	Power supply	Power supply for Gate on output.
AVDD	In	Power supply	Analog power supply for dot inversion system.
VDC	I/O	Power supply	Analog power supply for line inversion system.
VDD	In	Power supply	Digital power supply
VSS	In	Power supply	Grounding for VDD
VGL	Out	Power supply	Power supply for Gate off output.
VCL	Out	Power supply	COMMON buffer negative power supply
VBGR	Out	Power supply	Output pin of internal reference voltage.
VGR	Out	Power supply	Output pin of internal regulator circuit.
COMH	Out	Power supply	Output pin of regulator for COMMON output H level.
COML	Out	Power supply	Output pin of regulator for COMMON output L level.
COMPP	In	Power supply	Adjust the amplitude voltage level for COMMON output
COMC	In	Power supply	Adjust the amplitude voltage level for COMMON output
C1AP, C1BP, C1N, C2P, C2N C3P, C3N, C4P, C4N, C5P, C5N	-	Capacitor for boosting connection pins	Connect 1µF capacitor between CnP and CnN pins.
VCOM	Out	Power supply	This is output pin for COMMON signal of a TFT panel.
POL	In	Power supply	This is the input pin for COMMON signal of a TFT panel.
DISPG	In	Power circuit start-up	Power circuit start-up setting pin. When DISPG is set to H, DC/DC converter circuit starts the operation set by SEQ2 and SEQ1 sequentially.
RESETB	In	Reset pin	Low reset. Initialize the IC when low. It must be reset after power-on.

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Description</th></tr>
<tr><td>STB</td><td>In</td><td>Standby mode control</td><td>This pin decides if entering standby mode.
STB = L, standby mode, timing controller, gate driver, DC/DC are off.
STB = H, normal mode.
This pin is pulled high internally.</td></tr>
<tr><td>LNIV</td><td>In</td><td>Line/Dot inversion control</td><td>For line inversion system, set this pin to “H” thus VCOM will output an AC voltage toggled between COMH and COML decided by POL polarity.
For dot inversion system, set this pin to “L” and POL pin to “H”, thus VCOM will output a DC voltage equal to COMH.</td></tr>
<tr><td>TC1
TC2</td><td>In</td><td>Operation clock control</td><td>DC/DC converter operation clock frequency control. The setting of these pins is for controlling the operation clock frequency of DC/DC converter circuit. These pins are pulled high internally.</td></tr>
<tr><td>SEQ2
SEQ1</td><td>In</td><td>Power circuit start-up control</td><td>Power circuit start-up timing control. When DISPG set to H, DC/DC converter is active after a period of time decided by SEQ1 and SEQ2. These pins are pulled high internally.</td></tr>
<tr><td>VGHS1
VGHS2
VGHS3</td><td>In</td><td>VGH output voltage control</td><td>When DC/DC is constructed as 4 x VDC for VGH, these pins can adjust VGH output voltage level as below.
<table>
<tr><th>VGHS3</th><th>VGHS2</th><th>VGHS1</th><th>VGH voltage</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>13/5 x VDC</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>14/5 x VDC</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>15/5 x VDC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>16/5 x VDC</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>17/5 x VDC</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>18/5 x VDC</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19/5 x VDC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>20/5 x VDC</td></tr>
</table>
These pins are pulled high internally.</td></tr>
<tr><td>VGLS1
VGLS2
VGLS3</td><td>In</td><td>VGL output voltage control</td><td>When DC/DC is constructed as -2 x VDC for VGL, these pins can adjust VGL output voltage level as below.
<table>
<tr><th>VGLS3</th><th>VGLS2</th><th>VGLS1</th><th>VGL voltage</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="4">-6/5 x VDC</td></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>-7/5 x VDC</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>-8/5 x VDC</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>-9/5 x VDC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>-10/5 x VDC</td></tr>
</table>
These pins are pulled high internally.</td></tr>
<tr><td>TEST1
TEST2
TEST3</td><td>-</td><td>Test mode pins</td><td>TEST1=H ,TEST2=H, and TEST3=H: Normal mode
TEST1 or TEST2 or TEST3=L: TEST mode
These pins are pulled high internally.</td></tr>
<tr><td>OSCIN
OSCOUT</td><td>I/O</td><td>Oscillation pins</td><td>Connect 75K ohm resister between OSCIN and OSCOUT pins.</td></tr>
<tr><td>PASS</td><td>-</td><td>-</td><td>Linked together internal.</td></tr>
<tr><td>DUMMY</td><td>-</td><td>DUMMY</td><td>No DUMMY pins are connected with other pins inside IC.</td></tr>
</table>

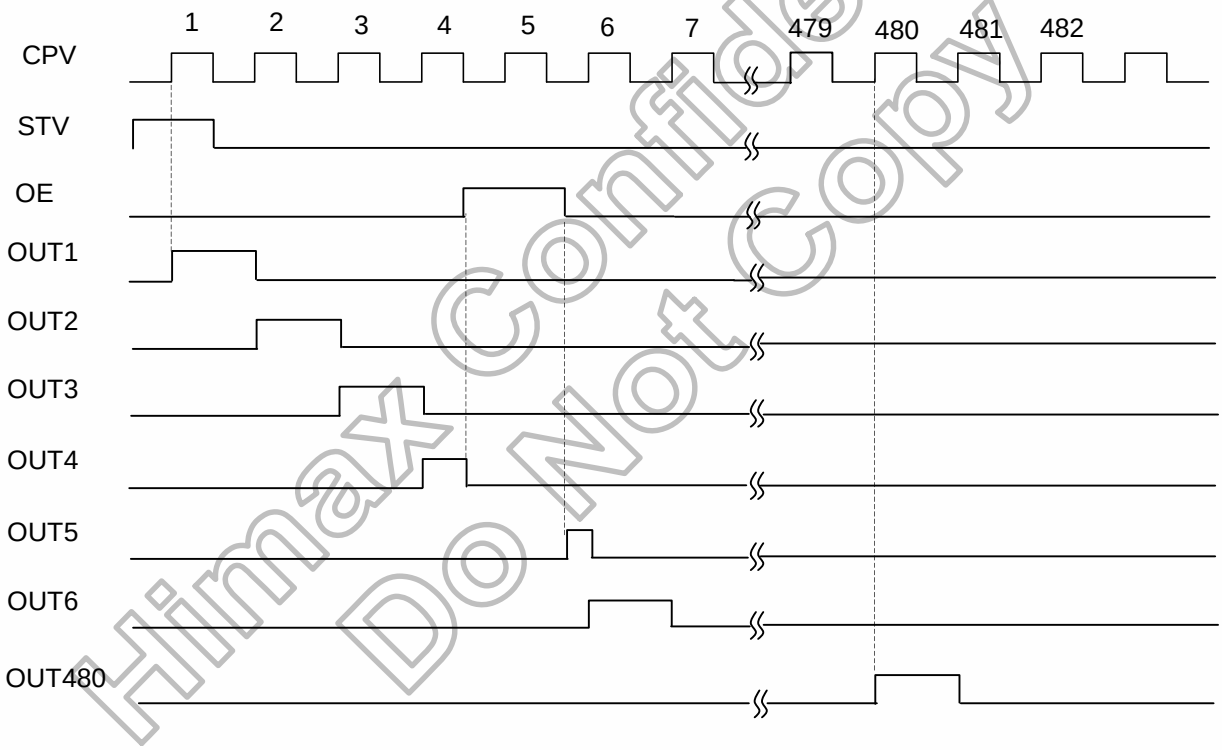
5. Function Description

5.1 Device operation

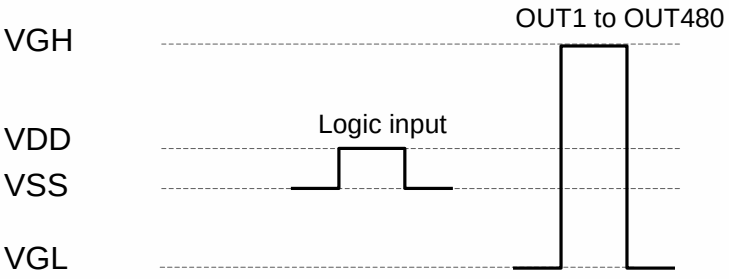
When L/R=H, the STV start pulse input is sensed on the rising edge of CPV and stored in the first stage of shift register, which makes the first scan signal output from the OUT1 pin. While stored data is transferred to the next stage shift register on the rising edge of next CPV, new data of STV is sensed and stored simultaneously.

The output pin (OUT1 to OUT480) supplies VGH voltage or VGL voltage to the LCD panel depending on the data stored in the shift register. For normal operation, a VGH voltage is outputted one by one from OUT1 to OUT480 in sync with CPV pulse.

When OE=H, the corresponding output channels are fixed to VSS regardless of CPV. The channel output returns to normal status as soon as OE goes back to L.



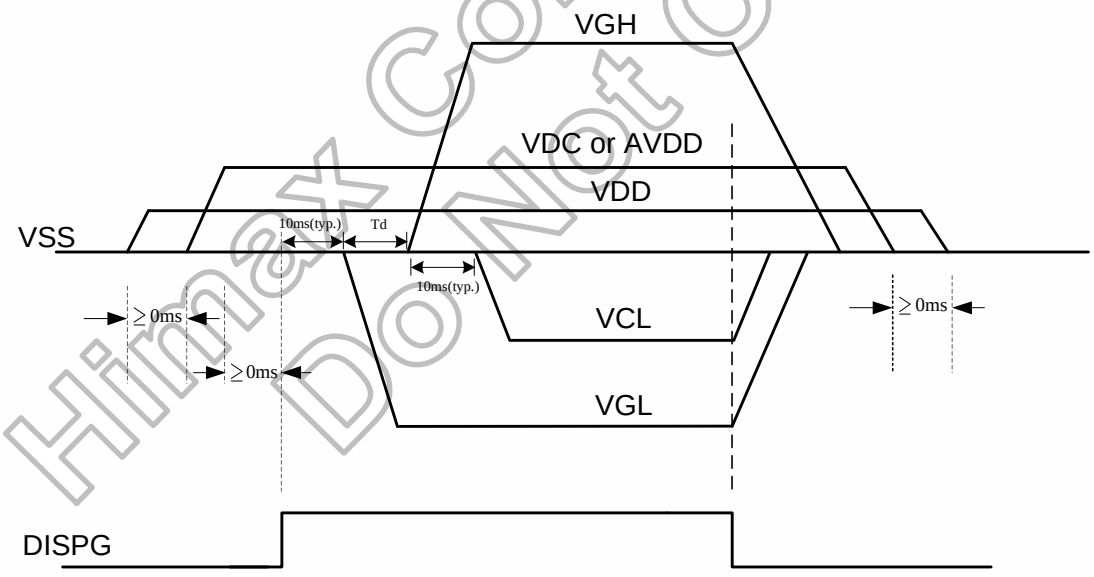
5.2 Device power supply



The input signal level of CPV, L/R, OE, CH_SEL and STV have to swing between VDD and VSS.

5.3 Power on/off sequence

To prevent the device from damage due to latch up, the power on/off sequence is shown below. The sequence of VGL, VGH and VCL is controlled by HX8662-C itself. The delay period between DISPG and VGL is decided by SEQ1 and SEQ2. The delay between VGH and VGL is decided by TC[2:1] setting and charge pump frequency. The value is shown in the table.



Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Time delay between VGH and VGL	Td	2	10	30	ms

5.4 Timing controller circuit

Timing controller circuit controls the operation frequency of DC-to-DC circuit.

TC2	TC1	Operation frequency
0	0	12.5KHz
0	1	100KHz
1	0	50KHz
1	1	25KHz (default)

5.5 Power circuit set-up sequencer

Power circuit set-up sequencer controls the start-up timing of DC-to-DC circuit.

SEQ2	SEQ1	Start-up time after DISPG=H
0	0	After 1/12Hz (83ms)
0	1	After 1/24Hz (42ms)
1	0	After 1/48Hz (21ms)
1	1	After 1/97Hz (10ms) (default)

5.6 Oscillator

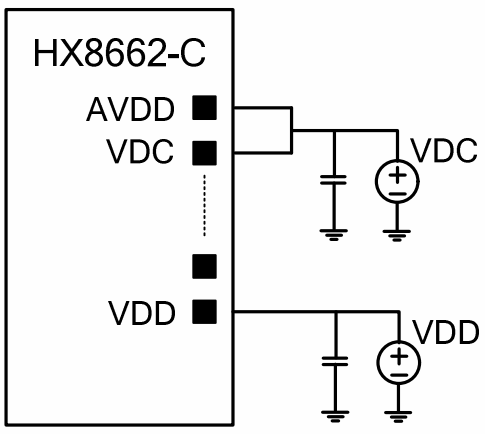
HX8662-C has an oscillator circuit inside the IC. A 75K ohm resistor must be connected between OSCIN and OSCOUT. The oscillator frequency is used as the base clock of power circuit.

5.7 Power supply for Line inversion and Dot inversion

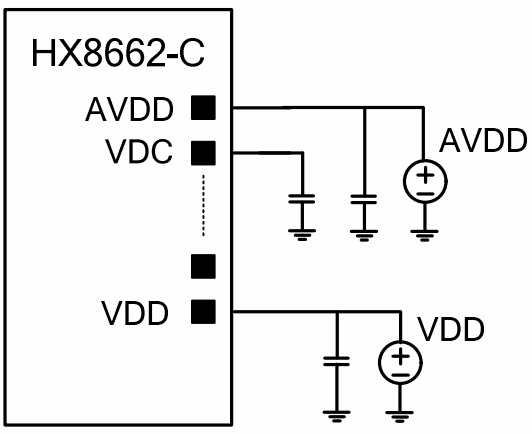
For Line inversion system, apply VDD and VDC as digital and analog power. AVDD pads should be connected to VDC power.

For Dot inversion system, apply VDD and AVDD power. The embedded regulator in HX8662-C will output a DC signal as internal analog power. The typical VDC voltage level is 6V.

[For Line inversion]



[For Dot inversion]



5.8 Common output circuit

HX8662-C has a common output circuit for TFT panel which provides AC VCOM voltage for line-inversion system or DC VCOM voltage for dot-inversion system.

For line-inversion system, POL is input to decide the polarity of common voltage, and common output circuit will provide a toggled signal with COMH and COML voltages to TFT panel.
COMH and COML voltage level are adjusted by input voltage COMPP and COMC. Relationship between COMH, COML, COMPP and COMC are shown as below:

COMH = COMC + COMPP
COML = COMC - COMPP
COMH = 4.3V ~ 2V
COML = -3.5V ~ -0.3V
COMPP, COMC = 0.1~(VDC-1V)

For dot-inversion system, set POL to “H” and COMPP to “VSS”. Common output circuit will provide a DC signal with COMH voltage to TFT panel.

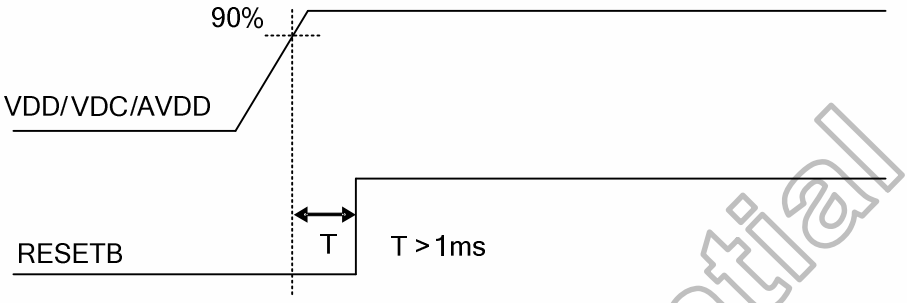
COMH = 2*COMC
COMH = 2V ~ 5.5V

5.9 Regulator for gamma circuit of source driver

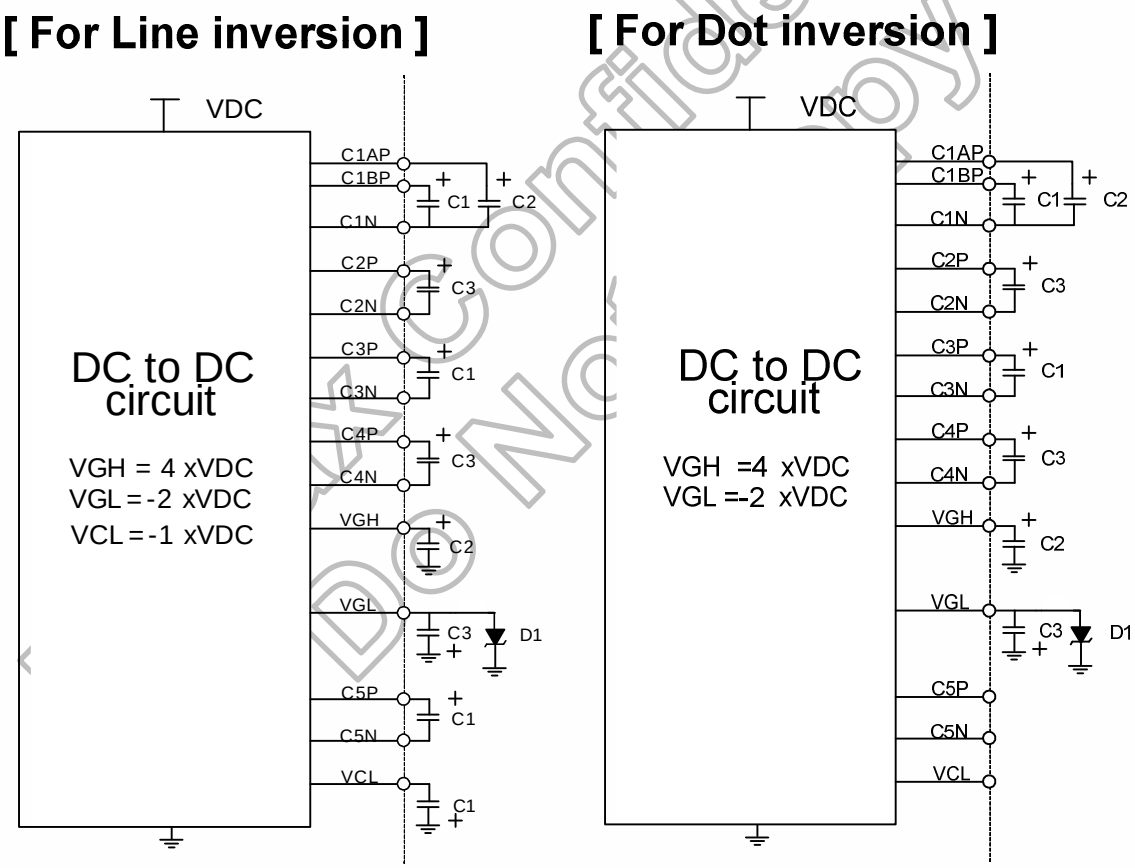
HX8662-C has regulator circuit for gamma circuit of source driver resistor strings. The output of this circuit must be connected to VGR pin of source driver. Typical VGR voltage level is 4.5V.

5.10 Reset

HX8662-C is reset internally by RESETB input. The RESETB must be held for at least 1ms after VDD, VDC and AVDD are stable.



5.11 DC/ DC external component

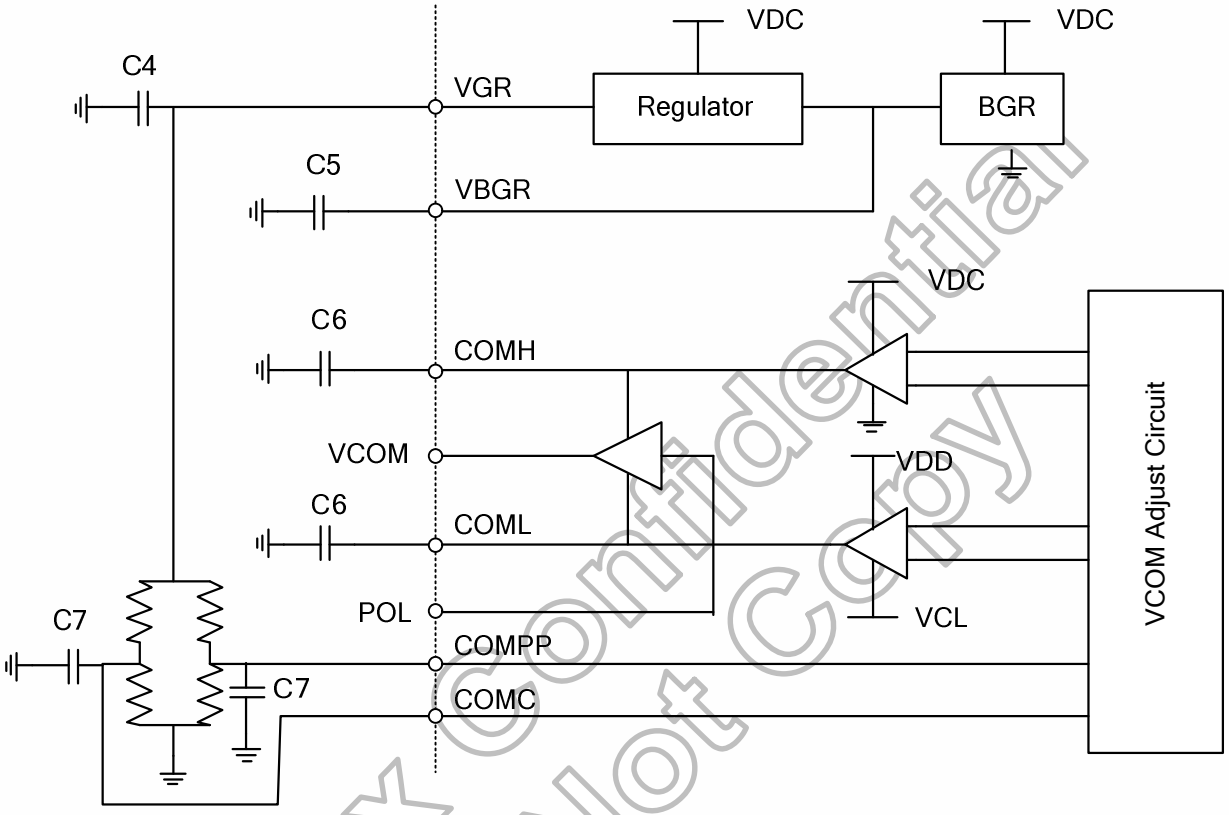


	Value	Accuracy	Voltage proof
C1	1.0μF	+/- 10%	10V
C2	1.0μF	+/- 10%	25V
C3	1.0μF	+/- 10%	16V

		Voltage proof	Characteristics
D1	Schottky_Barrier Diode	>25V	IF>200mA

5.12 Regulator for gamma circuit of source driver

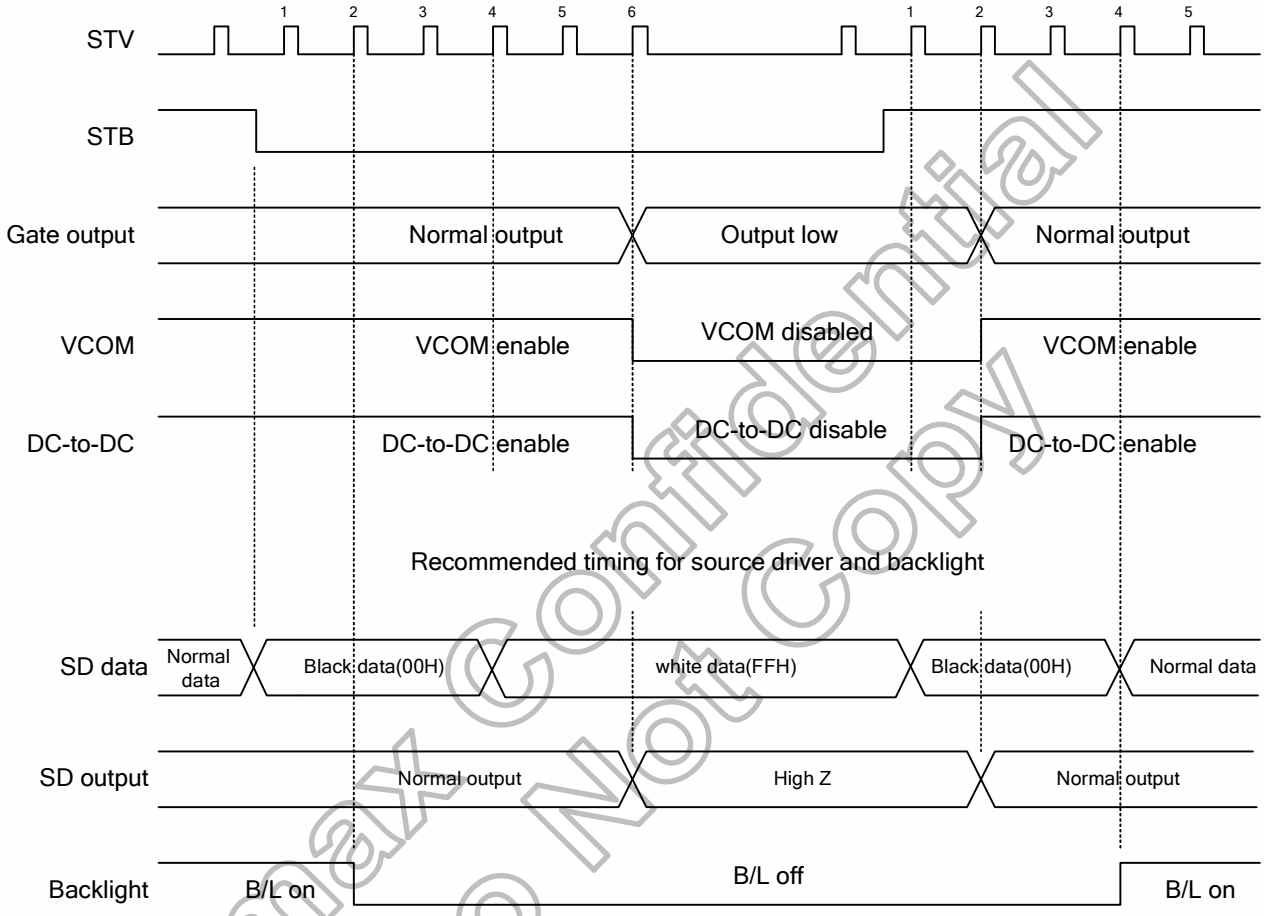
HX8662-C has a regulator circuit for source driver's gamma resistor strings. Connect this output to source driver VGR pin. VGR voltage level is 4.5V. (Typ.)



	Value	Accuracy	Voltage proof
C4	1.0μF	±10%	10V
C5	0.1μF	±10%	6.3V
C6	2.2μF ~10μF	±10%	10V
C7	0.01μF ~0.1μF	±10%	10V

5.13 Standby mode

When STB set to “L”, after 6 STV pulses past, gate driver, VCOM and DC/DC will be off. When STB returns to “H”, after 2 STV pulses past, gate driver, VCOM and DC/DC will operate normally.



5.14 Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance value(Ω)
VDD	< 30
VDC	< 5
AVDD	< 5
VSS	< 5
VGH	< 20
VGL	< 10
VCL	< 10
VBGR	< 30
VGR	< 20
COMH	< 10
COML	< 10
COMOUT	< 10
C1AP	< 20
C1BP	< 20
C1N	< 20
C2P	< 20
C2N	< 20
C3P	< 20
C3N	< 20
C4P	< 20
C4N	< 20
C5P	< 10
C5N	< 10
OSCIN	< 800(1)
OSCOUT	< 800(1)
POL	< 800
CPV	< 800
STV	< 800
OE	< 800
L/R	< 1000
SEQ1, 2	< 1000
TC1, 2	< 1000
VGHS1, 2, 3	< 1000
VGHL1, 2, 3	< 1000
COMPP	< 1000
COMC	< 1000
DISPG	< 1000
RESETB	< 1000
STB	< 1000

Note:(1) The total resistance of (OSCIN wiring resistance + OSCOUT wiring resistance + external resistance between OSCIN and OSCOUT) will decide the OSC frequency.

6. DC Characteristics

6.1 Absolute Maximum Rating (VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.3	-	+7.0	V
Power supply voltage 2	VDC	-0.3	-	+7.0	V
Power supply voltage 3	AVDD	-0.3	-	+20	V
Power supply voltage 4	VGH-VGL	-0.3	-	+42.0	V
Input voltage	V_{IN}	-0.5	-	VDD+0.5	V
Operation temperature	T_{OPR}	-30	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6.2 Recommended Operating Conditions (VSS=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	2.3	2.5	3.6	V
Power supply voltage 2	VDC	4.75	5.0	5.5	V
Power supply voltage 3	AVDD	8	10	15	V
Power supply voltage 4	VGH-VGL	28.5	30.0	33.0	V
Input Voltage	V_{IN}	0	-	VDD	V
Operation frequency	F_{CPV}		-	200	KHz
Operation temperature	Ta	-30	-	+80	℃

6.3 DC Electrical Characteristics (VSS=0V)

(VDD=2.25V to 3.6V, VDC=5V or AVDD=10V, VSS=0V, VGH=4*VDC, VGL=-2*VDC, VCL=-1*VDC)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input H voltage	V_{IH}	CKV, STV, R/L, OE	0.8VDD	-	VDD	V
Input L voltage	V_{IL}		VSS	-	0.2VDD	
Output H voltage	V_{OH}	I_{OH}=200μA	VDD-0.3	-	VDD	
Output L voltage	V_{OL}	I_{OL}=200μA	VSS	-	VSS+0.3	
Output H resistance	R_{OH}	V_{OUT} = VGH-1.0V	-	-	1000	Ω
Output L resistance	R_{OL}	V_{OUT} = VGL+1.0V	-	-	1000	Ω
Pull high resistance	R_{PU}	TC1, 2 SEQ1,2 TEST1, 2, 3 VGHS1, 2, 3 VGLS1, 2, 3 STB, CH_SEL	150	-	-	kΩ
VGR output current	I_{VGR}	-	-	-	2	mA
Regulator output voltage	VGR	No load	4.4	4.5	4.6	V
VGH voltage	VGH	External C=1μF	-	4VDC	-	V
VGL voltage	VGL	External C=1μF	-	-2VDC	-	V
VCL voltage(1)	VCL	External C=4.7μF	-	-VDC	-	V
VCOMH output voltage	VCOMH1	No load. LNIV=VDD, COMC=0.65V, COMPP=3.65V	4.2	4.3	4.4	V
VCOML output voltage	VCOML1	No load. LNIV=VDD, COMC=0.65V, COMPP=3.65V	-3.1	-3.0	-2.9	V
VCOMH output voltage	VCOMH2	No load. LNIV=VSS, COMC=2.75V, COMPP=VSS	5.4	5.5	5.6	V
Input leakage current	I_{IN}	V_I=0V or 3.6V	-1.0	-	+1.0	μA
VDD Power consumption(2)	I_{VDD1}	No load, LNIV=VDD, VDD=2.5V, VDC=5.0V, F_{CPV}=20KHz, OE =V_{IL}	-	150	200	μA
VDC Power consumption(2)	I_{VDC1}		-	1800	2500	
VDD Power consumption(3)	I_{VDD2}	No load, LNIV=VSS, VDD=2.5V, AVDD=10.0V, F_{CPV}=20KHz, OE =V_{IL}	-	150	200	μA
AVDD Power consumption(3)	I_{AVDD1}		-	2000	2500	
Digital standby current	I_{VDD3}	STB="L", all function shut down	-	-	100	μA
Analog standby current	I_{VDC3}		-	-	200	

Note: (1) VCL voltage will be disabled for Dot inversion setting.

(2) Power consumption with the following condition:
Output no load, VGH =20V, VGL = -10V, VDD =2.5V, VDC =5.0V, V_{IH}=VDD, V_{IL}=VSS, F_{CPV}=20KHz, OE =V_{IL},

(3)Power consumption with the following condition:
Output no load, VGH =20V, VGL = -10V, VDD =2.5V, AVDD =10.0V, V_{IH}=VDD, V_{IL}=VSS, F_{CPV}=20KHz, OE =V_{IL},

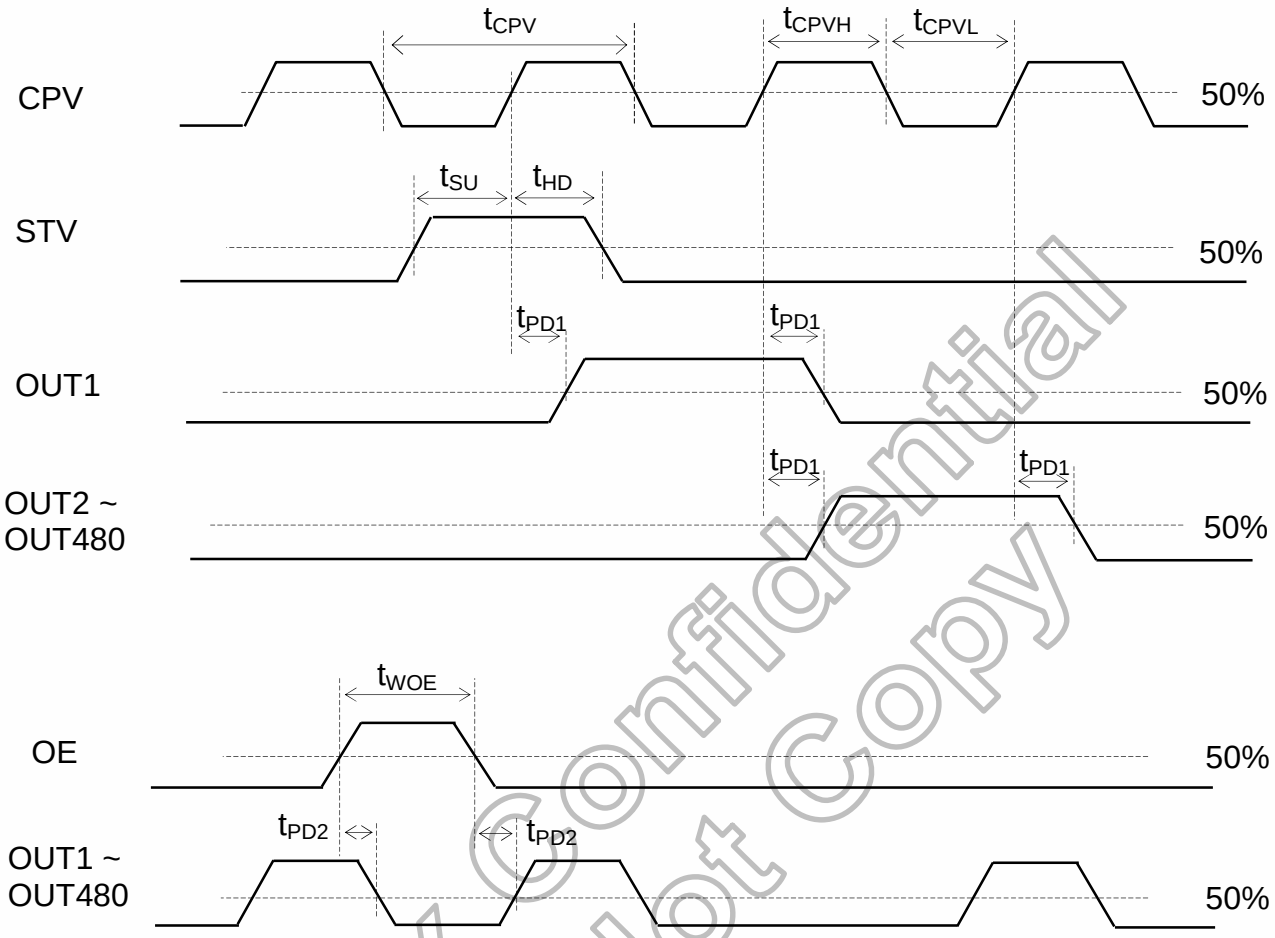
7. AC Characteristics

(VDD=2.25V to 3.6V, VDC=5V or AVDD=10V, VSS=0V, VGH=4*VDC, VGL=-2*VDC, VCL=-1*VDC)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Oscillation frequency	f_{OSC}		130	200	270	KHz
VCOM output rise time(1)	t_{COMR}	CL=100nF			32	µs
VCOM output fall time(2)	t_{COMF}	CL=100nF			32	
CPV period	t_{CPV}	-	5	-	-	
CPV pulse width(3)	t_{CPVH}, t_{CPVL}	50% duty cycle	2.5	-	-	
OE pulse width	t_{WOE}	-	1	-	-	
Data setup time	t_{SU}	-	0.2	-	-	
Data hold time	t_{HD}	-	0.3	-	-	
CPV to output delay time	t_{PD1}	CL=220pF	-	-	0.9	
OE to output delay time	t_{PD2}	CL=220pF	-	-	0.8	

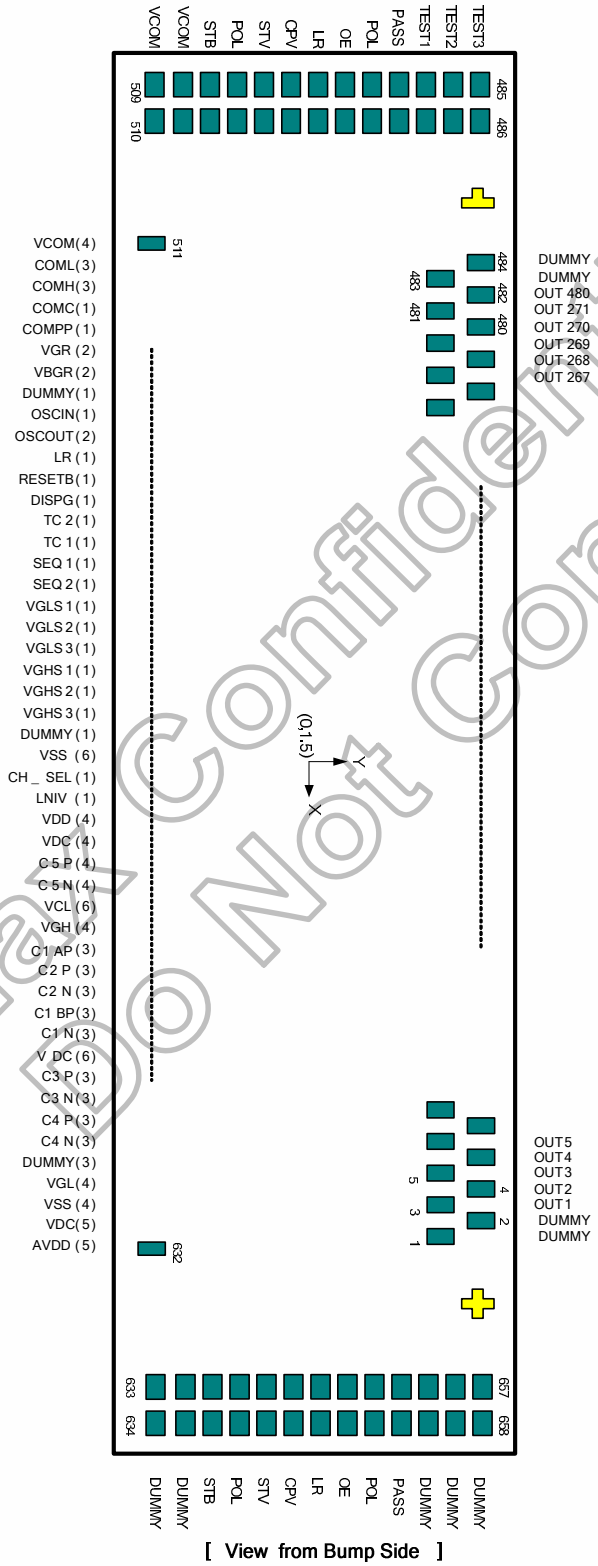
Note: (1) 10 to 90% of (COMH-COML)
(2) 90 to 10% of (COMH-COML)
(3) For non 50% duty cycle application, min. CPV pulse width t_{CPVH} =0.7µs

8. Waveform



9. Pad Coordinates

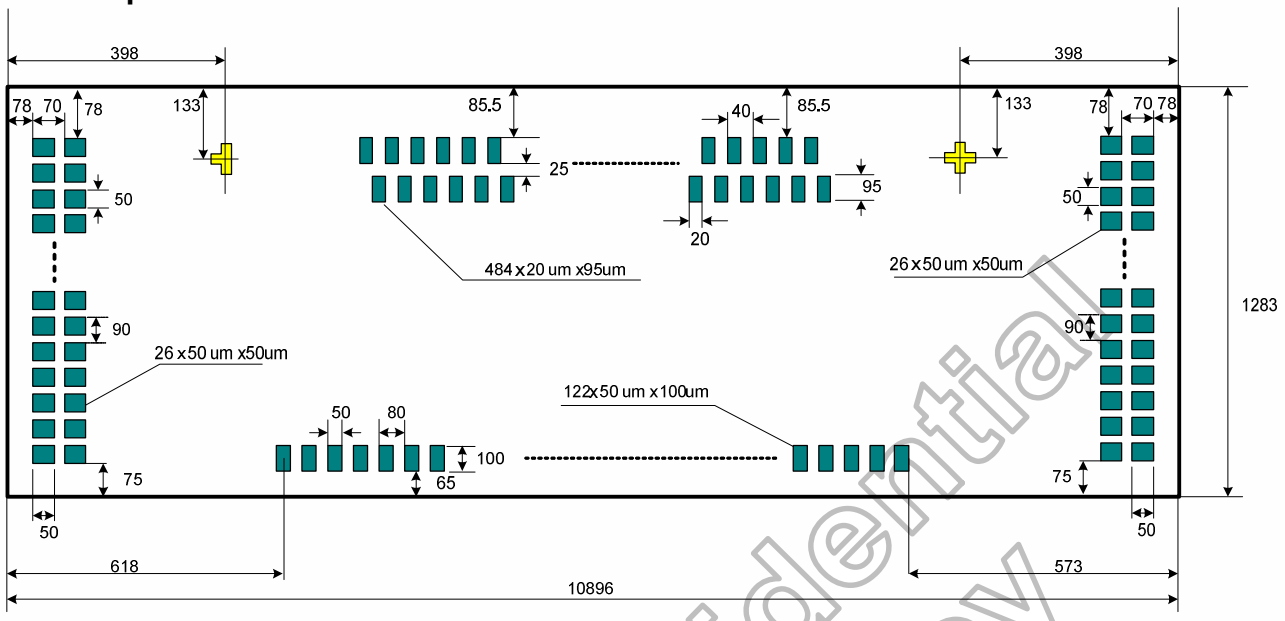
9.1 HX8662-C gate driver bump location



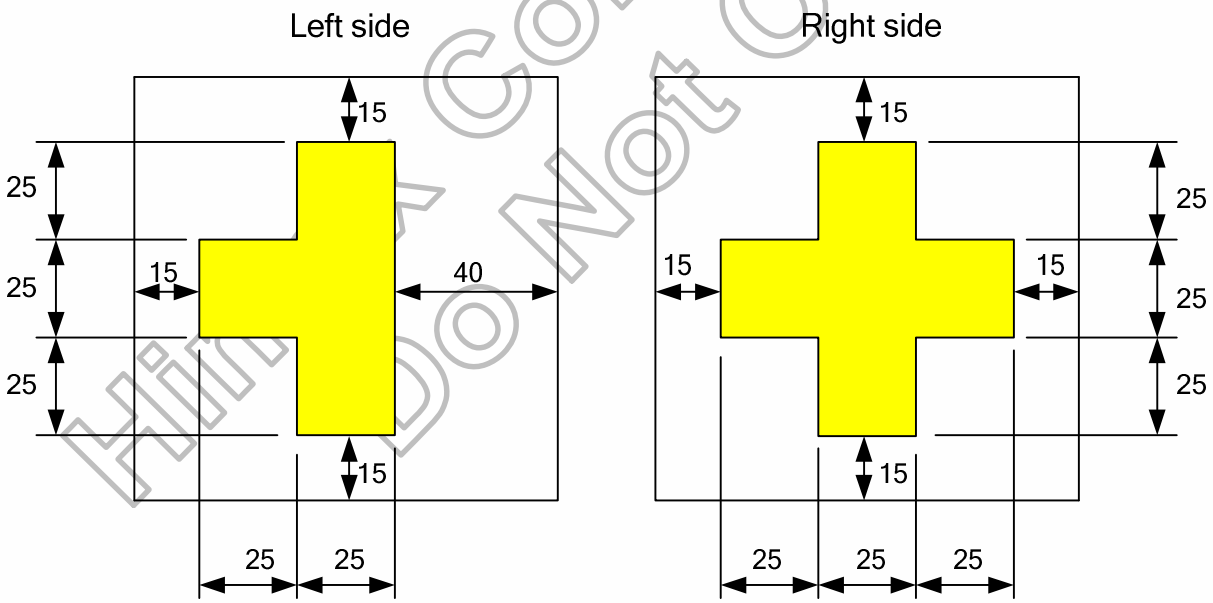
[View from Bump Side]

Chip size:10896μm x 1283μm (scribe line included)
Bump height: 15μm ± 3μm
Bump hardness: 60Hv ±15Hv
Scribe line width: 80μm

9.2 Bump outline dimensions



9.3 Alignment mark



9.4 Bump center coordinates

No.	Name	X	Y	bump size(μm)
1	DUMMY	4830	390	20*95
2	DUMMY	4810	510	20*95
3	OUT1	4790	390	20*95
4	OUT2	4770	510	20*95
5	OUT3	4750	390	20*95
6	OUT4	4730	510	20*95
7	OUT5	4710	390	20*95
8	OUT6	4690	510	20*95
9	OUT7	4670	390	20*95
10	OUT8	4650	510	20*95
11	OUT9	4630	390	20*95
12	OUT10	4610	510	20*95
13	OUT11	4590	390	20*95
14	OUT12	4570	510	20*95
15	OUT13	4550	390	20*95
16	OUT14	4530	510	20*95
17	OUT15	4510	390	20*95
18	OUT16	4490	510	20*95
19	OUT17	4470	390	20*95
20	OUT18	4450	510	20*95
21	OUT19	4430	390	20*95
22	OUT20	4410	510	20*95
23	OUT21	4390	390	20*95
24	OUT22	4370	510	20*95
25	OUT23	4350	390	20*95
26	OUT24	4330	510	20*95
27	OUT25	4310	390	20*95
28	OUT26	4290	510	20*95
29	OUT27	4270	390	20*95
30	OUT28	4250	510	20*95
31	OUT29	4230	390	20*95
32	OUT30	4210	510	20*95
33	OUT31	4190	390	20*95
34	OUT32	4170	510	20*95
35	OUT33	4150	390	20*95
36	OUT34	4130	510	20*95
37	OUT35	4110	390	20*95
38	OUT36	4090	510	20*95
39	OUT37	4070	390	20*95
40	OUT38	4050	510	20*95
41	OUT39	4030	390	20*95
42	OUT40	4010	510	20*95
43	OUT41	3990	390	20*95
44	OUT42	3970	510	20*95
45	OUT43	3950	390	20*95
46	OUT44	3930	510	20*95
47	OUT45	3910	390	20*95
48	OUT46	3890	510	20*95
49	OUT47	3870	390	20*95
50	OUT48	3850	510	20*95
51	OUT49	3830	390	20*95
52	OUT50	3810	510	20*95
53	OUT51	3790	390	20*95
54	OUT52	3770	510	20*95
55	OUT53	3750	390	20*95
56	OUT54	3730	510	20*95
57	OUT55	3710	390	20*95
58	OUT56	3690	510	20*95
59	OUT57	3670	390	20*95
60	OUT58	3650	510	20*95

No.	Name	X	Y	bump size(μm)
61	OUT59	3630	390	20*95
62	OUT60	3610	510	20*95
63	OUT61	3590	390	20*95
64	OUT62	3570	510	20*95
65	OUT63	3550	390	20*95
66	OUT64	3530	510	20*95
67	OUT65	3510	390	20*95
68	OUT66	3490	510	20*95
69	OUT67	3470	390	20*95
70	OUT68	3450	510	20*95
71	OUT69	3430	390	20*95
72	OUT70	3410	510	20*95
73	OUT71	3390	390	20*95
74	OUT72	3370	510	20*95
75	OUT73	3350	390	20*95
76	OUT74	3330	510	20*95
77	OUT75	3310	390	20*95
78	OUT76	3290	510	20*95
79	OUT77	3270	390	20*95
80	OUT78	3250	510	20*95
81	OUT79	3230	390	20*95
82	OUT80	3210	510	20*95
83	OUT81	3190	390	20*95
84	OUT82	3170	510	20*95
85	OUT83	3150	390	20*95
86	OUT84	3130	510	20*95
87	OUT85	3110	390	20*95
88	OUT86	3090	510	20*95
89	OUT87	3070	390	20*95
90	OUT88	3050	510	20*95
91	OUT89	3030	390	20*95
92	OUT90	3010	510	20*95
93	OUT91	2990	390	20*95
94	OUT92	2970	510	20*95
95	OUT93	2950	390	20*95
96	OUT94	2930	510	20*95
97	OUT95	2910	390	20*95
98	OUT96	2890	510	20*95
99	OUT97	2870	390	20*95
100	OUT98	2850	510	20*95
101	OUT99	2830	390	20*95
102	OUT100	2810	510	20*95
103	OUT101	2790	390	20*95
104	OUT102	2770	510	20*95
105	OUT103	2750	390	20*95
106	OUT104	2730	510	20*95
107	OUT105	2710	390	20*95
108	OUT106	2690	510	20*95
109	OUT107	2670	390	20*95
110	OUT108	2650	510	20*95
111	OUT109	2630	390	20*95
112	OUT110	2610	510	20*95
113	OUT111	2590	390	20*95
114	OUT112	2570	510	20*95
115	OUT113	2550	390	20*95
116	OUT114	2530	510	20*95
117	OUT115	2510	390	20*95
118	OUT116	2490	510	20*95
119	OUT117	2470	390	20*95
120	OUT118	2450	510	20*95

No.	Name	X	Y	bump size(μm)
121	OUT119	2430	390	20*95
122	OUT120	2410	510	20*95
123	OUT121	2390	390	20*95
124	OUT122	2370	510	20*95
125	OUT123	2350	390	20*95
126	OUT124	2330	510	20*95
127	OUT125	2310	390	20*95
128	OUT126	2290	510	20*95
129	OUT127	2270	390	20*95
130	OUT128	2250	510	20*95
131	OUT129	2230	390	20*95
132	OUT130	2210	510	20*95
133	OUT131	2190	390	20*95
134	OUT132	2170	510	20*95
135	OUT133	2150	390	20*95
136	OUT134	2130	510	20*95
137	OUT135	2110	390	20*95
138	OUT136	2090	510	20*95
139	OUT137	2070	390	20*95
140	OUT138	2050	510	20*95
141	OUT139	2030	390	20*95
142	OUT140	2010	510	20*95
143	OUT141	1990	390	20*95
144	OUT142	1970	510	20*95
145	OUT143	1950	390	20*95
146	OUT144	1930	510	20*95
147	OUT145	1910	390	20*95
148	OUT146	1890	510	20*95
149	OUT147	1870	390	20*95
150	OUT148	1850	510	20*95
151	OUT149	1830	390	20*95
152	OUT150	1810	510	20*95
153	OUT151	1790	390	20*95
154	OUT152	1770	510	20*95
155	OUT153	1750	390	20*95
156	OUT154	1730	510	20*95
157	OUT155	1710	390	20*95
158	OUT156	1690	510	20*95
159	OUT157	1670	390	20*95
160	OUT158	1650	510	20*95
161	OUT159	1630	390	20*95
162	OUT160	1610	510	20*95
163	OUT161	1590	390	20*95
164	OUT162	1570	510	20*95
165	OUT163	1550	390	20*95
166	OUT164	1530	510	20*95
167	OUT165	1510	390	20*95
168	OUT166	1490	510	20*95
169	OUT167	1470	390	20*95
170	OUT168	1450	510	20*95
171	OUT169	1430	390	20*95
172	OUT170	1410	510	20*95
173	OUT171	1390	390	20*95
174	OUT172	1370	510	20*95
175	OUT173	1350	390	20*95
176	OUT174	1330	510	20*95
177	OUT175	1310	390	20*95
178	OUT176	1290	510	20*95
179	OUT177	1270	390	20*95
180	OUT178	1250	510	20*95

No.	Name	X	Y	bump size(μm)
181	OUT179	1230	390	20*95
182	OUT180	1210	510	20*95
183	OUT181	1190	390	20*95
184	OUT182	1170	510	20*95
185	OUT183	1150	390	20*95
186	OUT184	1130	510	20*95
187	OUT185	1110	390	20*95
188	OUT186	1090	510	20*95
189	OUT187	1070	390	20*95
190	OUT188	1050	510	20*95
191	OUT189	1030	390	20*95
192	OUT190	1010	510	20*95
193	OUT191	990	390	20*95
194	OUT192	970	510	20*95
195	OUT193	950	390	20*95
196	OUT194	930	510	20*95
197	OUT195	910	390	20*95
198	OUT196	890	510	20*95
199	OUT197	870	390	20*95
200	OUT198	850	510	20*95
201	OUT199	830	390	20*95
202	OUT200	810	510	20*95
203	OUT201	790	390	20*95
204	OUT202	770	510	20*95
205	OUT203	750	390	20*95
206	OUT204	730	510	20*95
207	OUT205	710	390	20*95
208	OUT206	690	510	20*95
209	OUT207	670	390	20*95
210	OUT208	650	510	20*95
211	OUT209	630	390	20*95
212	OUT210	610	510	20*95
213	OUT211	590	390	20*95
214	OUT212	570	510	20*95
215	OUT213	550	390	20*95
216	OUT214	530	510	20*95
217	OUT215	510	390	20*95
218	OUT216	490	510	20*95
219	OUT217	470	390	20*95
220	OUT218	450	510	20*95
221	OUT219	430	390	20*95
222	OUT220	410	510	20*95
223	OUT221	390	390	20*95
224	OUT222	370	510	20*95
225	OUT223	350	390	20*95
226	OUT224	330	510	20*95
227	OUT225	310	390	20*95
228	OUT226	290	510	20*95
229	OUT227	270	390	20*95
230	OUT228	250	510	20*95
231	OUT229	230	390	20*95
232	OUT230	210	510	20*95
233	OUT231	190	390	20*95
234	OUT232	170	510	20*95
235	OUT233	150	390	20*95
236	OUT234	130	510	20*95
237	OUT235	110	390	20*95
238	OUT236	90	510	20*95
239	OUT237	70	390	20*95
240	OUT238	50	510	20*95

No.	Name	X	Y	bump size(μm)
241	OUT239	30	390	20*95
242	OUT240	10	510	20*95
243	OUT241	-10	390	20*95
244	OUT242	-30	510	20*95
245	OUT243	-50	390	20*95
246	OUT244	-70	510	20*95
247	OUT245	-90	390	20*95
248	OUT246	-110	510	20*95
249	OUT247	-130	390	20*95
250	OUT248	-150	510	20*95
251	OUT249	-170	390	20*95
252	OUT250	-190	510	20*95
253	OUT251	-210	390	20*95
254	OUT252	-230	510	20*95
255	OUT253	-250	390	20*95
256	OUT254	-270	510	20*95
257	OUT255	-290	390	20*95
258	OUT256	-310	510	20*95
259	OUT257	-330	390	20*95
260	OUT258	-350	510	20*95
261	OUT259	-370	390	20*95
262	OUT260	-390	510	20*95
263	OUT261	-410	390	20*95
264	OUT262	-430	510	20*95
265	OUT263	-450	390	20*95
266	OUT264	-470	510	20*95
267	OUT265	-490	390	20*95
268	OUT266	-510	510	20*95
269	OUT267	-530	390	20*95
270	OUT268	-550	510	20*95
271	OUT269	-570	390	20*95
272	OUT270	-590	510	20*95
273	OUT271	-610	390	20*95
274	OUT272	-630	510	20*95
275	OUT273	-650	390	20*95
276	OUT274	-670	510	20*95
277	OUT275	-690	390	20*95
278	OUT276	-710	510	20*95
279	OUT277	-730	390	20*95
280	OUT278	-750	510	20*95
281	OUT279	-770	390	20*95
282	OUT280	-790	510	20*95
283	OUT281	-810	390	20*95
284	OUT282	-830	510	20*95
285	OUT283	-850	390	20*95
286	OUT284	-870	510	20*95
287	OUT285	-890	390	20*95
288	OUT286	-910	510	20*95
289	OUT287	-930	390	20*95
290	OUT288	-950	510	20*95
291	OUT289	-970	390	20*95
292	OUT290	-990	510	20*95
293	OUT291	-1010	390	20*95
294	OUT292	-1030	510	20*95
295	OUT293	-1050	390	20*95
296	OUT294	-1070	510	20*95
297	OUT295	-1090	390	20*95
298	OUT296	-1110	510	20*95
299	OUT297	-1130	390	20*95
300	OUT298	-1150	510	20*95

No.	Name	X	Y	bump size(μm)
301	OUT299	-1170	390	20*95
302	OUT300	-1190	510	20*95
303	OUT301	-1210	390	20*95
304	OUT302	-1230	510	20*95
305	OUT303	-1250	390	20*95
306	OUT304	-1270	510	20*95
307	OUT305	-1290	390	20*95
308	OUT306	-1310	510	20*95
309	OUT307	-1330	390	20*95
310	OUT308	-1350	510	20*95
311	OUT309	-1370	390	20*95
312	OUT310	-1390	510	20*95
313	OUT311	-1410	390	20*95
314	OUT312	-1430	510	20*95
315	OUT313	-1450	390	20*95
316	OUT314	-1470	510	20*95
317	OUT315	-1490	390	20*95
318	OUT316	-1510	510	20*95
319	OUT317	-1530	390	20*95
320	OUT318	-1550	510	20*95
321	OUT319	-1570	390	20*95
322	OUT320	-1590	510	20*95
323	OUT321	-1610	390	20*95
324	OUT322	-1630	510	20*95
325	OUT323	-1650	390	20*95
326	OUT324	-1670	510	20*95
327	OUT325	-1690	390	20*95
328	OUT326	-1710	510	20*95
329	OUT327	-1730	390	20*95
330	OUT328	-1750	510	20*95
331	OUT329	-1770	390	20*95
332	OUT330	-1790	510	20*95
333	OUT331	-1810	390	20*95
334	OUT332	-1830	510	20*95
335	OUT333	-1850	390	20*95
336	OUT334	-1870	510	20*95
337	OUT335	-1890	390	20*95
338	OUT336	-1910	510	20*95
339	OUT337	-1930	390	20*95
340	OUT338	-1950	510	20*95
341	OUT339	-1970	390	20*95
342	OUT340	-1990	510	20*95
343	OUT341	-2010	390	20*95
344	OUT342	-2030	510	20*95
345	OUT343	-2050	390	20*95
346	OUT344	-2070	510	20*95
347	OUT345	-2090	390	20*95
348	OUT346	-2110	510	20*95
349	OUT347	-2130	390	20*95
350	OUT348	-2150	510	20*95
351	OUT349	-2170	390	20*95
352	OUT350	-2190	510	20*95
353	OUT351	-2210	390	20*95
354	OUT352	-2230	510	20*95
355	OUT353	-2250	390	20*95
356	OUT354	-2270	510	20*95
357	OUT355	-2290	390	20*95
358	OUT356	-2310	510	20*95
359	OUT357	-2330	390	20*95
360	OUT358	-2350	510	20*95

No.	Name	X	Y	bump size(μm)
361	OUT359	-2370	390	20*95
362	OUT360	-2390	510	20*95
363	OUT361	-2410	390	20*95
364	OUT362	-2430	510	20*95
365	OUT363	-2450	390	20*95
366	OUT364	-2470	510	20*95
367	OUT365	-2490	390	20*95
368	OUT366	-2510	510	20*95
369	OUT367	-2530	390	20*95
370	OUT368	-2550	510	20*95
371	OUT369	-2570	390	20*95
372	OUT370	-2590	510	20*95
373	OUT371	-2610	390	20*95
374	OUT372	-2630	510	20*95
375	OUT373	-2650	390	20*95
376	OUT374	-2670	510	20*95
377	OUT375	-2690	390	20*95
378	OUT376	-2710	510	20*95
379	OUT377	-2730	390	20*95
380	OUT378	-2750	510	20*95
381	OUT379	-2770	390	20*95
382	OUT380	-2790	510	20*95
383	OUT381	-2810	390	20*95
384	OUT382	-2830	510	20*95
385	OUT383	-2850	390	20*95
386	OUT384	-2870	510	20*95
387	OUT385	-2890	390	20*95
388	OUT386	-2910	510	20*95
389	OUT387	-2930	390	20*95
390	OUT388	-2950	510	20*95
391	OUT389	-2970	390	20*95
392	OUT390	-2990	510	20*95
393	OUT391	-3010	390	20*95
394	OUT392	-3030	510	20*95
395	OUT393	-3050	390	20*95
396	OUT394	-3070	510	20*95
397	OUT395	-3090	390	20*95
398	OUT396	-3110	510	20*95
399	OUT397	-3130	390	20*95
400	OUT398	-3150	510	20*95
401	OUT399	-3170	390	20*95
402	OUT400	-3190	510	20*95
403	OUT401	-3210	390	20*95
404	OUT402	-3230	510	20*95
405	OUT403	-3250	390	20*95
406	OUT404	-3270	510	20*95
407	OUT405	-3290	390	20*95
408	OUT406	-3310	510	20*95
409	OUT407	-3330	390	20*95
410	OUT408	-3350	510	20*95
411	OUT409	-3370	390	20*95
412	OUT410	-3390	510	20*95
413	OUT411	-3410	390	20*95
414	OUT412	-3430	510	20*95
415	OUT413	-3450	390	20*95
416	OUT414	-3470	510	20*95
417	OUT415	-3490	390	20*95
418	OUT416	-3510	510	20*95
419	OUT417	-3530	390	20*95
420	OUT418	-3550	510	20*95

No.	Name	X	Y	bump size(μm)
421	OUT419	-3570	390	20*95
422	OUT420	-3590	510	20*95
423	OUT421	-3610	390	20*95
424	OUT422	-3630	510	20*95
425	OUT423	-3650	390	20*95
426	OUT424	-3670	510	20*95
427	OUT425	-3690	390	20*95
428	OUT426	-3710	510	20*95
429	OUT427	-3730	390	20*95
430	OUT428	-3750	510	20*95
431	OUT429	-3770	390	20*95
432	OUT430	-3790	510	20*95
433	OUT431	-3810	390	20*95
434	OUT432	-3830	510	20*95
435	OUT433	-3850	390	20*95
436	OUT434	-3870	510	20*95
437	OUT435	-3890	390	20*95
438	OUT436	-3910	510	20*95
439	OUT437	-3930	390	20*95
440	OUT438	-3950	510	20*95
441	OUT439	-3970	390	20*95
442	OUT440	-3990	510	20*95
443	OUT441	-4010	390	20*95
444	OUT442	-4030	510	20*95
445	OUT443	-4050	390	20*95
446	OUT444	-4070	510	20*95
447	OUT445	-4090	390	20*95
448	OUT446	-4110	510	20*95
449	OUT447	-4130	390	20*95
450	OUT448	-4150	510	20*95
451	OUT449	-4170	390	20*95
452	OUT450	-4190	510	20*95
453	OUT451	-4210	390	20*95
454	OUT452	-4230	510	20*95
455	OUT453	-4250	390	20*95
456	OUT454	-4270	510	20*95
457	OUT455	-4290	390	20*95
458	OUT456	-4310	510	20*95
459	OUT457	-4330	390	20*95
460	OUT458	-4350	510	20*95
461	OUT459	-4370	390	20*95
462	OUT460	-4390	510	20*95
463	OUT461	-4410	390	20*95
464	OUT462	-4430	510	20*95
465	OUT463	-4450	390	20*95
466	OUT464	-4470	510	20*95
467	OUT465	-4490	390	20*95
468	OUT466	-4510	510	20*95
469	OUT467	-4530	390	20*95
470	OUT468	-4550	510	20*95
471	OUT469	-4570	390	20*95
472	OUT470	-4590	510	20*95
473	OUT471	-4610	390	20*95
474	OUT472	-4630	510	20*95
475	OUT473	-4650	390	20*95
476	OUT474	-4670	510	20*95
477	OUT475	-4690	390	20*95
478	OUT476	-4710	510	20*95
479	OUT477	-4730	390	20*95
480	OUT478	-4750	510	20*95

No.	Name	X	Y	bump size(μm)
481	OUT479	-4770	390	20*95
482	OUT480	-4790	510	20*95
483	DUMMY	-4810	390	20*95
484	DUMMY	-4830	510	20*95
485	TEST3	-5345	540	50*50
486	TEST3	-5275	540	50*50
487	TEST2	-5345	450	50*50
488	TEST2	-5275	450	50*50
489	TEST1	-5345	360	50*50
490	TEST1	-5275	360	50*50
491	PASS	-5345	270	50*50
492	PASS	-5275	270	50*50
493	POL	-5345	180	50*50
494	POL	-5275	180	50*50
495	OE	-5345	90	50*50
496	OE	-5275	90	50*50
497	LR	-5345	0	50*50
498	LR	-5275	0	50*50
499	CPV	-5345	-90	50*50
500	CPV	-5275	-90	50*50
501	STV	-5345	-180	50*50
502	STV	-5275	-180	50*50
503	POL	-5345	-270	50*50
504	POL	-5275	-270	50*50
505	STB	-5345	-360	50*50
506	STB	-5275	-360	50*50
507	VCOM	-5345	-450	50*50
508	VCOM	-5275	-450	50*50
509	VCOM	-5345	-540	50*50
510	VCOM	-5275	-540	50*50
511	VCOM	-4830	-525	50*100
512	VCOM	-4750	-525	50*100
513	VCOM	-4670	-525	50*100
514	VCOM	-4590	-525	50*100
515	COML	-4510	-525	50*100
516	COML	-4430	-525	50*100
517	COML	-4350	-525	50*100
518	COMH	-4270	-525	50*100
519	COMH	-4190	-525	50*100
520	COMH	-4110	-525	50*100
521	COMC	-4030	-525	50*100
522	COMPP	-3950	-525	50*100
523	VGR	-3870	-525	50*100
524	VGR	-3790	-525	50*100
525	VBGR	-3710	-525	50*100
526	VBGR	-3630	-525	50*100
527	DUMMY	-3550	-525	50*100
528	OSCIN	-3470	-525	50*100
529	OSCOUT	-3390	-525	50*100
530	OSCOUT	-3310	-525	50*100
531	LR	-3230	-525	50*100
532	RESETB	-3150	-525	50*100
533	DISPG	-3070	-525	50*100
534	TC2	-2990	-525	50*100
535	TC1	-2910	-525	50*100
536	SEQ1	-2830	-525	50*100
537	SEQ2	-2750	-525	50*100
538	VGLS1	-2670	-525	50*100
539	VGLS2	-2590	-525	50*100
540	VGLS3	-2510	-525	50*100

No.	Name	X	Y	bump size(μm)
541	VGHS1	-2430	-525	50*100
542	VGHS2	-2350	-525	50*100
543	VGHS3	-2270	-525	50*100
544	DUMMY	-2190	-525	50*100
545	VSS	-2110	-525	50*100
546	VSS	-2030	-525	50*100
547	VSS	-1950	-525	50*100
548	VSS	-1870	-525	50*100
549	VSS	-1790	-525	50*100
550	VSS	-1710	-525	50*100
551	CH_SEL	-1630	-525	50*100
552	LNIV	-1550	-525	50*100
553	VDD	-1470	-525	50*100
554	VDD	-1390	-525	50*100
555	VDD	-1310	-525	50*100
556	VDD	-1230	-525	50*100
557	VDC	-1150	-525	50*100
558	VDC	-1070	-525	50*100
559	VDC	-990	-525	50*100
560	VDC	-910	-525	50*100
561	C5P	-830	-525	50*100
562	C5P	-750	-525	50*100
563	C5P	-670	-525	50*100
564	C5P	-590	-525	50*100
565	C5N	-510	-525	50*100
566	C5N	-430	-525	50*100
567	C5N	-350	-525	50*100
568	C5N	-270	-525	50*100
569	VCL	-190	-525	50*100
570	VCL	-110	-525	50*100
571	VCL	-30	-525	50*100
572	VCL	50	-525	50*100
573	VCL	130	-525	50*100
574	VCL	210	-525	50*100
575	VGH	290	-525	50*100
576	VGH	370	-525	50*100
577	VGH	450	-525	50*100
578	VGH	530	-525	50*100
579	C1AP	610	-525	50*100
580	C1AP	690	-525	50*100
581	C1AP	770	-525	50*100
582	C2P	850	-525	50*100
583	C2P	930	-525	50*100
584	C2P	1010	-525	50*100
585	C2N	1090	-525	50*100
586	C2N	1170	-525	50*100
587	C2N	1250	-525	50*100
588	C1BP	1330	-525	50*100
589	C1BP	1410	-525	50*100
590	C1BP	1490	-525	50*100
591	C1N	1570	-525	50*100
592	C1N	1650	-525	50*100
593	C1N	1730	-525	50*100
594	VDC	1810	-525	50*100
595	VDC	1890	-525	50*100
596	VDC	1970	-525	50*100
597	VDC	2050	-525	50*100
598	VDC	2130	-525	50*100
599	VDC	2210	-525	50*100
600	C3P	2290	-525	50*100

No.	Name	X	Y	bump size(μm)
601	C3P	2370	-525	50*100
602	C3P	2450	-525	50*100
603	C3N	2530	-525	50*100
604	C3N	2610	-525	50*100
605	C3N	2690	-525	50*100
606	C4P	2770	-525	50*100
607	C4P	2850	-525	50*100
608	C4P	2930	-525	50*100
609	C4N	3010	-525	50*100
610	C4N	3090	-525	50*100
611	C4N	3170	-525	50*100
612	DUMMY	3250	-525	50*100
613	DUMMY	3330	-525	50*100
614	DUMMY	3410	-525	50*100
615	VGL	3490	-525	50*100
616	VGL	3570	-525	50*100
617	VGL	3650	-525	50*100
618	VGL	3730	-525	50*100
619	VSS	3810	-525	50*100
620	VSS	3890	-525	50*100
621	VSS	3970	-525	50*100
622	VSS	4050	-525	50*100
623	VDC	4130	-525	50*100
624	VDC	4210	-525	50*100
625	VDC	4290	-525	50*100
626	VDC	4370	-525	50*100
627	VDC	4450	-525	50*100
628	AVDD	4530	-525	50*100
629	AVDD	4610	-525	50*100
630	AVDD	4690	-525	50*100

No.	Name	X	Y	bump size(μm)
631	AVDD	4770	-525	50*100
632	AVDD	4850	-525	50*100
633	DUMMY	5275	-540	50*50
634	DUMMY	5345	-540	50*50
635	DUMMY	5275	-450	50*50
636	DUMMY	5345	-450	50*50
637	STB	5275	-360	50*50
638	STB	5345	-360	50*50
639	POL	5275	-270	50*50
640	POL	5345	-270	50*50
641	STV	5275	-180	50*50
642	STV	5345	-180	50*50
643	CPV	5275	-90	50*50
644	CPV	5345	-90	50*50
645	LR	5275	0	50*50
646	LR	5345	0	50*50
647	OE	5275	90	50*50
648	OE	5345	90	50*50
649	POL	5275	180	50*50
650	POL	5345	180	50*50
651	PASS	5275	270	50*50
652	PASS	5345	270	50*50
653	DUMMY	5275	360	50*50
654	DUMMY	5345	360	50*50
655	DUMMY	5275	450	50*50
656	DUMMY	5345	450	50*50
657	DUMMY	5275	540	50*50
658	DUMMY	5345	540	50*50

9.5 Alignment mark center coordinates

Name	X	Y
L_AMK	-5050	510
R_AMK	5050	510

10. Ordering Information

Part No.	Package
HX8662-C000PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400 μm)

11. Revision History

Version	Date	Description of Changes
01	2007/06/12	New setup
	2008/04/14	All Pages Remove “preliminary” wording from the data sheet
02	2008/06/09	Page 6 Add Spec. for the delay between VGH and VGL