



HX8801 Data Sheet

TFT-LCD AV CONTROLLER

Version 02

August, 2002

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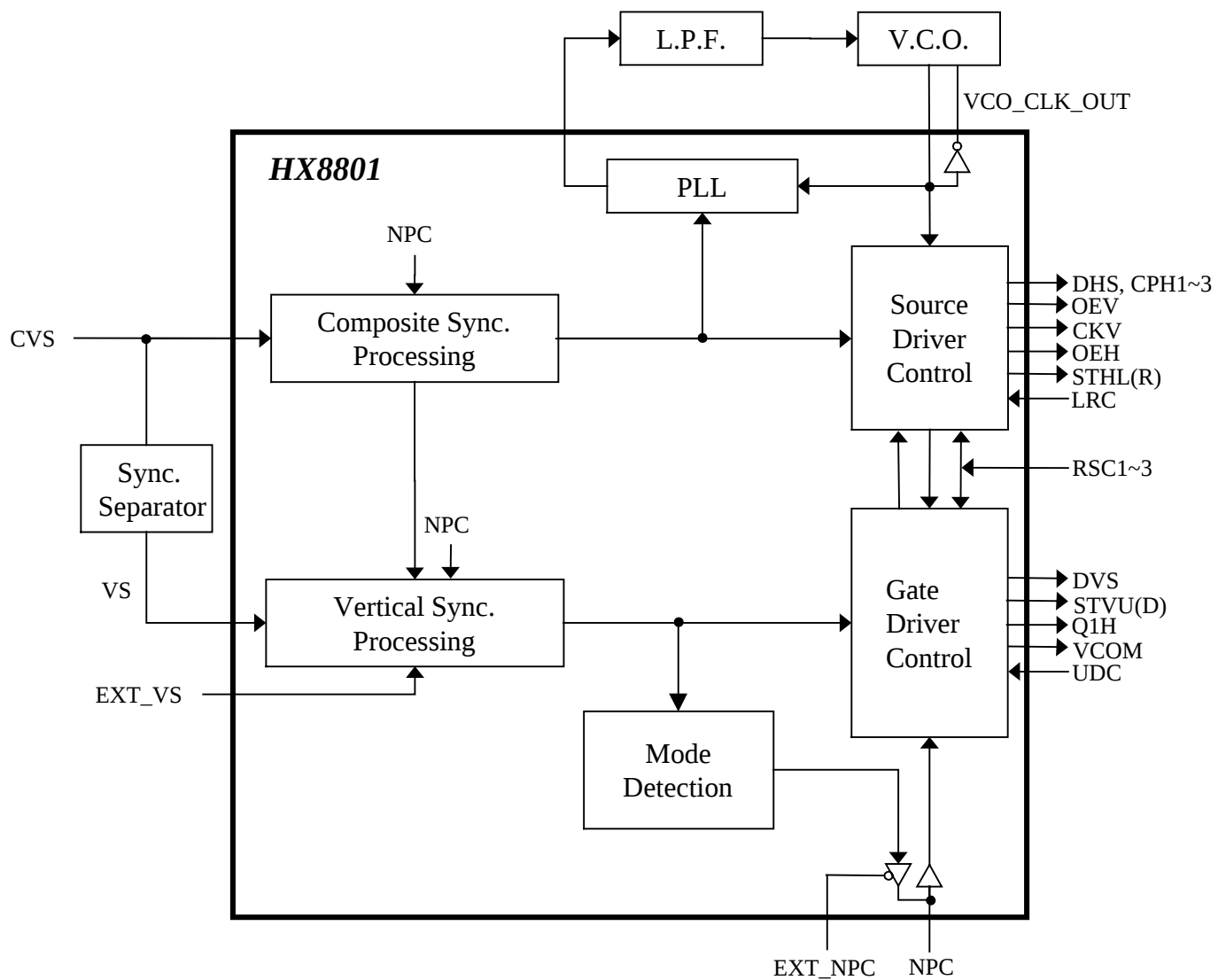
1. General Description

The HX8801 is a timing controller for small panel TFT-LCD. It provides horizontal and vertical control timing to TFT-LCD source and gate drivers. Built-in vertical synchronization detection generates vertical synchronization signal internally without the extra components. Built-in phase lock loop sub-function with external VCO and low pass filter circuits produces system clock which synchronizes input composite synchronization signal.

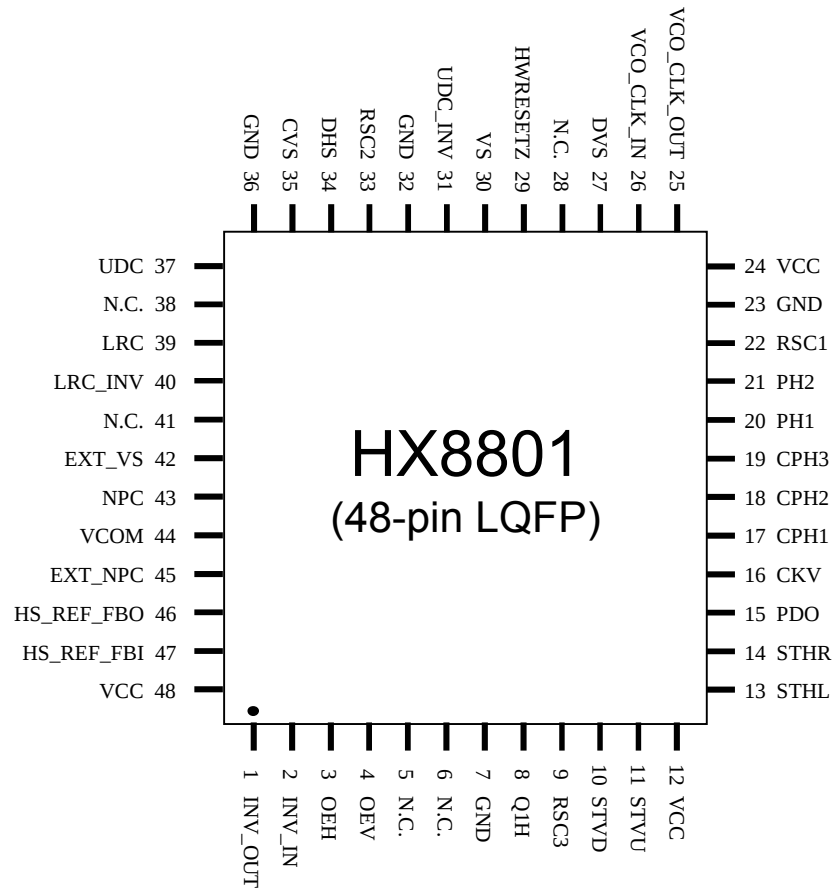
2. Features

- Support six display resolution mode, up to 1440×234 .
- Master clock frequency: 30 MHz max.
- Built-in vertical sync. detection to omit the external sync. separator.
- Single supply voltage: +5.0V.
- Shift clock signals for the source driver (3- ϕ Clock).
- Line inversion driving scheme.
- Support NTSC/PAL TV system.
- Provides source and gate drivers control timing.
- Provides flip and mirror scan control.
- 48 pins LQFP.

3. Block Diagram



4. Pin Assignment



5. Pin Description

Pin no.	Symbol	I/O	Description
1	INV_OUT	O	Inverter output
2	INV_IN	I	Inverter input
3	OEH	O	Source driver output enable control signal
4	OEV	O	Gate driver output enable control signal
5	N.C. ⁽¹⁾		
6	N.C. ⁽¹⁾		
7	GND		Ground
8	Q1H	O	R, G, B video signal sample & hold multiplexer control signal for source driver
9	RSC3 ⁽²⁾	I	Resolution mode setting pin III
10	STVD	O	Start pulse for gate driver. (1) STVD is "HiZ", when UDC="L" (2) STVD is "Output", when UDC="H"
11	STVU	O	Start pulse for gate driver. (1) STVU is "HiZ", when UDC="H" (2) STVU is "Output", when UDC="L"
12	VCC		+5.0V for controller power
13	STHL	O	Start pulse for source driver. (1) STHL is "HiZ", when LRC="H" (2) STHL is "Output", when LRC="L"
14	STHR	O	Start pulse for source driver. (1) STHR is "HiZ", when LRC="L" (2) STHR is "Output", when LRC="H"
15	PDO	O	Phase detector output
16	CKV	O	Shift clock for gate driver
17	CPH1	O	Shift clock ϕ_1 for source driver
18	CPH2	O	Shift clock ϕ_2 for source driver
19	CPH3	O	Shift clock ϕ_3 for source driver
20	PH1 ⁽³⁾	I	Phase compensation setting pin I
21	PH2 ⁽³⁾	I	Phase compensation setting pin II
22	RSC1 ⁽²⁾	I	Resolution mode setting pin I
23	GND		Ground
24	VCC		+5.0V for controller power
25	VCO_CLK_OUT	O	Inverted system clock signal output
26	VCO_CLK_IN	I	System clock input. It connects with external VCO and low pass filter circuits to generate system clock which synchronizes input composite synchronization signal
27	DVS	O	Negative polarity vertical synchronization signal output
28	N.C. ⁽¹⁾		
29	HWRESETZ ⁽⁴⁾	I	Active low global reset signal input
30	VS	I	Negative polarity vertical synchronization signal input which is from the external synchronization

Pin no.	Symbol	I/O	Description
			separator circuits
31	UDC_INV	O	UDC inverted signal output
32	GND		Ground
33	RSC2 ⁽²⁾	I	Resolution mode setting pin II
34	DHS	O	Horizontal synchronization signal output with negative polarity
35	CVS	I	Composite synchronization signal input with positive polarity
36	GND		Ground
37	UDC	I	Up / Down scan setting pin (1) Normal scan, when UDC="L" (2) Reverse scan, when UDC="H"
38	N.C. ⁽¹⁾		
39	LRC	I	Left / Right scan setting pin (1) Normal scan, LRC="L" (2) Reverse scan, LRC="H"
40	LRC_INV	O	LRC inverted signal output
41	N.C. ⁽¹⁾		
42	EXT_VS	I	VS detection setting pin (1) VS is from external detection , when EXT_VS="H" (2) VS is from internal detection , when EXT_VS="L"
43	NPC	I/O	Video signal input format setting pin (1) Input format is "PAL", when NPC="L" (2) Input format is "NTSC", when NPC="H"
44	VCOM	O	Toggling signal for common electrode generation circuits
45	EXT_NPC	I	NPC I/O setting pin (1) NPC is "Output", when EXT_NPC ="L" (2) NPC is "Input", when EXT_NPC ="H"
46	HS_REF_FBO	O	Reference signal output for phase lock loop operation
47	HS_REF_FBI	I	Reference signal input for phase lock loop operation
48	VCC		+5.0V for controller power

Note: (1) The N.C. pins should be set "OPEN" for normal operation.

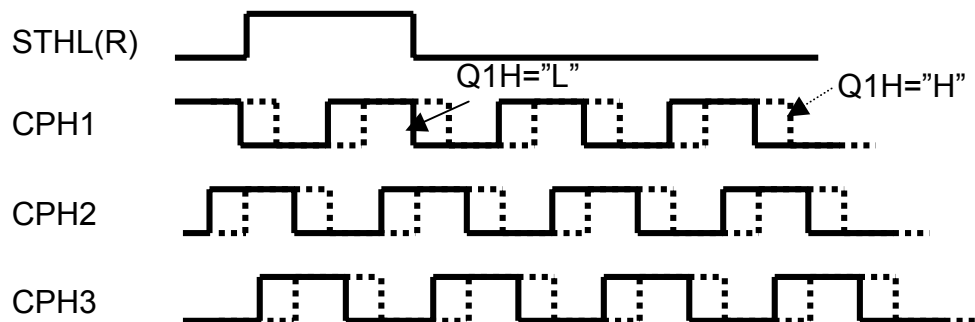
(2) Resolution mode setting:

RSC1	RSC2	RSC3	Resolution mode(H × V)
H	H	L	280 × 220
L	H	L	528 × 220
H	H	H	480 × 234
L	H	H	960 × 234
L	L	H	1152 × 234
H	L	H	1440 × 234

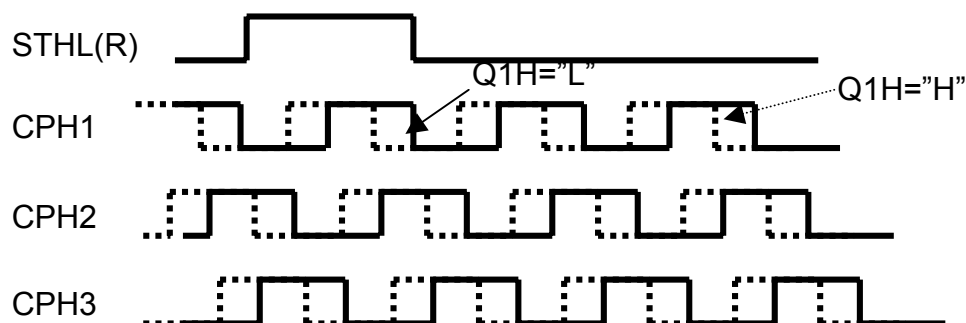
(3) Phase compensation setting:

PH1	PH2	Description
H	L	CPH1~3 phase lag as Q1H changes from 'L' to 'H'
L	L	CPH1~3 phase lead as Q1H changes from 'L' to 'H'
H	H	Normal phase operation
L	H	Normal phase operation

◆ PH1="H" and PH2="L"



◆ PH1="L" and PH2="L"



(4) Need external RC reset circuit.



6. DC Characteristics

6.1 Absolute maximum ratings:

Parameter	Symbol	Rating	Units
Power supply	V_{CC}	-0.3 to 6.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Storage temperature	T_{STG}	-40 to 125	°C

6.2 Recommended operating conditions:

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	-	V_{CC}	V
Operating temperature	T_{OPR}	TBD	-	85	°C

6.3 Electrical Characteristics:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA
Tri-state leakage current	I_{OZ}		-10	-	10	μA
Input capacitance	C_{IN}		-	3	-	pF
Output capacitance	C_{OUT}		3	-	6	pF
Logic input low voltage	V_{IL}	TTL	-	-	0.8	V
Schmitt input low voltage	$V_{SIL}^{(1)}$	TTL	-	TBD	-	V
Logic input high voltage	V_{IH}	TTL	2.0	-	-	V
Schmitt input high voltage	$V_{SIH}^{(1)}$	TTL	-	TBD	-	V
Output low voltage	V_{OL}	$I_{OL}=4mA$	-	-	$0.2V_{CC}$	V
Output high voltage	V_{OH}	$I_{OH}=-4mA$	$0.8V_{CC}$	-	-	V
Output low voltage	$V_{OL1}^{(2)}$	$I_{OL}=8mA$	-	-	$0.2V_{CC}$	V
Output high voltage	$V_{OH1}^{(2)}$	$I_{OH}=-8mA$	$0.8V_{CC}$	-	-	V
Input pull up/down resistance	R_I	$V_{IL}=0V$ or $V_{IH}=V_{CC}$	50	-	100	$k\Omega$

Note: (1) INV_IN, RSC3, HWRESETZ, VCO_CLK_IN, VS, CVS, HS_REF_FBI.
 (2) VCO_CLK_OUT.


6.4 Current consumption for 5 Volts operating:

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Full Chip Current Consumption	I_{IN}	$V_{CC}=+5.0V$, $f_{OSC} = 5.6 \text{ MHz}$	-	-	TBD	mA
		$V_{CC}=+5.0V$, $f_{OSC} = 9.6 \text{ MHz}$	-	-	TBD	mA
		$V_{CC}=+5.0V$, $f_{OSC} = 11.3 \text{ MHz}$	-	-	TBD	mA
		$V_{CC}=+5.0V$, $f_{OSC} = 19.2 \text{ MHz}$	-	-	TBD	mA
		$V_{CC}=+5.0V$, $f_{OSC} = 23.2 \text{ MHz}$	-	-	TBD	mA
		$V_{CC}=+5.0V$, $f_{OSC} = 29.1 \text{ MHz}$	-	-	TBD	mA

7. AC Characteristics

7.1 280 × 220 resolution mode

a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	150	166	183	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	lines
	PAL	-	312.5	-	lines

b. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time ⁽¹⁾	t_r	-	-	10	ns
Falling time ⁽¹⁾	t_f	-	-	10	ns
Clock high and low level pulse width ⁽²⁾	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- ϕ clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	9	-	t_{CPH}
OEH pulse width	t_{OEH}	-	2	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	16	-	t_{CPH}
OEV pulse width	t_{OEV}	-	10	-	t_{CPH}
CKV pulse width	t_{CKV}	-	11	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	7	-	t_{CPH}
DHS-CKV time	t_2	-	4	-	t_{CPH}
DHS-OEV time	t_3	-	3	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	6	-	t_{CPH}
STV setup time	t_{SUV}	-	2	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	27	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	27	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3


7.2 528 × 220 resolution mode
a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	85	94	103	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	line
	PAL	-	312.5	-	line

b. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time ⁽¹⁾	t_r	-	-	10	ns
Falling time ⁽¹⁾	t_f	-	-	10	ns
Clock high and low level pulse width ⁽²⁾	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	18	-	t_{CPH}
OEH pulse width	t_{OEH}	-	5	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}
OEV pulse width	t_{OEV}	-	14	-	t_{CPH}
CKV pulse width	t_{CKV}	-	24	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	13	-	t_{CPH}
DHS-CKV time	t_2	-	7	-	t_{CPH}
DHS-OEV time	t_3	-	1	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	12	-	t_{CPH}
STV setup time	t_{SUV}	-	4	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	28	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	28	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3



7.3 480 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	94	104	114	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	line
	PAL	-	312.5	-	line

b. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time ⁽¹⁾	t_r	-	-	10	ns
Falling time ⁽¹⁾	t_f	-	-	10	ns
Clock high and low level pulse width ⁽²⁾	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- ϕ clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	15	-	t_{CPH}
OEH pulse width	t_{OEH}	-	3	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}
OEV pulse width	t_{OEV}	-	13	-	t_{CPH}
CKV pulse width	t_{CKV}	-	20	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	11	-	t_{CPH}
DHS-CKV time	t_2	-	6	-	t_{CPH}
DHS-OEV time	t_3	-	2	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	10	-	t_{CPH}
STV setup time	t_{SUV}	-	3	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	27	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	27	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3


7.4 960 × 234 resolution mode
a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	47	52	57	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	line
	PAL	-	312.5	-	line

b. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time ⁽¹⁾	t_r	-	-	10	ns
Falling time ⁽¹⁾	t_f	-	-	10	ns
Clock high and low level pulse width ⁽²⁾	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- ϕ clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	30	-	t_{CPH}
OEH pulse width	t_{OEH}	-	7	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	54	-	t_{CPH}
OEV pulse width	t_{OEV}	-	26	-	t_{CPH}
CKV pulse width	t_{CKV}	-	40	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	21	-	t_{CPH}
DHS-CKV time	t_2	-	12	-	t_{CPH}
DHS-OEV time	t_3	-	4	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	20	-	t_{CPH}
STV setup time	t_{SUV}	-	6	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	27	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	27	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3


7.5 1152 × 234 resolution mode
a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	39	43	47	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	line
	PAL	-	312.5	-	line

b. Output signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time ⁽¹⁾	t_r	-	-	10	ns
Falling time ⁽¹⁾	t_f	-	-	10	ns
Clock high and low level pulse width ⁽²⁾	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- ϕ clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	36	-	t_{CPH}
OEH pulse width	t_{OEH}	-	9	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	61	-	t_{CPH}
OEV pulse width	t_{OEV}	-	40	-	t_{CPH}
CKV pulse width	t_{CKV}	-	50	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse WIDTH	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	27	-	t_{CPH}
DHS-CKV time	t_2	-	14	-	t_{CPH}
DHS-OEV time	t_3	-	12	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	26	-	t_{CPH}
STV setup time	t_{SUV}	-	8	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	27	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	27	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3


7.6 1440 × 234 resolution mode
a. Input signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period	t_{OSC}	33	34	35	ns
CVS period	t_H	61.5	63.5	65.5	us
CVS pulse width	t_{CVS}	4	4.7	5.4	us
CVS rising time	t_{Cr}	-	-	700	ns
CVS falling time	t_{Cf}	-	-	300	ns
VS pulse width	t_{VS}	1	3	5	t_H
VS rising time	t_{Vr}	-	-	700	ns
VS falling time	t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC	-	262.5	-	line
	PAL	-	312.5	-	line

b. Output signal characteristics

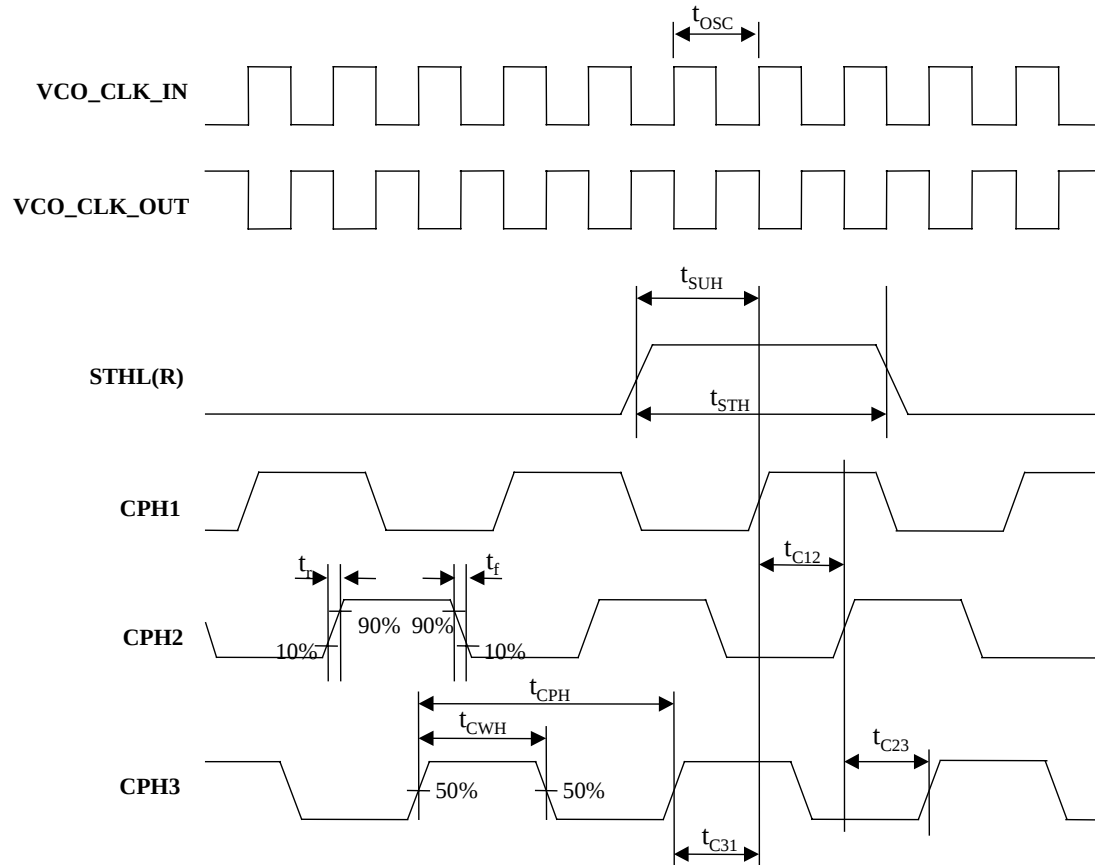
PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Rising time	t_r	-	-	10	ns
Falling time	t_f	-	-	10	ns
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty	t_{CWH}	40	50	60	%
3- ϕ clock phase difference	$t_{C12}, t_{C23}, t_{C31}$	-	$t_{CPH}/3$	-	ns
STH setup time	t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width	t_{STH}	-	1	-	t_{CPH}
DHS pulse width	t_{HS}	-	46	-	t_{CPH}
OEH pulse width	t_{OEH}	-	12	-	t_{CPH}
Sample & hold disable time	t_{DIS1}	-	80	-	t_{CPH}
OEV pulse width	t_{OEV}	-	46	-	t_{CPH}
CKV pulse width	t_{CKV}	-	37	-	t_{CPH}
HS_REF_FBO period	t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty	t_{WCP}	-	1/2	-	t_H
DHS-OEH time	t_1	-	34	-	t_{CPH}
DHS-CKV time	t_2	-	28	-	t_{CPH}
DHS-OEV time	t_3	-	8	-	t_{CPH}
DHS-HS_REF_FBO time	t_4	-	32	-	t_{CPH}
STV setup time	t_{SUV}	-	16	-	t_{CPH}
STV pulse width	t_{STV}	-	1	-	t_H
DVS-STVD time(UDC='H')	NTSC	t_{VS1}	-	19	t_H
	PAL	t_{VS1}	-	27	t_H
DVS-STVU time(UDC='L')	NTSC	t_{VS2}	-	19	t_H
	PAL	t_{VS2}	-	27	t_H
OEH-STV time	t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

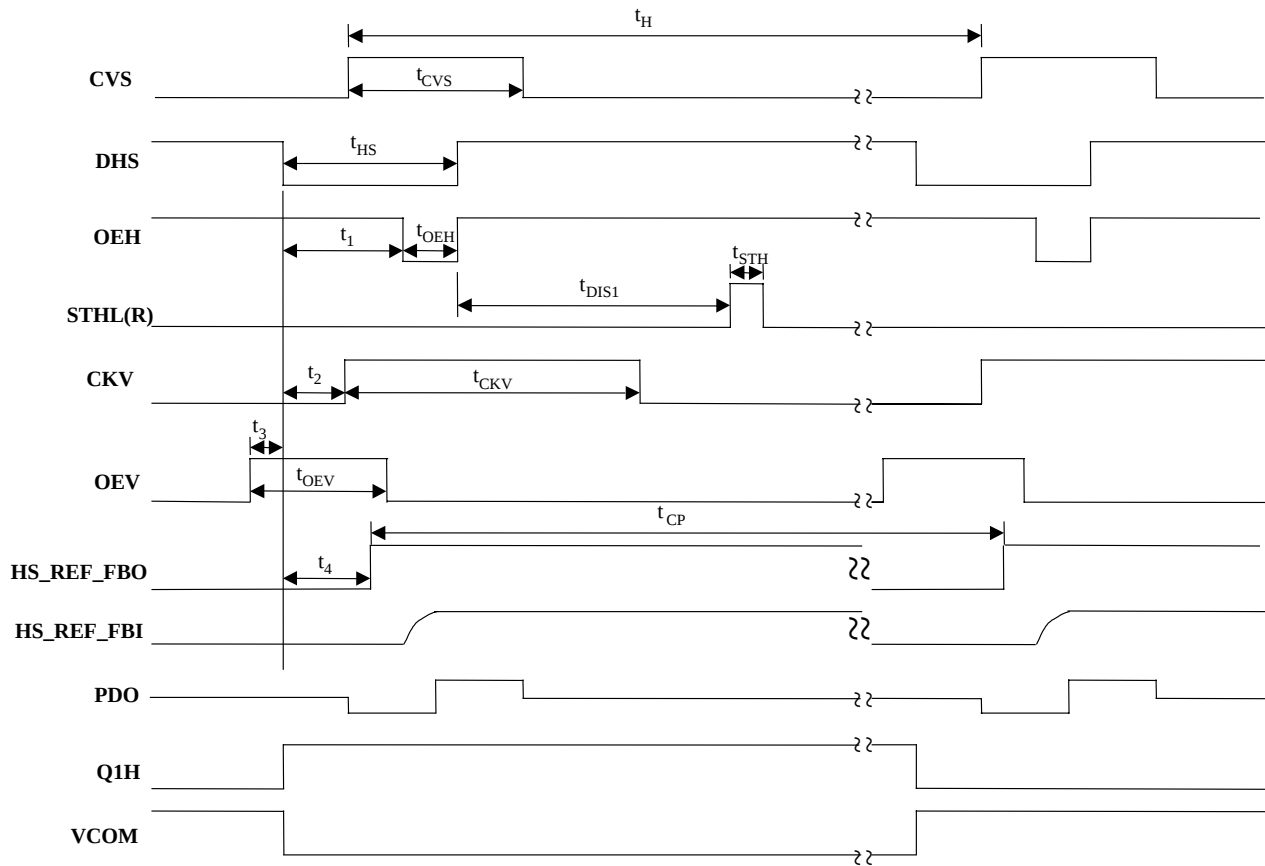
(2) CPH1~3

8. Waveform

8.1 VCO_CLK, STHL(R) and CPH1~3 timing waveform

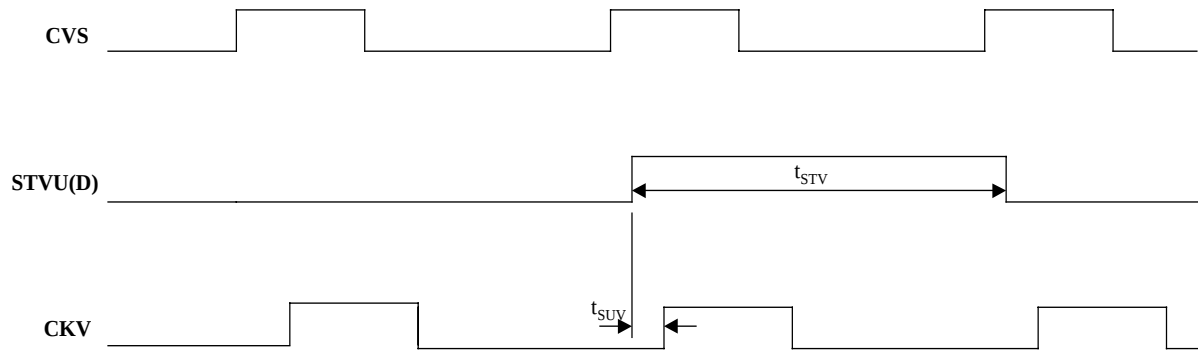


8.2 CVS and horizontal control timing waveform

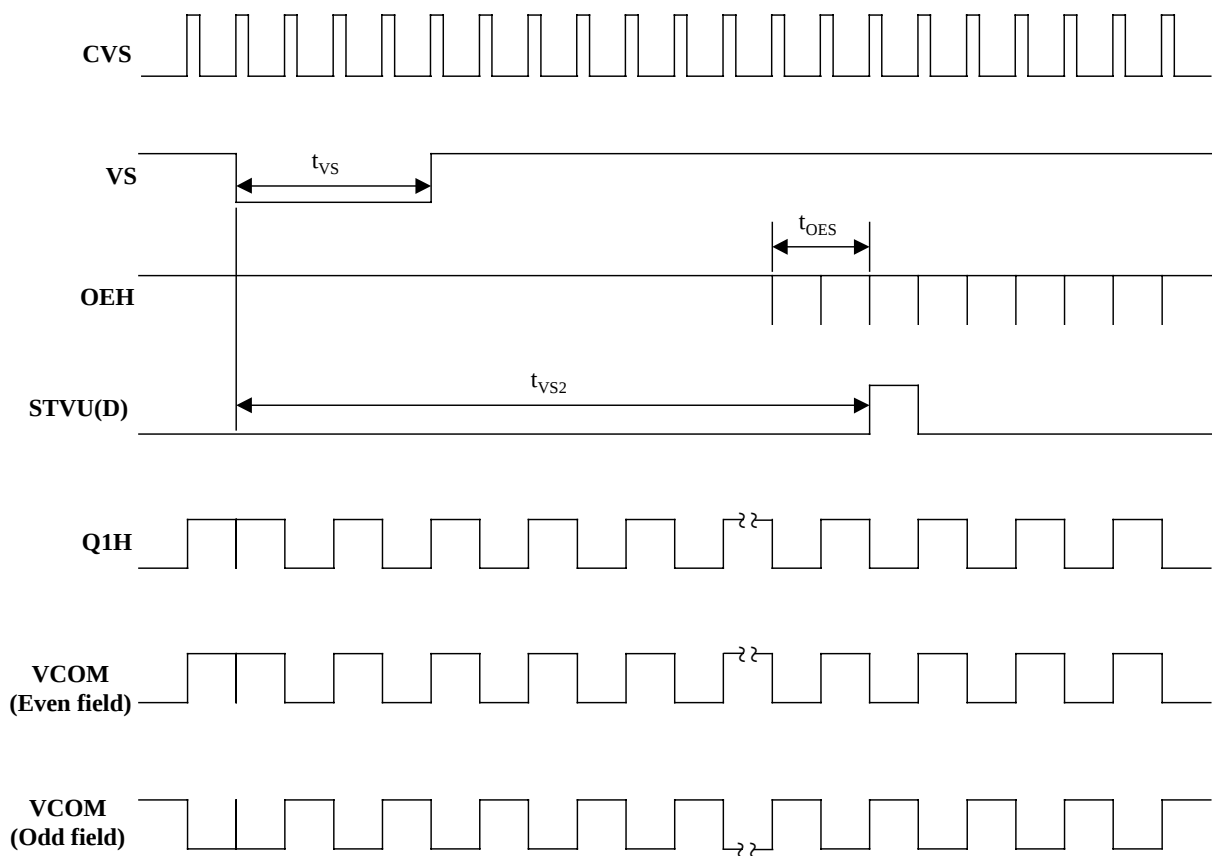


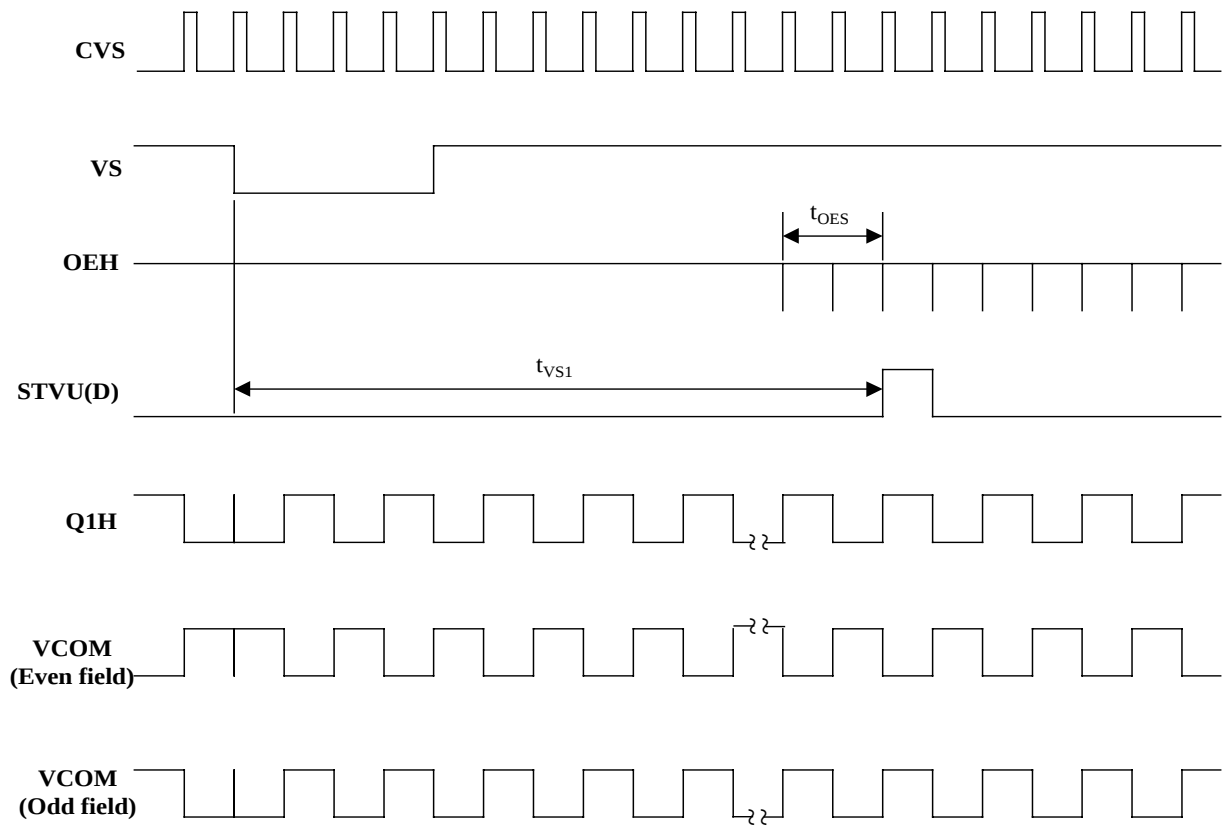
Note: In 960 x 234, 1152 x 234 and 1440 x 234 resolution mode, Q1H always keeps low.

8.3 CVS and vertical shift clock timing waveform

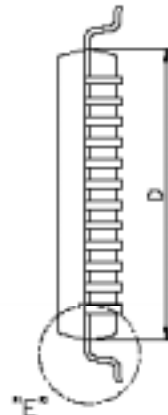
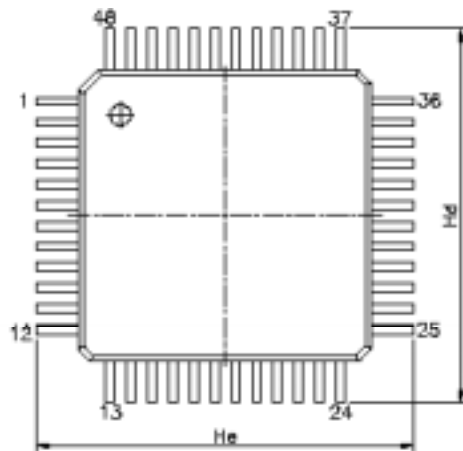


8.4 CVS and vertical control timing waveform (for the case of UDC="L")



8.5 CVS and vertical control timing waveform (for the case of UDC="H")

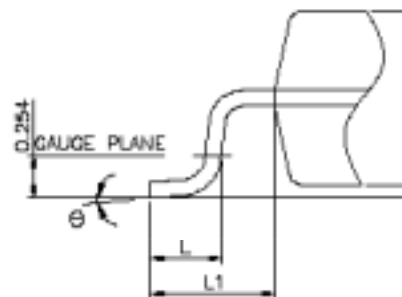
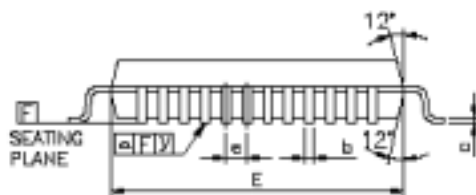
9. Package Outline Dimension



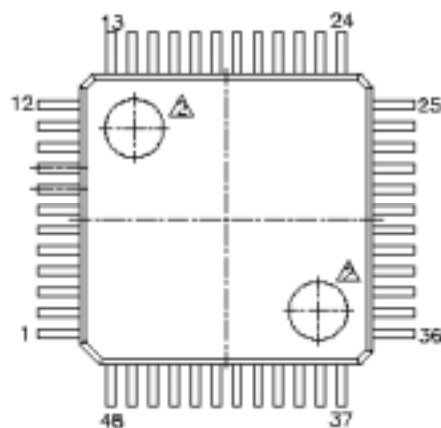
Unit Symbol	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400±0.05	0.0551±0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000±0.100	0.2756±0.0039
E	7.000±0.100	0.2756±0.0039
e	0.500TYP	0.0196TYP
Hd	9.000±0.250	0.3543±0.0098
He	9.000±0.250	0.3543±0.0098
L	0.600±0.150	0.0236±0.006
L1	1.000REF	0.0393REF
Y	0.100MAX.	0.0039MAX.
θ	0°~7°	0°~7°

NOTES:

1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
5. GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.



DETAIL "E"





10. Ordering Information

Part NO.	Package
HX8801 LA	48-pin LQFP

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2001/09/13	New setup
02	2002/8/5	Update "pin 20,21:N.C." to "phase compensation seting pin I, II."