HX8802A/HX8802B Data Sheet
TFT-LCD TCON with DAC

Version 06

March, 2004

Himax Technologies, Inc.
1F, No.12, Nanke 8th Road,
Tainan Science-Based Industrial Park,
Tainan County, Taiwan 741, R.O.C.

TEL: 886-6-505-0880
FAX: 886-6-505-0891

DOC No:HX8802-DS

HX8802A/HX8802B

TFT-LCD TCON with DAC

March, 2004, Version 06

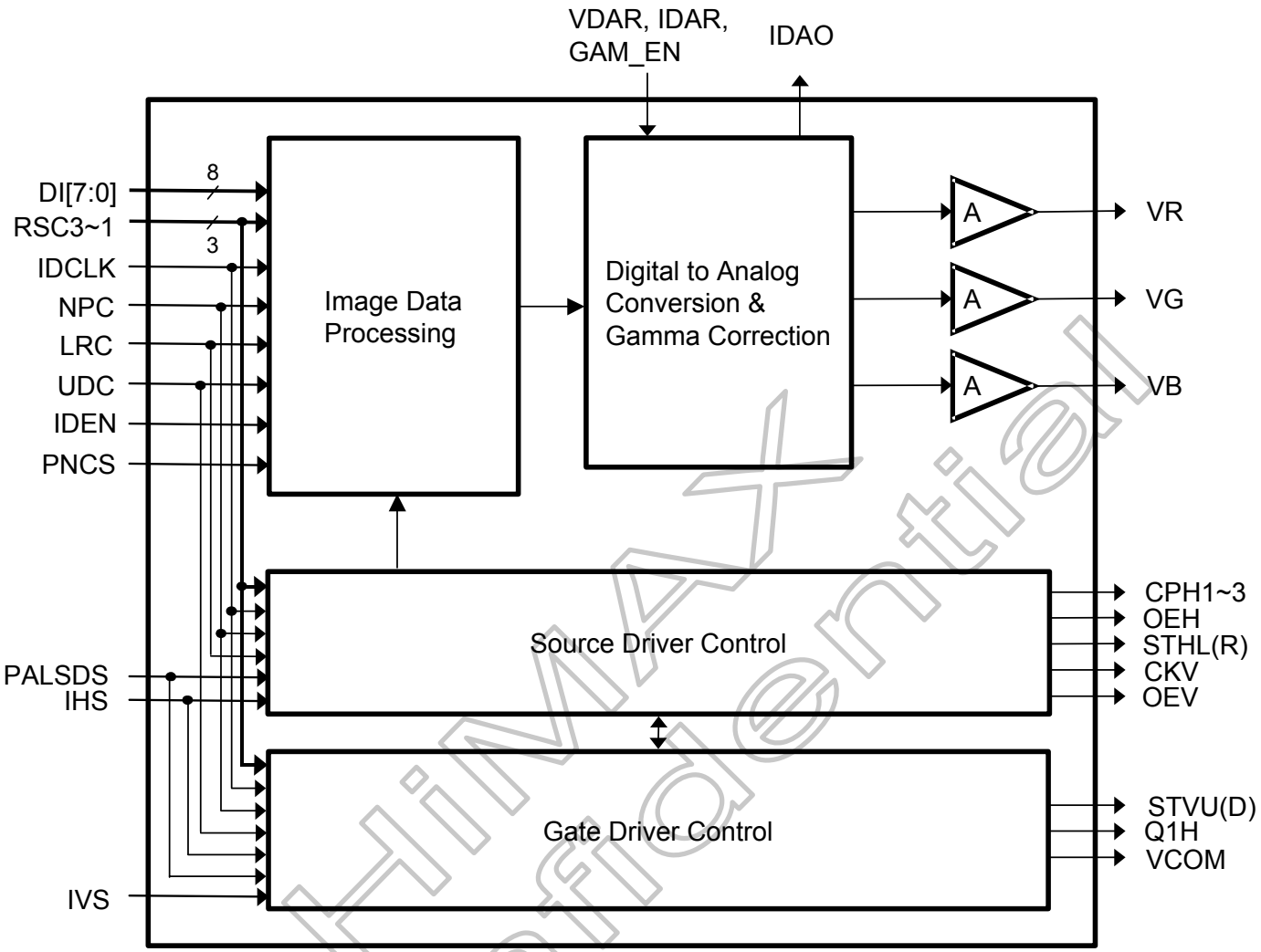
1. General Description

The HX8802A/HX8802B is a TFT-LCD timing controller with built-in gamma correction and DAC circuits. It provides horizontal and vertical control timing to TFT-LCD source and gate drivers. With built-in DAC and operational amplifiers, this controller performs gamma correction and polarity inverted function to convert digital RGB data into analog amplified and alternated RGB signals for TFT-LCD panel.

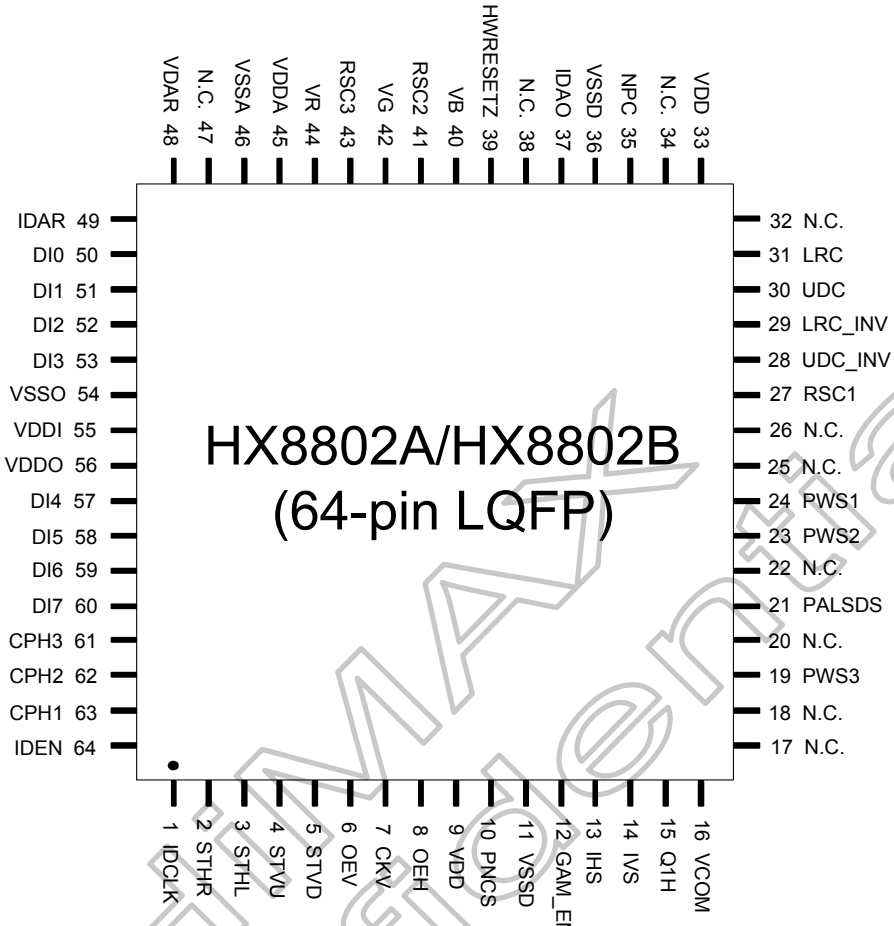
2. Features

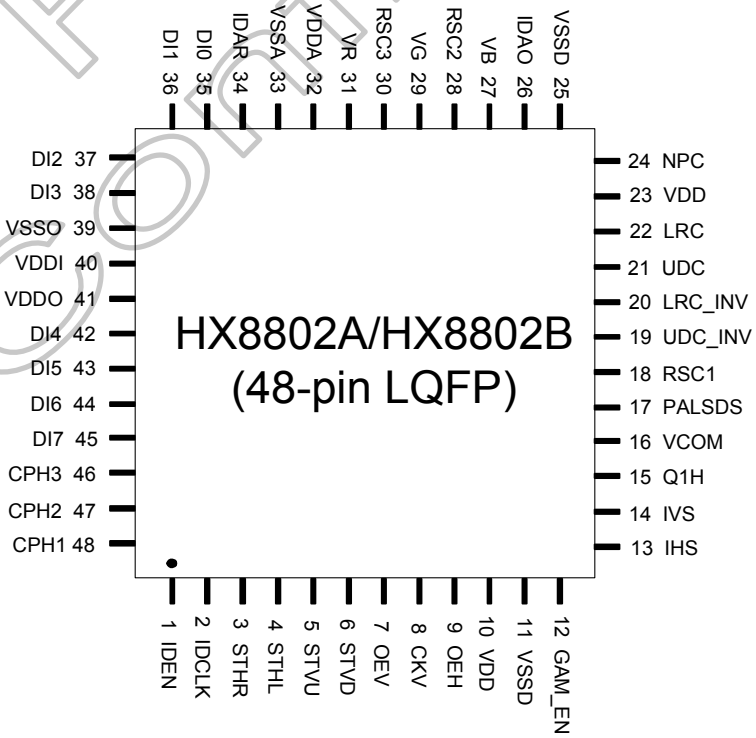
- Support different display resolution modes, up to 1440 x 234.
- Support two types of panel group.
- Master clock frequency: 30 MHz max.
- Support NTSC/PAL TV system.
- Built-in gamma correction function.
- Built-in polarity inverted function.
- Line inversion driving scheme.
- Provide source and gate drivers control timing.
- Shift clock signals for the source driver(3-ϕ clock).
- Provide flip and mirror scan control.
- Optional 3.3V input and output level.
- Single supply voltage: +5.0V
- 64 or 48 pins LQFP.

3. Block Diagram



4. Pin Assignment





5. Pin Description

Pin no. 64 pin	Pin no. 48 pin	Symbol	I/O	Description
1	2	IDCLK	I	Input data sampling clock at rising edge
2	3	STHR	O	Start pulse for source driver. (1) STHR is ”HiZ”, when LRC=”H” (2) STHR is ”Output”, when LRC=”L”
3	4	STHL	O	Start pulse for source driver. (1) STHL is ”HiZ”, when LRC=”L” (2) STHL is ”Output”, when LRC=”H”
4	5	STVU	O	Start pulse for gate driver. (1) STVU is “HiZ”, when UDC=”H” (2) STVU is ”Output”, when UDC=”L”
5	6	STVD	O	Start pulse for gate driver. (1) STVD is ”HiZ”, when UDC=”L” (2) STVD is ”Output”, when UDC=”H”
6	7	OEV	O	Gate driver output enable control
7	8	CKV	O	Shift clock for gate driver
8	9	OEH	O	Source driver output enable control
9	10	VDD		Digital supply voltage
10		PNCS(1)	I	Panel group setting (1) For panel group I, when PNCS=”L”(refer to HX8802A for this setting) (2) For panel group II, when PNCS=”H”(refer to HX8802B for this setting)
11	11	VSSD		Digital supply ground
12	12	GAM_EN	I	Gamma correction enable control(default pull-up) (1)Gamma correction enable, when GAM_EN=”H” (2)Gamma correction disable, when GAM_EN=”L”
13	13	IHS	I	Horizontal sync input with negative polarity
14	14	IVS	I	Vertical sync input with negative polarity
15	15	Q1H	O	R, G, B video signals sample & hold multiplexer control signal for source driver
16	16	VCOM	O	Toggling signal for common electrode generation circuits
17		N.C. (2)		
18		N.C. (2)		
19		PWS3	O	Pulse width signal III
20		N.C. (2)		
21	17	PALSDS(3)	I	PAL scale down algorithm setting pin I
22		N.C. (2)		
23		PWS2	O	Pulse width signal II
24		PWS1	O	Pulse width signal I
25		N.C. (2)		
26		N.C. (2)		

Pin no. 64 pin	Pin no. 48 pin	Symbol	I/O	Description
27	18	RSC1(1)	I	Resolution mode setting pin I
28	19	UDC_INV(3)	I/O	Strapped input pin used as PAL scale down algorithm setting pin II during reset. Normal operation is UDC inverted signal output.
29	20	LRC_INV(3)	I/O	Strapped input pin used as PAL scale down algorithm setting pin III during reset. Normal operation is LRC inverted signal output.
30	21	UDC	I	Up / Down scan setting (1) Normal scan, when UDC="L" (2) Reverse scan, when UDC="H"
31	22	LRC	I	Left / Right scan setting (1) Normal scan, when LRC="H" (2) Reverse scan, when LRC="L"
32		N.C. (4)		
33	23	VDD		Digital supply voltage
34		N.C. (4)		
35	24	NPC	I	Video signal input format setting (1) Input format is "PAL", when NPC="L" (2) Input format is "NTSC, when NPC="H"
36	25	VSSD		Digital supply ground
37	26	IDAO	O	Current output for DAC
38		N.C. (2)		
39		HWRESETZ	I	Active low global reset signal input
40	27	VB	O	Analog blue signal output
41	28	RSC2(1)	I	Resolution mode setting pin II
42	29	VG	O	Analog green signal output
43	30	RSC3(1)	I	Resolution mode setting pin III
44	31	VR	O	Analog red signal output
45	32	VDDA		Analog supply voltage
46	33	VSSA		Analog supply ground
47		N.C.		
48		VDAR	I	Reference voltage input for DAC(default open)
49	34	IDAR	O	Reference current output for DAC
50	35	DI0	I	Digital image data input, bit0(default pull-down)
51	36	DI1	I	Digital image data input, bit1(default pull-down)
52	37	DI2	I	Digital image data input, bit2
53	38	DI3	I	Digital image data input, bit3
54	39	VSSO		Digital supply ground
55	40	VDDI		Digital supply voltage for input pins
56	41	VDDO		Digital supply voltage for output pins
57	42	DI4	I	Digital image data input, bit4
58	43	DI5	I	Digital image data input, bit5
59	44	DI6	I	Digital image data input, bit6
60	45	DI7	I	Digital image data input, bit7
61	46	CPH3	O	Shift clock $\phi 3$ for source driver

Pin no. 64 pin	Pin no. 48 pin	Symbol	I/O	Description
62	47	CPH2	O	Shift clock $\phi 2$ for source driver
63	48	CPH1	O	Shift clock $\phi 1$ for source driver
64	1	IDEN	I	Input data enable control

Note: (1) Resolution mode setting:
Panel group I: set PNCS="L"(refer to HX8802A for this setting)

RSC3	RSC2	RSC1	Resolution mode(H × V)
L	L	L	280 × 220
H	L	L	320 × 240
H	H	L	528 × 220
H	H	H	480 × 234 (2.5")
L	L	H	480 × 234 (4.0")
H	L	H	960 × 234
L	H	L	1152 × 234
L	H	H	1440 × 234

Panel group II: set PNCS="H"(refer to HX8802B for this setting)

RSC3	RSC2	RSC1	Resolution mode(H × V)
L	L	L	240 × 234
H	H	L	320 × 240
H	H	H	480 × 234
H	L	L	640 × 240
L	L	H	720 × 234
H	L	H	960 × 234
L	H	L	1200 × 234
L	H	H	1440 × 234

(2) The N.C. pins should be set "OPEN" for normal operation.
(3) PAL scale down algorithm setting:

PALSDS	UDC_INV	LRC_INV	Algorithm
L	L	L	Algorithm I
L	L	H	Algorithm II
L	H	L	Algorithm III
L	H	H	Algorithm IV
H	L	L	Algorithm V
H	L	H	Algorithm VI
H	H	L	Algorithm VII
H	H	H	Algorithm VIII

Note: (1) LRC_INV should be pulled to VDD or VSSD via a pull resistance.
(2) UDC_INV should be pulled to VDD or VSSD via a pull resistance.
(3) The N.C. pins should be set "OPEN" or pull to VSSD for normal operation.

6. DC Characteristics

6.1 Absolute maximum ratings:

Parameter	Symbol	Rating	Units
Power supply	V_{DD}(1)	-0.3 to 6.0	V
Output voltage	V_R, V_G, V_B	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 95	ºC

Note: (1) For V_{DD}, V_{DDI}, V_{DDO}, V_{DDA}.

6.2 Recommended operating conditions:

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	V_{DD}(1)	4.5	5.0	5.5	V
Operating temperature	T_{OPR}	25	-	85	ºC

Note: (1) For V_{DD}, V_{DDI}, V_{DDO}, V_{DDA}.

6.3 Electrical Characteristics for 3.3V:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA
Tri-state leakage current	I_{OZ}		-10	-	10	μA
Input capacitance	C_{IN}		-	3	-	pF
Output capacitance	C_{OUT}		3	-	6	pF
Logic input low voltage	V_{IL}(1)	CMOS	-	-	0.3V_{DD}	V
Logic input high voltage	V_{IH}(1)	CMOS	0.7V_{DD}	-	-	V
Output low voltage	V_{OL}	I_{OL}=4mA	-	-	0.2V_{DD}	V
Output high voltage	V_{OH}	I_{OH}=-4mA	0.8V_{DD}	-	-	V
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{DD}	20	-	100	kΩ

Note: (1) IHS, IVS, IDEN, IDCLK, UDC, LRC, DI0~DI7.

6.4 Electrical Characteristics for 5V:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA
Tri-state leakage current	I_{OZ}		-10	-	10	μA
Input capacitance	C_{IN}		-	3	-	pF
Output capacitance	C_{OUT}		3	-	6	pF
Logic input low voltage	V_{IL} (1)	CMOS	-	-	$0.3V_{DD}$	V
Logic input high voltage	V_{IH} (1)	CMOS	$0.7V_{DD}$	-	-	V
Output low voltage	V_{OL}	I_{OL}=4mA	-	-	$0.2V_{DD}$	V
Output high voltage	V_{OH}	I_{OH}=-4mA	$0.8V_{DD}$	-	-	V
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{DD}	20-	-	100	kΩ

Note: (1) IHS, IVS, IDEN, IDCLK, UDC, LRC, DI0~DI7.

7. AC Characteristics

7.1 Set PNCS="L" and refer to HX8802A for the following timing

7.1.1 280 × 220 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	176	-	ns
		PAL	-	177	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	360	-	t_C
		PAL	-	64	-	us
		PAL	-	360	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	280	-	t_C
		PAL	-	49.5	-	us
		PAL	-	280	-	t_C
IHS pulse width	t_{HP}		5	25	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	13.97	-	ms
		NTSC	-	220	-	t_H
		PAL	-	16.45	-	ms
		PAL	-	257	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	288	-	t_C
IHS-IDEN time	t_{HE}	36	-	72	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 61th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	25	-	t_H
			34		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	3	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	9	-	t_{CPH}
OEV pulse width		t_{OEV}	-	5	-	t_{CPH}
CKV pulse width		t_{CKV}	-	5	-	t_{CPH}
IHS-OEH time		t_1	-	8	-	t_{CPH}
IHS -CKV time		t_2	-	6	-	t_{CPH}
IHS -OEV time		t_3	-	2	-	t_{CPH}
STV setup time		t_{SUV}	-	3	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.1.2 320 × 240 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	156	-	ns
		PAL	-	157.2	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	407	-	t_C
		PAL	-	64	-	us
		PAL	-	407	-	t_C
IHS display period	t_{HD}	NTSC	-	49.9	-	us
		NTSC	-	320	-	t_C
		PAL	-	50.3	-	us
		PAL	-	320	-	t_C
IHS pulse width	t_{HP}		5	28	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	15.24	-	ms
		NTSC	-	240	-	t_H
		PAL	-	17.92	-	ms
		PAL	-	280	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	324	-	t_C
IHS-IDEN time	t_{HE}	54	-	83	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 66th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	15	-	t_H
			24		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	4	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	4	-	t_{CPH}
OEV pulse width		t_{OEV}	-	7	-	t_{CPH}
CKV pulse width		t_{CKV}	-	17	-	t_{CPH}
IHS-OEH time		t_1	-	14	-	t_{CPH}
IHS -CKV time		t_2	-	9	-	t_{CPH}
IHS -OEV time		t_3	-	4	-	t_{CPH}
STV setup time		t_{SUV}	-	5	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.1.3 528 × 220 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	93	-	ns
		PAL	-	94	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	679	-	t_C
		PAL	-	64	-	us
		PAL	-	679	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	528	-	t_C
		PAL	-	49.5	-	us
		PAL	-	528	-	t_C
IHS pulse width	t_{HP}		5	48	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	13.97	-	ms
		NTSC	-	220	-	t_H
		PAL	-	16.45	-	ms
		PAL	-	257	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	576	-	t_C
IHS-IDEN time	t_{HE}	81	-	151	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 97th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	25	-	t_H
			34		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	6	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	12	-	t_{CPH}
OEV pulse width		t_{OEV}	-	11	-	t_{CPH}
CKV pulse width		t_{CKV}	-	13	-	t_{CPH}
IHS-OEH time		t_1	-	14	-	t_{CPH}
IHS -CKV time		t_2	-	9	-	t_{CPH}
IHS -OEV time		t_3	-	2	-	t_{CPH}
STV setup time		t_{SUV}	-	6	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.1.4 480 × 234(2.5") resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	103	-	ns
		PAL	-	103	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	617	-	t_C
		PAL	-	64	-	us
		PAL	-	617	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	480	-	t_C
		PAL	-	49.5	-	us
		PAL	-	480	-	t_C
IHS pulse width	t_{HP}		5	44	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	480	-	t_C
IHS-IDEN time	t_{HE}	51	-	137	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 109th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	6	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	18	-	t_{CPH}
OEV pulse width		t_{OEV}	-	10	-	t_{CPH}
CKV pulse width		t_{CKV}	-	7	-	t_{CPH}
IHS-OEH time		t_1	-	12	-	t_{CPH}
IHS -CKV time		t_2	-	10	-	t_{CPH}
IHS -OEV time		t_3	-	2	-	t_{CPH}
STV setup time		t_{SUV}	-	8	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.1.5 480 × 234(4") resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	103	-	ns
		PAL	-	103	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	617	-	t_C
		PAL	-	64	-	us
		PAL	-	617	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	480	-	t_C
		PAL	-	49.5	-	us
		PAL	-	480	-	t_C
IHS pulse width	t_{HP}		5	44	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	480	-	t_C
IHS-IDEN time	t_{HE}	66	-	137	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 109th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	4	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	13	-	t_{CPH}
OEV pulse width		t_{OEV}	-	15	-	t_{CPH}
CKV pulse width		t_{CKV}	-	28	-	t_{CPH}
IHS-OEH time		t_1	-	19	-	t_{CPH}
IHS -CKV time		t_2	-	11	-	t_{CPH}
IHS -OEV time		t_3	-	2	-	t_{CPH}
STV setup time		t_{SUV}	-	7	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.1.6 960 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	51.5	-	ns
		PAL	-	51.8	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1235	-	t_C
		PAL	-	64	-	us
		PAL	-	1235	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	960	-	t_C
		PAL	-	49.5	-	us
		PAL	-	960	-	t_C
IHS pulse width	t_{HP}		5	91	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	960	-	t_C
IHS-IDEN time	t_{HE}	120	-	275	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 211th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	8	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	29	-	t_{CPH}
OEV pulse width		t_{OEV}	-	28	-	t_{CPH}
CKV pulse width		t_{CKV}	-	50	-	t_{CPH}
IHS-OEH time		t_1	-	33	-	t_{CPH}
IHS -CKV time		t_2	-	19	-	t_{CPH}
IHS -OEV time		t_3	-	3	-	t_{CPH}
STV setup time		t_{SUV}	-	14	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.1.7 1152 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	42.9	-	ns
		PAL	-	43.1	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1482	-	t_C
		PAL	-	64	-	us
		PAL	-	1482	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	1152	-	t_C
		PAL	-	49.5	-	us
		PAL	-	1152	-	t_C
IHS pulse width	t_{HP}		5	109	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	1152	-	t_C
IHS-IDEN time	t_{HE}	171	-	330	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 250th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	12	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	25	-	t_{CPH}
OEV pulse width		t_{OEV}	-	39	-	t_{CPH}
CKV pulse width		t_{CKV}	-	60	-	t_{CPH}
IHS-OEH time		t_1	-	46	-	t_{CPH}
IHS -CKV time		t_2	-	22	-	t_{CPH}
IHS -OEV time		t_3	-	4	-	t_{CPH}
STV setup time		t_{SUV}	-	14	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.1.8 1440 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	34.3	-	ns
		PAL	-	34.5	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1853	-	t_C
		PAL	-	64	-	us
		PAL	-	1853	-	t_C
IHS display period	t_{HD}	NTSC	-	49.4	-	us
		NTSC	-	1440	-	t_C
		PAL	-	49.5	-	us
		PAL	-	1440	-	t_C
IHS pulse width	t_{HP}		5	137	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	1440	-	t_C
IHS-IDEN time	t_{HE}	171	-	413	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 313th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	11	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	46	-	t_{CPH}
OEV pulse width		t_{OEV}	-	40	-	t_{CPH}
CKV pulse width		t_{CKV}	-	71	-	t_{CPH}
IHS-OEH time		t_1	-	47	-	t_{CPH}
IHS -CKV time		t_2	-	27	-	t_{CPH}
IHS -OEV time		t_3	-	4	-	t_{CPH}
STV setup time		t_{SUV}	-	19	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2 Set PNCS="H" and refer to HX8802B for the following timing

7.2.1 240 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	212.3	-	ns
		PAL	-	213.3	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	300	-	t_C
		PAL	-	64	-	us
		PAL	-	300	-	t_C
IHS display period	t_{HD}	NTSC	-	50.9	-	us
		NTSC	-	240	-	t_C
		PAL	-	51.2	-	us
		PAL	-	240	-	t_C
IHS pulse width	t_{HP}		5	21	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Input data enable control

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	240	-	t_C
IHS-IDEN time	t_{HE}	36	-	60	t_C

b-2. IDEN disable mode (IDEN = “L”)

The display starts from 51st clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	3	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	4	-	t_{CPH}
OEV pulse width		t_{OEV}	-	5	-	t_{CPH}
CKV pulse width		t_{CKV}	-	13	-	t_{CPH}
IHS-OEH time		t_1	-	10	-	t_{CPH}
IHS -CKV time		t_2	-	6	-	t_{CPH}
IHS -OEV time		t_3	-	3	-	t_{CPH}
STV setup time		t_{SUV}	-	3	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC=’L’)	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC=’H’)	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2.2 320 × 240 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	156	-	ns
		PAL	-	157.2	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	407	-	t_C
		PAL	-	64	-	us
		PAL	-	407	-	t_C
IHS display period	t_{HD}	NTSC	-	49.9	-	us
		NTSC	-	320	-	t_C
		PAL	-	50.3	-	us
		PAL	-	320	-	t_C
IHS pulse width	t_{HP}		5	28	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	15.24	-	ms
		NTSC	-	240	-	t_H
		PAL	-	17.92	-	ms
		PAL	-	280	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	324	-	t_C
IHS-IDEN time	t_{HE}	54	-	87	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 66th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	15	-	t_H
			24		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	4	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	4	-	t_{CPH}
OEV pulse width		t_{OEV}	-	7	-	t_{CPH}
CKV pulse width		t_{CKV}	-	17	-	t_{CPH}
IHS-OEH time		t_1	-	14	-	t_{CPH}
IHS -CKV time		t_2	-	10	-	t_{CPH}
IHS -OEV time		t_3	-	4	-	t_{CPH}
STV setup time		t_{SUV}	-	5	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2.3 480 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	106	-	ns
		PAL	-	106.6	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	600	-	t_C
		PAL	-	64	-	us
		PAL	-	600	-	t_C
IHS display period	t_{HD}	NTSC	-	50.9	-	us
		NTSC	-	480	-	t_C
		PAL	-	51.2	-	us
		PAL	-	480	-	t_C
IHS pulse width	t_{HP}		5	41	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	480	-	t_C
IHS-IDEN time	t_{HE}	75	-	120	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 109th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	6	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	10	-	t_{CPH}
OEV pulse width		t_{OEV}	-	10	-	t_{CPH}
CKV pulse width		t_{CKV}	-	25	-	t_{CPH}
IHS-OEH time		t_1	-	20	-	t_{CPH}
IHS -CKV time		t_2	-	15	-	t_{CPH}
IHS -OEV time		t_3	-	6	-	t_{CPH}
STV setup time		t_{SUV}	-	8	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2.4 640 × 240 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	78	-	ns
		PAL	-	78.6	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	814	-	t_C
		PAL	-	64	-	us
		PAL	-	814	-	t_C
IHS display period	t_{HD}	NTSC	-	49.92	-	us
		NTSC	-	640	-	t_C
		PAL	-	50.3	-	us
		PAL	-	640	-	t_C
IHS pulse width	t_{HP}		5	55	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	15.24	-	ms
		NTSC	-	240	-	t_H
		PAL	-	17.92	-	ms
		PAL	-	280	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	648	-	t_C
IHS-IDEN time	t_{HE}	111	-	174	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 132th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	15	-	t_H
			24		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	8	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	8	-	t_{CPH}
OEV pulse width		t_{OEV}	-	14	-	t_{CPH}
CKV pulse width		t_{CKV}	-	34	-	t_{CPH}
IHS-OEH time		t_1	-	28	-	t_{CPH}
IHS -CKV time		t_2	-	20	-	t_{CPH}
IHS -OEV time		t_3	-	8	-	t_{CPH}
STV setup time		t_{SUV}	-	10	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2.5 720 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	69.5	-	ns
		PAL	-	70.0	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	914	-	t_C
		PAL	-	64	-	us
		PAL	-	914	-	t_C
IHS display period	t_{HD}	NTSC	-	50.0	-	us
		NTSC	-	720	-	t_C
		PAL	-	50.4	-	us
		PAL	-	720	-	t_C
IHS pulse width	t_{HP}		5	63	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	720	-	t_C
IHS-IDEN time	t_{HE}	75	-	194	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 147 th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	5	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	22	-	t_{CPH}
OEV pulse width		t_{OEV}	-	20	-	t_{CPH}
CKV pulse width		t_{CKV}	-	35	-	t_{CPH}
IHS-OEH time		t_1	-	22	-	t_{CPH}
IHS -CKV time		t_2	-	13	-	t_{CPH}
IHS -OEV time		t_3	-	5	-	t_{CPH}
STV setup time		t_{SUV}	-	9	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.

(2) CPH1~3.

7.2.6 960 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	52	-	ns
		PAL	-	52.3	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1222	-	t_C
		PAL	-	64	-	us
		PAL	-	1222	-	t_C
IHS display period	t_{HD}	NTSC	-	49.9	-	us
		NTSC	-	960	-	t_C
		PAL	-	50.2	-	us
		PAL	-	960	-	t_C
IHS pulse width	t_{HP}		5	84	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	960	-	t_C
IHS-IDEN time	t_{HE}	162	-	262	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 243 th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	13	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	26	-	t_{CPH}
OEV pulse width		t_{OEV}	-	21	-	t_{CPH}
CKV pulse width		t_{CKV}	-	51	-	t_{CPH}
IHS-OEH time		t_1	-	42	-	t_{CPH}
IHS -CKV time		t_2	-	30	-	t_{CPH}
IHS -OEV time		t_3	-	12	-	t_{CPH}
STV setup time		t_{SUV}	-	15	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.2.7 1200 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	42.4	-	ns
		PAL	-	42.7	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1497	-	t_C
		PAL	-	64	-	us
		PAL	-	1497	-	t_C
IHS display period	t_{HD}	NTSC	-	50.9	-	us
		NTSC	-	1200	-	t_C
		PAL	-	51.2	-	us
		PAL	-	1200	-	t_C
IHS pulse width	t_{HP}		5	101	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	1200	-	t_C
IHS-IDEN time	t_{HE}	231	-	297	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 243 th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	15	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	16	-	t_{CPH}
OEV pulse width		t_{OEV}	-	25	-	t_{CPH}
CKV pulse width		t_{CKV}	-	65	-	t_{CPH}
IHS-OEH time		t_1	-	50	-	t_{CPH}
IHS -CKV time		t_2	-	39	-	t_{CPH}
IHS -OEV time		t_3	-	15	-	t_{CPH}
STV setup time		t_{SUV}	-	15	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

7.2.8 1440 × 234 resolution mode

a. Input signal characteristics

PARAMETER	Symbol		Min.	Typ.	Max.	Unit.
IDCLK period	t_C	NTSC	-	34.7	-	ns
		PAL	-	34.9	-	ns
IDCLK high time	t_{Ch}		-	-	-	ns
IDCLK low time	t_{Cl}		-	-	-	ns
IHS period	t_H	NTSC	-	63.5	-	us
		NTSC	-	1830	-	t_C
		PAL	-	64	-	us
		PAL	-	1830	-	t_C
IHS display period	t_{HD}	NTSC	-	49.9	-	us
		NTSC	-	1440	-	t_C
		PAL	-	50.2	-	us
		PAL	-	1440	-	t_C
IHS pulse width	t_{HP}		5	126	-	t_C
IVS period	t_V	NTSC	-	16.6	-	ms
		NTSC	-	262	-	t_H
		PAL	-	20	-	ms
		PAL	-	312	-	t_H
IVS display period	t_{VD}	NTSC	-	14.83	-	ms
		NTSC	-	234	-	t_H
		PAL	-	17.47	-	ms
		PAL	-	273	-	t_H
IVS pulse width	t_{VP}		3	-	-	t_H
IDCLK-DI0~DI7 time	t_{DS}		10	-	-	ns
DI0~DI7-IDCLK time	t_{DH}		10	-	-	ns
DI0~DI7 rise time	t_{Drf}		-	-	10	ns
DI0~DI7 fall time						

b. Horizontal display position

b-1. IDEN enable mode

The interval between IDEN rising edge and STHL(R) rising edge is fixed at 3-IDCLK, therefore the display position is fixed.

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
IDEN pulse width	t_{EP}	-	1440	-	t_C
IHS-IDEN time	t_{HE}	159	-	391	t_C

b-2. IDEN disable mode (IDEN = "L")

The display starts from 313 th clk from the IHS falling edge.

c. Vertical display position

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Vertical display position	t_{VS}	-	18	-	t_H
			27		t_H

d. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_C
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	t_{CPH}/3	-	ns
STH setup time		t_{SUH}	-	t_{CPH}/2	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
OEH pulse width		t_{OEH}	-	10	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	50	-	t_{CPH}
OEV pulse width		t_{OEV}	-	40	-	t_{CPH}
CKV pulse width		t_{CKV}	-	71	-	t_{CPH}
IHS-OEH time		t_1	-	44	-	t_{CPH}
IHS -CKV time		t_2	-	25	-	t_{CPH}
IHS -OEV time		t_3	-	10	-	t_{CPH}
STV setup time		t_{SUV}	-	18	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
IVS-STVD time(UDC='L')	NTSC	t_{VS1}	-	16	-	t_H
	PAL	t_{VS1}	-	25	-	t_H
IVS-STVU time(UDC='H')	NTSC	t_{VS2}	-	16	-	t_H
	PAL	t_{VS2}	-	25	-	t_H
OEH-STV time		t_{OES}	-	2	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3.

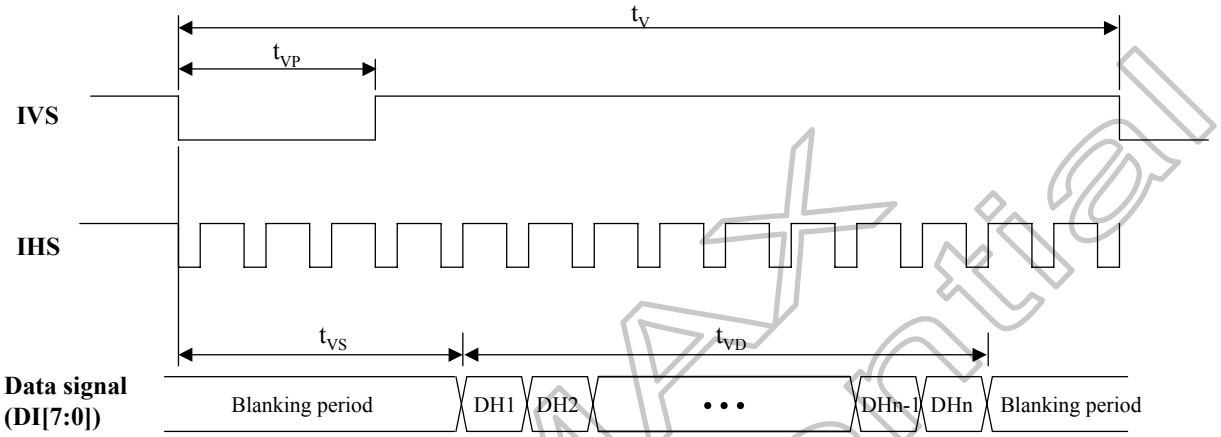
8. Analog video signal characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
Video signal amplitude (VR, VG, VB)	V_{IAC}(1)	-	3.98	-	V
	V_{IDC}(1)	-	2.5	-	V

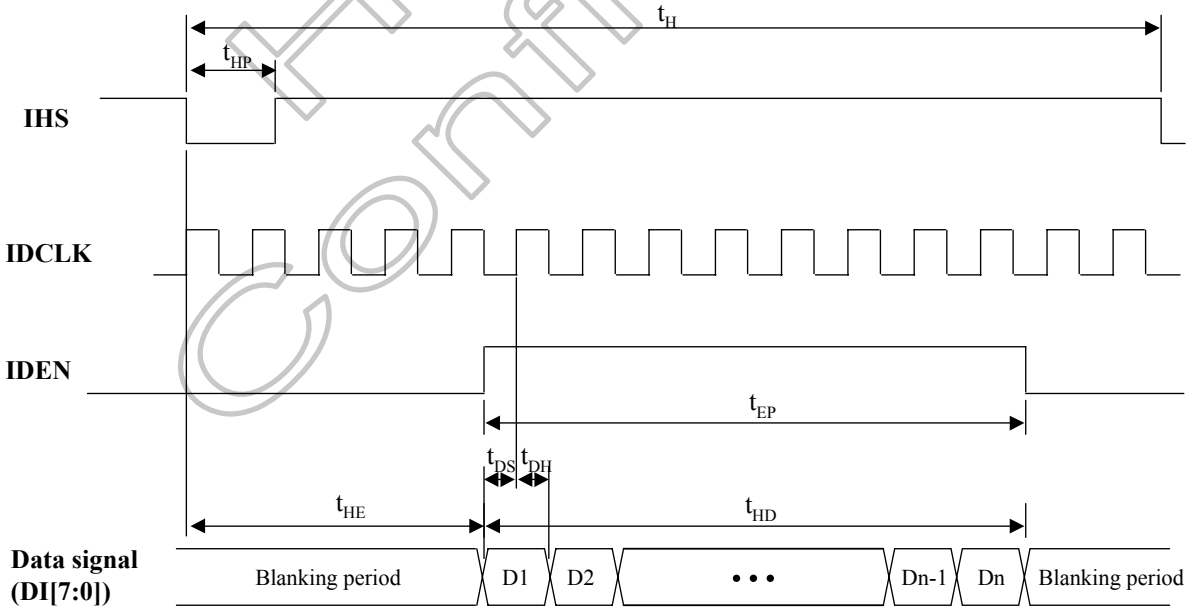
Note: (1) Refer to 9.8 for the related waveform

9. Waveform

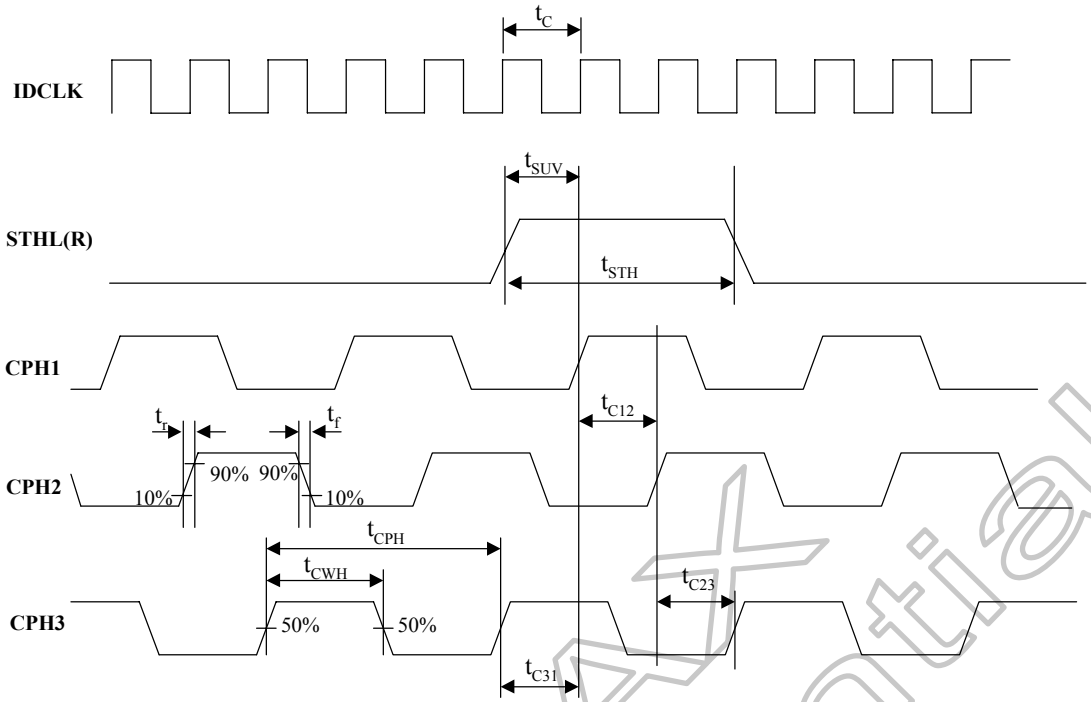
9.1 Input vertical timing



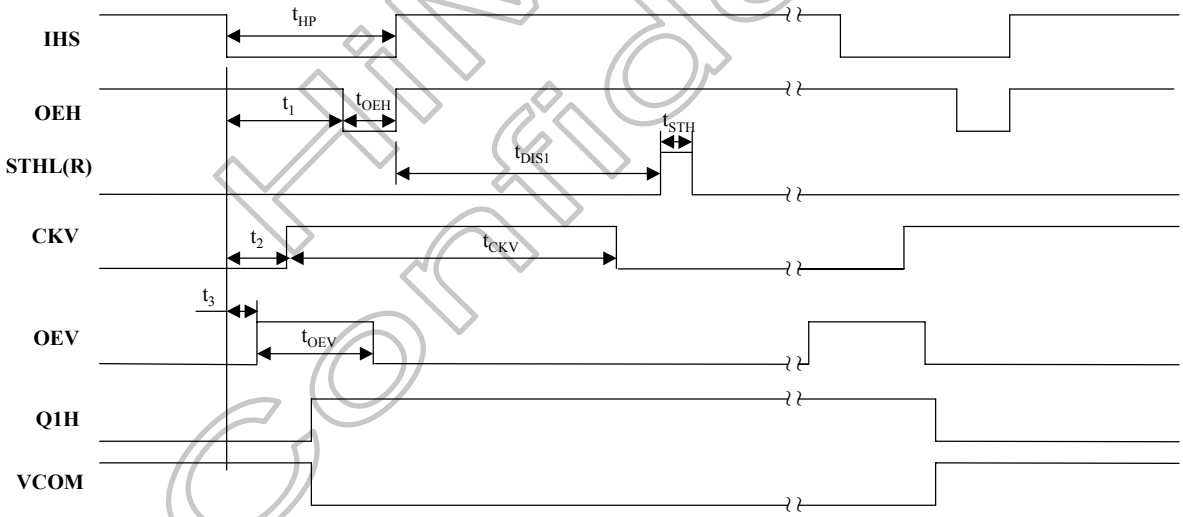
9.2 Input horizontal timing



9.3 IDCLK, STHL(R) and CPH1~3 timing waveform

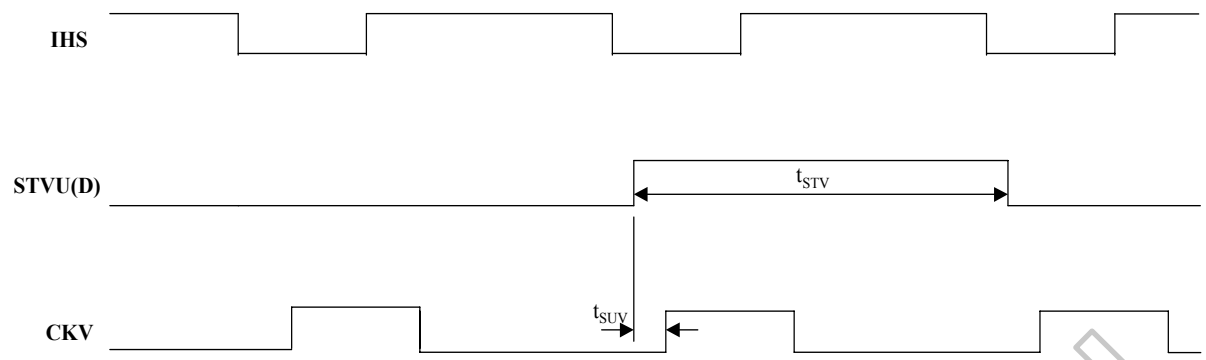


9.4 IHS and horizontal control timing waveform

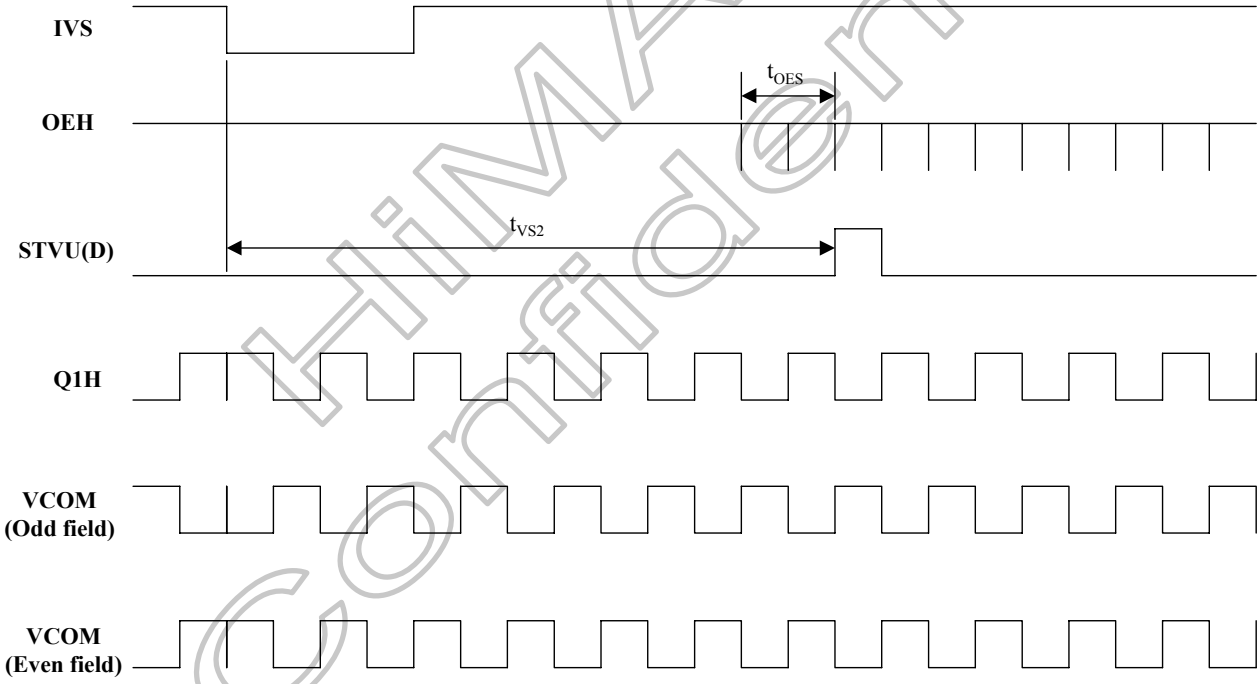


Note: In 960 x 234, 1152 x 234, 1200 x 234 and 1440 x 234 resolution mode, Q1H always keeps low.

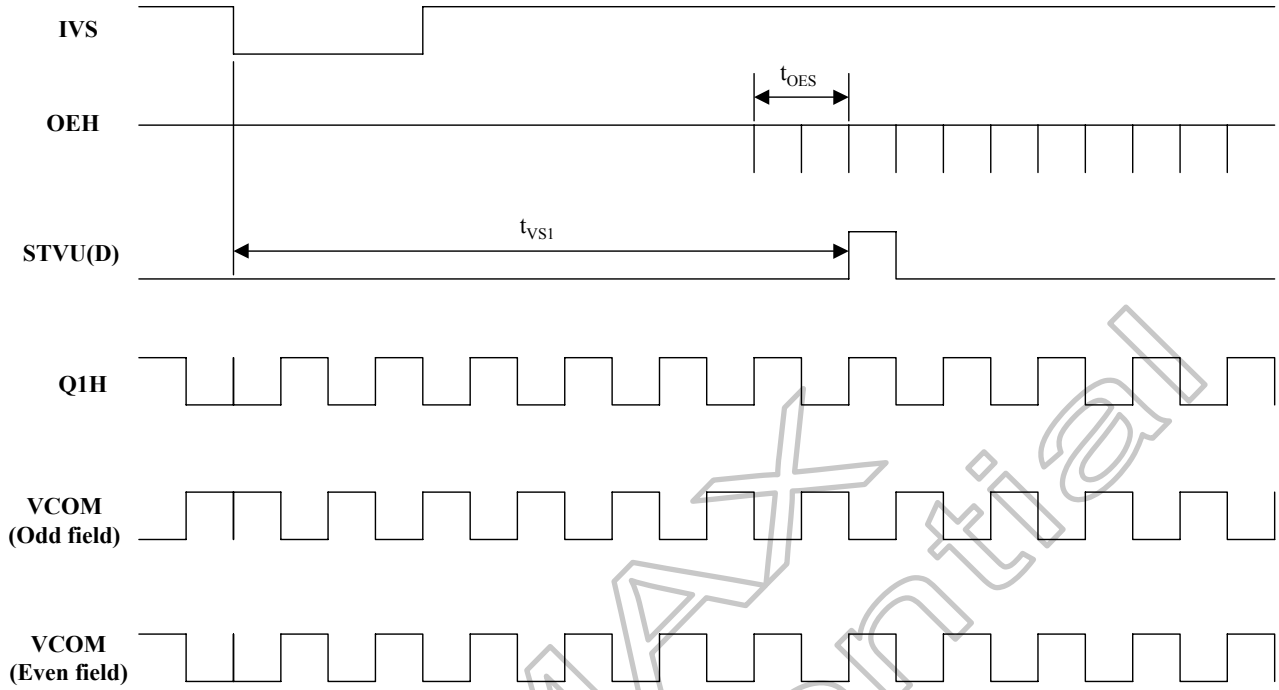
9.5 IHS and vertical shift clock timing waveform



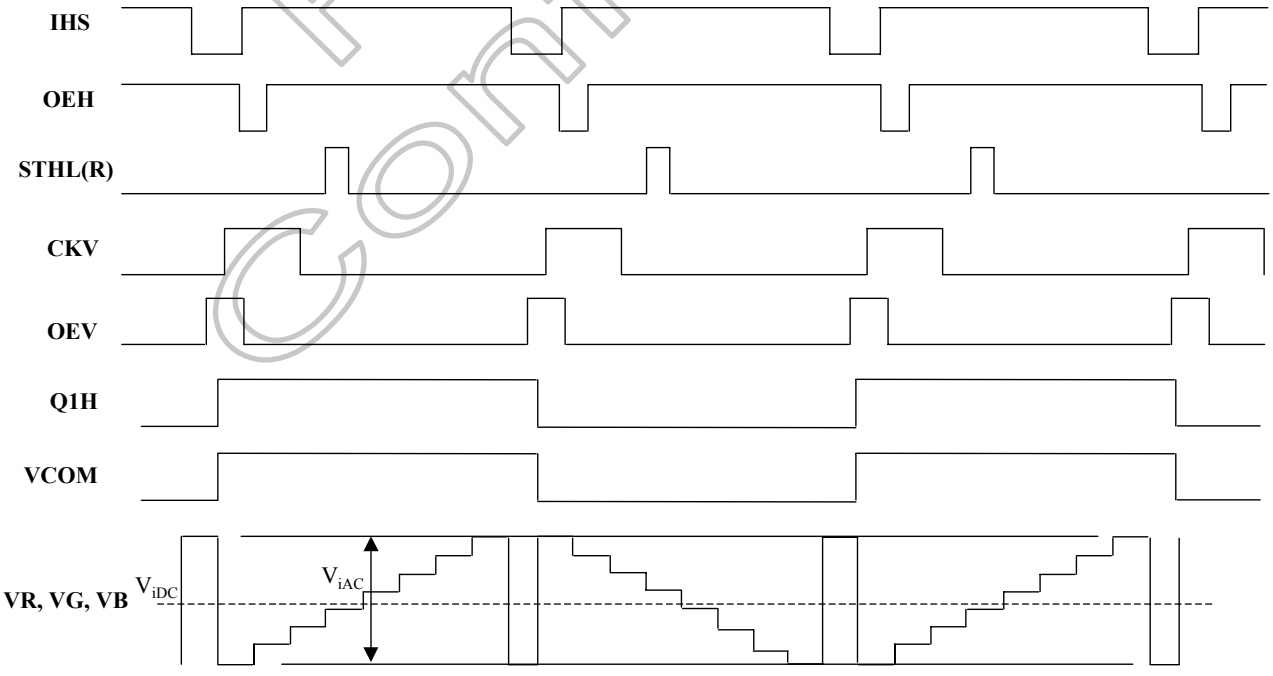
9.6 IHS and vertical control timing waveform (for the case of UDC="H")



9.7 IHS and vertical control timing waveform (for the case of UDC="L")



9.8 Analog video signal amplitude (VR, VG, VB)



10. Package Outline Dimension

10.1 64-pin LQFP

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BCD.

TITLE: 64LD LQFP (10x10x1.4mm) PACKAGE OUTLINE -Cu L/F FOOTPRINT 2.0mm	
L/F MATERIAL: C7025 1/2H	

10.2 48-pin LQFP

Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BBC.

TITLE: 48LD LQFP (7x7x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm	
L/F MATERIAL: C7025 1/2H	

11. Ordering Information

Part NO.	Package
HX8802ALB	64pin LQFP
HX8802ALC	64pin LQFP, pin64 no bonding
HX8802ALD	48pin LQFP
HX8802ALE	48pin LQFP, pin1 no bonding
HX8802BLB	64pin LQFP
HX8802BLC	64pin LQFP, 64 no bonding
HX8802BLD	48pin LQFP
HX8802BLE	48pin LQFP, pin1 no bonding

12. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2001/09/21	New setup
02	2002/03/01	1. Pin no. 2: STHR. 2. Pin no. 3: STHL. 3. Pin no. 31: LRC, “H” - normal scan. “L” - reverse scan. 4. Pin no. 10 : PNCS. 5. Pin no. 21 : PALSDS. 6. Add 48 pins pin description. 7. Support 16 resolution mode.
03	2002/05/28	1. Modify t_{dis1} and t_2 parameters. 2. Modify STHR(L) start position in IDEN disable mode.
04	2002/8/01	1.Modify HX8802 to HX8802A. 2.Add ordering information. 3. Update pin assignment.
05	2002/9/12	1.Update ordering information.
06	2004/03/19	1. Update Operating temperature. 2. Update Input/Output capacitance. 3. Modify Input pull up/down resistance. 4. Remove Schmitt input high/low voltage.