DATA SHEET

(DOC No. HX8819AFA/AFB/AFC--DS)

HX8819AFA/AFB/AFC

TFT-LCD TCON

Preliminary version 01 December, 2004

Himax Technologies, Inc.
http://www.himax.com.tw

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Preliminary Version 01

December, 2004

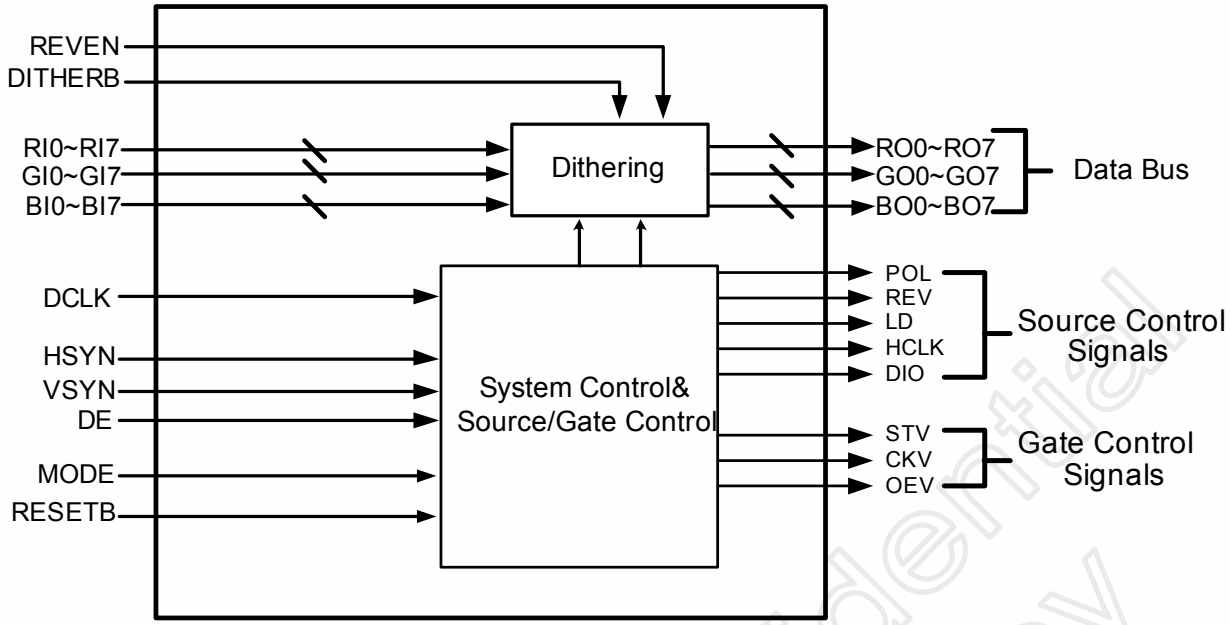
1. General Description

The HX8819AFA/ HX8819AFB/ HX8819AFC are TFT-LCD timing controller with built-in dithering function. They provide horizontal and vertical control timing to TFT-LCD source and gate drivers. This controller performs polarity inverted function to convert 8-bit digital RGB data into 6-bit digital RGB data for TFT-LCD panel.

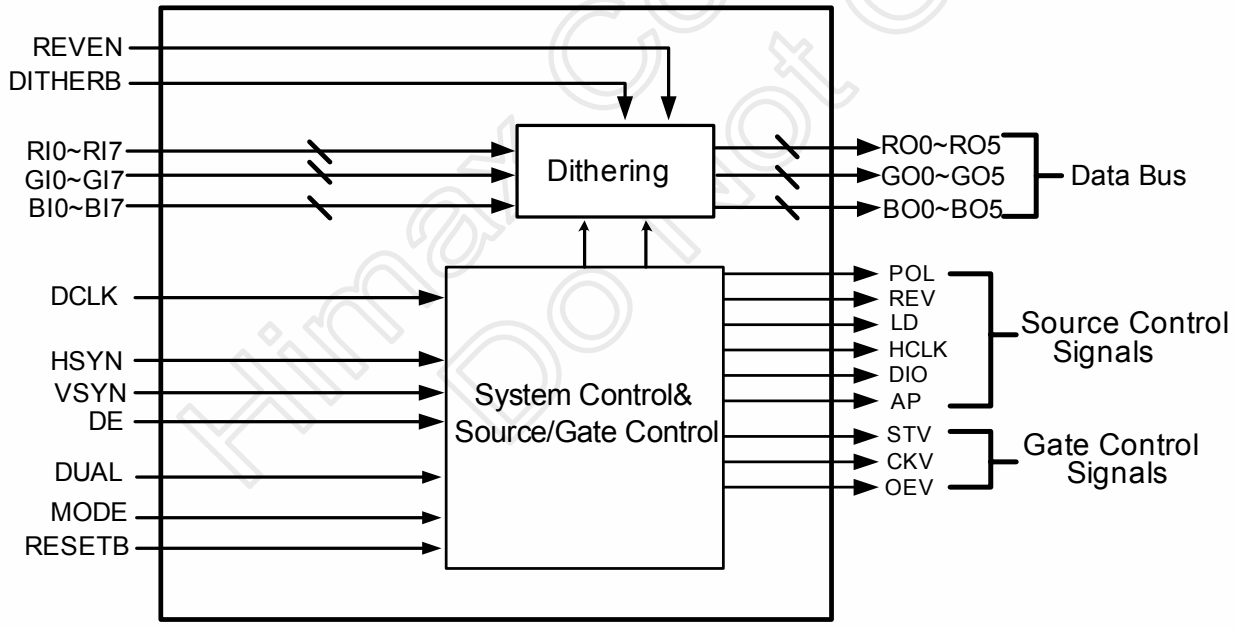
2. Features

- Support display resolution WVGA 800 x 480(HX8819AFA), WVGA 800 x 480 (HX8819AFB) and VGA 640 x 480 (HX8819AFC) modes depend on different bonding option.
- Master clock frequency: 40 MHz max.
- 8-bit digital RGB input signals
- Supporting both Sync(Hs/Vs) mode and Data enable (DE) mode
- Built-in dithering function.
- Built-in polarity inverted function.
- Provide source and gate drivers control timing.
- Support dual clock function (HX8819AFB and HX8819AFC)
- Single supply voltage: +3.3V
- 64 TQFP

3. Block Diagram

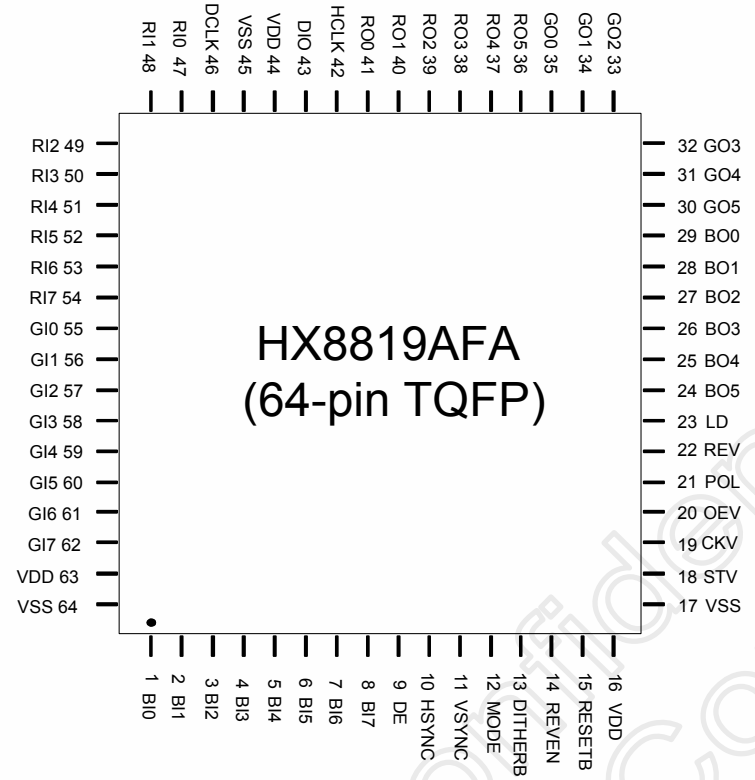


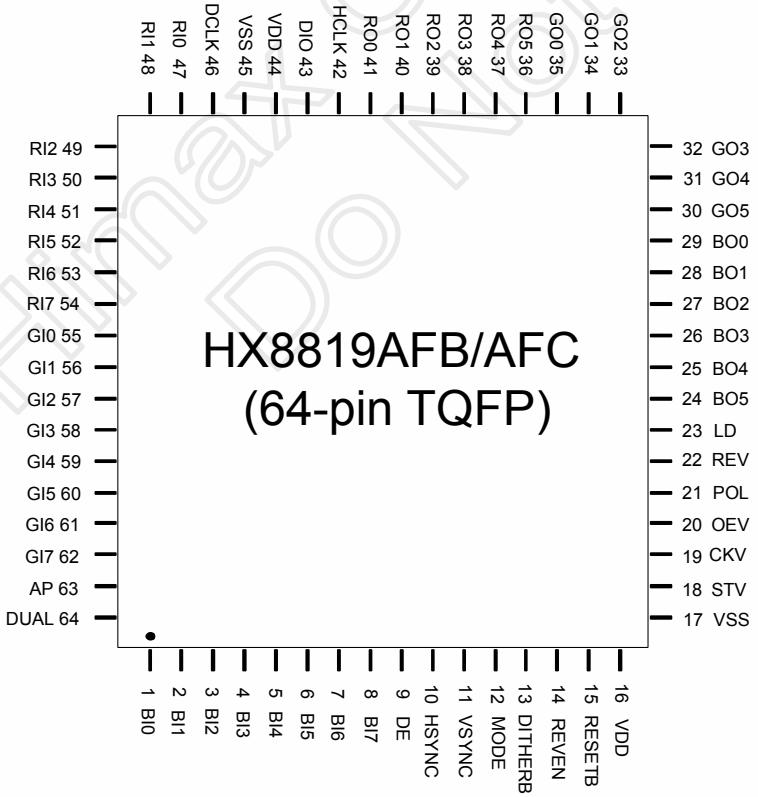
HX8819AFA



HX8819AFB/AFC

4. Pin Assignment





5. Pin Description

Pin no.	Symbol	I/O	Description
1	BI0	I	Blue data input, bit0(LSB)(default pull-down).
2	BI1	I	Blue data input, bit1(default pull-down).
3	BI2	I	Blue data input, bit2.
4	BI3	I	Blue data input, bit3.
5	BI4	I	Blue data input, bit4.
6	BI5	I	Blue data input, bit5.
7	BI6	I	Blue data input, bit6.
8	BI7	I	Blue data input, bit7(MSB).
9	DE/TEST(1)	I	MODE =1 : Data enable signal MODE =0 : Test function
10	HSYNC /TEST(2)	I	MODE=0 : Negative polarity horizontal sync input MODE=1 : Test function
11	VSYNC	I	Negative polarity vertical sync input
12	MODE	I	DE / SYNC mode select, normally pulled high. 1: DE mode 0: SYNC mode
13	DITHERB	I	Dithering disable, normally pulled high. 1: disable 0: enable
14	REVEN	I	Data invert enable, normally pulled high. 1: enable 0: disable
15	RESETB	I	Active low reset pin.
16	VDD	I	Power supply voltage.
17	VSS	I	Power supply ground.
18	STV	O	Gate driver start pulse.
19	CKV	O	Gate driver shift clock.
20	OEV	O	Gate driver output disable.
21	POL	O	Source driver polarity select.
22	REV	O	Source driver data reverse control.
23	LD	O	Source driver latch pulse and output enable.
24	BO5	O	Blue data output, bit5 (MSB).
25	BO4	O	Blue data output, bit4.
26	BO3	O	Blue data output, bit3.
27	BO2	O	Blue data output, bit2.
28	BO1	O	Blue data output, bit1.
29	BO0	O	Blue data output, bit0 (LSB).
30	GO5	O	Green data output, bit5 (MSB).
31	GO4	O	Green data output, bit4.
32	GO3	O	Green data output, bit3.
33	GO2	O	Green data output, bit2.
34	GO1	O	Green data output, bit1.
35	GO0	O	Green data output, bit0 (LSB).
36	RO5	O	Red data output, bit5 (MSB).
37	RO4	O	Red data output, bit4.
38	RO3	O	Red data output, bit3.

Pin no.	Symbol	I/O	Description
39	RO2	O	Red data output, bit2.
40	RO1	O	Red data output, bit1.
41	RO0	O	Red data output, bit0 (LSB).
42	HCLK	O	Source driver shift clock.
43	DIO	O	Source driver start pulse.
44	VDD	I	Power supply voltage.
45	VSS	I	Power supply ground..
46	DCLK	I	Clock signal; latch data at falling edge.
47	RI0	I	Red data input, bit0(LSB)(default pull-down).
48	RI1	I	Red data input, bit1(default pull-down).
49	RI2	I	Red data input, bit2.
50	RI3	I	Red data input, bit3.
51	RI4	I	Red data input, bit4.
52	RI5	I	Red data input, bit5.
53	RI6	I	Red data input, bit6.
54	RI7	I	Red data input, bit7(MSB).
55	GI0	I	Green data input, bit0(LSB)(default pull-down).
56	GI1	I	Green data input, bit1(default pull-down).
57	GI2	I	Green data input, bit2.
58	GI3	I	Green data input, bit3.
59	GI4	I	Green data input, bit4.
60	GI5	I	Green data input, bit5.
61	GI6	I	Green data input, bit6.
62	GI7	I	Green data input, bit7(MSB).
63	AP/	O	OP amp bias current ON/OFF control input AP="H", OP amp is on normal operation AP="L", OP amp is on standby mode
	VDD(3)	I	Power supply voltage
64	DUAL/	I	DUAL="0", latch data on the rising edge of CLK. DUAL="1", latch data on rising and falling edge of CLK.
	VSS(4)	I	Power supply ground

Note: (1) When Sync mode, The DE pin is TEST pin, and it should be connected VSS.
(2) When DE mode, The HSYNC pin is TEST pin, it should be connected VDD.
(3) In HX8819AFA the AP pin is the VDD pin.
(4) In HX8819AFA the DUAL pin is the VSS pin.

6. DC Characteristics

HX8819AFA/ HX8819AFB/HX8819AFC

6.1 Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Power supply	V_{DD}	2.5 to 3.6	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 85	ºC

6.2 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply	V_{DD}	2.7	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating temperature	T_{OPR}	0	-	85	ºC

6.3 Electrical Characteristics for 3.3V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	µA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	µA
Tri-state leakage current	I_{OZ}	-	-10	-	10	µA
Logic input low voltage	V_{IL} (1)	CMOS	-	-	$0.3V_{DD}$	V
Logic input high voltage	V_{IH} (1)	CMOS	$0.7V_{DD}$	-	-	V
Output low voltage	V_{OL} (2)	I_{OL}=4mA	-	-	$0.2V_{DD}$	V
Output high voltage	V_{OH} (2)	I_{OH}=-4mA	$0.8V_{DD}$	-	-	V
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{DD}	85	126	180	kΩ

Note: (1) IHS, IVS, IDEN, IDCLK, UDC, LRC, DI0~DI7.
(2) STV, CKV, POL, REV, LD, DIO, HCLK, RO0~RO7, GO0~GO7, BO0~BO7.

7. AC Characteristics

- **HX8819AFA/ HX8819AFB**

7.1 SYNC mode input signal characteristics

RESOLUTION :(800x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Clock Period	t_{CLK}	50.0	30.0	25.0	ns
Clock Frequency	f_{CLK}	20	33.3	40	MHz
Clock Low Level Width	t_{WCL}	8	-	-	ns
Clock High Level Width	t_{WCH}	8	-	-	ns
Clock Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
HSYNC Period	t_{HP}	895	928	990	t_{CLK}
HYNC Pulse Width	t_{HW}	48	48	48	t_{CLK}
HYNC Back Porch	t_{HBP}	40	40	40	t_{CLK}
HYNC Width+Back Porch	$t_{HW} + t_{HBP}$	88	88	88	t_{CLK}
Horizontal Vaild Data Width	t_{HV}	800	800	800	t_{CLK}
HYNC Front Porch	t_{HFP}	7	40	102	t_{CLK}
VSYNC Period	t_{VP}	513	525	610	t_{HP}
VYNC Pulse Width	t_{VW}	3	3	3	t_{HP}
VSYNC Back Porch	t_{VBP}	29	29	29	t_{HP}
Vertical Valid Data Width	t_{W}	480	480	480	t_{HP}
VSYNC Front Porch	t_{VFP}	1	13	98	t_{HP}
Data Setup Time	t_{DS}	5	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns

7.2 SYNC mode output signal characteristics

RESOLUTION :(800x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HCLK frequency	H_{CLK}	20	33.3	40	MHz
DIO pulse width	t_{DIOW}	-	1	-	H_{CLK}
LD pulse width	t_{LDW}	-	4	-	H_{CLK}
OEV pulse width	t_{OEV}	-	66	-	H_{CLK}
CKV pulse width	t_{CKV}	-	474	-	H_{CLK}
POL pulse width	t_{POL}	-	928	-	H_{CLK}
STV pulse width	t_{STV}	-	1281	-	H_{CLK}
Time that CKV to LD	t_{GS}	-	1	-	H_{CLK}
Time that POL to LD	t_{PL}	-	453	-	H_{CLK}
Time that LD to DIO	t_{LDO}	-	120	-	H_{CLK}

7.3 DE mode input signal characteristics

RESOLUTION :(800x480)

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Period	t_{CLK}	50.0	37.0	25.0	ns
	Frequency	f_{CLK}	20.0	27.0	40.0	MHz
	Low Level Width	t_{WCL}	8	-	-	ns
	High Level Width	t_{WCH}	8	-	-	ns
	Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
	Duty(1)	-	0.45	0.50	0.55	-
DE (Data Enable)	Setup Time	t_{DES}	5	-	-	ns
	Hold Time	t_{DEH}	10	-	-	ns
	Rise, Fall Time	t_{DEr}, t_{DEf}	-	-	16	ns
	Horizontal Period	t_{HP}	895	900	990	t_{CLK}
	Horizontal Valid	t_{HV}	800	800	800	t_{CLK}
	Horizontal Blank	t_{HBK}	95	100	190	t_{CLK}
	Vertical Period	t_{VP}	513	513	610	t_{HP}
	Vertical Valid	t_W	480	480	480	t_{HP}
	Vertical Blank	t_{VBK}	33	33	70	t_{HP}
Data	Setup Time	t_{DS}	5	-	-	ns
	Hold Time	t_{DH}	10	-	-	ns
	Rise, Fall Time	t_{Dr},t_{Df}	-	-	3	ns

Note: (1) t_{CLKL}/ t_{CLK}.

7.4 DE mode output signal characteristics

RESOLUTION :(800x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HCLK frequency	H_{CLK}	25	27	35	MHz
DIO pulse width	t_{DIOW}	-	1	-	H_{CLK}
LD pulse width	t_{LDW}	-	4	-	H_{CLK}
OEV pulse width	t_{OEV}	-	66	-	H_{CLK}
CKV pulse width	t_{CKV}	-	446	-	H_{CLK}
POL pulse width	t_{POL}	-	900	-	H_{CLK}
STV pulse width	t_{STV}	-	1249	-	H_{CLK}
Time that CKV to LD	t_{GS}	-	1	-	H_{CLK}
Time that POL to LD	t_{PL}	-	453	-	H_{CLK}
Time that LD to DIO	t_{LDO}	-	92	-	H_{CLK}

- **HX8819AFC**

7.5 SYNC mode input signal characteristics

RESOLUTION :(640x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Clock Period	t_{CLK}	-	40.0	25.0	ns
Clock Frequency	f_{CLK}	-	25	40	MHz
Clock Low Level Width	t_{WCL}	8	-	-	ns
Clock High Level Width	t_{WCH}	8	-	-	ns
Clock Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
HSYNC Period	t_{HP}	788	800	890	t_{CLK}
HYNC Pulse Width	t_{HW}	96	96	96	t_{CLK}
HYNC Back Porch	t_{HBP}	48	48	48	t_{CLK}
HYNC Width+Back Porch	t_{HW} + t_{HBP}	144	144	144	t_{CLK}
Horizontal Vaild Data Width	t_{HV}	640	640	640	t_{CLK}
HYNC Front Porch	t_{HFP}	4	16	106	t_{CLK}
VSYNC Period	t_{VP}	516	525	561	t_{HP}
VYNC Pulse Width	t_{VW}	2	2	2	t_{HP}
VSYNC Back Porch	t_{VBP}	33	33	33	t_{HP}
Vertical Valid data Width	t_{W}	480	480	480	t_{HP}
VSYNC Front Porch	t_{VFP}	1	10	46	t_{HP}
Data Setup Time	t_{DS}	5	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns

7.6 SYNC mode output signal characteristics

RESOLUTION :(640x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HCLK frequency	H_{CLK}	-	25	40	MHz
DIO pulse width	t_{DIOW}	-	1	-	H_{CLK}
LD pulse width	t_{LDW}	-	4	-	H_{CLK}
OEV pulse width	t_{OEV}	-	66	-	H_{CLK}
CKV pulse width	t_{CKV}	-	396	-	H_{CLK}
POL pulse width	t_{POL}	-	800	-	H_{CLK}
STV pulse width	t_{STV}	-	1047	-	H_{CLK}
Time that CKV to LD	t_{GS}	-	1	-	H_{CLK}
Time that POL to LD	t_{PL}	-	403	-	H_{CLK}
Time that LD to DIO	t_{LDO}	-	152	-	H_{CLK}

7.7 DE mode input signal characteristics

RESOLUTION :(640x480)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK	Period	t_{CLK}	-	40.0	25.0	ns
	Frequency	f_{CLK}	-	25	40	MHz
	Low Level Width	t_{WCL}	8	-	-	ns
	High Level Width	t_{WCH}	8	-	-	ns
	Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
	Duty(1)	-	0.45	0.50	0.55	-
DE (Data Enable)	Setup Time	t_{DES}	5	-	-	ns
	Hold Time	t_{DEH}	10	-	-	ns
	Rise, Fall Time	t_{DEr}, t_{DEf}	-	-	16	ns
	Horizontal Period	t_{HP}	788	800	890	t_{CLK}
	Horizontal Valid	t_{HV}	640	640	640	t_{CLK}
	Horizontal Blank	t_{HBK}	148	160	250	t_{CLK}
	Vertical Period	t_{VP}	516	525	561	t_{HP}
	Vertical Valid	t_W	480	480	480	t_{HP}
	Vertical Blank	t_{VBK}	36	45	81	t_{HP}
Data	Setup Time	t_{DS}	5	-	-	ns
	Hold Time	t_{DH}	10	-	-	ns
	Rise, Fall Time	t_{Dr},t_{Df}	-	-	3	ns

Note: (1) t_{CLKL}/ t_{CLK}.

7.8 DE mode output signal characteristics

RESOLUTION :(640x480)

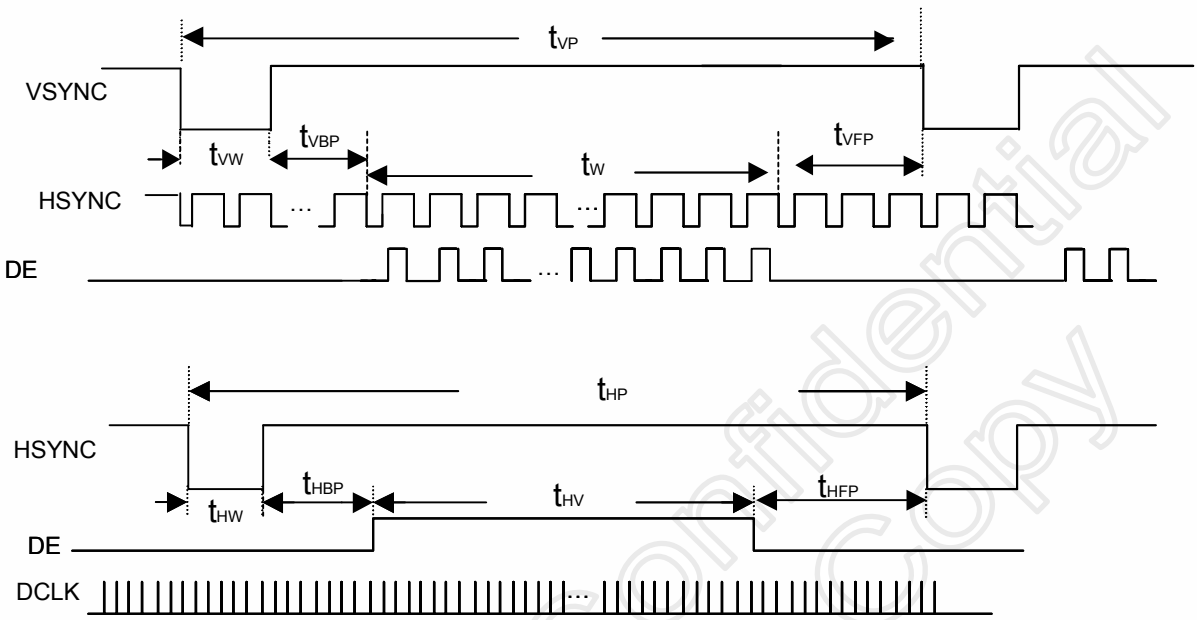
PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HCLK frequency	H_{CLK}	-	25	40	MHz
DIO pulse width	t_{DIOW}	-	1	-	H_{CLK}
LD pulse width	t_{LDW}	-	4	-	H_{CLK}
OEV pulse width	t_{OEV}	-	66	-	H_{CLK}
CKV pulse width	t_{CKV}	-	396	-	H_{CLK}
POL pulse width	t_{POL}	-	800	-	H_{CLK}
STV pulse width	t_{STV}	-	1039	-	H_{CLK}
Time that CKV to LD	t_{GS}	-	1	-	H_{CLK}
Time that POL to LD	t_{PL}	-	403	-	H_{CLK}
Time that LD to DIO	t_{LDO}	-	152	-	H_{CLK}

8. Waveform

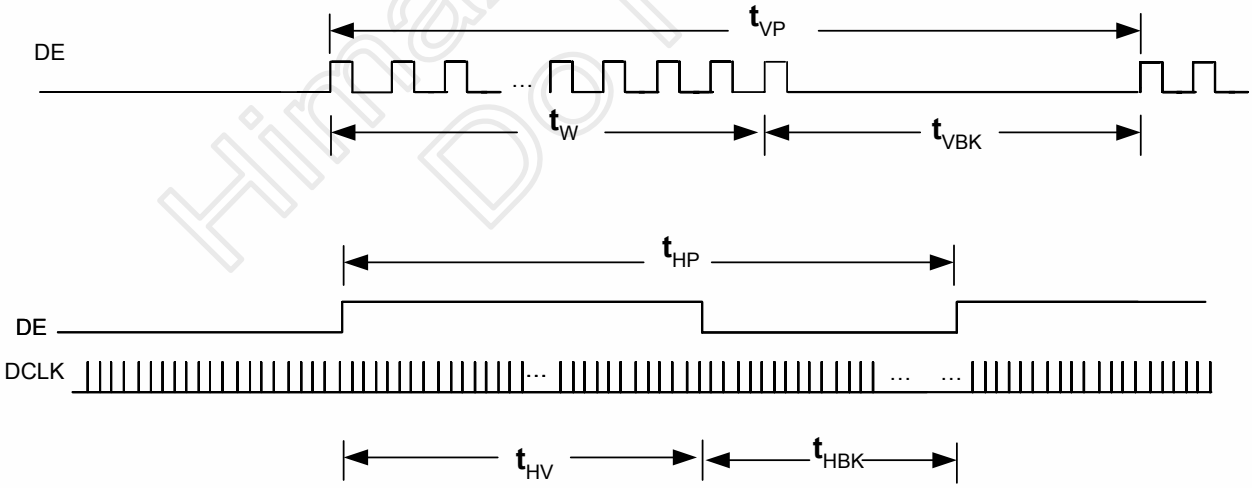
- **HX8819A/ HX8819AFB/HX8819AFC**

8.1 Input Signal Timing

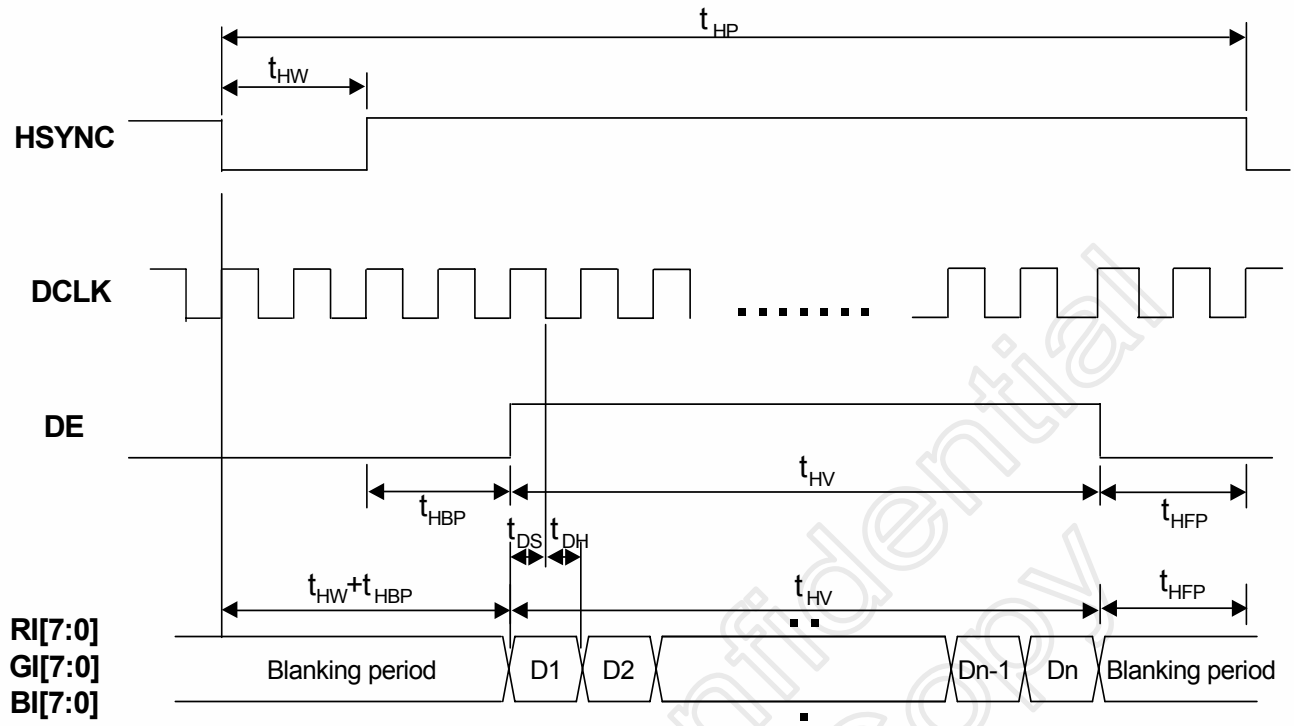
8.1.1 Sync. mode input timing



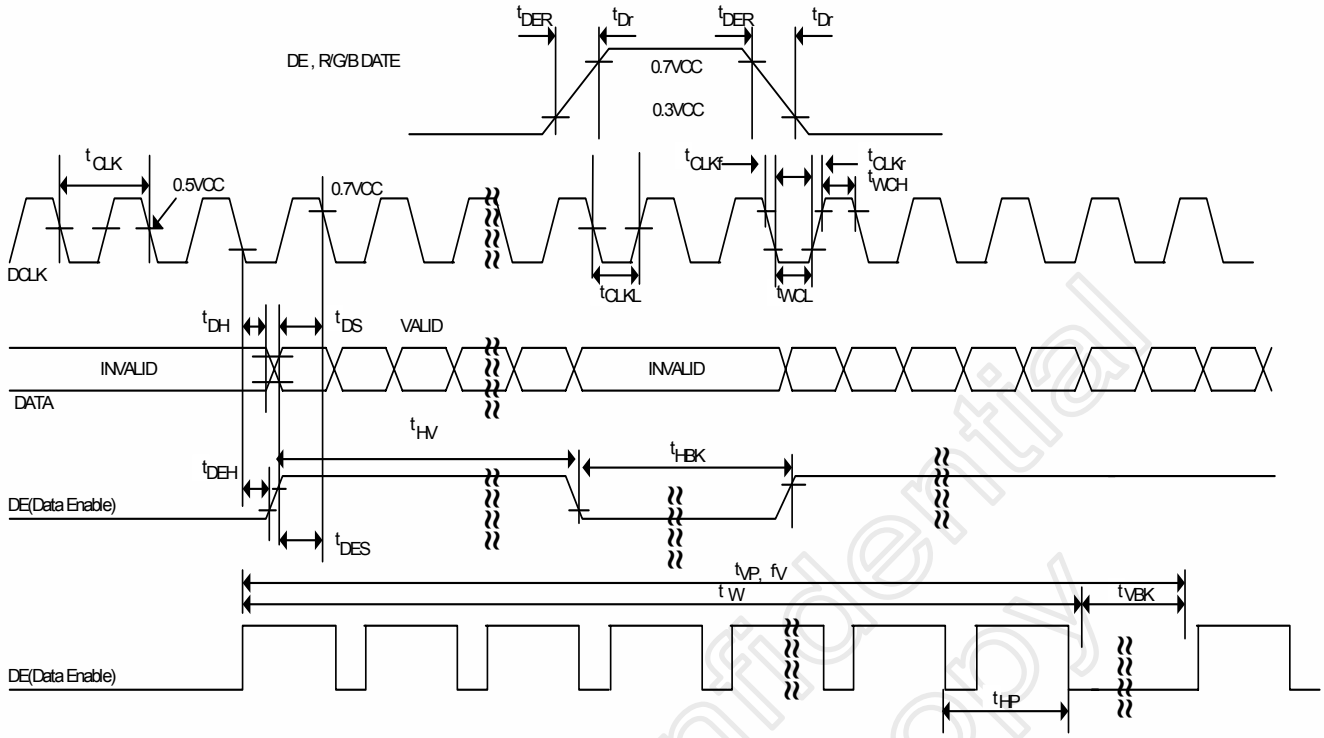
8.1.2 DE. mode input timing



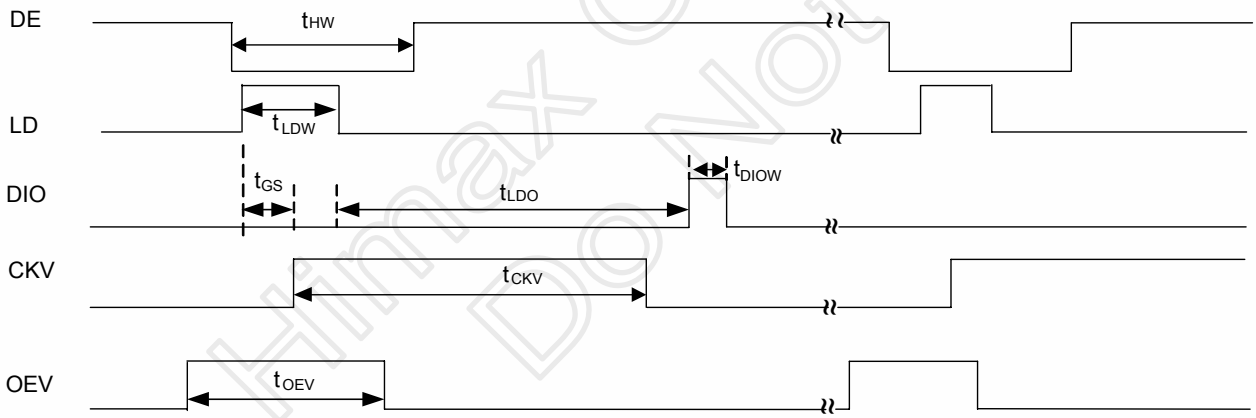
8.1.3 Input horizontal timing (Sync. mode && De mode)



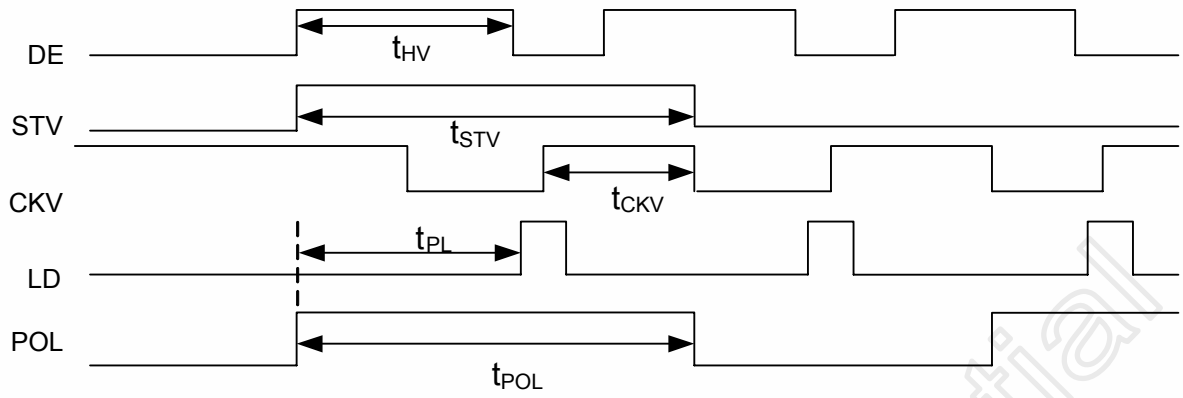
8.2 DE and RGB input data timing waveform



8.3 Output signal timing waveform (LD,DIO,CKV,OEV)



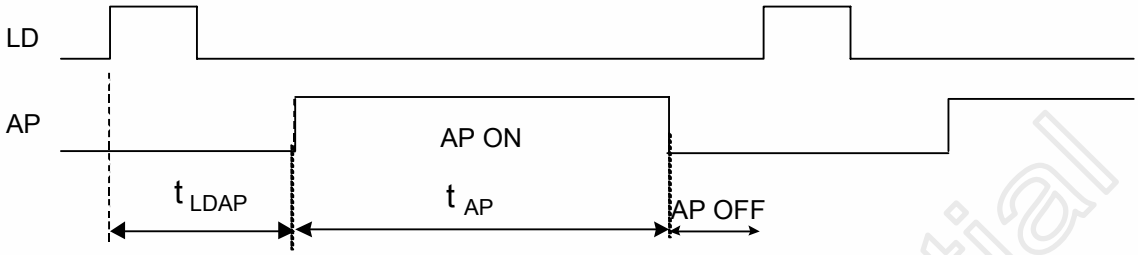
8.4 Output signal timing waveform (STV, CKV, LD, POL)



● **HX8819AFB/HX8819AFC**

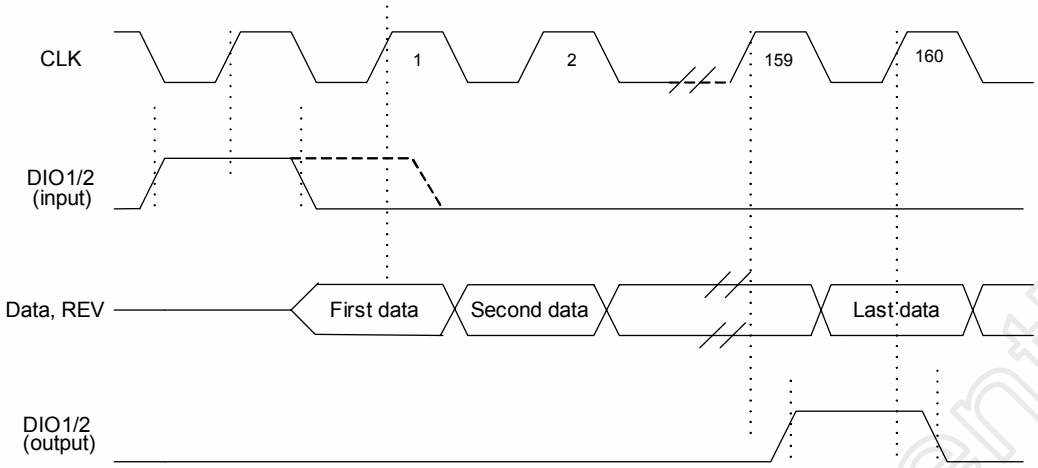
8.5 Relationship between LD and AP output waveform

AP=" H", source drive internal OP amp is on normal operation. In the other case, AP="L", OP amp is on standby mode for power saving.

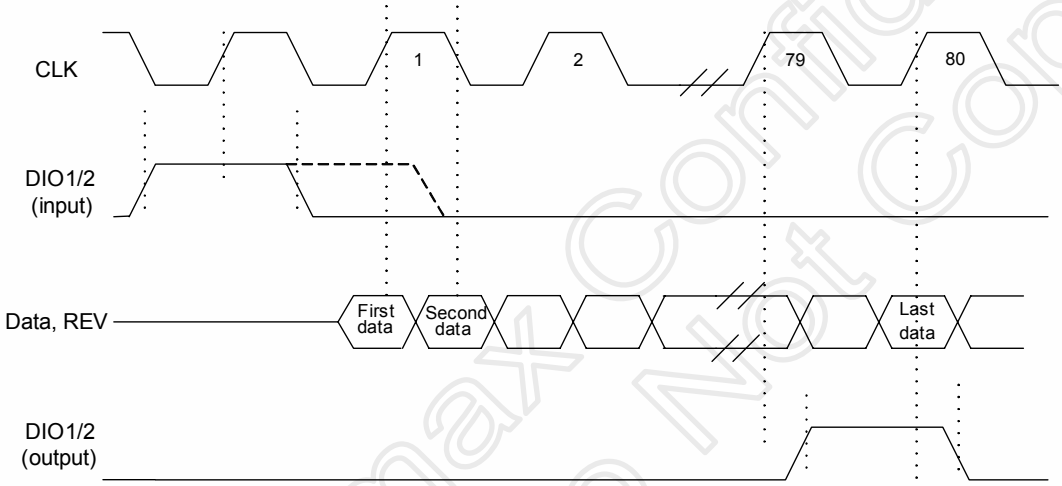


8.6 Dual clock function output waveform

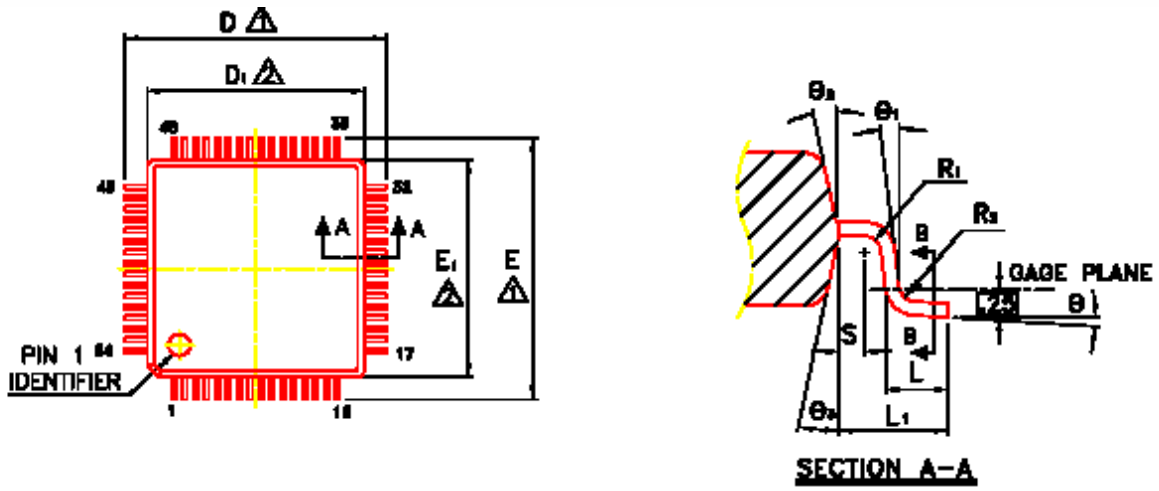
<< DUAL = ”0”>>



<< DUAL = ”1” >>



9. Package Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

10. Ordering Information

Part NO.	Package
HX8819AFA	64pin TQFP
HX8819AFB	64pin TQFP
HX8819AFC	64pin TQFP

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2004/12/30	New setup