DATA SHEET

(DOC No. HX8819AFAG/AFBG/AFCG--DS)

HX8819AFAG/AFBG /AFCG

AV TCON with RGB Input and Built-in Dithering Function

Version 04 September, 2006

Himax 奇景光電股份有限公司
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Date ： 2007.04.27
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Himax Technologies, Inc.
http://www.himax.com.tw

HX8819AFAG/AFBG/AFCG

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1. General Description

The HX8819AFAG/ HX8819AFBG/ HX8819AFCG are TFT-LCD timing controller with built-in dithering function. They provide horizontal and vertical control timing to TFT-LCD source and gate drivers. This controller performs polarity inverted function to convert 8-bit digital RGB data into 6-bit digital RGB data for TFT-LCD panel.

2. Features

- Supporting display resolution WVGA 800RGB x 480(HX8819AFAG/ HX8819AFBG) and VGA 640RGB x 480 (HX8819AFCG) modes depend on different bonding option.
- Master clock frequency: 40 MHz max.
- Supporting 24-bits (8-bits x3) digital parallel RGB input signals
- Supporting both Sync(Hs/Vs) mode and Data enable (DE) mode
- Built-in dithering function.
- Built-in polarity inverted function.
- Provide the control timing of the source drivers and the gate drivers.
- Support dual clock function (HX8819AFBG and HX8819AFCG)
- Single supply voltage: +3.3V
- 64 TQFP

3. Block Diagram

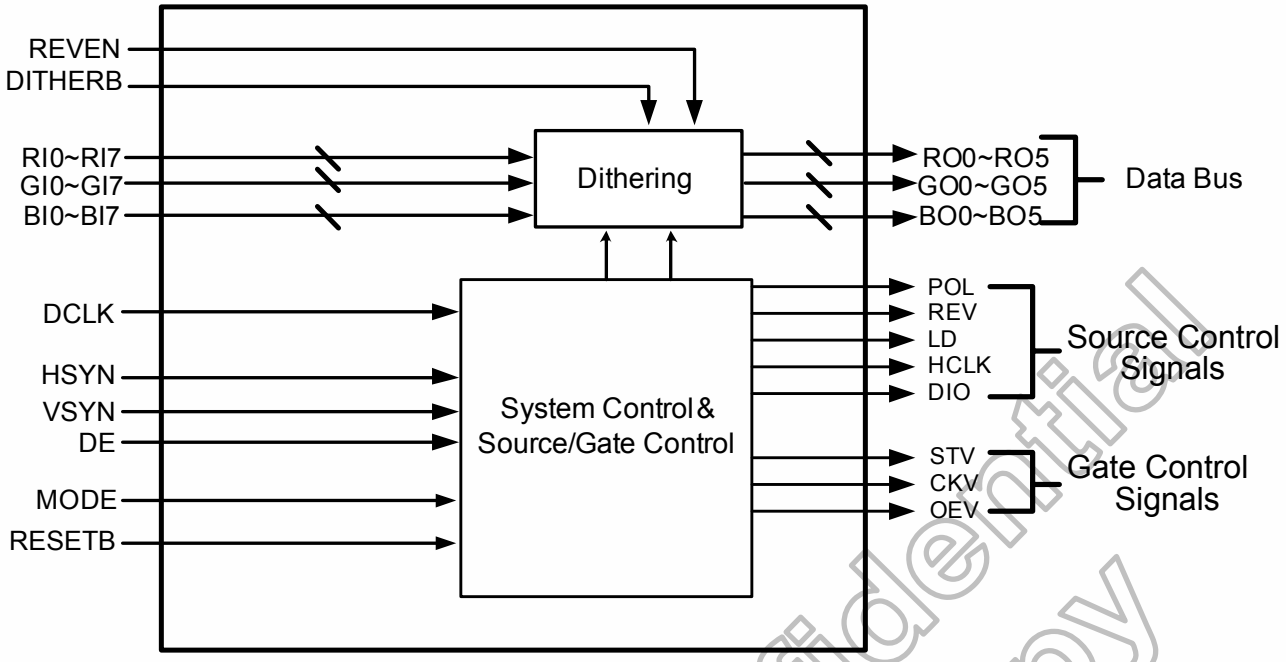


Figure 3. 1 HX8819AFAG block diagram

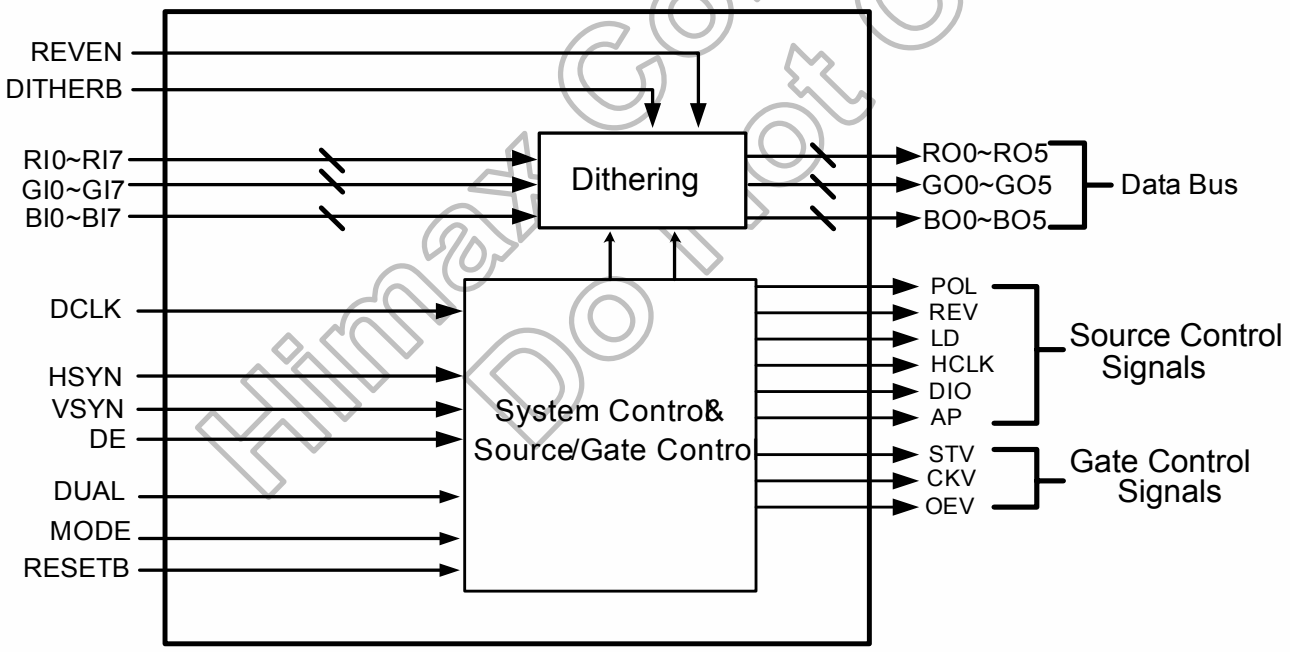


Figure 3. 2 HX8819AFBG/AFCG block diagram

4. Pin Assignment

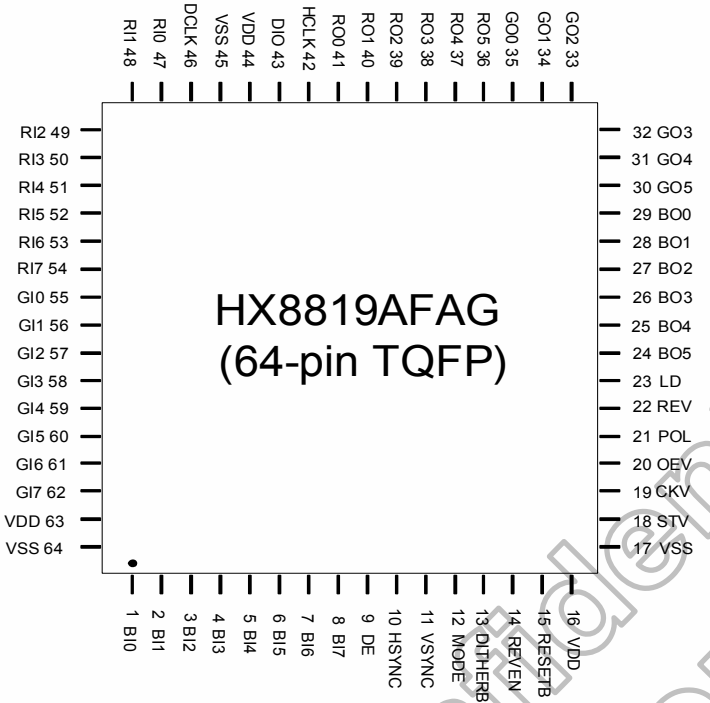


Figure 4. 1 HX8819AFAG pin assignment

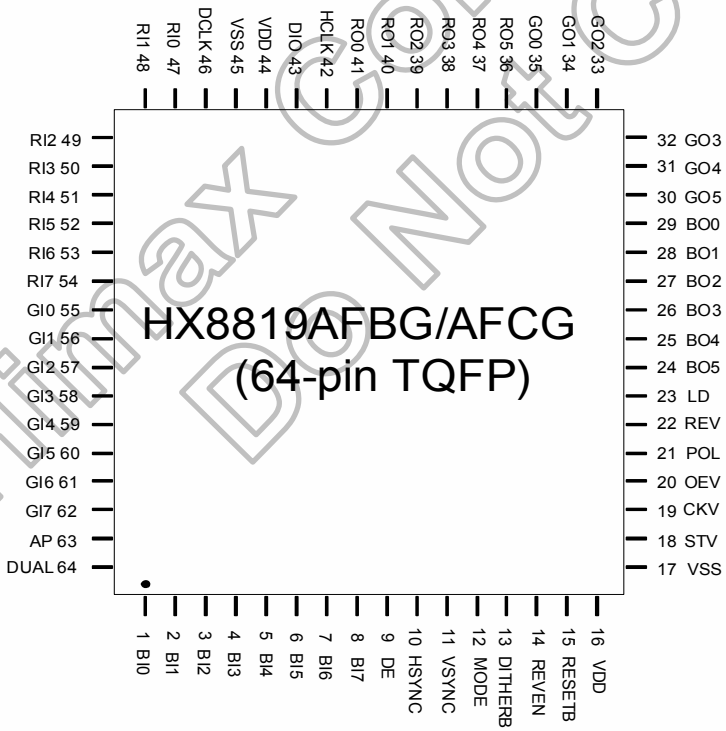


Figure 4. 2 HX8819AFBG/AFCG pin assignment

5. Pin Description

Pin no.	Symbol	I/O	Description
1	BI0	I	Blue data input, bit0(LSB)(default pull-down).
2	BI1	I	Blue data input, bit1(default pull-down).
3	BI2	I	Blue data input, bit2.
4	BI3	I	Blue data input, bit3.
5	BI4	I	Blue data input, bit4.
6	BI5	I	Blue data input, bit5.
7	BI6	I	Blue data input, bit6.
8	BI7	I	Blue data input, bit7(MSB).
9	DE/TEST(1)	I	MODE =1 : Data enable signal MODE =0 : Test function
10	HSYNC /TEST(2)	I	MODE=0 : Negative polarity horizontal sync input MODE=1 : Test function
11	VSYNC	I	Negative polarity vertical sync input
12	MODE	I	DE / SYNC mode select, normally pulled high. 1: DE mode 0: SYNC mode
13	DITHERB	I	Dithering disable, normally pulled high. 1: disable 0: enable
14	REVEN	I	Data invert enable, normally pulled high. 1: enable 0: disable
15	RESETB	I	Active low reset pin.
16	VDD	I	Power supply voltage.
17	VSS	I	Power supply ground.
18	STV	O	Gate driver start pulse.
19	CKV	O	Gate driver shift clock.
20	OEV	O	Gate driver output disable.
21	POL	O	Source driver polarity select.
22	REV	O	Source driver data reverse control.
23	LD	O	Source driver latch pulse and output enable.
24	BO5	O	Blue data output, bit5 (MSB).
25	BO4	O	Blue data output, bit4.
26	BO3	O	Blue data output, bit3.
27	BO2	O	Blue data output, bit2.
28	BO1	O	Blue data output, bit1.
29	BO0	O	Blue data output, bit0 (LSB).
30	GO5	O	Green data output, bit5 (MSB).
31	GO4	O	Green data output, bit4.
32	GO3	O	Green data output, bit3.
33	GO2	O	Green data output, bit2.
34	GO1	O	Green data output, bit1.
35	GO0	O	Green data output, bit0 (LSB).
36	RO5	O	Red data output, bit5 (MSB).
37	RO4	O	Red data output, bit4.
38	RO3	O	Red data output, bit3.

Pin no.	Symbol	I/O	Description
39	RO2	O	Red data output, bit2.
40	RO1	O	Red data output, bit1.
41	RO0	O	Red data output, bit0 (LSB).
42	HCLK	O	Source driver shift clock.
43	DIO	O	Source driver start pulse.
44	VDD	I	Power supply voltage.
45	VSS	I	Power supply ground..
46	DCLK	I	Clock signal; latch data at falling edge.
47	RI0	I	Red data input, bit0(LSB)(default pull-down).
48	RI1	I	Red data input, bit1(default pull-down).
49	RI2	I	Red data input, bit2.
50	RI3	I	Red data input, bit3.
51	RI4	I	Red data input, bit4.
52	RI5	I	Red data input, bit5.
53	RI6	I	Red data input, bit6.
54	RI7	I	Red data input, bit7(MSB).
55	GI0	I	Green data input, bit0(LSB)(default pull-down).
56	GI1	I	Green data input, bit1(default pull-down).
57	GI2	I	Green data input, bit2.
58	GI3	I	Green data input, bit3.
59	GI4	I	Green data input, bit4.
60	GI5	I	Green data input, bit5.
61	GI6	I	Green data input, bit6.
62	GI7	I	Green data input, bit7(MSB).
63	AP/	O	OP amp bias current ON/OFF control input AP="H", OP amp is on normal operation AP="L", OP amp is on standby mode
	VDD(3)	I	Power supply voltage
64	DUAL/	I	DUAL="0", latch data on the rising edge of HCLK. DUAL="1", latch data on rising and falling edge of HCLK.
	VSS(4)	I	Power supply ground

Note:(1) When Sync mode, The DE pin is TEST pin, and it should be connected VSS.
(2) When DE mode, The HSYNC pin is TEST pin, it should be connected VSS.
(3) In HX8819AFAG the AP pin is the VDD pin.
(4) In HX8819AFAG the DUAL pin is the VSS pin.

6. DC Characteristics

HX8819AFAG/ HX8819AFBG/HX8819AFCG

6.1 Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Power supply	V_{DD}	2.5 to 3.6	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 85	ºC

6.2 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply	V_{DD}	2.7	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating temperature	T_{OPR}	-30	-	85	ºC

6.3 Electrical Characteristics for 3.3V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA
Tri-state leakage current	I_{OZ}	-	-10	-	10	μA
Logic input low voltage	V_{IL} (1)	CMOS	-	-	$0.3V_{DD}$	V
Logic input high voltage	V_{IH} (1)	CMOS	$0.7V_{DD}$	-	-	V
Output low voltage	V_{OL} (2)	I_{OL}=4mA	-	-	$0.2V_{DD}$	V
Output high voltage	V_{OH} (2)	I_{OH}=-4mA	$0.8V_{DD}$	-	-	V
Operating current	I_{VDD}	V_{DD}=3.3V	-	74 (3)	94 (4)	mA
			-	77 (5)	101 (6)	
			-	66 (7)	105 (8)	
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{DD}	85	126	180	kΩ

Note: (1)HS, VS, DE, DCLK, RI0~RI7, GI0~GI7, BI0~BI7.
(2)STV, CKV, POL, REV, LD, DIO, HCLK, RO0~RO5, GO0~GO5, BO0~BO5.
(3)HX8819AFAG, f_{clk}=30MHz, pixel on-off pattern
(4)HX8819AFAG, f_{clk}=40MHz, pixel on-off pattern
(5)HX8819AFBG, f_{clk}=30MHz, pixel on-off pattern
(6)HX8819AFBG, f_{clk}=40MHz, pixel on-off pattern
(7)HX8819AFCG, f_{clk}=25MHz, pixel on-off pattern
(8)HX8819AFCG, f_{clk}=40MHz, pixel on-off pattern

7. AC Characteristics

- **HX8819AFAG/ HX8819AFBG**

7.1 SYNC mode input signal characteristics

RESOLUTION :(800x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Clock Period	t_{CLK}	25.0	30.0	50.0	ns
Clock Frequency	f_{CLK}	20	33.3	40	MHz
Clock Low Level Width	t_{WCL}	8	-	-	ns
Clock High Level Width	t_{WCH}	8	-	-	ns
Clock Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
HSYNC Period	t_{HP}	888	928	1054	t_{CLK}
HYNC Pulse Width(1)	t_{HW}	1	48	87	t_{CLK}
HYNC Back Porch(1)	t_{HBP}	1	40	87	t_{CLK}
HYNC Width+Back Porch(1)	$t_{HW} + t_{HBP}$	88	88	88	t_{CLK}
Horizontal Vaild Data Width	t_{HV}	800	800	800	t_{CLK}
HYNC Front Porch	t_{HFP}	0	40	166	t_{CLK}
VSYNC Period	t_{VP}	512	525	1056	t_{HP}
VYNC Pulse Width(2)	t_{VW}	1	3	31	t_{HP}
VSYNC Back Porch(2)	t_{VW}	1	29	31	t_{HP}
VYNC Width + Back Porch(2)	$t_{VW} + t_{VW}$	32	32	32	t_{HP}
Vertical Valid Data Width	t_W	480	480	480	t_{HP}
VSYNC Front Porch	t_{VFP}	0	13	544	t_{HP}
Data Setup Time	t_{DS}	5	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns

Note: (1) (HYNC Pulse Width+ HYNC Back Porch) must be 88 t_{CLK}.
(2) (VYNC Pulse Width+ VYNC Back Porch) must be 32 t_{HP}.

7.2 SYNC mode output signal characteristics

RESOLUTION :(800x480)

t11	t12	t13	t14	t15	t16	t17	t18	t19	t20	unit
88.5	446.5	899.5	845.5	911.5	898.5	902.5	927.5	888.5	94.5	t_{CLK}

Note: Refer to figure 8. 5 Output signal timing waveform (Sync mode)

7.3 DE mode input signal characteristics

RESOLUTION :(800x480)

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Period	t_{CLK}	25.0	37.0	50.0	ns
	Frequency	f_{CLK}	20.0	27.0	40.0	MHz
	Low Level Width	t_{WCL}	8	-	-	ns
	High Level Width	t_{WCH}	8	-	-	ns
	Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
	Duty(1)	-	0.45	0.50	0.55	-
DE (Data Enable)	Setup Time	t_{DES}	5	-	-	ns
	Hold Time	t_{DEH}	10	-	-	ns
	Rise, Fall Time	t_{DEr}, t_{DEf}	-	-	16	ns
	Horizontal Period	t_{HP}	832	900	1054	t_{CLK}
	Horizontal Valid	t_{HV}	800	800	800	t_{CLK}
	Horizontal Blank	t_{HBK}	32	100	254	t_{CLK}
	Vertical Period	t_{VP}	481	513	1023	t_{HP}
	Vertical Valid	t_W	480	480	480	t_{HP}
	Vertical Blank	t_{VBK}	1	33	543	t_{HP}
Data	Setup Time	t_{DS}	5	-	-	ns
	Hold Time	t_{DH}	10	-	-	ns
	Rise, Fall Time	t_{Dr},t_{Df}	-	-	3	ns

Note: (1) t_{CLKL}/ t_{CLK}.

7.4 DE mode output signal characteristics

RESOLUTION :(800x480)

t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	unit
8.5	358.5	11.5	757.5	23.5	10.5	14.5	39.5	894.5	6.5	t_{CLK}

Note: Refer to figure 8. 6 Output signal timing waveform (DE mode)

- **HX8819AFCG**

7.5 SYNC mode input signal characteristics

RESOLUTION :(640x480)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
Clock Period	t_{CLK}	25.0	40.0	-	ns
Clock Frequency	f_{CLK}	-	25	40	MHz
Clock Low Level Width	t_{WCL}	8	-	-	ns
Clock High Level Width	t_{WCH}	8	-	-	ns
Clock Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
HSYNC Period	t_{HP}	784	800	894	t_{CLK}
HYNC Pulse Width(1)	t_{HW}	1	96	143	t_{CLK}
HYNC Back Porch(1)	t_{HBP}	1	48	143	t_{CLK}
HYNC Width+Back Porch(1)	t_{HW} + t_{HBP}	144	144	144	t_{CLK}
Horizontal Vaild Data Width	t_{HV}	640	640	640	t_{CLK}
HYNC Front Porch	t_{HFP}	0	16	110	t_{CLK}
VSYNC Period	t_{VP}	515	525	1059	t_{HP}
VYNC Pulse Width(2)	t_{VW}	1	2	34	t_{HP}
VSYNC Back Porch(2)	t_{VBP}	1	33	34	t_{HP}
VSYNC Width + Back Porch(2)	t_{VW} + t_{VBP}	35	35	35	
Vertical Valid data Width	t_{W}	480	480	480	t_{HP}
VSYNC Front Porch	t_{VFP}	0	10	544	t_{HP}
Data Setup Time	t_{DS}	5	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns

Note: (1) (HYNC Pulse Width+ HYNC Back Porch) must be 144 t_{CLK}.
(2) (VYNC Pulse Width+ VYNC Back Porch) must be 35 t_{HP}.

7.6 SYNC mode output signal characteristics

RESOLUTION :(640x480)

t11	t12	t13	t14	t15	t16	t17	t18	t19	t20	unit
144.5	392.5	795.5	741.5	807.5	794.5	798.5	823.5	784.5	150.5	t_{CLK}

Note: Refer to figure 8. 5 Output signal timing waveform (Sync mode)

7.7 DE mode input signal characteristics

RESOLUTION :(640x480)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK	Period	t_{CLK}	25.0	40.0	-	ns
	Frequency	f_{CLK}	-	25	40	MHz
	Low Level Width	t_{WCL}	8	-	-	ns
	High Level Width	t_{WCH}	8	-	-	ns
	Rise, Fall Time	t_{CLKr}, t_{CLKf}	-	-	3	ns
	Duty(1)	-	0.45	0.50	0.55	-
DE (Data Enable)	Setup Time	t_{DES}	5	-	-	ns
	Hold Time	t_{DEH}	10	-	-	ns
	Rise, Fall Time	t_{DEr}, t_{DEf}	-	-	16	ns
	Horizontal Period	t_{HP}	672	800	894	t_{CLK}
	Horizontal Valid	t_{HV}	640	640	640	t_{CLK}
	Horizontal Blank	t_{HBK}	32	160	254	t_{CLK}
	Vertical Period	t_{VP}	481	525	1023	t_{HP}
	Vertical Valid	t_W	480	480	480	t_{HP}
	Vertical Blank	t_{VBK}	1	45	543	t_{HP}
Data	Setup Time	t_{DS}	5	-	-	ns
	Hold Time	t_{DH}	10	-	-	ns
	Rise, Fall Time	t_{Dr},t_{Df}	-	-	3	ns

Note: (1) t_{CLKL}/ t_{CLK}.

7.8 DE mode output signal characteristics

RESOLUTION :(640x480)

t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	unit
8.5	248.5	11.5	597.5	23.5	10.5	14.5	39.5	790.5	6.5	t_{CLK}

Note: Refer to figure 8. 6 Output signal timing waveform (DE mode)

8. Waveform

- **HX8819AFAG/ HX8819AFBG/HX8819AFCG**

8.1 Input Signal Timing

8.1.1 Sync. mode input timing

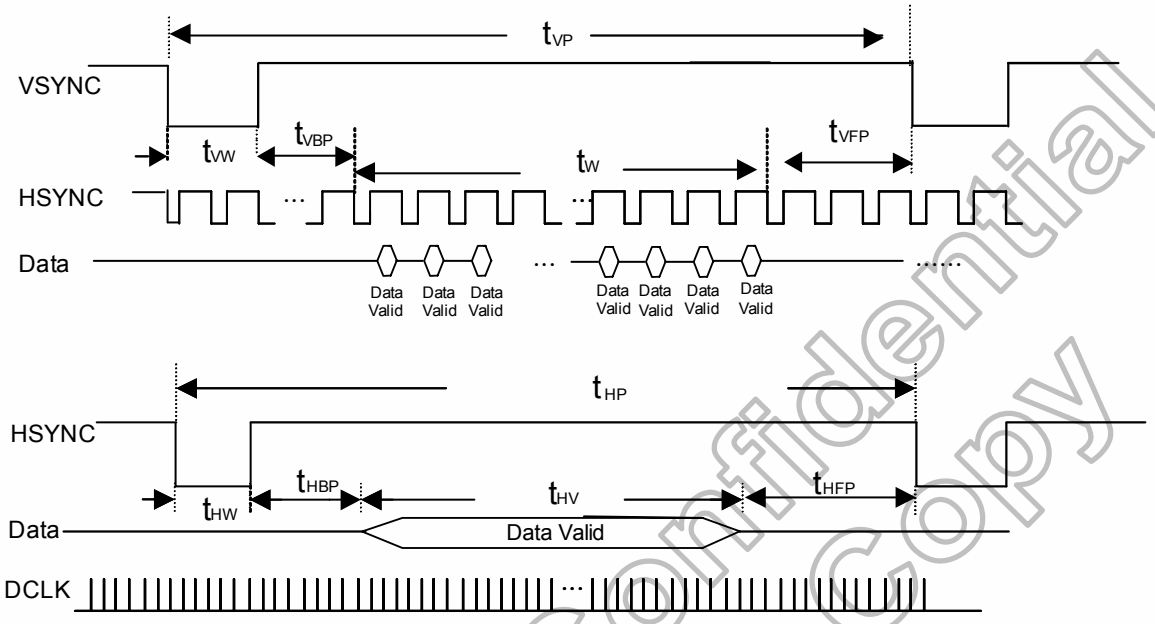


Figure 8. 1 Sync. mode input timing

8.1.2 DE. mode input timing

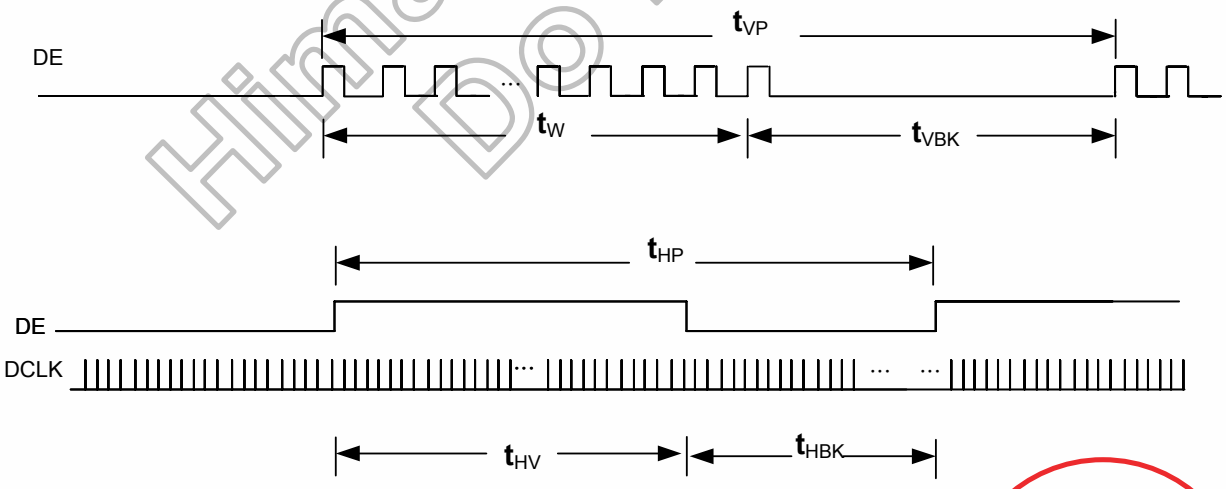


Figure 8. 2 DE mode input timing

8.1.3 Input horizontal timing (Sync. mode && De mode)

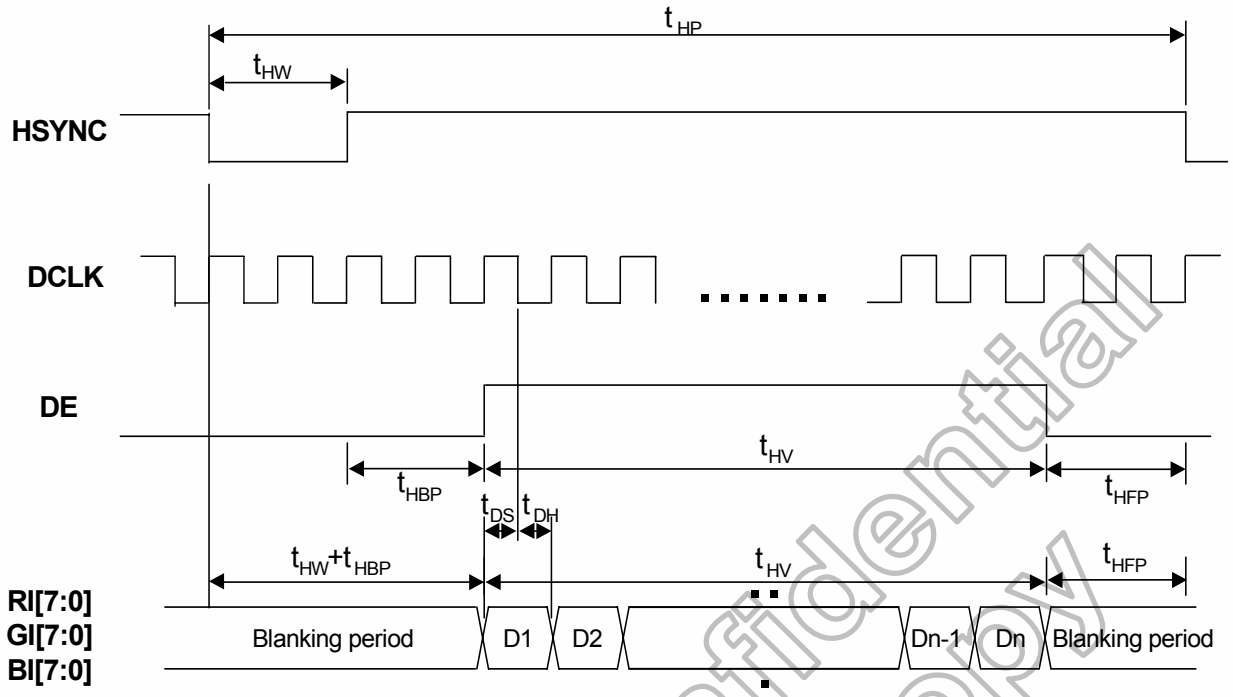


Figure 8. 3 Input horizontal timing

8.2 DE and RGB input data timing waveform

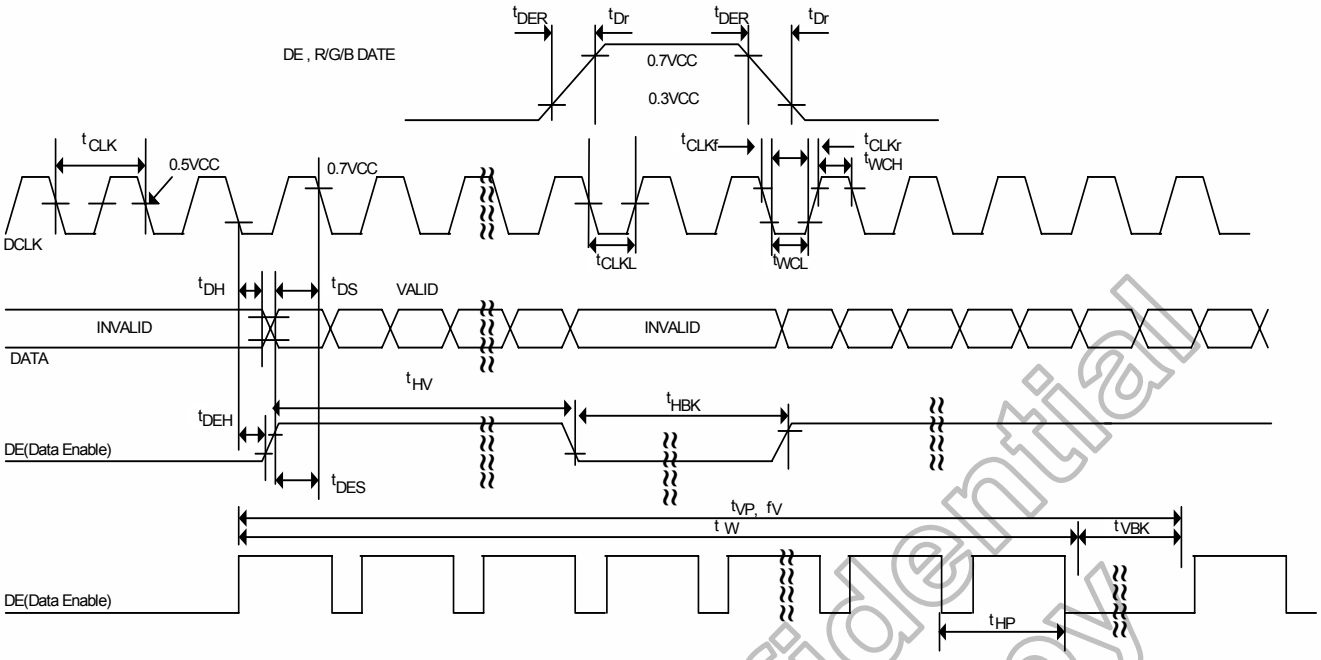


Figure 8. 4 DE and RGB input data timing waveform

8.3 Output signal timing waveform (Sync mode)

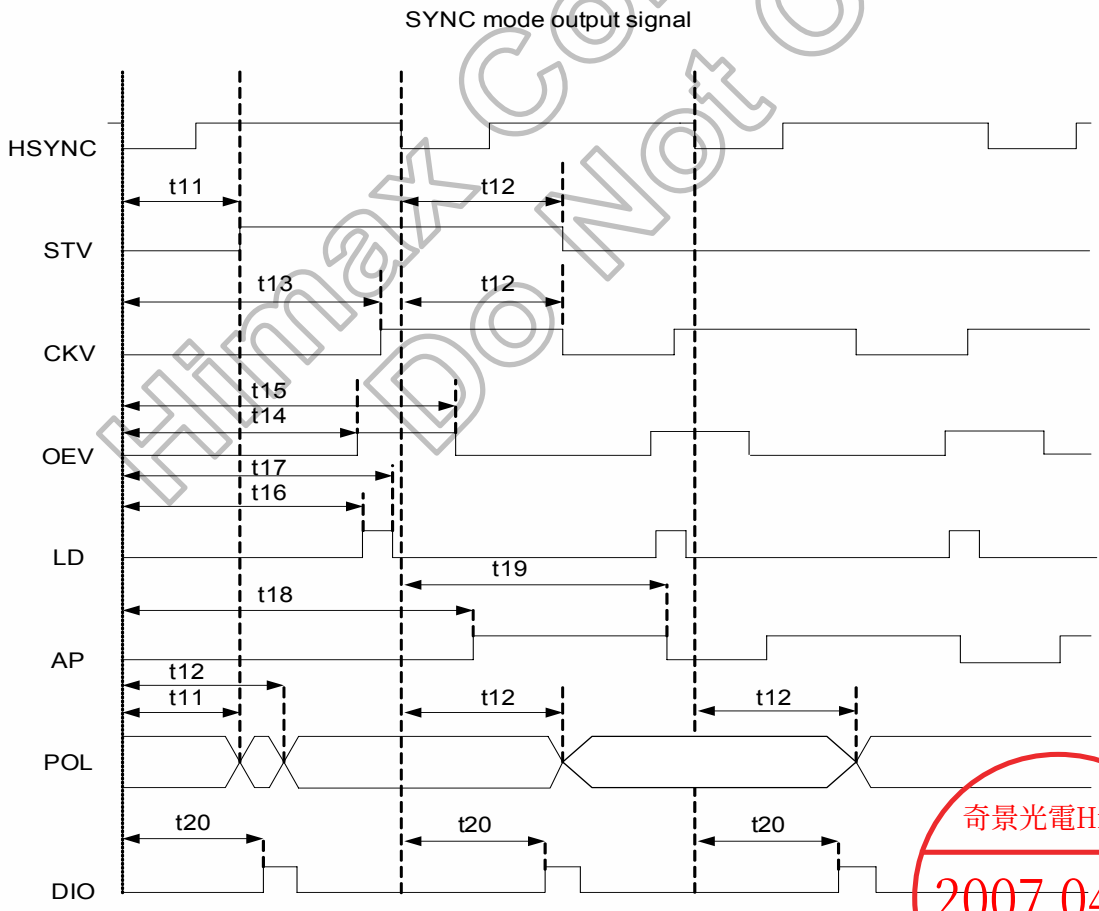


Figure 8. 5 Output signal timing waveform (Sync mode)

8.4 Output signal timing waveform (DE mode)

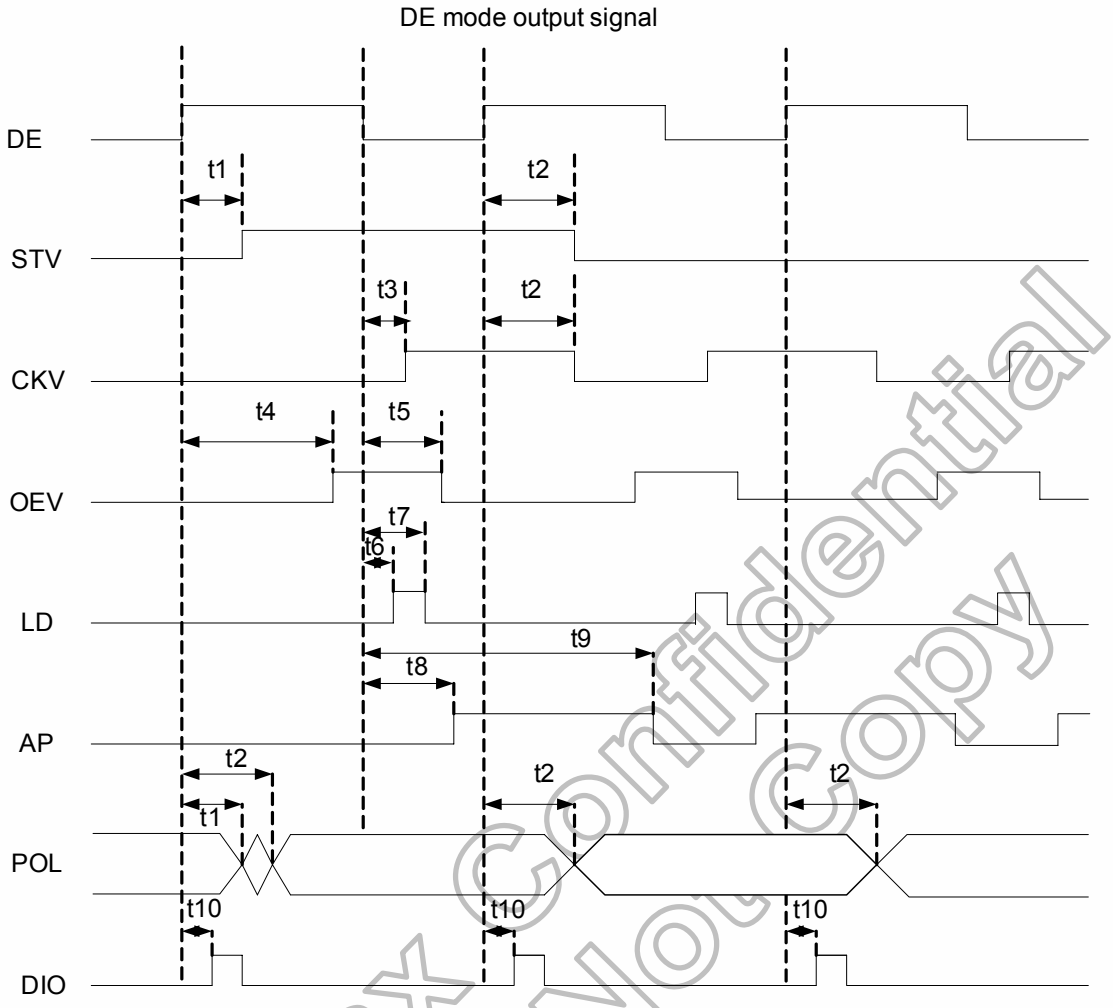


Figure 8. 6 Output signal timing waveform (DE mode)

● **HX8819AFBG/HX8819AFCG**

8.5 Relationship between LD and AP output waveform

AP=" H", source drive internal OP amp is on normal operation. In the other case, AP="L", OP amp is on standby mode for power saving.

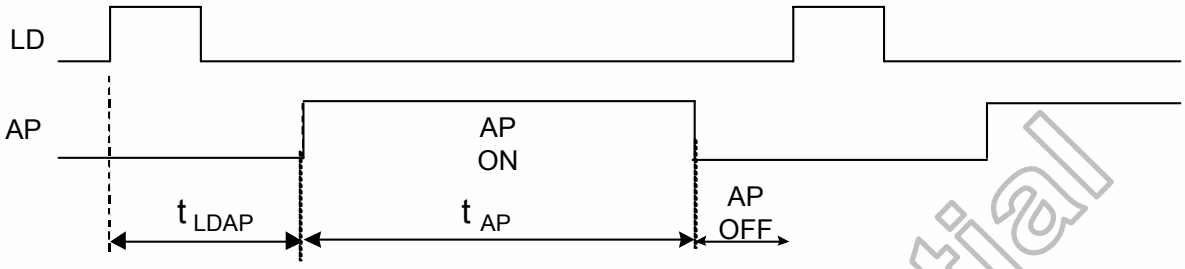


Figure 8. 7 Relationship between LD and AP output waveform

Resolution	Mode	t_{LDAP}	t_{AP}	unit
800x480	Sync mode	29 (t_{18}-t_{16})	889	t_{CLK}
	De mode	29 (t_8-t_6)	855	t_{CLK}
640x480	Sync mode	29 (t_{18}-t_{16})	761	t_{CLK}
	De mode	29 (t_8-t_6)	751	t_{CLK}

8.6 Dual clock function output waveform

<< DUAL = ”0”>>

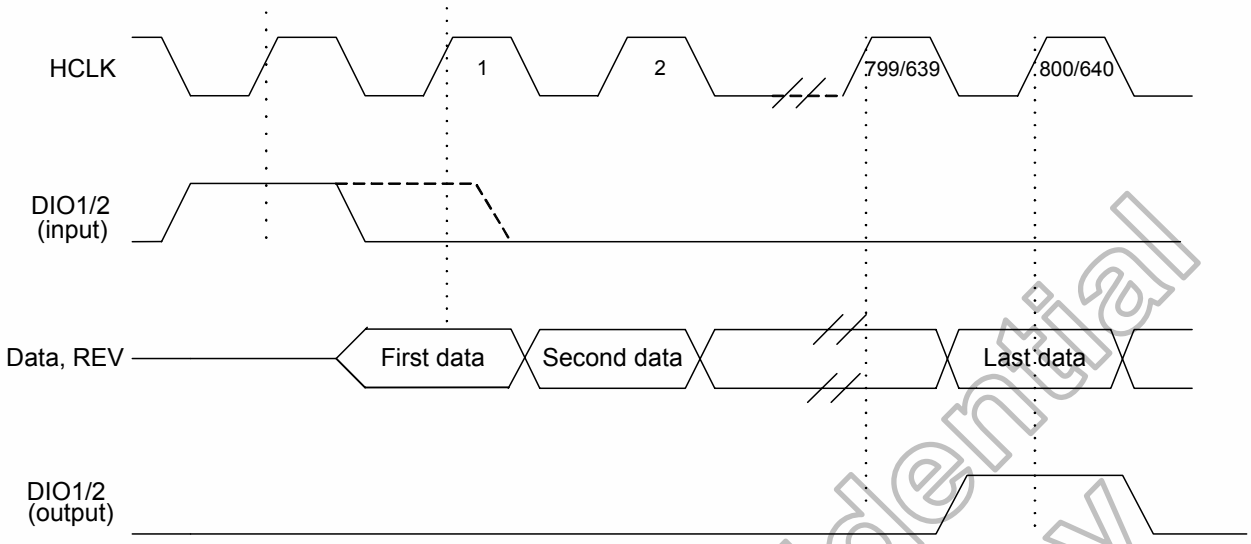


Figure 8. 8 Dual clock function output waveform (DUAL = ”0”)

<< DUAL = ”1” >>

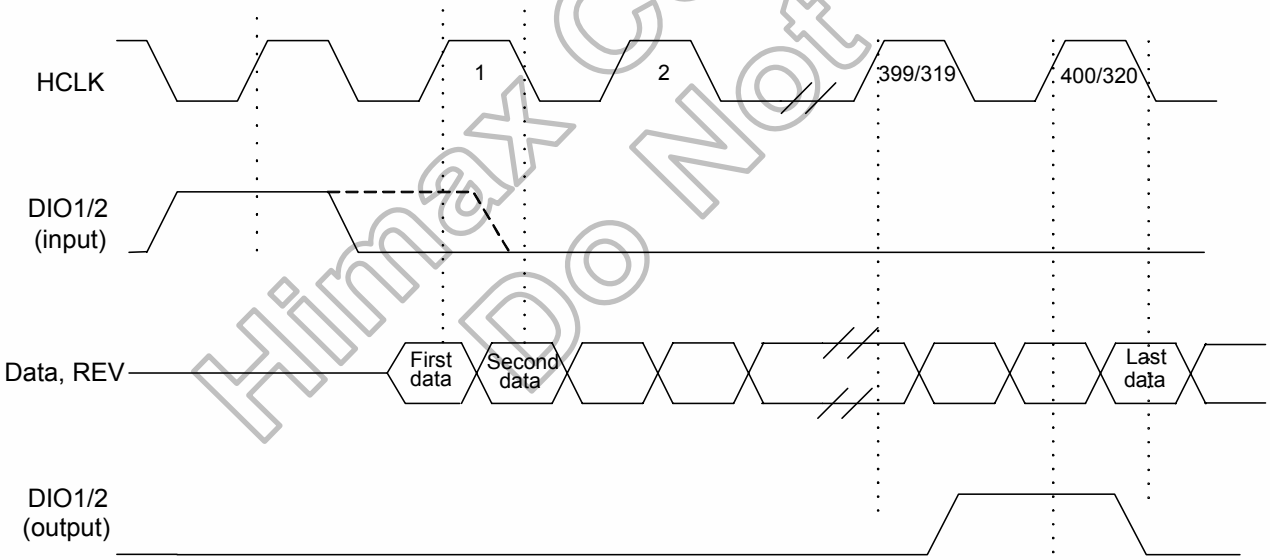
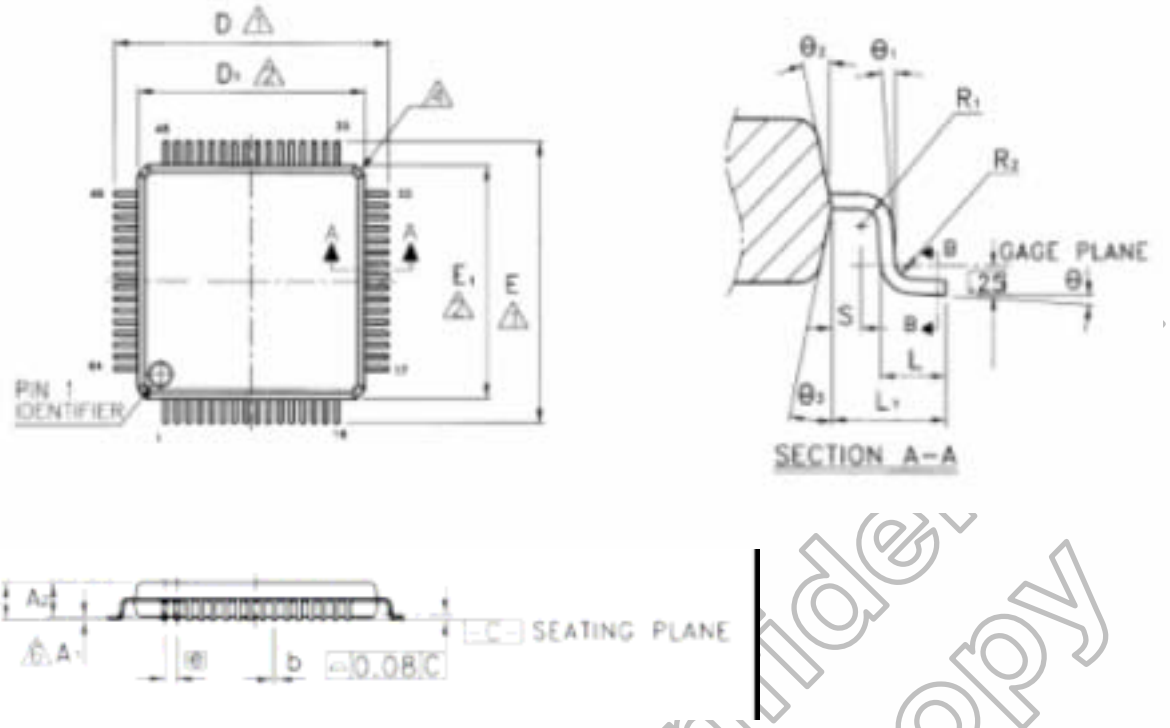


Figure 8. 9 Dual clock function output waveform (DUAL = ”1”)

9. Package Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	NOM	Max	Min	NOM	Max
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	---	0.20	0.004	---	0.008
c1	0.09	---	0.16	0.004	---	0.006
D	12.00BSC			0.472BSC		
D1	10.00BSC			0.394BSC		
E	12.00BSC			0.472BSC		
E1	10.00BSC			0.394BSC		
θ	0.50BSC			0.020BSC		
L	0.45	0.80	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
R1	0.08	---	---	0.003	---	---
R2	0.08	---	0.20	0.003	---	0.008
S	0.20	---	---	0.008	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	---	---	0°	---	---
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

10. Ordering Information

Part NO.	Package
HX8819AFAG	64pin TQFP
HX8819AFBG	64pin TQFP
HX8819AFCG	64pin TQFP
HX8819AFBG-LT	64pin TQFP LT :mean low temperature

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2004/12/30	New setup
02	2005/05/30	1. Modify 7 AC Characteristics 2. Modify 8.3 and 8.4 3. Add 8.5 section Table 4. Modify 8.6 figure 5. Modify section 5,Note 2
	2005/07/22	1. Modify 7.2, 7.4, 7.6, and 7.8 output signal characteristics
	2005/08/17	1. Adding operating current in 6.3 Electrical Characteristics for 3.3V
	2005/08/23	1. Modify feature 1st and 6th point 2. Adding note during section 7.1 to 7.8 3. Modify figure 8.8 and 8.9
03	2006/03/29	1. Modify HX8819AFA/AFB/AFC to HX8819AFAG/AFBG/AFCG
	2006/07/12	1. Modify output pin in block diagram. 2. Modify 6.3 Electrical Characteristics, Note(1)(2)
04	2006/09/12	1. Modify DUAL pin description 2. Modify figure 8.8 and 8.9 3. Adding HX8819AFBG-LT in 10. ordering information and LT :mean low temperature 4. Modify 6.2 operating temperature min value